

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

IKEA SUPPLY AG,
Petitioner,

v.

EVERLIGHT ELECTRONICS CO., LTD.,
Patent Owner.

IPR2024-00988
Patent 7,554,126 B2

Before NABEEL U. KHAN, ARTHUR M. PESLAK, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

PESLAK, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

IKEA Supply AG (“Petitioner”) filed a Petition pursuant to 35 U.S.C. §§ 311–319 requesting an *inter partes* review of claims 1, 2, and 4–13 (“the challenged claims”) of U.S. Patent No. 7,554,126 B2 (“the ’126 patent,” Ex. 1001). Paper 2. Petitioner filed a Declaration of Dr. Michael S. Lebbly in support of the Petition. Ex. 1003. Everlight Electronics Co., Ltd. (“Patent Owner”) did not file a Preliminary Response.

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314(a). *See* 37 C.F.R. § 42.4(a) (2024) (“The Board institutes the trial on behalf of the Director.”). Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

Pursuant to 35 U.S.C. § 314, after consideration of the Petition and the evidence cited therein, and for the reasons stated below, we do not institute an *inter partes* review of the challenged claims of the ’126 patent.

A. Related Matters

The parties identify the following proceedings as related matters: *Everlight Electronics Co., Ltd. v. IKEA US Retail LLC, et al.*, 2:23-cv-00126-JRG (E.D. Tex.); *Everlight Electronics Co., Ltd. v. IKEA US Retail LLC, et al.*, 6:23-cv-00481 (W.D. Tex.) (“IKEA-Everlight Litigation”);

Everlight Electronics Co., Ltd. v. Walmart Inc., 6:23-cv-00439¹ (W.D. Tex.) (“Walmart-Everlight Litigation”). Pet. 2; Paper 5, 1.

In addition to the ’126 patent, Petitioner identifies U.S. Patent No. 9,640,733 (“the ’733 patent”), and U.S. Patent No. 9,905,742 (“the ’742 patent”) as being asserted by Patent Owner in the IKEA-Everlight Litigation. Pet. 2. Petitioner states that it has challenged the ’733 patent in IPR2024-00972, and the ’742 patent in IPR2024-00987. *Id.* Petitioner also identifies a foreign counterpart to the ’733 patent being asserted by Patent Owner and the nullity proceedings filed against the foreign counterpart in Germany. *Id.* at 2–3.

B. Real Parties in Interest

Petitioner identifies IKEA Supply AG (“ISAG”), IKEA US Retail LLC, and IKEA North America Services, LLC as real parties-in-interest. Pet. 1. Petitioner represents that ISAG is a subsidiary of Inter IKEA Holding BV (“Inter IKEA”), and that IKEA US Retail LLC and IKEA North America Services, LLC are “currently named as Defendants in the district court proceeding identified in [the related matters] and related through contracts and/or related company’s contracts by franchise agreements and/or indemnification agreements with Inter IKEA and/or ISAG.” Pet. 1.

Petitioner also states that

OSRAM Opto Semiconductors GmbH, of Regensburg, Germany, Samsung Electronics Co., Ltd., of Suwon-si, South Korea, Seoul Semiconductor Co., Ltd, of Ansan-si, South Korea, Philips Lumileds Lighting LLC, of San Jose, California, Bridgelux, Inc. of Fremont, California, Shenzhen Smalite Semiconductor Co.,

¹ Patent Owner mis-identifies the case number for *Everlight Electronics Co., Ltd. v. Walmart Inc.* in the Western District of Texas as “6:23-cv-00481.” Paper 5, 1.

Ltd., of Shenzhen, China, and/or Intematix, Inc., of Fremont, California, may be real-parties-in-interest insofar as they supply components to ISAG that Patent Owner has accused of infringement and have certain contractual and/or indemnification obligations to ISAG in relation to those accused products.

Id. at 1–2.

Patent Owner identifies itself and no others as a real party-in-interest.

Paper 5, 1.

C. The '126 Patent

The '126 patent is titled “Semiconductor Light-Emitting Element, Manufacturing Method and Mounting Method of the Same and Light-Emitting Device.” Ex. 1001, code (54). The '126 patent issued on June 30, 2009, from Application No. 11/662,547, which was filed on September 22, 2005 as PCT International Application No. PCT/JP2005/017467. *Id.* at codes (45), (21), (22), (86).

The '126 patent relates to “a technique in which a number of bare chips of semiconductor light-emitting elements are mounted on a circuit board, typically represented by a light emitting diode (hereinafter, referred to as ‘LED’), to manufacture illuminating and display devices or the like.” Ex. 1001, 1:16–20. As background, the '126 patent describes a conventional structure of bare chips for the LED, which the '126 patent refers to as an “LED chip.” *Id.* at 1:21–28.

Figures 16 and 17 of the '126 patent are reproduced below:

Fig. 16

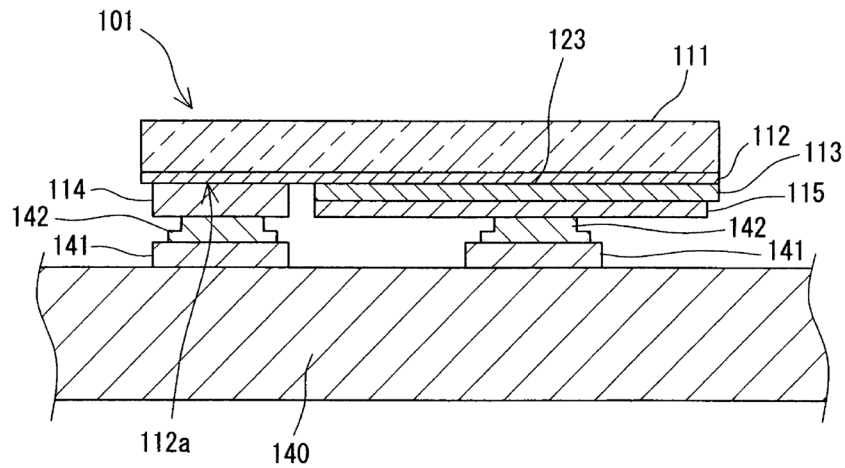


Fig.17

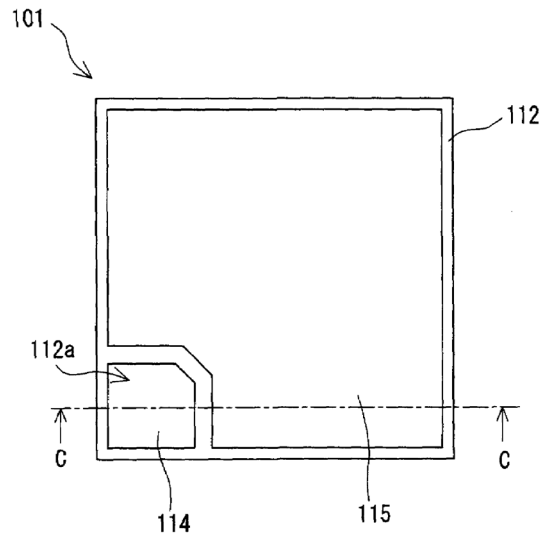


Figure 17 shows a bottom view of the conventional LED chip, and Figure 16 shows a cross-sectional view of a cross section of the conventional LED chip taken along line C-C of Figure 17. Ex. 1001, 1:26–31. The '126 patent describes that the LED chip 101 has:

a light-transmitting substrate 111 (hereinafter, referred to as “element substrate”), an n-type semiconductor layer 112 formed on the element substrate 111 so as to cover the element substrate 111, a p-type semiconductor layer 113 formed so as to cover an

area on the n-type semiconductor layer 111*a* from which an area 112*a* for an n-electrode (see FIG. 17) on the corners of the n-type semiconductor layer 112 is excluded, an n-electrode 114 formed on the area 112*a* for the n-electrode on the n-type semiconductor layer 112, and a p-electrode 115 formed on the p-type semiconductor layer 113.

Id. at 1:31–42. The '126 patent further describes that “[t]he LED chip 101 is electrically connected to a circuit board 140 by respectively joining the n-electrode 114 and the p-electrode 115 to a plurality of bumps 142 formed on the electrode 141 on the circuit board 140 by utilizing ultrasonic waves,” and “is allowed to emit light when an electric current flows through a pn junction 123 between the n-type semiconductor layer 112 and the p-type semiconductor layer 113.” *Id.* at 1:43–51.

The '126 patent notes that in the conventional mounting technique, “when the size of the LED chip exceeds 0.5 mm in each side of square, it becomes necessary to form a number of bumps on the p-electrode in order to allow the LED chip to uniformly emit light,” but forming “a number of bumps on the p-electrode is not desirable because of a higher possibility of a reduction in the yield of junctions and of short-circuiting and connection failure, due to positional deviations at the time of mounting.” Ex. 1001, 2:3–11. The '126 patent also describes that

in the case of the conventional LED chip 101, since the light emission is executed through the pn junction 123 as described above, the junction face between the n-type semiconductor layer 112 and the n-electrode 114 needs to be made as small as possible and the junction face between the n-type semiconductor layer 112 and the p-type semiconductor layer 113, which corresponds to the light-emitting area, needs to be made larger, in order to enlarge the light-emitting area. . . .

Therefore, upon mounting the conventional LED chip 101, since the area on the[]n-electrode 114 is small, it is difficult to use a

Id. at 2:16–40. According to the ’126 patent, “its main objective is to provide a semiconductor light-emitting element which can be mounted on a circuit board by using a conductive bonding material, typically represented by solder, at low costs.” *Id.* at 2:42–45.

Fig.1

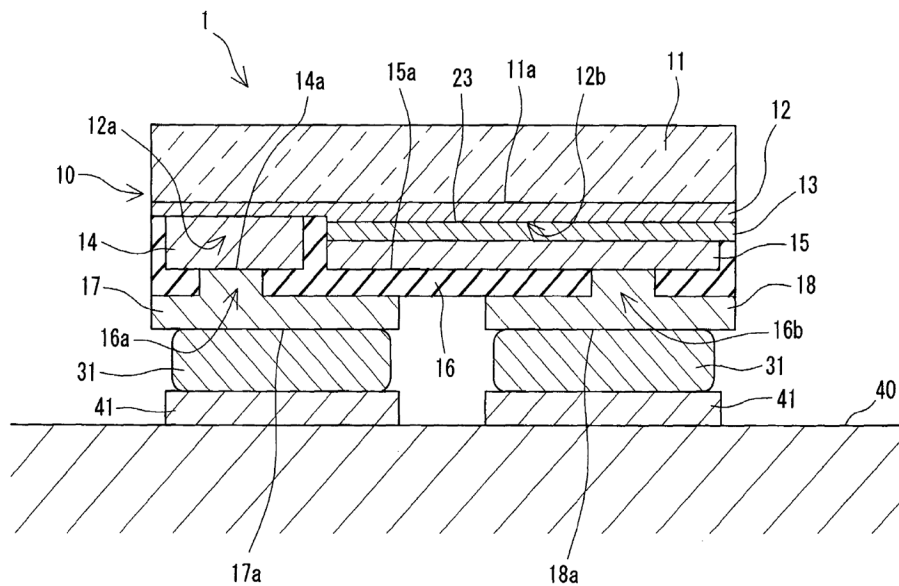


Fig.2

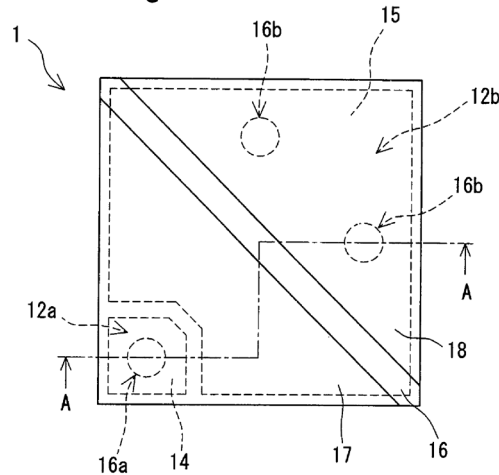


Figure 1 shows a cross-sectional view of a light-emitting device in accordance with a first embodiment of the '126 patent disclosure, in which an LED chip 1 is mounted on circuit board 40 via solder 31, and Figure 2 is a bottom view of LED chip 1. Ex. 1001, 6:61–67. The '126 patent describes that LED chip 1 is provided with:

an element substrate 11, an n-type semiconductor layer 12 formed on the element substrate 11 so as to cover the element substrate 11, a p-type semiconductor layer 13 formed on an area 12b for the p-type semiconductor layer of the n-type semiconductor layer 12 from which a corner area 12a for an n-electrode is excluded, a first n-electrode 14 formed on the area 12a for the n-electrode and a first p-electrode 15 formed on the p-type semiconductor layer 13[; and]

... a first insulating layer 16 formed so as to cover the first n-electrode 14 and the first p-electrode 15, and is formed so as to insulate the first n-electrode 14 and the first p-electrode from each other, a second n-electrode 17 that is formed on the first insulating layer 16 (that is, the lowest side of the LED chip 1 in FIG. 1), and penetrates the first insulating layer 14 to be electrically connected to the first n-electrode 14 and a second p-electrode 18 that is electrically connected to the first p-electrode 15.

Id. at 7:7–24.

The '126 patent describes that “[e]ach of the second n-electrode 17 and the second p-electrode 18 is formed on the first insulating layer 16 through sputtering, plating or the like, by a thin film having a thickness, for example, in a range from 0.1 μm to 0.3 μm ,” and “the second n-electrode 17 and the second p-electrode 18 are electrically connected and fixed onto the electrode 41 on the circuit board 40 through solder 31 that is one example of the conductive bonding material layer.” *Id.* at 7:65–8:1, 8:30–34. According to the '126 patent, “a current is applied between the second n-electrode 17 and the second p-electrode 18 through the circuit board 40 so that light is generated between the n-type semiconductor layer 12 and the p-type semiconductor layer 13” and emitted through the element substrate 11. *Id.* at 8:55–62.

D. Illustrative Claim

Claims 1, 2, 9, and 10 are independent claims. Claim 1 is representative of the claimed subject matter and is reproduced below:

1. A semiconductor light-emitting element comprising:
 - a light-transmitting element substrate;
 - an n-type semiconductor layer formed on the element substrate so as to cover the element substrate;
 - a p-type semiconductor layer formed so as to cover an area on the n-type semiconductor layer from which an area for an n-electrode on the n-type semiconductor layer is excluded, for emitting light in cooperation with the n-type semiconductor layer;
 - a first n-electrode that is a thin film formed on the area for the n-electrode of the n-type semiconductor layer;
 - a first p-electrode that is a thin film formed on the p-type semiconductor layer;
 - a first insulating layer that is formed so as to insulate the first n-electrode and the first p-electrode from each other;

a second n-electrode formed on the first n-electrode and the first insulating layer as a thin film having an area larger than a joined face between the n-type semiconductor and the first n-electrode so that the second n-electrode is electrically connected to the first n-electrode, the second n-electrode being insulated from the first p-electrode by the first insulating layer; and

a second p-electrode formed as a thin film having an area smaller than a joined face between the n-type semiconductor layer and the p-type semiconductor layer, the second p-electrode being electrically connected to the first p-electrode.

Ex. 1001, 13:47–14:7.

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1, 2, and 4–13 would have been unpatentable on the following grounds (Pet. 5–6):

Ground	Claim(s) Challenged	35 U.S.C. § ²	References/Basis
1	1, 2, 5–12	102	Terashima ³
2	1, 5, 6, 9, 12	102	Sugimoto ⁴

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103. Because the ’126 patent issued from an application filed before March 16, 2013 (the effective date of the amendments), the pre-AIA versions of §§ 102 and 103 apply.

³ Japanese Unexamined Patent Application Publication No. JP 2004-103975 A (published April 2, 2004) (Ex. 1004 (Japanese original), Ex. 1010 (certified translation), “Terashima”).

⁴ U.S. Patent Application Publication No. US 2004/0159836 A1 (filed February 19, 2004; published August 19, 2004) (Ex. 1006, “Sugimoto”).

Ground	Claim(s) Challenged	35 U.S.C. § ²	References/Basis
3	1, 2, 5, 7–10	103(a)	Shin ⁵ in view of one or more of Sugimoto, Terashima, Uemura '259, ⁶ Uemura '999, ⁷ and/or Inoue ⁸
4	4	103(a)	Terashima or Ground 3 in view of Shelton ⁹ or Inoue
5	5	103(a)	Terashima in view of Shin, Sugimoto, or Inoue
6	6	103(a)	Terashima, Sugimoto, or Ground 3 in view of Shelton and/or OLSA ¹⁰
7	7	103(a)	Terashima, Sugimoto, or Ground 3 in view of Shelton and/or OLSA
8	8	103(a)	Terashima, Sugimoto, or Ground 3 in view of Shelton and/or OLSA
9	11	103(a)	Sugimoto or Ground 3 in view of Terashima or OLSA
10	12	103(a)	Ground 3 in view of Terashima, Sugimoto, or OLSA
11	13	103(a)	Terashima, Sugimoto, or Ground 3 in view of Shelton and/or OLSA

⁵ U.S. Patent Application Publication No. US 2004/0256631 A1 (filed November 6, 2003; published December 23, 2004) (Ex. 1005, “Shin”).

⁶ U.S. Patent Application Publication No. US 2003/0160259 A1 (filed February 5, 2003; published August 28, 2003) (Ex. 1007, “Uemura '259”).

⁷ U.S. Patent Application Publication No. US 2004/0149999 A1 (filed June 3, 2002; published August 5, 2004) (Ex. 1008, “Uemura '999”).

⁸ U.S. Patent No. 6,333,522 B1 (issued December 25, 2001) (Ex. 1021, “Inoue”).

⁹ U.S. Patent Application Publication No. US 2005/0194605 A1 (filed March 5, 2004; published September 8, 2005) (Ex. 1011, “Shelton”).

¹⁰ Petitioner refers “the ordinary level of skill in the art” as “OLSA.” Pet. 6.

Ground	Claim(s) Challenged	35 U.S.C. § ²	References/Basis
12	1, 2, 4–13	103(a)	Grounds 1, 4–8, and 11 regarding Terashima in view of Sugimoto, Uemura '259, Uemura '999 and/or OLSA

II. ANALYSIS

A. Overview

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

To establish anticipation under 35 U.S.C. § 102, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008); *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). Each element of the challenged claim must be found, either expressly or inherently, in the single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). When evaluating a prior art reference in the context of anticipation, the reference must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). “[A] reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Kennametal, Inc. v. Ingersoll Cutting*

Tool Co., 780 F.3d 1376, 1381 (Fed. Cir. 2015) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations).¹¹ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

The Supreme Court explained in *KSR International Co. v. Teleflex Inc.* that

[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning

¹¹ No evidence of secondary considerations has been presented at this stage of the proceeding.

with some rational underpinning to support the legal conclusion of obviousness.” (alteration in original)).

“Whether an ordinarily skilled artisan would have been motivated to modify the teachings of a reference is a question of fact.” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1327 (Fed. Cir. 2016) (citations omitted).

“[W]here a party argues a skilled artisan would have been motivated to combine references, it must show the artisan ‘would have had a reasonable expectation of success from doing so.’” *Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1360–61 (Fed. Cir. 2017) (quoting *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1068–69 (Fed. Cir. 2012)).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) “in the field of the ’126 patent at the time of the effective filing date would have had: (1) a Bachelor’s degree in electrical engineering, physics, or a comparable field of study, and (2) at least three years of professional experience with semiconductor optoelectronic devices that includes designing/analysis, mounting, manufacturing, and packaging.” Pet. 19 (citing Ex. 1003 ¶ 44). Petitioner further states that “a higher level of education or skill might make up for less experience, and additional experience could make up for a lower education level.” *Id.* (citing Ex. 1003 ¶ 44).

For the purposes of this Decision, we apply Petitioner’s proffered level of skill in the art, with the exception of the phrase “at least” which injects potential ambiguity into the level of skill, because its proffered level

of skill appears consistent with the problems addressed in the '126 patent and the prior art.

C. Claim Construction

We apply the same claim construction standard used by Article III federal courts and the International Trade Commission, both of which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. 37 C.F.R. § 42.100(b). Accordingly, we construe each challenged claim of the '126 patent to generally have “the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *Id.*

If the specification “reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor’s lexicography governs.” *Phillips*, 415 F.3d at 1316 (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). Another exception to the general rule that claims are given their ordinary and customary meaning is “when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Uship Intellectual Props., LLC v. United States*, 714 F.3d 1311, 1313 (Fed. Cir. 2013) (quoting *Thorner v. Sony Comput. Ent. Am., LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)).

Petitioner states that it applies the construction of the term “forming a first insulating layer” set forth in the claim construction order issued in the Walmart-Everlight Litigation. Pet. 34 (citing Ex. 1016, 2–3). Petitioner further asserts that “[g]iven that the prior art is nearly identical to the structures disclosed in the '126 patent, additional constructions do not

appear necessary and plain meaning is applied.” *Id.* at 34–35 (citing *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

We determine that no express construction of any claim term is necessary for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Overview of Petitioner’s Asserted References

1. Terashima (Ex. 1010)

Terashima is titled “Optical Semiconductor Element Manufacturing Method, Optical Semiconductor Element, and Optical Semiconductor Device Equipped with Optical Semiconductor Element.” Ex. 1010, code (54). Terashima relates to:

a manufacturing method of an optical semiconductor element having p-type and n-type semiconductor layers formed on the same side of a substrate, and a pair of connection electrodes consisting of a p-electrode and an n-electrode respectively formed from the same metal material on the p-type and n-type semiconductor layers, and having respective functions of a light-emitting element that converts electricity into light and emits such, and a light-receiving element that receives incident light and converts such into electricity

Id. ¶ 1.

Figure 1(d) of Terashima is reproduced below:

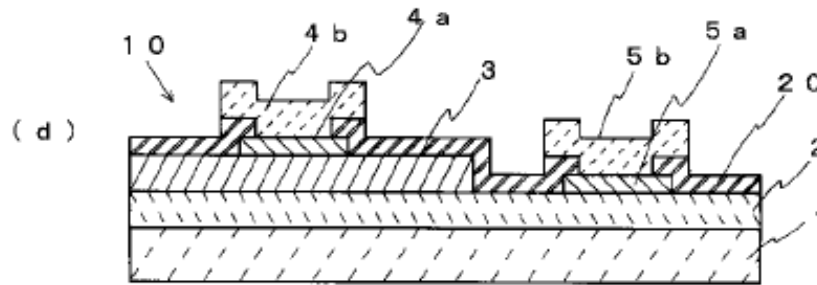


Figure 1(d) shows a cross-sectional view of an optical semiconductor element according to an embodiment of Terashima's invention. Ex. 1010 ¶ 28. According to Terashima, the optical semiconductor element 10 has "an n-type nitride semiconductor layer 2 on a transparent insulating substrate 1, and a p-type nitride semiconductor layer 3 electrically connected to the upper layer thereof," "plating growth films 4a and 5a . . . provided on exposed upper layers of the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3," "a protective film 20 . . . provided by forming an opening in a portion of the plating growth films 4a and 5a, the p-electrode 4b . . . provided on the plating growth film 4a exposed from the opening of the protective film 20, and the n-electrode 5b on the plating growth film 5a," wherein "these electrodes 4b and 5b are connected to respective nitride semiconductor layers 3 and 2." *Id.* ¶¶ 28–29. Terashima explains that "by applying a predetermined voltage across the p-electrode 4b and the n-electrode 5b, electron holes from the p-electrode 4b and electrons from the n-electrode 5b are recombined near the junction interface across the n-type nitride semiconductor layer 2 and the p-type nitride semiconductor layer 3, thereby emitting light." *Id.* ¶ 30.

high-frequency devices.” *Id.* ¶ 2. Sugimoto describes a nitride semiconductor device including “a first electrode for establishing an ohmic contact provided on a semiconductor layer and a second electrode used mainly as [an] extraction electrode in contact with the first electrode,” wherein “[t]he interface between the first electrode and the second electrode has a specific structure to achieve superior adhesion, low interface resistance, and stable operating characteristics.” *Id.* ¶ 52.

Figure 1 of Sugimoto is reproduced below:

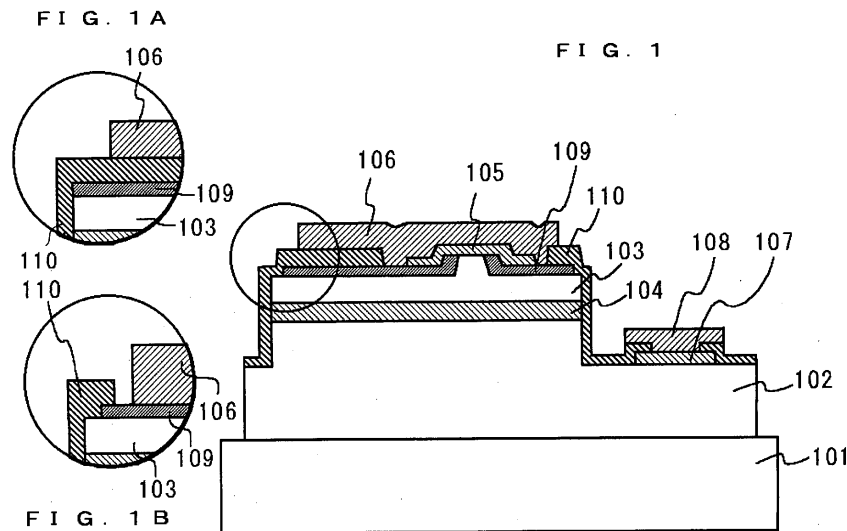


Figure 1 shows a nitride semiconductor device, which is “a semiconductor laser diode (LD) including an n-type nitride semiconductor layer 102, an active layer 104, and a p-type nitride semiconductor layer 103 deposited in that order on a substrate 101.” Ex. 1006 ¶ 72. According to Sugimoto, “[t]he p-type nitride semiconductor layer 103 has a ridge stripe,” which may be “formed by partially etching the p-type nitride semiconductor layer or other processes to function as an effective refractive-index waveguide.” *Id.* Sugimoto also describes: a first insulating layer 109 “extend[ing] from the side surfaces of the ridge stripe to the upper surfaces of the p-type nitride

semiconductor layer 103 continuing from the ridge stripe,” a first p electrode 105 “extend[ing] over the upper surfaces of the ridge and the first insulating layer 109,” a first n electrode 107 “extend[ing] on the upper surface of the n-type nitride semiconductor layer 102,” a second insulating layer 110 “extend[ing] from the upper surface of the first n electrode 107 to the upper surface of the first insulating layer 109,” a second p electrode 106 “in contact with the second insulating layer 110 and first p electrode 105 . . . provided over the p-type nitride semiconductor layer 103,” and a second n electrode 108 “provided on the first n electrode 107.” *Id.* ¶ 73. According to Sugimoto, “the contact area of the first p electrode 105 with the first insulating layer 109 is reduced to prevent the electrode from peeling even if the adhesion to the first insulating layer 109 is low, in comparison with the case where the first electrode is formed from one end to the other across the surface of the semiconductor layer.” *Id.* ¶ 75.

3. *Shin (Ex. 1005)*

Shin is titled “GaN LED for Flip-Chip Bonding and Method of Fabricating the Same.” Ex. 1005, code (54). Shin relates to “a GaN light emitting diode for a flip-chip bonding, which secures a sufficient bonding area while optimizing an electrode arrangement, prevents an electric current from concentrating on a predetermined portion, and has higher brightness and reliability, and a method of fabricating the same.” *Id.* ¶ 2.

Figure 5 of Shin is reproduced below:

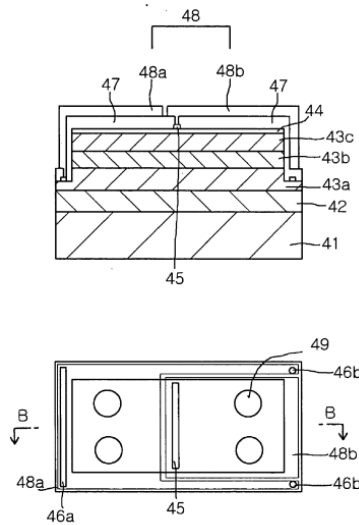


FIG. 5

Figure 5 shows a sectional view and a plan view of a light emitting diode chip, which includes “a sapphire substrate 41, and a light emitting structure 43 including an n-type GaN clad layer 43a, an activation layer 43b, and a p-type GaN clad layer 43c sequentially formed on the sapphire substrate 41.” Ex. 1005 ¶ 60. Shin also describes a plurality of n-electrodes 46 and p-electrodes 45 “respectively formed on the exposed portions of the n-type GaN clad layer 43a and the transparent electrode 44,” a passivation layer 47 “formed on the light emitting structure 43 and the p- and n-electrodes 45, 46 and punched at portions thereof to protect the portions of the p- and n-electrodes 45, 46 and the light emitting structure 43,” and first and second bonding electrodes 48a, 48b “formed on the passivation layer 47 as a way to insulate each other and connect to the p- and n-electrodes 45, 46 through punched portions of the passivation layer 47.” *Id.*

4. Uemura '259 (Ex. 1007)

Uemura '259 is titled “Light Emitting Device.” Ex. 1007, code (54). Uemura '259 relates to a light emitting device including:

a light-emitting element comprising a light emitting layer for emitting a light of a predetermined wavelength and p- and n-type electrodes for applying a predetermined voltage across the light emitting layer, a lead structure including p- and n-leads for mounting the light-emitting element thereon, and a light-transmitting paste containing a phosphor for fixing the light-emitting element to the lead structure.

Id. at code (57).

Uemura '259 describes that “a p-type electrode has a film thickness or a layer composition through which the light emitted from a light emitting layer transmits.” Ex. 1007 ¶ 41. According to Uemura '259, the p-type electrode “is formed by vapor deposition, sputtering, or other well-known methods” and “may have a two-layer or multilayer structure in which layers of different compositions are stacked on each other.” *Id.* ¶¶ 51–52. For example, referring to its Figure 2, Uemura '259 describes a p-electrode 17, which “has a stacked structure of rhodium and gold” and “is formed on the p-type layer 15 by vapor deposition,” wherein the “film thickness of the p-electrode 17 is about 1.5 μm .” *Id.* ¶ 77.

5. *Uemura '999 (Ex. 1008)*

Uemura '999 is titled “LLL Group Nitride Based Semiconductor Luminescent Element.” Ex. 1008, code (54). Uemura '999 relates to “a Group III nitride compound semiconductor light-emitting element having a p-side electrode and an n-side electrode formed on one surface side and preferably used in a flip chip type light-emitting device.” *Id.* ¶ 1. According to Uemura '999,

[t]he Group III nitride compound semiconductor layer can be formed by a known method such as a metal organic chemical vapor deposition method (MOCVD method), a molecular beam epitaxy method (MBE method), a halide vapor phase epitaxy

method (HVPE method), a sputtering method, an ion-plating method, an electron showering method, etc.

Id. ¶ 16.

Uemura '999 describes that “[t]he p-side electrode may be formed as a two-layer or multi-layer structure in which layers different in composition are laminated.” Ex. 1008 ¶ 20. Uemura '999 also describes a p-side electrode film containing Au (gold), which is formed on the surface of the p-side electrode. *Id.* ¶ 22. According to Uemura '999,

[t]he p-side electrode film enhances adhesion of the p-side electrode to an adhesive member of Au . . . used at the time of mounting the light-emitting element on the support to consequently enhance bonding strength between the light-emitting element and the support.

Id.

In addition, Uemura '999 describes that “[t]he n-side electrode may be formed as a two-layer or multi-layer structure,” such as “a two-layer structure of V and Al.” Ex. 1008 ¶ 27. Uemura '999 also describes an n-side electrode film containing Au (gold), which is formed on the surface of the n-side electrode. *Id.* ¶ 29. According to Uemura '999,

the n-side electrode film enhances adhesion (close contact) between the n-side electrode and the Au bump at the time of mounting the light-emitting element on the support by the Au bump to consequently improve bonding strength between the light-emitting element and the support.

Id.

6. Inoue (Ex. 1021)

Inoue is titled “Light-Emitting Element, Semiconductor Light-Emitting Device, and Manufacturing Methods Therefor.” Ex. 1021, code (54). Inoue relates “to a light-emitting element comprising a semiconductor multilayer film formed on an insulating substrate, to a semiconductor light-

emitting device including such a semiconductor light-emitting element, and to manufacturing methods therefor.” *Id.* at 1:8–12.

Figure 2 of Inoue is reproduced below:

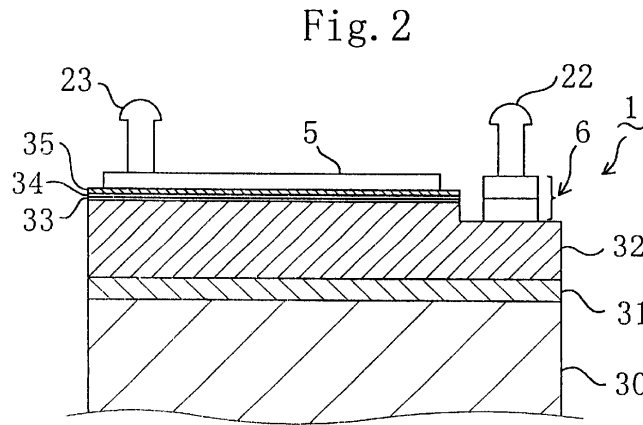


Figure 2 shows a cross-sectional view of a GaN LED element 1. Ex. 1021, 12:20–22. As shown in Figure 2,

the GaN LED element 1 has a double heterostructure comprising a GaN buffer layer 31, an n-type GaN layer 32, an InGaN active layer 33, a p-type AlGaIn layer 34, and a p-type GaN layer 35 which are stacked sequentially in layers on the top face of a sapphire substrate 30.

Id. at 12:22–27. According to Inoue, an n-side electrode 6 is made of a Ti/Au multi-layer film, a p-side electrode 5 is made of Ni, and microbumps 22 and 23 made of Au or an Au alloy are formed on the n-side electrode 6 and on the p-side electrode 5, respectively. *Id.* at 12:31–32, 12:38, 12:43–45.

7. *Shelton (Ex. 1011)*

Shelton is titled “Flip-Chip Light Emitting Diode Device Without Sub-Mount.” Ex. 1011, code (54). Shelton relates to “flip chip light emitting diodes for indicator lights, illumination applications, and the like.” *Id.* ¶ 1.

Figure 2 of Shelton is reproduced below:

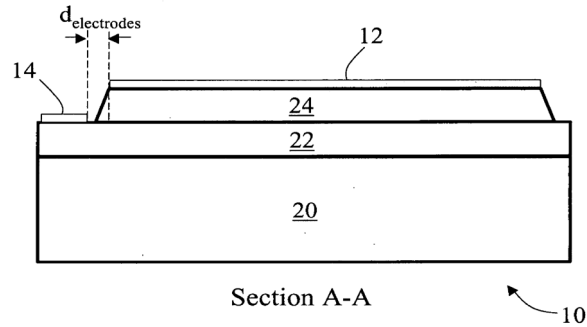


FIG 2

Figure 2 shows a side sectional view of an exemplary flip chip light emitting diode having front-side n-type and p-type electrodes. Ex. 1011 ¶¶ 13–14. According to Shelton, “the exemplary light emitting diode 10 prior to formation of the bonding pads includes a substrate 20, an n-type base layer 22, and one or more device mesas 24.” *Id.* ¶ 30.

Shelton describes a process for “forming bonding pads on a flip chip light emitting diode 10 in a way which adapts fine features including a small minimum spacing $d_{\text{electrodes}}$ between electrodes 12, 14 of the light emitting diode 10 to a larger tolerance of the flip chip bonding process.” Ex. 1011 ¶ 29. According to Shelton, “[t]he spacing $d_{\text{electrodes}}$ between the electrodes 12, 14 is preferably small to reduce resistance to current flow,” and “the device mesas 24 and the n-type electrode 14 are preferably distributed over the lateral area of the light emitting diode 10 to maximize lateral current spreading across the mesa 24.” *Id.* ¶ 35. Shelton notes that

[t]he fine lateral features of the p-type and n-type electrodes 12, 14 and the small minimum spacing $d_{\text{electrodes}}$ therebetween make flip-chip bonding of the light emitting diode 10 directly to a printed circuit board without an interposed sub-mount difficult. *Id.* ¶ 36.

Figure 4 of Shelton is reproduced below:

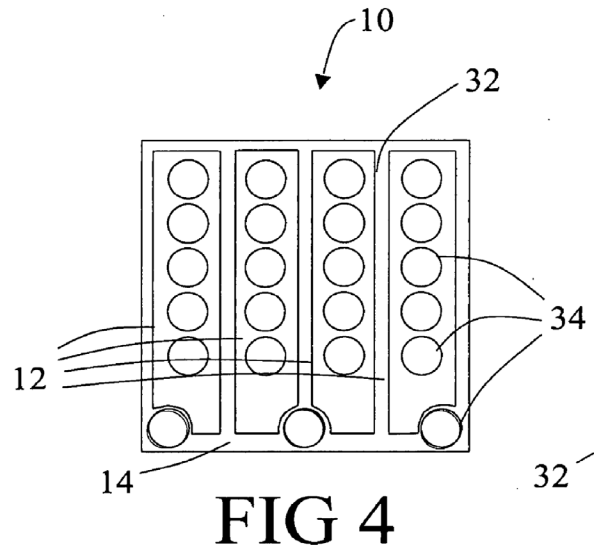


Figure 4 shows “the light emitting diode 10 after the dielectric layer 32 is disposed thereon and the vias 34 are formed, but before the electrically conductive material 36 is disposed.” Ex. 1011 ¶ 38. According to Shelton, this is a part of the bonding pads formation process used “to adapt the fine features of the electrodes 12, 14 to the larger tolerance of the flip chip bonding process.” *Id.* ¶ 37. The bonding pads formation process includes:

depositing a dielectric layer 32 in which vias 34 are formed to provide access to the p-type electrode 12 and the n-type electrode 14, followed by metallization processing that fills the vias 34 with an electrically conductive material 36 and that forms intermediate connecting pads, specifically an intermediate p-type connecting pad 42 and an intermediate n-type connecting pad 44.

Id. According to Shelton, preferably “several vias 34 contacting each of the electrodes 12, 14 are distributed across the lateral area of the light emitting diode 10 to promote current spreading across the light emitting diode 10.” *Id.* ¶ 39.

E. Discretionary Denial of Institution

We start with the proposition that “the PTO is permitted, but never compelled, to institute an IPR proceeding.” *Harmonic Inc. v. Avid Tech.*,

Inc., 815 F.3d 1356, 1367 (Fed. Cir. 2016). In deciding whether to institute a trial, we either institute as to all claims and challenges or as to no claims and deny institution, but we cannot institute on fewer than all claims or challenges in a petition. *See* 37 C.F.R. § 42.108(a); Consolidated Trial Practice Guide (“CTPG”),¹² 64 (PTAB Nov. 2019) (citing *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1359–62 (Fed. Cir. 2018); and *Adidas AG v. Nike, Inc.*, 894 F.3d 1256, 1258 (Fed. Cir. 2018)). We “retain[] discretion to deny institution of the petition as a whole . . . even when the petition includes at least one claim subject to a challenge that otherwise meets the criteria for institution.” CTPG, 64 (citing *Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 (PTAB Jan. 24, 2019) (informative); *Chevron Oronite Co. v. Infineum USA L.P.*, IPR2018-00923, Paper 9 (PTAB Nov. 7, 2018) (informative)).

A petition must identify “with particularity, each claim challenged, the grounds on which the challenges to each claim are based, and the evidence that supports the grounds for challenge to each claim.” 35 U.S.C. § 312(a)(3); *see also* *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’” (quoting 35 U.S.C. § 312(a)(3))). In a case where failure to meet the particularity requirement “results in voluminous and excessive grounds,” the Board can exercise its discretion to deny an entire petition “in the interests of efficient administration of the Office and integrity of the patent system and as a matter of procedural fairness to Patent

¹² Available at: <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

Owner.” *Adaptics Ltd. v. Perfect Co.*, IPR2018-01596, Paper 20 at 24.
(PTAB Mar. 6, 2019) (informative).

With these principles in mind, we analyze whether or not the Petition complies with the particularity requirement of 35 U.S.C. § 312(a)(3).

Petitioner’s first two grounds allege anticipation of claims 1, 2, and 5–12 by Terashima and claims 1, 5, 6, 9, and 12 by Sugimoto. Pet. 5. Grounds 3–12 are obviousness grounds based on a multiplicity of prior art combinations. *Id.* at 5–6.

Ground 3 relies on Shin as the primary reference and “one or more of Terashima, Sugimoto, Uemura ’259, Uemura ’999 *and/or* Inoue (Collectively the ‘Thin Film Art’).” Pet. 65 (emphasis added).¹³ Petitioner relies on these references for disclosure of the “thin film” requirement of the recited “first n-electrode,” “first p-electrode,” “second n-electrode,” and “second p-electrode.” Pet. 69–75, 76–80. Petitioner’s use of “and/or” in defining this ground results in potentially at least 25 different combinations of Shin with the cited Thin Film Art. The unduly burdensome nature of Ground 3 is puzzling in light of Petitioner’s argument that “[u]sing thin film electrodes as taught in each of the Thin Film Art was well-understood, common knowledge, predictable, and routine in 2003.” Pet. 71–72. Petitioner compounds the multiplicity of potential combinations resulting from Ground 3 by further combining the 25 combinations of prior art asserted in Ground 3 with Shelton, Inoue, Terashima, Sugimoto, and/or the level of ordinary skill in the art in Grounds 4 and 6–11.

¹³ In connection with its explanation of the Thin Film Art in Ground 3, Petitioner cites to an additional reference, Song. Pet. 71–72 (citing Ex. 1017).

Ground 12 alleges that claims 1, 2, and 4–13 would have been obvious based on “Grounds 1, 4–8, and 11 regarding Terashima in view of Sugimoto, Uemura ’259, Uemura ’999 and/or the” ordinary level of skill in the art. Pet. 6. Petitioner fails to offer any meaningful explanation of this ground other than to refer back to Petitioner’s reasoning with respect to a proposed modification of Shin, which is the primary reference relied on in Ground 3. *See id.* at 94. Ground 12 is analogous to the ground in *Adaptics* referred to as a “catch-all” that was determined to be “not reasonably bounded in scope and unduly burdensome for both the Board and Patent Owner to address.” *Adaptics*, Paper 20 at 21.

For the foregoing reasons, we determine that the Petition fails to meet the particularity requirement of 35 U.S.C. § 312(a)(3) resulting in voluminous and excessive grounds. Even, if we were to determine that Petitioner met its burden to establish a reasonable likelihood that one or more claims are anticipated by either Terashima or Sugimoto, in order to address all challenged claims, including claims 4 and 13, in a Final Written Decision, we would need to address at least Grounds 3, 11, and 12. Such an undertaking would be unduly burdensome for the Patent Owner and inefficient for the Board. Therefore, we further determine that “in the interests of efficient administration of the Office and integrity of the patent system and as a matter of procedural fairness to Patent Owner, the entire petition should be denied under 35 U.S.C. § 314(a).” *Adaptics*, Paper 20 at 24.

III. CONCLUSION

We exercise our discretion under 35 U.S.C. § 314(a) and deny institution of *inter partes* review.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, the Petition is *denied* and no trial is instituted.

IPR2024-00988
Patent 7,554,126 B2

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