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CONFIRMATION NO. 2837

FILING RECEIPT

31817
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Date Mailed: 01/26/2018

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Early Publication Request: No

Title

TIME DOMAIN RESOURCE ALLOCATION AND SOFT BUFFER HANDLING IN NEW RADIO (NR)

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

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Title of Invention

TIME DOMAIN RESOURCE ALLOCATION AND SOFT BUFFER HANDLING IN NEW RADIO (NR)

Attorney Docket Number (if applicable)

111027-AA7997-Z

Correspondence Address

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31817

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• No.

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Signature	Ryan N. Strauss/			Date (YYYY-MM-DD)	2018-01-12
First Name	Ryan N.	Last Name	Strauss	Registration Number (If appropriate)	68392

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UNITED STATES PROVISIONAL APPLICATION

For

**TIME DOMAIN RESOURCE ALLOCATION AND SOFT BUFFER HANDLING IN
NEW RADIO (NR)**

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TIME DOMAIN RESOURCE ALLOCATION AND SOFT BUFFER HANDLING IN NEW RADIO (NR)

BACKGROUND

Various embodiments generally may relate to the field of wireless communications.

DETAILED DESCRIPTION

The following detailed description refers to the accompanying drawings. The same reference numbers may be used in different drawings to identify the same or similar elements. In the following description, for purposes of explanation and not limitation, specific details are set forth such as particular structures, architectures, interfaces, techniques, etc. in order to provide a thorough understanding of the various aspects of various embodiments. However, it will be apparent to those skilled in the art having the benefit of the present disclosure that the various aspects of the various embodiments may be practiced in other examples that depart from these specific details. In certain instances, descriptions of well-known devices, circuits, and methods are omitted so as not to obscure the description of the various embodiments with unnecessary detail. For the purposes of the present document, the phrase “A or B” means (A), (B), or (A and B).

Introduction

Mobile communication has evolved significantly from early voice systems to today's highly sophisticated integrated communication platform. The next generation wireless communication system, 5G, or new radio (NR) will provide access to information and sharing of data anywhere, anytime by various users and applications. NR is expected to be a unified network/system that target to meet vastly different and sometime conflicting performance dimensions and services. Such diverse multi-dimensional requirements are driven by different services and applications. In general, NR will evolve based on 3GPP LTE-Advanced with additional potential new Radio Access Technologies (RATs) to enrich people lives with better, simple and seamless wireless connectivity solutions. NR will enable everything connected by wireless and deliver fast, rich contents and services.

Embodiments herein provide mechanisms for time-domain resource allocation for DL and UL shared channels (PDSCH and PUSCH) that may be scheduled dynamically using DCI carried by PDCCH or based on semi-static configurations, e.g., DL Semi-persistent Scheduling (DL SPS) or UL transmissions without UL grant.

Specifically, the details of indication of time-domain symbol using a combination of higher layer and DCI signaling for PDSCH and PUSCH are disclosed. Handling of time-domain resource allocation field and related signaling for fallback DCI formats (i.e., DCI formats 0_0 and 1_0) are also disclosed.

Further, for PDSCH or PUSCH with aggregated slots wherein the transport block (TB) is repeated with same or different redundancy versions (RVs), the details of resource mapping for multiple slots with PDSCH/PUSCH mapping type A, and for multiple “mini-slots”, latter at least with lengths of 2, 4, 7 symbols with PDSCH/PUSCH mapping type B, are disclosed.

In particular, details of time domain resource allocation indication for mini-slot operation, solutions for conflict resolution in case of link direction conflicts or collisions between physical channels are disclosed. Various embodiments may include the following:

- Details of indication of time-domain symbol using a combination of higher layer and DCI signaling for PDSCH and PUSCH are disclosed.
- Time domain resource allocation indication for mini-slot operation.
- Postponing and dropping rules for multi-mini-slot transmission.
- Collision handling of SRS with semi-statically or semi-persistently configured UL transmission.

Time-Domain Resource Allocation Embodiments

The following [3GPP TS 38.214 Editor’s CR, R1-1721344] has been agreed in 3GPP regarding time-domain resource allocation, with the exact details of time-domain resource indication being open.

For PDSCH:

6.1.2.1 Resource allocation in time domain

When the UE is scheduled to transmit PUSCH by a DCI, the Time-domain PUSCH resources field of the DCI provides a row index of an RRC configured table [pusch-symbolAllocation], where the indexed row defines the slot offset K_2 , the start and length indicator SLIV, and the PUSCH mapping type to be applied in the PUSCH reception.

- *The slot where the UE shall transmit the PUSCH is determined by K_2 of the indexed row as*

$$\left\lfloor n \cdot \frac{2^{\mu_{\text{PUSCH}}}}{2^{\mu_{\text{PDSCH}}}} \right\rfloor + K_2 \quad \text{where } n \text{ is the slot with the scheduling DCI, } K \text{ is based on the numerology of PUSCH, and}$$

- *The starting symbol S relative to [the start of the slot], and the number of consecutive symbols L counting from the symbol S allocated for the PUSCH are determined from the start and length indicator SLIV of the indexed row:*

if $(L-1) \leq 7$ then
 $SLIV = 14 \cdot (L-1) + S$
 else
 $SLIV = 14 \cdot (14-L+1) + (14-1-S)$
 where $0 < L \leq 14-S$, and
 - The PUSCH mapping type is set to Type A or Type B as defined in [38.211 Subclause 6.4.1.1.3] as given by the indexed row.

For PUSCH:

5.1.2.1 Resource allocation in time domain

When the UE is scheduled to receive PDSCH by a DCI, the Time-domain PDSCH resources field of the DCI provides a row index of an RRC configured table [pdsch-symbolAllocation], where the indexed row defines the slot offset K_0 , the start and length indicator SLIV, and the PDSCH mapping type to be assumed in the PDSCH reception.

- The slot allocated for the PDSCH is determined by K_0 of the indexed row $n+K_0$, where n is the slot with the scheduling DCI, K_0 is based on the numerology of PDSCH, and
- The starting symbol S relative to [the start of the slot], and the number of consecutive symbols L counting from the symbol S allocated for the PDSCH are determined from the start and length indicator SLIV of the indexed row:

if $(L-1) \leq 7$ then
 $SLIV = 14 \cdot (L-1) + S$
 else
 $SLIV = 14 \cdot (14-L+1) + (14-1-S)$
 where $0 < L \leq 14-S$, and
 - The PDSCH mapping type is set to Type A or Type B as defined in sub-clause 7.4.1.1.2 [4, TS 38.211] as given by the indexed row.

When the UE is configured with aggregation-factor-DL > 1, the same symbol allocation is applied across the aggregation-factor-DL consecutive slots not defined as UL by the slot format indication.

The following were also agreed for the details of configuration of each row of the table configured by RRC (“higher layers”) [3GPP RAN1 #91 Chairman’s Notes]:

Agreements:

- One table for UL, one table for DL configured by RRC in Rel-15
 - Each table is up to 16 rows
- In the table, each row is configured by RRC with
 - K_0 using 2 bits (for DL table), K_2 using 3 bits (for UL table)
 - an index (6-bit) into a table/equation in RAN1 specs capturing valid combinations of start symbol and length (jointly encoded)
 - PDSCH mapping type A or B
- The reference point for starting OFDM symbol:
 - No RRC impact (e.g., slot boundary, start of CORESET where the PDCCH was found, or part of the table/equation in RAN1 specs. FFS details)
- Aggregation factor (1, 2, 4, 8 for DL or UL) is semi-statically configured separately (i.e. not part of table)

- *No additional RRC impact how to use the aggregation factor along with the tables*

It can be noted that considering 14 symbols in a slot, and using the mechanism of Starting and length indication value (SLIV) to jointly indicate starting symbol and the length of the PDSCH/PUSCH, 7 bits are needed, while the above-quoted decision indicates use of 6 bits for this indication. Next, embodiments for indicating the starting symbol and length of PDSCH/PUSCH using no more than 6 bits of RRC signaling are provided.

Aspects of such embodiments are based on the observation that not all combinations of starting symbols and lengths for PDSCH/PUSCH may be supported for each of the mapping types (i.e., PDSCH/PUSCH mapping types A and B).

Note that it is assumed that the allocated PDSCH/PUSCH symbols are contiguous in time. Specifically, the following constraints may be applied:

- PDSCH/PUSCH mapping type A
 - In embodiments, the indicated starting symbol may only be one of symbols #0, 1, 2, 3.
 - In embodiments, the indicated length of the PDSCH/PUSCH is at least $L_{\min}$, with $L_{\min}$ no less than 2 symbols and with a maximum of 14 symbols
 - In an example, $L_{\min} = 3$, or, in another example, $L_{\min} = 7$
- PDSCH/PUSCH mapping type B
 - In embodiments, the indicated length of the PDSCH/PUSCH can be one of 2, 4, or 7 symbols
 - In other embodiments, the indicated length of the PDSCH/PUSCH can be one of 1, 2, 4, or 7 symbols

Next, recall that it has been agreed that the rows of the time-domain resource allocation table are configured using semi-static RRC signaling, via the signaling of the following components by higher layers:

1. Slot index indication: K0 using 2 bits (for DL table), K2 using 3 bits (for UL table);
2. An index (6-bit) into a table/equation in RAN1 specs capturing valid combinations of start symbol and length (jointly encoded);
3. PDSCH/PUSCH mapping type A or B

In embodiments, the starting symbol and length of the PDSCH/PUSCH for a row of the RRC-configured table is determined as a function of the PDSCH/PUSCH mapping type for that row.

In embodiments, the slot index indication (K0 and K2 values) for a row of the RRC-configured table is determined as a function of the PDSCH/PUSCH mapping type for that row.

In embodiments, when PDSCH/PUSCH mapping type is A, a table in the RAN1 specs is used (instead of an SLIV based formulation) such that all combinations of the following are supported:

- Starting symbol = 0, 1, 2, or 3
- Alt1: PDSCH/PUSCH length may range between 7 through 14 symbols
 - Alt2: PDSCH/PUSCH length may range between 3 and 14 symbols

For mapping type A, Alt1 would require 4 states each for lengths 7 – 10, and 1, 2, 3, and 4 states respectively for lengths 14, 13, 12, 11. Thus, a total of 26 states. For Alt2, this becomes 26 states + 4*4 states = 42 states.

In embodiments, when PDSCH/PUSCH mapping type is B, a table in the RAN1 specs, that is different from the one for PDSCH/PUSCH mapping type A, is used (instead of an SLIV based formulation) such that all combinations of the following are supported:

- Starting symbol = All possible starting locations within a slot possible for the lengths listed in the next bullet such that the allocated symbols do not cross the slot-boundary.
- Alt1: PDSCH/PUSCH length may be one of: 2, 4, or 7 symbols
 - Alt2: PDSCH/PUSCH length may be one of: 1, 2, 4, or 7 symbols

For mapping type B, Alt1 would require 13, 11, and 8 states respectively for lengths 2, 4, and 7 symbols. Thus, a total of 32 states. For Alt2, this becomes 32 states + 14 states = 46 states.

Therefore, in embodiments, a 5-bit (for Alt1 options above) or 6-bit table is defined in specifications – one each for mapping types A and B, to indicate the candidate combinations of starting symbol and length of the PDSCH/PUSCH to construct the RRC-configured table.. The UE uses the appropriate table based on the 1 bit PDSCH/PUSCH mapping type indicator to determine the starting symbol and length information corresponding to a row to build the RRC table. If a 6-bit table is used the unused states are reserved.

Further, in embodiments, for PDSCH mapping type B, the possible valid values of K0 are limited to only one of two values: 0 or 1.

Further, in embodiments, for PUSCH mapping type B, the possible valid values of K2 are limited to only one of two or four values instead of eight values (corresponding to 3-bit for K2 as quoted above).

Further, in embodiments, when fallback DCI formats (formats 0_0 and 1_0) are used, the number of bits of the time-domain RA field is reduced from 4 to 2 bits. To help facilitate such reduction, the candidate values for K0, K2 could be reduced to effectively 0 or 1 bit, i.e., either a fixed value or one of two values.

For the above, it is assumed that the reference point for the starting symbol for the PDSCH/PUSCH is with respect to the slot-boundary. However, the above ideas can be straightforwardly applied if the reference point for the starting symbol is with respect to the start of CORESET where the PDCCH was found.

In other embodiments, for PDSCH/PUSCH mapping type B, the reference is the start of CORESET where the PDCCH was found, while for mapping type A, the reference is slot boundary. In such a case, for PDSCH mapping type B, under the assumption that the scheduled PDSCH may only be scheduled within the same slot where the PDCCH was found (i.e., $K0 = 0$), the starting symbols of PDSCH may only be such that the resulting symbol index is greater than the symbol index of the CORESET where the PDCCH was found and less than #13. Without the $K0 = 0$ constraint, the table specified for mapping type B would indicate negative values when the start of the CORESET is different from symbol #0.

Time domain resource allocation indication for mini-slot operation

Note: In the rest of the disclosure, an SLIV-based starting symbol and length indication is assumed, but the ideas in the rest of the disclosure can be straightforwardly adapted if the starting symbol and length indication is based on the mechanism described in previous section – i.e., using different tables specified based on the PDSCH/PUSCH mapping type.

Current agreements for NR state that DCI resource allocation field encodes starting symbol and duration of PDSCH/PUSCH transmission by a Start and Length Indication Value (SLIV) approach which encodes these parameters jointly. This approach assumes contiguous allocation of resources.

It was also agreed, that aggregation factor of {1, 2, 4, 8} is configured semi-statically (i.e. using RRC). The aggregation factor is used to populate the time-domain allocation over multiple slots or within a slot in order to organize bundled / repeated transmission of a transport block.

In case of slot-based resource allocation, i.e. PDSCH/PUSCH mapping type A, if aggregation is configured, the dynamically indicated SLIV-based resource allocation or semi-statically derived start and duration (in case of semi-persistent allocation) may be assumed to be repeated in K consecutive valid slots, where K is the aggregation factor configured by RRC.

In embodiments of mini-slot based / non-slot based resource allocation, i.e. PDSCH/PUSCH mapping type B, if aggregation is configured, the dynamically indicated SLIV-based resource allocation or semi-statically derived start and duration (in case of semi-persistent allocation) may be assumed to be repeated in consecutive K groups of valid symbols, where K is the aggregation factor configured by RRC. The first group of valid symbols is directly derived from the time domain resource allocation field including SLIV indication which signals starting symbol and length in symbols. The other groups of symbols have the same length as the first one and starting symbol index derived as the next valid symbol after the previous group of symbols in an aggregation. In other words, the mini-slots are repeated back-to-back without gaps within the valid symbols.

Herein, the valid symbols are defined as all symbols of currently scheduled transmission direction, i.e. DL for PDSCH and UL PUSCH.

Further, PUSCH transmission case is discussed in more details without loss of generality and assuming the PDSCH multi-slot and multi-mini-slot transmission may follow the same principles if applicable.

Postponing and dropping rules for multi-mini-slot transmission

The described multi-mini-slot transmission procedure may lead to cases when mini-slot crosses slot boundary and/or collides with at least scheduled SRS transmission. For such cases, dropping and/or postponing rules may need to be defined.

In embodiments, in case a group of symbols in an aggregated multi-mini-slot transmission, i.e. aggregated PUSCH transmission of mapping type B, is going to cross the slot boundary, it may need to be postponed i.e. shifted in time to the first valid symbol in the next slot relative to the slot where the previous group of symbols was mapped. For example, if resource allocation (semi-static or dynamic) indicates starting symbol 7 (counting from 0) and duration 4 symbols, while the aggregation factor is configured to 4, then the overall repeated resource allocation would look the following:

```
N-th slot:  -----00001111--
N+1-th slot: 22223333-----
```

In another option, the groups of symbols which are going to cross the slot boundary and be mapped to the next slots(s) are completely dropped as illustrated below taking the same example as previously:

N-th slot: -----00001111-----
 N+1-th slot: -----

In another option, the groups of symbols which are going to cross the slot boundary are dropped while the groups of symbols which are going to be mapped to the next slot(s) are kept:

N-th slot: -----00001111-----
 N+1-th slot: ---3333-----

In other embodiments, if the dynamic or semi-static time-domain resource allocation indicates resources which overlapped with SRS resources, the group(s) of PUSCH symbols fully or partially overlapped with SRS resources are not transmitted. In this case, these PUSCH symbols are either dropped or postponed. The same options as described above for the case of crossing slot boundary are applicable. Alternatively, the PUSCH transmission may be prioritized over the SRS resources and be transmitted instead. The prioritization rule may be based on logical channel priority mapped to the corresponding PUSCH. E.g. the logical channel serving URLLC services may be prioritized over SRS transmissions.

Collision handling of SRS with semi-statically or semi-persistently configured UL transmission

As captured below in TS38.214 V15.0.0 [1], priority rules or dropping rules are defined when sounding reference signal (SRS) collides with physical uplink control channel (PUCCH) with short duration.

A UE shall not transmit SRS when semi-persistent and periodic SRS are configured in the same symbol(s) with short PUCCH carrying only CSI reports, or if aperiodic SRS is configured and short PUCCH consists of beam failure request. In the case that SRS is not transmitted due to overlap with short PUCCH, only the SRS symbol(s) that overlap with short PUCCH symbol(s) are dropped. Short PUCCH shall not be transmitted when aperiodic SRS happens to overlap in the same symbol with semi-persistent or periodic short PUCCH carrying semi-persistent/periodic CSI report only.

A UE is not expected to be configured with aperiodic SRS and short PUCCH with aperiodic CSI report in the same symbol.

A UE is not expected to be configured with SRS and PUSCH/UL DMRS/UL PTRS/Long PUCCH in the same symbol.

However, in case of SRS collision with semi-statically or semi-persistently configured uplink transmission, including Type 1 and Type 2 grant free uplink transmission, UL semi-persistent transmission, or configured scheduling uplink transmission, etc., certain priority rule or dropping rule needs to be defined.

In embodiments, UE shall not transmit SRS when semi-persistent and periodic SRS are configured in the same symbol(s) with uplink transmission which is semi-statically or semi-persistently configured. In the case that SRS is not transmitted due to overlap with uplink transmission which is semi-statically or semi-persistently configured, only the SRS symbol(s) that overlap with uplink transmission which is semi-statically or semi-persistently configured are dropped.

In other embodiments, UE shall not transmit uplink transmission which is semi-statically or semi-persistently configured when aperiodic SRS happens to overlap in the same symbol with transmit uplink transmission which is semi-statically or semi-persistently configured.

In another option, for type 2 UL transmission without grant, when the transmission at the first activated resource collides with aperiodic SRS transmission, aperiodic SRS transmission is dropped. For the uplink transmission after the first activation, in case when UL transmission without grant collides with aperiodic SRS transmission, UL transmission without grant is dropped.

In other embodiments, in case when physical random access channel (PRACH) and physical uplink control channel carrying beam failure request collide with uplink transmission which is semi-statically or semi-persistently configured, UE shall not transmit uplink transmission which is semi-statically or semi-persistently configured.

In other embodiments, the dropping rule or priority rule may depend on transmission duration or type of uplink transmission. For instance, mini-slot based uplink transmission which is semi-statically or semi-persistently configured may have higher priority than aperiodic SRS transmission, but slot based uplink transmission which is semi-statically or semi-persistently configured may have lower priority than aperiodic SRS transmission.

Soft buffer handling in NR

In last RAN1 meeting (including email discussion [91-NR-16]), the final details of LBRM text were agreed. While the specification is correctly capturing the agreements, it should be noted that some potential clarifications that could further improve the text :

1. First with respect to the parameters (maximum number of layers supported by the UE for the serving cell and maximum modulation order configured for the serving cell), it should be noted that for each link (downlink or uplink), the corresponding parameters for that link are used i.e. for PDSCH, the downlink parameter settings are used, and for uplink the uplink parameter settings are used.

Proposed Clarification 2.1 (In 38.212, sec 5.4.2.1): LBRM is applied using downlink parameter settings for downlink TBs and using uplink parameter settings for uplink TBs.

2. A UE can support upto eight layers for downlink. The intention of the original agreement was that the “*maximum number of layers supported by the UE for the serving cell*” should be the maximum number of layers for one transport block. Therefore, in various embodiments, the following clarification may be added: “*maximum number of layers supported by the UE for the serving cell for a TB*”. With this clarification, it would be clear that LBRM is applied based on four layers (i.e. a TB cannot map to more than four layers).

Proposed Clarification 2.2 (In 38.212, sec 5.4.2.1): add text in red: “*maximum number of layers supported by the UE for the serving cell for a TB*”

In our understanding, it is important to note that the soft buffer should be dimensioned so as to not require simultaneous support of peak rate, full IR support, and the maximum number of HARQ processes. One option could be to use $M_{limit} * (TBS_{LBRM} / R_{LBRM})$ as the number of soft buffer bits stored for a given CC. If the maximum number of HARQ processes supported for NR is 8 or 16, then M_{limit} can be a smaller value than 8 or 16 (e.g. 4, may depend on N1 value) to reflect the UE storage is not dimensioned for the simultaneous support of peak rate/full IR and max HARQ processes.

In offline discussions in last RAN1 meeting, some concerns were raised on applying very small value such as 2 ms always. On the other hand, from a UE perspective, it is highly desirable to not offer excessive soft buffer by using larger RTTs, in particular for case where UE is supporting aggressive processing times which should allow faster RTT. Then one compromise may be to use different reference RTTs for carriers in different frequency region, and using a much

more aggressive reference RTT numbers for scenarios where higher data rates and faster roundtrip times are necessary.

Then, the following formulation may be used.

- Below 3 GHz and FR1, reference HARQ_RTT is [X] ms,
- For 3-6 GHz and FR1 and for FR2 => reference HARQ_RTT is [2] ms

The peak data rate formula from last meeting (R1-1721733) can be adapted to include reference HARQRTT per component carrier to obtain the soft buffer dimensioning. An example is shown below.

$$SoftBuffer = \sum_{j=1}^J \left(v_{Layers}^{(j)} \cdot Q_m^{(j)} \cdot f^{(j)} \cdot R_{max} \cdot \frac{N_{PRB}^{BW(j),\mu} \cdot 12}{T_s^{\mu}} \cdot (1 - OH^{(j)}) \right) \cdot refHARQRTT^{(j)}$$

Figures XQ-XZ

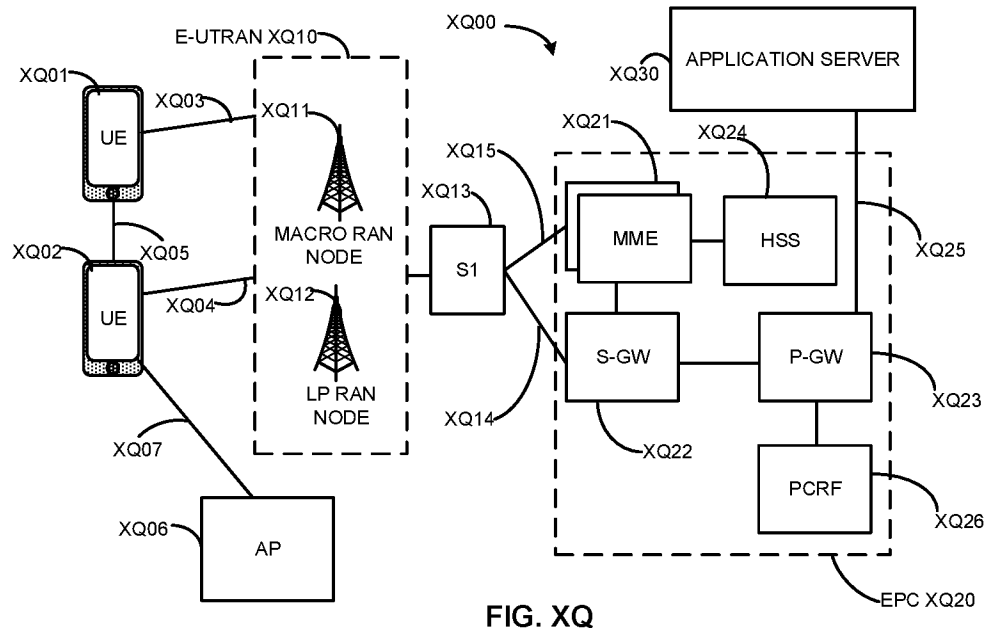


FIG. XQ

FIG. XQ illustrates an architecture of a system XQ00 of a network in accordance with some embodiments. The system XQ00 is shown to include a user equipment (UE) XQ01 and a UE XQ02. The UEs XQ01 and XQ02 are illustrated as smartphones (e.g., handheld touchscreen mobile computing devices connectable to one or more cellular networks), but may also comprise any mobile or non-mobile computing device, such as Personal Data Assistants (PDAs), pagers, laptop computers, desktop computers, wireless handsets, or any computing device including a wireless communications interface.

In some embodiments, any of the UEs XQ01 and XQ02 can comprise an Internet of Things (IoT) UE, which can comprise a network access layer designed for low-power IoT applications utilizing short-lived UE connections. An IoT UE can utilize technologies such as machine-to-machine (M2M) or machine-type communications (MTC) for exchanging data with an MTC server or device via a public land mobile network (PLMN), Proximity-Based Service (ProSe) or device-to-device (D2D) communication, sensor networks, or IoT networks. The M2M or MTC exchange of data may be a machine-initiated exchange of data. An IoT network describes interconnecting IoT UEs, which may include uniquely identifiable embedded computing devices (within the Internet infrastructure), with short-lived connections. The IoT UEs may execute background applications (e.g., keep-alive messages, status updates, etc.) to facilitate the connections of the IoT network.

The UEs XQ01 and XQ02 may be configured to connect, e.g., communicatively couple, with a radio access network (RAN) XQ10 — the RAN XQ10 may be, for example, an Evolved Universal Mobile Telecommunications System (UMTS) Terrestrial Radio Access Network (E-UTRAN), a NextGen RAN (NG RAN), or some other type of RAN. The UEs XQ01 and XQ02 utilize connections XQ03 and XQ04, respectively, each of which comprises a physical communications interface or layer (discussed in further detail infra); in this example, the connections XQ03 and XQ04 are illustrated as an air interface to enable communicative coupling, and can be consistent with cellular communications protocols, such as a Global System for Mobile Communications (GSM) protocol, a code-division multiple access (CDMA) network protocol, a Push-to-Talk (PTT) protocol, a PTT over Cellular (POC) protocol, a Universal Mobile Telecommunications System (UMTS) protocol, a 3GPP Long Term Evolution (LTE) protocol, a fifth generation (5G) protocol, a New Radio (NR) protocol, and the like.

In this embodiment, the UEs XQ01 and XQ02 may further directly exchange communication data via a ProSe interface XQ05. The ProSe interface XQ05 may alternatively be referred to as a sidelink interface comprising one or more logical channels, including but not limited to a Physical Sidelink Control Channel (PSCCH), a Physical Sidelink Shared Channel (PSSCH), a Physical Sidelink Discovery Channel (PSDCH), and a Physical Sidelink Broadcast Channel (PSBCH). In various implementations, the SL interface XQ05 may be used in vehicular applications and communications technologies, which are often referred to as V2X systems. V2X is a mode of communication where UEs (for example, UEs XQ01, XQ02) communicate with each

other directly over the PC5/SL interface 105 and can take place when the UEs XQ01, XQ02 are served by RAN nodes XQ11, XQ12 or when one or more UEs are outside a coverage area of the RAN XS10. V2X may be classified into four different types: vehicle-to-vehicle (V2V), vehicle-to-infrastructure (V2I), vehicle-to-network (V2N), and vehicle-to-pedestrian (V2P). These V2X applications can use “co-operative awareness” to provide more intelligent services for end-users. For example, vUEs XQ01, XQ02, RAN nodes XQ11, XQ12, application servers XQ30, and pedestrian UEs XQ01, XQ02 may collect knowledge of their local environment (for example, information received from other vehicles or sensor equipment in proximity) to process and share that knowledge in order to provide more intelligent services, such as cooperative collision warning, autonomous driving, and the like. In these implementations, the UEs XQ01, XQ02 may be implemented/employed as Vehicle Embedded Communications Systems (VECS) or vUEs.

The UE XQ02 is shown to be configured to access an access point (AP) XQ06 (also referred to as also referred to as “WLAN node XQ06”, “WLAN XQ06”, “WLAN Termination XQ06” or “WT XQ06” or the like) via connection XQ07. The connection XQ07 can comprise a local wireless connection, such as a connection consistent with any IEEE 802.11 protocol, wherein the AP XQ06 would comprise a wireless fidelity (WiFi®) router. In this example, the AP XQ06 is shown to be connected to the Internet without connecting to the core network of the wireless system (described in further detail below). In various embodiments, the UE XQ02, RAN XQ10, and AP XQ06 may be configured to utilize LTE-WLAN aggregation (LWA) operation and/or WLAN LTE/WLAN Radio Level Integration with IPsec Tunnel (LWIP) operation. The LWA operation may involve the UE XQ02 in RRC_CONNECTED being configured by a RAN node XQ11, XQ12 to utilize radio resources of LTE and WLAN. LWIP operation may involve the UE XQ02 using WLAN radio resources (e.g., connection XQ07) via Internet Protocol Security (IPsec) protocol tunneling to authenticate and encrypt packets (e.g., internet protocol (IP) packets) sent over the connection XQ07. IPsec tunneling may include encapsulating entirety of original IP packets and adding a new packet header thereby protecting the original header of the IP packets.

The RAN XQ10 can include one or more access nodes that enable the connections XQ03 and XQ04. These access nodes (ANs) can be referred to as base stations (BSs), NodeBs, evolved NodeBs (eNBs), next Generation NodeBs (gNB), RAN nodes, Road Side Units (RSUs), and so forth, and can comprise ground stations (e.g., terrestrial access points) or satellite stations providing coverage within a geographic area (e.g., a cell). The term “Road Side Unit” or “RSU”

may refer to any transportation infrastructure entity implemented in or by an gNB/eNB/RAN node or a stationary (or relatively stationary) UE, where an RSU implemented in or by a UE may be referred to as a “UE-type RSU”, an RSU implemented in or by an eNB may be referred to as an “eNB-type RSU.” The RAN XQ10 may include one or more RAN nodes for providing macrocells, e.g., macro RAN node XQ11, and one or more RAN nodes for providing femtocells or picocells (e.g., cells having smaller coverage areas, smaller user capacity, or higher bandwidth compared to macrocells), e.g., low power (LP) RAN node XQ12.

Any of the RAN nodes XQ11 and XQ12 can terminate the air interface protocol and can be the first point of contact for the UEs XQ01 and XQ02. In some embodiments, any of the RAN nodes XQ11 and XQ12 can fulfill various logical functions for the RAN XQ10 including, but not limited to, radio network controller (RNC) functions such as radio bearer management, uplink and downlink dynamic radio resource management and data packet scheduling, and mobility management.

In accordance with some embodiments, the UEs XQ01 and XQ02 can be configured to communicate using Orthogonal Frequency-Division Multiplexing (OFDM) communication signals with each other or with any of the RAN nodes XQ11 and XQ12 over a multicarrier communication channel in accordance various communication techniques, such as, but not limited to, an Orthogonal Frequency-Division Multiple Access (OFDMA) communication technique (e.g., for downlink communications) or a Single Carrier Frequency Division Multiple Access (SC-FDMA) communication technique (e.g., for uplink and ProSe or sidelink communications), although the scope of the embodiments is not limited in this respect. The OFDM signals can comprise a plurality of orthogonal subcarriers.

In some embodiments, a downlink resource grid can be used for downlink transmissions from any of the RAN nodes XQ11 and XQ12 to the UEs XQ01 and XQ02, while uplink transmissions can utilize similar techniques. The grid can be a time-frequency grid, called a resource grid or time-frequency resource grid, which is the physical resource in the downlink in each slot. Such a time-frequency plane representation is a common practice for OFDM systems, which makes it intuitive for radio resource allocation. Each column and each row of the resource grid corresponds to one OFDM symbol and one OFDM subcarrier, respectively. The duration of the resource grid in the time domain corresponds to one slot in a radio frame. The smallest time-frequency unit in a resource grid is denoted as a resource element. Each resource grid comprises a

number of resource blocks, which describe the mapping of certain physical channels to resource elements. Each resource block comprises a collection of resource elements; in the frequency domain, this may represent the smallest quantity of resources that currently can be allocated. There are several different physical downlink channels that are conveyed using such resource blocks.

The physical downlink shared channel (PDSCH) may carry user data and higher-layer signaling to the UEs XQ01 and XQ02. The physical downlink control channel (PDCCH) may carry information about the transport format and resource allocations related to the PDSCH channel, among other things. It may also inform the UEs XQ01 and XQ02 about the transport format, resource allocation, and H-ARQ (Hybrid Automatic Repeat Request) information related to the uplink shared channel. Typically, downlink scheduling (assigning control and shared channel resource blocks to the UE 102 within a cell) may be performed at any of the RAN nodes XQ11 and XQ12 based on channel quality information fed back from any of the UEs XQ01 and XQ02. The downlink resource assignment information may be sent on the PDCCH used for (e.g., assigned to) each of the UEs XQ01 and XQ02.

The PDCCH may use control channel elements (CCEs) to convey the control information. Before being mapped to resource elements, the PDCCH complex-valued symbols may first be organized into quadruplets, which may then be permuted using a sub-block interleaver for rate matching. Each PDCCH may be transmitted using one or more of these CCEs, where each CCE may correspond to nine sets of four physical resource elements known as resource element groups (REGs). Four Quadrature Phase Shift Keying (QPSK) symbols may be mapped to each REG. The PDCCH can be transmitted using one or more CCEs, depending on the size of the downlink control information (DCI) and the channel condition. There can be four or more different PDCCH formats defined in LTE with different numbers of CCEs (e.g., aggregation level, $L=1, 2, 4$, or 8).

Some embodiments may use concepts for resource allocation for control channel information that are an extension of the above-described concepts. For example, some embodiments may utilize an enhanced physical downlink control channel (EPDCCH) that uses PDSCH resources for control information transmission. The EPDCCH may be transmitted using one or more enhanced the control channel elements (ECCEs). Similar to above, each ECCE may correspond to nine sets of four physical resource elements known as an enhanced resource element groups (EREGs). An ECCE may have other numbers of EREGs in some situations.

The RAN XQ10 is shown to be communicatively coupled to a core network (CN) XQ20—via an S1 interface XQ13. In embodiments, the CN XQ20 may be an evolved packet core (EPC) network, a NextGen Packet Core (NPC) network, or some other type of CN. In this embodiment the S1 interface XQ13 is split into two parts: the S1-U interface XQ14, which carries traffic data between the RAN nodes XQ11 and XQ12 and the serving gateway (S-GW) XQ22, and the S1-mobility management entity (MME) interface XQ15, which is a signaling interface between the RAN nodes XQ11 and XQ12 and MMEs XQ21.

In this embodiment, the CN XQ20 comprises the MMEs XQ21, the S-GW XQ22, the Packet Data Network (PDN) Gateway (P-GW) XQ23, and a home subscriber server (HSS) XQ24. The MMEs XQ21 may be similar in function to the control plane of legacy Serving General Packet Radio Service (GPRS) Support Nodes (SGSN). The MMEs XQ21 may manage mobility aspects in access such as gateway selection and tracking area list management. The HSS XQ24 may comprise a database for network users, including subscription-related information to support the network entities' handling of communication sessions. The CN XQ20 may comprise one or several HSSs XQ24, depending on the number of mobile subscribers, on the capacity of the equipment, on the organization of the network, etc. For example, the HSS XQ24 can provide support for routing/roaming, authentication, authorization, naming/addressing resolution, location dependencies, etc.

The S-GW XQ22 may terminate the S1 interface XQ13 towards the RAN XQ10, and routes data packets between the RAN XQ10 and the CN XQ20. In addition, the S-GW XQ22 may be a local mobility anchor point for inter-RAN node handovers and also may provide an anchor for inter-3GPP mobility. Other responsibilities may include lawful intercept, charging, and some policy enforcement.

The P-GW XQ23 may terminate an SGi interface toward a PDN. The P-GW XQ23 may route data packets between the EPC network XQ23 and external networks such as a network including the application server XQ30 (alternatively referred to as application function (AF)) via an Internet Protocol (IP) interface XQ25. Generally, the application server XQ30 may be an element offering applications that use IP bearer resources with the core network (e.g., UMTS Packet Services (PS) domain, LTE PS data services, etc.). In this embodiment, the P-GW XQ23 is shown to be communicatively coupled to an application server XQ30 via an IP communications interface XQ25. The application server XQ30 can also be configured to support one or more

communication services (e.g., Voice-over-Internet Protocol (VoIP) sessions, PTT sessions, group communication sessions, social networking services, etc.) for the UEs XQ01 and XQ02 via the CN XQ20.

The P-GW XQ23 may further be a node for policy enforcement and charging data collection. Policy and Charging Enforcement Function (PCRF) XQ26 is the policy and charging control element of the CN XQ20. In a non-roaming scenario, there may be a single PCRF in the Home Public Land Mobile Network (HPLMN) associated with a UE's Internet Protocol Connectivity Access Network (IP-CAN) session. In a roaming scenario with local breakout of traffic, there may be two PCRFs associated with a UE's IP-CAN session: a Home PCRF (H-PCRF) within a HPLMN and a Visited PCRF (V-PCRF) within a Visited Public Land Mobile Network (VPLMN). The PCRF XQ26 may be communicatively coupled to the application server XQ30 via the P-GW XQ23. The application server XQ30 may signal the PCRF XQ26 to indicate a new service flow and select the appropriate Quality of Service (QoS) and charging parameters. The PCRF XQ26 may provision this rule into a Policy and Charging Enforcement Function (PCEF) (not shown) with the appropriate traffic flow template (TFT) and QoS class of identifier (QCI), which commences the QoS and charging as specified by the application server XQ30.

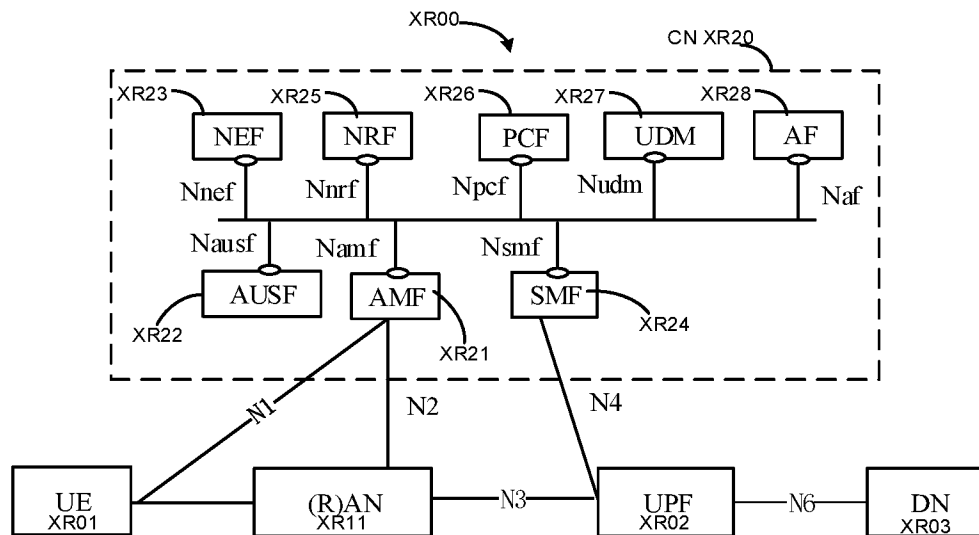


FIG. XR

FIG. XR illustrates an architecture of a system XR00 of a network in accordance with some embodiments. The system XR00 is shown to include a UE XR01, which may be the same or similar to UEs XQ01 and XQ02 discussed previously; a RAN node XR11, which may be the same or similar to RAN nodes XQ11 and XQ12 discussed previously; a User Plane Function (UPF) XR02;

a Data network (DN) XR03, which may be, for example, operator services, Internet access or 3rd party services; and a 5G Core Network (5GC or CN) XR20.

The CN XR20 may include an Authentication Server Function (AUSF) XR22; a Core Access and Mobility Management Function (AMF) XR21; a Session Management Function (SMF) XR24; a Network Exposure Function (NEF) XR23; a Policy Control function (PCF) XR26; a Network Function (NF) Repository Function (NRF) XR25; a Unified Data Management (UDM) XR27; and an Application Function (AF) XR28. The CN XR20 may also include other elements that are not shown, such as a Structured Data Storage network function (SDSF), an Unstructured Data Storage network function (UDSF), and the like.

The UPF XR02 may act as an anchor point for intra-RAT and inter-RAT mobility, an external PDU session point of interconnect to DN XR03, and a branching point to support multi-homed PDU session. The UPF XR02 may also perform packet routing and forwarding, packet inspection, enforce user plane part of policy rules, lawfully intercept packets (UP collection); traffic usage reporting, perform QoS handling for user plane (e.g. packet filtering, gating, UL/DL rate enforcement), perform Uplink Traffic verification (e.g., SDF to QoS flow mapping), transport level packet marking in the uplink and downlink, and downlink packet buffering and downlink data notification triggering. UPF XR02 may include an uplink classifier to support routing traffic flows to a data network. The DN XR03 may represent various network operator services, Internet access, or third party services. NY XR03 may include, or be similar to application server XQ30 discussed previously.

The AUSF XR22 may store data for authentication of UE XR01 and handle authentication related functionality. The AUSF XR22 may facilitate a common authentication framework for various access types.

The AMF XR21 may be responsible for registration management (e.g., for registering UE XR01, etc.), connection management, reachability management, mobility management, and lawful interception of AMF-related events, and access authentication and authorization. AMF XR21 may provide transport for SM messages between and SMF XR24, and act as a transparent proxy for routing SM messages. AMF XR21 may also provide transport for short message service (SMS) messages between UE XR01 and an SMS function (SMSF) (not shown by FIG. XR). AMF XR21 may act as Security Anchor Function (SEA), which may include interaction with the AUSF XR22 and the UE XR01, receipt of an intermediate key that was established as a result of the UE XR01

authentication process. Where USIM based authentication is used, the AMF XR21 may retrieve the security material from the AUSF XR22. AMF XR21 may also include a Security Context Management (SCM) function, which receives a key from the SEA that it uses to derive access-network specific keys. Furthermore, AMF XR21 may be a termination point of RAN CP interface (N2 reference point), a termination point of NAS (N1) signalling, and perform NAS ciphering and integrity protection.

AMF XR21 may also support NAS signalling with a UE XR01 over an N3 interworking-function (IWF) interface. The N3IWF may be used to provide access to untrusted entities. N3IWF may be a termination point for the N2 and N3 interfaces for control plane and user plane, respectively, and as such, may handle N2 signalling from SMF and AMF for PDU sessions and QoS, encapsulate/de-encapsulate packets for IPsec and N3 tunnelling, mark N3 user-plane packets in the uplink, and enforce QoS corresponding to N3 packet marking taking into account QoS requirements associated to such marking received over N2. N3IWF may also relay uplink and downlink control-plane NAS (N1) signalling between the UE XR01 and AMF XR21, and relay uplink and downlink user-plane packets between the UE XR01 and UPF XR02. The N3IWF also provides mechanisms for IPsec tunnel establishment with the UE XR01.

The SMF XR24 may be responsible for session management (e.g., session establishment, modify and release, including tunnel maintain between UPF and AN node); UE IP address allocation & management (including optional Authorization); Selection and control of UP function; Configures traffic steering at UPF to route traffic to proper destination; termination of interfaces towards Policy control functions; control part of policy enforcement and QoS; lawful intercept (for SM events and interface to LI System); termination of SM parts of NAS messages; downlink Data Notification; initiator of AN specific SM information, sent via AMF over N2 to AN; determine SSC mode of a session. The SMF XR24 may include the following roaming functionality: handle local enforcement to apply QoS SLAs (VPLMN); charging data collection and charging interface (VPLMN); lawful intercept (in VPLMN for SM events and interface to LI System); support for interaction with external DN for transport of signalling for PDU session authorization/authentication by external DN.

The NEF XR23 may provide means for securely exposing the services and capabilities provided by 3GPP network functions for third party, internal exposure/re-exposure, Application Functions (e.g., AF XR28), edge computing or fog computing systems, etc. In such embodiments,

the NEF XR23 may authenticate, authorize, and/or throttle the AFs. NEF XR23 may also translate information exchanged with the AF XR28 and information exchanged with internal network functions. For example, the NEF XR23 may translate between an AF-Service-Identifier and an internal 5GC information. NEF XR23 may also receive information from other network functions (NFs) based on exposed capabilities of other network functions. This information may be stored at the NEF XR23 as structured data, or at a data storage NF using a standardized interfaces. The stored information can then be re-exposed by the NEF XR23 to other NFs and AFs, and/or used for other purposes such as analytics.

The NRF XR25 may support service discovery functions, receive NF Discovery Requests from NF instances, and provide the information of the discovered NF instances to the NF instances. NRF XR25 also maintains information of available NF instances and their supported services.

The PCF XR26 may provide policy rules to control plane function(s) to enforce them, and may also support unified policy framework to govern network behaviour. The PCF XR26 may also implement a front end (FE) to access subscription information relevant for policy decisions in a UDR of UDM XR27.

The UDM XR27 may handle subscription-related information to support the network entities' handling of communication sessions, and may store subscription data of UE XR01. The UDM XR27 may include two parts, an application FE and a User Data Repository (UDR). The UDM may include a UDM FE, which is in charge of processing of credentials, location management, subscription management and so on. Several different front ends may serve the same user in different transactions. The UDM-FE accesses subscription information stored in the UDR and performs authentication credential processing; user identification handling; access authorization; registration/mobility management; and subscription management. The UDR may interact with PCF XR26. UDM XR27 may also support SMS management, wherein an SMS-FE implements the similar application logic as discussed previously.

The AF XR28 may provide application influence on traffic routing, access to the Network Capability Exposure (NCE), and interact with the policy framework for policy control. The NCE may be a mechanism that allows the 5GC and AF XR28 to provide information to each other via NEF XR23, which may be used for edge computing implementations. In such implementations, the network operator and third party services may be hosted close to the UE XR01 access point of attachment to achieve an efficient service delivery through the reduced end-to-end latency and

load on the transport network. For edge computing implementations, the 5GC may select a UPF XR02 close to the UE XR01 and execute traffic steering from the UPF XR02 to DN XR03 via the N6 interface. This may be based on the UE subscription data, UE location, and information provided by the AF XR28. In this way, the AF XR28 may influence UPF (re)selection and traffic routing. Based on operator deployment, when AF XR28 is considered to be a trusted entity, the network operator may permit AF XR28 to interact directly with relevant NFs.

As discussed previously, the CN XR20 may include an SMSF, which may be responsible for SMS subscription checking and verification, and relaying SM messages to/from the UE XR01 to/from other entities, such as an SMS-GMSC/IWMSC/SMS-router. The SMS may also interact with AMF XR21 and UDM XR27 for notification procedure that the UE XR01 is available for SMS transfer (e.g., set a UE not reachable flag, and notifying UDM XR27 when UE XR01 is available for SMS).

The system XR00 may include the following service-based interfaces: Namf: Service-based interface exhibited by AMF; Nsmf: Service-based interface exhibited by SMF; Nnef: Service-based interface exhibited by NEF; Npcf: Service-based interface exhibited by PCF; Nudm: Service-based interface exhibited by UDM; Naf: Service-based interface exhibited by AF; Nnrf: Service-based interface exhibited by NRF; and Nausf: Service-based interface exhibited by AUSF.

The system XR00 may include the following reference points: N1: Reference point between the UE and the AMF; N2: Reference point between the (R)AN and the AMF; N3: Reference point between the (R)AN and the UPF; N4: Reference point between the SMF and the UPF; and N6: Reference point between the UPF and a Data Network. There may be many more reference points and/or service-based interfaces between the NF services in the NFs, however, these interfaces and reference points have been omitted for clarity. For example, an N5 reference point may be between the PCF and the AF; an N7 reference point may be between the PCF and the SMF; an N11 reference point between the AMF and SMF; etc. In some embodiments, the CN XR20 may include an Nx interface, which is an inter-CN interface between the MME (e.g., MME XQ21) and the AMF XR21 in order to enable interworking between CN XR20 and CN XQ20.

Although not shown by FIG. XR, system XR00 may include multiple RAN nodes XR11 wherein an Xn interface is defined between two or more RAN nodes XR11 (e.g., gNBs and the like) that connecting to 5GC XR20, between a RAN node XR11 (e.g., gNB) connecting to 5GC

XR20 and an eNB (e.g., a RAN node XQ11 of FIG. XQ), and/or between two eNBs connecting to 5GC XR20.

In some implementations, the Xn interface may include an Xn user plane (Xn-U) interface and an Xn control plane (Xn-C) interface. The Xn-U may provide non-guaranteed delivery of user plane PDUs and support/provide data forwarding and flow control functionality. The Xn-C may provide management and error handling functionality, functionality to manage the Xn-C interface; mobility support for UE XR01 in a connected mode (e.g., CM-CONNECTED) including functionality to manage the UE mobility for connected mode between one or more RAN nodes XR11. The mobility support may include context transfer from an old (source) serving RAN node XR11 to new (target) serving RAN node XR11; and control of user plane tunnels between old (source) serving RAN node XR11 to new (target) serving RAN node XR11.

A protocol stack of the Xn-U may include a transport network layer built on Internet Protocol (IP) transport layer, and a GTP-U layer on top of a UDP and/or IP layer(s) to carry user plane PDUs. The Xn-C protocol stack may include an application layer signaling protocol (referred to as Xn Application Protocol (Xn-AP)) and a transport network layer that is built on an SCTP layer. The SCTP layer may be on top of an IP layer. The SCTP layer provides the guaranteed delivery of application layer messages. In the transport IP layer point-to-point transmission is used to deliver the signaling PDUs. In other implementations, the Xn-U protocol stack and/or the Xn-C protocol stack may be same or similar to the user plane and/or control plane protocol stack(s) shown and described herein.

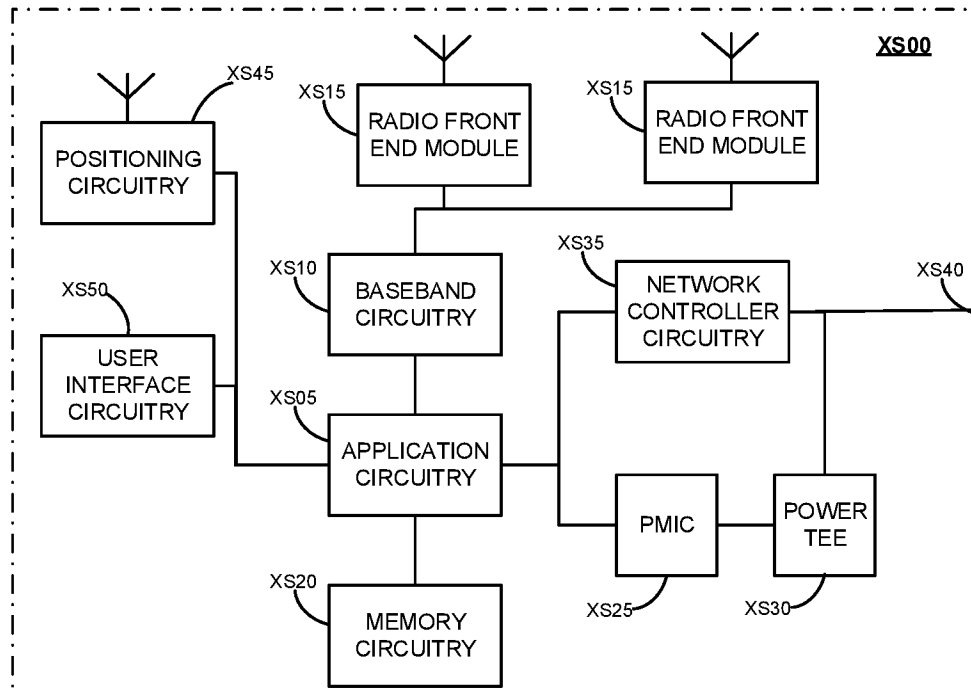
**FIG. XS**

FIG. XS illustrates an example of infrastructure equipment XS00 in accordance with various embodiments. The infrastructure equipment XS00 (or “system XS00”) may be implemented as a base station, radio head, RAN node, etc., such as the RAN nodes XQ11 and XQ12, and/or AP XQ06 shown and described previously. In other examples, the system XS00 could be implemented in or by a UE. The system XS00 may include one or more of application circuitry XS05, baseband circuitry XS10, one or more radio front end modules XS15, memory XS20, power management integrated circuitry (PMIC) XS25, power tee circuitry XS30, network controller XS35, network interface connector XS40, satellite positioning circuitry XS45, and user interface XS50. In some embodiments, the device XT00 may include additional elements such as, for example, memory/storage, display, camera, sensor, or input/output (I/O) interface. In other embodiments, the components described below may be included in more than one device (e.g., said circuitries may be separately included in more than one device for Cloud-RAN (C-RAN) implementations).

As used herein, the term “circuitry” may refer to, is part of, or includes hardware components such as an electronic circuit, a logic circuit, a processor (shared, dedicated, or group) and/or memory (shared, dedicated, or group), an Application Specific Integrated Circuit (ASIC), a field-programmable device (FPD), (for example, a field-programmable gate array (FPGA), a

programmable logic device (PLD), a complex PLD (CPLD), a high-capacity PLD (HCPLD), a structured ASIC, or a programmable System on Chip (SoC)), digital signal processors (DSPs), etc., that are configured to provide the described functionality. In some embodiments, the circuitry may execute one or more software or firmware programs to provide at least some of the described functionality. In addition, the term “circuitry” may also refer to a combination of one or more hardware elements (or a combination of circuits used in an electrical or electronic system) with the program code used to carry out the functionality of that program code. In these embodiments, the combination of hardware elements and program code may be referred to as a particular type of circuitry.

Application circuitry XS05 may include one or more central processing unit (CPU) cores and one or more of cache memory, low drop-out voltage regulators (LDOs), interrupt controllers, serial interfaces such as SPI, I²C or universal programmable serial interface module, real time clock (RTC), timer-counters including interval and watchdog timers, general purpose input/output (I/O or IO), memory card controllers such as Secure Digital (SD)/MultiMediaCard (MMC) or similar, Universal Serial Bus (USB) interfaces, Mobile Industry Processor Interface (MIPI) interfaces and Joint Test Access Group (JTAG) test access ports. As examples, the application circuitry XS05 may include one or more Intel Pentium®, Core®, or Xeon® processor(s); Advanced Micro Devices (AMD) Ryzen® processor(s), Accelerated Processing Units (APUs), or Epyc® processors; and/or the like. In some embodiments, the system XS00 may not utilize application circuitry XS05, and instead may include a special-purpose processor/controller to process IP data received from an EPC or 5GC, for example.

User interface circuitry XS50 may include one or more user interfaces designed to enable user interaction with the system XS00 or peripheral component interfaces designed to enable peripheral component interaction with the system XS00. User interfaces may include, but are not limited to one or more physical or virtual buttons (e.g., a reset button), one or more indicators (e.g., light emitting diodes (LEDs)), a physical keyboard or keypad, a mouse, a touchpad, a touchscreen, speakers or other audio emitting devices, microphones, a printer, a scanner, a headset, a display screen or display device, etc. Peripheral component interfaces may include, but are not limited to, a non-volatile memory port, a universal serial bus (USB) port, an audio jack, a power supply interface, etc.

Additionally or alternatively, application circuitry XS05 may include circuitry such as, but not limited to, one or more a field-programmable devices (FPDs) such as field-programmable gate arrays (FPGAs) and the like; programmable logic devices (PLDs) such as complex PLDs (CPLDs), high-capacity PLDs (HCPLDs), and the like; ASICs such as structured ASICs and the like; programmable SoCs (PSoCs); and the like. In such embodiments, the circuitry of application circuitry XS05 may comprise logic blocks or logic fabric including and other interconnected resources that may be programmed to perform various functions, such as the procedures, methods, functions, etc. of the various embodiments discussed herein. In such embodiments, the circuitry of application circuitry XS05 may include memory cells (e.g., erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), flash memory, static memory (e.g., static random access memory (SRAM), anti-fuses, etc.) used to store logic blocks, logic fabric, data, etc. in lookup-tables (LUTs) and the like.

The baseband circuitry XS10 may be implemented, for example, as a solder-down substrate including one or more integrated circuits, a single packaged integrated circuit soldered to a main circuit board or a multi-chip module containing two or more integrated circuits. Although not shown, baseband circuitry XS10 may comprise one or more digital baseband systems, which may be coupled via an interconnect subsystem to a CPU subsystem, an audio subsystem, and an interface subsystem. The digital baseband subsystems may also be coupled to a digital baseband interface and a mixed-signal baseband sub-system via another interconnect subsystem. Each of the interconnect subsystems may include a bus system, point-to-point connections, network-on-chip (NOC) structures, and/or some other suitable bus or interconnect technology, such as those discussed herein. The audio sub-system may include digital signal processing circuitry, buffer memory, program memory, speech processing accelerator circuitry, data converter circuitry such as analog-to-digital and digital-to-analog converter circuitry, analog circuitry including one or more of amplifiers and filters, and/or other like components. In an aspect of the present disclosure, baseband circuitry XS10 may include protocol processing circuitry with one or more instances of control circuitry (not shown) to provide control functions for the digital baseband circuitry and/or radio frequency circuitry (for example, the radio front end modules XS15).

The radio front end modules (RFEMs) XS15 may comprise a millimeter wave RFEM and one or more sub-millimeter wave radio frequency integrated circuits (RFICs). In some implementations, the one or more sub-millimeter wave RFICs may be physically separated from

the millimeter wave RFEM. The RFICs may include connections to one or more antennas or antenna arrays, and the RFEM may be connected to multiple antennas. In alternative implementations, both millimeter wave and sub-millimeter wave radio functions may be implemented in the same physical radio front end module XS15. The RFEMs XS15 may incorporate both millimeter wave antennas and sub-millimeter wave antennas.

The memory circuitry XS20 may include one or more of volatile memory including dynamic random access memory (DRAM) and/or synchronous dynamic random access memory (SDRAM), and nonvolatile memory (NVM) including high-speed electrically erasable memory (commonly referred to as Flash memory), phase change random access memory (PRAM), magnetoresistive random access memory (MRAM), etc., and may incorporate the three-dimensional (3D) cross-point (XPOINT) memories from Intel® and Micron®. Memory circuitry XS20 may be implemented as one or more of solder down packaged integrated circuits, socketed memory modules and plug-in memory cards.

The PMIC XS25 may include voltage regulators, surge protectors, power alarm detection circuitry, and one or more backup power sources such as a battery or capacitor. The power alarm detection circuitry may detect one or more of brown out (under-voltage) and surge (over-voltage) conditions. The power tee circuitry XS30 may provide for electrical power drawn from a network cable to provide both power supply and data connectivity to the infrastructure equipment XS00 using a single cable.

The network controller circuitry XS35 may provide connectivity to a network using a standard network interface protocol such as Ethernet, Ethernet over GRE Tunnels, Ethernet over Multiprotocol Label Switching (MPLS), or some other suitable protocol. Network connectivity may be provided to/from the infrastructure equipment XS00 using a physical connection, which may be electrical (commonly referred to as a “copper interconnect”), optical, or wireless. The network controller circuitry XS35 may include one or more dedicated processors and/or FPGAs to communicate using one or more of the aforementioned protocol. In some implementations, the network controller circuitry XS35 may include multiple controllers to provide connectivity to other networks using the same or different protocols.

The positioning circuitry XS45, which may include circuitry to receive and decode signals transmitted by one or more navigation satellite constellations of a global navigation satellite system (GNSS). Examples of navigation satellite constellations (or GNSS) may include United States’

Global Positioning System (GPS), Russia's Global Navigation System (GLONASS), the European Union's Galileo system, China's BeiDou Navigation Satellite System, a regional navigation system or GNSS augmentation system (e.g., Navigation with Indian Constellation (NAVIC), Japan's Quasi-Zenith Satellite System (QZSS), France's Doppler Orbitography and Radio-positioning Integrated by Satellite (DORIS), etc.), or the like. The positioning circuitry XS45 may comprise various hardware elements (e.g., including hardware devices such as switches, filters, amplifiers, antenna elements, and the like to facilitate the communications over-the-air (OTA) communications) to communicate with components of a positioning network, such as navigation satellite constellation nodes.

Nodes or satellites of the navigation satellite constellation(s) ("GNSS nodes") may provide positioning services by continuously transmitting or broadcasting GNSS signals along a line of sight, which may be used by GNSS receivers (e.g., positioning circuitry XS45 and/or positioning circuitry implemented by UEs XQ01, XQ02, or the like) to determine their GNSS position. The GNSS signals may include a pseudorandom code (e.g., a sequence of ones and zeros) that is known to the GNSS receiver and a message that includes a time of transmission (ToT) of a code epoch (e.g., a defined point in the pseudorandom code sequence) and the GNSS node position at the ToT. The GNSS receivers may monitor/measure the GNSS signals transmitted/broadcasted by a plurality of GNSS nodes (e.g., four or more satellites) and solve various equations to determine a corresponding GNSS position (e.g., a spatial coordinate). The GNSS receivers also implement clocks that are typically less stable and less precise than the atomic clocks of the GNSS nodes, and the GNSS receivers may use the measured GNSS signals to determine the GNSS receivers' deviation from true time (e.g., an offset of the GNSS receiver clock relative to the GNSS node time). In some embodiments, the positioning circuitry XS45 may include a Micro-Technology for Positioning, Navigation, and Timing (Micro-PNT) IC that uses a master timing clock to perform position tracking/estimation without GNSS assistance.

The GNSS receivers may measure the time of arrivals (ToAs) of the GNSS signals from the plurality of GNSS nodes according to its own clock. The GNSS receivers may determine ToF values for each received GNSS signal from the ToAs and the ToTs, and then may determine, from the ToFs, a three-dimensional (3D) position and clock deviation. The 3D position may then be converted into a latitude, longitude and altitude. The positioning circuitry XS45 may provide data to application circuitry XS05 which may include one or more of position data or time data.

Application circuitry XS05 may use the time data to synchronize operations with other radio base stations (e.g., RAN nodes XQ11, XQ12, XR11 or the like).

The components shown by FIG. XS may communicate with one another using a suitable bus technology, which may include any number of technologies, including industry standard architecture (ISA), extended ISA (EISA), peripheral component interconnect (PCI), peripheral component interconnect extended (PCIx), PCI express (PCIe), or any number of other technologies. The bus may be a proprietary bus, for example, used in a SoC based system. Other bus systems may be included, such as an I²C interface, an SPI interface, point to point interfaces, and a power bus, among others.

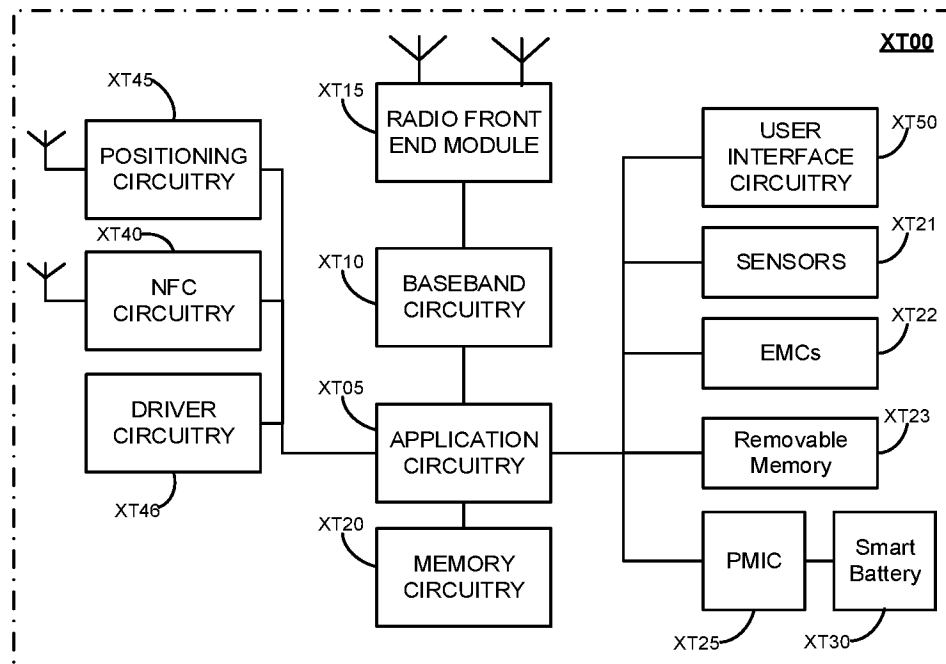


FIG. XT1

FIG. XT1 illustrates an example of a platform XT00 (or "device XT00") in accordance with various embodiments. In embodiments, the computer platform XT01 may be suitable for use as UEs XQ01, XQ02, XR01, application servers XQ30, and/or any other element/device discussed herein. The platform XT00 may include any combinations of the components shown in the example. The components of platform XT00 may be implemented as integrated circuits (ICs), portions thereof, discrete electronic devices, or other modules, logic, hardware, software, firmware, or a combination thereof adapted in the computer platform XT00, or as components

otherwise incorporated within a chassis of a larger system. The block diagram of FIG. XT1 is intended to show a high level view of components of the computer platform XT00. However, some of the components shown may be omitted, additional components may be present, and different arrangement of the components shown may occur in other implementations.

The application circuitry XT05 may include circuitry such as, but not limited to single-core or multi-core processors and one or more of cache memory, low drop-out voltage regulators (LDOs), interrupt controllers, serial interfaces such as serial peripheral interface (SPI), inter-integrated circuit (I²C) or universal programmable serial interface circuit, real time clock (RTC), timer-counters including interval and watchdog timers, general purpose input-output (IO), memory card controllers such as secure digital / multi-media card (SD/MMC) or similar, universal serial bus (USB) interfaces, mobile industry processor interface (MIPI) interfaces and Joint Test Access Group (JTAG) test access ports. The processor(s) may include any combination of general-purpose processors and/or dedicated processors (e.g., graphics processors, application processors, etc.). The processors (or cores) may be coupled with or may include memory/storage and may be configured to execute instructions stored in the memory/storage to enable various applications or operating systems to run on the platform XT00. In some embodiments, processors of application circuitry XS05/XT05 may process IP data packets received from an EPC or 5GC.

Application circuitry XT05 be or include a microprocessor, a multi-core processor, a multithreaded processor, an ultra-low voltage processor, an embedded processor, or other known processing element. In one example, the application circuitry XT05 may include an Intel® Architecture Core™ based processor, such as a Quark™, an Atom™, an i3, an i5, an i7, or an MCU-class processor, or another such processor available from Intel® Corporation, Santa Clara, CA. The processors of the application circuitry XT05 may also be one or more of Advanced Micro Devices (AMD) Ryzen® processor(s) or Accelerated Processing Units (APUs); A5-A9 processor(s) from Apple® Inc., Snapdragon™ processor(s) from Qualcomm® Technologies, Inc., Texas Instruments, Inc.® Open Multimedia Applications Platform (OMAP)™ processor(s); a MIPS-based design from MIPS Technologies, Inc; an ARM-based design licensed from ARM Holdings, Ltd.; or the like. In some implementations, the application circuitry XT05 may be a part of a system on a chip (SoC) in which the application circuitry XT05 and other components are formed into a single integrated circuit, or a single package, such as the Edison™ or Galileo™ SoC boards from Intel® Corporation.

Additionally or alternatively, application circuitry XT05 may include circuitry such as, but not limited to, one or more a field-programmable devices (FPDs) such as FPGAs and the like; programmable logic devices (PLDs) such as complex PLDs (CPLDs), high-capacity PLDs (HCPLDs), and the like; ASICs such as structured ASICs and the like; programmable SoCs (PSoCs); and the like. In such embodiments, the circuitry of application circuitry XT05 may comprise logic blocks or logic fabric including and other interconnected resources that may be programmed to perform various functions, such as the procedures, methods, functions, etc. of the various embodiments discussed herein. In such embodiments, the circuitry of application circuitry XT05 may include memory cells (e.g., erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), flash memory, static memory (e.g., static random access memory (SRAM), anti-fuses, etc.) used to store logic blocks, logic fabric, data, etc. in lookup-tables (LUTs) and the like.

The baseband circuitry XT10 may be implemented, for example, as a solder-down substrate including one or more integrated circuits, a single packaged integrated circuit soldered to a main circuit board or a multi-chip module containing two or more integrated circuits. Although not shown, baseband circuitry XT10 may comprise one or more digital baseband systems, which may be coupled via an interconnect subsystem to a CPU subsystem, an audio subsystem, and an interface subsystem. The digital baseband subsystems may also be coupled to a digital baseband interface and a mixed-signal baseband sub-system via another interconnect subsystem. Each of the interconnect subsystems may include a bus system, point-to-point connections, network-on-chip (NOC) structures, and/or some other suitable bus or interconnect technology, such as those discussed herein. The audio sub-system may include digital signal processing circuitry, buffer memory, program memory, speech processing accelerator circuitry, data converter circuitry such as analog-to-digital and digital-to-analog converter circuitry, analog circuitry including one or more of amplifiers and filters, and/or other like components. In an aspect of the present disclosure, baseband circuitry XT10 may include protocol processing circuitry with one or more instances of control circuitry (not shown) to provide control functions for the digital baseband circuitry and/or radio frequency circuitry (for example, the radio front end modules XT15).

The radio front end modules (RFEMs) XS15 may comprise a millimeter wave RFEM and one or more sub-millimeter wave radio frequency integrated circuits (RFICs). In some implementations, the one or more sub-millimeter wave RFICs may be physically separated from

the millimeter wave RFEM. The RFICs may include connections to one or more antennas or antenna arrays, and the RFEM may be connected to multiple antennas. In alternative implementations, both millimeter wave and sub-millimeter wave radio functions may be implemented in the same physical radio front end module XS15. The RFEMs XS15 may incorporate both millimeter wave antennas and sub-millimeter wave antennas.

The memory circuitry XT20 may include any number and type of memory devices used to provide for a given amount of system memory. As examples, the memory circuitry XT20 may include one or more of volatile memory including be random access memory (RAM), dynamic RAM (DRAM) and/or synchronous dynamic RAM (SDRAM), and nonvolatile memory (NVM) including high-speed electrically erasable memory (commonly referred to as Flash memory), phase change random access memory (PRAM), magnetoresistive random access memory (MRAM), etc. The memory circuitry XT20 may be developed in accordance with a Joint Electron Devices Engineering Council (JEDEC) low power double data rate (LPDDR)-based design, such as LPDDR2, LPDDR3, LPDDR4, or the like. Memory circuitry XS20 may be implemented as one or more of solder down packaged integrated circuits, single die package (SDP), dual die package (DDP) or quad die package (Q17P), socketed memory modules, dual inline memory modules (DIMMs) including microDIMMs or MiniDIMMs, and/or soldered onto a motherboard via a ball grid array (BGA). In low power implementations, the mass storage XQ08 may be on-die memory or registers associated with the application circuitry XT05. To provide for persistent storage of information such as data, applications, operating systems and so forth, memory circuitry XT20 may include one or more mass storage devices , which may include, inter alia, a solid state disk drive (SSDD), hard disk drive (HDD), a micro HDD, resistance change memories, phase change memories, holographic memories, or chemical memories, among others. For example, the computer platform XT00 may incorporate the three-dimensional (3D) cross-point (XPOINT) memories from Intel® and Micron®.

Removable memory circuitry XT23 may include devices, circuitry, enclosures/housings, ports or receptacles, etc. used to coupled portable data storage devices with the platform XT00. These portable data storage devices may be used for mass storage purposes, and may include, for example, flash memory cards (e.g., Secure Digital (SD) cards, microSD cards, xD picture cards, and the like), and USB flash drives, optical discs, external HDDs, and the like.

The platform XT00 may also include interface circuitry (not shown) that is used to connect external devices with the platform XT00. The external devices may include sensors XT21, such as accelerometers, level sensors, flow sensors, temperature sensors, pressure sensors, barometric pressure sensors, and the like. The interface circuitry may be used to connect the platform XT00 to electro-mechanical components (EMCs) XT22, which may allow platform XT00 to change its state, position, and/or orientation, or move or control a mechanism or system. The EMCs XT22 may include one or more power switches, relays including electromechanical relays (EMRs) and/or solid state relays (SSRs), actuators (e.g., valve actuators, etc.), an audible sound generator, a visual warning device, motors (e.g., DC motors, stepper motors, etc.), wheels, thrusters, propellers, claws, clamps, hooks, and/or other like electro-mechanical components. In embodiments, platform XT00 may be configured to operate one or more EMCs XT22 based on one or more captured events and/or instructions or control signals received from a service provider and/or various clients.

In some implementations, the interface circuitry may connect the platform XT00 with positioning circuitry XT45, which may be the same or similar as the positioning circuitry XT45 discussed with regard to FIG. XS.

In some implementations, the interface circuitry may connect the platform XT00 with near-field communication (NFC) circuitry XT40, which may include an NFC controller coupled with an antenna element and a processing device. The NFC circuitry XT40 may be configured to read electronic tags and/or connect with another NFC-enabled device.

The driver circuitry XT46 may include software and hardware elements that operate to control particular devices that are embedded in the platform XT00, attached to the platform XT00, or otherwise communicatively coupled with the platform XT00. The driver circuitry XT46 may include individual drivers allowing other components of the platform XT00 to interact or control various input/output (I/O) devices that may be present within, or connected to, the platform XT00. For example, driver circuitry XT46 may include a display driver to control and allow access to a display device, a touchscreen driver to control and allow access to a touchscreen interface of the platform XT00, sensor drivers to obtain sensor readings of sensors XT21 and control and allow access to sensors XT21, EMC drivers to obtain actuator positions of the EMCs XT22 and/or control and allow access to the EMCs XT22, a camera driver to control and allow access to an

embedded image capture device, audio drivers to control and allow access to one or more audio devices.

The power management integrated circuitry (PMIC) XT25 (also referred to as “power management circuitry XT25”) may manage power provided to various components of the platform XT00. In particular, with respect to the baseband circuitry XT10, the PMIC XT25 may control power-source selection, voltage scaling, battery charging, or DC-to-DC conversion. The PMIC XT25 may often be included when the platform XT00 is capable of being powered by a battery XT30, for example, when the device is included in a UE XS01, XS02, XR01.

In some embodiments, the PMIC XT25 may control, or otherwise be part of, various power saving mechanisms of the platform XT00. For example, if the platform XT00 is in an RRC_Connected state, where it is still connected to the RAN node as it expects to receive traffic shortly, then it may enter a state known as Discontinuous Reception Mode (DRX) after a period of inactivity. During this state, the platform XT00 may power down for brief intervals of time and thus save power. If there is no data traffic activity for an extended period of time, then the platform XT00 may transition off to an RRC_Idle state, where it disconnects from the network and does not perform operations such as channel quality feedback, handover, etc. The platform XT00 goes into a very low power state and it performs paging where again it periodically wakes up to listen to the network and then powers down again. The platform XT00 may not receive data in this state, in order to receive data, it must transition back to RRC_Connected state. An additional power saving mode may allow a device to be unavailable to the network for periods longer than a paging interval (ranging from seconds to a few hours). During this time, the device is totally unreachable to the network and may power down completely. Any data sent during this time incurs a large delay and it is assumed the delay is acceptable.

A battery XT30 may power the platform XT00, although in some examples the platform XT00 may be mounted deployed in a fixed location, and may have a power supply coupled to an electrical grid. The battery XT30 may be a lithium ion battery, a metal-air battery, such as a zinc-air battery, an aluminum-air battery, a lithium-air battery, and the like. In some implementations, such as in V2X applications, the battery XT30 may be a typical lead-acid automotive battery.

In some implementations, the battery XT30 may be a “smart battery,” which includes or is coupled with a Battery Management System (BMS) or battery monitoring integrated circuitry. The BMS may be included in the platform XT00 to track the state of charge (SoCh) of the battery

XT30. The BMS may be used to monitor other parameters of the battery XT30 to provide failure predictions, such as the state of health (SoH) and the state of function (SoF) of the battery XT30. The BMS may communicate the information of the battery XT30 to the application circuitry XT05 or other components of the platform XT00. The BMS may also include an analog-to-digital (ADC) convertor that allows the application circuitry XT05 to directly monitor the voltage of the battery XT30 or the current flow from the battery XT30. The battery parameters may be used to determine actions that the platform XT00 may perform, such as transmission frequency, network operation, sensing frequency, and the like.

A power block, or other power supply coupled to an electrical grid may be coupled with the BMS to charge the battery XT30. In some examples, the power block XQ28 may be replaced with a wireless power receiver to obtain the power wirelessly, for example, through a loop antenna in the computer platform XT00. In these examples, a wireless battery charging circuit may be included in the BMS. The specific charging circuits chosen may depend on the size of the battery XT30, and thus, the current required. The charging may be performed using the Airfuel standard promulgated by the Airfuel Alliance, the Qi wireless charging standard promulgated by the Wireless Power Consortium, or the Rezence charging standard, promulgated by the Alliance for Wireless Power, among others.

Although not shown, the components of platform XT00 may communicate with one another using a suitable bus technology, which may include any number of technologies, including industry standard architecture (ISA), extended ISA (EISA), peripheral component interconnect (PCI), peripheral component interconnect extended (PCIx), PCI express (PCIe), a Time-Trigger Protocol (TTP) system, or a FlexRay system, or any number of other technologies. The bus may be a proprietary bus, for example, used in a SoC based system. Other bus systems may be included, such as an I²C interface, an SPI interface, point to point interfaces, and a power bus, among others.

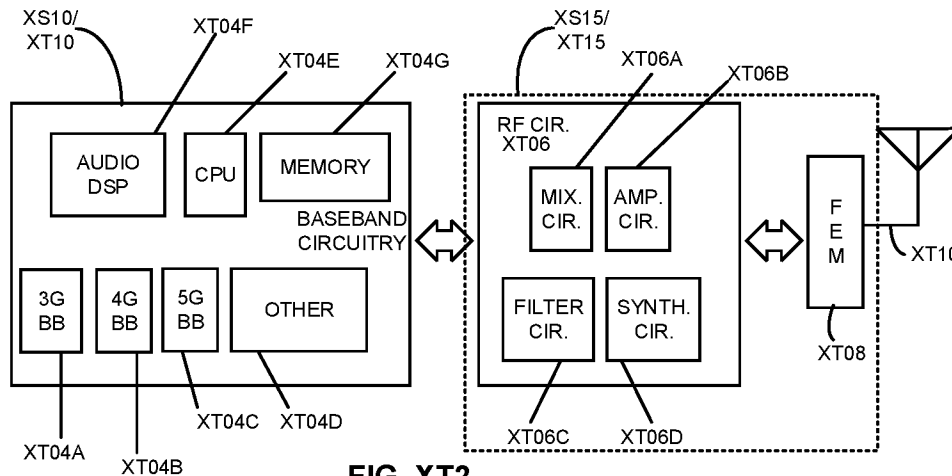
**FIG. XT2**

FIG. XT2 illustrates example components of baseband circuitry XS10/XT10 and radio front end modules (RFEM) XS15/XT15 in accordance with some embodiments. As shown, the RFEM XS15/XT15 may include Radio Frequency (RF) circuitry XT06, front-end module (FEM) circuitry XT08, one or more antennas XT10 coupled together at least as shown.

The baseband circuitry XS10/XT10 may include circuitry such as, but not limited to, one or more single-core or multi-core processors. The baseband circuitry XS10/XT10 may include one or more baseband processors or control logic to process baseband signals received from a receive signal path of the RF circuitry XT06 and to generate baseband signals for a transmit signal path of the RF circuitry XT06. Baseband processing circuitry XS10/XT10 may interface with the application circuitry XS05/XT05 for generation and processing of the baseband signals and for controlling operations of the RF circuitry XT06. For example, in some embodiments, the baseband circuitry XS10/XT10 may include a third generation (3G) baseband processor XT04A, a fourth generation (4G) baseband processor XT04B, a fifth generation (5G) baseband processor XT04C, or other baseband processor(s) XT04D for other existing generations, generations in development or to be developed in the future (e.g., second generation (2G), sixth generation (6G), etc.). The baseband circuitry XS10/XT10 (e.g., one or more of baseband processors XT04A-D) may handle various radio control functions that enable communication with one or more radio networks via the RF circuitry XT06. In other embodiments, some or all of the functionality of baseband processors XT04A-D may be included in modules stored in the memory XT04G and executed via a Central Processing Unit (CPU) XT04E. The radio control functions may include, but are not limited to, signal modulation/demodulation, encoding/decoding, radio frequency shifting, etc. In some embodiments, modulation/demodulation circuitry of the baseband circuitry XS10/XT10 may

include Fast-Fourier Transform (FFT), precoding, or constellation mapping/demapping functionality. In some embodiments, encoding/decoding circuitry of the baseband circuitry XS10/XT10 may include convolution, tail-biting convolution, turbo, Viterbi, or Low Density Parity Check (LDPC) encoder/decoder functionality. Embodiments of modulation/demodulation and encoder/decoder functionality are not limited to these examples and may include other suitable functionality in other embodiments.

In some embodiments, the baseband circuitry XS10/XT10 may include one or more audio digital signal processor(s) (DSP) XT04F. The audio DSP(s) XT04F may include elements for compression/decompression and echo cancellation and may include other suitable processing elements in other embodiments. Components of the baseband circuitry may be suitably combined in a single chip, a single chipset, or disposed on a same circuit board in some embodiments. In some embodiments, some or all of the constituent components of the baseband circuitry XS10/XT10 and the application circuitry XS05/XT05 may be implemented together such as, for example, on a system on a chip (SOC).

In some embodiments, the baseband circuitry XS10/XT10 may provide for communication compatible with one or more radio technologies. For example, in some embodiments, the baseband circuitry XS10/XT10 may support communication with an evolved universal terrestrial radio access network (EUTRAN) or other wireless metropolitan area networks (WMAN), a wireless local area network (WLAN), a wireless personal area network (WPAN). Embodiments in which the baseband circuitry XS10/XT10 is configured to support radio communications of more than one wireless protocol may be referred to as multi-mode baseband circuitry.

RF circuitry XT06 may enable communication with wireless networks using modulated electromagnetic radiation through a non-solid medium. In various embodiments, the RF circuitry XT06 may include switches, filters, amplifiers, etc. to facilitate the communication with the wireless network. RF circuitry XT06 may include a receive signal path which may include circuitry to down-convert RF signals received from the FEM circuitry XT08 and provide baseband signals to the baseband circuitry XS10/XT10. RF circuitry XT06 may also include a transmit signal path which may include circuitry to up-convert baseband signals provided by the baseband circuitry XS10/XT10 and provide RF output signals to the FEM circuitry XT08 for transmission.

In some embodiments, the receive signal path of the RF circuitry XT06 may include mixer circuitry XT06a, amplifier circuitry XT06b and filter circuitry XT06c. In some embodiments, the

transmit signal path of the RF circuitry XT06 may include filter circuitry XT06c and mixer circuitry XT06a. RF circuitry XT06 may also include synthesizer circuitry XT06d for synthesizing a frequency for use by the mixer circuitry XT06a of the receive signal path and the transmit signal path. In some embodiments, the mixer circuitry XT06a of the receive signal path may be configured to down-convert RF signals received from the FEM circuitry XT08 based on the synthesized frequency provided by synthesizer circuitry XT06d. The amplifier circuitry XT06b may be configured to amplify the down-converted signals and the filter circuitry XT06c may be a low-pass filter (LPF) or band-pass filter (BPF) configured to remove unwanted signals from the down-converted signals to generate output baseband signals. Output baseband signals may be provided to the baseband circuitry XS10/XT10 for further processing. In some embodiments, the output baseband signals may be zero-frequency baseband signals, although this is not a requirement. In some embodiments, mixer circuitry XT06a of the receive signal path may comprise passive mixers, although the scope of the embodiments is not limited in this respect.

In some embodiments, the mixer circuitry XT06a of the transmit signal path may be configured to up-convert input baseband signals based on the synthesized frequency provided by the synthesizer circuitry XT06d to generate RF output signals for the FEM circuitry XT08. The baseband signals may be provided by the baseband circuitry XS10/XT10 and may be filtered by filter circuitry XT06c.

In some embodiments, the mixer circuitry XT06a of the receive signal path and the mixer circuitry XT06a of the transmit signal path may include two or more mixers and may be arranged for quadrature downconversion and upconversion, respectively. In some embodiments, the mixer circuitry XT06a of the receive signal path and the mixer circuitry XT06a of the transmit signal path may include two or more mixers and may be arranged for image rejection (e.g., Hartley image rejection). In some embodiments, the mixer circuitry XT06a of the receive signal path and the mixer circuitry XT06a may be arranged for direct downconversion and direct upconversion, respectively. In some embodiments, the mixer circuitry XT06a of the receive signal path and the mixer circuitry XT06a of the transmit signal path may be configured for super-heterodyne operation.

In some embodiments, the output baseband signals and the input baseband signals may be analog baseband signals, although the scope of the embodiments is not limited in this respect. In some alternate embodiments, the output baseband signals and the input baseband signals may be

digital baseband signals. In these alternate embodiments, the RF circuitry XT06 may include analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuitry and the baseband circuitry XS10/XT10 may include a digital baseband interface to communicate with the RF circuitry XT06.

In some dual-mode embodiments, a separate radio IC circuitry may be provided for processing signals for each spectrum, although the scope of the embodiments is not limited in this respect.

In some embodiments, the synthesizer circuitry XT06d may be a fractional-N synthesizer or a fractional $N/N+1$ synthesizer, although the scope of the embodiments is not limited in this respect as other types of frequency synthesizers may be suitable. For example, synthesizer circuitry XT06d may be a delta-sigma synthesizer, a frequency multiplier, or a synthesizer comprising a phase-locked loop with a frequency divider.

The synthesizer circuitry XT06d may be configured to synthesize an output frequency for use by the mixer circuitry XT06a of the RF circuitry XT06 based on a frequency input and a divider control input. In some embodiments, the synthesizer circuitry XT06d may be a fractional $N/N+1$ synthesizer.

In some embodiments, frequency input may be provided by a voltage controlled oscillator (VCO), although that is not a requirement. Divider control input may be provided by either the baseband circuitry XS10/XT10 or the applications processor XS05/XT05 depending on the desired output frequency. In some embodiments, a divider control input (e.g., N) may be determined from a look-up table based on a channel indicated by the applications processor XS05/XT05.

Synthesizer circuitry XT06d of the RF circuitry XT06 may include a divider, a delay-locked loop (DLL), a multiplexer and a phase accumulator. In some embodiments, the divider may be a dual modulus divider (DMD) and the phase accumulator may be a digital phase accumulator (DPA). In some embodiments, the DMD may be configured to divide the input signal by either N or $N+1$ (e.g., based on a carry out) to provide a fractional division ratio. In some example embodiments, the DLL may include a set of cascaded, tunable, delay elements, a phase detector, a charge pump and a D-type flip-flop. In these embodiments, the delay elements may be configured to break a VCO period up into N_d equal packets of phase, where N_d is the number of delay elements in the delay line. In this way, the DLL provides negative feedback to help ensure that the total delay through the delay line is one VCO cycle.

In some embodiments, synthesizer circuitry XT06d may be configured to generate a carrier frequency as the output frequency, while in other embodiments, the output frequency may be a multiple of the carrier frequency (e.g., twice the carrier frequency, four times the carrier frequency) and used in conjunction with quadrature generator and divider circuitry to generate multiple signals at the carrier frequency with multiple different phases with respect to each other. In some embodiments, the output frequency may be a LO frequency (fLO). In some embodiments, the RF circuitry XT06 may include an IQ/polar converter.

FEM circuitry XT08 may include a receive signal path which may include circuitry configured to operate on RF signals received from one or more antennas XT10, amplify the received signals and provide the amplified versions of the received signals to the RF circuitry XT06 for further processing. FEM circuitry XT08 may also include a transmit signal path which may include circuitry configured to amplify signals for transmission provided by the RF circuitry XT06 for transmission by one or more of the one or more antennas XT10. In various embodiments, the amplification through the transmit or receive signal paths may be done solely in the RF circuitry XT06, solely in the FEM XT08, or in both the RF circuitry XT06 and the FEM XT08.

In some embodiments, the FEM circuitry XT08 may include a TX/RX switch to switch between transmit mode and receive mode operation. The FEM circuitry may include a receive signal path and a transmit signal path. The receive signal path of the FEM circuitry may include an LNA to amplify received RF signals and provide the amplified received RF signals as an output (e.g., to the RF circuitry XT06). The transmit signal path of the FEM circuitry XT08 may include a power amplifier (PA) to amplify input RF signals (e.g., provided by RF circuitry XT06), and one or more filters to generate RF signals for subsequent transmission (e.g., by one or more of the one or more antennas XT10).

Processors of the application circuitry XS05/XT05 and processors of the baseband circuitry XS10/XT10 may be used to execute elements of one or more instances of a protocol stack. For example, processors of the baseband circuitry XS10/XT10, alone or in combination, may be used to execute Layer 3, Layer 2, or Layer 1 functionality, while processors of the baseband circuitry XS10/XT10 may utilize data (e.g., packet data) received from these layers and further execute Layer 4 functionality (e.g., transmission communication protocol (TCP) and user datagram protocol (UDP) layers). As referred to herein, Layer 3 may comprise a radio resource control (RRC) layer, described in further detail below. As referred to herein, Layer 2 may comprise a

medium access control (MAC) layer, a radio link control (RLC) layer, and a packet data convergence protocol (PDCP) layer, described in further detail below. As referred to herein, Layer 1 may comprise a physical (PHY) layer of a UE/RAN node, described in further detail below.

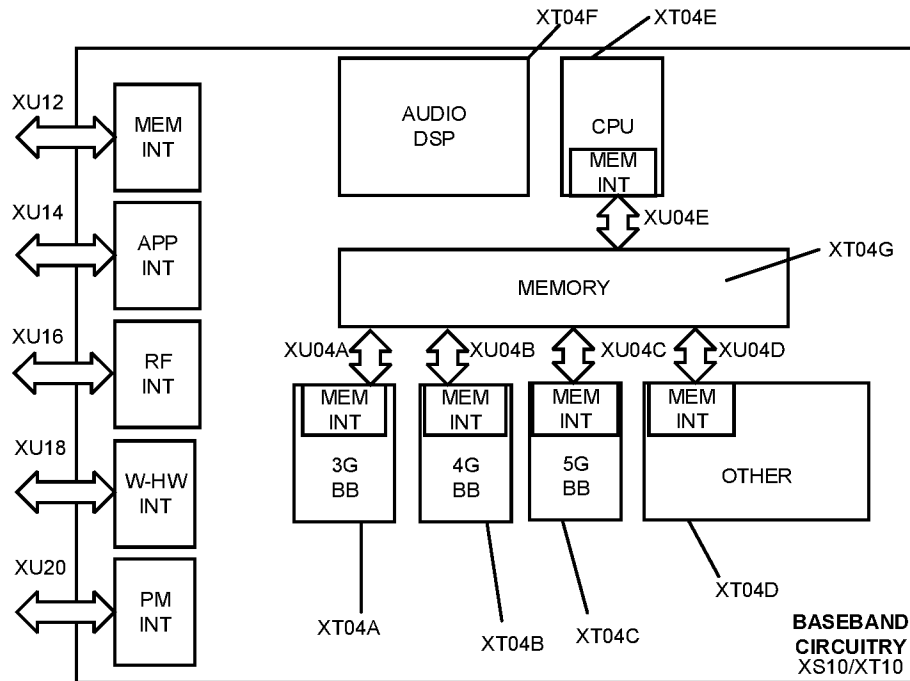


FIG. XU

FIG. XU illustrates example interfaces of baseband circuitry in accordance with some embodiments. As discussed above, the baseband circuitry XS10/XT10 of FIG. XT may comprise processors XT04A-XT04E and a memory XT04G utilized by said processors. Each of the processors XT04A-XT04E may include a memory interface, XU04A-XU04E, respectively, to send/receive data to/from the memory XT04G.

The baseband circuitry XS10/XT10 may further include one or more interfaces to communicatively couple to other circuitries/devices, such as a memory interface XU12 (e.g., an interface to send/receive data to/from memory external to the baseband circuitry XS10/XT10), an application circuitry interface XU14 (e.g., an interface to send/receive data to/from the application circuitry XS05/XT05 of FIG. XT), an RF circuitry interface XU16 (e.g., an interface to send/receive data to/from RF circuitry XT06 of FIG. XT), a wireless hardware connectivity interface XU18 (e.g., an interface to send/receive data to/from Near Field Communication (NFC) components, Bluetooth® components (e.g., Bluetooth® Low Energy), Wi-Fi® components, and other communication components), and a power management interface XU20 (e.g., an interface to send/receive power or control signals to/from the PMIC XT25).

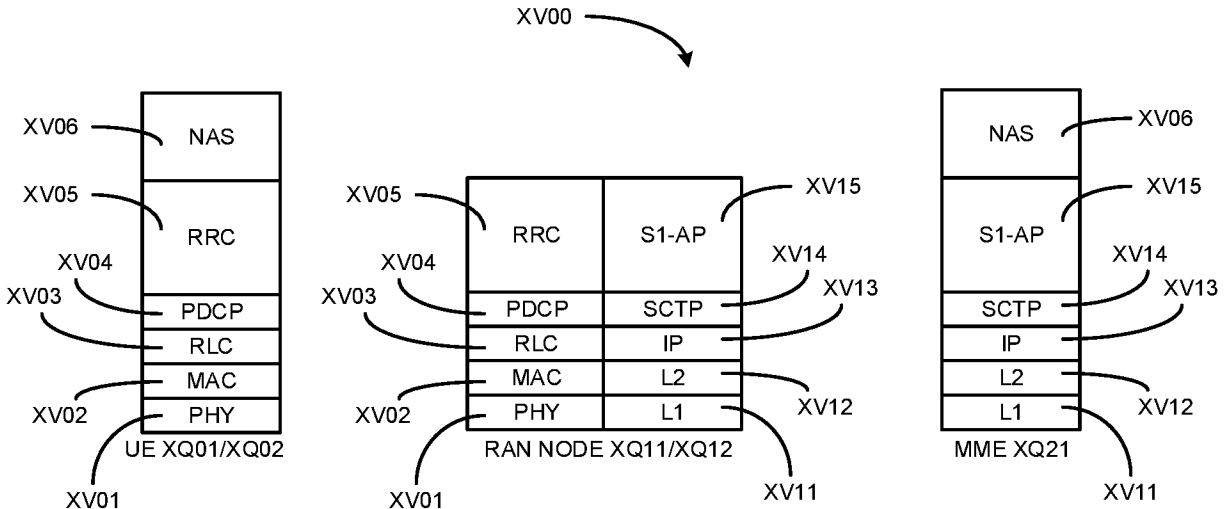


FIG. XV

FIG. XV is an illustration of a control plane protocol stack in accordance with some embodiments. In this embodiment, a control plane XV00 is shown as a communications protocol stack between the UE XQ01 (or alternatively, the UE XQ02), the RAN node XQ11 (or alternatively, the RAN node XQ12), and the MME XQ21.

The PHY layer XV01 may transmit or receive information used by the MAC layer XV02 over one or more air interfaces. The PHY layer XV01 may further perform link adaptation or adaptive modulation and coding (AMC), power control, cell search (e.g., for initial synchronization and handover purposes), and other measurements used by higher layers, such as the RRC layer XV05. The PHY layer XV01 may still further perform error detection on the transport channels, forward error correction (FEC) coding/decoding of the transport channels, modulation/demodulation of physical channels, interleaving, rate matching, mapping onto physical channels, and Multiple Input Multiple Output (MIMO) antenna processing.

The MAC layer XV02 may perform mapping between logical channels and transport channels, multiplexing of MAC service data units (SDUs) from one or more logical channels onto transport blocks (TB) to be delivered to PHY via transport channels, de-multiplexing MAC SDUs to one or more logical channels from transport blocks (TB) delivered from the PHY via transport channels, multiplexing MAC SDUs onto TBs, scheduling information reporting, error correction through hybrid automatic repeat request (HARQ), and logical channel prioritization.

The RLC layer XV03 may operate in a plurality of modes of operation, including: Transparent Mode (TM), Unacknowledged Mode (UM), and Acknowledged Mode (AM). The RLC layer XV03 may execute transfer of upper layer protocol data units (PDUs), error correction

through automatic repeat request (ARQ) for AM data transfers, and concatenation, segmentation and reassembly of RLC SDUs for UM and AM data transfers. The RLC layer XV03 may also execute re-segmentation of RLC data PDUs for AM data transfers, reorder RLC data PDUs for UM and AM data transfers, detect duplicate data for UM and AM data transfers, discard RLC SDUs for UM and AM data transfers, detect protocol errors for AM data transfers, and perform RLC re-establishment.

The PDCP layer XV04 may execute header compression and decompression of IP data, maintain PDCP Sequence Numbers (SNs), perform in-sequence delivery of upper layer PDUs at re-establishment of lower layers, eliminate duplicates of lower layer SDUs at re-establishment of lower layers for radio bearers mapped on RLC AM, cipher and decipher control plane data, perform integrity protection and integrity verification of control plane data, control timer-based discard of data, and perform security operations (e.g., ciphering, deciphering, integrity protection, integrity verification, etc.).

The main services and functions of the RRC layer XV05 may include broadcast of system information (e.g., included in Master Information Blocks (MIBs) or System Information Blocks (SIBs) related to the non-access stratum (NAS)), broadcast of system information related to the access stratum (AS), paging, establishment, maintenance and release of an RRC connection between the UE and E-UTRAN (e.g., RRC connection paging, RRC connection establishment, RRC connection modification, and RRC connection release), establishment, configuration, maintenance and release of point to point Radio Bearers, security functions including key management, inter radio access technology (RAT) mobility, and measurement configuration for UE measurement reporting. Said MIBs and SIBs may comprise one or more information elements (IEs), which may each comprise individual data fields or data structures.

The UE XQ01 and the RAN node XQ11 may utilize a Uu interface (e.g., an LTE-Uu interface) to exchange control plane data via a protocol stack comprising the PHY layer XV01, the MAC layer XV02, the RLC layer XV03, the PDCP layer XV04, and the RRC layer XV05.

The non-access stratum (NAS) protocols XV06 form the highest stratum of the control plane between the UE XQ01 and the MME XQ21. The NAS protocols XV06 support the mobility of the UE XQ01 and the session management procedures to establish and maintain IP connectivity between the UE XQ01 and the P-GW XQ23.

The S1 Application Protocol (S1-AP) layer XV15 may support the functions of the S1 interface and comprise Elementary Procedures (EPs). An EP is a unit of interaction between the RAN node XQ11 and the CN XQ20. The S1-AP layer services may comprise two groups: UE-associated services and non UE-associated services. These services perform functions including, but not limited to: E-UTRAN Radio Access Bearer (E-RAB) management, UE capability indication, mobility, NAS signaling transport, RAN Information Management (RIM), and configuration transfer.

The Stream Control Transmission Protocol (SCTP) layer (alternatively referred to as the SCTP/IP layer) XV14 may ensure reliable delivery of signaling messages between the RAN node XQ11 and the MME XQ21 based, in part, on the IP protocol, supported by the IP layer XV13. The L2 layer XV12 and the L1 layer XV11 may refer to communication links (e.g., wired or wireless) used by the RAN node and the MME to exchange information.

The RAN node XQ11 and the MME XQ21 may utilize an S1-MME interface to exchange control plane data via a protocol stack comprising the L1 layer XV11, the L2 layer XV12, the IP layer XV13, the SCTP layer XV14, and the S1-AP layer XV15.

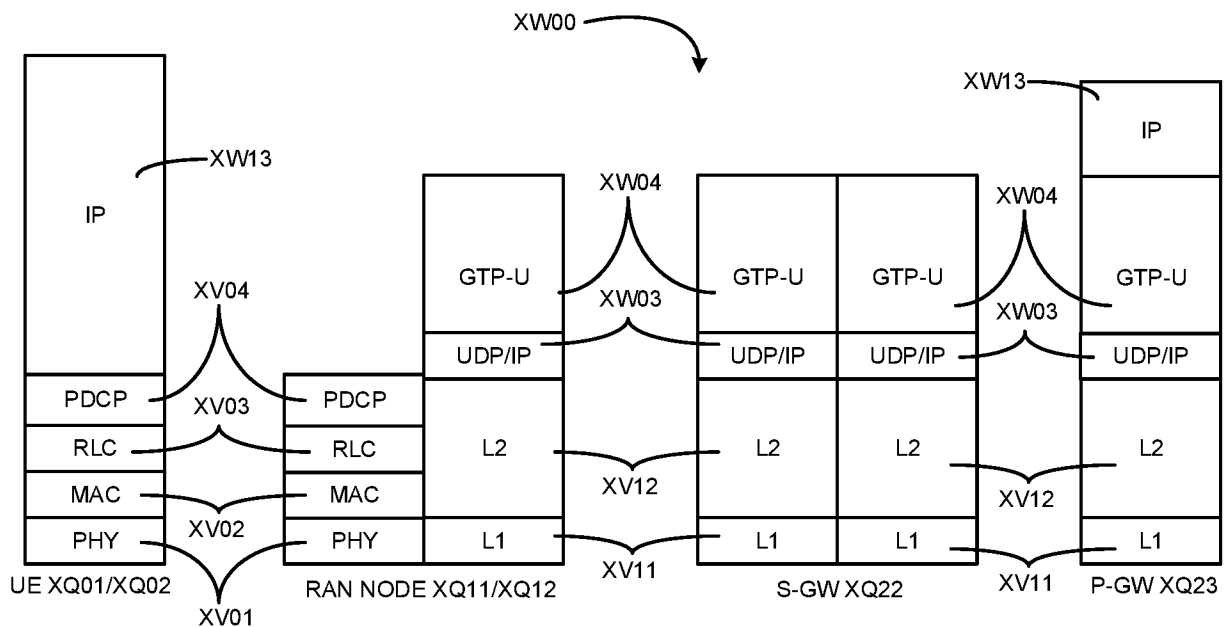


FIG. XW

FIG. XW is an illustration of a user plane protocol stack in accordance with some embodiments. In this embodiment, a user plane XW00 is shown as a communications protocol stack between the UE XQ01 (or alternatively, the UE XQ02), the RAN node XQ11 (or

alternatively, the RAN node XQ12), the S-GW XQ22, and the P-GW XQ23. The user plane XW00 may utilize at least some of the same protocol layers as the control plane XV00. For example, the UE XQ01 and the RAN node XQ11 may utilize a Uu interface (e.g., an LTE-Uu interface) to exchange user plane data via a protocol stack comprising the PHY layer XV01, the MAC layer XV02, the RLC layer XV03, the PDCP layer XV04.

The General Packet Radio Service (GPRS) Tunneling Protocol for the user plane (GTP-U) layer XW04 may be used for carrying user data within the GPRS core network and between the radio access network and the core network. The user data transported can be packets in any of IPv4, IPv6, or PPP formats, for example. The UDP and IP security (UDP/IP) layer XW03 may provide checksums for data integrity, port numbers for addressing different functions at the source and destination, and encryption and authentication on the selected data flows. The RAN node XQ11 and the S-GW XQ22 may utilize an S1-U interface to exchange user plane data via a protocol stack comprising the L1 layer XV11, the L2 layer XV12, the UDP/IP layer XW03, and the GTP-U layer XW04. The S-GW XQ22 and the P-GW XQ23 may utilize an S5/S8a interface to exchange user plane data via a protocol stack comprising the L1 layer XV11, the L2 layer XV12, the UDP/IP layer XW03, and the GTP-U layer XW04. As discussed above with respect to FIG. XV, NAS protocols support the mobility of the UE XQ01 and the session management procedures to establish and maintain IP connectivity between the UE XQ01 and the P-GW XQ23.

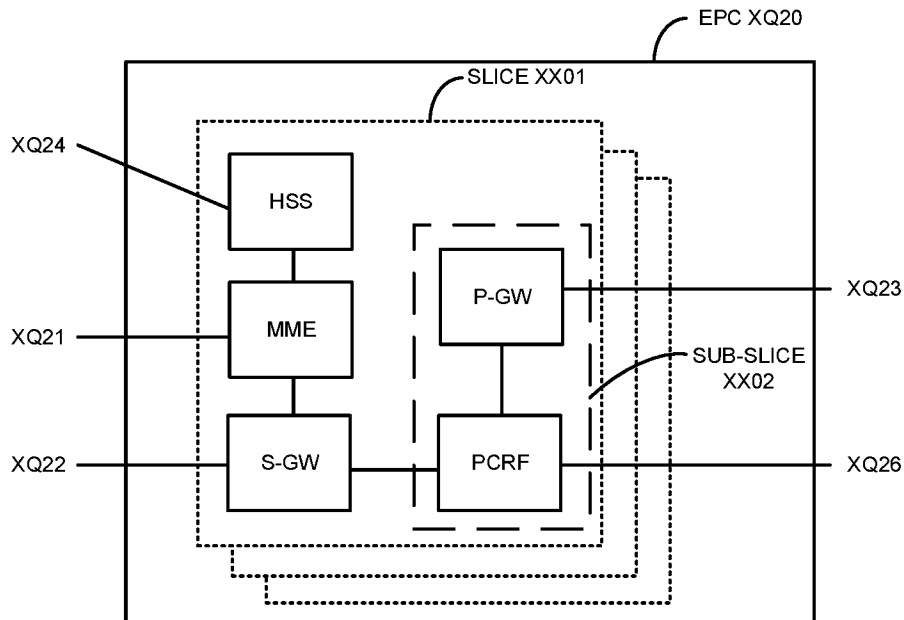


FIG. XX

FIG. XX illustrates components of a core network in accordance with some embodiments. The components of the CN XQ20 may be implemented in one physical node or separate physical nodes including components to read and execute instructions from a machine-readable or computer-readable medium (e.g., a non-transitory machine-readable storage medium). In embodiments, the components of CN XR20 may be implemented in a same or similar manner as discussed herein with regard to the components of CN XQ20. In some embodiments, Network Functions Virtualization (NFV) is utilized to virtualize any or all of the above described network node functions via executable instructions stored in one or more computer readable storage mediums (described in further detail below). A logical instantiation of the CN XQ20 may be referred to as a network slice XX01. A logical instantiation of a portion of the CN XQ20 may be referred to as a network sub-slice XX02 (e.g., the network sub-slice XX02 is shown to include the PGW XQ23 and the PCRF XQ26).

NFV architectures and infrastructures may be used to virtualize one or more network functions, alternatively performed by proprietary hardware, onto physical resources comprising a combination of industry-standard server hardware, storage hardware, or switches. In other words, NFV systems can be used to execute virtual or reconfigurable implementations of one or more EPC components/functions.

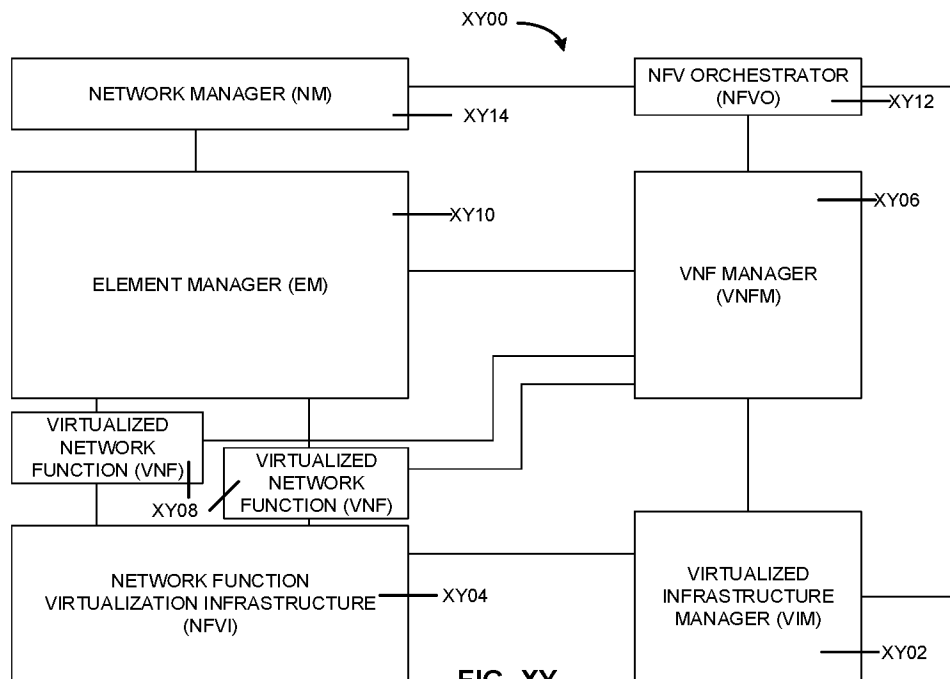


FIG. XY

FIG. XY is a block diagram illustrating components, according to some example embodiments, of a system XY00 to support NFV. The system XY00 is illustrated as including a virtualized infrastructure manager (VIM) XY02, a network function virtualization infrastructure (NFVI) XY04, a VNF manager (VNFM) XY06, virtualized network functions (VNFs) XY08, an element manager (EM) XY10, an NFV Orchestrator (NFVO) XY12, and a network manager (NM) XY14.

The VIM XY02 manages the resources of the NFVI XY04. The NFVI XY04 can include physical or virtual resources and applications (including hypervisors) used to execute the system XY00. The VIM XY02 may manage the life cycle of virtual resources with the NFVI XY04 (e.g., creation, maintenance, and tear down of virtual machines (VMs) associated with one or more physical resources), track VM instances, track performance, fault and security of VM instances and associated physical resources, and expose VM instances and associated physical resources to other management systems.

The VNFM XY06 may manage the VNFs XY08. The VNFs XY08 may be used to execute EPC components/functions. The VNFM XY06 may manage the life cycle of the VNFs XY08 and track performance, fault and security of the virtual aspects of VNFs XY08. The EM XY10 may track the performance, fault and security of the functional aspects of VNFs XY08. The tracking data from the VNFM XY06 and the EM XY10 may comprise, for example, performance measurement (PM) data used by the VIM XY02 or the NFVI XY04. Both the VNFM XY06 and the EM XY10 can scale up/down the quantity of VNFs of the system XY00.

The NFVO XY12 may coordinate, authorize, release and engage resources of the NFVI XY04 in order to provide the requested service (e.g., to execute an EPC function, component, or slice). The NM XY14 may provide a package of end-user functions with the responsibility for the management of a network, which may include network elements with VNFs, non-virtualized network functions, or both (management of the VNFs may occur via the EM XY10).

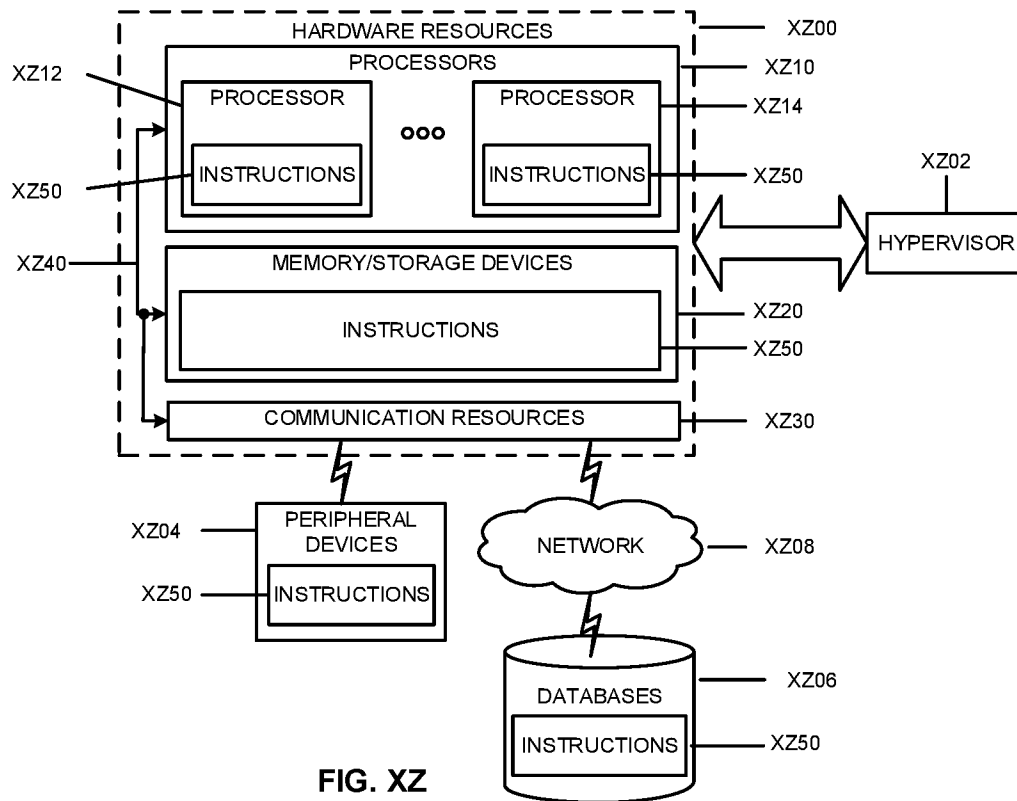


FIG. XZ

FIG. XZ is a block diagram illustrating components, according to some example embodiments, able to read instructions from a machine-readable or computer-readable medium (e.g., a non-transitory machine-readable storage medium) and perform any one or more of the methodologies discussed herein. Specifically, FIG. XZ shows a diagrammatic representation of hardware resources XZ00 including one or more processors (or processor cores) XZ10, one or more memory/storage devices XZ20, and one or more communication resources XZ30, each of which may be communicatively coupled via a bus XZ40. For embodiments where node virtualization (e.g., NFV) is utilized, a hypervisor XZ02 may be executed to provide an execution environment for one or more network slices/sub-slices to utilize the hardware resources XZ00

The processors XZ10 (e.g., a central processing unit (CPU), a reduced instruction set computing (RISC) processor, a complex instruction set computing (CISC) processor, a graphics processing unit (GPU), a digital signal processor (DSP) such as a baseband processor, an application specific integrated circuit (ASIC), a radio-frequency integrated circuit (RFIC), another processor, or any suitable combination thereof) may include, for example, a processor XZ12 and a processor XZ14.

The memory/storage devices XZ20 may include main memory, disk storage, or any suitable combination thereof. The memory/storage devices XZ20 may include, but are not limited to any type of volatile or non-volatile memory such as dynamic random access memory (DRAM), static random-access memory (SRAM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), Flash memory, solid-state storage, etc.

The communication resources XZ30 may include interconnection or network interface components or other suitable devices to communicate with one or more peripheral devices XZ04 or one or more databases XZ06 via a network XZ08. For example, the communication resources XZ30 may include wired communication components (e.g., for coupling via a Universal Serial Bus (USB)), cellular communication components, NFC components, Bluetooth® components (e.g., Bluetooth® Low Energy), Wi-Fi® components, and other communication components.

Instructions XZ50 may comprise software, a program, an application, an applet, an app, or other executable code for causing at least any of the processors XZ10 to perform any one or more of the methodologies discussed herein. The instructions XZ50 may reside, completely or partially, within at least one of the processors XZ10 (e.g., within the processor's cache memory), the memory/storage devices XZ20, or any suitable combination thereof. Furthermore, any portion of the instructions XZ50 may be transferred to the hardware resources XZ00 from any combination of the peripheral devices XZ04 or the databases XZ06. Accordingly, the memory of processors XZ10, the memory/storage devices XZ20, the peripheral devices XZ04, and the databases XZ06 are examples of computer-readable and machine-readable media.

In some embodiments, the electronic device(s), network(s), system(s), chip(s) or component(s), or portions or implementations thereof, of any figure herein may be configured to perform one or more processes, techniques, or methods as described herein, or portions thereof.

EXAMPLES

Example 1 may include a method of wireless communication for a fifth generation (5G) or new radio (NR) system comprising one or more of the following:

a time-domain resource allocation for PDSCH or PUSCH is determined using a combination of higher layer and DCI based signaling; and

collisions and conflict resolution between different UL physical channels or signals are resolved by dropping or postponing of one of the collided channels or signals.

Example 2 may include the method of example 1 and/or some other examples herein, wherein the starting symbol and length of the PDSCH/PUSCH for a row of the RRC-configured table is determined as a function of the PDSCH/PUSCH mapping type for that row.

Example 3 may include the method of example 1 and/or some other examples herein, wherein the slot index indication (K0 and K2 values) for a row of the RRC-configured table is determined as a function of the PDSCH/PUSCH mapping type for that row.

Example 4 may include the method of example 2 and/or some other examples herein, wherein a 5-bit or 6-bit table is defined in specifications – one each for mapping types A and B, to indicate the candidate combinations of starting symbol and length of the PDSCH/PUSCH to construct the RRC-configured table.

Example 5 may include the method of example 1 and/or some other examples herein, wherein for PDSCH/PUSCH mapping type B (non-slot or mini-slot-based transmission), if aggregation is configured, the dynamically indicated SLIV-based resource allocation or semi-statically derived start and duration (in case of semi-persistent allocation) is repeated in consecutive K groups of valid symbols, where K is the aggregation factor configured by RRC.

Example 6 may include the method of example 1 and/or some other examples herein, wherein in case a group of symbols in an aggregated multi-mini-slot transmission, i.e. aggregated PUSCH transmission of mapping type B, is going to cross the slot boundary, the transmission is postponed i.e. shifted in time to the first valid symbol in the next slot relative to the slot where the previous group of symbols was mapped.

Example 7 may include the method of example 1 and/or some other examples herein, wherein if the dynamic or semi-static time-domain resource allocation indicates resources which overlapped with SRS resources, the group(s) of PUSCH symbols fully or partially overlapped with SRS resources are not transmitted.

Example 8 may include the method of example 1 and/or some other examples herein, wherein UE does not transmit SRS when semi-persistent and periodic SRS are configured in the same symbol(s) with uplink transmission which is semi-statically or semi-persistently configured.

Example 9 may include the method of example 1 and/or some other examples herein, wherein UE does not transmit uplink transmission which is semi-statically or semi-persistently configured when aperiodic SRS happens to overlap in the same symbol with transmit uplink transmission which is semi-statically or semi-persistently configured.

Example 10 may include the method of example 1 and/or some other examples herein, wherein the dropping rule or priority rule may depend on transmission duration or type of uplink transmission.

Example 11 may include an apparatus comprising means to perform one or more elements of a method described in or related to any of examples 1-10, or any other method or process described herein.

Example 12 may include one or more non-transitory computer-readable media comprising instructions to cause an electronic device, upon execution of the instructions by one or more processors of the electronic device, to perform one or more elements of a method described in or related to any of examples 1-10, or any other method or process described herein.

Example 13 may include an apparatus comprising logic, modules, or circuitry to perform one or more elements of a method described in or related to any of examples 1-10, or any other method or process described herein.

Example 14 may include a method, technique, or process as described in or related to any of examples 1-10, or portions or parts thereof.

Example 15 may include an apparatus comprising: one or more processors and one or more computer readable media comprising instructions that, when executed by the one or more processors, cause the one or more processors to perform the method, techniques, or process as described in or related to any of examples 1-10, or portions thereof.

Example 16 may include a signal as described in or related to any of examples 1-10, or portions or parts thereof.

Example 17 may include a signal in a wireless network as shown and described herein.

Example 18 may include a method of communicating in a wireless network as shown and described herein.

Example 18 may include a system for providing wireless communication as shown and described herein.

Example 19 may include a device for providing wireless communication as shown and described herein.

Any of the above described examples may be combined with any other example (or combination of examples), unless explicitly stated otherwise. The foregoing description of one or more implementations provides illustration and description, but is not intended to be exhaustive or to limit the scope of embodiments to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of various embodiments.

Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	TIME DOMAIN RESOURCE ALLOCATION AND SOFT BUFFER HANDLING IN NEW RADIO (NR)			
First Named Inventor/Applicant Name:	Debdeep Chatterjee			
Filer:	Ryan Nathan Strauss/Brandi Henley			
Attorney Docket Number:	111027-AA7997-Z			
Filed as Large Entity				
Filing Fees for Provisional				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
PROVISIONAL APPLICATION FILING	1005	1	260	260
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				260

Electronic Acknowledgement Receipt

EFS ID:	31495453
Application Number:	62617106
International Application Number:	
Confirmation Number:	2837
Title of Invention:	TIME DOMAIN RESOURCE ALLOCATION AND SOFT BUFFER HANDLING IN NEW RADIO (NR)
First Named Inventor/Applicant Name:	Debdeep Chatterjee
Customer Number:	31817
Filer:	Ryan Nathan Strauss/Brandi Henley
Filer Authorized By:	Ryan Nathan Strauss
Attorney Docket Number:	111027-AA7997-Z
Receipt Date:	12-JAN-2018
Filing Date:	
Time Stamp:	20:03:41
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$260
RAM confirmation Number	011618INTEFSW00007590500393
Deposit Account	500393
Authorized User	Brandi Henley

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

Petitioners' Exhibit 1013, p. 62
AT&T et al v. Asustek Computer
IPR2024-00992

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Provisional Cover Sheet (SB16)	IDFAA7997_Provisional_Cover_Sheet.pdf	1477290	no	4
			197a29927725d2f65cc0df0fe692de69d5ef8784		

Warnings:**Information:**

2	Specification	IDFAA7797_Provisional_Application.pdf	537995	no	52
			9d9526041d163c4427bec2c42167d6e57da169bc		

Warnings:**Information:**

3	Fee Worksheet (SB06)	fee-info.pdf	30142	no	2
			24f09bc11bb5a45be111f4b26c13fce5a1ea19a		

Warnings:**Information:**

Total Files Size (in bytes):			2045427
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.