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Research Note

Determination of the dice forward I–V characteristics of a power diode from a packaged device and its applications

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Abstract

The forward voltage drop (V_F) of a power diode is an important electrical parameter for a power diode. Diode with excessive V_F can be due to either defects in wafer fabrication or soldering processes. To identify if the defects in soldering process is the root cause to excessive V_F, the obvious method will be the method to extract the series resistance from the diode. However, the present series resistance extraction methods are either inaccurate or requires extensive computation time, and they are not practical for failure analysis and process monitoring. In this work, a modified series resistance extraction method is developed. Experimental results showed that the modified method is accurate, and the computation time is short.
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1. Introduction

High power diode is an essential component in power electronic circuits. Among the various electrical parameters of a power diode, forward voltage drop (V_F) of a high power diode is an importance parameter because it affects the static power loss during conduction. The factors that determine V_F in power diode can be classified as wafer fabrication and assembly related. The Wafer Fabrication related factors include the carrier lifetime in the base region [1], base width [1], p+/n+ diffusion concentrations [2] and the area of the dice that in turn affect the current density. The Assembly related factors include the solder integrity, such as solder voids, solder resistance, solder coverage, and lead frame resistance because these parameters introduce series resistance to the power diode, and hence increases the V_F at a given current as illustrated in Fig. 1. The effect of series resistance on V_F is more significant for power diode with higher current rating as can be seen in Fig. 1.

Therefore, when a power diode is found to have excessive V_F, it is difficult to pin point if the failure mechanism is due to assembly or wafer fabrication related defects. Even if the dice is taken out from the package through decapsulation, the contact resistance of the probes on the dice could also increase the actual V_F of the dice due to the probes' contact resistances. If Kelvin probe is used to eliminate the contact resistance, the extreme small contact area of each probe head to the dice could bring current filamentation at high current measurement as shown by Blonskis et al. [3]. This current filamentation is the results of highly non-uniform injected carriers with high concentration into the devices [4]. The current filamentation leads to excessive V_F for a given forward current as shown by Barnett [4].

Furthermore, decapsulation is a destructive failure analysis method, and with this method, it is hard to find the root cause if assembly defects are indeed the reason for excessive V_F. Therefore, soft X-ray is being used for the study of the possible assembly related defects before decapsulation. However, this is not practical in production as the production lot size tend to be very large for power diode.

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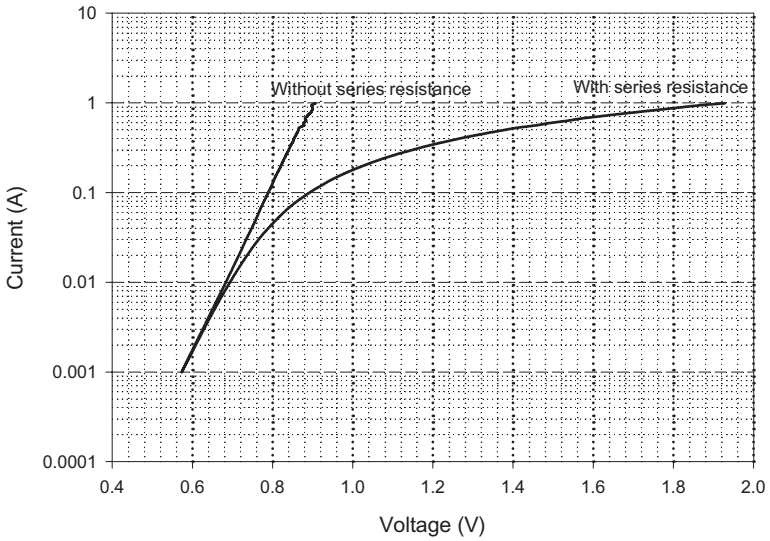


Fig. 1. Experimental data illustrating the effect of serials resistance on the forward I–V characteristics of a Power Diode 1N4007. Y-axis is $\ln(I)$, and x-axis is V.

One method to overcome the above-mentioned problem is to determine the dice forward I–V curve from a packaged power diode. This can be done if the series resistance introduced by the packaging can be determined.

Many methods [5–10] have been presented to extract the series resistance of a package diode. Norde [6] and Lee et al. [8] presented the method for Schottky diode which is not the focus of this work. Banwell and Jayakumar [10] and Jain and Kapoor [11] employed the Lambert W-function for the estimation of the series resistance. However, iteration is required, though the function has a rapid convergence. Ortiz-Conde et al. [5] used direct optimization from the I–V characteristics of a diode to extract the series resistance, and again iteration is needed. Garcia et al. [7] constructed a new function that allows the determination of the series resistance, and recently, Ranuarez et al. [9] extended the application of the function to extract both the series and parallel parasitic resistances. The new function is given as follows, independent of the value of the series parasitic resistance [7,9]

$$G(I,V) \equiv \frac{IV - 2\int_0^V I'\,\mathrm{d}V'}{I} \approx nV_{\mathrm{th}}\left(\ln\left(\frac{I}{I_{\mathrm{s}}}\right) - 2\right), \qquad (1)$$

where n is the ideality factor, I_{s} is the saturation current, and V_{th} is the thermal voltage. Thus, a plot of $G(I,V)$ vs. $\ln(I)$ should produce a straight line, and from the plot, n and I_{s} can be determined, and hence the dice V_{F} can be determined [7,9].

In deriving Eq. (1), the ideality factor is assumed to be constant. However, for power diode of medium and high current rating, the ideality factor changes with current as the injection level changes from low to high during forward bias. In this work, the effect of this changing ideality factor on the accuracy of the method presented by Ortiz-Conde et al. [5] and Ranuarez et al. [9] will be studied, and modification of the method will be introduced. The accuracy of the modified method will be verified experimentally in this work.

2. Accuracy of the existing methods

In order to verify the above-mentioned methods, a 1 A power diode, 1N4007 is used. Five precision resistors of known resistance values are connected in series to the diode, one at a time. The resistances used in this work are 0.05, 0.1, 0.5, 1.0 and 1.5 Ω. The series resistance of the diode plus the external resistor is computed from the measured forward I–V curve using the methods. The forward I–V curve of the power diode is obtained with the precautious to avoid heating of the junction as V_{F} is sensitive to the junction temperature. This is achieved by using a pulsed forward current.

If the methods are accurate, a plot of the computed series resistance vs. the external resistance should produce a straight line of slope equal to 1, and the intercept to the y-axis will be the intrinsic series resistance of the power diode. Fig. 2a shows the plot for the five resistors used. One can see that the slope is less than 1, and the intrinsic series resistance computed is a negative value, which is not possible. Also, not all the data points fall onto a straight line.

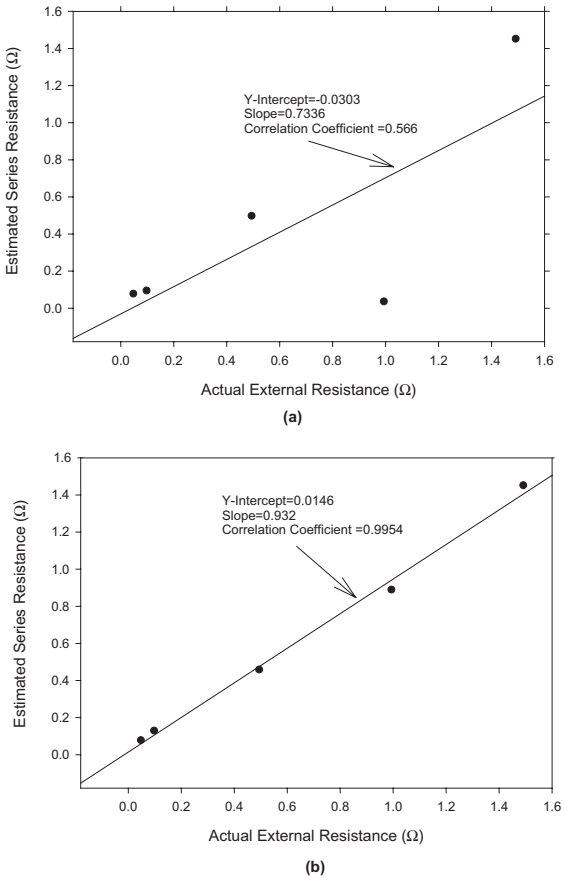


Fig. 2. Resistance plot using existing methods: (a) for the entire region of current in the $G(I,V)$ plot; (b) after the removal of the oscillation portion in the $G(I,V)$ plot.

Upon careful examination of the $G(I,V)$ vs. $\ln(I)$ plot as shown in Fig. 3 for an external series resistor of 1 Ω, one could identify some oscillations at the top as circled. If the current window is selected from zero current up to the lower bound of the oscillation, the oscillation region is eliminated, and one obtained the plot as shown in Fig. 2b. Now, most of the data points fall on a straight line, and its value seems reasonable. However, the slope of the straight line is still not close to 1, which indicate some doubt to its accuracy. In fact, from the non-linearity of the $G(I,V)$ vs. $\ln(I)$ plot in Fig. 3, its correctness in computing the series resistance is doubtful based on Eq. (1).

Ranuarez et al. [9] explained the non-linearity of the plot to be due to the presence of a shunt parasitic resistance R_{sh} which could represents the leakage path through the passivation of a power diode. They estimated the shunt resistance by adjusting the value of R_{sh} till the plot is a straight line. However, the shunt resistance will affect the forward I–V curve only at very low current as can be shown below.

If a diode has both the series and shunt parasitic resistances as shown in Fig. 4, which is extracted from [9], we have

$$\begin{aligned} I &= I_s e^{V_D/(nV_T)} + \frac{V}{R_{sh}}, \\ V_D &= V - I_D R_s, \\ I_D &= I_s e^{V_D/(nV_T)}. \end{aligned} \tag{2}$$

Hence, the function $G(I,V)$ will need to be modified as

$$G(I,V) = \frac{IV - 2\int_0^V I'\,dV'}{I - V/R_{sh}} = nV_T\left(\ln\frac{I_D}{I_s} - 2\right). \tag{3}$$

Comparing Eq. (3) with Eq. (1), one can see a modification in the denominator. Since R_{sh} is usually large, and V is small for forward voltage, V/R_{sh} is a very small value, and its effect can be felt only if I is very small as well. For the case shown in Fig. 3, at $I = 0.015$ A, which is in the non-linear region of the $G(I,V)$ plot, the corresponding forward voltage is 0.718 V. If R_{sh} is assumed to be 1 MΩ, a very low value indeed, $V/R_{sh} = 7.18 \times 10^{-7}$ A, one can see that the effect of V/R_{sh} cannot be felt when compared to 0.015 A. Hence, the non-linearity is unlikely to be due to the presence of R_{sh}.

Upon careful examination of the derivation of Eq. (1), we found that the ideality factor is assumed to be a constant in the forward current region considered, from zero current onward. This might be true for small signal diode. However, for power diode, the injection will go from low to high-level injection as mentioned earlier. Hence, the ideality factor is not a constant [12]. Thus, the integration limit in Eq. (1) cannot start from zero unless the upper limit is low enough to keep the entire operation in low level injection. But then the effect of R_{sh} has to be considered as Ranuarez et al. [9] did.

Since n varies from 1 to 2 in power diode as its operating current varies from very low to high, we can split the current operation region of a power diode into three regions, namely the very low current region (region 1), medium current region (region 2) and high current region (region 3). In region 1, $n = 1$; in region 3, $n = 2$; and in region 2, n varies. The three regions are also reflected in the plot of $G(I,V)$ vs. $\ln(I)$ plot as shown in Fig. 3, as the slope of the plot is proportional to the value of n. Therefore, if either region 1 or 3 is chosen for the computation of the $G(I,V)$ function, we should expect a straight line which will then provide the value of the series resistance.

To avoid the influence of the parasitic parallel resistance in the computation, region 1 should not be considered, hence only region 3 is considered in this work, with the exclusion of the oscillation region.

However, if region 3 is selected, the lower limit of the integration in Eq. (1) has to change to a non-zero value,

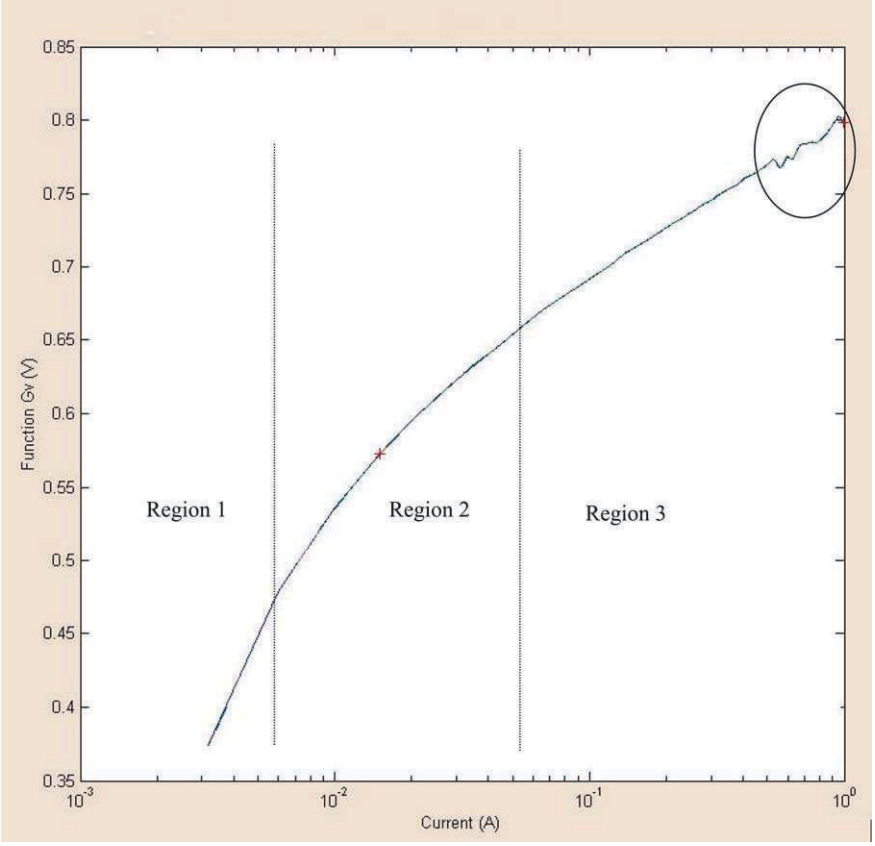


Fig. 3. $G(I,V)$ plot for 1N4007 with 1 Ω external resistor connected in series.

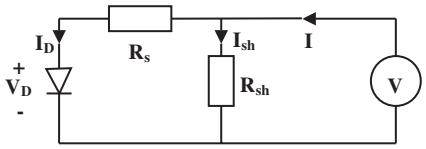


Fig. 4. Equivalent circuit diagram of diode with parasitic series and shunt resistances.

says V_1, and the upper limit is V_2, thus Eq. (1) will be modified as follows:

$$G(I_2,V_2)=\frac{(I_2V_2-I_1V_1)-2\int_{V_1}^{V_2}I'\,\mathrm{d}V'}{I_2}=nV_{\mathrm{T}}\left[\ln\frac{I_2}{I_s}-2\right]-\frac{I_1}{I_2}nV_{\mathrm{T}}\left[\ln\frac{I_1}{I_s}-2\right], \quad (4)$$

where I_j is the corresponding current at a measured voltage V_j in a forward I–V characteristics. Hence, we can see that a plot of $G(I_2,V_2)$ vs. $\ln(I_2)$ will not produce a straight line, and care has to be taken if only region 3 is used for the calculation.

From Eq. (4), if $I_2 \gg I_1$, the second term in Eq. (4) can be neglected, and hence we can get a straight line plot for $G(I,V)$ vs. $\ln(I)$ as can be observed in Fig. 3 for the larger current region (region 3). Also, with larger current, n value is a constant. The n value obtained in this work using region 3 is 2.04 which is close to the value of the ideality factor for high level injection in a power diode [12].

3. The modified series resistance determination method for power diode application

Fig. 5a shows the similar resistance plot as in Fig. 2, but it is obtained using the manual selection of the appropriate $G(I,V)$ regime in region 3. One can see that the accuracy is much improved.

To facilitate the extraction of series resistance for manufacturers usage, an auto-selection of the appropriate region is developed. [1] Fig. 5b shows the similar

[1] The auto-selection method is under copyright protection; hence disclosure of the method is restricted.

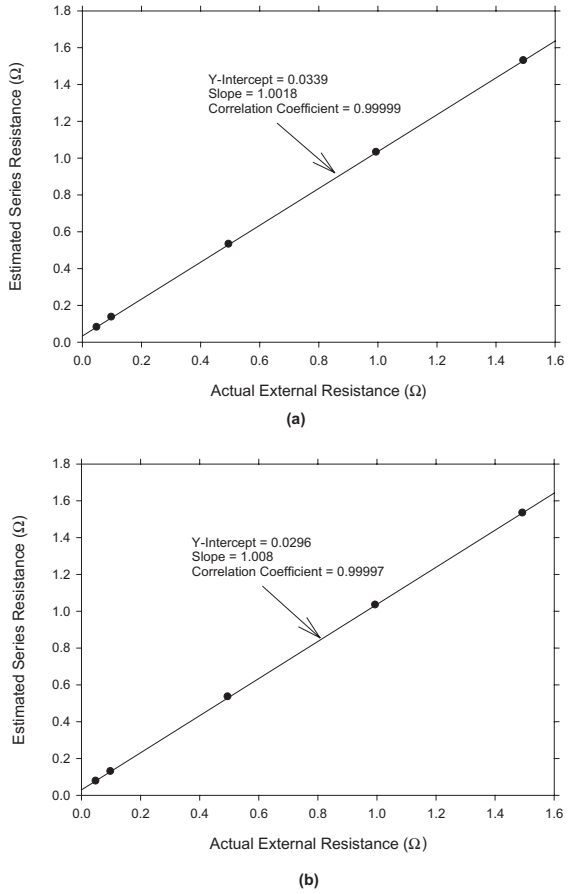


Fig. 5. Resistance plot using the modified method: (a) manual selection; (b) auto selection.

resistance plot as in Fig. 5a, and good accuracy can again be obtained.

To further verify the accuracy of the modified method, diodes of two other current ratings are used. Table 1 summaries the slopes, Y-intercepts (or the intrinsic series resistances) and the correlation coefficients of the resistance plot for the three different power diodes. The higher value of the intrinsic series resistance of the 100 mA diode package is because the lead to dice contact is not via soldering, but rather by blazing.

Table 1
Summary of the slopes, intrinsic series resistances and correlation coefficients for the three power diodes experimented

	Manual method		
	1N4007	100 mA diode	6 A diode
Slope	1.002	1.001	1.0063
Y-intercept (ohm)	0.03394	0.7997	0.0096
Correlation coefficient	0.99999	0.9978	0.999994

One can see that in all the three cases, good accuracy can be obtained by using the manual method as can be seen from the values of the slopes and the correlation coefficients. The lesser accuracy for diode with lower current rating is due to the fact that I_2 is not much greater than I_1. The time taken to obtain the series resistance value is less than 0.1 second with the standard Pentium III PC. Hence, the method is rapid enough for production environment.

The modified series resistance method has been applied for the detection of abnormal solder shape in power diode assembly, and it is elaborated elsewhere [13,14].

4. Conclusions

Series resistance of a power diode has a significant effect on its forward electrical characteristic. The existing methods of series resistance extraction are examined, and their accuracy and limitations are demonstrated. A modified method is developed, and it is shown that the accuracy of the new method is excellent, and the calculation is rapid enough for production line testing, making it a good tool for failure analysis and quality monitoring of both assembly and wafer fabrication processes in power diode manufacturing.

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