

Conferences > 2008 33rd IEEE Photovoltaic S... ?

Effect of annealing of multi crystalline edge wafers and Cz mono crystalline wafers based on metallurgical silicon

Publisher: IEEE Cite This PDF

Arve Holt ; Birger Retterstol Olaisen ; Erik Enebakk ; Anne-Karin Soiland All Authors

73 Full Text Views

Alerts

Manage Content AlertsAdd to Citation Alerts

Abstract

Document Sections

» Introduction» Methods» Results and Discussion» Conclusions

Authors

Figures

References

Keywords

Metrics

More Like This

Abstract:

The objective of this study has been to investigate the effect of annealing of multi crystalline edge wafers and Cz mono crystalline wafers based on metallurgically refin... View more

▼ Metadata

Abstract:

The objective of this study has been to investigate the effect of annealing of multi crystalline edge wafers and Cz mono crystalline wafers based on metallurgically refined silicon. Sets of neighboring wafers have been annealed at different temperatures and compared with as cut wafers as well as P-gettered wafers. The wafers have been characterized by μ -PCD, QSSPC, FeB-pair splitting and SIMS. The lifetime of minority carriers showed an improvement up to 100 times both in the edge zone and in the bulk region after P-gettering of multi crystalline wafers, dependent upon the position in the block and position within the wafer. However, Cz wafers showed no significant effect of gettering with respect to electrical properties in the bulk region. An edge region with lower lifetime for Cz wafers was observed from the surface and about one cm inwards. Temperature annealing showed only an improvement of the electrical properties in the edge zones for both multi crystalline wafers and Cz wafers. The effect after annealing is highest in the temperature range 500–600 °C in both cases.

Published in: 2008 33rd IEEE Photovoltaic Specialists Conference

Date of Conference: 11-16 May 2008

DOI: 10.1109/PVSC.2008.4922483

Date Added to IEEE Xplore: 12 May 2009

Publisher: IEEE

► ISBN Information:

Conference Location: San Diego, CA, USA



Introduction

The market of use of PV is expanding rapidly. Even though the production costs and the use of more efficient methods through the value chain, the price for the end user remains high. This is due to high feedstock prices due to limited amount of feedstock material available. Traditionally Si feedstock has been made from decompositions of silane or TCS by using the Siemens process. Lately the FBR process has been introduced to be able to do a more energy efficient decomposition.

In parallel several initiatives for making silicon by other methods have been initiated. The method given most attention is the metallurgical route. This route is based on various purification processes of the metallurgical silicon, for example by slag treatment, leaching and solidification amongst other [1]. Initial studies of such materials have shown comparable electrical properties [ii] and solar cell efficiencies [iii] for multi crystalline silicon solar cells.

It has also successfully been shown growing of mono crystalline ingots from this kind of material previously [iv].

The objective of this study has been to further investigate the effect of annealing and gettering of multi crystalline edge wafers and Cz mono crystalline wafers based on metallurgical silicon. The goal is to find methods to minimize the effect of the impurities and defects in this kind of material. Two main strategies have been studied: double sided P-gettering and temperature annealing at intermediate temperatures.

In principle, phosphorus diffusion gettering works in three steps [v]. First the metallic impurities has to be released from whatever state they are trapped in. Some impurities, like the 3d transition metals, are predominantly interstitially dissolved in the silicon, and thus are free to move around. Other impurities may be immobile at substitutional sites in the silicon or in precipitates, and they need to be released before they can be gettered out of the wafer by for example high temperature treatment. The next step is the diffusion step, where the impurities have to move from the bulk of the wafer to the gettering region, which for phosphorus diffusion gettering is a thin layer on one or both surfaces. The third step is for the impurities to be captured at gettering sites in this region. This can be obtained by either avoid further high temperature treatment or by using a etch a-way process etch which effectively removes the mobile impurities and the P-layer from the wafer.

Methods

Both multi crystalline and mono crystalline silicon wafers have been studied. The wafers have been made from blocks and ingots based on silicon made by the metallurgical route.

Sets of neighboring wafers have been annealed at different temperatures and compared with as cut wafers as well as P-gettered wafers. The Cz wafers were originally 156 mm semi square. However, in order to process the wafers simultaneously as the mc wafers the size was reduced to 125 mm quasi semi square wafers. In other words, only one round corner was present. Only wafers from one position within an ingot have been studied in the case of Cz wafers.

Detailed mapping of lifetime of minority carriers have been studied by microwave photo conductance decay (μ -PCD) method. The bulk [Fe] has been studied by FeB-pair splitting by comparing the lifetime measurements before and after light soaking. The recombination of FeB pairs after light soaking is both dependent on time and temperature. Increasing the temperature shorten the relaxation process. If too long measurement time has been used to record the lifetime

For the SIMS measurements samples from three different positions on two multi crystalline wafers were made. The first position was made from the outmost 8 mm from the edge, the second from the inner edge zone correspond to from a distance between 8–16 mm from the edge and the third sample was made from the centre of the wafer. The sample size used was 8×8 mm. Both the as cut and the gettered wafer were chemically polished before the SIMS measurements.

Results and Discussion

P-Gettering of Multi-Crystalline Wafers

Multi crystalline wafers based on feedstock from the metallurgical route have been investigated. The lifetime after P-gettering showed an improvement up to 100 times both in the edge zone and in the bulk region of multi crystalline wafers, dependent upon position in the block and within the wafer, see Figure 2. In the inner edge region the improvement was highest and material was fully recovered here. Figure 1 shows the lifetime before and after gettering at different positions in a block. The increased lifetime shown in position 6 and upwards after gettering may be due to non-recombinative traps. This is supported by the QSSPC measurements, which showed an increased lifetime with decreasing injection level, for then to go through a maximum at low injection levels. Such behavior has also previously been shown by A. Bentzen [vi] when non-recombinative traps have been included into a recombination model.

 Figure 1 - Lifetime of minority carriers before and after gettering of mc wafers from different positions in a block.

Figure 1

Lifetime of minority carriers before and after gettering of mc wafers from different positions in a block.

 Figure 2 - Lifetime maps of two neighboring wafers from position 7 of an edge block before and after P-gettering.

Figure 2

Lifetime maps of two neighboring wafers from position 7 of an edge block before and after P-gettering.

Annealing of Multi Crystalline Wafers

Figure 3 shows lifetime profiles after annealing at 400–800 °C of an edge block. As shown, the annealing showed no effect on the bulk properties at lower temperatures. At temperatures above 600°C the lifetime starts to degrade. In the edge zone the material quality starts to improve by increasing the temperature and reaches a maximum around 600°C.

 Figure 3 - Lifetime profiles after annealing at different temperatures from position 7 of an ES edge block from the edge and inwards.

Figure 3

Lifetime profiles after annealing at different temperatures from position 7 of an ES edge block from the edge and inwards.

M. D. Pickett and T. Buonassisi [vii] have also shown that annealing process has the advantage of passivating the impurities by formation of less electrical active clusters or precipitates within wafers containing initially high impurity concentrations. They obtained the best results around 400-500°C.

It is also in this work assumed the clustering process starts to form less electrically active clusters during low temperature annealing/cooling. By heating, these complexes are dissolved again and can be removed by a gettering process.

Interestingly the lifetime profiles shows two peaks in the edge zone part where the effect of annealing is largest. This is also clearly shown in Figure 4, a lifetime map before and after annealing at 600 °C.

Figure 4 - Lifetime map of a sample from position 7 of an edge block after annealing at 600 °C.

Figure 4

Lifetime map of a sample from position 7 of an edge block after annealing at 600 °C.

By measuring line scan of a [Fe] from the edge and inwards, the results also show two peaks in the [Fe], see Figure 5 which also shows a line scan of the lifetime in the same region. As shown from the figure, the [Fe] goes through a minimum in the regions where peaks in the lifetime measurements have been observed.

Figure 5 - Lifetime and [Fe] line scan of a sample from position 7 of an edge block after annealing at 600 °C.

Figure 5

Lifetime and [Fe] line scan of a sample from position 7 of an edge block after annealing at 600 °C.

By comparing the [Fe] line scans from the as cut wafers, the free [Fe] has been reduced about a decade.

The observed peaks in the edge zone may be due to different cluster regimes or different precipitates of iron containing silisids. S. K. Estreicher et al [viii] published a modeling paper on different possible Fe-clusters, however is not possible in this study to predict the composition of the two main regions. Since these clusters have been formed in an [Fe] gradient over several decades ($10^{14} - 10^9$ atoms/cm³) it is assumed the [Fe] of the clusters/ precipitates is lower in the region where the second lifetime peak was observed.

By comparing the annealing results with the gettering results, P-gettering process showed higher improvement with respect on lifetime of the minority carriers. This is the case both in the edge zone region and in the bulk region not contaminated by inward diffusion of impurities during crystallization.

Furthermore the gettering recover completely the area in the edge zone where the second peak in lifetime was observed after annealing in the temperature range 500–600 °C. An implication of this is that the clusters formed in this region during annealing dissolves again at higher temperatures.

It is concluded that annealing do not have any positive effect on high quality materials. It is observed that in bulk areas with low lifetime the annealing further expands these areas. This effect increases with increasing temperature. Further, the results show that only in highly contaminated areas of dissolved impurities, like the part of the block contaminated by inward diffusion from the crucible, the annealing process improves the electrical properties of material.

Sims Measurements of Multi-Crystalline Wafers

In order to study in more detail the nature of the impurities, SIMS measurements were initiated. Since the impurity level was well below the detection limit for this method, ion mapping of different elements was used in order to detect possible precipitates. In this paper, the results from the Al-mapping are presented, shown in Figure 6.

Figure 6 - SIMS ion maps of Al of two multi crystalline wafers. On the top line from the left is an image taken from the outer edge zone of an as cut mc wafer. The image in the middle of the first line is an image from the inner edge zone of an as cut mc wafer and to the left on the first line is an image taken from the centre of the same wafer. The second line shows the results from a neighboring P-gettered wafer.

Figure 6

SIMS ion maps of Al of two multi crystalline wafers. On the top line from the left is an image taken from the outer edge zone of an as cut mc wafer. The image in the middle of the first line is an image from the inner edge zone of an as cut mc wafer and to the left on the first line is an image taken from the centre of the same wafer. The second line shows the results from a neighboring P-gettered wafer.

The raster used during the measurements was 500×500 microns. Depth profiling was used in order to determine the particles size. The size of the particles are shown, are typically less than 100 nm. The particles in Figure 6 seem to be much larger, but this is due to the large ion-sputtering diameter (10µm) which limit the visual resolution.

The results from the as cut wafers show presence of a gradient in the surface particles of Al from the edge. One explanation could be inward diffusion of Al from the crucible / crucible coating. This is supported by the high Al concentration in commercial available crucibles[ix]. However the diffusion coefficient of Al in silicon is orders of magnitudes lower than Fe. Inward diffusion of Al may therefore not be the main explanation.

After a gettering process high Al concentration of precipitates is no longer observed. This may be due to the removal of Fe and other elements during the gettering process. Presence of impurities may have the effect of accelerating the diffusion of solved Al to the surface.

P-Gettering of Mono Crystalline CZ Wafers

Mono crystalline wafers based on feedstock from the metallurgical route have also been investigated. Gettering studies of Cz wafers showed no significant effect of gettering with respect to electrical properties in the bulk region and only a very low [Fe_i] was detected in this region. However, an edge region with lower lifetime for Cz wafers was observed from the surface and about one cm in-wards. This is shown in Figure 7.

Figure 7 - Lifetime maps of an as cut wafer (left) and a P-gettered wafer (right) from a cz ingot made from ES feed-stock. The fine structure lines observed on the as cut wafer may be due to stacking faults.

Figure 7

Lifetime maps of an as cut wafer (left) and a P-gettered wafer (right) from a cz ingot made from ES feed-stock. The fine structure lines observed on the as cut wafer may be due to stacking faults.

It is assumed that the reduction of lifetime near the surface is due to accumulation of impurities like Fe under the Cz crystallization process. [Fe] mapping showed also 1–2 order of magnitude higher concentration in these areas compared with the bulk regions. This edge Fe rich zone has also been observed in some commercial available wafers with initially high [Fe], see Figure 8.

P-gettering improves the material and removes the impurities present near the surface on a similar way as for multi crystalline wafers in the edge zone, see Figure 9.

Figure 8

Lifetime maps of an as cut (left) and a gettered cz wafer (right) containing initially high [fe].

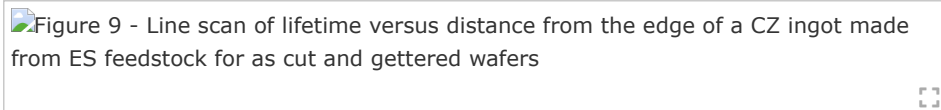


Figure 9

Line scan of lifetime versus distance from the edge of a CZ ingot made from ES feedstock for as cut and gettered wafers

It is also shown in Figure 9 that the edge zone is not completely recovered after P-gettering, but only partly due to formation/ or already present precipitated clusters. Also observed is only the minor improvement of the electrical properties after gettering in the bulk of the wafers. An interpretation of the minor improvement could be that during crystallization crystal defects are formed and acts as the dominant recombination centers. The nature of the crystal defects is currently under investigation.

In case for the Cz sample initially containing high [Fe], P-gettering dramatically increases the electrical properties in the outer region and completely removes the edge zone, see Figure 8. However, in the inner region only a minor improvement is observed. It seems like there is a transition from one kind of crystal defects in the center region to an other type of crystal defects in the outer region. Other [x], [xi] have suggested that this kind of behavior is due to a transition from vacancy dominated region in the inner part to a rich region of self interstitial in the outer part. According to the authors, the size of the different regions may be altered by adjusting the Cz crystal growth rate.

By comparing the results from the two different feed-stocks, an explanation of the overall low lifetime for the Cz wafers based on metallurgically refined silicon, is presence of only one type of crystal defects.

Annealing of Mono Crystalline CZ Wafers

Temperature annealing showed only an improvement of the electrical properties in the edge zones for the Cz wafers, see Figure 10. The best improvement is observed at 600 °C. It is also shown that the lifetime in the bulk region starts to degrade at higher temperatures. This may be due to contamination from the belt furnace system used to do the annealing experiments. However, an alternative explanation could be dissolution of extended defects [v].

The mechanism for the partly recovering of the edge zone is assumed to be due to formation of less electrically active clusters, similar as for the mc wafers.

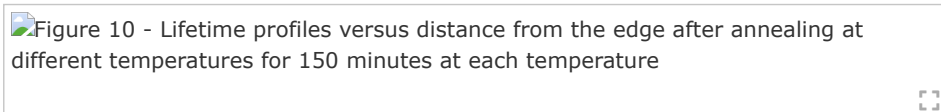


Figure 10

Lifetime profiles versus distance from the edge after annealing at different temperatures for 150 minutes at each temperature

Conclusions

For multi-crystalline wafers based on ES solar material, P-gettering improves both the edge zone and bulk regions. Annealing forms less electrically active clusters/precipitates in the edge zone.

Download

PDF For Cz wafers based on ES solar material studied in this paper, crystal defects are the limiting factor with respect on lifetime of the minority carriers. Regions with high impurity levels are improved by gettering and annealing. The effect after annealing is highest in the temperature range 500–600 °C.

By comparing the gettering process and annealing process at intermediate temperatures, the gettering process always shows highest improvement of the electrical properties.

ACKNOWLEDGEMENTS

This project is partly funded by the Norwegian Research Council through the project 173999/S30.

Authors

Figures

References

Export



References & Cited By

☐ Select All

1. C. Zahedi. et. Al., "Solar grade from silicon metallurgical route" PVSEC-14, Bangkok, (2004) 26-30
► Show in Context [Google Scholar](#)
2. A. Holt, E. Enebakk and AK. Soiland, "Effect of impurities on the minority carrier lifetime of silicon made by the metallurgical route" , Proceedings of the 22nd European Photovoltaic Solar Energy Conference, Milan, (2007) 1155-1159
► Show in Context [Google Scholar](#)
3. A. Kranzl, M. Kas, K. Peter and E. Enebakk, future cell concepts for mc solar grade silicon feedstock material, Proceedings of the 21st European Photovoltaic Solar Energy Conference, Dresden, Germany, (2006) 1038-1041
► Show in Context [Google Scholar](#)
4. J. Vedde and R. Tronstad, Proceedings of the 21st European Photovoltaic Solar Energy Conference, Dresden, (2006), 976-977
► Show in Context [Google Scholar](#)
5. M. Seibt, A. Sattler, C. Rudolf, O. Vol, V. Kveder, W. Schroter, "Gettering in silicon photovoltaics: current state and future perspectives", phys. stat. sol. (a) 203, No. 4, (2006) 696-713
► Show in Context [CrossRef](#) [Google Scholar](#)
6. A. Bentzen, Phosphorus diffusion and gettering in silicon solar cells, PhD Dissertation, University of Oslo, Norway (2006) 108-110
► Show in Context [Google Scholar](#)
7. M. D. Pickett and T. Buonassis, " Iron point defect reduction in multicrystalline silicon solar cells", Applied Physics Letters 92, (2008) 122103



Download

► Show in Context

CrossRef [↗](#)

Google Scholar [↗](#)



Contents

PDF

8. S. K. Estreicher, M Sanati and N Gonzalez Azwacki, Fundamental interactions of Fe in silicon, Solid State Phenomena, 131-133 (2008) 233-240

► Show in Context

CrossRef [↗](#)

Google Scholar [↗](#)

PDF

9. R. Kvande, L. Amberg, C. Martin, G. Rancoule, L. Du-puy, A. Holt, effect of crucible purity and interface characteristics on multicrystalline silicon ingot quality, Proceedings of the 21 st European Photovoltaic Solar Energy Conference, Dresden, Germany, (2006) 1052-1056

► Show in Context

Google Scholar [↗](#)

10. G. Zoth, S. Geyer and H.-J. Schulze, Silicon contamination control by lifetime measurements, Electrochemical Soc. Proceedings Volum 99-16 (1999) 5-20

► Show in Context

Google Scholar [↗](#)

11. A. Voigt and C. Weichmann, Defect formation in Cz silicon growth, J. of Crystal Growth 266 (2004) 126-131

► Show in Context

CrossRef [↗](#)

Google Scholar [↗](#)

[View More](#)

Keywords



Metrics



More Like This

Formation of polycrystalline silicon films with μm -order-long grains through liquid-phase explosive crystallization by flash lamp annealing
2012 38th IEEE Photovoltaic Specialists Conference
Published: 2012

Crystallization of poly-silicon film by different annealing techniques
2011 Saudi International Electronics, Communications and Photonics Conference (SIEPCP)
Published: 2011

[Show More](#)



Download
PDF



IEEE Personal Account

CHANGE
USERNAME/PASSWORD

Purchase Details

PAYMENT OPTIONS
VIEW PURCHASED
DOCUMENTS

Profile Information

COMMUNICATIONS
PREFERENCES
PROFESSION AND
EDUCATION
TECHNICAL INTERESTS

Need Help?

US & CANADA: +1 800
678 4333
WORLDWIDE: +1 732
981 0060
CONTACT & SUPPORT

Follow



[About IEEE Xplore](#) | [Contact Us](#) | [Help](#) | [Accessibility](#) | [Terms of Use](#) | [Nondiscrimination Policy](#) | [IEEE Ethics Reporting](#)  | [Sitemap](#) | [IEEE Privacy Policy](#)

A not-for-profit organization, IEEE is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity.

© Copyright 2024 IEEE - All rights reserved, including rights for text and data mining and training of artificial intelligence and similar technologies.

IEEE Account

- » Change Username/Password
- » Update Address

Purchase Details

- » Payment Options
- » Order History
- » View Purchased Documents

Profile Information

- » Communications Preferences
- » Profession and Education

» Technical Interests
Need Help?



Download
PDF

 Contents

» **US & Canada:** +1 800 678 4333

» **Worldwide:** +1 732 981 0060

» Contact & Support



[About IEEE Xplore](#) | [Contact Us](#) | [Help](#) | [Accessibility](#) | [Terms of Use](#) | [Nondiscrimination Policy](#) | [Sitemap](#) | [Privacy & Opting Out of Cookies](#)

A not-for-profit organization, IEEE is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity.

© Copyright 2024 IEEE - All rights reserved. Use of this web site signifies your agreement to the terms and conditions.