

INTERFACE STATES AT THE SiO_2 –Si INTERFACE

M. SCHULZ

Institut für Angewandte Physik der Universität Erlangen–Nürnberg, Glückstrasse 9, D-8520 Erlangen, Fed. Rep. of Germany

Received 31 August 1982; accepted for publication 26 October 1982

The present understanding of interface states at the SiO_2 –Si interface is reviewed. Typical results of measurement techniques are presented and critically discussed with respect to identification of types and origins of interface states. Only one type of interface state is observed after strong hydrogen annealing. The density of these interface states decays from $D_{it} \geq 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ near the conduction band to extremely low values of $D_{it} \leq 10^8 \text{ cm}^{-2} \text{ eV}^{-1}$ in the lower half of the Si band gap. A peak of interface states is observed below midgap. The density of bulk traps in silicon is comparable to the low interface state density. Among the various models of interface states proposed, the trivalent silicon dangling bond, bond angle distortions, and discrete traps in the interfacial layer are possible explanations of the various types of interface states.

1. Introduction

The oxide SiO_2 thermally grown on Si is the backbone of the metal–oxide–semiconductor (MOS) technology in semiconductor device industry. The importance is based on the fact that the interface SiO_2 –Si exhibits ideal properties for surface-controlled devices because an extremely low interface state density can be achieved. The SiO_2 –Si system has no comparison among other semiconductors.

Interface states are traps located at the Si– SiO_2 interface which rapidly interact with free charge carriers in the semiconductor substrate as indicated in fig. 1. The traps are filled with majority carriers when the interface is biased into accumulation. When the interface is biased into depletion or inversion, the charge in the interface states is changed in contrast to the fixed or mobile oxide charge which is located in the bulk of the oxide and which does not interact with the silicon substrate except by charge carrier injection across the interface barrier by photoexcitation or after heating of free carriers in Si by a high electric field.

Only interface states having an energy position within the bandgap of the silicon substrate affect devices and are therefore considered here because charge trapping at interface states is possible in the same manner as for bulk

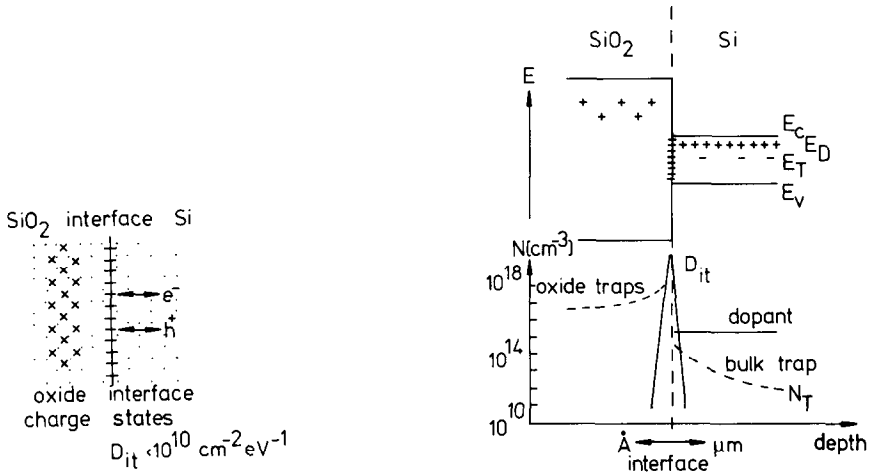


Fig. 1. Definition of interface states at the SiO₂-Si interface. Interface states rapidly interact with free charge carriers, i.e. holes or electrons, in the silicon substrate.

Fig. 2. Schematics of the energy distribution and the spatial distribution of interface states.

traps in Si. As is schematically indicated in fig. 2, the density of the interface state peaks at the SiO₂-Si interface. This trap density which is continuously distributed in the energy gap of Si, is denoted by D_{it} in units of $\text{cm}^{-2} \text{ eV}^{-1}$ in accordance with the standardized terminology of Deal [1]. It is not clear at present whether the interface states are located in a monolayer at the interface or whether they are distributed within a tunneling depth of a few angstroms into the SiO₂. Traps in the bulk silicon substrate may also originate from the SiO₂-Si interface. Such traps will be treated as bulk traps at concentration $N_T(x)$. The concentration of bulk traps is generally less than the dopant concentration. They are distributed throughout the space charge layer width of the order of micrometers. Their total concentration in the space charge layer may be comparable to the interface state density.

Interface states at the SiO₂-Si interface have received strong scientific attention since the advent of the first MOS transistors in the early sixties. At that time, interface states still limited the device performance. Since then the interface state density measured has continuously dropped. Best values reported for each year are plotted in fig. 3. The observed improvement of four orders of magnitude from $D_{it} = 10^{12}$ to $D_{it} = 10^8 \text{ cm}^{-2} \text{ eV}^{-1}$ has been achieved entirely by empirical methods. Today interface states are barely detectable in uniform MOS structures. They are, however, still of importance in submicron structures for large scale integration, in radiation effects, and after impurity contamination among others. Many review papers deal with various aspects of

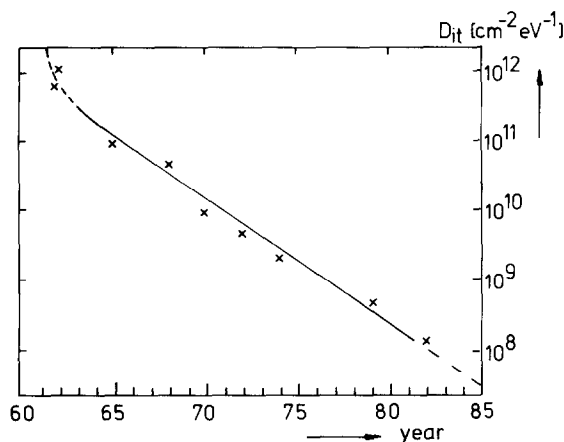


Fig. 3. Drop of interface state density versus time. The points represent the lowest interface state density observed in each year as reported in ref. [3]. The lowest two points are recent measurements. Large error bars are probably associated with each point.

interface states [2–8]. Studies on interface states are still the topics of conferences and are reported in the proceedings [9–12].

In spite of 20 years of research, the origin of the residual interface states is still not known. The approach in this survey of the present knowledge therefore is to try to disentangle the vast amount of information collected and to interpret the data by models proposed. In section 2, the measurement techniques used in the study of interface states are reinspected to discuss the information that can be extracted from the data. The results on interface state properties are then reviewed in section 3 on selected examples which are discussed in the light of models in section 4.

2. Measurement techniques

2.1. Quasistatic C - V technique

The quasistatic capacitance–voltage (C - V) measurement on MOS capacitor structures is the standard method in laboratory practice for determining the distribution of interface states in the forbidden gap of silicon. The method is usually automated and the high-frequency (1 MHz) differential capacitance $C_{\text{HF}}(V)$ is recorded by a commercial bridge. The low-frequency static curve is obtained by recording the displacement current for a slow ($\approx 10 \text{ mV s}^{-1}$) voltage ramp. The displacement current I is proportional to the low-frequency

differential capacitance $C_{LF}(V)$

$$I = C_{LF}(V) dV/dt. \quad (1)$$

The interface state density is determined in the depletion region (dip of the C - V curves) from the difference between the high- and low-frequency capacitance

$$D_{it} = D_{it}(V) = \frac{C_{ox}}{qA} \left[\frac{C_{LF}/C_{ox}}{1 - C_{LF}/C_{ox}} - \frac{C_{HF}/C_{ox}}{1 - C_{HF}/C_{ox}} \right]. \quad (2)$$

C_{ox} is the oxide capacitance, q the elementary charge, and A the area of the capacitor. Various methods exist to relate the bias voltage V applied to the band bending at the interface so that the energy position E_{it} of the interface state density measured may be determined [3].

A typical set of capacitance curves is shown in fig. 4 for a high-quality MOS capacitor on a p-type silicon substrate. No separation of the high- and low-frequency capacitance curves is observed on this sample except in the inversion region. An interface state density cannot be extracted from these data because the error in the measurement of the difference signal in eq. (2) is too large. From this measurement, we only deduce that the interface state density must be less than $D_{it} < 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$. In fact, the interface state density measured by transient spectroscopy (see below) is as low as $D_{it} \approx 10^8 \text{ cm}^{-2} \text{ eV}^{-1}$, which represents the state of the art today.

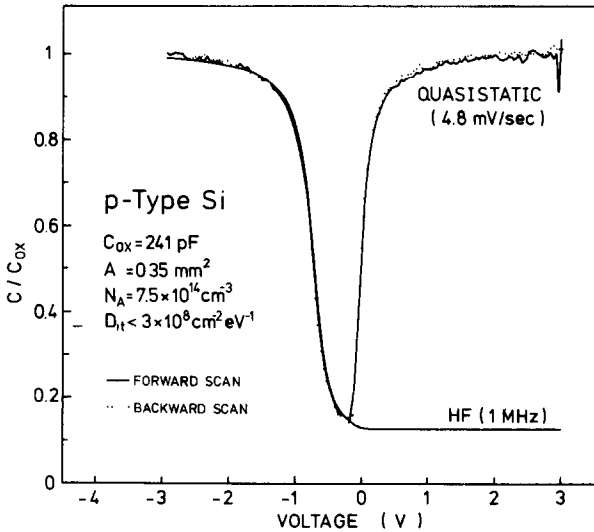


Fig. 4. Capacitance-voltage (C - V) plot of an MOS capacitor on p-type silicon substrate. The capacitor data are shown in the insert. The interface state density $D_{it} \approx 10^8 \text{ cm}^{-2} \text{ eV}^{-1}$ cannot be determined from this measurement.

The quasistatic C - V measurement can only be used to check the quality of the interface, i.e. the upper limit of the interface state density and the flatband voltage which is a measure of the oxide charge. Electrical measurement techniques which exhibit sufficiently high sensitivity are the conductance technique [13,14] and the transient spectroscopy [15,16].

2.2. Conductance technique

In the conductance technique, the full frequency dispersion of the MOS capacitance is analysed rather than just the high- and low-frequency capacitance. In the same manner as for the quasistatic technique, the Fermi energy is used to probe the energy position of the interface states (fig. 5). The conductance signal G_m of the MOS capacitor assumes a maximum at frequency

$$\omega_{\max} = f_{\tau} \sigma v_{th} n_s \simeq \omega_t = 2 \sigma v_{th} n_s, \quad (3)$$

which is approximately determined by the trapping frequency ω_t . f_{τ} is a correction factor of the order of 2 which takes into account surface potential fluctuations [3]. σ is the capture cross-section, v_{th} the thermal velocity of charge carriers in silicon, and n_s the charge carrier density at the interface which is dependent on the position of the Fermi energy. The maximum of a reduced conductance G_p which is obtained by subtracting the effect of the series oxide capacitance,

$$\frac{G_p}{\omega C_{ox}} = \frac{G_m / \omega C_{ox}}{(1 - C_m / C_{ox})^2 + (G_m / \omega C_{ox})^2}, \quad (4)$$

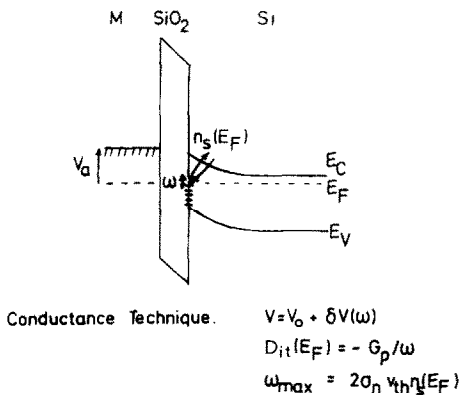


Fig. 5. Schematic illustration of the basic measurement principle of the quasistatic C - V and the conductance technique. The Fermi energy is used to probe the energy position of interface states.

is directly proportional to the interface state density,

$$D_{it} = \frac{C_{ox}}{qAf_N} \left[\frac{G_p}{\omega C_{ox}} \right]_{\max}, \quad (5)$$

where f_N is a correction factor of the order of 0.4 which again takes into account surface potential fluctuations [3]. The measurement by the conductance technique is usually quite elaborate because a wide frequency range must be used for each position of the Fermi energy. The sample temperature has to be lowered in order to reduce the trapping frequency into the measurement range for interface states at shallow energy positions.

Fig. 6 shows a normalized diagram of the conductance G_p/ω versus frequency $\omega/\omega_{\max}$. It is noticed that the width of the maximum is wider than the ideal curve $\sigma_g = 0$ without surface potential fluctuations. The curves measured can be fitted by assuming a gaussian surface potential fluctuation at variance σ_g of the order 40–70 mV [13,9].

2.3. Transient spectroscopy

Deep level transient spectroscopy (DLTS) is also useful to determine interface traps in MOS capacitors [15,16] and MOSFETs [17,18]. The measurement principle is illustrated in fig. 7. Interface states are filled by biasing the semiconductor surface into accumulation. The spectrum of emission time constants is analysed in depletion. Because the emission rate is thermally activated similar to bulk traps

$$1/\tau = \sigma v_{th} N_C \exp(-E_{it}/kT), \quad (6)$$

with N_C the effective density of states in the band, a trap spectrum may be

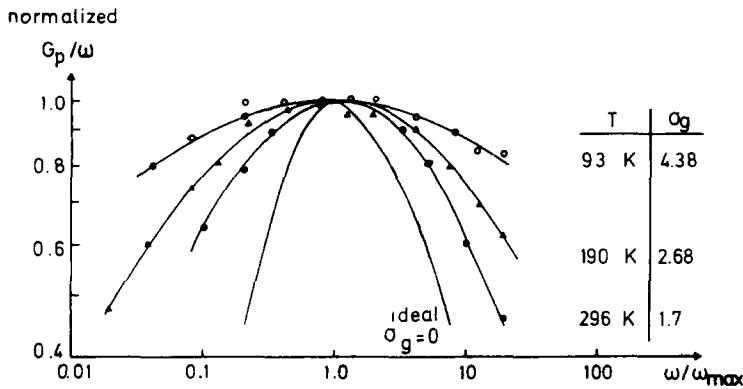


Fig. 6. Normalized G_p/ω curves obtained at various temperatures by the conductance technique. The variance σ_g in units kT/q is obtained by curve fitting [9,14].

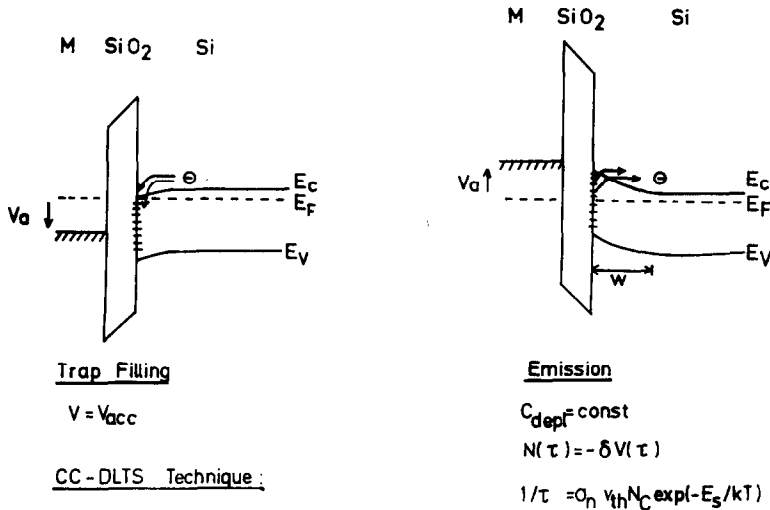


Fig. 7. Schematic illustration of the basic measurement principle of the transient spectroscopy CC-DLTS. By biasing the semiconductor surface into accumulation, interface states are filled (left). Reemission is monitored in depletion (right). A voltage transient is observed for the charge exchange at the interface when a constant capacitance is maintained.

obtained in a temperature scan of the transient signal when a fixed time constant is selected in the DLTS analysis [19]. In CC-DLTS, the bias voltage is adjusted by a feedback of the capacitance signal to maintain a constant capacitance. The interface state density is then simply determined by

$$D_{it}(\tau) = \frac{C_{ox}}{AkT \ln(t_2/t_1)} \delta V, \quad (7)$$

where δV is the voltage of the DLTS signal and $t_{1,2}$ are the DLTS sampling times. The energy position E_{it} of the interface state is approximately given by

$$E_{it} = kT \ln[\sigma v_{th} N_C t_1 / \ln(t_2/t_1)]. \quad (8)$$

The capture cross-section σ is obtained from two or more temperature scans taken at different delay time constants t_1 in the DLTS analysis [16,20]. The evaluation, however, assumes a constant cross-section which generally is not valid. The exact evaluation has to take into account the energy-dependent capture cross-section [21]. Usually it is quite appropriate to assume a constant average capture cross-section in eq. (8). It is noted that CC-DLTS is independent of the position of the Fermi energy and thus of the surface potential of the semiconductor.

2.4. Comparison of the conductance and CC-DLTS technique

In fig. 8, the transient spectroscopy and the conductance technique are compared. The transitions of charge carriers which are sensed by the two techniques are shown in an in-depth view with respect to the band bending and in an in-plane view of the capacitor area with respect to potential fluctuations. The conductance technique only senses transitions in the immediate vicinity (approximately $\Delta E = kT$) of the Fermi energy. Bulk levels are only measured in a small portion of the space charge region at the crossover with the Fermi energy. The conductance technique therefore is rather insensitive to bulk traps. Surface potential fluctuations cause a spread of the energy resolution.

Since CC-DLTS is independent of the potentials, bulk traps are measured in the full width of the space charge region independent of the band bending. The signal size due to bulk traps may be comparable to that of the interface states in CC-DLTS. Potential fluctuations do not hamper the energy resolution in CC-DLTS. Only the size of the signal is reduced when states submerge in the Fermi energy and do not reemit the trapped charge. The problem with DLTS is the deconvolution of the time constant spectrum $N(\tau)$ into an energy spectrum.

The analysis of interface state properties by the techniques discussed is explained in fig. 9. The diagram shows the possible distributions of interface states in the area with the energy position in the x -dimension and the capture cross-section in the y -dimension in a log scale. A discrete level, e.g. a bulk level having a definite energy position and a definite capture cross-section, is represented in this diagram by a dot. A continuum of interface states in the forbidden gap of Si is represented by a continuous line or even can cover an area if the capture cross-section for a state at a given energy is also distributed. This may occur, when the states are spread out into the depth of the SiO₂ and

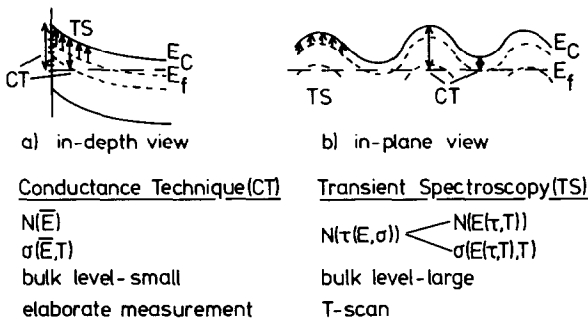


Fig. 8. Comparison of the conductance technique CT and transient spectroscopy TS in the measurement of bulk traps in the semiconductor and interface states in MOS structures. The properties are listed in the insert.

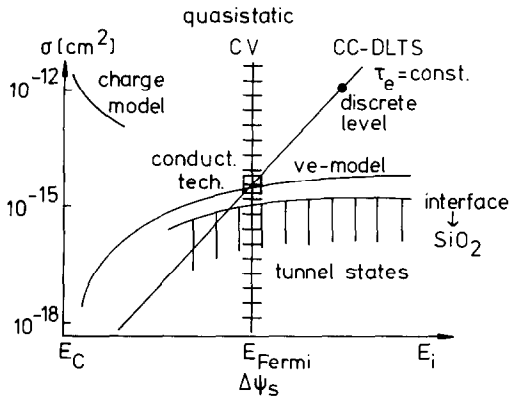


Fig. 9. Schematics of the measurement of interface state properties.

the capture and the emission rate are dominated by tunneling into traps at a variable depth. This case is indicated in fig. 9 by the lined area. States may also be distinguished by the magnitude of the capture cross-section. Electrons bound to a positive fixed charge (charge model, see below) are expected to be rapidly trapped by the attractive Coulomb force. Bulk donor centers in Si have capture cross-sections of the order of $\sigma = 10^{-12} - 10^{-13} \text{ cm}^2$ for electrons. The capture probability for states deep in the SiO₂ is assumed to be low because the tunneling barrier is several volts at the interface and thus inhibits the capture to states deeper than a few ångströms in the SiO₂.

The quasistatic *C-V* technique senses all traps, independent of the magnitude of the capture cross-section, along the vertical line in fig. 9 which is determined by the position of the Fermi energy. In the conductance technique, where the full frequency dispersion is measured, a spot on the vertical line is resolved. In principle, the full interface state area of the diagram in fig. 9 can be analysed by the conductance technique. In practice, the resolution is limited due to the potential fluctuations at the interface which smear out the energy resolution of the position of the Fermi energy as is indicated by the bars along the vertical line.

The CC-DLTS technique is not affected by potential fluctuations. It detects all the interface states that emit at the same time constant $\tau = \text{const.}$ These interface states and bulk traps are located at a given sample temperature on the diagonal straight line in fig. 9. From this diagram, we can see that additional information on interface state properties may be obtained when results of both techniques, the conductance technique and CC-DLTS, are carefully compared.

2.5. Other measurement techniques

Numerous variations of the quasistatic $C-V$ technique [3], the conductance technique [3,22-26,52], and the CC-DLTS technique [27-31,159,160] exist. The transfer loss of CCDs allows the determination of interface state densities and capture cross-sections with good accuracy [32]. Illumination of the sample with bandgap light during the $C-V$ measurement offers additional possibilities to independently determine majority and minority carrier cross-sections [22,23] and to speed up slow states [33]. Photoexcitation of interface states using infrared light in combination with the electrical measurement of the charge exchange has been used to determine the cross-section of the optical transition [34-36]. Basically, the charge exchange near the Fermi energy or the quasi-Fermi energy or the transient is sensed in all these electrical measurement techniques. Density of states and capture cross-sections are determined, but no information on the incorporation of the defect is usually obtained.

Information on the crystallographic structure of the defects at the interface may be obtained by EPR, which has been applied to the interface state characterization recently [37-40]. In comparison to the electrical measurement of interface states, EPR is rather insensitive. The identification of contributions from interface states to the EPR signal is only possible for rather high densities in excess of $D_{it} \geq 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ [38].

Fowler-Nordheim tunneling yields information on the depth distribution profile of interface charges in thin tunnel structures having a high interface state density after stressing by current injection [41].

3. Experimental results on interface state properties

3.1. Energy distributions

Measurements on interface state distributions within the energy gap of Si have been reported in numerous papers, e.g. in refs. [23,33,42,43]. The shape of the interface state distribution shown in fig. 10 is now generally accepted. The results of the static method and the conductance method are in good agreement for this sample which shows a rather high density of states of $D_{it} > 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ where the measurements could be easily performed at reasonable accuracy. A U-shaped distribution is observed, where the density of states increases towards both band edges. One or several peaks are frequently observed at this high density thus indicating that more than one type of interface states is present. Peaks near the band edges [44] could not be confirmed. They seem to be an artefact of the measurement technique used [45]. If there is a peak it is very near or in the conduction band [46].

A similar result of ref. [23] taken on a sample having a high density of states

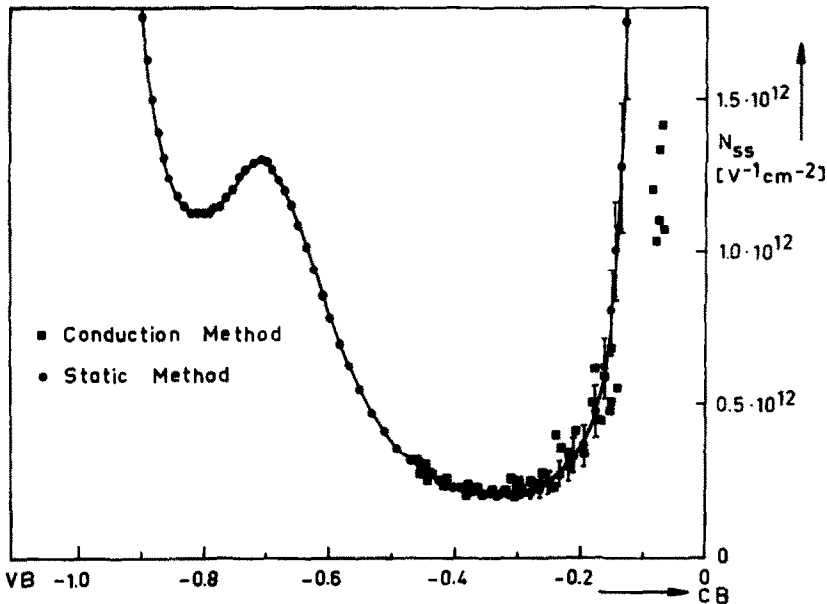


Fig. 10. Distribution of the interface state density D_{it} versus energy E from the conduction band CB to the valence band VB. Measurement results obtained by the conductance technique and by the static technique are compared [3,43]. The n-type (111) sample was oxidized in dry O_2 at 1140°C . Post-metallization anneal at 350°C in hydrogen ambient was applied.

is shown in fig. 11. The quasistatic $C-V$ measurement result (curve 1) represents the total density of interface states measured. By the conductance technique, three different types of states could be separated (curves 2–4). It is noted that the density of one type of fast interface state decays over four orders of magnitude from the conduction band edge towards the valence band edge. This curve 3 is shown in fig. 12 again together with other results taken on samples showing a lower density of interface states. A general trend is noticed. The highest density is observed in the thin oxide without hydrogen anneal. The standard dry oxide measured by CC-DLTS shows the same decay towards the valence band. The CCD measurement (dashed line) of ref. [32] fits very well into this group. Data, e.g. of refs. [22,27,47] among others also match these data. The curves are not included in the graph for clarity.

The result of the lowest curve [48] and the two points [49] are measured by CC-DLTS on a sample which has received a strong hydrogen anneal [50,51]. The two measurement dots are the lowest interface state density values reported at present. Only 10^8 states per cm^2 are observed in the lower half of the band gap. On average, one state is observed in an area of $(1 \mu\text{m})^2$. Why the increase in a tail of states near the valence band is not observed, is not

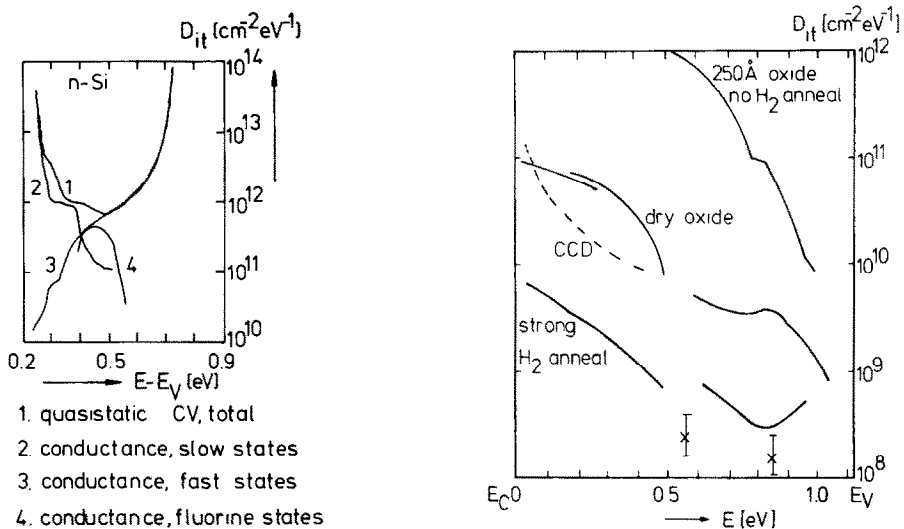


Fig. 11. Distribution of the interface state density D_{it} versus energy $E - E_V$. The measurements were performed by the quasistatic and the conductance technique with bandgap illumination [33]. Three types of states are resolved as indicated. The oxidation of the (100)Si sample to a thickness of 250 Å was performed in dry O₂ at 1150°C with no exposure to hydrogen. A 250 Å film of LaF₃ was deposited on the oxide by e-gun evaporation [33].

Fig. 12. Distribution of interface state density D_{it} versus energy E from the conduction band E_C to the valence band E_V . The top curve taken on the sample without hydrogen anneal is from fig. 11 (curve 3, fast states [33]). The curves in the center are for samples having standard dry oxides as used in devices. The CC-DLTS measurement is taken from refs. [53,5] and the CCD measurement is taken from ref. [32]. The CC-DLTS result of the lowest curve and the two dots [49] are taken on samples which have received a strong hydrogen anneal [50,51]. The CC-DLTS measurements are taken on n-type Si substrates to observe states in the upper half of the band gap and p-type Si to observe states in the lower half.

clear at present. These states may not be present at all in hydrogen annealed samples [54,20] or they may exhibit a very slow time constant so that they are not detected in the frequency/time constant range under investigation [20]. From the general trend it is concluded that all the curves describe the same type of interface state, the density of which may be reduced by strong hydrogen annealing.

A comparison of measurement results obtained by the conductance technique and CC-DLTS is shown in fig. 13. For more data see ref. [5]. Both measurements agree very well. With the above discussion on the resolution of the measurement techniques, we may conclude that in the tail from the conduction band in the residual low density of interface states, we only observe one type of state having one definite capture time constant at a given energy

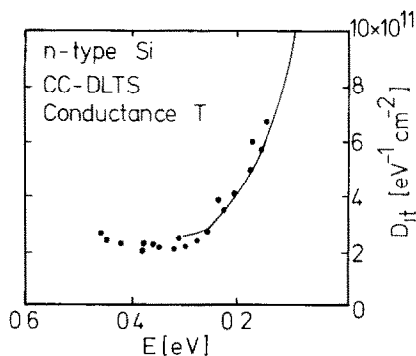


Fig. 13. Comparison of interface state measurements by CC-DLTS (solid line) and by the conductance technique (solid circles) on an n-type Si sample [5,21].

position. A distributed capture cross-section would cause a disagreement of the two measurement techniques as discussed above in fig. 9. However, the interface state density is distributed with respect to energy in the forbidden gap of silicon showing high values near the conduction band and low values near the valence band.

The characteristic peak in the interface state distribution in fig. 10 located at approximately 0.3 eV above the valence band maximum is frequently observed [3,60,54–56,64]. It is also strictly related to hydrogen and deuterium annealing [54–56,15]. The annealing behavior is shown in fig. 14. The capture cross-section determined is $\sigma = 5 \times 10^{-14} \text{ cm}^2$ [56]. The defect could not be related to the Pb spin center observed in EPR results [38] which showed a different annealing threshold [54,37,38].

Other peaks are observed in the D_{it} spectrum especially after bias-temperature stressing [62,151] and after irradiation [63,67,80,121,156–158]. The origin of these states is not well established or is due to impurities in the interface region [67,152].

3.2. Capture cross-sections

Typical capture cross-sections measured for electrons in the tail of the fast interface traps from the conduction band are shown in figs. 15 and 16. Values range from $\sigma_n = 10^{-17} - 10^{-14} \text{ cm}^2$ in a plateau near midgap [3,5]. Near the conduction band edge, the capture cross-section drops several orders of magnitude to values of less than $\sigma_n \leq 10^{-19} \text{ cm}^2$. The cross-section is independent of or very little dependent on temperature [32,57]. The magnitude of the cross-section seems to depend on processing and on the substrate orientation.

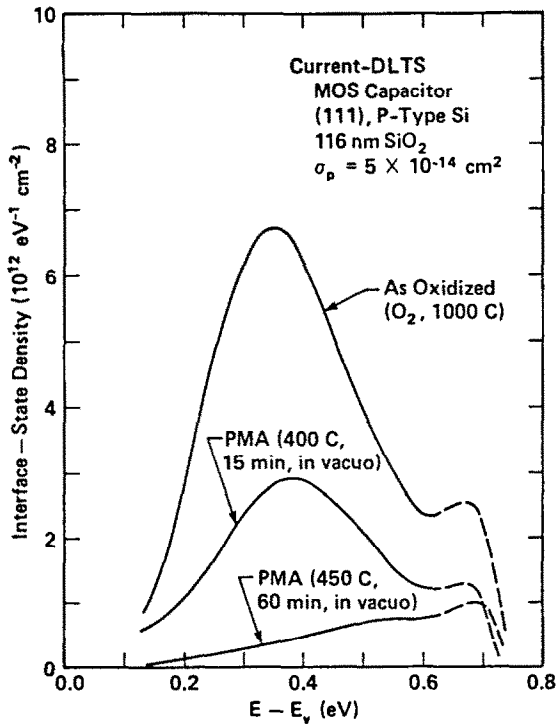


Fig. 14. Interface state density in the region of the characteristic peak approximately 0.3 eV above the valence band maximum. The density measured by DLTS is shown as-oxidized and for post-metallization anneals (PMA) as indicated [54].

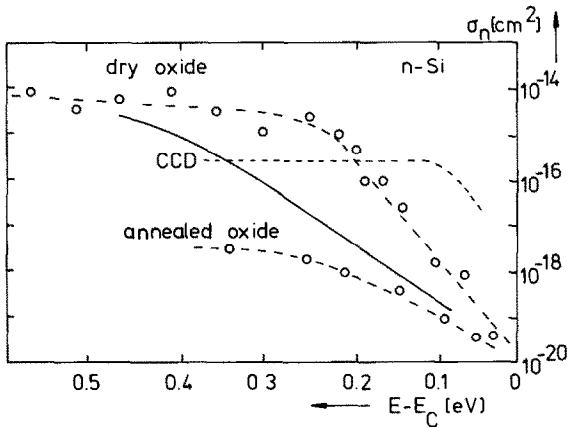


Fig. 15. Electron capture cross-section σ_n of fast interface states near the conduction band. Measurement points are shown for CC-DLTS results of dry oxide and dry oxide annealed at high temperatures. The dashed curve is taken from the CCD measurement of ref. [32]. The solid curve is taken from a transient measurement of ref. [27].

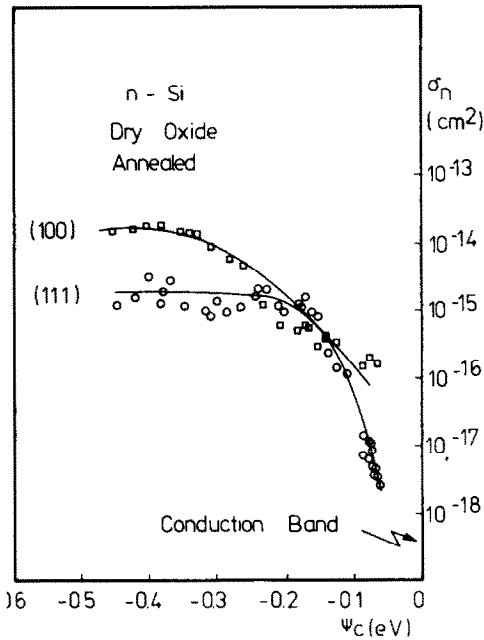


Fig. 16. Electron capture cross-section σ_n , measured for two surface orientations by the conductance technique on an n-type sample having dry oxide [3].

The results shown in figs. 15 and 16 are consistent with other measurements, e.g. in refs. [47,22,23,66] among others.

It is noted that only one definite time constant is measured for states at a given energy. The conductance measurement shows only one discrete resonance peak with a symmetrical smear-out to high and low frequencies (fig. 6). The symmetry is used as an argument that the increased width is due to potential fluctuations rather than to tunneling into states in SiO_2 which would cause an unsymmetrical resonance peak [53]. Potential fluctuations are also visible in transient measurements when the Fermi energy is varied [27].

The hole capture cross-section as shown in fig. 17 is measured in p-type Si. The measurement probably is somewhat obscured by the discrete peak around 0.3 eV above the valence band. However, the hole cross-section seems to assume high values $\sigma_p \approx 10^{-14}\text{--}10^{-15} \text{ cm}^2$ near the valence band [28,31,27,2] rather than to decrease as it does near the conduction band. Slow time constants are reported for hole capture especially for low interface state densities [58,3]. These properties still have to be confirmed. Slow capture rates may be due to the valence band tail of interface states [33] which is not

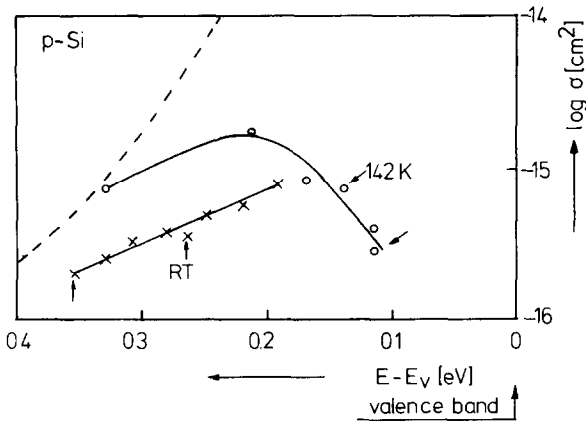


Fig. 17. Hole capture cross-section σ_p of fast interface states in the lower half of the Si bandgap. Measurement points are shown for conductance measurements on two samples [5]. The dashed line represents a result obtained by transient measurements taken from ref. [27].

observed by CC-DLTS or the conductance technique [5,20].

Interface states may also be excited by shining infrared light on the MOS sample [34–36,74]. Optical cross-sections determined for the transition assume very low values $\sigma^0 \leq 10^{-19} \text{ cm}^2$ for states near the conduction band.

The magnitude of the cross-sections suggests that the fast states behave like acceptors in agreement with the charge variation in the CV analysis [59,61,36]. However, since in capacitance measurements, only the charge change is measured, it is very difficult to determine the absolute charge value of interface states, especially at the low densities which are state of the art. The problems associated with the $C-V$ measurement in the determination of trap charge, e.g. donor- or acceptor-type, are discussed in ref. [4]. The properties of charge fluctuations, for instance, are in favor of donor-type behavior of the fast interface states (see below). The trap type therefore is still uncertain.

3.3. Effects of processing

The continuous decrease of the interface state density over the past twenty years is a hint that impurities and technology may play an important role because the cleanliness standards in semiconductor technology have been continuously improved.

Strong reduction of the interface state density with hydrogen annealing is already seen in figs. 12 and 14. Both, the fast interface states near the conduction band and those in the peak near 0.3 eV above the valence band maximum, are reduced in the presence of hydrogen or water at elevated temperatures. This effect of hydrogen is confirmed by many other studies

[59,60,4,154]. It is generally accepted that hydrogen saturates some forms of unsaturated bonds in the oxide and at its interface to silicon, thus removing interface states from the silicon bandgap energy region [68,69].

Detailed processing studies of interface state and oxide charge have been performed [59,70,61,4]. The results are still not conclusive because of the complex nature of interface states. A proportionality of the interface state density to the fixed oxide charge is frequently observed [59,71]; both follow Deal's oxidation triangle which predicts an increased density of oxide charge and interface state density for decreasing oxidation temperature [70]. The (111) orientation generally yields higher values of both oxide charge and interface state density [70,59,72,3,4]. However, annealing in dry nitrogen and argon may result in a decrease of the oxide charge and an increase in interface state density [59,60]. Hydrogen annealing is not as effective in removing the oxide charge as it is in reducing the fast interface states [59]. The processing also seems to affect the energy dependence of the capture cross-section (figs. 15 and 16). The variations observed are beyond the error of the determination.

At present it is not possible to draw conclusions on the origin of interface states based on the technological behaviour. The effects may be rather indirectly caused by the reaction kinetics and its influence on an interfacial layer than directly by creating and annihilating interface states [84,81-85].

3.4. Impurity effects

Impurities have been intentionally introduced into the SiO₂-Si system in order to examine specific effects. Ion implantation was used to introduce many different impurities [67,66]. Many discrete defects in the interface region have been observed; these defects, however, are mostly related to ion implantation effects. Very often, radiation damage levels of the silicon substrate are observed [67,30].

Introduction of heavy metals into the interface before the oxide growth shows little direct effect on interface state densities, which can be attributed to a specific defect caused by the impurity [75-77]. In thin SiO₂ films, the contact metal may penetrate to the interface and cause discrete peaks [78]. An increase of the interface state density is observed when the semiconductor substrate is doped by donors or acceptors in excess of $N > 10^{17} \text{ cm}^{-3}$ [79]. This effect may again be related to the oxidation kinetics which is also affected by large doping concentrations [81-83].

It is known that alkali ions cause a positive charge in the oxide [87-89]. Especially, sodium causes a drift instability in devices and has to be removed or neutralized by chlorine [90]. Cesium generates a stable positive charge in SiO₂ [90,91,3].

A trap level associated with the sodium ion in SiO₂, which is located well above the Si conduction band edge, cannot be related to interface states [93].

An impurity band of fast states, which is related to Na⁺ ions in SiO₂, is observed in the conductivity of MOSFET channels at low temperatures of 4–70 K [94–96]. The result is shown in fig. 18. A peak in the channel conductance is observed which is associated to either thermally activated conductivity from an impurity level or to hopping in an impurity band 15–30 meV below the conduction band edge [94,108].

The observations are explained by the charge model of interface states [99,100] which assumes that electrons in Si are bound to positively charged Na⁺ ions in SiO₂ similarly as to a donor center in silicon (see fig. 26). The bound electron, however, remains in silicon because the interface barrier repels the charge carriers. The experimental results of the impurity band conductivity just below the conduction band seem to be in good agreement to the theoretical predictions of a shallow binding energy for the assumption of Na⁺ ions close to the interface. This assumption, however is partly contradictory to the trapping properties of sodium observed in SiO₂. The trapping occurs further away from the interface [93]. The sodium also tends to agglomerate and to cause gross potential fluctuations at the interface [101,102,16]. The resolution of an impurity state at 10–30 meV below the conduction band edge requires potential fluctuations of less than 30 meV. This is less than the fluctuations observed in state of the art clean samples (see above and refs. [103–106]). With

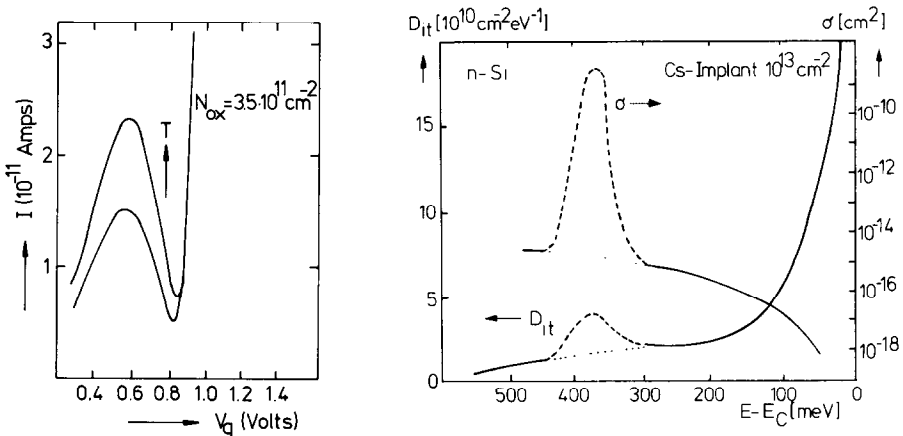


Fig. 18. Conductance in a MOSFET channel at low temperatures versus gate voltage. Impurity band conductivity is observed below the mobility edge of the conduction band. After Fowler and Hartstein [94].

Fig. 19. Density of interface states D_{it} and electron capture cross-section σ observed by CC-DLTS for a Cs contaminated MOS capacitor. Cs⁺ implantation was performed into the bare Si surface before dry oxidation of the wafer at 1050°C. The discrete peak (dashed line) is caused by residual radiation damage. It does not correspond to the energy scale given.

the presence of sodium, the fluctuations should be even worse. However, if the interface states are donor centers, the charge fluctuations may disappear at low temperatures when all the donor states are neutral and the charge is well screened. A donor-type charge behavior of the centers is also deduced from the variation of charge fluctuations at shallow energies in clean samples [106].

Very small contributions to fast interface states are measured for sodium by transient spectroscopy [16,18]. A spectrum of interface states as measured by CC-DLTS is shown in fig. 19 for the case of the stable Cs contamination and in fig. 20 for Na contamination. In both cases, the alkali contamination was introduced in a controlled quantity by ion implantation into the bare Si surface before oxidation. The interface state measurement is possible by CC-DLTS because it is not affected by potential fluctuations (see above, fig. 8). Cs^+ ions do not drift in SiO_2 at room temperature. Sodium may be drifted at room temperature to and away from the interface by an appropriate electric field applied; however, it is also frozen in at low temperatures so that a measurement is possible. Fig. 19 also shows an implantation damage level which is not completely removed by the high-temperature treatment. In the midgap region, the interface state density is not affected by the presence of sodium. A steep increase of the interface state density is observed near the

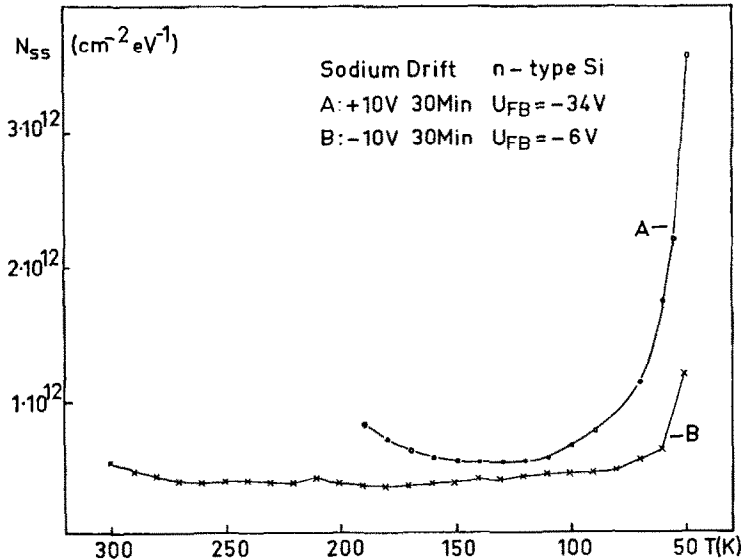


Fig. 20. Density of interface states observed by CC-DLTS for a sodium-contaminated MOS structure. The signal observed at low temperature corresponds to states near the conduction band. The signal at high temperature is due to states near midgap. Sodium ions are drifted to the interface (curve A) and away from the interface (curve B).

conduction band edge in accordance with the shallow impurity state observed in the MOSFET conductance in fig. 18. However, the capture cross-section decreases in the same manner as for the fast states in fig. 15. The interface state density observed for the high sodium contamination is generally high. Drift of sodium shows an effect near the conduction band edge where an increased density is observed when sodium is drifted to the interface.

Both, the standard interface state density measurement techniques and the MOSFET channel conductance indicate a strong impurity band close to the conduction band edge. Puzzling is the absence of potential fluctuations which would indicate the donor-type behavior of the binding of an electron to the positive charge. This is, however, in contradiction to the low capture cross-section measured which does not indicate an attractive Coulomb potential. Speculations on a repulsive barrier proposed to explain the slow trapping of the sodium oxide trap [93], may also be valid for the interface states. It is also possible that the shallow attractive Coulomb centers are not observed in transient spectroscopy because the time constant is too fast.

3.5. Thin SiO_2 films

For oxides thinner than 40–20 Å, most of the studies were performed by tunneling experiments [109,153]. Interface states are difficult to determine because of the tunneling current through the SiO_2 and the high capacitance of the thin oxide. Structures in the transition region of thin to thick oxides, which is around ≥ 40 Å, already permit an interface state measurement. Tunneling [41] and conductance measurements [78,110,111] show that the general behavior of the interface state density is the same as in thick oxides; however, the density observed is much larger (approximately $D_{it} = 10^{11}$ – 10^{12} cm^{-2} eV^{-1}) than for state of the art thick oxides. The high density may be due to the oxidation technology which has to be different because of the low growth rate required, and it may be due to the effect of the transition interfacial layer which is present in thick oxides and which is not well developed in thin oxides.

Thin oxides may easily be studied by standard MOS techniques when a top layer of nitride (MNOS) or another insulating film is deposited so that a normal capacitor is obtained. A result has already been shown in fig. 11 where the similarity of the interface state properties is clearly demonstrated. A result observed on an MNOS structure is presented in fig. 21. The density of interface states observed is high, in the order of a few 10^{11} cm^{-2} eV^{-1} . The disagreement between the measurement result obtained by CC-DLTS and the quasistatic C - V measurement in fig. 21a is explained by the sensitivity of the C - V measurement to tunneling through the thin SiO_2 to nitride traps which contribute to the density of states observed. The CC-DLTS technique is too fast, so that only states right at the interface are sensed. The measurement in fig. 21b for a slightly thicker oxide shows good agreement of the two tech-

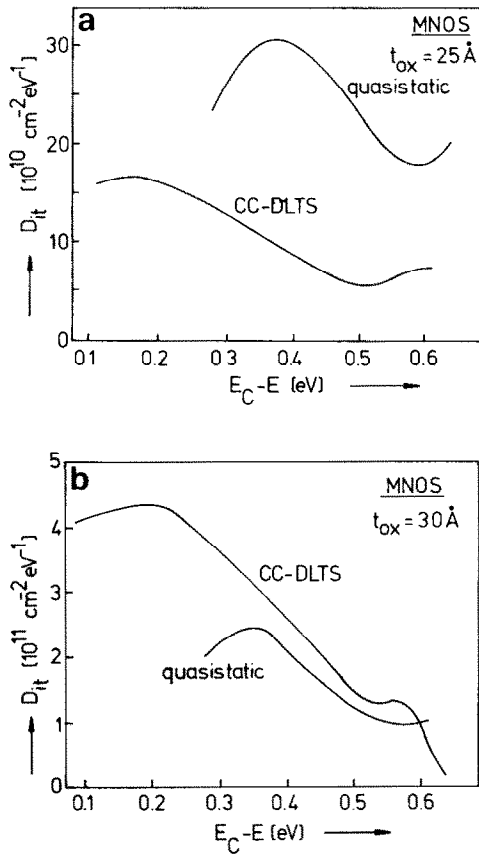


Fig. 21. Interface state distribution measured in an MNOS structure having a 25 Å SiO₂ film (a) and a 30 Å SiO₂ film (b). The measurements are performed by CC-DLTS and the quasistatic CV technique. The difference observed between the two measurements for the thin SiO₂ film is due to tunneling into nitride traps [49].

niques because tunneling is also inhibited in the quasistatic technique. The result is in agreement with experiments performed by pulsed charging of nitride traps [112] and demonstrates very well the various properties of the measurement techniques discussed in section 2.4. Annealing or stressing of the MNOS structure influences the interface state density distribution due to reactions and interpenetration of the nitride and the oxide [135,136].

It is generally accepted that an interfacial layer also exists for the standard MOS structure [84–86]. In the interfacial layer, the oxide varies with respect to stoichiometry [84,113–115] and with respect to strain because of the lattice mismatch [117,118]. The interface shows roughness of the order of 10 Å in

TEM micrographs [119,120]. On a direct relation of this interfacial layer on interface states can only be speculated in the models proposed which are discussed in section 4.

3.6. Lateral non-uniformities

Potential fluctuations are observed in the conductance technique (fig. 6) [2,66,103,104,106,155] and are also observed in transient spectroscopy [27,21]. The fluctuations are uniformly distributed in the capacitor with a minimal fluctuation length of $\lambda \approx 70\text{--}200 \text{ \AA}$ [105,103,106]. In state of the art clean MOS samples, the variance of the potential fluctuations is a few kT at room temperature corresponding to $30\text{--}70 \text{ meV}$ (fig. 6) or larger [2,66,103,106]. In the presence of sodium or after stressing, the fluctuations may be considerably larger.

A considerable number of interface states may occur at boundaries of small gate structures [121]. The double-gate structure shown in fig. 22 having a large boundary-to-area ratio has been used to study the interface state density at gate boundaries by CC-DLTS measurements. The result obtained is shown in fig. 23. CC-DLTS is advantageous in this measurement because it is not affected by the potential variations inherent to the boundary region. One gate of the double-gate structure is used as a guard electrode to vary the contribution of interface states in the boundary region to the transient measurements. The interface state density is increased by a factor of 100 from the value $D_{it} < 10^9 \text{ cm}^{-2} \text{ eV}^{-1}$ in the bulk gate area to $D_{it} > 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ in the

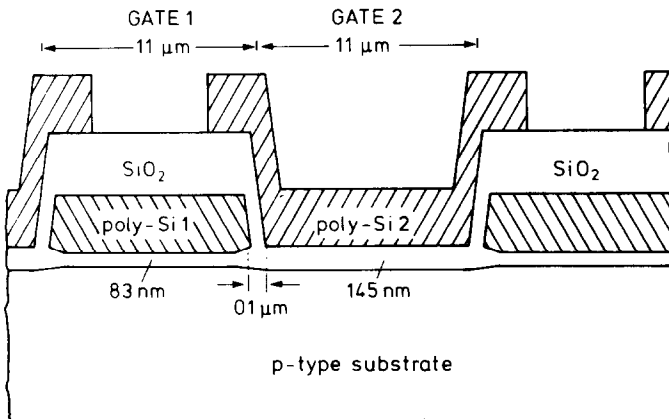


Fig. 22. Schematic view of the double-gate striped MOS capacitor structure used in the study of the interface state boundary effect. The structure consists of 2×32 narrow ($11 \mu\text{m}$) and long ($700 \mu\text{m}$) stripes adding up to a total gate area of $2 \times 0.26 \text{ mm}^2$ [48].

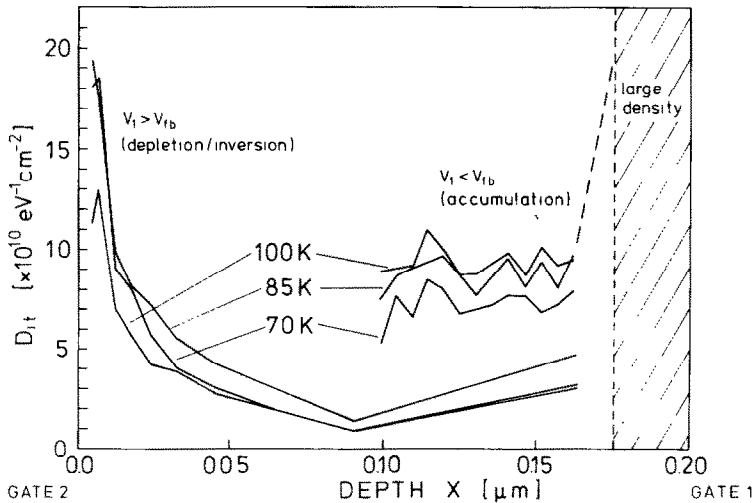


Fig. 23. Interface state density D_{it} versus depth x in the transition region of the striped structure in fig. 22. Two sets of curves are obtained depending on different evaluations in the accumulation and in the depletion/inversion regions of gate 1, respectively. The discrepancy indicates the error of the measurement. A large density of interface states is present in the immediate boundary of the two gates [48].

immediate boundary of the gates. The origin of these interface states is not known. It may be related to strain induced by the processing technology.

3.7. Irradiation effects

The irradiation effects in SiO₂ may be broadly classified into two major categories [80]: (a) in ionizing effects and (b) in atomic displacement damage. In the first category, an electron-hole pair is generated in the SiO₂ by irradiation at sufficiently high energy (> 9 eV), e.g. by X-rays, γ -rays, or MeV electrons. Atomic displacement is mainly observed after ion implantation.

The most commonly observed effects of ionizing radiation (category (a)) are a build-up of positive charge in SiO₂ inherent with a build-up of interface states [122,123]. In SiO₂ films thinner than 50 Å no additional interface states have been detected [124]. Traps are also induced in the oxide, which become affective after carrier injection [125,126].

It is generally accepted that electron-hole pairs generated by the irradiation are partly separated in the SiO₂ before recombining. Since electrons have a large mobility they can reach the electrodes leaving behind the rather immobile holes which are trapped in the SiO₂ [122]. A high concentration of hole traps

exists near the SiO₂-Si interface in the interfacial layer [127]. The presence of an electric field serves to separate the electron-hole pairs and to redistribute the charge depending on the orientation of the electric field [128].

The interface state build-up has been found to occur even for non-penetrating radiation [129] and occurs only after the positive charge has been transported to the interface [130]. This behavior suggests the charge model again for the interface states. The interface states created are not limited to the vicinity of the conduction band edge, so that chemical bond breaking and transport of H and OH ions are also very likely [123,80,131]. All the model speculations for the interpretation of interface states are more or less also valid for the irradiation effects [123]. No preference to any particular model can be given at present.

3.8. Bulk states in Si

Bulk trap centers are frequently observed in MOS structures by DLTS especially after ion implantation [16,18,30], because DLTS is sensitive to the total number of bulk states in the space charge region. In fig. 19, the peak is probably caused by a bulk level due to ion implantation damage. Several bulk levels are observed after oxygen implantation into the interface and low-temperature annealing at 600°C (fig. 24). Besides the well known level at 0.11 eV

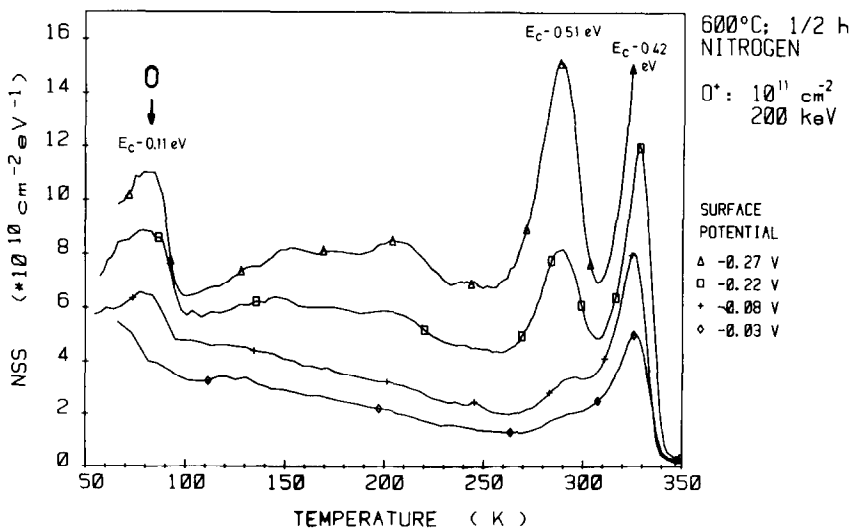


Fig. 24. Interface state density measured by CC-DLTS in a temperature scan for various surface potentials. The samples has received a low-dose of oxygen implanted into the interface region and is moderately annealed at 600°C for half an hour. Peaks are due to bulk states in Si which are related to oxygen and radiation damage [49].

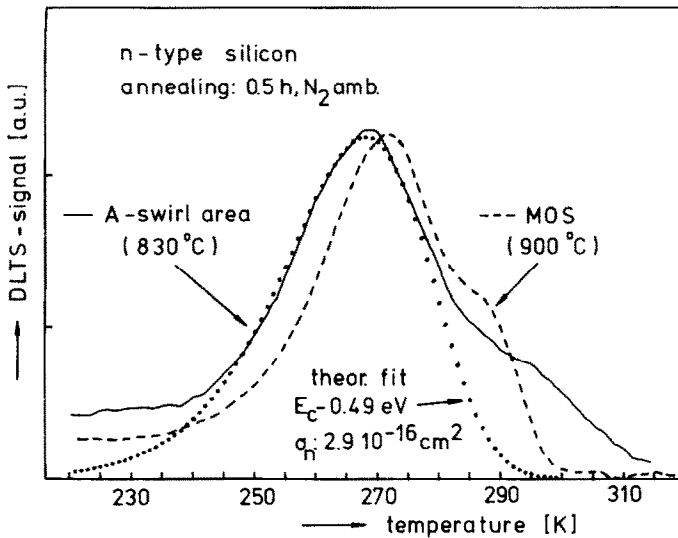


Fig. 25. Bulk level $E_C - 0.49$ eV observed by CC-DLTS in standard dry oxide after 900°C annealing. The DLTS signal observed in bulk silicon containing swirl defects (possibly interstitial Si) is shown for comparison [132].

attributed to oxygen two more bulk levels are observed. Bulk levels are identified by their sharp and discrete structure. They strongly decrease in density with a reduced width of the space charge region as is demonstrated by the surface potential variation in fig. 24.

An intrinsic level at $E_C - 0.49$ eV ($\sigma_n = 2.9 \times 10^{-16} \text{ cm}^2$) associated with the SiO_2 -Si interface is shown in fig. 25. This level is observed after high-temperature annealing of the MOS structure. This level is remarkable because the same level is observed in bulk silicon containing swirls [132]. It possibly is a level of interstitial Si which is also expected to be generated during oxide growth [81–83]. Another bulk level in the lower half of the band gap at $E_V + 0.30$ eV ($\sigma_n = 3 \times 10^{-16} \text{ cm}^2$, $N_T = 9 \times 10^{12} \text{ cm}^{-3}$) is reported for standard oxides in ref. [133]. After growing thick oxides at high pressures and at low temperatures, several defects have been observed in bulk silicon when the thick oxide was stripped [134].

4. Theoretical models

The very low density of interface states results from the fact that there are no interface states in the band gap region of Si for a Si surface when all the bonds are saturated by the SiO_2 surface film. Computations using various

techniques all show that levels due to bonds at the silicon surface are removed from the gap region and bonding states are created several eV or more below the valence band maximum [137–142]. States observed at the interface are therefore created by defects, e.g. broken bonds, impurities or other imperfections (e.g. bond angle distortions). Theoretical calculations on defect states are still limited in accuracy and reliability [138,140] and also the basis for the model assumptions is still speculative although plausibility considerations may favor one or the other model [4]. A selection of models are given in the following subsections with some arguments in favor or with experimental data which make this model less likely.

4.1. Charge model

The charge model or effective mass approximation model [99,100,3,4] has already been discussed in section 3.4. A hydrogenic binding energy of 15–30 meV is estimated in effective mass approximation when electrons in the Si conduction band are bound to the positive Na^+ ions in the SiO_2 . The sodium ions have to be a few Å units close to or at the interface. The sodium ions cannot be neutralized because they are energetically inaccessible. The electronic wave function is mainly kept in the silicon because of the high SiO_2 barrier. The potential trough and the electronic wave function are sketched in fig. 26.

The shallow centers of the charge model are possibly observed in the low-temperature channel conductance of sodium-contaminated MOSFETs. The low capture cross-section measured by CC-DLTS and the low trapping probability of the Na^+ ions in SiO_2 indicate that the situation may not be that simple. Potential fluctuations which are expected to be larger than 30 meV are expected to mask the observed conductance peak.

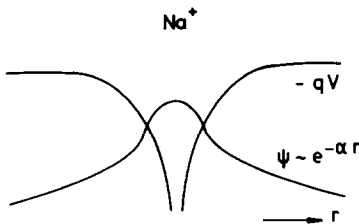


Fig. 26. Potential through due to Na^+ ions in SiO_2 close to the interface and the wave function of an electron in Si bound to the potential well. The wave functions fall off as $\exp(-\alpha/r)$ in effective mass approximation.

still very speculative. It only explains the properties experimentally observed and does not yield information on the defect itself.

Bond angle distortions may cause a tail of states from the Si conduction band [138] in good accordance with the experimental observations. Such states would be of acceptor type [148]. The bond angle of Si-O is very soft and may easily be distorted at the interface [149]. An impression of the distorted interface is shown in fig. 28. This interpretation seems very likely, especially because interface states are strongly affected by strain in the interface; however, distorted bonds cannot or only indirectly account for the strong hydrogen and water annealing effects of interface states which support a real bonding defect which may be saturated rather than just a distortion of a bond angle. EPR does not show any bond angle distortion of the dangling bond at the silicon surface independent of the orientation of the surface plane [37].

4.3. Microscopic defect structure

Possible microscopic defect structures that may occur at the interface are listed in refs. [123,60,150,161] among other references. The structures are shown in fig. 29. The most likely defect is the trivalent silicon $\equiv\text{Si}\cdot$, a silicon surface dangling bond. The trivalent silicon acts as a donor center and is calculated to generate a level at approximately midgap energy position [138]. The trivalent silicon center has been identified by EPR in as-oxidized MOS structures showing a high interface state density and showing especially the interface state peak just below midgap. It has been suggested [15] that this peak may be due to the trivalent silicon donor, but recent annealing studies [54] show different annealing thresholds of the trivalent silicon EPR center and

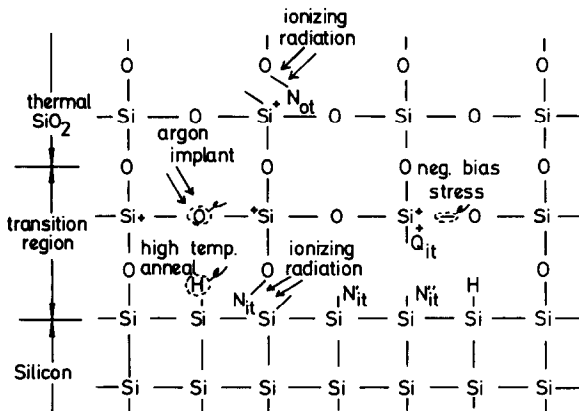
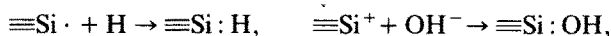


Fig. 29. Schematics of the microscopic and chemical SiO₂-Si interface structure showing possible defects and the mechanism introducing them. After Deal [60].

the interface state peak, so that the identification is still open. A complicated behavior of the trivalent Si is predicted [162]. The trivalent Si may be saturated by hydrogen or OH groups according to



where the centers created are assumed to be electrically inactive. The strong hydrogen annealing effect can therefore easily be explained.

Other defects shown in fig. 29 are believed to mainly occur after various kinds of excitations as indicated and to be mainly responsible for the oxide charge and oxide traps. Such defects are [123,60,161]:

$\equiv\text{Si}-\text{O}\cdot$	non-bridging oxygen	single acceptor or amphoteric;
V_{O}	oxygen vacancy ($=\text{Si}\cdot \cdot \text{Si}=\text{}$)	double donor;
V_{Si}	silicon vacancy	single donor or amphoteric;
Si_i	interstitial silicon	double donor;
O_i	interstitial oxygen	single donor or amphoteric.

These defects could so far not be identified by EPR. Interstitial silicon which is produced by the oxidation is a likely candidate for the oxide charge.

5. Conclusions

Capacitance measurements, e.g. the conductance technique and transient spectroscopy and combinations thereof are the only measurement techniques which are sufficiently sensitive to measure the residual interface state densities in state of the art SiO₂-Si structures. An interface state density as low as $D_{\text{it}} = 10^8 \text{ cm}^{-2} \text{ eV}^{-1}$ is observed because bonding states are completely removed from the energy region of the silicon band gap by saturating the silicon bonds with oxygen and the remaining defects due to imperfections by H or OH groups.

Only one type of interface state is observed after strong hydrogen annealing, the density of which continuously decays from $D_{\text{it}} \geq 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ near the conduction band minimum to values $D_{\text{it}} \leq 10^8 \text{ cm}^{-2} \text{ eV}^{-1}$ in the lower half of the Si band gap. A similar tail from the valence band is only observed for high interface state densities in samples having no strong hydrogen annealing received or for thin oxides.

A peak of interface state density observed without hydrogen annealing of the MOS sample may be due to trivalent silicon dangling bonds at the interface. The tail of states from the conduction band may be due to bond angle distortions or due to a discrete SiO₂ trap, the energy of which is dependent on the distance in the interfacial layer from the silicon surface.

A binding of electrons in silicon to the positive charge of alkali ions in SiO₂ is possibly observed in the conductance of MOSFETs at low temperatures.

Additional types of interface states are observed after various technological treatments and especially after irradiation of MOS structures. The experimental results known at present are insufficient to prefer one of the many possible origins of the defect nature.

Acknowledgements

The author is grateful to K. Hofmann for giving permission to present some of his experimental results prior to publication. The critical reading of the manuscript and comments by G. Pensl, K. Hofmann, and H. Lefevre are very much appreciated.

References

- [1] B.E. Deal, *J. Electrochem. Soc.* 127 (1980) 979.
- [2] A. Goetzberger and S.M. Sze, in: *Applied Solid State Science*, Vol. 1, Eds. R. Wolfe and C.J. Kiessmann (1969) p. 154.
- [3] A. Goetzberger, E. Klausmann and M. Schulz, *CRC Critical Rev. Solid State Sci.* 6 (1976) 1.
- [4] Y.C. Cheng, *Progr. Surface Sci.* 8 (1977) 181.
- [5] M. Schulz, K. Blumenstock and E. Klausmann, in: *Semiconductor Silicon 1981*, *Electrochem. Soc. Proc. Vol. 81-5*, Eds. H.R. Huff, R.J. Kriegler and Y. Takeishi (Electrochem. Soc., Princeton, NJ, 1981) p. 463.
- [6] P. Balk, Ed., *The Si-SiO₂ System* (Elsevier, Amsterdam, 1983).
- [7] J. Giber, in: *New Developments in Semiconductor Physics*, *Lecture Notes in Physics*, Vol. 122, Eds. F. Beleznyay, G. Ferenczi and J. Giber (Springer, Berlin, 1980) p. 226.
- [8] E.H. Nicollian and J.R. Brews, *MOS (Metal-Oxide-Semiconductor) Physics and Technology* (Wiley, New York, 1982).
- [9] S. Pantelides, Ed., *The Physics of SiO₂ and its Interfaces*, *Proc. Intern. Topical Conf.*, Yorktown Heights, NY (Pergamon, New York, 1978).
- [10] G.G. Roberts and M.J. Morant, Eds., *Insulating Films on Semiconductors*, *Proc. Intern. Conf. on Insulating Films on Semiconductors (INFOS 79)*, Durham, UK, *Inst. Phys. Conf. Ser.* 50 (Inst. Phys., Brighton, 1979).
- [11] G. Lucovsky, S.T. Pantelides and F.L. Galeener, Eds., *The Physics of MOS Insulators*, *Proc. Intern. Topical Conf.*, Raleigh, NC (Pergamon, New York, 1980).
- [12] M. Schulz and G. Pensl, Eds., *Insulating Films on Semiconductors*, *Proc. Intern. Conf. on Insulating Films on Semiconductors (INFOS 81)*, Erlangen, *Springer Series in Electrophysics* No. 7 (Springer, Berlin, 1981).
- [13] E.H. Nicollian and A. Goetzberger, *Bell Syst. Techn. J.* 46 (1967) 1055.
- [14] H. Deuling, E. Klausmann and A. Goetzberger, *Solid State Electron.* 15 (1972) 559.
- [15] N.M. Johnson, D.J. Bartelink and M. Schulz, in ref. [9], p. 42.
- [16] M. Schulz and E. Klausmann, *Appl. Phys.* 18 (1979) 169.
- [17] K.L. Wang and A.o. Ewvaraye, *J. Appl. Phys.* 47 (1976) 4574.
- [18] K.L. Wang, in: *Semiconductor Silicon 1977*, *Electrochem. Soc. Proc. Vol. 77-2*, Eds. H.R. Huff and E.H. Sirtl (Electrochem. Soc., Princeton, NU, 1977) p. 404.
- [19] D.V. Lang, *J. Appl. Phys.* 45 (1974) 3023.
- [20] M. Schulz and N.M. Johnson, *Appl. Phys. Letters* 31 (1977) 622.

- [21] E. Klausmann, in ref. [10], p. 97.
- [22] T.C. Poon and H.C. Card, *J. Appl. Phys.* 51 (1980) 6273.
- [23] T.C. Poon and H.C. Card, *J. Appl. Phys.* 51 (1980) 5881.
- [24] H. Lefevre and M. Schulz, in ref. [6].
- [25] J.A. Cooper and R.J. Schwartz, *Solid State Electron.* 17 (1974) 641.
- [26] J. Boucher and M. Lescure, in ref. [12], p. 165.
- [27] T.J. Tredwell and C.R. Viswanathan, *Appl. Phys. Letters* 36 (1980) 460.
- [28] N.M. Johnson, *Appl. Phys. Letters* 34 (1979) 802.
- [29] K.L. Wang, *IEEE Trans. Electron Devices* ED-26 (1979) 819.
- [30] K. Yamasaki, M. Yoshida and T. Sugano, *Japan. J. Appl. Phys.* 18 (1979) 113.
- [31] K. Asada and R. Sugano, *Rev. Sci. Instr.* 53 (1982) 1001.
- [32] R.J. Kriegler, T.F. Devenyi, K.D. Chick and J. Shappir, *J. Appl. Phys.* 50 (1979) 398.
- [33] A. Sher, Y.H. Tsuo, P. Su and W.E. Miller, in ref. [11], p. 236;
A. Sher, Y.H. Tsuo, P. Su and W.E. Miller, *J. Appl. Phys.* 50 (1979) 398.
- [34] K. Blumenstock and M. Schulz, in ref. [12], p. 48.
- [35] D.W. Greve and W.E. Dahlke, in ref. [10], p. 107.
- [36] R.F. Pierret and B.R. Roesner, *Appl. Phys. Letters* 24 (1974) 8.
- [37] E.H. Poindexter and P.J. Caplan, in ref. [12], p. 150;
P.J. Caplan, E.H. Poindexter, B.E. Deal and R.R. Razouk, *J. Appl. Phys.* 50 (1979) 5847.
- [38] C. Bunstrom and C. Svensson, *Solid State Commun.* 37 (1981) 219.
- [39] Y. Nishi, *Japan. J. Appl. Phys.* 10 (1971) 52.
- [40] G. Mendz and D. Haneman, *Appl. Phys.* A26 (1981) 87.
- [41] J. Maserjian and N. Zamani, *J. Appl. Phys.* 53 (1982) 559.
- [42] M. Kuhn, *Solid State Electron.* 13 (1970) 873.
- [43] K. Ziegler and E. Klausmann, *Appl. Phys. Letters* 26 (1975) 400.
- [44] P.V. Gray and D.M. Brown, *Appl. Phys. Letters* 8 (1966) 31;
P.V. Gray, *Proc. IEEE* 57 (1969) 1543.
- [45] M.R. Boudry, *Appl. Phys. Letters* 22 (1973) 530.
- [46] T.P. Ma and R.C. Barker, *Solid State Electron.* 17 (1974) 913.
- [47] M. Morita, K. Tsubouchi and N. Mikoshiba, *Appl. Phys. Letters* 33 (1978) 745.
- [48] X.Q. Zheng, K. Hofmann, M. Schulz and L. Risch, *J. Appl. Phys.* 53 (1982) 9146.
- [49] K. Hofmann, private communication.
- [50] L. Risch, E. Pammer and K. Friedrich, in ref. [10], p. 114.
- [51] L. Risch, in ref. [12], p. 43.
- [52] M.R. Boudry, *J. Phys. E (Sci. Instr.)* 11 (1978) 237.
- [53] M. Schulz, in ref. [10], p. 87.
- [54] N.M. Johnson, D.K. Biegelsen and M.D. Moyer, in ref. [12], p. 35.
- [55] N.M. Johnson, D.K. Biegelsen, M.D. Moyer, V.R. Deline and C.A. Evans, Jr., *Appl. Phys. Letters* 38 (1981) 995.
- [56] N.M. Johnson, D.J. Bartelink and J.P. McVittie, *J. Vacuum Sci. Technol.* 16 (1979) 1407.
- [57] M. Schulz and N.M. Johnson, *Solid State Commun.* 26 (1978) Erratum.
- [58] J.A. Cooper, Jr. and R.J. Schwartz, *Solid State Electron.* 17 (1974) 641.
- [59] R.R. Razouk and B.E. Deal, *J. Electrochem. Soc.* 126 (1979) 1573.
- [60] B.E. Deal, in: *Semiconductor Silicon 1977*, *Electrochem. Soc. Proc. Vol. 77-2*, Eds. H.R. Huff and E. Sirtl (*Electrochem. Soc., Princeton, NJ*, 1977) p. 276.
- [61] J.L. Pautrat and J.C. Pfister, *Phys. Status Solidi (a)* 11 (1972) 669.
- [62] A. Goetzberger, A.D. Lopez and R.J. Strain, *J. Electrochem. Soc.* 120 (1973) 90.
- [63] E. Rosencher, A. Chantre and D. Bois, in ref. [11], p. 331.
- [64] Y.T. Yeow, D.R. Lamb and S.D. Brotherton, *J. Phys. D10* (1977) 83.
- [65] H. Flietner, W. Füssel and N.D. Sinh, *Phys. Status Solidi (a)* 43 (1977) K99.
- [66] W. Fahrner and A. Goetzberger, *Appl. Phys. Letters* 17 (1970) 16.

- [67] W. Fahrner and A. Goetzberger, *Appl. Phys. Letters* 21 (1972) 329.
- [68] E. Kooi, *Philips Res. Rept.* 20 (1965) 578.
- [69] P. Balk, *Electrochem. Soc. Meeting* (1965) Abstr. 11.
- [70] B.E. Deal, *J. Electrochem. Soc.* 121 (1974) 1980.
- [71] W.M. Werner, *J. Electrochem. Soc.* 123 (1976) 540.
- [72] E. Arnold, J. Ladell and G. Abowith, *Appl. Phys. Letters* 13 (1968) 413.
- [73] W. Fahrner and A. Goetzberger, *Appl. Phys. Letters* 44 (1973) 725.
- [74] E. Kamieniecki and R. Nitecki, in ref. [9], p. 417;
E. Kamieniecki, *Solid State Electron.* 16 (1973) 1487.
- [75] P.F. Schmidt and L.P. Adda, *J. Appl. Phys.* 45 (1974) 1826.
- [76] G. Kaden, *Phys. Status Solidi (a)* 3 (1970) 161.
- [77] M. Schulz, E. Klausmann and A. Hurre, *CRC Critical Rev. Solid State Sci.* 5 (1975) 319.
- [78] S. Kar and W. Dahlke, *Solid State Electron.* 15 (1972) 869.
- [79] J. Snel, in ref. [10], p. 119.
- [80] T.P. Ma, in: *Semiconductor Silicon 1981*, *Electrochem. Soc. Proc. Vol. 81-5*, Eds. H.R. Huff, R.J. Kriegler and Y. Takeishi (*Electrochem. Soc.*, Princeton, NJ, 1981) p. 427.
- [81] J.D. Plummer, in: *Semiconductor Silicon 1981*, *Electrochem. Soc. Proc. Vol. 81-5*, Eds. H.R. Huff, Kriegler and Y. Takeishi (*Electrochem. Soc.*, Princeton, NJ, 1981) p. 445.
- [82] W.A. Tiller, *J. Electrochem. Soc.* 127 (1980) 619.
- [83] C.P. Ho and J.D. Plummer, *J. Electrochem. Soc.* 126 (1979) 1516, 1523.
- [84] C.R. Helms, in ref. [12], p. 19;
C.R. Helms, *J. Vacuum Sci. Technol.* 16 (1979) 608.
- [85] T. Sugano, *Surface Sci.* 98 (1980) 145.
- [86] T. Sugano, J.J. Chen and T. Homano, *Surface Sci.* 98 (1980) 154.
- [87] E.H. Snow, A.S. Grove, B.E. Deal and C.T. Sah, *J. Appl. Phys.* 36 (1965) 1664.
- [88] S.R. Hofstein, *IEEE Trans. Electron Devices* ED-13 (1966) 222.
- [89] T. Hickmott, *Appl. Phys. Letters* 22 (1973) 267.
- [90] R.J. Kriegler, *Denki Kagaku* 41 (1973) 466.
- [91] G. Sixt and A. Goetzberger, *Appl. Phys. Letters* 19 (1971) 478.
- [92] G. Sixt, M. Schulz and A. Goetzberger, *Appl. Phys.* 4 (1974) 217.
- [93] D.J. DiMaria, *J. Appl. Phys.* 52 (1981) 7251.
- [94] A.B. Fowler and A. Hartstein, *Phil. Mag.* B42 (1980) 949.
- [95] A. Hartstein and A.B. Fowler, *Phys. Rev. Letters* 34 (1975) 1435.
- [96] A. Hartstein and A.B. Fowler, *Surface Sci.* 73 (1978) 19.
- [97] J. Verwey, in ref. [10], p. 62.
- [98] M.R. Boudry and J.P. Stagg, *J. Appl. Phys.* 50 (1979) 942.
- [99] A. Goetzberger, V. heine and E.H. Nicollian, *Appl. Phys. Letters* 12 (1968) 95.
- [100] N.O. Lipari, *J. Vacuum Sci. Technol.* 15 (1978) 1412.
- [101] R. Williams and M.H. Woods, *Appl. Phys. Letters* 22 (1973) 458.
- [102] W.R. Bottoms, and D. Guterman, *J. Vacuum Sci. Technol.* 11 (1974) 965.
- [103] K. Ziegler, *Appl. Phys. Letters* 32 (1978) 249.
- [104] C. Werner, H. Bernt and A. Eder, in ref. [10], p. 124.
- [105] J.R. Brews, *J. Appl. Phys.* 43 (1972) 2036.
- [106] K. Ziegler and E. Klausmann, *Appl. Phys. Letters* 28 (1976) 678.
- [107] G. Declerck, R. van Overstraten and G. Broux, *J. Appl. Phys.* 45 (1974) 2593.
- [108] T. Ando, A.B. Fowler and F. Stern, *Rev. Mod. Phys.* 54 (1982) 437.
- [109] H.C. Card, in ref. [10], p. 140.
- [110] P.V. Dressendorfer, S.K. Lai, R.C. Barker and T.P. Ma, *Appl. Phys. Letters* 36 (1980) 850.
- [111] S.K. Lai, in: *Semiconductor Silicon 1981*, *Electrochem. Soc. Proc. Vol. 81-5*, Eds. H.R. Huff, R.J. Kriegler and Y. Takeishi (*Electrochem. Soc.*, Princeton, NJ, 1981) p. 416.
- [112] E. Arnold and H. Schauer, *Appl. Phys. Letters* 32 (1978) 333;

- H. Schauer and E. Arnold, IEEE Trans. Electron Devices ED-25 (1978) 1037.
- [113] C.R. Helms, Y.E. Strausser and W.E. Spicer, Appl. Phys. Letters 33 (1978) 767.
- [114] H. Frenzel and P. Balk, in ref. [11], p. 246.
- [115] D.E. Aspnes and J.B. Theeten, J. Electrochem. Soc. 127 (1980) 1359.
- [116] F.J. Grünthaler, P.J. Grünthaler, R.P. Vasquez, B.F. Lewis, J. Maserjian and A. Madhukar, J. Vacuum Sci. Technol. 16 (1979) 1443;
F.J. Grünthaler, P.J. Grünthaler, R.P. Vasquez, B.F. Lewis, J. Maserjian and A. Madhukar, in ref. [11], p. 290.
- [117] R. Williams and A.M. Goodman, Appl. Phys. Letters 25 (1974) 53.
- [118] S. Pantelides and M. Long, in ref. [9], p. 339.
- [119] O.L. Krivanek and J.H. Mazur, Appl. Phys. Letters 37 (1980) 392;
O.L. Krivanek, T.T. Sheng and D.C. Tsui, Appl. Phys. Letters 32 (1978) 392.
- [120] J.B. Blanc, C.J. Buiocchi, M.S. Abraham and W.E. Ham, Appl. Phys. Letters 30 (1977) 120.
- [121] S.K. Lai, Appl. Phys. Letters 39 (1981) 58;
S.K. Lai and D.R. Young, J. Appl. Phys. 52 (1981) 6231.
- [122] K.H. Zeininger and A.G. Holmes-Siedle, RCA Rev. 28 (1967) 208.
- [123] C.T. Sah, IEEE Trans. Nucl. Sci. NS-23 (1976) 1563.
- [124] T.P. Ma and R.C. Barker, J. Appl. Phys. 45 (1974) 317.
- [125] J.M. Aitken, D.R. Young and K. Pan, J. Appl. Phys. 49 (1978) 3386.
- [126] J.M. Aitken, IEEE Trans. Electron Devices ED-26 (1979) 372.
- [127] D.J. Dimaria, Z.A. Weinberg and J.M. Aitken, J. Appl. Phys. 45 (1974) 4506.
- [128] O.L. Curtis, Jr., J.R. Srouer and K.Y. Chiu, J. Appl. Phys. 45 (1974) 4506.
- [129] P.S. Winokur and M.M. Sokoloski, Appl. Phys. Letters 28 (1976) 627.
- [130] P.S. Winokur, J.M. McGarrity and H.E. Boesch, Jr., IEEE Trans. Nucl. Sci. NS-23 (1976) 1580.
- [131] F.B. McLean, IEEE Trans. Nucl. Sci. NS-27 (1980).
- [132] H. Lefevre, Appl. Phys. 22 (1980) 15; Appl. Phys. A29 (1982) 105.
- [133] E. Klausmann, in ref. [12], p. 169.
- [134] L.E. Katz and L.C. Kimerling, J. Electrochem. Soc. 125 (1978) 1680.
- [135] P. Balk, in: Proc. 8th Intern. Vacuum Congr., Cannes, 1980.
- [136] N. Lieske and R. Hezel, in ref. [10], p. 206.
- [137] T. Kunjunny and D.K. Ferry, Phys. Rev. B24 (1981) 4593.
- [138] R.B. Lauglin, J.D. Joannopoulos and D.J. Chadi, in ref. [9], p. 321;
R.B. Lauglin, J.D. Joannopoulos and D.J. Chadi, Phys. Rev. B21 (1980) 5733.
- [139] F. Herman, I.P. Batra and R.V. Kasowski, in ref. [9], p. 333.
- [140] F. Herman, in ref. [12], p. 1.
- [141] T. Iizuka and T. Sugano, Japan. J. Appl. Phys. 12 (1973) 73.
- [142] F. Yndurain and J. Rubio, Phys. Rev. Letters 26 (1971) 138.
- [143] A.G. Revesz, K.H. Zeininger and R.J. Evans, J. Phys. Chem. Solids 28 (1967) 197.
- [144] G.F. Neumark, Phys. Rev. B1 (1970) 2613; Phys. Rev. Letters 21 (1968) 1252.
- [145] G.V. Litovchenko, Soviet Phys.-Semiophys. 6 (1972) 696.
- [146] M. Preier, Appl. Phys. Letters 10 (1967) 362.
- [147] D.J. DiMaria, in ref. [9], p. 160.
- [148] H. Flietner, Surface Sci. 46 (1974) 251.
- [149] A.G. Revesz and G.V. Gibbs, in ref. [9], p. 92.
- [150] C. Svensson, in ref. [9], p. 328.
- [151] K. Saminadyev and J.C. Pfister, Solid State Electron. 20 (1977) 891.
- [152] T.C. Poon and H.C. Card, Electron. Letters 15 (1979) 756.
- [153] Y. Takase and A. Odajima, Japan. J. Appl. Phys. 19 (1980) 919.
- [154] T.W. Hickmott, J. Appl. Phys. 48 (1977) 723.
- [155] P.A. Muls, G.J. Declerck and R.J. van Overstraaten, Solid State Electron. 20 (1977) 911.
- [156] P.M. Lenahan, K.L. Brower, P.V. Dressendorfer and W.C. Johnson, IEEE Trans. Nucl. Sci. NS-28 (1981) 4105.

- [157] N. Bluzer, D. Affinito and F.C. Blaha, IEEE Trans. Nucl. Sci. NS-28 (1981) 4074.
- [158] A.R. Stivers and C.T. Sah, J. Appl. Phys. 51 (1980) 6292.
- [159] P.D. Esqueda and M.B. Das, Solid State Electron. 23 (1980) 365.
- [160] Y. Takuda, M. Hayashi and A. Usami, J. Phys. D14 (1981) 895.
- [161] G. Lukowsky, J. Phys. Soc. Japan 49 Suppl. A (1980) 1129;
G. Lukowsky and J. Chadi, in ref. [11], p. 301.
- [162] K.L. Ngai and C.T. White, J. Appl. Phys. 52 (1981) 320.