

IPR2024-01038 and -01194

*Canadian Solar Inc. v. Maxeon Solar Pte Ltd.*

Petitioner Canadian Solar's Demonstrative Exhibit

Hearing Date: October 15, 2025

# Grounds

## IPR2024-01038

| Claim(s) Challenged | 35 U.S.C. §      | Reference(s)/Basis                         |
|---------------------|------------------|--------------------------------------------|
| 10–12, 15           | 103 <sup>1</sup> | Li, King, Swanson-352, Marvin              |
| 10, 13–15           | 103              | Li, Muller                                 |
| 10–12, 15           | 103              | Li, King, Swanson-352, Marvin, Hu, Ramappa |

## IPR2024-01194

| Claim(s) Challenged | 35 U.S.C. §      | Reference(s)/Basis                         |
|---------------------|------------------|--------------------------------------------|
| 16, 19              | 103 <sup>1</sup> | Li, King, Swanson-352, Marvin              |
| 16, 19              | 103              | Li, Muller                                 |
| 16, 19              | 103              | Li, King, Swanson-352, Marvin, Hu, Ramappa |
| 16, 19              | 103              | Li, Muller, Hu, Ramappa                    |

# '315 Patent: Claims 10 and 16

10. A solar cell, the solar cell having a front side which faces the sun during normal operation and a back side opposite the front side, the solar cell comprising:

a silicon substrate, wherein a portion of the silicon substrate has a dopant concentration of *approximately less than or equal to  $2 \times 10^{18} \text{ cm}^{-3}$*  and wherein the portion of the silicon substrate is formed at the front side of the solar cell;

a dielectric region formed over the silicon substrate, wherein the dielectric region is formed over the back side of solar;

a *first emitter region having metal impurities* formed over the dielectric region; and

a first metal contact formed over the first emitter region.

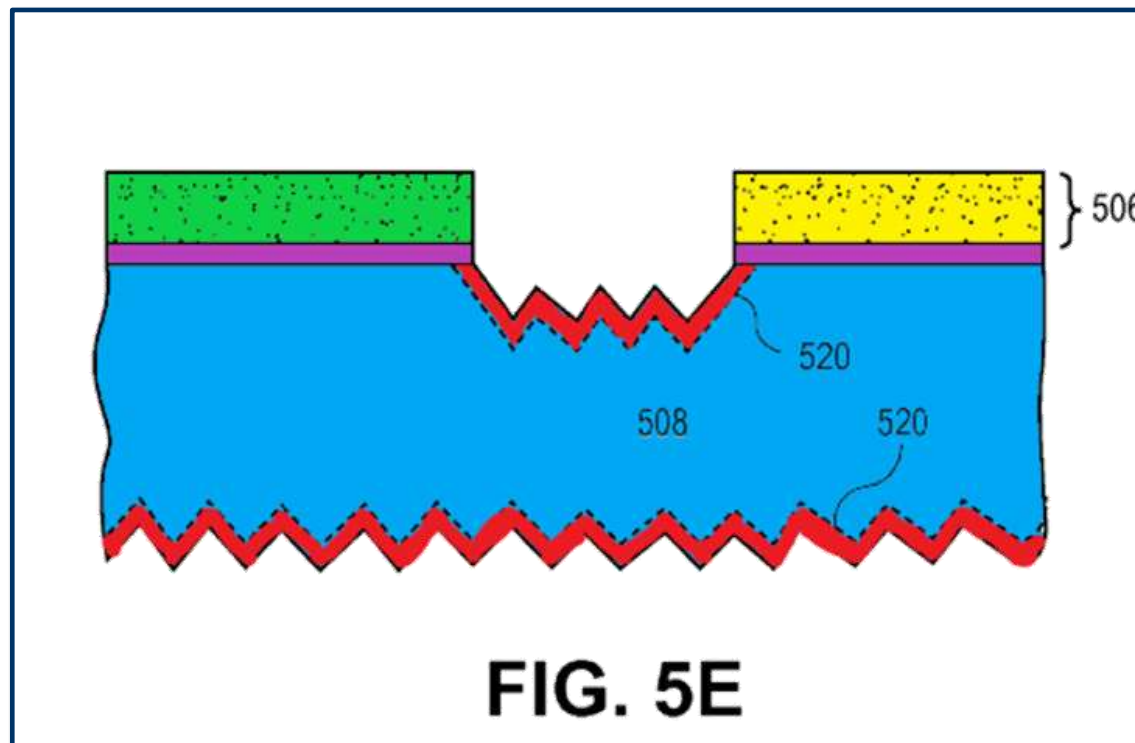
16. The solar cell of claim 10 , further comprising :

a *second emitter region having metal impurities* formed over the dielectric region ;  
and

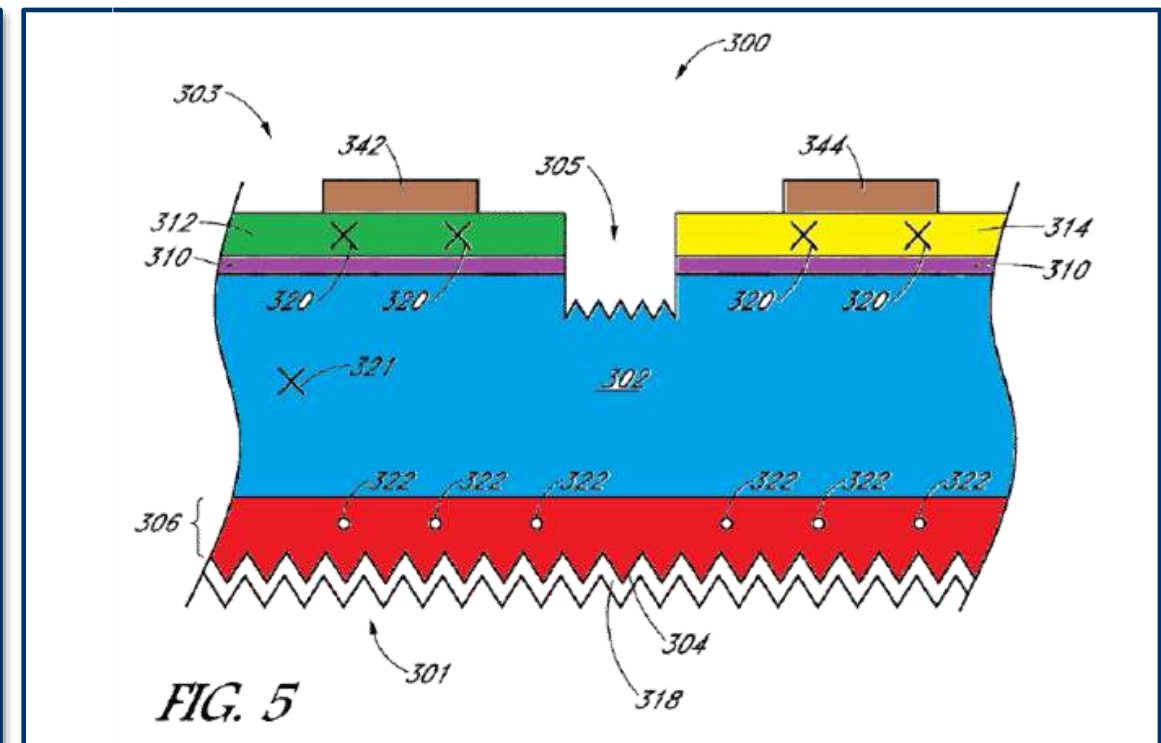
a second metal contact formed over the second emitter region.

# Both 315 and Li Disclose Back-Contact Solar Cells

Li, EX1005



315 Patent



Green/yellow = First/second polysilicon emitter regions

Purple = Dielectric region (tunnel oxide)

Blue = Silicon substrate

Bottom red = Front dopant portion

# Issues

- Grounds 1 and 2: Inherency of Metal Impurities in Li's Emitter Regions
  - Metal impurities in Li's substrate
  - Effect of Thin Oxide Layer and Temperature on Inherent Gettering
- Grounds 3 and 4: If not inherent, obviousness of gettering metal impurities into emitter regions
- Grounds 1 and 3: Motivation to combine Li and King/Swanson/Marvin
- Grounds 2 and 4: Motivation to combine Li and Muller

# Institution Decision Correctly Found Inherency

*Pharms., Inc.*, 773 F.3d 1186, 1195–96 (Fed. Cir. 2014). Petitioner, therefore, must show that metal impurities are necessarily present in Li’s N-type region 308 and P-type region 310 formed over dielectric film 320 (the claimed “first emitter region . . . formed over the dielectric region.”). On this record, we are persuaded that Petitioner sufficiently establishes that the natural result of the structures and processes described in Li is the gettering of metal impurities from substrate 304 to N-type region 308 and P-type region 310 in material layer 302, such that N-type region 308 and P-type region 310 contain metal impurities.

In particular, Dr. Banerjee testifies, with objective evidentiary support, that “multicrystalline silicon substrates were known to contain substantial concentrations of metal impurities.” Ex. 1003 ¶ 88 (citing Ex. 1010, 283; Ex. 1021, 402; Ex. 1020 ¶ 6). Hu teaches that when a

*IPR2024-01038, Paper 13 at 16*

# Li Discloses Substrates with High Metal Impurities

[0037] In accordance with an embodiment of the present invention, material layer 302 of back-contact solar cell 300 is a poly-crystalline silicon layer, substrate 304 is a single-crystalline silicon substrate, P-type region 310 includes boron dopant impurity atoms, and N-type region includes phosphorous dopant impurity atoms. In an alternative embodiment, instead of forming a poly-crystalline material layer 302, a non-poly-crystalline absorbing material is formed instead such as, but not limited to, an amorphous layer, a polymer layer, or a multi-crystalline layer. In another alternative embodiment, instead of using a single-crystalline substrate 304, a multi-crystalline substrate is used in its place.

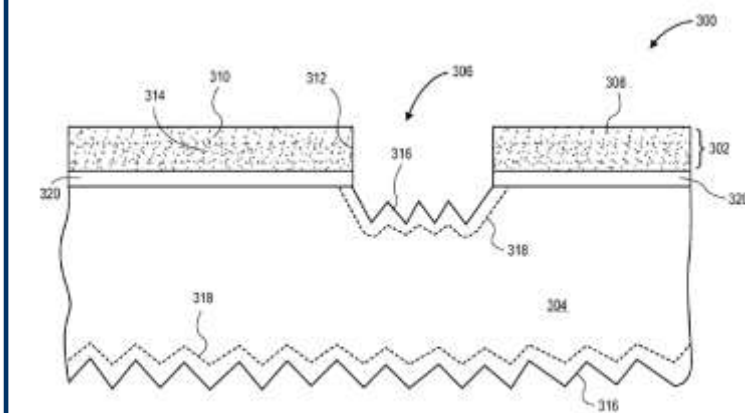


FIG. 3

*Ex. 1005 (Li) at ¶37; Pet. at 45-46; Reply at 1*

# Multi-Crystalline Silicon Has High Metal Impurities

## 1 Introduction

Low-cost crystalline silicon materials are increasingly used for main-stream photovoltaic applications. Such materials contain various extended defects, e.g. grain boundaries, second phase precipitates and in particular grown-in dislocations. The latter are known to strongly affect the minority carrier lifetime and hence the solar cell efficiency, especially when decorated with metal impurities either in form of various point defect species or as metal silicide precipitates. Hence, the incorporation of gettering steps into the processing scheme is a prerequisite for the production of efficient solar cells. Metal impurities may be incorporated into solar cell silicon materials during crystal growth and also during device processing. Recent investigations of the metal impurity content of silicon solar cell materials have shown surprisingly high concentrations, e.g.  $10^{14}$ – $10^{16}$  cm<sup>-3</sup> iron in different multicrystalline materials [1].

*Ex. 1016 (Seibt) at 696; Pet. at 18; Reply at 2*

## 7.6 MULTICRYSTALLINE CELLS

It has already been pointed out that the peculiarities of mc cells may prevent, in some cases, the use of standard processing technologies. Some of the proposed alternatives are not yet so cost-effective as to be incorporated in an industrial production line, but others are finding their way. Two main differences with single-crystalline silicon can be highlighted:

- Mc-material quality is poorer because of crystalline defects (such as grain boundaries, dislocations, etc) and metallic impurities (dissolved or precipitated), giving lower bulk lifetimes and hence lower cell efficiencies. To address this problem, two main strategies are followed: implementation of gettering steps and defect passivation with hydrogen.

*Ex. 1020 (Luque) at 283; Pet. at 18*

## 1. Introduction

Recent neutron activation analysis (NAA) studies revealed metal concentrations in ingot-cast multicrystalline silicon (mc-Si) materials as high as  $10^{13}$ – $10^{16}$  cm<sup>-3</sup> (i.e., in the ppb to ppm range) [1–3]. Subsequent studies [4,5] indicated that the majority of metals are present either in (a) metal silicide nanoprecipitates typically <100 nm in diameter, composed of medium- or fast-diffusing metal species, and present in high spatial densities (especially

*Ex. 1021 (Buonassisi) at 402; Pet. at 18*

Multicrystalline silicon wafers are commonly used in the solar industry for the production of wafer-based solar cells. Metal impurities such as iron are present in the wafers due to the manufacturing process of the multicrystalline silicon (mc-Si) ingots and reduce the carrier bulk lifetime. These

*Ex. 1018 (Ferre 2011) at 22102; Pet. at 18*

# Maxeon's Expert: Even the "Good Stuff" Had High Metal Impurities in 2014-2015

Q. Do you have a recollection of what the highest level of concentration on an atomic basis was that you observed in that 2010-to-2015 time frame?

A. I do not remember exactly. I know that it was over 10 to the 15, but that -- beyond that, I don't remember exactly what the number was in front of the 10 to the 15.

For the average silicon semiconductor that you were using, is that -- is that 10 to the 15th like approximately what you would expect?

A. Yes, because we bought silicon that could be used for either the electronic applications or for applications in solar or whatever else, so we bought pretty good stuff. The reason for that, of course, is as experimentalists, we want to control what we have.

*Ex. 1087 (Carroll Depo.) at 152:3-153:16; Reply at 3*

# Dr. Banerjee: “Practically Impossible” To Make Silicon with No Impurities

Q But if someone with enough money, and maybe more money than sense, wants to implement a super high efficient solar cell whatever the cost, they could implement something with silicon without impurities.

Is that right?

A No. So if you say silicon with no impurities, that would be impossible, if not practically impossible.

*Ex. 2022 (Banerjee) at 76:14-22; Reply at 4*

# Maxeon's Expert: "Extraordinarily Expensive To Do"

Q. What would it take to prepare a completely pure silicon substrate as of 2014?

A. Well, that would take me into the realms of speculation because, again, it's impossible to know exactly. But we do know what the sources of most of these impurities are. And so what we would have done -- if you ask me to do that in a laboratory, what I would have done would be to construct growth apparatus that did not contain very specific elements. Iron is a problem, so I would've made sure that both the feed stock for the silicon and the growth chambers and the growth hearth did not have iron in them, and so on.

So you would have done it that way, which would have made it extraordinarily expensive to do. But that's only speculation on my part right now, uh-huh.

*Ex. 1087 (Carroll Depo.) at 150:2-16; Reply at 4-5*

# Solar Cell Fabrication Routinely Used Gettering to Remove Metal Impurities From Substrates

Gettering occurs during dopant diffusion that forms the emitter

Multicrystalline silicon wafers are commonly used in the solar industry for the production of wafer-based solar cells. Metal impurities such as iron are present in the wafers due to the manufacturing process of the multicrystalline silicon (mc-Si) ingots and reduce the carrier bulk lifetime. These metal impurities are gettered during the formation of the emitter, conventionally done by diffusion at 800–900 °C in POCl<sub>3</sub> atmosphere to form an n<sup>+</sup>-type emitter on a p-type substrate.<sup>11</sup> After that, a HF dip is necessary to remove the

*Ex. 1018 (Ferre 2011) at 22102; Pet. at 17-18; Reply at 20-21*

point defect species or as metal silicide precipitates. Hence, the incorporation of gettering steps into the processing scheme is a prerequisite for the production of efficient solar cells. Metal impurities may be

the technique of choice [3, 4]. Solar cells, however, are whole-wafer devices implying that *external gettering* techniques have to be used. In fact, phosphorus diffusion gettering (PDG) and aluminum gettering (AlG) are the gettering techniques predominantly applied in silicon photovoltaics. Both steps are not primarily included for the sake of gettering but to produce functional parts of the device, i.e. the highly phosphorus doped emitter and the backsurface field, respectively, both for p-type silicon solar cells.

*Ex. 1016 (Seibt) at 696-697; Pet. at 17-18; Reply at 20-21*

# Gettering Into A Backside Polysilicon Layer Was Known Decades Before 2014

|                                  |  |      |                      |
|----------------------------------|--|------|----------------------|
| <b>United States Patent</b> [19] |  | [11] | <b>4,053,335</b>     |
| <b>Hu</b>                        |  | [45] | <b>Oct. 11, 1977</b> |

|                              |                                                                                                 |                 |           |                |         |
|------------------------------|-------------------------------------------------------------------------------------------------|-----------------|-----------|----------------|---------|
| [54]                         | <b>METHOD OF GETTERING USING BACKSIDE POLYCRYSTALLINE SILICON</b>                               | 3,997,368       | 12/1976   | Petroff et al. | 148/1.5 |
| [75]                         | Inventor: <b>Shih-Ming Hu</b> , Hopewell Junction, N.Y.                                         |                 |           |                |         |
| [73]                         | Assignee: <b>International Business Machines Corporation</b> , Armonk, N.Y.                     |                 |           |                |         |
| [21]                         | Appl. No.: <b>672,906</b>                                                                       |                 |           |                |         |
| [22]                         | Filed: <b>Apr. 2, 1976</b>                                                                      |                 |           |                |         |
| [51]                         | Int. Cl. <sup>2</sup> ..... <b>H01L 21/324; H01L 29/04</b>                                      |                 |           |                |         |
| [52]                         | U.S. Cl. .... <b>148/174; 148/1.5; 148/175; 156/612; 357/52; 357/59; 357/64; 427/82; 427/86</b> |                 |           |                |         |
| [58]                         | Field of Search ..... <b>148/1.5, 174, 175; 156/612; 357/52, 59, 64; 427/82, 86</b>             |                 |           |                |         |
| [56]                         | References Cited                                                                                |                 |           |                |         |
| <b>U.S. PATENT DOCUMENTS</b> |                                                                                                 |                 |           |                |         |
| 2,841,510                    | 7/1958                                                                                          | Mayer           | 148/1.5   |                |         |
| 3,370,980                    | 2/1968                                                                                          | Anderson        | 148/175 X |                |         |
| 3,494,809                    | 2/1970                                                                                          | Ross            | 148/175   |                |         |
| 3,632,438                    | 1/1972                                                                                          | Carlson et al.  | 357/52 X  |                |         |
| 3,694,276                    | 9/1972                                                                                          | Wakamiya et al. | 148/174   |                |         |
| 3,723,201                    | 3/1973                                                                                          | Keil            | 148/175   |                |         |
| 3,745,423                    | 7/1973                                                                                          | Hiroyuki        | 357/59 X  |                |         |
| 3,862,852                    | 1/1975                                                                                          | Kamins          | 148/174 X |                |         |
| 3,871,007                    | 3/1975                                                                                          | Wakamiya et al. | 357/59 X  |                |         |
| 3,900,597                    | 8/1975                                                                                          | Chruma et al.   | 427/82    |                |         |
| 3,929,529                    | 12/1975                                                                                         | Poponiak        | 148/175 X |                |         |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                 |  |  |  |  |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--|--|--|--|
| <b>OTHER PUBLICATIONS</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                 |  |  |  |  |
| Gates, H.R., "Gettering Process for Wafer Defect Reduction" I.B.M. Tech. Discl. Bul., vol. 15, No. 6, Nov. 1972, p. 177.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                 |  |  |  |  |
| Primary Examiner—L. Dewayne Rutledge                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                 |  |  |  |  |
| Assistant Examiner—W. G. Saba                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                 |  |  |  |  |
| Attorney, Agent, or Firm—George O. Saile                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                 |  |  |  |  |
| [57]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | <b>ABSTRACT</b> |  |  |  |  |
| An integrated circuit structure and method for manufacturing same which provides for gettering with a backside layer of polycrystalline silicon. The gettering of unwanted impurities from the integrated circuits involves the deposition of a polycrystalline silicon film on a semiconductor wafer prior to any or some high temperature processing steps. The semiconductor body is then subjected to the normal semiconductor processing steps to form semiconductor devices on the surface opposite to the surface having the polycrystalline silicon layer. During these high temperature processing steps, unwanted impurities such as copper, iron, nickel, sodium and potassium ions move toward and into the polycrystalline silicon layer and thereby away from the semiconductor devices. This produces improved yield in the integrated circuit process. |                 |  |  |  |  |
| <b>11 Claims, 8 Drawing Figures</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                 |  |  |  |  |

During these processing steps the temperature seen by the semiconductor body 10 and polycrystalline layer 12 are for the N-type diffusion 870° C, the oxidation steps 970° C and 1000° C and the post-aluminum annealing at 400° C. During the temperature cycling, the gettable impurities such as copper, lithium, sodium, potassium, iron, cobalt, nickel, chromium, and gold will diffuse to, and become trapped in, the polycrystalline silicon film impurity sink, thus relieving the integrated circuit region of these contaminants which have an adverse effect on yield. Another yield detracting defect,

Ex. 1001 (315 Patent) at 5:10-25; Pet. at 17; Reply at 21

# The 315 Patent Uses Gettering To Move and Trap the Metal Impurities Into the Polysilicon Regions

## 900°C is a key transition temperature

The emitter regions 212, e.g., polysilicon regions, can be a good sink and/or trap for the metal impurities 220 discussed above. A gettering process can be used to trap the metal impurities 220 in the emitter regions 212, reducing recombination within the silicon substrate 202 and improving overall solar cell lifetime. Oxides and/or tunnel oxides, such as the dielectric region 210 of FIG. 2, can be barriers to gettering of the metal impurities 220 to emitter regions 212. In one example, heating at temperature at 900 degrees Celsius or below can be insufficient to diffuse metal impurities through a tunnel oxide and into a polysilicon region. Thus, in an embodiment, heating at temperatures above 900 degrees Celsius can include gettering metal impurities 220 through the dielectric region 210, e.g., tunnel oxide, to into the emitter region 212, e.g., polysilicon regions, as discussed in detail at 106 of FIG. 1 below.

*Ex. 1001 (315 Patent) at 5:10-25; Pet. at 8-9, 44; Reply at 8-9*

# Li Diffuses Dopants into Polysilicon By Heating at 950°C

[0045] In accordance with an embodiment of the present invention, heating N-type dopant source layer 502 and P-type dopant source layer 504 includes transferring N-type dopants and P-type dopants, respectively, into portions 512 and 514, respectively, of material layer 506, as depicted in FIG. 5B. In one embodiment, heating N-type dopant source layer 502 and P-type dopant source layer 504 includes heating at a temperature of approximately 950 degrees Celsius. In one embodi-

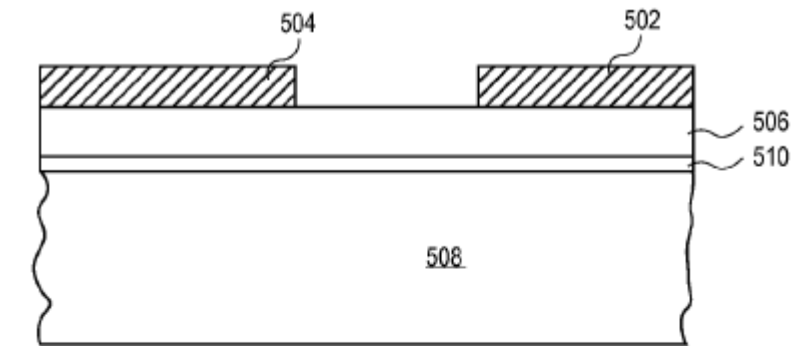


FIG. 5A

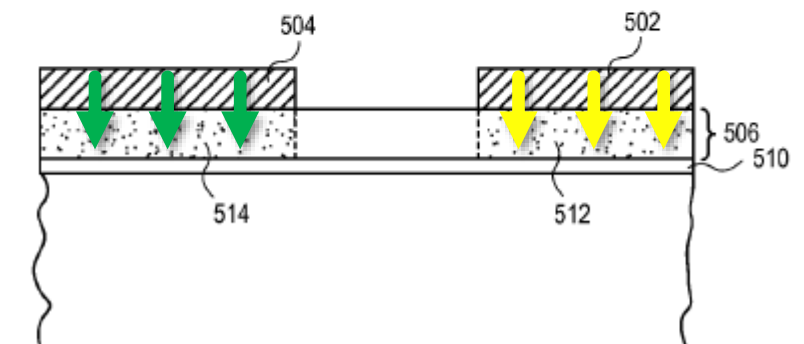


FIG. 5B

*Ex. 1005 (Li) at ¶45; Pet. at 22, 44; Reply at 8*

# Undisputed That At Least Trace Amounts of Iron Would Be Gettered Into The Polysilicon Regions of Li

Maxeon's Expert: Iron Impurities Would Getter To the Polysilicon Through 1-2 nm SiOx Under His Assumptions and Calculations

Q. And under the assumptions that you articulate in paragraph 60, you calculate that a small number of iron impurity atoms would gather through the silicon oxide and into the polysilicon, correct?

A. Yes, that's correct.

*Ex. 1087 (Carroll Depo.) at 85:12-16; Reply at 13*

# Undisputed That Metal Impurities Are *Present* In The Polysilicon Regions Of Li

Maxeon's Expert: Not Saying that Metal Impurities Would Not Getter Through  
Li's 1-2 nm Oxide into the Polysilicon

Q. And you are not providing an opinion in your  
declaration that no metal impurities whatsoever would  
getter through these 1-to-2-nanometer silicon oxide  
layer and into the polysilicon layer, correct?

A. No, I am not.

*Ex. 1087 (Carroll Depo) at 87:18-22; Reply at 13*

# Maxeon Expert's Assumptions

59. Figure 5 of Ramappa (above) shows a concentration difference across the SiO<sub>2</sub>-Si interface of many orders of magnitude. In the SiO<sub>2</sub>, iron concentration measures near 10<sup>20</sup> cm<sup>-3</sup> (in any event well above 10<sup>19</sup> cm<sup>-3</sup>). By contrast, in the silicon, the concentration varies between approximately 10<sup>11</sup> cm<sup>-3</sup> and approximate 2×10<sup>13</sup> cm<sup>-3</sup>. With particular reference to the concentrations at 900°C, the lowest measured value in the SiO<sub>2</sub> is above 3×10<sup>19</sup> cm<sup>-3</sup>, and the highest measured value in the Si was approximately 5×10<sup>11</sup> cm<sup>-3</sup>. That is a difference of a factor of over sixty million (60,000,000). Stated differently, for every 60,000,000 atoms measured on one side of the SiO<sub>2</sub>-Si interface, only one atom was measured on the other side.

*Ex. 2021 (Carroll Decl) ¶59; POR at 19; Sur-Reply at 5*

# Institution Decision: Silicon Oxide Does Not Impede Gettering at Increased Temperatures

(Example 1); § II.C.5.a, *supra*. Ramappa teaches that a silicon dioxide layer placed between the substrate and the polycrystalline layer does not impede the gettering of metal impurities at increased diffusion temperatures. *See* Ex. 1025, 3775 (Ramappa stating “for a given SiO<sub>2</sub> thickness, there exists a diffusion temperature beyond which the oxide fails to mask the silicon bulk from iron impurity incorporation”); § II.C.5.a, *supra*. On this record, and

*IPR2024-01038, Paper 13, Institution Decision at 26*

The masking effect of the silicon dioxide film against iron impurity incorporation into silicon is also evident from Fig. 3. The data indicates that if and when the SiO<sub>2</sub> layer is present the amount of iron diffused into the silicon at lower temperatures (<900°C) is relatively small. At temperatures above 900°C, there is a significant increase in the amount of iron that is transported to the Si bulk. This suggests that for a given SiO<sub>2</sub> thickness, there exists a diffusion temperature beyond which the oxide fails to mask the silicon bulk from iron impurity incorporation.

*Ex. 1025 (Ramappa) ¶3775; Reply at 17*

# Liu-2 Identifies Key Parameters For Effective Gettering

## 4. Conclusion

Moderate diffusion temperatures, which are required to achieve optimum surface passivation and low contact resistance for the polysilicon/oxide structure, have been found to also result in significant gettering of bulk metallic contaminants, for both phosphorus and boron diffused polysilicon/oxide contacts. The strong gettering effect of the polysilicon passivating contacts mainly comes from the efficient gettering capabilities of heavily phosphorus doped silicon in the case of POCl<sub>3</sub>-diffused polysilicon/oxide contacts, and from the gettering action of boron-rich layers in the case BBr<sub>3</sub>-diffused polysilicon/oxide contacts. The gettering effectiveness increases with increasing diffusion temperature for samples removed from the furnace at moderate or low temperatures. The presence of the oxide interlayer hinders the gettering effectiveness, although at optimum polysilicon fabrication conditions (very thin oxides combined with sufficiently high diffusion temperatures), the blocking effect is small, enabling the removal of more than 99.9% of the bulk iron.

1

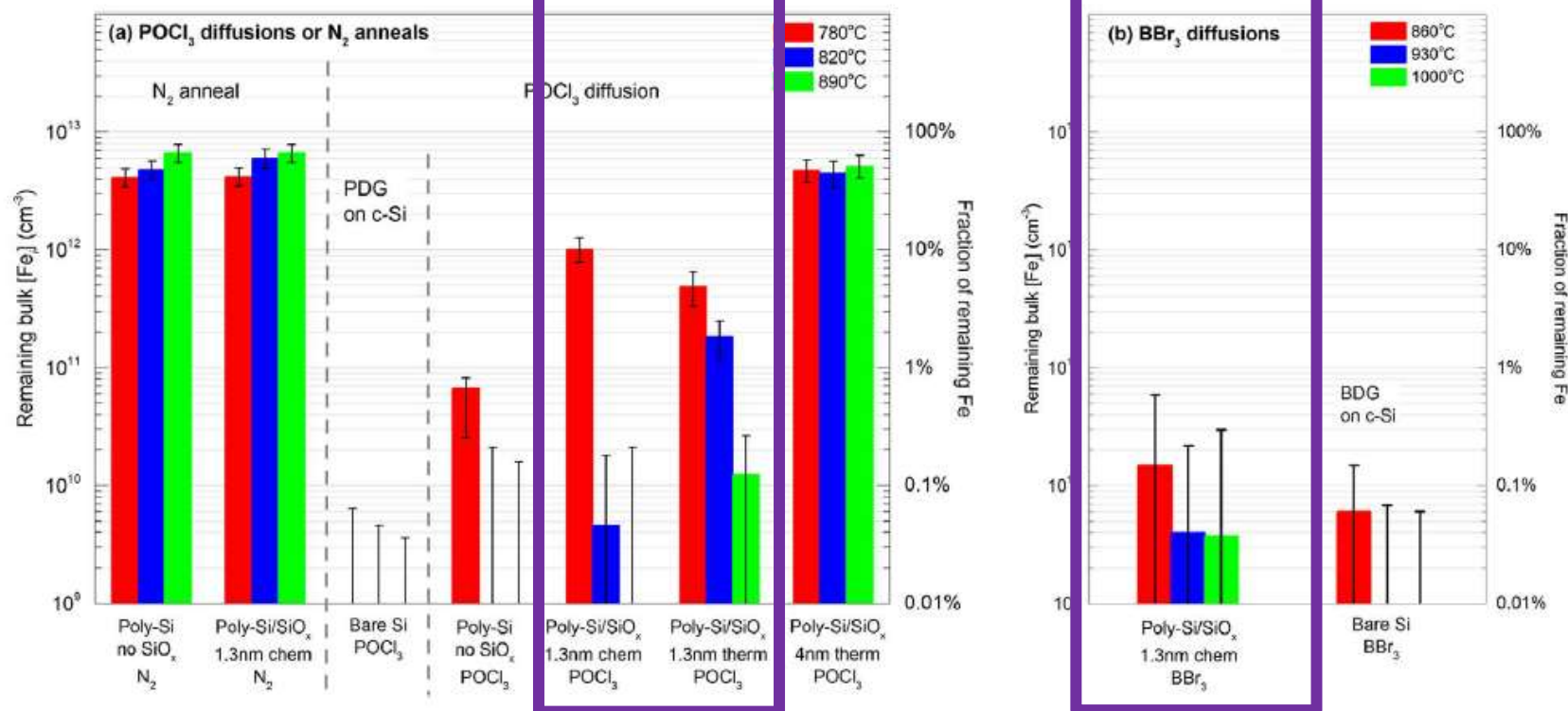
2

*Ex. 1029 (Liu-2) at 141; Pet. at 50; Institution Decision at 17*

# Liu-2 Identifies Key Parameters For Effective Gettering

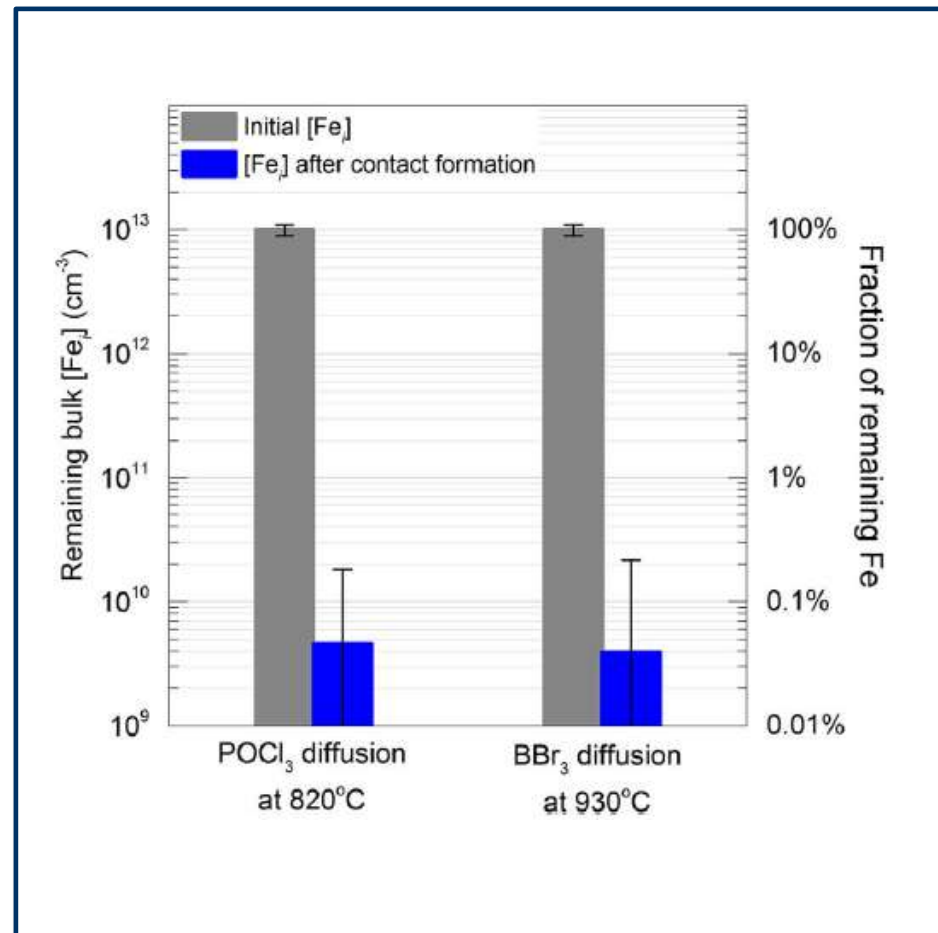
## 3.2.3. Effect of interlayer oxide on gettering effectiveness

Fig. 3(a) also illustrates the impact of the interfacial oxide on the gettering effectiveness. Samples with no oxide, chemically grown oxide of  $\sim 1.3$  nm, and thermally grown oxides of  $\sim 1.3$  nm and  $\sim 4$  nm underwent the same PECVD deposition and  $\text{POCl}_3$  diffusion processes. Comparing the remaining bulk  $[\text{Fe}_i]$  for each diffusion temperature, it can be seen that the presence of an oxide interlayer hinders the gettering action, and that the gettering effectiveness decreases with increasing oxide thickness. At lower diffusion temperatures, the samples with no oxide show the best gettering efficiency, but a similar efficiency can be achieved in the presence of a thin chemical oxide by increasing the diffusion temperature, as evidence by a residual  $[\text{Fe}_i]$  below the detection limit. The different gettering effectiveness of the chemical and



Ex. 1029 (Liu-2) 139; Pet. at 50; Institution at 17

# Gettering Increases With Increasing Temperature Above 900°C



As shown in Fig. 2, very effective gettering is achieved through the formation of diffusion-doped polysilicon/oxide passivating contacts, for both phosphorus and boron doped polysilicon. Note that the two samples in Fig. 2 underwent process conditions that result in the optimum polysilicon contact properties, in terms of the passivation and carrier transport qualities, and they were not designed to optimise the gettering effectiveness. These samples are coated with 30–40 nm polysilicon layers with ~1.3 nm chemical oxide interlayers, and were subjected to either POCl<sub>3</sub> or BBr<sub>3</sub> diffusion at moderate temperatures of 820 °C and 930 °C, respectively. As will be shown later in Section 3.2.2, the gettering effectiveness increases with increasing diffusion temperature. Nevertheless, the moderate diffusion temperatures used to achieve the best passivating contact properties (detailed in Ref [21,22] and also shown in Section 3.3) already enable very effective gettering of bulk impurities, removing more than 99.9% of bulk iron during the contact formation processes. This indicates that effective gettering can be achieved concurrently with the formation of high performance polysilicon passivating contacts.

*Ex. 1029 (Liu-2) at 138; Reply at 18-19*

# Maxeon's Expert Calculations Do Not Account For Effects of Li's Dopant Diffusion

Q. Is it your understanding that the silicon substrate that was utilized in Ramappa's experiment was an undoped substrate?

A. Let me remind myself, but I believe that's correct. So my understanding is that, yes, it was initially undoped.

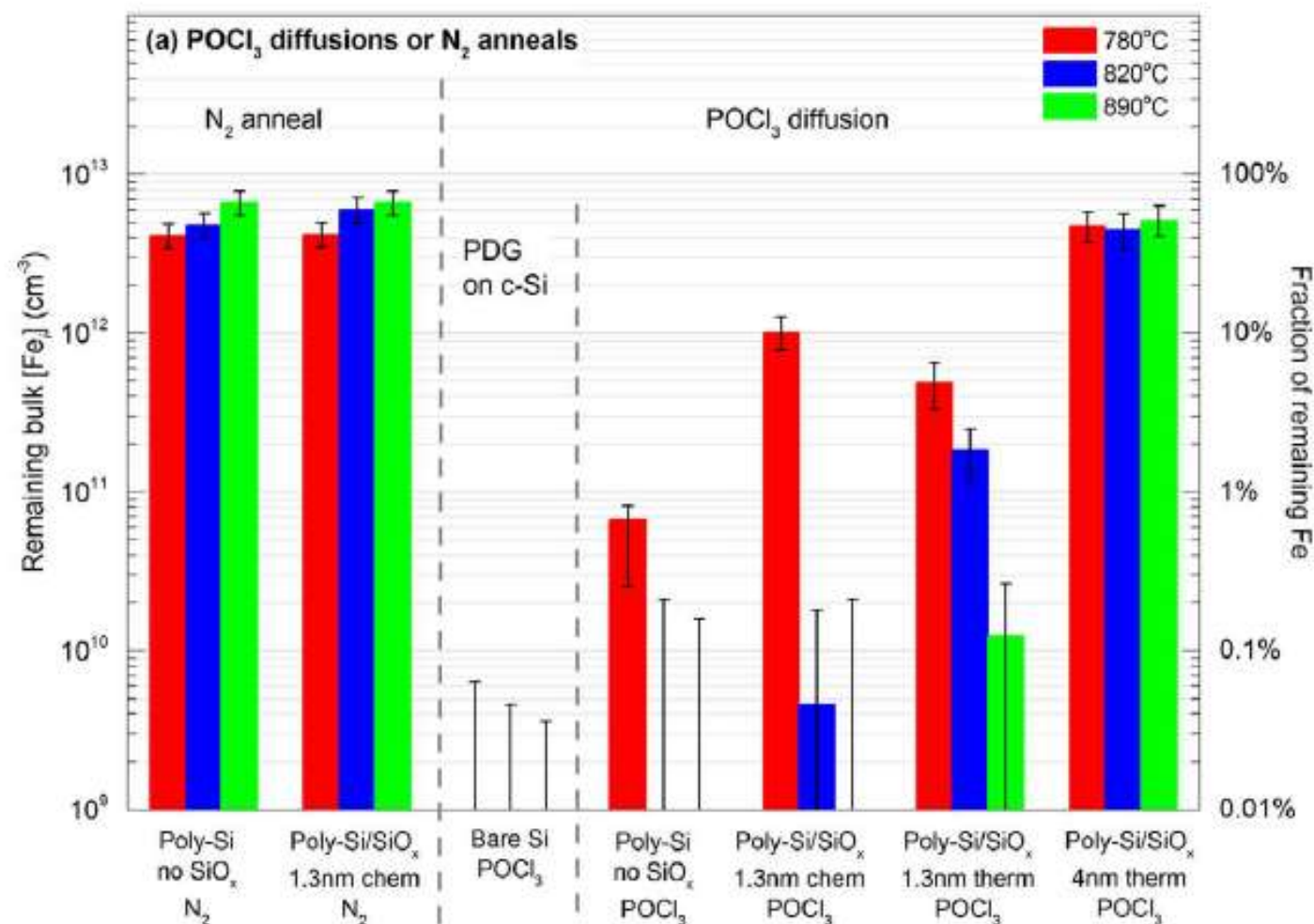
Q. Ramappa doesn't report any results reporting what the pileup effect at the oxide interface would have been if the substrate had been doped, does it?

A. This -- this reference does not, no.

*Ex. 1087 (Carroll) 84:5-14; Reply at 18*

# Undoped Polysilicon Getters Metal Impurities, But Doping (As In Li) Increases Gettering

Fig. 3(a) shows that the **intrinsic polysilicon films** used in this work do not have a significant gettering action, removing only **half of the initial bulk  $Fe_i$  concentrations**. The gettering ineffectiveness is similar for samples with and without the oxide interlayer, and is also similar for intrinsic polysilicon films annealed at different temperatures in 780–890 °C.

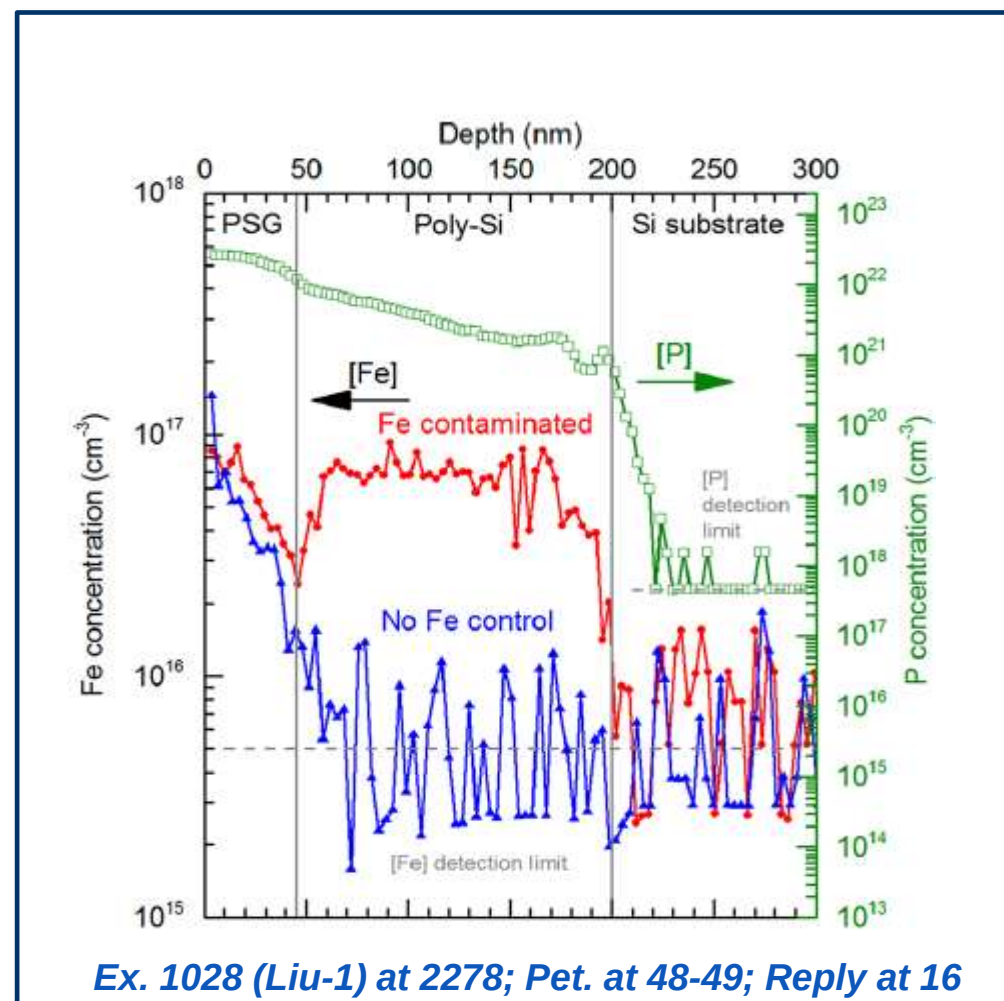


Ex. 1029 (Liu-2) at 139; Reply at 18-19

# Dr. Banerjee: Liu-1 Confirms Getting of Iron Into Phosphorus-Diffused Polysilicon

“thickness of around 1.3-1.4 nm.” EX1028, 2276-2277. For example, as shown by the red line in Figure 4 of Liu-1 reproduced below, iron atoms are gettered and present in the phosphorus-diffused polysilicon (“Poly-Si”) layer as they move from the substrate to the PSG layer. EX1028, Figure 4. PSG refers to phosphosilicate glass. The phosphorus diffusion was performed at 890°C. EX1028, 2276.

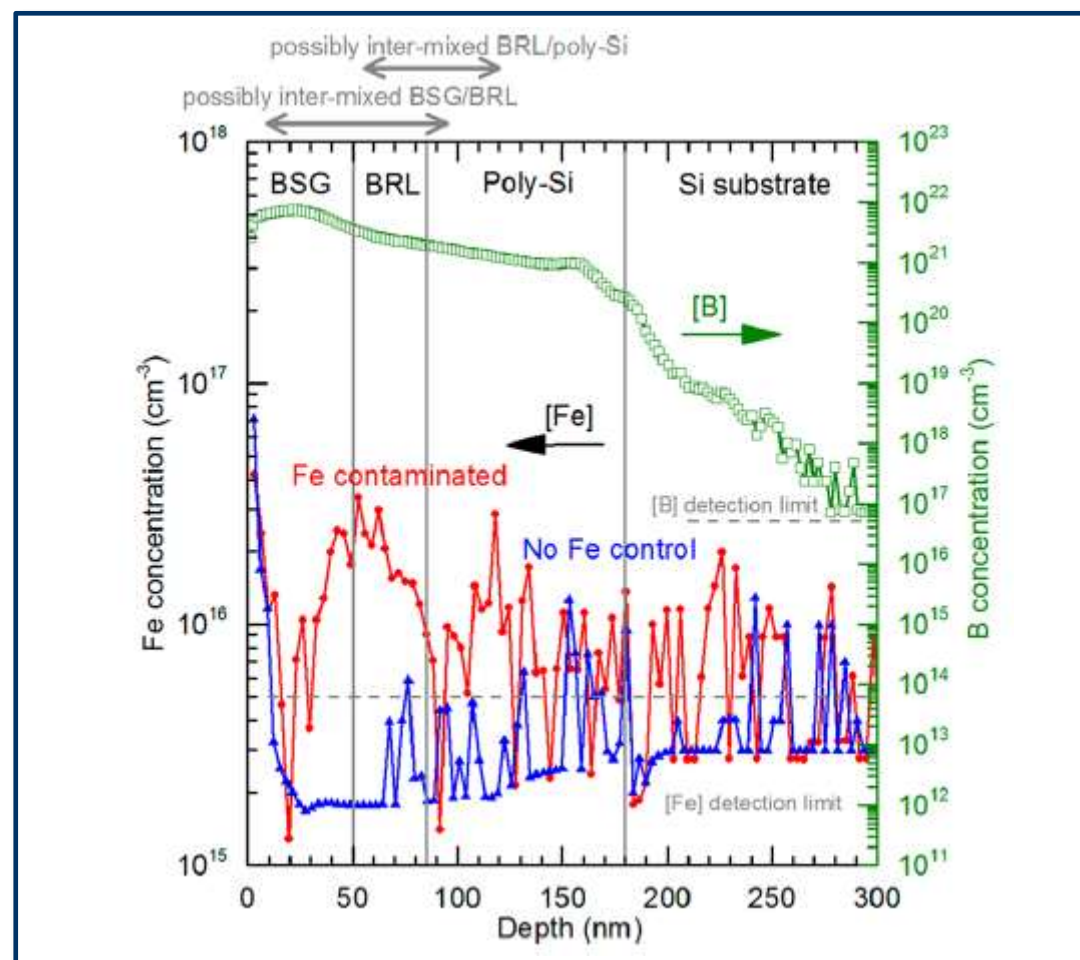
*Ex. 1003 (Banerjee) ¶164; Pet. at 48-49*



# Dr. Banerjee: Liu-1 Confirms Gettering of Iron Into Boron-Diffused Polysilicon

165. Similarly Liu-1 reported that for boron-diffusion polysilicon layers, iron impurities are gettered and present in the polysilicon layer ("Poly-Si") as they move from the substrate to the BSG layer, as seen from the red line in Figure 7 reproduced below. EX1028, Figure 7. BSG refers to borosilicate glass. The boron diffusion was performed at 900°C. EX1028, 2276.

*Ex. 1003 (Banerjee) ¶165; Pet. at 49-50*



*Ex. 1028 (Liu-1) at 2279; Pet. at 49-50; Reply at 16*

# Maxeon's Expert Agrees: Gettering Of Iron Into Boron-Diffused Polysilicon

Q. Let's take a look at Figure 7, which is on page 2279.

A. Sure. Yes.

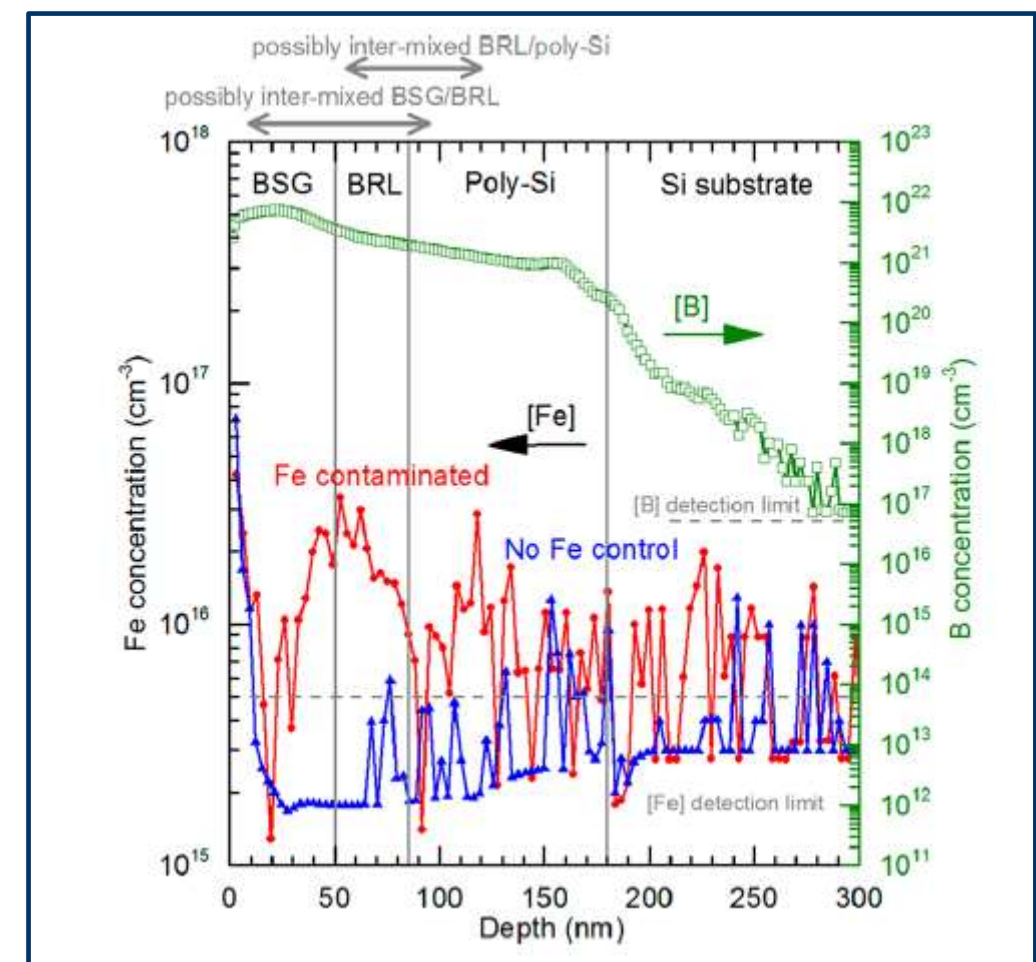
Q. Okay. And, now, this is a -- this graph is quite similar to what was reported in Figure 4, but this time what's being reported is for the boron-diffused polysilicon contact, correct?

A. That's correct.

Q. And would you agree with me that what is intended here, what the authors are intending to show, is that iron gettered from the silicon substrate through the poly- -- the silicon oxide interface and into the polysilicon?

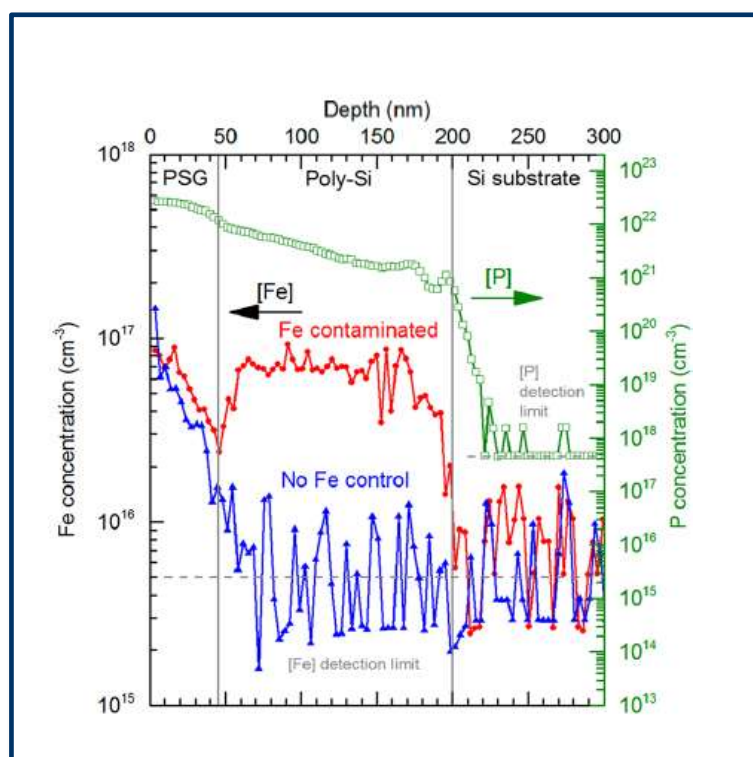
A. Yes. That is what's intended, yes.

*Ex. 1087 (Carroll) at 100:16-101:7; Reply at 16*

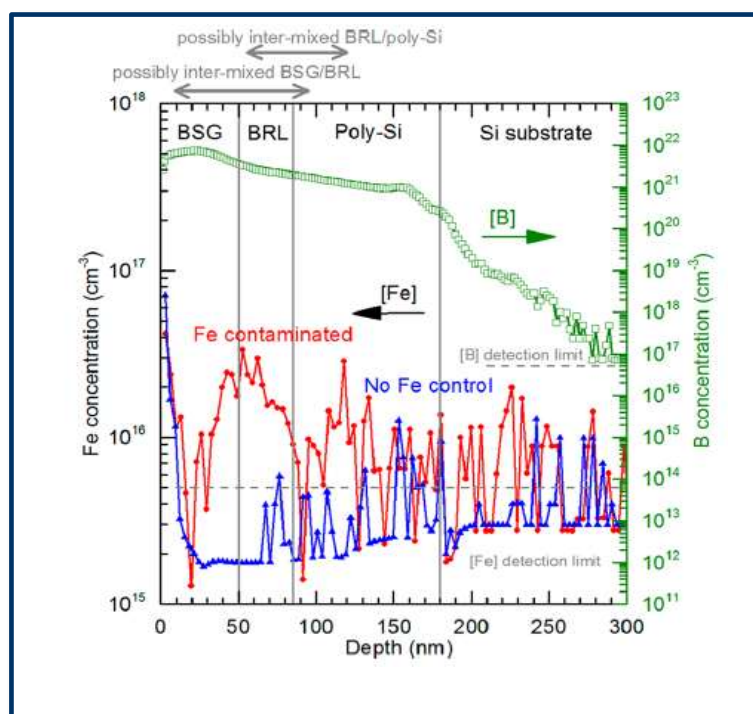


*Ex. 1028 (Liu-1) at 2279; Pet. at 49-50; Reply at 16*

# Gettering Occurs Simultaneously With Dopant Diffusion



Phosphorus-Diffusion



Boron-Diffusion

85. In solar cell manufacturing, it was also standard industry practice before 2014 to use the dopant diffusion step for simultaneously gettering metal impurities because it was also well known that gettering would occur during the high temperature formation and doping of emitter regions. Numerous publications before 2014 described the simultaneous diffusion of dopants and gettering in solar cell fabrication. For example, a 2011 publication by Ferre et al. titled

*Ex. 1003 (Banerjee) ¶85; Reply at 18*

Thin silicon oxide layers were grown on the silicon wafer surfaces via immersion in a 68 wt % nitric acid bath at 90 °C for 30 min, resulting in an oxide thickness of around 1.3–1.4 nm, from previous ellipsometry measurements.<sup>12</sup> The samples were then coated with intrinsic amorphous silicon (a-Si) films from plasma-enhanced chemical vapor deposition (PECVD), at an on-sample temperature of ~250 °C. The samples were held at ~250 °C for a total of 1 h.

*Ex. 1028 (Liu-1) at 2276; Pet. at 49-50*

depth profiles. The a-Si/oxide coated samples were then subjected to thermal diffusions in quartz tube furnaces in either POCl<sub>3</sub> or BBr<sub>3</sub> sources. POCl<sub>3</sub> diffusion was carried out at 890 °C for a total of 40 min, and BBr<sub>3</sub> diffusion was performed at 900 °C for 45 min. The samples were loaded in and out of the furnaces at 700 °C, with a ramp-up and ramp-down rate of 10 °C/min. The thermal diffusion processes also resulted in a partial recrystallization of the amorphous silicon into polycrystalline silicon, as will be revealed by TEM results.

*Ex. 1028 (Liu-1) at 2276; Pet. at 49-50*

# Maxeon's Expert's Alleged "De Minimis" Metal Impurities Can Be Detected

Q. And when you were referring to "reasonable detection means," what did you mean by that?

A. Well, there are means that you can use that we would have available to us in most laboratories like mine, which tend to be nondestructive. They are electron-dispersive spectroscopy, X-ray, photoelectron spectroscopy and so forth. There are a number of them. Those have detection limits which are significantly larger than what you would need for this. And so that's one thing.

However, there are some destructive means where you essentially take the system, evaporate the whole thing, and then look at the gas, right. In those cases you can detect slightly lower levels. And today we are at a point where we would be able to see levels this small. However, at the time of Ramappa, you would not have been able to do that. Those -- those techniques had not been refined to that point.

Q. How about in 2014?

A. In 2014 I don't think that they were commercially available, but some laboratories were doing them, including one here at Wake Forest.

*Ex. 1087 (Carroll Depo.) at 85:19-87:2; Reply at 13*

# Issues

- Grounds 1 and 2: Inherency of Metal Impurities in Li's Emitter Regions
  - Metal impurities in Li's substrate
  - Effect of Oxide Layer and Temperature
- Grounds 3 and 4: If not inherent, obviousness of gettering metal impurities into emitter regions
- Grounds 1 and 3: Motivation to combine Li and King/Swanson/Marvin
- Grounds 2 and 4: Motivation to combine Li and Muller

# Maxeon's Expert: Would Have Been Obvious in 2014 To Adjust The Heating Processes to Increase Gettering

Q. As of 2014, would a person of ordinary skill in the art have known that gettering is a general function of time and temperature?

A. As of 2014, they would have known this about gettering, yes.

Q. So if that person needed to increase the amount of gettering of metal impurities from a silicon substrate, he or she would know that she could increase the time or the temperature of the heating process, right?

A. Purely for the process of gettering, yes.

*Ex. 1087 (Carroll Depo.) at 80:7-19; Reply at 21*

# Dr. Banerjee: Integrating Gettering into Dopant Diffusion Was Well Known in Solar Cell Manufacturing Before 2014

85. In solar cell manufacturing, it was also standard industry practice before 2014 to use the dopant diffusion step for simultaneously getting metal impurities because it was also well known that getting would occur during the high temperature formation and doping of emitter regions. Numerous publications before 2014 described the simultaneous diffusion of dopants and getting in solar cell fabrication. For example, a 2011 publication by Ferre et al. titled

*Ex. 1003 (Banerjee) ¶¶ 85-86; Pet. at 72; Reply at 18*

# Dr. Banerjee: Combination of Li with Hu and Ramappa Would Yield Predictable Results

emitter region. Combining any of the above Li combinations with Hu and Ramappa as described here would have been well within the level of ordinary skill in the art as this would have required no material changes to the process of Li and therefore would have been done with a high expectation of success. It would also have been routine optimization for the Skilled Artisan to combine multiple heating steps into one single step for annealing such that the gettering and diffusion steps would all occur simultaneously, as was known in the art, and would have also conserved energy and costs. This would also have *not* resulted in any unpredictable results as seen from the teachings of Hu and Ramappa. Thus, the combination would simply have been the combination of prior art elements according to known methods to yield predictable results. Any adjustments, if needed at all, would have been routine and well within the level of skill of the Skilled Artisan.

*Ex. 1003 (Banerjee) ¶223; Pet. at 73*

# Issues

- Grounds 1 and 2: Inherency of Metal Impurities in Li's Emitter Regions
  - Metal impurities in Li's substrate
  - Effect of Oxide Layer and Temperature
- Grounds 3 and 4: If not inherent, obviousness of gettering metal impurities into emitter regions
- Grounds 1 and 3: Motivation to combine Li and King/Swanson/Marvin
- Grounds 2 and 4: Motivation to combine Li and Muller

# Maxeon Expert Was Doping Back-Contact Solar Cells At $1 \times 10^{18} \text{cm}^{-3}$ in 2014-2015

Q. Do you recall what the concentration was at the surface of the silicon substrate?

A. So at the very surface of that substrate, the concentration after treatment, after you have driven everything in, would have been at or about  $10^{18}$ .

*Ex. 1087 (Carroll Depo.) at 45:5-9; Reply at 24*

Q. And the work -- the solar cell that transitioned from front and back contact to all back contact, what time period was that?

A. That would've been toward the end of its time, so that would've been about 2014, 2015, somewhere in there. That's a rough guess.

*Ex. 1087 (Carroll Depo.) at 48:16-49:4; Reply at 24*

*See also, Ex. 1087 (Carroll Depo.) at 40:5-45:9, 47:13-49:4, 63:20-64:16, 190:18-191:7.; Reply at 24*

# Maxeon Expert: “Everyone Knows” $1 \times 10^{18} \text{cm}^{-3}$

Do you recall the concentration that was used at the front surface for the dopants?

A. So, yeah, that -- so that's a very -- that's a very detailed -- that involves a very detailed answer, because when you say "concentration," the concentration changes as you go in. The way in which it changes determines how well the cell -- how well the cell is going to function. So if I say, oh, well, let's start off at the dopant level that gives you -- that makes the silicon metallic all together, right -- so this is the generate doping -- everyone knows that that's about 10 to the 18 or so. And you don't necessarily want everything to be completely degenerate as you go into the system, right. I don't want a piece of metal in the front of -- it will block the light. So you have to have that fall off, and you have to have it fall off in a gradient in such a way that you enhance the performance and don't decrease it.

*Ex. 1087 (Carroll Depo.) at 44:3-21; Reply at 24*

# Li Does Not Preclude A Front Oxide Layer

[0021] Methods of fabricating back-contact solar cells and devices thereof are described herein. In the following description, numerous specific details are set forth, such as specific process flow operations, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known fabrication techniques, such as lithographic techniques, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

*Ex. 1005 (Li) ¶21; Reply at 25*

# A Front Side Silicon Oxide Layer Was Well Known

So, Dr. Carroll, of the front surface passivation techniques that were available in 2014, would you say that silicon oxidation passivation was the most popular?

A. In 2014, yes, I would say so.

Q. And would you say that passivating with a silicon oxide layer on the front surface was quite common for back-contact solar cells?

A. Yes, for all the manufacturers that I knew in 2014. I didn't know anyone that used anything other than silicon dioxide.

Q. Are you aware of any manufacturers as of 2014 that didn't utilize any passivation layer on the front surface?

A. I am not aware of anyone that -- that did not use anything, no.

*Ex. 1087 (Carroll Depo.) at 164:8-165:1; Reply at 25*

# Maxeon Expert: King/Swanson/Marvin Provided Better Performance Than Most Conditions

Q. And so it appears that the red -- the red-highlighted deep diffusion example is resulting in better performance than the three thin oxide examples that are not highlighted, correct?

A. Yes. In this example, that's exactly right for these particular front surface field diffusions.

*Ex. 1087 (Carroll Depo.) at 199:15-20; Reply at 27-28*

**Table II.** Summary of the results for the textured samples with different front surface field diffusions.

| $n^+$ diffusion<br>[ $\Omega/\text{sq.}$ ] | $\rho_{\text{base}} = 1 \Omega \text{ cm}$<br>low-level-injection |                                | $\rho_{\text{base}} = 10 \Omega \text{ cm}$<br>high-level-injection |                                |
|--------------------------------------------|-------------------------------------------------------------------|--------------------------------|---------------------------------------------------------------------|--------------------------------|
|                                            | $J_{0s}$<br>[fA/cm <sup>2</sup> ]                                 | $V_{OC, \text{Limit}}$<br>[mV] | $J_{0s}$<br>[fA/cm <sup>2</sup> ]                                   | $V_{OC, \text{Limit}}$<br>[mV] |
|                                            |                                                                   |                                |                                                                     |                                |
| Thin Oxides {                              | 32                                                                | 1170                           | 615                                                                 | 1180                           |
|                                            | 73                                                                | 290                            | 651                                                                 | 296                            |
|                                            | 96                                                                | 138                            | 671                                                                 | 161                            |
|                                            | 353                                                               | 31                             | 710                                                                 | 36                             |
| 148 (deep)                                 | 38                                                                | 705                            | 40                                                                  | 703                            |
| no diffusion                               | 27                                                                | 714                            | 31                                                                  | 710                            |

Thick Oxide  
(e.g., King,  
Swanson-352,  
Marvin)

Ex. 2015, Table II (annotated).

*EX. 2021 (Carroll) at 71*

# Dr. Banerjee: Granek's Thick and Thin Oxide Data Are "Pretty Close" And Not Significantly Different

But interestingly enough, in the Granek paper, at the very end of I think it's Table 2, they're comparing thick oxides, which are typical of the art that I recited, and they're optimal. Interesting enough, the values are pretty close.

If you look at the open circuit voltages, I forget the exact numbers, but I think it was 703 versus 707. I don't know if Granek did any statistically significant studies. But I can tell from my experience when you measure these parameters of solar cells, there is always some range of these values. You know, I think two or three -- I forget the exact difference, but a 3-millivolt difference for an open circuit voltage that is around 700 millivolts or so did not seem like a very significant difference.

*Ex. 2022 (Banerjee.) at 30:2-17; Reply at 27*

**Table II.** Summary of the results for the textured samples with different front surface field diffusions.

| $n^+$ diffusion<br>[ $\Omega/\text{sq.}$ ] | $\rho_{\text{base}} = 1 \Omega \text{ cm}$<br>low-level-injection |                                | $\rho_{\text{base}} = 10 \Omega \text{ cm}$<br>high-level-injection |                                |
|--------------------------------------------|-------------------------------------------------------------------|--------------------------------|---------------------------------------------------------------------|--------------------------------|
|                                            | $J_{0s}$<br>[fA/cm <sup>2</sup> ]                                 | $V_{OC, \text{Limit}}$<br>[mV] | $J_{0s}$<br>[fA/cm <sup>2</sup> ]                                   | $V_{OC, \text{Limit}}$<br>[mV] |
|                                            |                                                                   |                                |                                                                     |                                |
| Thin Oxides                                | 32                                                                | 1170                           | 615                                                                 | 615                            |
|                                            | 73                                                                | 290                            | 651                                                                 | 651                            |
|                                            | 96                                                                | 138                            | 671                                                                 | 667                            |
|                                            | 353                                                               | 31                             | 710                                                                 | 706                            |
|                                            | 148 (deep)                                                        | 38                             | 705                                                                 | 703                            |
| no diffusion                               | 27                                                                | 714                            | 31                                                                  | 710                            |

Thick Oxide  
(e.g., King,  
Swanson-352,  
Marvin)

Ex. 2015, Table II (annotated).

*EX. 2021 (Carroll) at 71*

# Maxeon Expert: POSITA Would Have Been Able to Implement Either Thick or Thin Oxide Option

Q. Okay. How about as of 2014? Would you agree that a skilled artisan would have known that you could either use a low dopant concentration and a thick oxide or a higher dopant concentration and a thin oxide?

A. I would say that they would be more likely to have known, yes. There was still a lot of debate in the literature, but, yes, they would have been more likely to have known.

Q. And would you say that a skilled artisan would have been able to implement either of those options?

A. Oh, yes, I think so.

*Ex. 1087 (Carroll Depo.) at 202:3-13; Reply at 27*

# Issues

- Grounds 1 and 2: Inherency of Metal Impurities in Li's Emitter Regions
  - Metal impurities in Li's substrate
  - Effect of Oxide Layer and Temperature
- Grounds 3 and 4: If not inherent, obviousness of gettering metal impurities into emitter regions
- Grounds 1 and 3: Motivation to combine Li and King/Swanson/Marvin
- Grounds 2 and 4: Motivation to combine Li and Muller

# Muller Discloses The Front Dopant Concentration Limitation

## 3. Results

### 3.1. Doping profiles & lifetimes

Figure 1 shows ECV profiles measured after ion implantation of boron or phosphorus and furnace annealing. With the ion implanter used in this study it is possible to run perfectly controlled and uniform processes with doses down to  $1\text{e}13$  ions/ $\text{cm}^2$  resulting in extremely weak doping profiles with peak doping concentrations in the range of  $1\text{e}17$  to  $2\text{e}18$   $\text{cm}^{-3}$ . The sheet resistance ( $R_{\text{Sheet}}$ ) of the implanted FFE and FSF samples is in the range of several hundred ( $1\text{e}14$   $\text{cm}^{-2}$  dose) to thousands ( $1\text{e}13$   $\text{cm}^{-2}$  dose) Ohm per square (see Table 1).

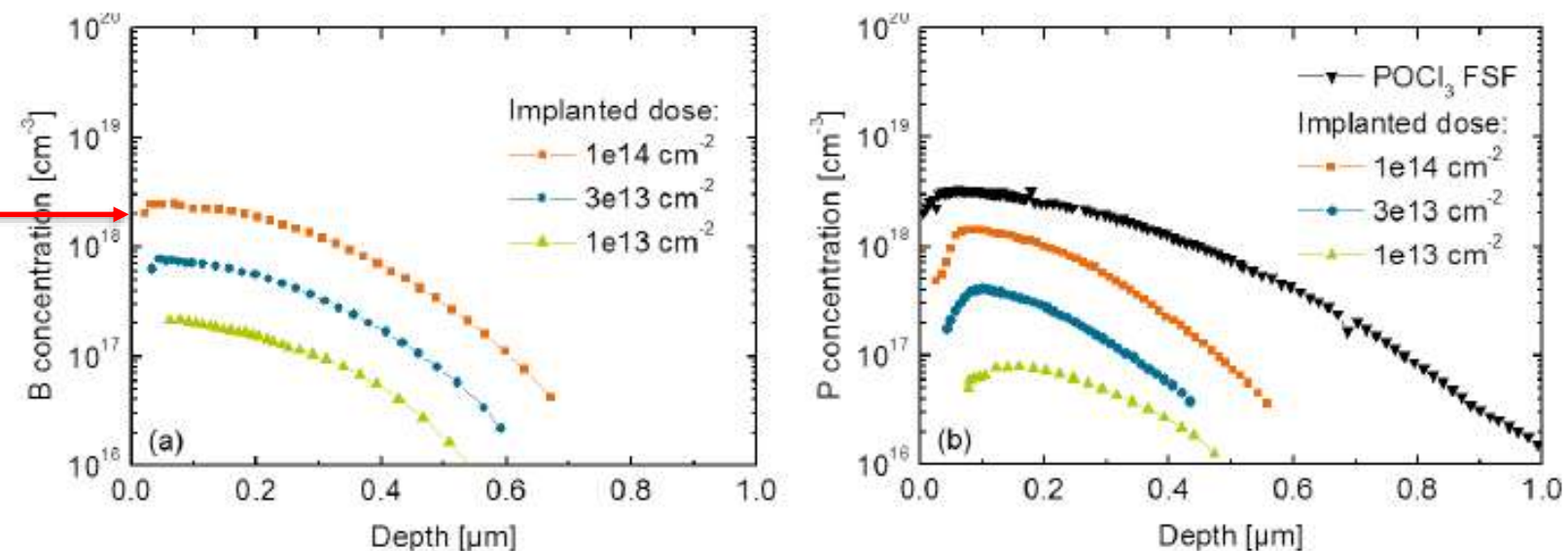


Fig. 1. ECV profiles measured on planar samples after ion implantation and annealing for 80 min at  $1050^\circ\text{C}$ . (a) Low dose boron implantations for a floating emitter; (b) low dose phosphorus implantations for a front surface field. A conventional  $\text{POCl}_3$ -diffused FSF used in Ref [8] is shown for comparison.

Ex. 1008 (Muller) at 267; Pet. at 60

# Maxeon's Expert Agrees That Muller Discloses The Claimed Front Dopant Concentration Limitation

Q. In your declaration you do not dispute that King, Swanson-352, Marvin and Muller all disclose examples in which solar cells were constructed with a front portion of the substrate that was doped to a concentration of approximately 2 times 10 to the 18th per cubic centimeter or less, right?

A. That's right. I do not dispute that they disclose that particular dopant for a very specific region of their cells.

*Ex. 1087 (Carroll Depo.) at 188:17-189:3; Reply at \_\_*

# The Board Correctly Found Motivation To Combine and Reasonable Expectation of Success

Petitioner further contends that it would have been obvious to combine Li and Muller “to replace the phosphorous diffused front portion of Li with the ion-implanted boron-doped FFE at the dopant concentration taught by Muller because” the combination “would result in increased solar cell efficiency and better stability under UV illumination,” as taught by Muller.” *Id.* (citing Ex. 1003 ¶¶ 192–203); *see also id.* at 61–64 (explaining that, in the proposed combination, Muller’s ion-implanted boron-doped FFE replaces Li’s phosphorous (N-type) doped front portion 520).

We are also persuaded, on this record, that Petitioner, with supporting testimony from Dr. Banerjee, provides adequate reasons why using the ion-implanted front floating emitter and aluminum oxide and silicon nitride passivation of Muller with Li would have been a “predictable use of prior art elements according to their established functions.” *KSR*, 550 U.S. at 401; *see Pet.* 61–64 (and evidence cited therein). We acknowledge that Patent

fact that are best resolved on a full trial record. Accordingly, we find that Petitioner shows sufficiently that a Skilled Artisan would have had reason to combine the disclosures set forth in Li and Muller with a reasonable expectation of success in arriving at the subject matter of claims 10 and 13–15. *See Pet.* 61–66.

*Institution Decision, Paper 13 at 23-24*

# Li Recognizes That Improving Solar Cell Efficiency Is Desirable

[0005] Efficiency is an important characteristic of a solar cell as it is directly related to the solar cell's capability to generate power. Accordingly, techniques for increasing the efficiency of solar cells are generally desirable. Embodiments of the present invention allow for increased solar cell efficiency by providing processes for fabricating novel solar cell structures.

*Ex. 1005 (Li) at ¶5; Reply at 4*

# Li's Objective Is *Not* Reduction in Process Steps

P-type regions of absorbing layers, the regions free from features associated with a signature from a “ledge” feature described below in association with FIGS. 2A-2E. In some embodiments, a reduction in the sheer number of process operations is achieved by using process flows described herein, as compared with conventional process flows. In some embodiments, using process flows such as those described in detail herein may be preferable over conventional flows even though some of the process flows described herein include an additional heating or anneal operation.

[0025] In an aspect of the present invention, it may be

*Ex. 1005 (Li) ¶24; Reply at 29*

# Maxeon Expert: Li Does Not Require Reduced Process Steps

Q. It's not a requirement of Li that in all cases there is a reduction in the number of process steps, right?

A. Exactly, yes. Exactly. Exactly.

*Ex. 1087 (Carroll Depo.) at 182:17-20; Reply at 29*

Q. So in some embodiments, Li may actually result in more process steps than a conventional process flow, right?

A. Yes, uh-huh.

*Ex. 1087 (Carroll Depo.) at 183:6-9; Reply at 29*

# Rhotagi: Ion-Implantation Can Improve Solar Cell Efficiency

## Abstract

This paper presents the use of ion-implantation for high-volume manufacturing of silicon solar cells. Ion-implantation provides a unique opportunity to obtain grid-parity because it simplifies the fabrication of advanced cell structures. It is shown in production that a streamlined ion-implantation process with homogeneous phosphorus doped emitter can raise the efficiency of 239 cm<sup>2</sup> p-base Cz cells by 0.8 % absolute, from 18.3 % to 19.1 %, while reducing the process sequence by one step relative to traditional POCl<sub>3</sub> process. Average production cell efficiency is about 18.6 % with

*Ex. 1036 (Rhotagi) at 10; Pet. At 62-63; Reply at 28*

# Muller's Boron FFE with AlO<sub>3</sub>/SiNx Provides Better Passivation and UV Stability

Table 1. Characteristics of the investigated profiles (best values achieved so far). Sheet resistance was measured by 4 point probe on planar reference samples.  $J_0$  was extracted from QSSPC measurements (textured samples for FSF & FFE and planar samples for emitter and BSF) using the high injection method [11].

| Sample type               | Species    | Implanted dose<br>[cm <sup>-2</sup> ] | $R_{\text{Sheet}}$<br>[Ω/sq] | $J_0$<br>[fA/cm <sup>2</sup> ] | Passivation                        |
|---------------------------|------------|---------------------------------------|------------------------------|--------------------------------|------------------------------------|
| Floating emitter (FFE)    | Boron      | 1e13                                  | 3900                         | 5                              | Al <sub>2</sub> O <sub>3</sub>     |
|                           |            | 3e13                                  | 1500                         | 6                              |                                    |
|                           |            | 1e14                                  | 650                          | 7                              |                                    |
| Front surface field (FSF) | Phosphorus | 1e13                                  | 2200                         | 12                             | SiO <sub>2</sub> /SiN <sub>x</sub> |
|                           |            | 3e13                                  | 880                          | 15                             |                                    |
|                           |            | 1e14                                  | 440                          | 10                             |                                    |
| Emitter                   | Boron      | 7e14                                  | 147                          | 9                              | Al <sub>2</sub> O <sub>3</sub>     |
|                           |            | 1e15                                  | 108                          | 22                             |                                    |
|                           |            | 1.5e15                                | 73                           | 24                             |                                    |
| Back surface field (BSF)  | Phosphorus | 3e15                                  | 39                           | 370                            | Al <sub>2</sub> O <sub>3</sub>     |

*Ex. 1008 (Muller) at 268; Pet. at 62; Reply at 28*

Table 2. Degradation of IBC solar cells under UV-illumination in a sun tester for 36 h at 500 W/m<sup>2</sup>.

| Front side                | State              | $V_{\text{oc}}$<br>[mV] | $J_{\text{sc}}$<br>[mA/cm <sup>2</sup> ] | $FF$<br>[%] | $\eta$<br>[%] |
|---------------------------|--------------------|-------------------------|------------------------------------------|-------------|---------------|
| Front surface field (FSF) | before UV exposure | 672                     | 39.2                                     | 79.6        | 20.9          |
|                           | after UV exposure  | 612                     | 19.8                                     | 79.3        | 9.6           |
| Floating emitter (FE)     | before UV exposure | 673                     | 39.9                                     | 77.3        | 20.7          |
|                           | after UV exposure  | 668                     | 38.2                                     | 76.7        | 19.6          |

*Ex. 1008 (Muller) at 270; Pet. at 62; Reply at 28*

# Maxeon's Expert: Ion-Implantation Is Only "A Little Bit More Expensive" But Has Recognized Advantages

Q. And in terms of cost, how would ion implantation compare to other methodologies for doping the front surface?

A. The other methodologies are generally cheaper.

Q. Is it a lot cheaper or -- what's the magnitude?

A. No, no, it's not a lot cheaper, but it does take a lot of power to do ion implantation, and you have to have very pure gases to do -- put into the implanters. So, generally, yeah, it's a little bit more expensive.

*Ex. 1087 (Carroll Depo.) at 207:18-208:4; Reply at 28*

Q. Are there advantages to using ion implantation over other methods of doping the front surface?

A. The advantage is generally conceded to be better positioning of the concentration as you go in normal to the surface. So you have better control over that. That's typically the advantage.

*Ex. 1087 (Carroll Depo.) at 207:6-11; Reply at 28*

# Dr. Banerjee: Combining Li and Muller Is Well Within Ordinary Skill

5E). The Skilled Artisan would recognize that Muller's teaching to dope the front surface with an ion-implanted boron floating emitter to a peak concentration of approximately  $2 \times 10^{18} \text{ cm}^{-3}$  could be readily implemented by the Skilled Artisan. Any modifications or optimization of the process steps to implement the ion-implanted boron FFE of Muller would have been within the level of skill of the Skilled Artisan before 2014. For example, it is within the level of skill of the Skilled Artisan before 2014 to insert the Muller ion-implanted boron FFE process steps before Li's process steps of forming the backside dielectric region and polysilicon emitter regions, and the doping the remaining exposed surfaces of the substrate (i.e., trench) with a gaseous N-type dopant. (EX1005, ¶0049). The Skilled Artisan would have recognized that the fabrication of the front portion of the solar cell could be done independently of the application and treatment of layers on the back surface of the solar cell, and without impacting the layers applied to the back surface of the solar cell. Muller's boron-implanted FFE and passivation layers would also be entirely consistent with the solar cell fabrication process described in Li, even for the diffusion of the back side trench region 520 using a gaseous N-type dopant source. In the combination of Li and Muller, the

*Ex. 1003 (Banerjee) ¶99; Pet. at 65-66*

## **CERTIFICATE OF SERVICE**

I hereby certify that on this 9th day of October, 2025, a copy of **Petitioner's Demonstrative** has been served in its entirety by electronic mail on the following counsel of record for patent owner:

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Dated: October 9, 2025

Respectfully submitted,

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