

Exhibit 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANADIAN SOLAR INC.,
Petitioner

v.

MAXEON SOLAR PTE, LTD.,
Patent Owner

Case IPR2024-01039
U.S. Patent No. 8,222,516

**DECLARATION OF DOUGLAS RUBY, PH.D. IN SUPPORT OF
PATENT OWNER'S RESPONSE**

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I, Douglas Ruby, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been asked by counsel for Patent Owner Maxeon Solar Pte. Ltd. (“Maxeon” or “Patent Owner”) to provide my opinions on certain matters raised in the Petition for Inter Partes Review (Paper No. 1, “Petition”) filed by Petitioner Canadian Solar Inc. (“CSI” or “Petitioner”) with respect to U.S. Patent No. 8,222,516 (Ex. 1001, “the ’516 patent”) and the declaration of Dr. Sanjay Banerjee in support of the Petition (Ex. 1003). This declaration sets forth the opinions that I have reached to date regarding these matters.

2. My independent expert consulting services are being billed at the rate of \$450/hour (plus reasonable expenses) for consulting, review, preparation, and \$475/hour (plus reasonable expenses) for depositions. My compensation is not contingent on the outcome of my review and analysis. I have no financial interest in Patent Owner.

II. QUALIFICATIONS

3. Exhibit 2021 is a true and correct copy of my *curriculum vitae* (CV).

4. As set forth in my CV, I have over 30 years of experience leading teams, managing R&D projects, and advancing solar energy technologies.

5. The following is a brief summary of my relevant qualifications and professional experience.

6. In 1978, I received my Bachelor of Science degree in Physics from the Massachusetts Institute of Technology (MIT). My Bachelor's Thesis, titled *A Study of Linewidths in Rydberg States of Atomic Sodium*, discussed light emissions from highly excited states of sodium atoms. In 1980, I received my Master's degree in Semiconductor Physics from the University of Illinois. And in 1985, I received my Ph.D. in Semiconductor Physics from the University of Illinois. My Ph.D. Thesis, titled *A Study of Electron Traps in VPE GaAs Grown With Added Oxygen*, discussed impurities and defects in semiconductors.

7. I am currently a consultant to the photovoltaics ("PV") industry, specializing in PV cell and system design and performance modeling, PV cell and module test procedures, measurement protocols and performance analysis, and PV cell module fabrication process development. My work typically includes but is not limited to (1) working with PV cell manufacturers to improve the performance and reduce the cost of their cell designs and fabrication processes, (2) providing due diligence and technical expertise on technology selection, conceptual layouts, specification development, and energy production estimates for PV power plant proposals, (3) using numerical modeling to pinpoint sources of loss mechanisms and to determine technical requirements necessary for cost-effective PV cell and module performance, (4) providing expert witness services for legal proceedings requiring photovoltaic technology expertise, (5) writing and presenting short

courses on Silicon PV Manufacturing and Technology to PV manufacturers worldwide, and (6) providing PV module, array and system performance measurements and comparison with energy-production model predictions.

8. From 1985 to 2008, I was a principal member of the technical staff at the Sandia National Laboratories in Albuquerque, NM. The work I performed there include but is not limited to (1) acting as Team Leader of PV Cell Development Team and the \$2M/year semiconductor fabrication facility, where I directed 7 team members, authored annual operating plan, directed all PV cell research projects, and was responsible for tasks and milestones of Si cell research and maintaining quality control, (2) acting as director of Crystalline Silicon Research Cooperative, a government/industry consortium for mutually beneficial research consisting of representatives from the entire US Si-PV manufacturing and research communities, (3) acting as contract monitor and advisor for several R&D contracts in the DOE Concentrator Initiative Program from 1990 to 1993, where I was closely involved and providing technical feedback for manufacturers developing Concentrator Photovoltaics systems, (4) acting as a charter member of the PV Manufacturing Technology Program Implementation Committee, a DOE/National Lab group directing \$11M/year in industry-contracted DOE research, (5) successfully led two 3-year competitively awarded projects as Principal Investigator in silicon solar cell processing, submitting original

proposals, building successful interdisciplinary teams, authoring review presentations, and meeting all milestones. (6) initiated and directed a graduate student research program at the University of New Mexico with Professor Charles Fleddermann, resulting in several graduate student thesis projects in solar cell fabrication processing to improve solar cell performance, (7) authored competitively evaluated proposal to DOE Hydrogen Program to lead a multidisciplinary team in a project to improve efficiency and cost-effectiveness of PV-powered water-electrolysis for hydrogen production, (8) served as subarea chairman of 2000 IEEE PV Specialists Conference in Silicon Cell Processing, (9) served as Session Chairman of PV session at 1999 ASME Renewable Energy Conference, (10) directed graduate student research program contract at Georgia Institute of Technology with Professor Ajeet Rohatgi, and managed a \$2.8M solar cell research and development contract, and (11) initiated and successfully conducted several direct industry joint experiments with most major US Si solar cell manufacturers, resulting in numerous publications and several process improvements adopted by industry into manufacturing production lines.

9. Beyond my academic experience, I have significant professional experience in the field of PV technology. In 1993, I designed and fabricated the world's first 20% efficient Si concentrator solar cell on low-cost Si. In 1999, I received the Best Paper Award at the ASME Renewable Energy Conference.

10. My work has been published in over 60 publications since 1981, including over 50 publications on my work with solar cell technologies. A complete list of my publications and publication metrics are listed on pages 12-18 of my CV.

11. I am an inventor on 5 issued U.S. patents related to solar cell technologies. A complete list of my patents can be found on pages 6-7 of my CV.

III. DOCUMENTS CONSIDERED

12. In formulating my opinions, I have considered the documents cited in this declaration and the following:

- Petition for *Inter Partes* Review of U.S. Patent No. 8,822,516 (Paper No. 2)
- U.S. Patent No. 8,822,516 (Ex. 1001)
- File History of U.S. Patent No. 8,822,516 (Ex. 1002)
- Declaration of Dr. Sanjay Banerjee in Support of Petition for *Inter Partes* Review of U.S. Patent No. 8,822,516 (Ex. 1003)
- File History of U.S. Patent Application No. 14/504,771 (“771 Application”) (Ex. 1005)
- EP17322142A1 to Armin Froitzheim (“Froitzheim”) (Ex. 1006)
- J.Y. Gan et al., “Polysilicon Emitters for Silicon Concentrator Solar Cells,” May 1990, Proceedings of the 21st IEEE-PVSC (“Gan”) (Ex. 1007)
- Kwark, Y.H. et al. “SIPOS Heterojunction contacts to silicon.” 1984 International Electron Devices Meeting (1984): 742-745 (“Kwark”) (Ex. 1008)
- WO2009/094578 to Borden (“Borden”) (Ex. 1009)
- U.S. Provisional Patent Application No. 61/023,342 (“Borden Provisional”), filed January 24, 2008 (Ex. Ex. 1010)
- U.S. Patent No. 6,262,359 to Meier (“Meier”) (Ex. 1011)
- JP07-106611 to Okayasu (Okayasu) (Human Translation) (Ex. 1012)
- U.S. Patent Pub. No. 2002-0142500 to Foglietti (Ex. 1014)

- U.S. Patent Pub. No. 2005-0268963 to Jordan (Jordan) (Ex 1015)
- Yablonovitch, Eli et al., A Study of n⁺-SIPOA-p-Si Heterojunction Emitters (Ex 1016)
- Sinton et al, Design Criteria for Si Point-Contact Concentrator Solar Cells (Ex 1017)
- File History of U.S. Patent Application No. 16-460,035 (035 Application) (Ex 1018)
- Luque, A, Handbook of Photovoltaic Science and Engineering (2003) pts 1 and 2 (Ex 1019)
- Lindholm, Heavily Doped Polysilicon-Contact Solar Cells. July 1985 (Ex 1020)
- Silvestre, Series Resistance in Double-Polysilicon-Contacted Silicon, 1996 (Ex 1021)
- Duerinckx, Defect passivation of industrial multicrystalline, 2002 (Ex 1022)
- Ashburn, Comparison of Experimental and Theoretical Results on Polysi, 1984 (Ex 1023)
- Declaration of Sylvia Hall-Ellis (Ex. 1024)
- Feldmann, et al., “A Passivated Rear Contact for High-Efficiency n-Type Silicon Solar Cells Enabling High VocS and FF > 82%” (28th European PV Solar Energy Conference & Exhibition, Paris, Sept. 30 – Oct. 4, 2013) (Ex. 1037).
- File History of U.S. Patent No. 8,878,053 (Ex 1038)
- Green, High Efficiency N-Silicon Solar Cells Using Rear Junction 1993 (Ex 1039 Ex 1039)
- Gan, Jon-Yiew, Polysilicon emitters for silicon concentrator solar cells, Stanford University (July 1990) (“Gan Thesis”) (Ex. 2003)
- Declaration of Mary K. Bolin, Ph.D. (Ex. 2022)
- Transcript of Deposition of Sanjay Banerjee, Ph.D., taken March 20, 2024 (Ex. 2023)

IV. ASSUMPTIONS

A. Date of Invention

13. I have been asked to assume that the date of the inventions of the claims of the '516 patent was February 20, 2008.

B. Person of Ordinary Skill in the Art

14. I have been asked to apply the skill level of a person of ordinary skill in the art (“POSITA”) that is proposed in the Petition, which is “someone with an advanced degree involving the discipline of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field.” Petition, 3.

15. At the time of the inventions of the claims of the ’516 patent, I was aware of the understandings and capabilities of a person having the skill level described above. This awareness was informed by my experience in academia where I worked with many persons that possessed such a level of skill at and around the time of the invention.

V. RELEVANT PATENT LAW STANDARDS

A. Claim Construction

16. I understand that patent claim terms are generally given their ordinary and customary meaning as understood by a POSITA in the art when read in the context of the specification and prosecution history. Two exceptions are when (1) the patentee acts as their own lexicographer, or (2) the patentee disavows the full scope of the claim term.

17. I also understand that, in construing the claims, the analysis should focus on the words of the claims. However, patent claims are not read in a vacuum

and should instead be read in view of the specification and prosecution history, i.e., the back-and-forth correspondence between the patent applicant and the U.S. Patent and Trademark Office. I further understand that the patent specification is the single best guide to the meaning of a claim term. Thus, a construction that is not supported by the specification should be rejected, even if that construction is plausible, if divorced from the specification. However, it is improper to read limitations from the specification into a claim absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited. At bottom, the interpretation to be given a claim term can be determined and confirmed only with a full understanding of what the inventors actually invented and intended to envelop with the claim.

B. Obviousness

18. I understand that a determination that a claim is “obvious” is based on underlying factual issues including the content of the prior art and the level of skill in the art. I understand that for a single prior art reference or a combination of prior art references to render a claim obvious, and thus unpatentable, a POSITA in the art must have been able to arrive at the claim by altering or combining the references. I have been informed that all elements of a claim must be considered in an obviousness analysis.

19. I further understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when combining or modifying the prior art. I understand that this test should not be applied rigidly, but that the test can be important to avoid such hindsight.

20. I have been informed that, for a claim to have been obvious, a POSITA must have had a reasonable expectation of success in combining or modifying prior art references to arrive at the claim. I understand that absolute predictability is not required. I further understand that the test is reasonable probability of success not some degree of unpredictability.

C. Standard of Proof

21. I understand that the standard to prove unpatentability is by a preponderance of the evidence, which means more likely than not.

VI. BACKGROUND OF THE '516 PATENT AND RELATED TECHNOLOGY

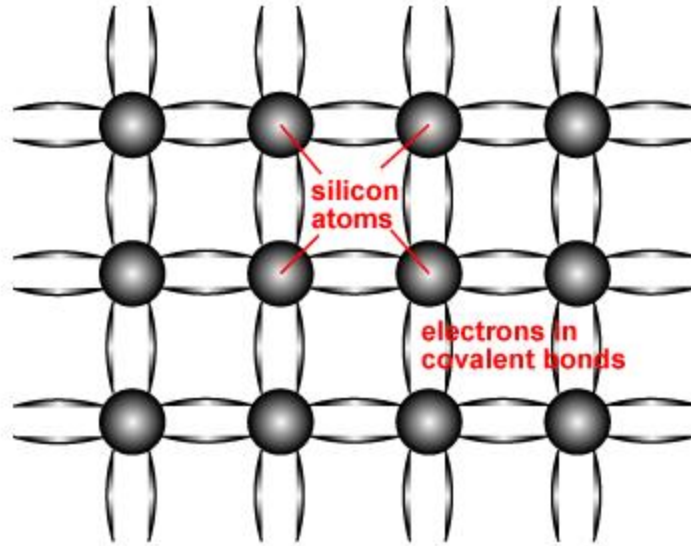
22. The '516 patent "relates generally to solar cells." Ex. 1001, 1:21. According to the '516 patent, "[s]olar cells are well known devices for converting solar radiation to electrical energy." Ex. 1001, 1:19-20. This field is also known as photovoltaics.

A. Theory of Converting Solar Energy into Electricity

23. Sunlight is composed of a flux of individual particles called photons. A photon is characterized by its wavelength, λ , or its energy, E. The total radiant power emitted from the sun is composed not of a single wavelength, but of many wavelengths and, therefore, does not appear as individual colors to the human eye.

24. According to the '516 patent, solar cells “may be fabricated on a semiconductor wafer.” Ex. 1001, 1:20-22. One type of semiconductor uses a silicon (Si) substrate which is made up of individual Si atoms bonded together in a regular, periodic structure to form an arrangement whereby each atom is surrounded by eight electrons. Each silicon atom has four valence electrons which are individually shared with those of four neighboring Si atoms, forming four covalent bonds with the four surrounding Si atoms.

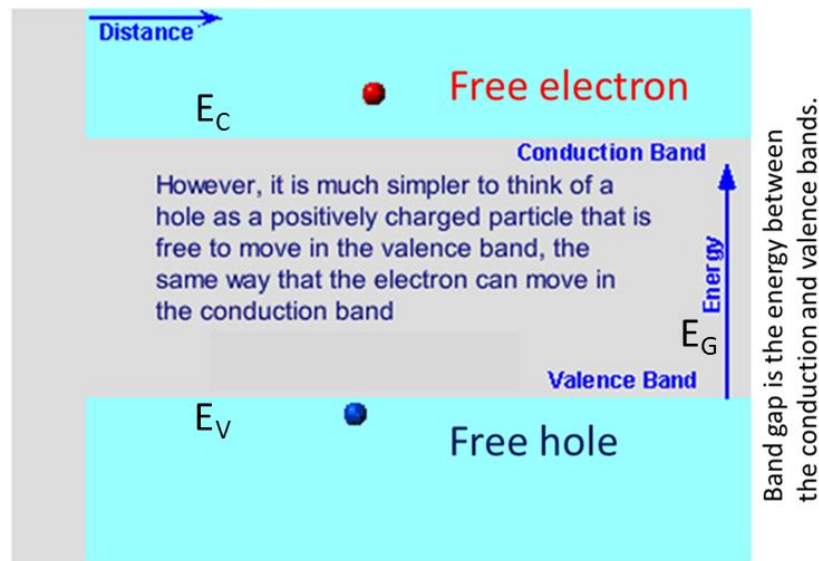
25. Below is a schematic representation of covalent bonds in a silicon crystal lattice. Each line connecting the atoms represents an electron being shared between two atoms. Two electrons being shared are what form the covalent bond.



26. The lowest energy position for an electron to be in is its bound state. If the electron has enough thermal energy to break free of its bond, then it becomes free and available for electric conduction (in the conduction band). The electron cannot attain energy values intermediate to these two levels; it is either at a low energy position in the valence band (valence electron) or it has gained enough energy to break free and contribute to conduction (jumps to conduction band). The minimum energy required is the difference between conduction and valence band energies and is called the “band gap” of a semiconductor.

27. The vacancy left behind by an electron that has been promoted to the conduction band allows the empty covalent bond to move freely from one atom to another, acting like a positive charge moving through the crystal lattice, much like a bubble moving through a liquid. This empty bond is commonly called a “hole” and acts like a positive charge with unique properties such as mass and mobility,

and also contributes to conduction. The lower energy level is E_V and the energy level at which an electron can be considered free is E_C . The band gap (E_G) is the energy difference between the conduction band and valence band.



B. Doping

28. It is possible to shift the balance of electrons and holes in a silicon crystal lattice by “doping” it with other atoms. Donor atoms with one more valence electron than silicon are used to produce “N-type” semiconductor material, which adds electrons to the conduction band and hence increases the number of free electrons (negatively charged carriers). Acceptor atoms with one fewer valence electron result in “P-type” material. In P-type material, the number of electrons missing from covalent bonds is higher, thus effectively increasing the number of free holes (positively charged carriers). In doped material, there is always more of one type of carrier than the other and the type of carrier with the

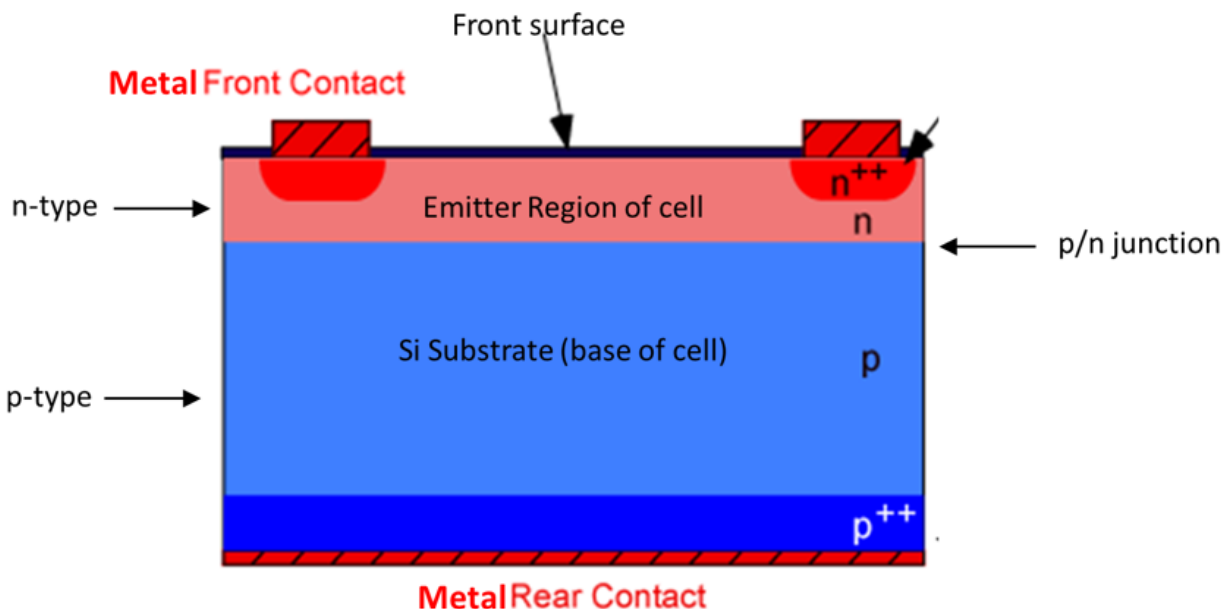
higher concentration is called a “majority carrier,” while the carrier with lower concentration is called a “minority carrier.”

C. Annealing

29. Annealing is a general term for a process during which the atoms of a material are given enough time and thermal energy to find and relax into their lowest energy state.

D. Solar Cell Structure

30. According to the '516 patent, a solar cell has a “front side” that “faces the sun during normal operation to collect solar radiation.” Ex. 1001, 1:32-34. Opposite the front side is the backside. *Id.* at 1:34. This is illustrated in the following diagram of a generic solar cell.



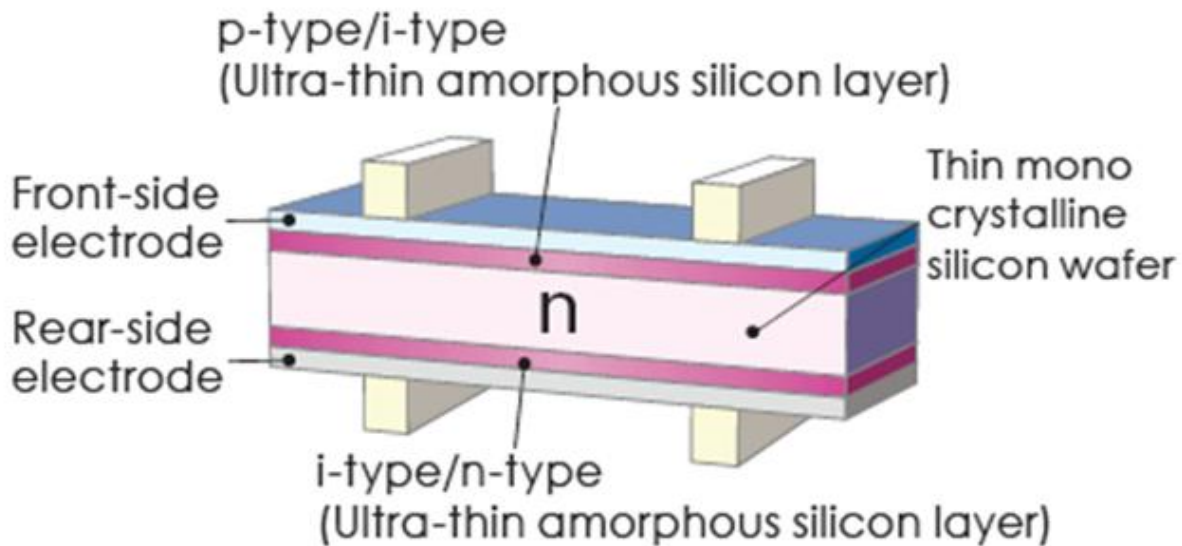
1. *Junctions*

31. A junction is a general term for a region of a semiconductor device where the properties of the material on one side are dissimilar in some way from those on the other side. These can include homojunctions where the two regions are each made of the same material but have different electrical properties, or heterojunctions where the two regions are actually made of different materials with differences in crystal structure, chemical composition, bandgap, or other molecular properties. Claim 9 in '516 patent recite forming a poly-Si layer on a Si substrate. This material discontinuity constitutes a heterojunction.

a. Heterojunction

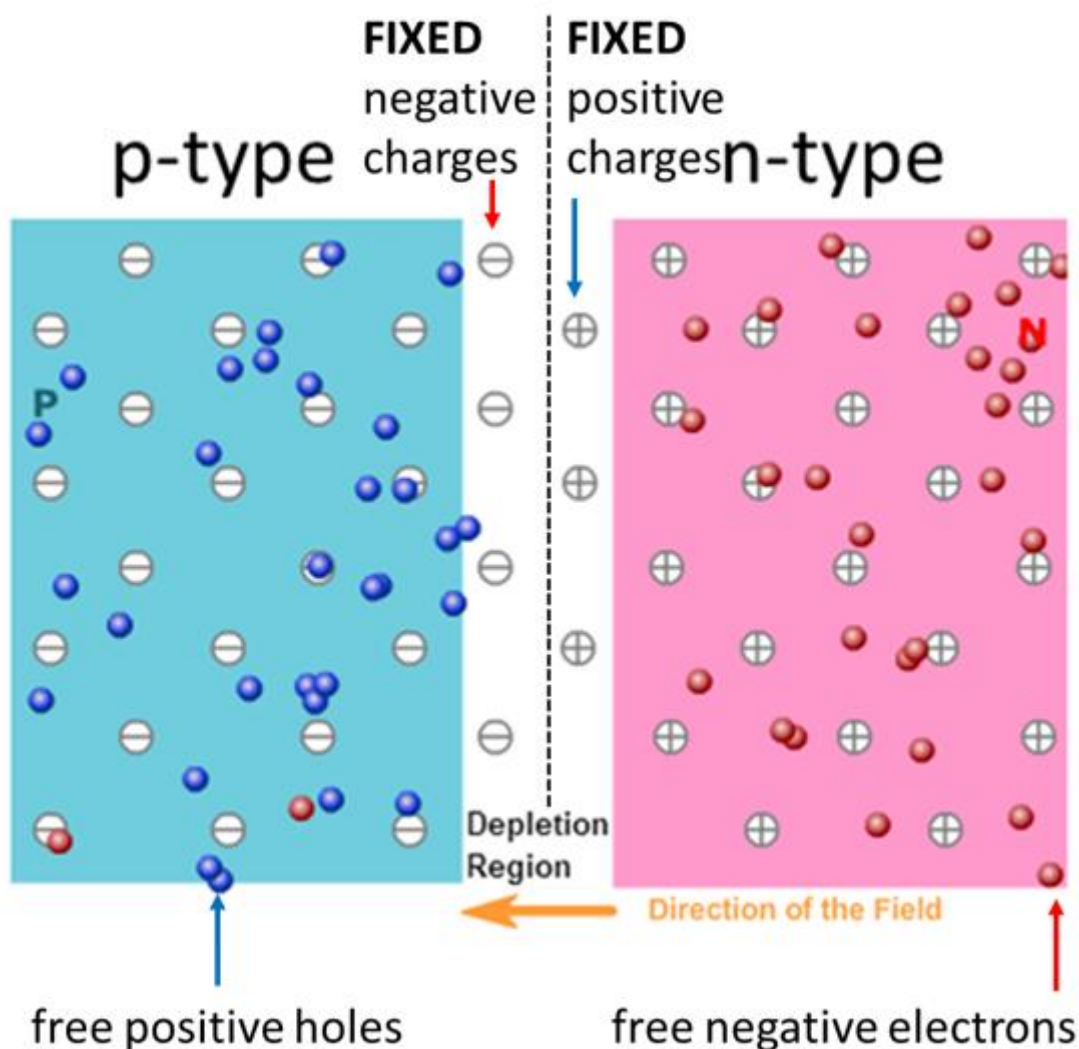
32. As noted, a heterojunction is formed by joining of dissimilar materials in contact with a semiconductor substrate. This can be a poly-Si layer, as in the '516 patent, or an amorphous Si (a-Si) layer as shown below in the famous heterojunction cell invented by Sanyo Corporation. It is the abrupt change in material properties between the c-Si and the a-Si which lead to the excellent performance of this type of solar cell, which held the world record for energy conversion efficiency for many years.

SANYO HIT® Solar Cell Structure



b. P-N Junction

33. An example of a P-N junction is that region of a solar cell where a P-type Si base adjoins directly with an N-type emitter region. This can be created by heavily doping a P-type Si substrate with N-type dopant atoms until a shallow layer of N-type Si is formed near the surface of the substrate. Since the N-type region has a high electron concentration and the P-type a high hole concentration, electrons diffuse from the N-type side to the P-type side and holes flow by diffusion from the P-type side to the N-type side. Diffusion in semiconductors is the motion of charge carriers due to their concentration gradient.



34. After the electrons and holes move to the other side of the P-N junction, they leave behind exposed charges on dopant atom sites, which are fixed in the crystal lattice and are unable to move. On the N-type side, positive ion cores are exposed with donor charge density N_D . On the P-type side, negative ion cores are exposed with acceptor charge density N_A .

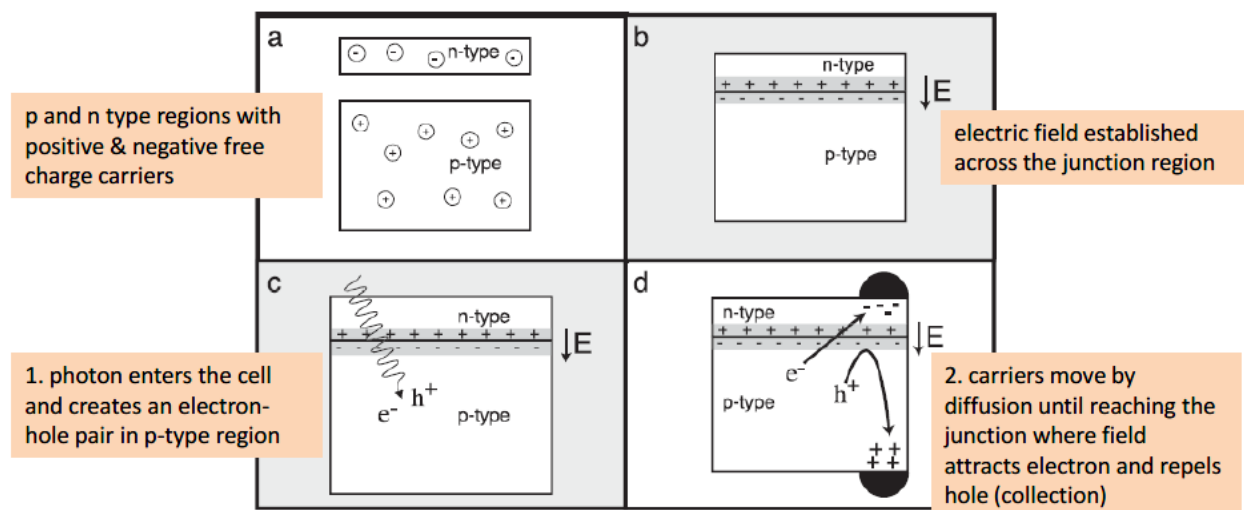
35. A built-in electric field $\hat{E}$ forms between the positive ion cores in the N-type material and negative ion cores in the P-type material. This region is called

the "depletion region" since the electric field there quickly sweeps any free carriers across, hence the region is depleted of free carriers. This region extends further into the more lightly doped side to expose an equal number of fixed ion cores as on the more heavily doped side.

36. A solar cell absorbs light to generate electric power. This is a three-step process: First, it absorbs as much sunlight as possible through the front side of the solar cell to photogenerate electrons and holes. In a doped region, the increase in photogenerated majority carriers is just a tiny fraction of the majority carriers already present, so these have little effect.

37. Second, since the photogenerated minority carriers represent a large increase in the number of minority carriers present, the process of diffusion of these minority carriers towards the depletion region at the P-N junction naturally takes place. These minority carriers diffuse a distance of what is called the minority carrier diffusion length, which is the average distance they can diffuse before recombining during the average minority carrier lifetime.

38. Third, the electric field present at the junction then sweeps the minority carriers across, at which point they are collected and simply need to pass through contacts into the external circuit.



39. As shown above, in box (a), the basic structure of a solar cell may include an N-type region with negative free charge carriers on the front side, and P-type region with positive free charge carriers on the backside.

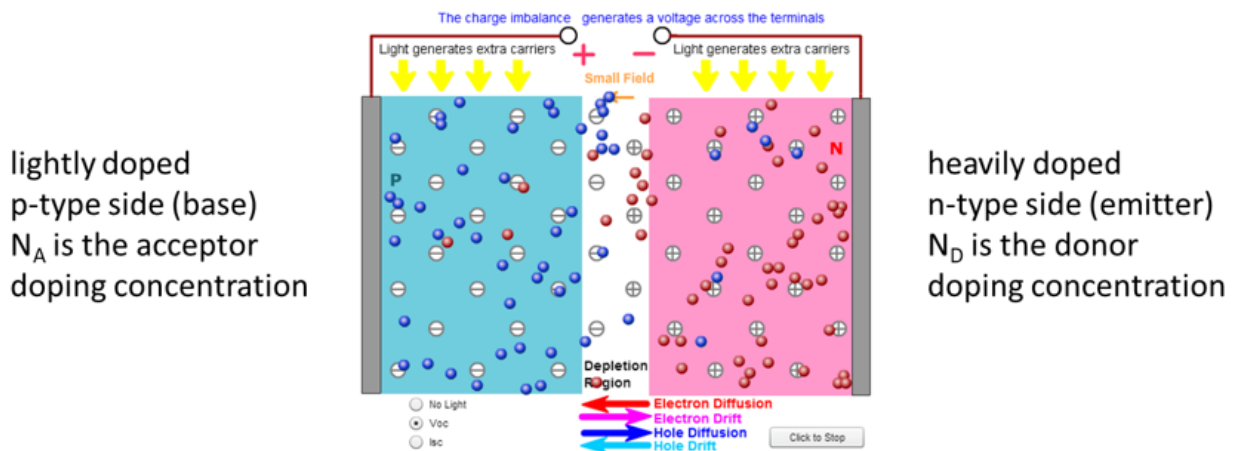
40. In box (b), a built-in electric field is shown to be established across the P-N junction region.

41. In box (c), upon absorbing sunlight, a photon enters the solar cell. If the photon has an energy greater than that of the band gap, an electron-hole pair can be photogenerated, in this instance, in the p-type region.

42. In box (d), the minority carrier electrons move by diffusion until reaching the P-N junction region where they are swept across by the built-in electric field there. Specifically in the case shown here, the electron is swept across the junction and becomes a majority carrier in the N-region where it can then no longer recombine since there are so few holes present there. The

photogenerated hole is repelled by the junction electric field and increases the majority carrier hole concentration slightly in the P-region. This buildup of charged majority carriers creates a voltage across the P-N junction. If an external circuit is present, these excess majority carriers can be pushed through low-resistance metal contacts, thereby generating a negative photocurrent in the circuit and delivering electric power.

43. To generate power, a voltage must be generated as well as a current. If light-generated carriers are prevented from leaving the solar cell (such as in the case of an open-circuit shown below), the number of electrons on the N-side and holes on the P-side increase. This creates an electric field at the P-N junction opposite to the built-in field.



44. This forward voltage across the junction creates a forward bias current, which exactly balances the negative photogenerated current, so the net current is zero at open circuit. The voltage to cause these two currents to exactly

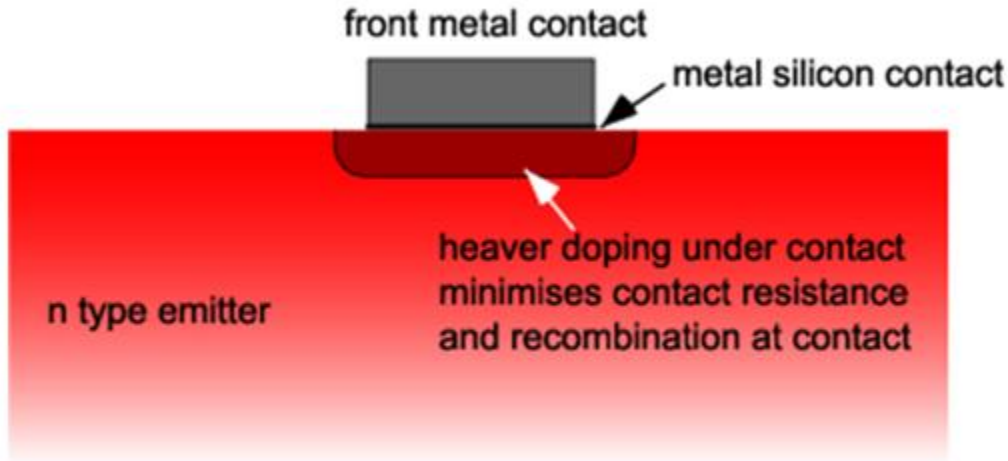
balance is called the “open-circuit voltage.” In actual operation, the voltage across the cell is maintained at a slightly lower value so that current can be delivered to an external circuit at the maximum power point. These operating parameters are known as the max power voltage and max power current.

45. The above discussion assumes a P-type substrate doped with N-type dopants to form the emitter. A P-N junction can also be formed with “a P-type polysilicon emitter formed over [an] N-type silicon substrate.” Non-asserted claim 1 of the ’516 patent is directed to such a junction structure. Ex. 1001, 6:12-14. Moreover, as recited in claim 9, providing “an emitter layer formed over a back surface of [a] substrate” also forms a junction, *i.e.*, a heterojunction. *Id.* at 6:46-48.

2. *Emitter*

46. In a semiconductor device, the emitter of the device is usually defined as the region which is doped to have the opposite majority carrier polarity compared to the substrate. However, as in claim 9 of the ’516 patent, the emitter can be a polysilicon layer on the back side of the substrate. Ex. 1001, 6:46-48.

3. *Contacts*



47. The contacts of a solar cell are metal regions deposited on the cell surface intended to conduct the photogenerated current from the semiconductor to an external circuit.

E. Types of Solar Cells: One Sun and Concentrator Solar Cells

48. Solar cells designed for use on earth rather than in outer space are called terrestrial cells as opposed to space cells. Terrestrial cells can be further divided into cells designed to use normal sunlight (one-sun cells) and those designed to use concentrated sunlight (concentrator cells).

49. The distinguishing characteristic of concentrator cells is that they generate many times more free carriers than one sun solar cells do, requiring concentrator solar cells to have a much lower series resistance from the substrate through the emitter, contacts, and gridlines than in a one sun solar cell.

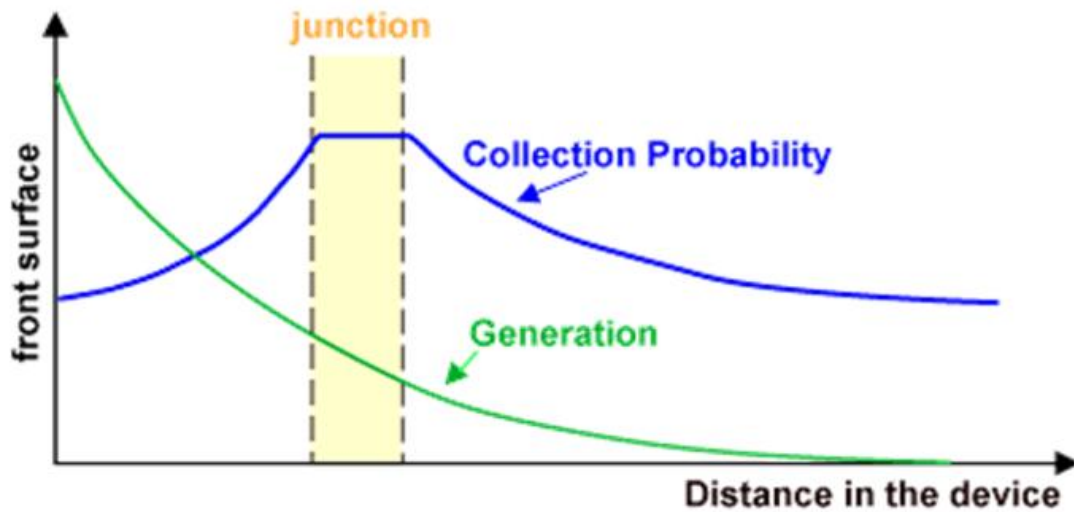
50. In particular, the contact resistances must be much lower than those of one-sun cells, and the metal gridlines are usually much thicker to reduce gridline resistance.

F. Solar Cell Efficiency

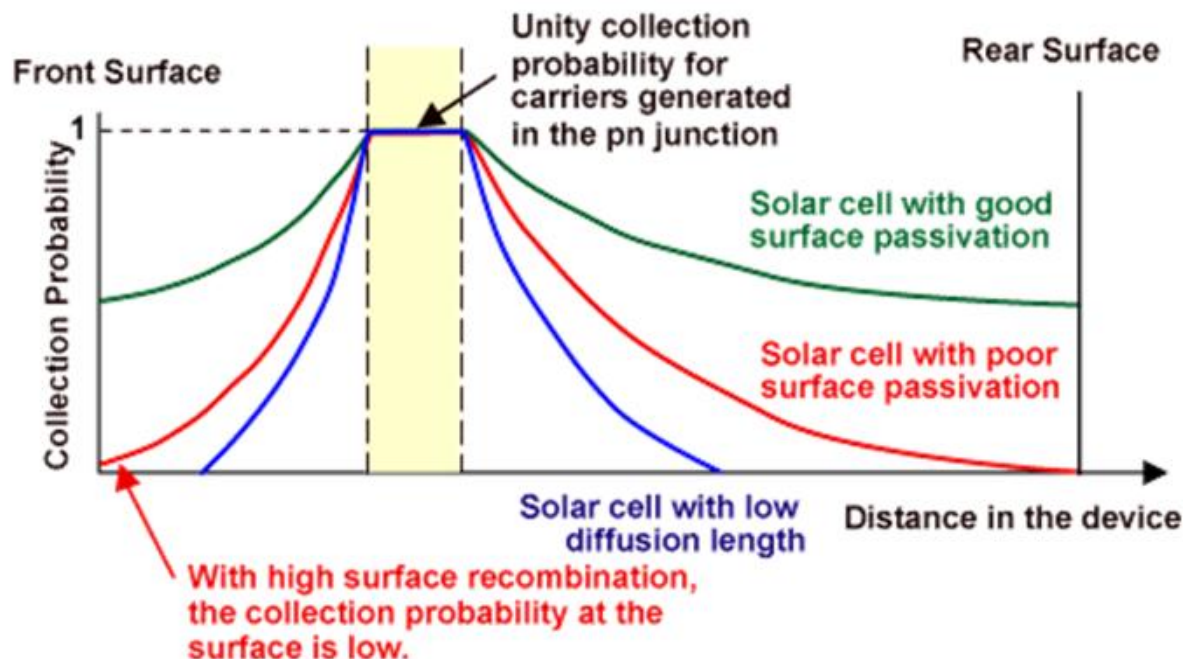
51. The overarching goal of the solar cell industry is to increase the efficiency of the solar cell, which is the ratio of electrical power output at the max power point to the photo power incident in the incoming sunlight. This is achieved by maximizing light absorption, reducing photocarrier recombination to increase current and voltage, and maintaining low electrical resistance within the cell.

1. Recombination and Passivation

52. The free electrons photogenerated by absorbed sunlight can recombine with any free holes present by falling back into the covalent bond vacancies, in which case neither free carrier can contribute to conduction any longer. Most photogeneration takes place close to the front surface of the cell where the light is mainly absorbed. The probability that photocarriers will be collected by the junction decreases with distance from the junction.

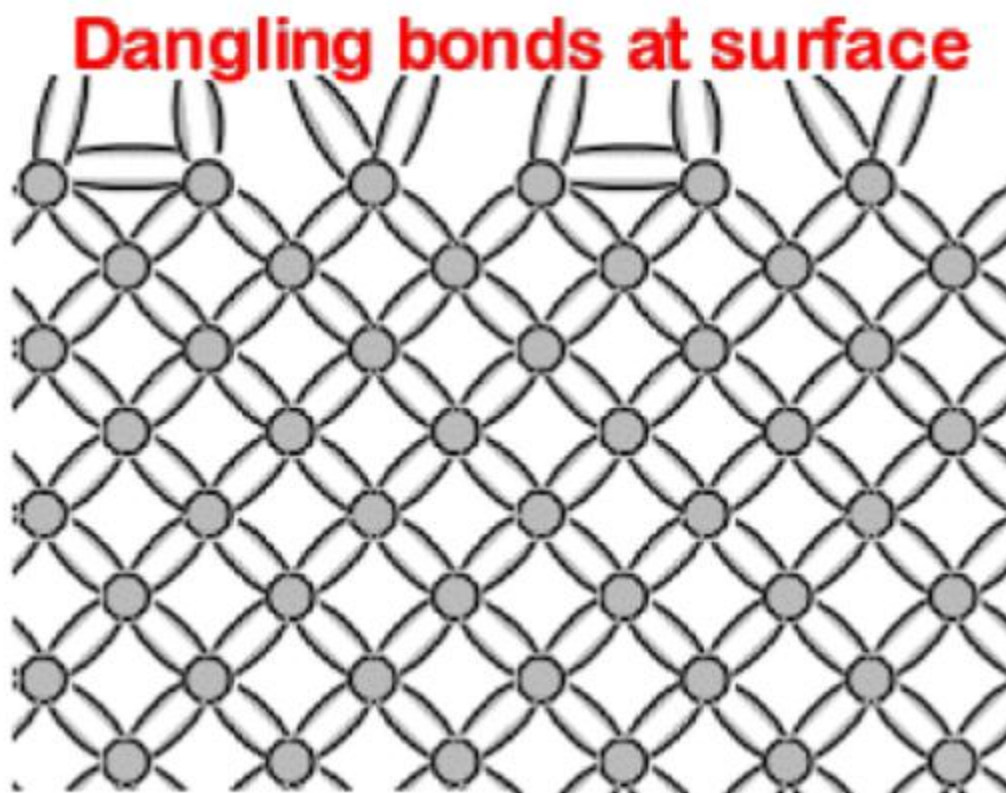


53. The mean time that free carriers exist before recombination is called the minority carrier lifetime. The distance they can diffuse during this time is called the minority carrier diffusion length. This is sometimes measured as a saturation current density called J_0 . The goal of effective solar cell design is to minimize this recombination by maximizing carrier lifetimes and diffusion lengths, thereby keeping J_0 low.



54. Defects at either surface of the semiconductor wafer or impurities within it increase the level of recombination occurring in each of these areas, thereby decreasing the concentration of photogenerated carriers available to generate current and voltage. Each of these regions can be characterized by its own J_0 value, which all add together to determine overall cell efficiency. Effective solar cell design implements the invention and inclusion of critical features to reduce the amount of recombination occurring at surfaces, which is known as surface passivation.

55. The surface of a solar cell represents a severe disruption of the periodic crystal lattice, and these surfaces of the solar cell are a site of particularly high recombination unless they are effectively passivated.



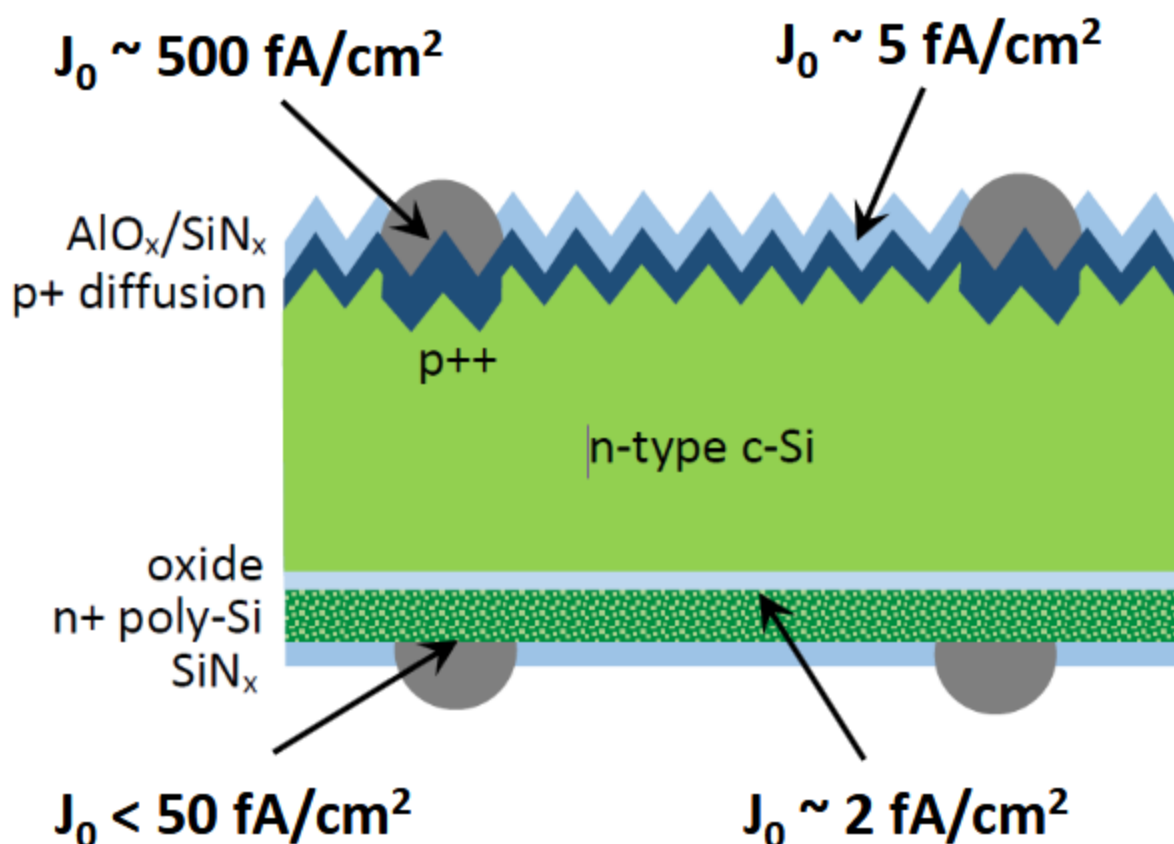
56. The defects at a semiconductor surface are caused by the interruption to the periodicity of the crystal lattice, which causes dangling bonds to form at the semiconductor surface where high levels of recombination can occur. The high recombination rate in the vicinity of a surface reduces the concentration of minority carriers in this region.

57. The reduction of the number of dangling bonds, and hence surface recombination, is often achieved by carefully growing a matching layer on top of the semiconductor surface, whose chemical structure is perfect for tying up some of these dangling bonds. This reduction of dangling bonds is known as surface passivation. Thermally grown silicon dioxide (SiO_2) is an excellent match for

passivating Si surfaces. This oxide is carefully grown at high temperatures in a clean environment containing only oxygen and possibly some inert gas. This thermal oxide needs to be differentiated from the many other types of oxides that can be found on Si surfaces, such as chemical oxides produced at room temperature.

58. The amount of recombination can be quantified by measuring J_o , which represents recombination in a region of the cell, and is related to the voltage a cell can deliver. Specifically, it is related to the mean lifetime of minority carriers before they recombine. A low J_o indicates less recombination. This means that more carriers migrate outside the cell and deliver useable power, thereby increasing cell conversion efficiency.

59. A good TOPCon one sun cell, shown in the literature in 2023, such as the one shown by MacDonald in Figure 1 below has rear surface J_o of $2 \text{ fA/cm}^2 = 2 \times 10^{-15} \text{ A/cm}^2$. This is about 5-30 times lower than that of the concentrator cell, which is the subject of Kwark's experiments (discussed below), and 10-25 times lower than the results of Gan's experiments. Gan is also directed to a concentrator cell.

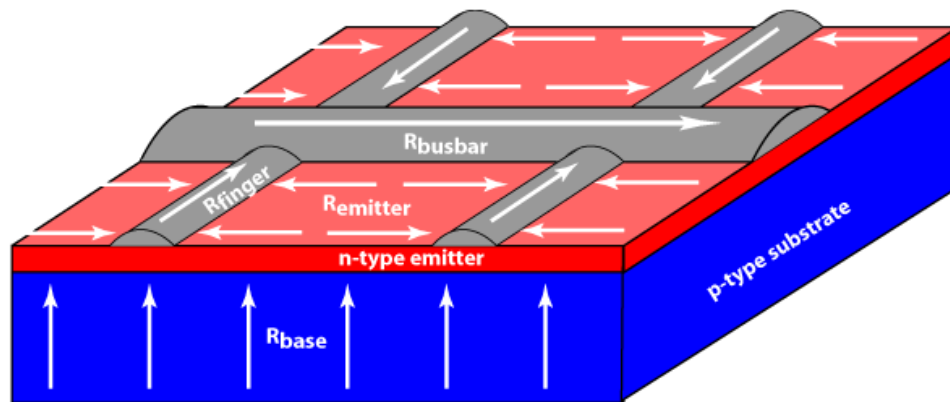


D. MacDonald, Achieving 26% silicon solar cells in mass production with passivating contacts – TOPCon or heterojunctions? Australian National University, UNSW School of Photovoltaic & Renewable Energy Engineering (Sept. 2023) (<https://www2.pv.unsw.edu.au/videos/Daniel-Macdonald-7September2023/slides/UNSW-SPREE-seminar-Sept-2023-DanM.pdf>).

2. Resistance

60. Series resistance in solar cells reduces their efficiency by dissipating power in the cell that would otherwise be delivered to an external circuit. The most common parasitic resistances are series resistance and shunt resistance.

61. Series resistance in a solar cell has three causes: (1) the movement of current through the emitter and base of the solar cell; (2) the contact resistance between the metal contacts and the substrate; and (3) the resistance of the top and rear metal contacts. The diagram below illustrates the components of series resistance:



62. The metallic top contacts are necessary to collect the current generated by a solar cell. “Busbars” are connected directly to the external metal ribbons in a solar panel, while “gridline-fingers” are fine areas of metallization which collect current for delivery to the busbars. A tradeoff is made by having sufficient metal coverage to reduce series resistance without shading too much of the cell, which reduces the capture of sunlight and, therefore, reduces current.

63. Series resistance due to contacts can be quantified as ρ_c , which represents the contact resistivity of any contact of a given area and is due to forcing the current from the Si to the metal of the contact. It is measured by sending current through the contact, and measuring the voltage across the contact for

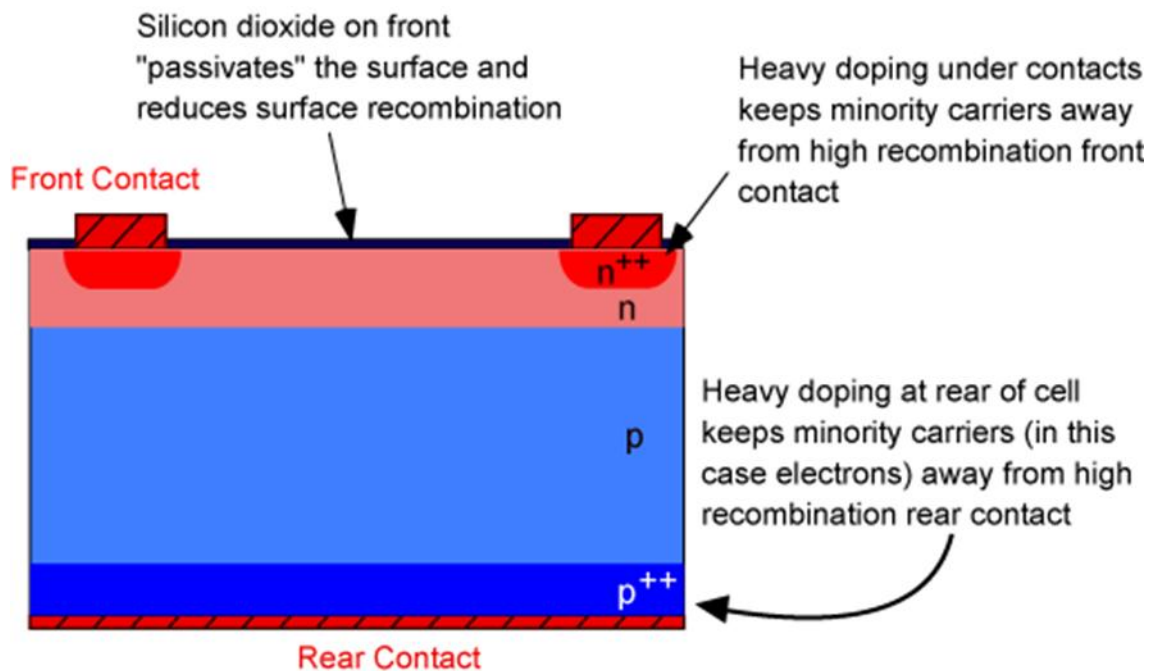
various values of the current, or measuring the resistance of contacts of different areas, using Ohms Law, *i.e.*, $R=V/I$.

64. A high ρ_c results in excessive loss of power and lower efficiency. Total series resistance for one-sun cells such as described in the '516 patent typically needs to be less than 1 ohm-cm². Back contact resistance typically makes up about 1% of this, so it should be less than 1×10^{-2} ohm-cm². This is only one component of total series resistance, and all need to be optimized simultaneously along with allowing maximum light collection at the front surface to maximize cell efficiency. This involves several tradeoffs and careful optimization.

65. Series resistance is particularly problematic for concentrator solar cells. Concentrator solar cells use external optics to concentrate high intensity sunlight on a cell front surface resulting in much higher current generation. Due to Ohm's law, higher currents make it necessary to significantly reduce series resistance to keep voltage losses low. Simply put, the high level of current generated in concentrator cells increases the losses due to series resistance proportional to the ratio of the concentration intensity. For so-called concentrator cells, the series resistance needs to be made lower by the same ratio as the solar concentration ratio. For this reason, concentrator cells have a very different metal gridline structure than that of the one-sun cell shown above. Using the example of acceptable contact resistivity for one-sun cells mentioned above, back contact

resistivity for a concentrator cell operating at 100 suns concentration should be less than 1×10^{-4} ohm-cm².

66. A commonly used method to reduce contact resistivity is to selectively provide especially heavy doping concentration in emitter regions of the cell that are in direct contact with the metal contacts. This not only reduces contact resistivity, but also produces a slight electric field between the heavily doped region and the more lightly doped regions of the cell, which repels some of the minority carriers away from the metal contacts where they would otherwise certainly recombine.



67. This method of surface and contact passivation is known as field effect passivation because the weak electric field between the heavily and lightly

doped regions does introduce a small barrier to minority carriers. The minority carrier concentration is then maintained at higher levels in the base region.

G. Solar Cell Design Principles

68. For one sun silicon solar cells, the design constraints caused by surface reflection, carrier collection, recombination, and resistance result in a maximum device efficiency of about 26%. To optimize solar cell performance, each objective must be pursued concurrently.

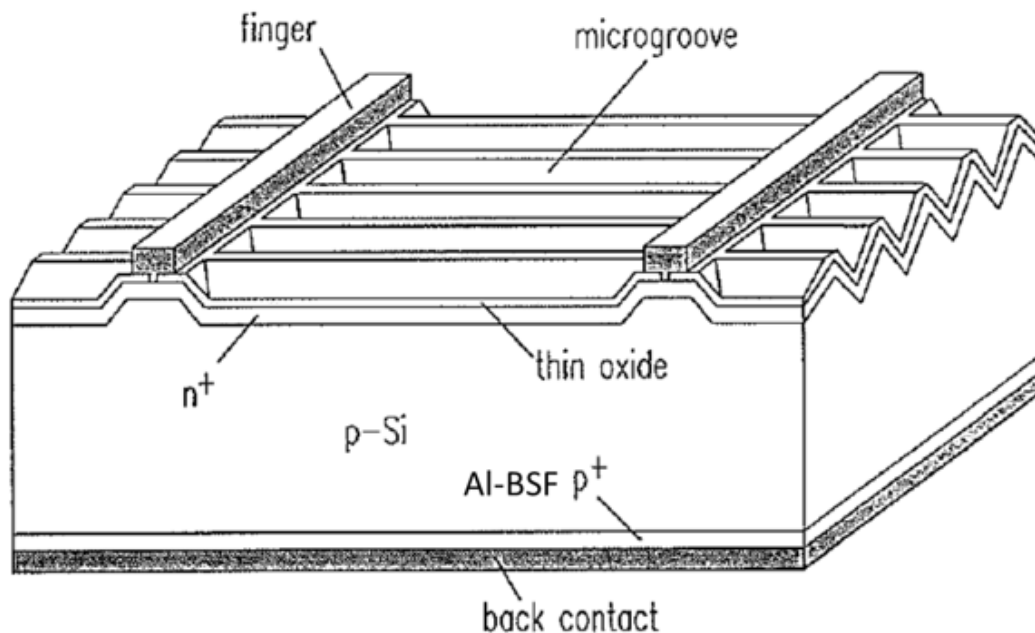
- Maximize the absorption of light and the generation of free carriers;
- Optimize collection of the photocarriers to deliver a current;
- Minimize recombination to generate a larger voltage; and
- Minimize dissipation of power in parasitic resistances.

69. The '516 patent describes the process for making a solar cell that addresses improvements pertaining to the last two of these points, reducing recombination and parasitic resistance by reconfiguring the back surface of the cell to substantially reduce recombination there while still allowing the current to pass to the metal contacts with acceptably low resistance. This is done using a new method for back surface design by introducing two elements on the back surface and forming a heterojunction comprised of a tunnel oxide layer and a heavily doped polysilicon (poly-Si) layer.

1. *Passivated Emitter Solar Cells*

70. Prior to the introduction of TOPCon solar cells, the most prevalent type of Si cells commercially produced were of the PESC, PERC or PERT type. The PESC (Passivated Emitter Solar Cell) was primarily focused on passivating the front emitter of the cell where most of the photogeneration takes place. A simple rear heavily diffused region using alloyed Al formed the back contact with a Back Surface Field (BSF).

The Passivated Emitter Solar Cell (PESC)



PESC

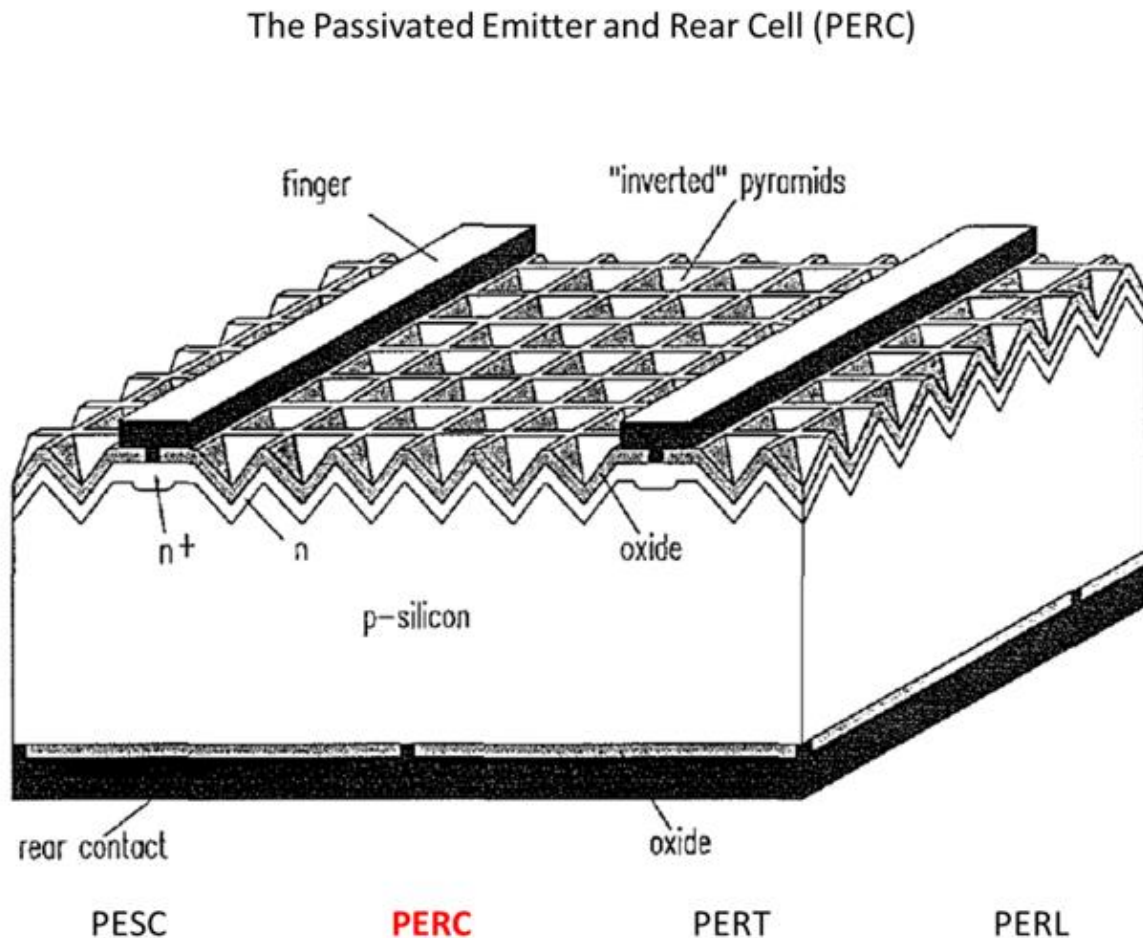
PERC

PERT

PERL

From Ph.D. Thesis of Aihua Wang, UNSW, 1992

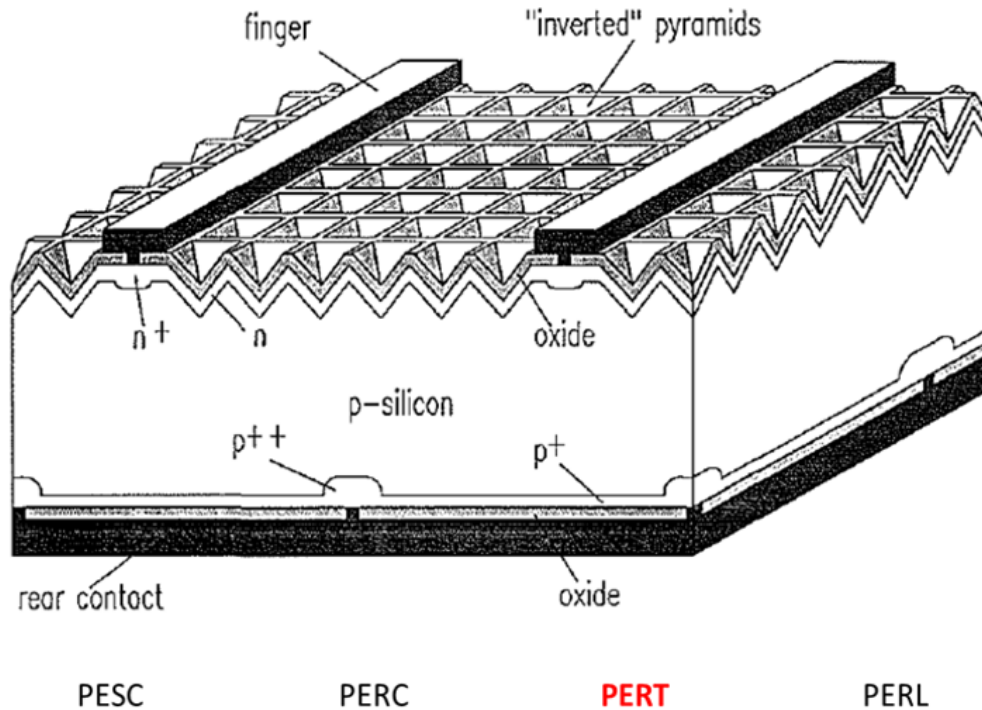
71. The PERC (Passivated Emitter and Rear Cell) was the next historical improvement in solar cell technology. This cell used a high-quality thermal oxidation on the rear of the cell to passivate most of its surface far more effectively than a simple Al-alloyed BSF was able to achieve. However, small holes had to be formed in this passivating oxide layer in order to make low-resistance contact to the metal beneath.



From Ph.D. Thesis of Aihua Wang, UNSW, 1992

72. Eventually, cell producers were able to get even better results by using an additional doping diffusion on the back surface specifically to get better BSF passivation there. The PERT (Passivated Emitter and Rear Total area diffused) included a dopant-diffused region over the entire rear surface to get better passivation than using a back-surface oxide alone. It also included an extra-heavy diffusion over the regions near the metal contacts for lower contact resistance and improved contact passivation. These cells still required the penetration of the passivating oxide layer in order to open conducting paths to the rear metal contacts.

Passivated Emitter, Rear Totally-diffused Cell (PERT)



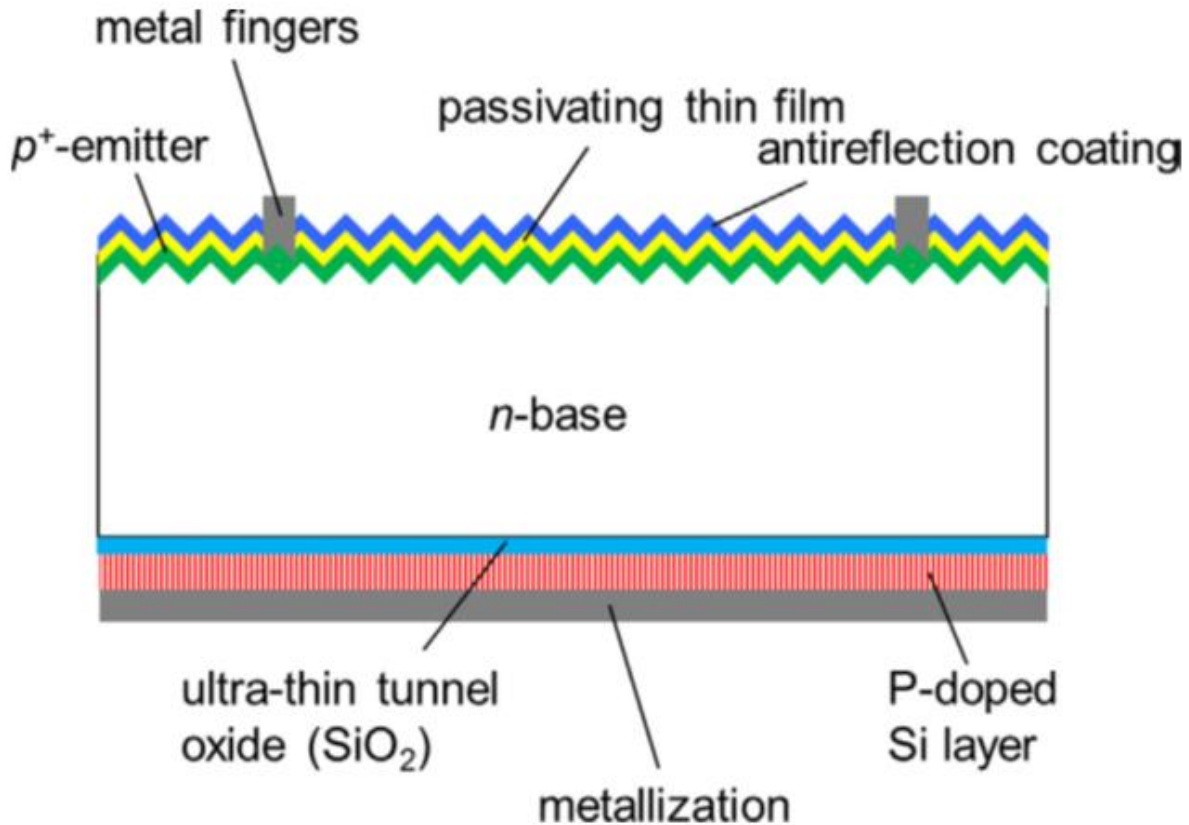
From Ph.D. Thesis of Aihua Wang, UNSW, 1992

73. This is where the technology stood for many years until the invention of the TOPCon cell (Tunnel Oxide Passivated rear Contact).

2. TOPCon Solar Cells

74. The term TOPCon was coined by researchers at the Fraunhofer Institute for Solar Energy Systems (Fraunhofer ISE) in 2013. See, e.g., Feldmann, et al., “A Passivated Rear Contact for High-Efficiency N-Type Silicon Solar Cells Enabling High VocS and FF > 82%” (28th European PV Solar Energy Conference & Exhibition, Paris, Sept. 30 – Oct. 4, 2013) (Ex. 1037).

75. Exhibit 1037 includes the Figure below:



TOPCon cell (Tunnel Oxide Passivated Rear Contact).

76. In this cell design, the back heavily diffused c-Si region of the PERT cell has been replaced by two layers: an ultra-thin tunnel oxide and a deposited phosphorus-doped N-type poly-Si layer.

a. Components of TOPCon Solar Cells

(i) Tunnel Oxides

77. Tunnel oxides are high-quality SiO₂ layers that are extremely thin, about 1.5nm, just about three atomic monolayers that cover the entire back side surface of the substrate. They are so thin that due to alignment of Si-SiO₂

bandgaps, majority carriers in the Si (the same polarity as the n-type substrate -- electrons in this case) can pass through them with very low resistance, while minority carriers (holes) are nearly all blocked. This significantly reduces the number of minority carriers in the poly-Si and at the metal contacts and suppresses recombination there. The high quality of the tunnel oxide layer (no dangling bonds or impurities) keeps recombination at the c-Si-SiO₂ interface low.

78. Tunneling can take place when the wave function of the electrons penetrates the oxide layer according to quantum theory. This can only occur to a substantial degree when the oxide layer is less than 2 nm.

79. Quantum tunneling enables majority carrier movement across the interface and almost completely blocks minority carriers. Due to its thinness, electrons can “tunnel” through the oxide layer rather than being blocked like the holes are.

80. The tunneling mechanism is described in Foglietti. Ex. 1014. Although Foglietti relates to bipolar transistors, the tunneling mechanism it describes also applies to solar cells.

81. According to Foglietti, interfacial oxides (tunnel oxides) are “generally less restrictive with respect to majority carriers (electrons) moving from the emitter region of the transistor into the base region than minority carriers (holes) moving from the base region into the emitter region. This phenomenon is

due to the tunneling probability of electrons being greater than the tunneling probability of holes.” Ex. 2014, ¶3.

82. According to Foligetti, the majority carrier “can tunnel through the interfacial oxide, Ex. 2014, ¶4, whereas holes are blocked from passing the interfacial oxide, *id.* at ¶5. Thus, Foglietti concludes, “under appropriate circumstances,” interfacial oxides (tunnel oxides) “may be modeled as a selective diode . . . wherein the electrons [] see a forward biased, conductive path, and the holes [] see a reverse-biased, non-conductive path.” *Id.* at ¶5. This tunneling mechanism improves transistor gain in Foglietti’s system. *Id.* at ¶¶4-5.

83. Notably, Foglietti specifies this improvement (provided by tunneling) “is substantially dependent upon various properties of the interfacial oxide.” Ex. 2014, ¶6. For one, the interfacial oxide (tunnel oxide) cannot be “too thick,” otherwise “the number of electrons which can tunnel through from the emitter into the base is reduced substantially.” *Id.* On the other hand, the interfacial oxide (tunnel oxide) cannot be “too thin,” otherwise “an insufficient barrier exists to block the hole current.” *Id.*

84. Moreover, the interfacial oxide (tunnel oxide) must also maintain integrity:

For example, since the interfacial oxide is subject to various types of subsequent thermal processing (e.g., subsequent poly CVD processing, metal deposition, anneal steps, etc.), the interfacial oxide

may lose its integrity, that is, the oxide may exhibit non-uniform characteristics spatially thereacross which in some cases may negatively impact the transistor performance. For example, if the interfacial oxide is fractured or becomes discontinuous, resulting in oxide islands, such fractures will be random and not repeatable from device to device; consequently, such fracturing causes unreliable transistor gain performance.

Ex. 2014, ¶7.

85. A “tunnel oxide” is different from the “chemical oxides” used by Kwark. See Ex. 1008, 743 (“For both structures, devices were prepared with and without a chemically grown oxide (chemox) by dipping half of the wafer which underwent a full RCA clean in dilute HF”); *see also id.* at Figs. 4-6 (descriptions referencing a “chemically grown interfacial layer”). Chemical oxides are formed using a wet (aqueous) chemical process, such as by dipping a Si wafer into a water-diluted HF solution. The chemical reaction that takes place between the Si, H₂O, and HF creates a thin SiO_x layer (Chemox) on the surface of the Si, not stoichiometric SiO₂. This Chemox layer is not necessarily of the high quality obtained from the thermal oxidation of Si in an O₂ environment. It may contain contaminants that were dissolved in the water, is not guaranteed to be completely uniform or reproducible, and does not result in an oxide with the exact ratio of 1:2 in the SiO₂ formulation, so it may contain dangling bonds and other defects which would make it unreliable.

86. Another type of oxide used in solar cells is a masking oxide. It is relatively thick, normally microns in thickness, compared to tunnel oxides, which are commonly extremely thin ($<2\text{nm}$). A masking oxide can be produced by a wet oxidation (grown with H_2O) which grows very fast. An effective tunnel oxide, which is a tunnel oxide with high reproducibility, quality, and uniformity, is typically grown in a dry oxidation (with O_2).

(ii) The Polycrystalline Silicon Layer

87. In a TOPCon structure, a layer of polysilicon heavily doped with N-type dopants is formed on the tunnel oxide. Polycrystalline silicon consists of many small, randomly oriented Si crystals. However, the band gap remains roughly the same as that of c-Si. The combination of a tunnel oxide and a doped polycrystalline silicon layer provides excellent passivation and carrier selectivity on the N-type substrate.

VII. THE '516 PATENT

88. The '516 patent discloses and claims a novel front contact solar cell with former emitter. Ex. 1001, Title.

89. The '516 patent describes, with reference to Fig. 1, a cross-section of a solar cell in accordance with an embodiment of the present invention. Ex. 1001, 1:66-67.

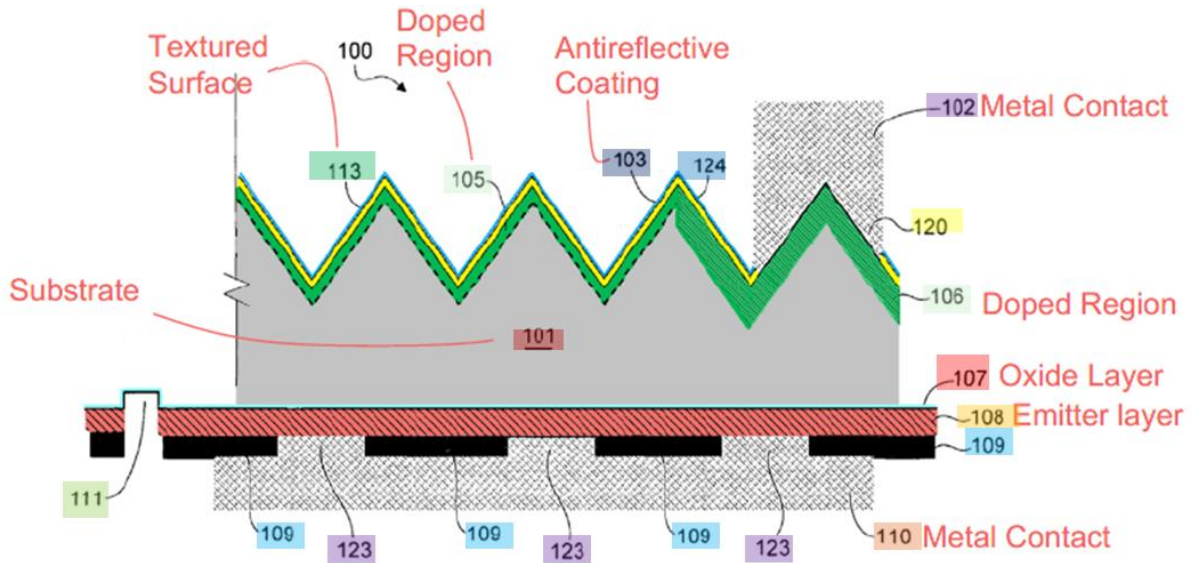


FIG. 1

Ex. 1001, Fig. 1 (annotated).

90. In this embodiment, an N-type silicon substrate 101 is formed from a crystalline silicon wafer. Ex. 1001, 3:50-54. The front side of the substrate is located at the top of Fig. 1 and faces the sun, the back side of the substrate is at the bottom of Fig. 1 and faces away from the sun. *Id.* at 2:27. A tunnel oxide 107, which can be silicon dioxide, is provided on the back side of the substrate 101. *Id.* at 3:62-66.

91. A layer of polysilicon 108 is deposited on the tunnel oxide layer 107 to form the polysilicon emitter 108. Ex. 1001, 3:66-4:2. A dopant source layer 461 (not shown in Fig. 1) is formed on the polysilicon emitter 108 (i.e., formed on the back side of the polysilicon emitter) and the dopant is later driven into the polysilicon with a drive-in step. *Id.* at 4:5-58. A capping layer 462 (not shown in

Fig. 1) is formed over this dopant layer to keep the dopants from escaping during the dopant drive in process. *Id.* at 4:10-13. An edge isolation trench 111 is formed near the edge of the substrate 101 and is cut through the capping layer all the way through to contact a small area of the substrate 101. *Id.* at 4:20-27.

92. Exposed surfaces of the substrate 101 (on the front side) are etched to form pyramid 113 like structures. Ex. 1001, 4:28-33. This etching step removes the previously applied layers 401 and 402, as can be seen in Figs. 4D and 4E. An N-type dopant source 412 is formed on the textured surface of the substrate. *Id.* at 4:35-38. The N-type dopants from dopant layer 412 are then driven-in to the substrate 101 forming N-type doping regions 105 and 106. This drive-in step also drives in the dopants from the doping source layer 461 into the back side of the polysilicon (polysilicon emitter 108), thus forming a **backside junction**. *Id.* at 2:28-31, 4:52-65. This drive-in step may be formed in-situ, which the patent explains is “a single manual (i.e., by fabrication personnel) loading of the substrate 101 in a furnace or other single chamber of multi-chamber processing tool.” *Id.* at 4:58-68. After this drive-in step, layers 461 and 462 become silicon dioxide layer 109 and the front side of the silicon becomes N-doped region 106. *Id.* at 4:58-65, 2:28-31. A thin thermal silicon dioxide layer 124 is provided as a passivation layer on the surface of the silicon substrate 101. *Id.* at 4:65-67.

93. An antireflective (also serving as a dielectric) coating of silicon nitride layer 103 is formed over the textured surface 113 after removal of the N-type dopant source layer 412. Ex. 1001, 5:20-26. A front contact mask is then provided on the silicon nitride layer 103 to create a pattern for forming contact holes 102. *Id.* at 5:28-32. A back contact mask 422 is used on the silicon dioxide layer 109 to create a pattern for the back side contact holes 123. The holes 102 and 123 are then etched away. *Id.* at 5:33-43.

94. A back side metal contact 110 is formed on the silicon dioxide layer 109 to fill the contact holes 123 and make electrical connection to the polysilicon emitter 108. Ex. 1001, 5:48-55. Finally, front side metal contact 120 is formed on the silicon nitride layer 103 to fill contact holes 120 and make electrical connection to the substrate 101. *Id.* at 5:56-58.

95. While the above description may describe a solar cell with an N-type substrate and a P-type polysilicon emitter forming a backside junction, the patent claims are broader than that and can encompass an N-type crystalline substrate having an N-type polysilicon emitter forming a heterojunction, which is the “backside junction” of claim 9. This is shown in the below comparison of the independent claims 1 and 9 below.

Claim 1	Claim 9
1. A solar cell having a front side facing the sun to collect solar radiation during normal operation and a	9. A solar cell having a front side facing the sun to collect solar radiation during normal operation and a backside

Claim 1	Claim 9
backside opposite the front side, the solar cell comprising: an N-type silicon substrate; a textured surface on the N-type silicon substrate on the front side of the solar cell; an antireflective layer over the textured surface of the N-type silicon substrate; a P-type polysilicon emitter formed over the N-type silicon substrate and forming a backside junction with the N-type silicon substrate; an oxide layer formed between the P-type polysilicon emitter and the N-type silicon substrate; a negative polarity metal contact making an electrical connection to the N-type silicon substrate from the front side of the solar cell; and a positive polarity metal contact making an electrical connection to the P-type polysilicon emitter from the back-side of the solar cell.	opposite the front side, the solar cell comprising: a substrate having a textured front surface; an emitter layer formed over a back surface of the substrate, the emitter layer formed over a backside junction with the substrate; an oxide layer formed between the back surface of the substrate and the emitter layer; a first metal contact making an electrical connection to the substrate on the front side of the solar cell; and a second metal contact making an electrical connection to the emitter layer of the backside of the solar cell, the first metal contact and the second metal contact being configured to allow an external electrical circuit to be powered by the solar cell.

Ex. 1001, claims 1 (6:4-22), 9 (6:42-57) (emphasis added).

96. As is shown above, claim 1 is directed toward specific N-type and P-type dopant sources in the silicon and polysilicon layers, respectively. Claim 9, on the other hand, is silent with respect to the types of dopant sources used to dope the silicon and polysilicon layers. Therefore, at least with respect to the dopant sources, claim 9 is broader in scope than claim 1. Therefore, I understand that claim 9 is not limited to N-type silicon and P-type polysilicon layers.

VIII. THE '516 PATENT PROSECUTION HISTORY AND RELATED APPLICATIONS

97. During prosecution of the '516 patent's application, the Examiner issued a restriction requirement between the claims "drawn to a solar cell" and those "drawn to a method of making a solar cell." Ex. 1002, 61. SunPower elected the solar cell claims for the '516 patent and filed a divisional application to pursue the method claims challenged here. Ex. 1002.

98. Original claim 9 (application claim 17) recited all elements is claim 9 except for "an oxide layer formed between the backside of the substrate and the emitter layer." Ex. 1002, 19. The examiner rejected this original claim. Ex. 1002, 76-78. Applicant amended the original claim to recite "an oxide layer formed between the back surface of the substrate and the emitter layer." Ex. 1002, 135. The Examiner then allowed the amended claims 17-20 in the application (claims 9-12 of the '516 patent. Ex. 1002, 152.

99. Patent Owner then filed the application that led to U.S. Patent No. 8,878,053 (the other subject of the divisional required by the Examiner) on July 13, 2012. Ex. 1038, 8.

100. After allowance of the '516 patent, three continuations were filed seeking additional claims of varying scope:

- U.S. Patent Application No. 14/504,771 (the “’771 application”), filed October 2, 2014, claiming “a doped diffusion region in the substrate” and “a front electrode that is coupled to the doped diffusion region on the front surface of the substrate.” Ex. 1005, 470. This application was abandoned after an appeal of the Examiner’s decision to the Board. *Id.*, 506-520, 522.
- U.S. Patent Application No., 16/460,035 (the “’035 application”), filed July 2, 2019, claiming “a plurality of dot-shaped N-type doped regions in the N-type silicon substrate under the antireflective layer, each of the plurality of dot-shaped doped regions having a dot shape as seen from a plan view of the solar cell” and “a first metal contact disposed on the front surface of the N-type silicon substrate, wherein the first metal contact is in electrical contact with the plurality of dot-shaped N-type doped regions.” Ex. 1018, 235. This application was abandoned after an appeal of the Examiner’s decision to the Board. *Id.*, 285-293, 295.

- U.S. Patent Application No. 17/870,268 (the “’268 application”), filed July 21, 2022, filed with claims directed towards a solar cell including a dielectric layer. Ex. 2013, 25-27. The ’268 application is currently under examination. *Id.*, 287-304 (a Final Rejection was issued September 16, 2024).

IX. PERSON OF ORDINARY SKILL IN THE ART

101. CSI and its declarant, Dr. Sanjay Banerjee, assert that the “person of ordinary skill in the art in the ’513 Patent’s field of solar cell design or manufacture in the [sic] 2008 (‘Skilled Artisan’) would have been someone with an advanced degree involving the discipline of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field.” Petition, 3-4; Ex. 1003, ¶45. CSI also asserts, alternatively, that the Skilled Artisan “would have had a bachelor’s degree in electrical engineering, applied physics, or materials science, and at least three years of experience designing, developing, or researching in the field.” *Id.* For the purposes of this Response, I have applied CSI’s level of ordinary skill.

X. CLAIM CONSTRUCTION

102. CSI does not believe that claim construction is necessary to resolve this Petition. Petition, 10. Patent Owner concurs.

103. Patent Owner's counsel provided me with legal principles that are relevant to claim construction. See § V above. I considered those legal principles in forming my opinions in this section.

104. Patent Owner's counsel asked me to consider claim construction as of the date of the invention. See § IV.A above. My opinions are the same regardless of which date is used.

XI. THE CITED REFERENCES AND OTHER PRIOR ART

105. CSI's Petition asserts five grounds of unpatentability against the Challenged Clams.

106. In Ground 1, CSI claims that claims 9-11 are obvious in view of Meier, Okayasu, Borden, and Jordan. Petition, 3. In Ground 2, CSI claims that claims 9-11 are obvious in view of Meier, Okayasu, Gan, Foglietti, and Jorden. *Id.* In Ground 3, CSI claims that claims 9-12 are obvious in view of Froitzheim and Gan. *Id.* In Ground 4, CSI claims that claims 9-12 are obvious in view of Froitzheim and Kwark. *Id.* In Ground 5, CSI claims that claims 9-12 are obvious in view of Froitzheim and Borden. *Id.*

107. I understand that with regard to Grounds 1 and 2, the Board has reviewed these Grounds and found that CSI's arguments are an improper incorporation by reference of ten paragraphs of Dr. Banerjee's declaration and that there is no provided authority establishing CSI may rely of findings of an

Examiner of a Board decision involving different claims from a different patent application for this proceeding. Institution Decision (Paper 13), 26-28. As this is a legal issue, I am not providing any analysis regarding this issue.

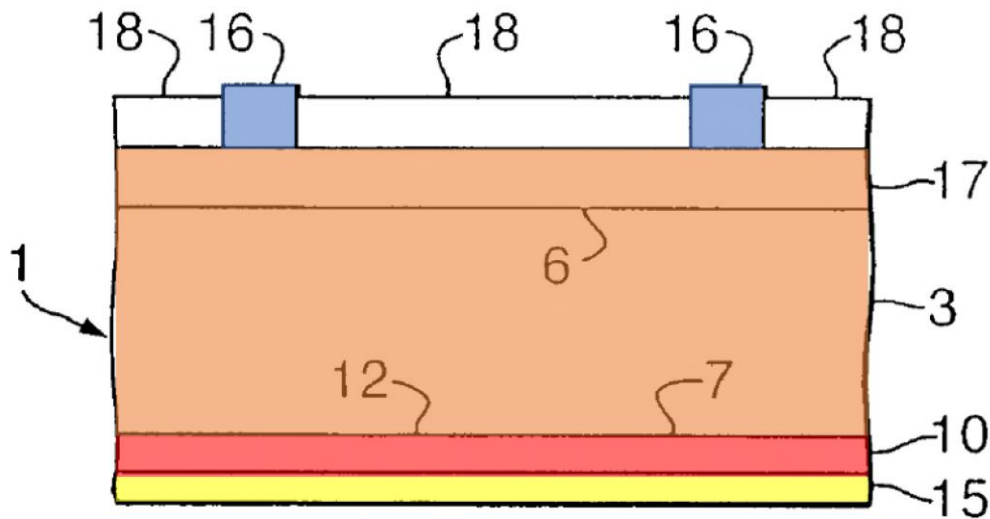
108. As is discussed below, Froitzheim discloses a manufacturing process that requires a very high temperature anneal. I will explain how both Gan and Kwark warn against using a high temperature anneal because annealing at a high temperature causes the beneficial interfacial oxide to break up such that all the benefits of adding the oxide in the first place disappear, which defeats the purpose that Gan and Kwark disclose they are trying to achieve. The Gan Thesis further discusses this fundamental incompatibility. Therefore, in my opinion, at the time of the priority date of the '516 patent it is my opinion that a POSITA in the art would not have believed there would be a reasonable expectation of success in making these combinations and, consequently, would not have been motivated to combine them as proposed by Petitioner.

109. In my opinion, and based on the requirements discussed in § V.B above for analyzing if something would have been obvious, I disagree with the conclusions of Dr. Banerjee and Petitioner that the subject claims would have been obvious to a POSITA at the time of the priority date. As I explain below, CSI has not satisfied its burden with respect to *any* of its obviousness grounds.

A. Froitzheim (Ex. 1006)

110. EP1732142A1 (“Froitzheim”) explains that in conventional solar cells, an N-type emitter is located on the front of the cell to form a P/N junction with an oppositely doped P-type substrate. Petition, 21; Ex. 1006, ¶2; Ex 1003, ¶84. In contrast to such conventional cells, Froitzheim proposes to form the emitter at the rear (back) side of a solar cell creating a P/N junction on the rear side. Ex. 1006, ¶8.

111. I will refer to Figure 1 of Froitzheim as provided in the Petition.



Petition, 21 (citing Ex. 1006, ¶24) (annotations in Petition).

112. As described by Froitzheim, the proposed solar cell includes an N-doped substrate 3 having a front side 6 and a rear side 7. Ex. 1006, ¶24.

Froitzheim provides a P-doped layer 10, *id.* at ¶22, which is actually a region of the substrate 3 doped with boron to form a P/N junction 12, *id.* at ¶25. A contact 15

covers a large part or substantially all of the rear side 7 of the cell. *Id.* at ¶27. The front side 6 of the substrate is heavily doped with an N-type dopant, e.g., phosphorous, to provide a heavily N-doped layer 17, which is formed in a region extending from the front side 6. *Id.* at ¶28. Contacts 16 are fabricated to contact the top side 6 of the underlying substrate 3. *Id.* Passivation layer 18 is formed over the exposed areas of the N-type doped layer 17. *Id.* at ¶30.

113. It should be noted that Froitzheim teaches doping the front side 6 of the substrate 7 with an N-type dopant and doping the back side 7 of the same silicon substrate 3 with a P-type dopant. Petition, 21; Ex. 1006, Abstract (“A solar cell comprising a silicon body layer of N-type bulk doping having a front side and a rear side; a non-alloyed P-type doped region at the rear side of the body layer and forming a P/N junction therewith; a rear side contact in electrical connection with the P-type doped region; and a front side contact in electrical connection with the N-type silicon body layer, and a method of manufacturing such a solar cell.”) ; *see also id.* at ¶¶10, 11, 40.

114. To drive in dopants into the rear side 7, Froitzheim teaches “the wafer is treated in an atmosphere that contains oxygen at a temperature of 900 to 1200 degrees centigrade, preferably between 1000 and 1100 degree C, to generate and oxide layer and to drive in the dopant.” Ex. 1006, ¶042.

115. Dr. Banerjee testified as to why Froitzheim preferred a temperature between 1000°C and 1100°C:

Q: Why would they prefer to use 1000 to 1100 degrees, do you know?

A: That's because the higher the temperature, the higher is the diffusion coefficient which has a so-called Arrhenius dependency... So higher temperature, more will be the diffusivity. And that will determine the junction depth. But it also depends on diffusion time...

Q: So they're trying to achieve a higher diffusion. Is that correct?

A: . . . So you are trying to achieve a certain junction depth and a certain doping concentration. And the two main parameters, the diffusion temperature, and the diffusion time. Longer the diffusion time, higher the temperature. Everything else being the same, you'd get a deeper junction and the higher concentration of the surface. Shorter the temperature – or diffusion time and lower the temperature, you get a shallow junction. So those are the norms that a POSITA would use.

Q: Why would it be preferable to have a deeper junction?

A: It depends on the device design parameters. You'd want a junction of the appropriate depth to achieve the maximum efficiency in your solar cell.

Ex. 2023, 81:16-83:10.

116. I agree with Dr. Banerjee that the 1000°C to 1100°C temperature preferred by Froitzheim maximizes the efficiency of the solar cell. Reducing the

dopant drive in temperature to the lower temperatures taught by Gan and Kwark would reduce the efficiency of the solar cell described by Froitzheim.

117. It should be noted that Froitzheim does not disclose the use of an oxide and emitter layer recited in claims 1 and 9, and instead proposes using a silicon substrate 3 with doped regions on its front side and back side. Froitzheim also does not teach or suggest the use of an oxide layer, e.g., a tunnel oxide, between the rear surface of the substrate and an emitter layer as required by claim 9.

118. It is also clear from reading the references that Froitzheim is the only example among the prior art applied by Petitioner which shows an operable solar cell. As I will explain below, the Gan and Kwark references that Petitioner relies upon were research papers reporting on the theoretical use of an oxide layer and polysilicon layer formed on the back side of a crystalline silicon substrate. The Gan Thesis explains that neither Gan nor Kwark was able to create this structure so that it was reproducible and reliable. Given the discouraging results reported in the Gan Thesis and a divergence in processing temperature discussed below between Froitzheim's teachings and the teachings of Gan and Kwark, a POSITA would have little motivation to combine the unproven and unreliable teachings of Gan and Kwark to modify Froitzheim's solar cell according to their teachings.

Moreover, any expectation of success from doing so would have been highly speculative.

119. Petitioner tries to modify Froitzheim to include an oxide/polysilicon layer from Gan and Kwark to meet the emitter layer/oxide layer requirements of claim 9. However, Petitioner leaves unexplained how that would work since Froitzheim teaches driving in dopants at a high temperature that Gan and Kwark both teach must be avoided to obtain acceptable values of contact resistivity (ρ_c) and emitter saturation current density (J_o).

B. Gan (Ex. 1007)

120. First, it should be understood that there are two Gan publications of relevance to the positions of Petitioner. One is a publication that Petitioner uses as the Gan prior art reference in combination with Froitzheim. This is Gan et al., “*Polysilicon Emitters for Silicon Concentrator Solar cells*,” Proceedings of the 21st IEEE-PVSC (“Gan”), which was a paper presented in 1990 (Ex. 1007, face, ii-iii). Petition, 22.

121. The other is the Gan Thesis (Ex. 2003). The Gan Thesis was published and publicly available on the shelves in the Stanford Library on April 10, 1991, which is prior to the priority date of the ’516 patent. See Ex. 2022, ¶23. I understand that it can be assumed that a POSITA would have had knowledge of the Gan Thesis before that priority date. The Gan Thesis is important for several

reasons, including telling the complete story of why the technology disclosed in Gan was experimental, could not be reliably reproduced, and was not suitable for use in commercial concentrator cells.

122. In both Gan (Ex. 1007) and the Gan Thesis (Ex. 2003), the common author, Gan, is describing experiments trying to thread a needle to produce the optimum temperature to break up an interfacial oxide a little, but not too much. This interfacial oxide layer is formed between a crystalline silicon substrate and a polysilicon layer applied over the rear surface of the substrate. Gan tried different anneal temperatures and durations, and determines that above 900°C, the oxide breakup becomes too much. *See, e.g.*, Ex. 1007, 248 (“Considering the significant increase of J_o caused by increasing the drive-in temperature from 900 to 1000°C. . .”); *see also id.* at (Table 1). Gan is not describing building an actual one sun solar cell, rather Gan is describing experiments on poly-Si emitters that might be useful in a concentrator solar cell.

123. Petitioner and its expert, Dr. Banerjee have made clear that the proposed Froitzheim-Gan, Froitzheim-Kwark, and Froitzheim-Borden combinations start with the method described in Froitzheim to make the silicon substrate and stops prior to adding the dopants. Petition, 44, 60. Then the combinations switch to Gan/Kwark/Borden to “perform Gan’s steps of thin thermal oxide growth to form the interfacial layer and polysilicon deposition to

form the polysilicon on the back side of the wafer” after which the polysilicon would be doped using the steps in Froitzheim to form the polysilicon emitter. *Id.* at 45-46 (citing Ex. 1003, ¶150, Ex. 1008, 742, 745); see also Ex. 2023, 85:14-20 (“Q: Then after you add the oxide in [and] and the polysilicon layer from Gan, then you would follow Froitzheim steps to add the dopant. Correct? A: Yes. Q: And would that be the same with Kwark and Borden? A: Well, this part essentially, yes.”).

124. Below is shown the specific steps used in Gan to add the oxide and polysilicon layers. Note, the steps with an “*” are the steps where Gan measures the J_o values.

- | | |
|--|---|
| <p>Start of process used in Gan ➡</p> | <ol style="list-style-type: none"> 1. Field oxidation (2000 Å)*. 2. Polysilicon-substrate contact opening*. 3. Thin thermal oxide growth at 800 °C*. (10-minute oxygen flow) 4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C)*. 5. First-step anneal *. 6. Polysilicon finger definition. |
| <p>End of process used in Gan ➡</p> | <ol style="list-style-type: none"> 7. Undoped glass deposition (2000 Å). 8. Metal-polysilicon and metal-substrate contact opening. 9. Doped glass deposition on both sides of the wafer*. 10. Drive-in; 900-1000 °C*. 11. Doped glass stripping and Al-1% Si alloy deposition. 12. Metal finger definition. |

Ex. 1007, 246 (annotations added)

125. Step 4 (the anneal performed at 1050°C) causes breakup of the oxide layer. This step and step 10, the drive-in step, were the subject of Gan’s

measurements to try to achieve acceptably low J_o values. Ex. 1007, 246. The anneal of step 4 is used to break up the thin oxide layer, and the second anneal performed at step 10 is used in Gan to drive in the dopants. This step 10 anneal is referred to as “the second-step anneal” in Gan’s table 1 below. Ex. 1007, 248.

Table 1: The effect of the second-step anneal on J_o and ρ_c .

	N-type		P-type	
	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

Ex. 1007, 248, Table 1

126. Note that Table 1 of Gan shows that as you increase the temperature and time in the second step appeal, the value of J_o increases, which means more recombination and lower cell efficiency and is not a desired result.

127. The Petition states that “before introducing the boron dopant by diffusion at the rear side of the substrate (for example, as described in ¶40-41 of Froitzheim, the Skilled Artisan would perform Gan’s steps” to grow the thin thermal oxide and form the polysilicon layer. Petition, 47. Paragraphs 40-42 of Froitzheim are shown below which are the sections of Froitzheim that Petitioner used to add the dopant to the proposed combination and then drive in the dopants.

30 **[0040]** Providing a non-alloyed p-type doped region is done by a process which introduces dopant, preferably boron, only by diffusion into the rear surface of the body layer. Several processes for boron diffusion are known in the art, including diffusion from the gas phase or from liquid and solid phases applied to the surface. A preferred process is that known for the making of a p+ back surface field on the rear side of conventional p-type cells. This process as well as prior art is described in USA patents No. 5899704 and 6096968, which are incorporated by reference.

35 **[0041]** In general terms, a diffusion source layer that contains boron as a dopant is applied, e.g. spun, only onto the back of the n- doped silicon wafer. The diffusion source layer is one that contains boron and out of which the boron is thermally driven. The diffusion source layer is preferably applied by means of a boron doping resist. In addition to boron or its compounds, this resist contains powdery SiO₂ in a suspension. This doping resist is normally used for generating high dopings in power semiconductors. It may be applied in liquid form and may for example be spun on.

40 **[0042]** A suitable doping liquid is Siodop (TM) of Merck. Then the wafer is treated in an atmosphere that contains oxygen at a temperature of 900 to 1200 degree centigrade, preferably between 1000 and 1100 degree C, to generate an oxide layer and to drive in the dopant.

Ex. 1006, ¶¶40-42 (annotations added)

128. Froitzheim’s dopant drive-in steps are performed at preferably between 1000°C and 1100°C. Ex. 1006, ¶42. Froitzheim uses these high temperatures to get the correct dopant concentration and junction depth. Ex. 2023, 81:7-83:10. However, at these dopant drive in temperatures, the benefit of adding the thin oxide layer of Gan is eliminated, to the point that Gan did not even test dopant drive in steps at temperatures greater than 1000°C.

129. As discussed in the Petition, Gan examined “polysilicon emitters with a thermally grown interfacial oxide” for solar cells. Petition, 36 (citing Ex. 1007, 245). Gan also taught that “a very thin oxide (interfacial oxide)” “[a]lways exists” between the polysilicon emitter and the substrate.” Ex. 1007, 245. In my opinion, Petitioner cherry picks isolated quotes from Gan and stitches them together to spin the false tale that Gan’s experiments with an interfacial oxide layer between a silicon substrate and a polysilicon layer were completely successful and ready for adoption by a POSITA. Petition, 36 (“Gan found that solar ‘cell performance can

be improved if the diffused-emitter [*i.e.*, an emitter doped into the substrate, as in Froitzheim] is replaced with the polysilicon emitter,...””) (citing Ex. 1007, 245; Ex. 1003, ¶128). This is not true because, as explained below, Petitioner ignores teachings about drive-in temperatures in Froitzheim and Gan that a POSITA would have understood to make such combination incompatible.

130. First, a POSITA would have understood from the title of the Gan reference—“*Polysilicon Emitters for **Silicon Concentrator Solar Cells***”—that the experiments discussed in the article pertained to the specialized field of concentrator cells discussed above. As I explain in ¶¶48-50, concentrator solar cells and one sun solar cells like Froitzheim are different and operate in very different environments with different resistivity requirements.

131. Next, Petitioner ignores the full extent of the failures that Gan encountered which, as shown below, are documented in the Gan Thesis. As I will explain below, Gan was not able to show reliable or consistent results with his experiments, and, therefore, Petitioner does not (1) show a reasonable expectation of success and (2) establish that a POSITA would have been motivated to combine Gan’s experiments with the one sun solar cell of Froitzheim.

132. I note that Petitioner relies heavily on the below Fig. 4 of Kwark in reaching its conclusion that it would have been obvious to a POSITA to combine

the teachings of either the Gan reference or Kwark and the teachings of Froitzheim. See Petition, 46. I will explain below why that is not so.

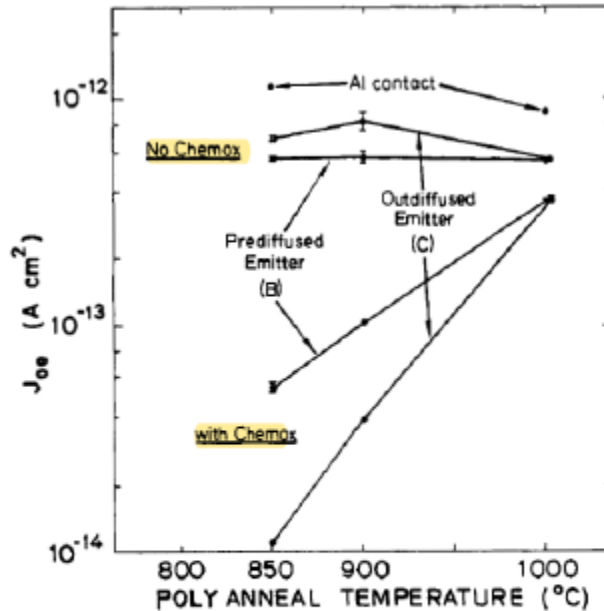


Fig. 4: emitter saturation current for POLY contacts with and without a chemically grown interfacial layer vs. anneal temperature. Thicknesses range from 3000-3600 angstroms. Note the large difference when the interfacial oxide is missing.

Petition, 27 (citing Ex. 1008, Fig. 4) (annotations in Petition).

133. Petitioner’s expert states that the combination “would have been well within the level of ordinary skill in the art” and involved “simple substitution of one known element and corresponding fabrication steps for another to obtain predictable results.” Petition, 34 (citing Ex. 1003, ¶104). With reference to teachings in Gan and the Gan Thesis, I demonstrate below that this is not true and is inconsistent—even contrary—with the teachings in the art.

134. As will be shown below, the Gan Thesis, which discusses Gan's own work and also Kwarck's work in more detail, catalogs for a POSITA a variety of failures and overall lack of success. Further, I find no merit in CSI's citations to Dr. Banerjee's testimony support for its contention that the combination of Gan and Froitzheim would yield predictable results. See Petition, 47-48 (citing Ex. 1003, ¶¶152-55).

135. Starting with the title of Gan (Ex. 1007), a POSITA would have understood that Gan addresses silicon **concentrator** solar cells and not one sun solar cells that are the concern of Froitzheim and the '516 patent. Ex. 1007, 245, Title ("Polysilicon Emitters for Silicon **Concentrator** Solar Cells.") (emphasis added). The Petition and Dr. Banerjee's declaration also allegedly quote Gan and say "[w]hile Gan referred in part to silicon concentrator solar cells, it more broadly suggested that a polysilicon emitter with interfacial oxide is "quite useful for silicon solar cells." Petition, 43 (citing Ex 1007, 249); *id.* at 44 (citing Ex. 1007, 249; Ex. 1003, ¶147). However, in the Conclusion to his paper Gan states "[f]rom the cell modeling, polysilicon emitters with these qualities can be useful for silicon concentrator solar cells." Ex 1007, 249. As I explained in ¶¶48-50, concentrator cells generate multiple times more free electrons than one sun solar cells, requiring concentrator solar cells to have a much lower resistive path from the substrate to the emitter, through the metal contacts and gridlines, than in a one sun solar cell.

A review of the experimental and modeling results reported in the Gan Thesis, including mention of high current levels in the range of 100 A/cm² (equivalent to 2500 suns), Ex. 2003, 28 (9 in original), indicate that the “modeling” referred to by Gan (Ex. 1007) were of silicon concentrator solar cells.

136. In sum, a POSITA focused on developing a one sun cell as taught by the '516 patent would not turn to the teachings of Gan because of its focus on silicon concentrator solar cells. Therefore, a POSITA would not look to modifying the one sun solar cell structure of Froitzheim with the teachings of Gan relating to concentrator solar cells.

137. Turning to the substance of the teachings of Gan, that reference is very specific about the effect of a high temperature anneal on the interfacial oxide layer between the silicon and polysilicon layers:

In either case, the oxide is not thermally stable; *i.e.*, it tends to break up during high temperature anneals. The breakup of the interfacial oxide has direct impact on both majority and minority carrier transport in the polysilicon emitter. This can be seen from the dependence on the specific contact resistivity (ρ_c) [6] and the emitter saturation current density (J_o) [1,2,3,4,5,6,7] upon either the anneal condition or the oxide integrity.

Ex. 1007, 245.

138. Gan specifically says that when the temperature is high and the oxide loses its integrity, the ρ_c is low and the J_o is high:

With the effect of the interfacial oxide is negligible, such as when the interfacial oxide loses its integrity in high temperature anneals, the ρ_c is low ($\sim 2 \times 10^{-7} \text{ } \Omega\text{-cm}^2$) [6] and the J_o is high ($\sim 1 \times 10^{-12}$) [1,3].

Conversely, when both the carriers are mostly blocked by the interfacial oxide, like for an intact chemical oxide ($\sim 15 \text{ } \text{\AA}$), the ρ_c is high and the J_o is low.

Ex. 1007, 245.

139. Gan tells a POSITA that it is optimal to have both a low value for J_o [emitter saturation current density] and ρ_c [contact resistivity], and this is achieved when “when both carriers are mostly blocked by the interfacial oxide.” Ex. 1007, 245, 249. What Gan is trying to determine is the “ ρ_c and J_o when only a small fraction of the interfacial oxide is broken.” *Id.* According to Gan “there always exists a very thin oxide (interfacial oxide), which can be the by-product of the cleaning process or is grown intentionally . . . In either case, **the oxide is not thermally stable, i.e., it tends to break up during the high temperature anneals.**” *Id.* at 245 (emphasis added). Gan explains that “[t]he first-step anneal, which serves to break up the oxide, was performed at higher temperature than that for the second-step anneal which aims for the dopant drive-in.” *Id.*

140. Gan also states that “one [example] has the first-step anneal at 1050°C for 30 minutes, the other [example] has 1050°C for 2 hours . . . Note that, the devices that received a 30-minute first-step anneal have higher intercepts than those that received a 2-hour first-step anneal. This indicates that more oxide

breakup occurs when the anneal time increases.” Ex. 1007, 247. Gan further states “[w]hen only a very small fraction of the interfacial oxide is broken, it is possible that the interfacial oxide on each contact may not be broken equally. Consequently, this gives rise to the fluctuation of the resistance measured. On the other hand, the fluctuation will be subdued when more oxide is broken.” *Id.* In fact, this oxide layer breakup happens in both Gan and Kwark. The Gan Thesis discusses this same phenomenon about Kwark, as is discussed below.

141. Gan teaches, and Dr. Banerjee agrees, that dopant drive in for the polysilicon layer on the rear surface of the substrate occurs at step 10 of Gan’s process flow, see, ¶123, *supra.*, This is Gan’s “second step anneal” and is optimal when performed at “900°C for 4 hours.” Ex. 1007, 247.

142. As explained above (¶¶114-116), Froitzheim teaches “the wafer is treated in an atmosphere that contains oxygen at a temperature of 900 to 1200 degrees centigrade, preferably between 1000 and 1100 degree C, to generate and oxide layer and to drive in the dopant.” Ex. 1006, ¶42.

143. Gan ran multiple experiments for combinations of temperatures for the first anneal and the second anneal (for dopant drive in) and reported the results in Figure 6, which is a plot of ρ_c v. J_o , with a key in the top right that shows “the type of polysilicon emitter, the first-step anneal (temperature/minute), and the

second-step anneal (temperature/minute).” Ex. 1007, 249, Fig. 6. The goal was to provide low values for J_o .

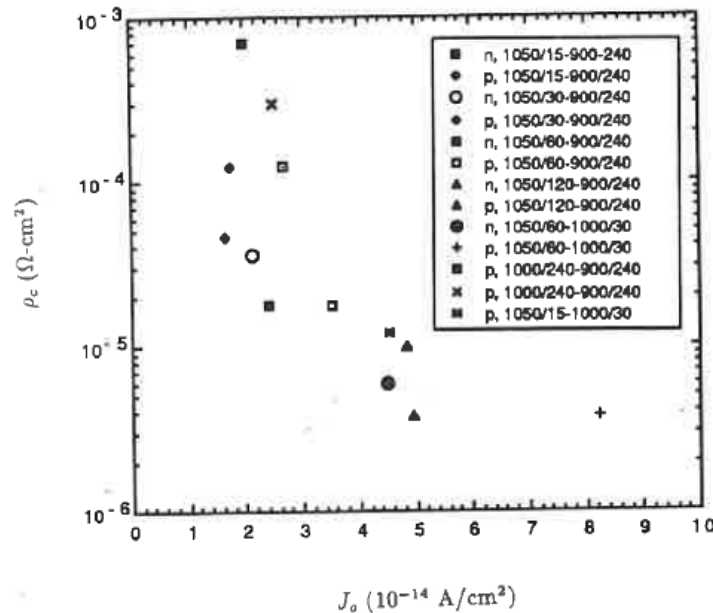


Figure 6: ρ_c - J_o of this work.

Ex. 1007, Fig. 6.

144. This graph clearly shows that the higher the temperatures of the second step anneal (the anneal to drive the dopants into the polysilicon), the higher the value of J_o . In fact, this figure shows much lower J_o values for the 900°C second anneal (“regime 1”) than for the 1000°C second anneal (“regime 2”). Gan then discusses this figure and observes for regimes 1 “ J_o is almost constant while ρ_c drops drastically” and for regime 2 “ ρ_c decreases very slowly and J_o increases in much faster pace.” Ex. 1007 at 249.

145. Gan provided further analysis of the experimental results in this Table 1, below. These results show that the higher the temperature of the second-step anneal and the longer its duration the worse the device works.

Table 1: The effect of the second-step anneal on J_o and ρ_c .

	N-type		P-type	
	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$	$J_{o,e} (\times 10^{-14} \text{ A/cm}^2)$	$\rho_c (\mu\Omega\text{-cm}^2)$
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

Ex. 1007, Table 1

146. Gan shows that as the temperature increases above 900°C, ρ_c decreases but J_o increases rather than decreases, such that anything above 900°C results in a rapid decrease in the efficacy of the system. Since Froitzheim teaches that, to achieve dopant drive in for the rear surface of the substrate, “the wafer is treated in an atmosphere that contains oxygen at a temperature of 900 to 1200 degrees centigrade, preferably between **1000 and 1100 degree C**, to generate an oxide layer and to drive in the dopant,” Ex. 1006, ¶42 (emphasis added), combining Froitzheim and Gan either results in annealing at 900°C, which is at the lowest limit of Froitzheim’s teachings for the dopant drive in temperature, or performing the second step anneal (dopant drive in) at temperatures above 900°C that Gan teaches causes “ J_o [to] increase[] in much faster pace,” Ex. 1007, 249, which would lead to poor cell efficiency. Simply put, while Gan teaches best

results are achieved when the second anneal to drive in dopants is at 900°C or

below, Froitzheim teaches that the temperature to drive in dopants is preferably at 1000°C to 1100°C. Consequently, following Froitzheim's teachings nullifies the benefits sought by Gan and following Gan's lower annealing temperature degrades the dopant drive in sought by Froitzheim. *See*, ¶¶107-109, *supra*. The temperatures required by each are incompatible.

147. Rather than being motivated to combine Froitzheim and the Gan reference, a POSITA would have found the substance of the references' teachings to be contradictory and would have rejected the combination. Therefore, CSI's reasonable expectation of success arguments fail not only on the merits because they are contradicted by teachings in the art, but also are unsupported by expert testimony.

148. I note that Gan teaches performing the second step anneal for dopant drive in at temperatures of 900° or below, *see*, ¶137, *supra*, and Froitzheim teaches "a temperature of 900 to 1200 degrees centigrade, preferably between 1000 and 1100 degree C, to generate an oxide layer and to drive in the dopant," Ex. 1006, ¶42. These teachings admittedly overlap at a single temperature of exactly 900°C. However, from the perspective of a POSITA, the teachings of Gan and Froitzheim will be viewed as being incompatible. Froitzheim says that it may be possible to drive in the dopants at 900°C, but it is preferable to use a much higher temperature, i.e., 1000°C to 1100°C, whereas Gan teaches that acceptable J_o and ρ_c values may

occur at 900°C, but poor results for J_o occur higher temperatures. *See*, ¶137, *supra*.

149. To make an analogy, it is like a driver approaching a fork in the road and having two maps: one map instructs to turn left not right (high temperature drive-in) and the other map instructs the driver to turn right not left (low temperature drive-in). It would be obvious to the driver that these instructions were incompatible.

150. Considering Froitzheim and Gan as a whole a POSITA would readily understand the incompatibility in the teachings of Froitzheim and Gan with regard to dopant drive in temperatures and would not have modified Froitzheim in view of Gan as proposed by Petitioner and would not have had a reasonable expectation of success if such combination were pursued.

C. Gan Thesis (Ex. 2003)

151. The Gan Thesis provides a more comprehensive review of the experiments and methodologies described in Gan (Ex. 1007), *see, e.g.*, Ex. 2003, 89-125 (70-106 in original) (Chapter 5), and provides significantly more details about the theory, experimental results, and conclusions set forth in Gan (Ex. 1007).

152. I also understand that the Gan Thesis was published and publicly available on the shelves in the Stanford Library on April 10, 1991, which is prior to the priority date of the '516 patent (as discussed in § IV.A). *See* Ex. 2022, ¶23. I

further understand that it can be assumed that a POSITA would have had knowledge of the information in the Gan Thesis before that priority date. It is my understanding that a librarian expert confirmed public availability. *Id.*

153. The Gan Thesis discusses the findings in Kwark. *Compare* Ex. 2003, Fig. 3.6 with Ex. 1008, Fig. 4. I note that the two figures are identical:

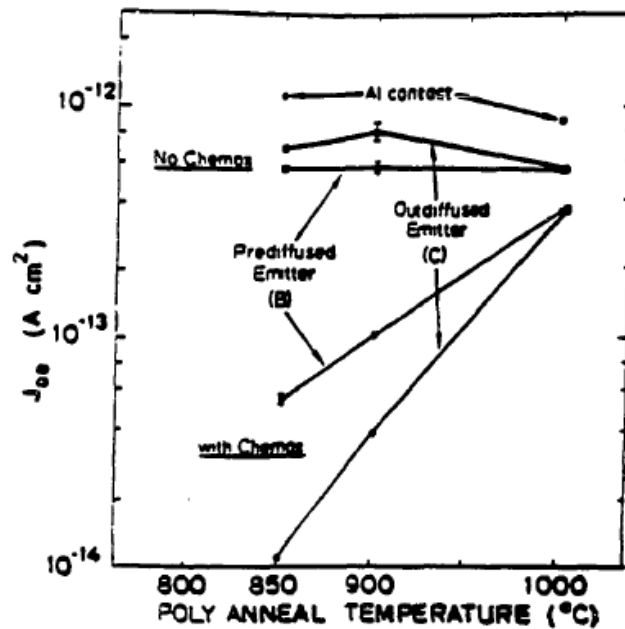
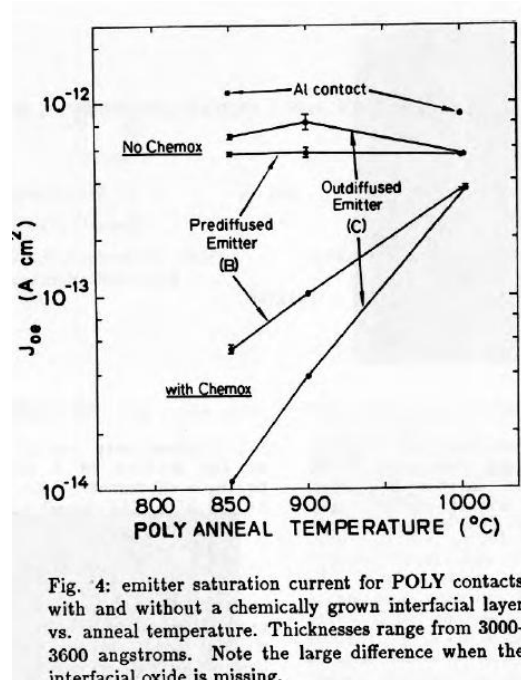


Figure 3.6: J_{oe} for n-type polysilicon emitters with and without a chemically grown interfacial oxide.

Ex. 2003, Fig 3.6.



Ex. 1008, Fig 4.

154. The Gan Thesis states:

[T]he very low J_o of the polysilicon SIS emitter has been demonstrated by other authors [7,10]. Figure 3.6 is the J_o of a polysilicon emitter reported by Kwark [7]. **Note that J_o of 1×10^{-14} A/cm² was observed on the device annealed at 850°C. The rapid increase of J_o upon the anneal temperature is due to breakup of the interfacial oxide which will be discussed later.** A relatively intact interfacial oxide also explains a much lower J_{os} observed on the 900°C-1 hour curve in Figure 3.3.

Ex. 2003, 53 (34 in original) (emphasis added).

155. The Gan Thesis recognized the same phenomenon as in Gan (Ex. 1007). From this data, a POSITA would understand that any benefit of the interfacial oxide is not achievable at the preferred temperatures described for the

anneal step in Froitzheim. Therefore, there would be no reasonable expectation of success from, or a motivation for combining Froitzheim and Kwark as proposed by Petitioner.

156. Further, I note that the Gan Thesis acknowledges inconsistent oxide growth during “ramp-up” and “stand-by” periods, and explains that “it is *possible* that the thin-oxide growth can be improved by performing the oxidation at lower temperatures such that the oxide rate can be controlled more precisely.” Ex. 2003, 131 (112 in original). This was referenced by the Board in its Institution Decision. Paper 13, 13.

157. I further note that the Gan Thesis did recognize there were **possibilities** his theoretical results **could** be demonstrated. For instance, Gan Thesis stated the following. “***Theoretically***, it is **possible** to make a polysilicon SIS emitter with an intact inter-facial oxide having low J_o and “acceptable” ρ_c simultaneously.” Ex. 2003 at 72 (53 in original) (emphasis added). Gan Thesis also stated “**[t]heoretically**, a model was proposed to make the polysilicon emitter with both low J_o ($\sim 3 \times 10^{-14} \text{ A/cm}^2$) and low contact resistance ($\rho_c \leq 1 \times 10^{-5} \Omega\text{-cm}^2$).” *Id.* at 8 (Abstract) (emphasis added). Gan Thesis further stated, “[T]he polysilicon emitter with low J_o and ρ_c **can be made** with a very small fraction of interfacial oxide breakup.” *Id.* at 126 (107 in original)(emphasis added). Further, “[w]ith a few percentages of the interfacial oxide being broken, the ρ_c will be

negligible for the application in concentrator solar cells. Under such a condition, there is a regime in which the J_o will not be affected by the oxide breakup because it is dominated by the recombination at the oxide interface. Thus it is **possible** for polysilicon SIS emitter to have both low J_o and ρ_c .” *Id.* at 88 (69 in original) (emphasis added). Stepping back, however, a POSITA would recognize Gan Thesis’s musings as admittedly just theories and unproven speculation, which lack consistent success in experimental results, demonstrating that the theories fell far short of supporting a reasonable expectation of success. This is particularly true in view of experimental data reproduced in both the Gan Thesis and Kwark that show irreproducible oxide thicknesses, especially when oxide thickness is a critical parameter for acceptable achievement of both low J_o and ρ_c .

158. Further, in my respectful opinion, both the Petitioner and the Board overlooked the other findings of the Gan Thesis that undermine the motivation to combine Froitzheim and Kwark. *See, e.g.*, the above discussion of Figure 3.6 of the Gan Thesis and the identical Figure 4 from Kwark. It is my opinion that in order to manufacture solar cells, one must have confidence that consistent, predictable, and reproducible results will be attained, not just that there is a theoretical possibility that the underlying technology may work occasionally. There is no evidence that either Kwark or Gan that they could repeatedly achieve

the precisely small amount of interfacial oxide breakup that was necessary for concentrator or one sun solar cells to perform reliably.

159. The Gan Thesis stated “[i]n this chapter, we found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that **our thin-oxide growth recipe is not reliable...**” Ex. 2003, 135-136 (116-117 in original) (emphasis added). Gan Thesis was trying to obtain a low J_o of around $\sim 1 \times 10^{-14}$ A/cm², see, e.g., Ex. 2003, 8 (Abstract); *id.* at 22 (3 in original); *id.* at 41 (22 in original), which is understandable because Gan, Kwark, and the Gan Thesis are all trying to solve the same problem, namely a very small and consistent breakup of the interfacial oxide to achieve low J_o . In fact, the Gan Thesis showed that there was no known method for getting the correct oxide thickness reliably to obtain his best results. *Id.* at 138 (119 in original) (“It appears that the oxide breakup depends **critically** on the interfacial oxide thickness. **The thin-oxide growth recipe used in this work was not reliable**; the oxide thickness variations between 15 and 20 Å have been found using the same growth condition. As a result, this contributes to the **fluctuation** of the ρ_c results. **It is then clear that a more reliable way of growing the thin oxide is needed.**”) (emphasis added); *id.* at 126 (107 in original) (“Although a thermally grown interfacial oxide seems **essential** for a polysilicon emitter to have both low J_o and ρ_c , **the breakup process is still**

difficult to control. On several occasions, we have encountered **reproducibility problems.** For example, we find that the ρ_c is quite different between two separate experiments with identical processing conditions. Even worse, **solar cells that were made in this study all suffered high contact resistance. The problem is primarily due to insufficient oxide breakup, and is caused by the fluctuation of the thickness of the interfacial oxide.**)” (emphasis added); *id.* at 129 (110 in original) (“Later in the real solar cell runs, the **situation grew even worse...** Although the $(J_{on} + J_{op})$ measured from those cells are between 8×10^{-14} and $4 \times 10^{-14} A/cm^2$, **the cell efficiency is greatly degraded by such a high emitter resistance.**”); *id.* (“As shown in the figure, **the cell is in fact plagued by two things: the high surface recombination velocity ($S = 58$ cm/sec), and high emitter resistance ($\rho_{cm} + \rho_{cp} = 1 \times 10^{-3} \Omega\text{-cm}^2$).** . . . From the low emitter recombination and high emitter resistance, **it is clear that the interfacial oxide did not break as expected.**”) (emphasis added); *id.* at 130 (111 in original) (“Although these results can be attributed to many other reasons, the following experiment shows that **the effect of the oxide thickness cannot be ignored. This, combined with the non-reliable oxide-growth recipe gives rise to the mishap of our solar-cell runs.**”) (emphasis added); *id.* at 133 (114 in original) (“It becomes clear that the wide fluctuation of our results is mainly due to the poor control over the oxide thickness.”); *id.* at 133-136 (114-117 in original) (“[W]e found that a

consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that **our thin-oxide recipe is not reliable.**”); *id.* at 75 (56 in original) (“With a window so narrow, it is not possible to have good control over the characteristics of a polysilicon SIS emitter.”). One thing is clear based on a thorough reading of the Gan Thesis. He thought that one day it might be possible to achieve his best results, as well as those in his presentation and in Kwark, such that they could be used in one sun solar cells, but Gan and Kwark were a long way away from producing the repeatable results necessary to accomplish this.

160. Figure 4 of Kwark (figure 3.6 of the Gan Thesis) shows that the polysilicon with Chemox shows a rapid degrading of the oxide layer at temperatures over 850 degrees as shown by the increase in J_o . Further, Froitzheim suggests that in order to dope its silicon layer and create an oxide layer “the wafer is treated in an atmosphere that contains oxygen at a temperature of 900 to 1200 degree centigrade, preferably between 1000 and 1100 degree C, to generate an oxide layer and to drive in the dopant.” Ex. 1006, ¶42. The temperature ranges exceed the temperatures Gan and Kwark both recognized as the maximum temperatures possible before a rapid loss of effectiveness occurred.

161. Simply, the Gan Thesis established that the processes found in the Gan reference and Kwark would not achieve good results consistently or reliably.

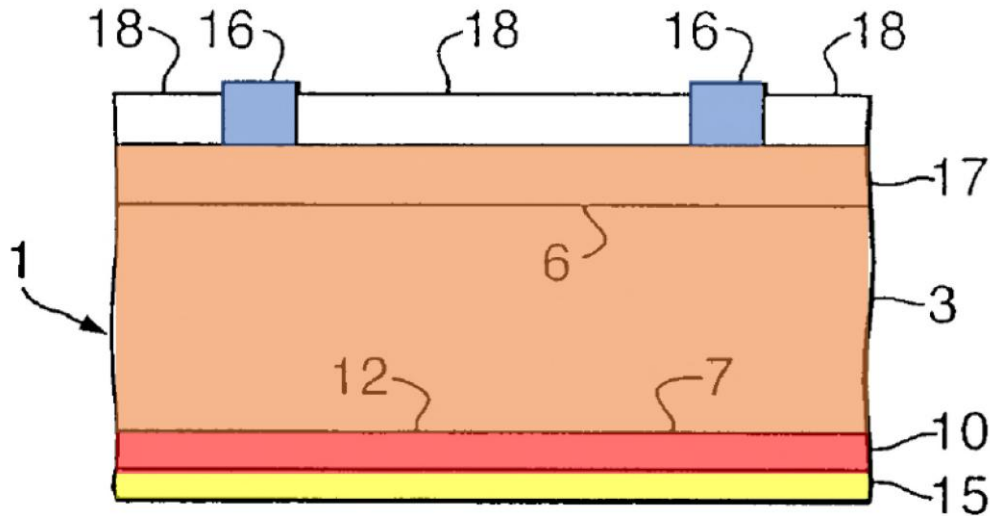
Especially at the temperatures used by Froitzheim which are incompatible with their maximum temperatures. In my opinion, a POSITA would not have had a reasonable expectation of success with the proposed Froitzheim-Gan and Froitzheim-Kwark combinations, and therefore would not be motivated to combine these references.

D. Kwark (Ex. 1008)

162. I have reviewed Kwark et al. “*SIPOS Heterojunction Contacts to Silicon*,” International Electron Devices Meeting (1984): 742-745 (“Kwark”, Ex. 1008). Like Gan, Kwark does not concern a commercial embodiment of a solar cell, but focuses on the results of laboratory experiments on test structures relating to possible ways to increase the efficiency of a solar cell. As discussed below, some of these experiments failed and others identified developments that Kwark considered should be explored further.

163. Contrary to CSI’s claim, Kwark does not teach or suggest that “modify[ing] Froitzheim’s emitter [(i.e., a diffused in-substrate emitter)] to be a polysilicon emitter with an oxide layer” “would be an improvement.” Petition, 60 (citing Ex. 1003, ¶189). In Froitzheim, the “in-substrate emitters” are the area 10 in which P-dopants (boron) are diffused into the back side 7 of the substrate 3 and the area 17 at the front side 6 of the substrate 3 in which N-type dopants

(phosphorous) are diffused. Ex. 1006, ¶¶25, 41 (disclosing boron diffusion); *id.* at ¶¶24, 44 (disclosing phosphorus diffusion).



Petition, 21 (citing Ex. 1006, ¶¶24) (annotations in Petition).

164. To be clear, Froitzheim makes no reference to polysilicon emitters and Kwark does not mention in-substrate emitters at all, never mind suggesting improvements thereto. CSI incorrectly attributes the “potential improvements” and “good results” that Kwark found for SIPOS emitter contacts to a polysilicon emitter. *Compare* Petition, 7 (citing Ex. 1008, 742) (“Incorporation of [SIPOS] films into the emitter structure of an NPN bipolar transistor had been found to reduce the emitter saturation current fifty fold; this translates into potential improvements of energy conversion for solar cells”) *with* Ex. 1008, 742 (“That the γ films [(aka $\gamma=0$ SIPOS contacts)] produced such good results was surprising

since POLY films of comparable thickness should yield a J_{oe} an order of magnitude larger.”).

165. In particular, Petitioner argues that Kwark showed that in the “SIPOS contact structure[,] . . . the increase in J_{oe} at higher temperature is not as severe as for the devices in Fig. 4,” which shows the polysilicon emitter. Petition, 60-61; *but see* Ex. 1007, 743; *see also id.* at Figs. 4, 6 (below). However, in both cases, J_o values increase to unacceptably high levels for anneal temperatures above 900°C.

).

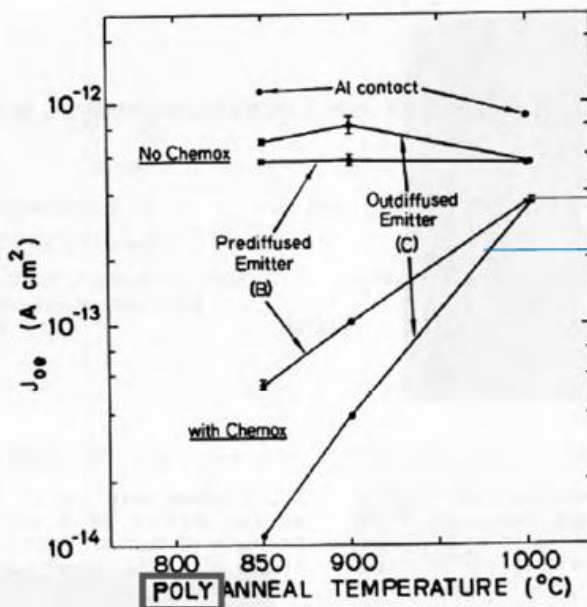


Fig. 4: emitter saturation current for POLY contacts with and without a chemically grown interfacial layer vs. anneal temperature. Thicknesses range from 3000-3600 angstroms. Note the large difference when the interfacial oxide is missing.

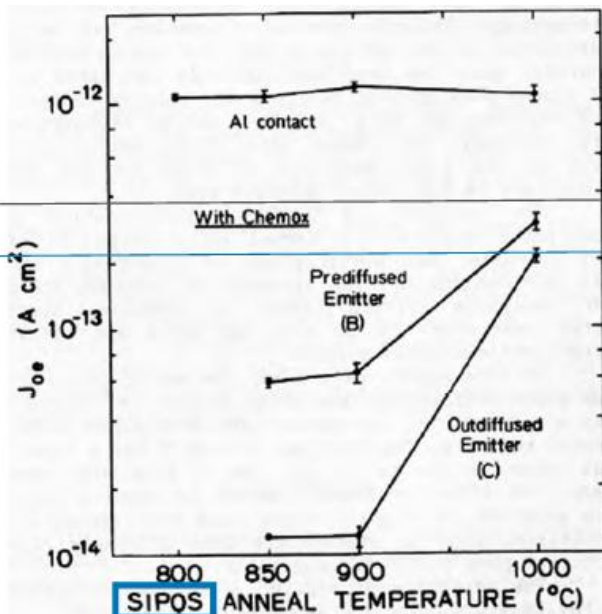
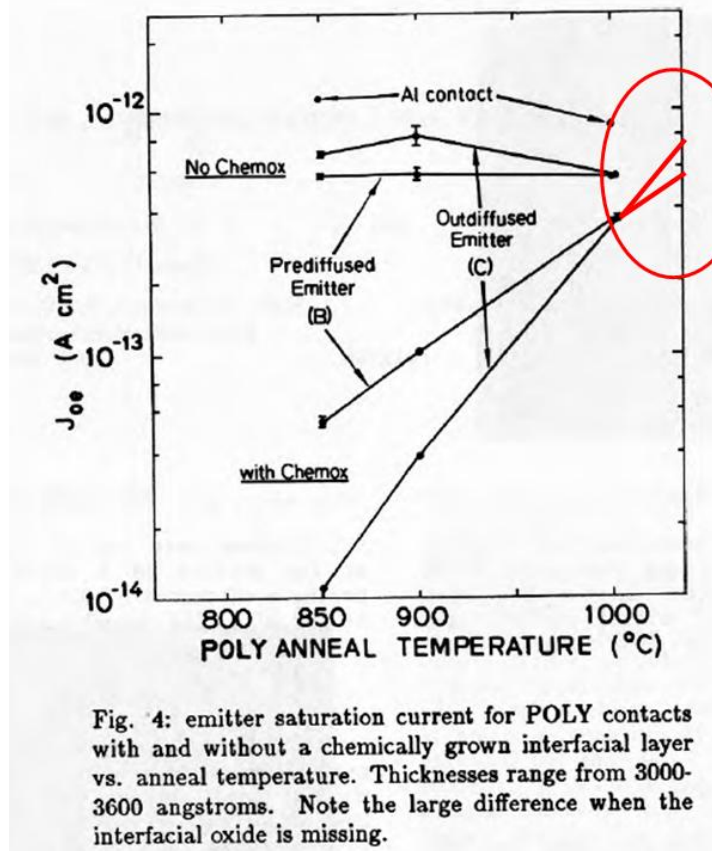


Fig. 6: emitter saturation current vs. anneal temperature for SIPOS contacts with a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

Ex. 1008, Figs. 4, 6 (annotated).

166. In other words, Petitioner posits that Kwark recognized that polysilicon emitters with a chemical oxide (“Chemox”) rapidly lose performance in saturation current density after high temperature anneal steps above 850°C whereas the SIPOS emitters are more resilient, but still lose their ability to passivate the contacts above 900°C.

167. However, a POSITA would have understood from Kwark that the Chemox layer works far better when subject to low temperature anneals, 900°C or below. Ex. 1008, 742 (“In fact for devices annealed at 900°C/13 min, there is very little dependence on γ as seen in Fig. 2, although increasing the anneal temperature to 1000°C adversely affected J_{oe} .”), *id.*, 743 (“Fig. 4 displays the resulting J_{oe} as a function of annealing temperature for emitter B which has a Gaussian (3×10^{19} surface concentration, 1 micron depth into 5×10^{16} background) emitter diffused prior to the POLY deposition and emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction”), *id.* (“To this is added a component due to outdiffusion from the heavily doped POLY which becomes increasingly significant for annealing temperatures above 900°. . . At 1000° this outdiffusion is **severe** enough to dominate the J_{oe} which accounted for the lack of difference between emitters B and C.”) (emphasis added).



Ex. 1008, Fig. 4 (annotated)

168. A POSITA would also have known that Froitzheim teaches “the wafer is treated in an atmosphere that contains oxygen at a temperature of 900 to 1200 degrees centigrade, preferably between 1000 and 1100 degree C, to generate an oxide layer and to drive in the dopant.” Ex. 1006, ¶42. Petitioner posits applying the drive in process of Froitzheim, i.e., preferably at 1000°C and 1100°C. But like Gan, Kwark’s data show that such high temperatures would negate the alleged benefits attributed to Kwark’s use of a low temperature for driving in the dopants. As can be seen above in red, when the emitter lines are extended into the

temperature ranges disclosed as preferable in Froitzheim, the alleged benefits from the use of Chemox are lost.

169. Convincingly, the Gan Thesis, discussed above, reports on test results when using Chemox, and specifically considers Kwark's Fig. 4 analysis. *Compare* Ex. 1008, Fig. 4 *with* Ex. 2003, Fig. 3.6. As discussed above, the Gan Thesis demonstrates that the results suggested by Kwark are not consistently reproducible.

170. A POSITA would not have chosen to modify Froitzheim by adopting the Chemox layer and polysilicon layer disclosed by Kwark and driving in the dopants at the temperatures suggested by Froitzheim, 900°C to 1200°C with 1000°C to 1100°C being preferred. A POSITA would have been further deterred from that combination by the poor results reported in the Gan Thesis from annealing within the temperature range taught in Froitzheim for dopant drive in.

E. Borden (Ex. 1009)

171. PCT Patent Publication WO2009/094578 ("Borden"), published in 2009, is directed to improving HIT cells (Heterojunction with Intrinsic Thin layer cells) by providing it with "a controlled interface [] through insertion of a thin tunnel oxide." Ex. 1009, Abstract (57). Borden-575 claims priority to U.S. Patent Application No. 61/023,342 filed on January 24, 2008. *Id.* at Cover (30).

172. Borden distinguishes HIT cells from polysilicon emitter cells:
“[Polysilicon emitter solar cells] do not provide the heterojunction and its benefit of a higher cell voltage due to the higher bandgap of a-Si.” Ex. 1009, ¶16.

F. Foglietti (Ex. 1014)

173. U.S. Patent Publication US 2002/0142500 (“Foglietti”), published in 2002, relates to a “method of forming an interfacial oxide in a bipolar transistor.” Ex. 1014, Abstract.

174. Foglietti teaches that in NPN bipolar transistors using polysilicon emitter on a monocrystalline silicon substrate, an interfacial oxide sometimes forms at the interface of the two. Ex. 1014, [0002]. Specifically, Foglietti states:

It is well known in the art that in NPN bipolar transistors where polycrystalline silicon (polysilicon) is used as the emitter contact to a monocrystalline silicon substrate, a thin film sometimes is formed at the interface between the polysilicon and the silicon substrate, usually in the form of a thin oxide layer. This thin oxide layer can affect substantially the operation of the transistor and impact its current gain. Such a film is typically called an interfacial oxide.

Ex. 1014, ¶2.

175. Foglietti also teaches that the interfacial oxide “tends to have a beneficial impact on the gain of the bipolar transistor.” Ex. 1014, ¶3. Specifically:

[T]he gain of the transistor (often called the “beta” (β)) is defined as a ratio between the collector current I_C and the base current I_B ($\beta = I_C/I_B$).

Therefore, in order to obtain a high transistor gain, a device designer

wants to devise ways in which the collector current I_C may be increased, or the base current I_B may be decreased, or both. The interfacial oxide has been found to exhibit an advantageous property that its resistance is a function of the type of carrier within the transistor. That is, the interfacial oxide is generally less resistive with respect to majority carriers (electrons) moving from the emitter region of the transistor into the base region than minority carriers (holes) moving from the base region into the emitter region. This phenomenon is due to the tunneling probability of electrons being greater than the tunneling probability of holes.

Ex. 1014, ¶3.

176. In addition, Foglietti discloses the following functions of an interfacial oxide:

[E]lectrons 30, the majority carrier in an NPN transistor, can tunnel through the interfacial oxide 22 from the emitter 20 to the base 14, and contribute to the collector current I_C .

Conversely. . . the interfacial oxide 22 blocks holes 32 from passing therethrough from the base 14 to the emitter 20, thus working to minimize the base current I_B . Therefore the interfacial oxide 22 tends to allow the collector current to be maintained while reducing the base current associated therewith, thereby improving the transistor gain.

Thus the interfacial oxide 22, under appropriate circumstances, may be modeled as a selective diode. . . and designated at reference numeral 34, wherein the electrons 30 see a forward biased, conductive path, and the holes 32 see a reverse-biased, non-conductive path.

Ex. 1014, ¶¶4-5.

177. Foglietti teaches that the interfacial oxide must have certain properties to perform the above functions. For example, the interfacial oxide cannot be too thick or too thin:

The improvement in transistor gain cited above, however, is substantially dependent upon various properties of the interfacial oxide. For example, for interfacial oxides which are too thick, the number of electrons which can tunnel therethrough from the emitter into the base is reduced substantially, thereby reducing disadvantageously the collector current I_C . Likewise, for interfacial oxides which are too thin, an insufficient barrier exists to block the hole current, thereby resulting disadvantageously in an increased base current which reduces transistor gain.

Ex. 1014, ¶6.

178. The interfacial oxide must also maintain integrity:

In addition to the thickness of the interfacial oxide being an important characteristic, the oxide integrity also may play a role in device performance. For example, since the interfacial oxide is subject to various types of subsequent thermal processing (e.g., subsequent poly CVD processing, metal deposition, anneal steps, etc.), the interfacial oxide may lose its integrity, that is, the oxide may exhibit non-uniform characteristics spatially thereacross which in some cases may negatively impact the transistor performance. For example, if the interfacial oxide is fractured or becomes discontinuous, resulting in oxide islands, such fractures will be random and not

repeatable from device to device; consequently, such fracturing causes unreliable transistor gain performance.

Similarly, oxide re-agglomeration may cause a subsequently formed polysilicon emitter to directly contact the underlying single crystal base region which may result in crystal re-orientation of portions of the poly. An example of such epitaxial realignment is illustrated in prior art FIGS. 4 *a* and 4 *b*, respectively. As illustrated in FIG. 4*a*, when a uniform, stable oxide interface separates a polysilicon layer having various grain boundaries associated therewith from an underlying single crystal lattice, no realignment takes place. As illustrated in prior art FIG. 4*b*, however, if the oxide interface exhibits poor integrity, the underlying single crystal lattice may cause a partial realignment of the polysilicon grains. Such epitaxial realignment of the polysilicon grains may disadvantageously increase hole current by increasing hole recombination efficiency, thereby increasing the base current, and decreasing the transistor gain. Furthermore, such epitaxial realignment of polysilicon grains will occur non-uniformly and unpredictably; therefore even if the decrease in gain were acceptable, such degradation would be variable and cause reduced repeatability in transistor performance from device to device.

Ex. 1014, ¶¶7-9.

XII. THE PETITION HAS NOT SHOWN ANY CHALLENGED CLAIM IS UNPATENTABLE

179. In my opinion, the Petition fails to show that any of the claims in the '516 patent are unpatentable. Some of the errors in the Petition follow.

A. Claims 9-11 of the '516 Patent Are Patentable Under Meier, Okayasu, Borden, and Jordan (Ground 1)

180. CSI's proposed Meier-Okayasu Froitzheim-Borden combination uses polysilicon emitters, but Borden's purported benefits are directed to HIT cells, not polysilicon emitter cells. Petition, 23 (referencing Okayasu's "method of depositing doped polysilicon layers"); *id.* at 24 (referencing Borden's tunnel oxides). Borden's Abstract, when read in full, makes this clear:

Benefits of the invention include that it provides a controlled interface for the HIT cell through insertion of a thin tunnel oxide. Moreover, the tunnel oxide prevents epitaxial growth of amorphous silicon, allowing it to remain amorphous for the optimum band structure. Still further, it provides a layer to protect the surface from plasma damage during deposition of the a-Si layer.

Ex. 1009, Abstract (emphasis added).

181. Amorphous silicon (also referenced as "a-Si layer" in Borden) is a feature of "[a] typical HIT type solar cell." Ex. 1009, ¶4; *see also id.* at Fig. 1B. Borden also expressly distinguishes HIT cells from polysilicon emitter cells "[Polysilicon emitter solar cells] do not provide the heterojunction and its benefit of a higher cell voltage due to the higher bandgap of a-Si." *Id.* at ¶16.

182. In other words, Borden’s purported benefit of the thin tunnel oxide is solely related to amorphous silicon, and amorphous silicon is not present in the proposed Meier-Okayasu combination. Thus, a POSITA would not have been motivated to insert Borden’s tunnel oxide layer (unclear whether this is CSI’s proposed “interfacial oxide layer”) on the proposed Meier-Okayasu combination because Borden’s purported benefits would not have been applicable.

B. Claims 9-11 of the ’516 Patent Are Patentable Under Meier, Okayasu, Foglietti, Gan, and Jordan (Ground 2)

183. A POSITA would not have been motivated to combine Foglietti and Gan because they pursue opposite goals.

184. Foglietti’s goal is to form “an interfacial oxide with good control which maintains its integrity during subsequent processing.” Ex. 1014, ¶10. Specifically, Foglietti teaches that, “under appropriate circumstances,” an interfacial oxide allows majority carriers (electrons) to tunnel through, but blocks minority carriers (holes). *Id.* at ¶¶3-5. These appropriate circumstances include the interfacial oxide being thin enough to permit majority carriers to tunnel through, but not too thin so as to form an insufficient barrier, *id.* at ¶¶4, 6, and the interfacial oxide maintaining its integrity and not become “fractured” or “discontinuous,” *id.* at ¶3.

185. Gan’s goal, on the other hand, is to break up the interfacial oxide. According to Gan, contact resistance is high “[w]hen the interfacial oxide is intact

[and] tunneling is the only process available for the majority carriers to pass through the interfacial oxide.” Ex. 1007, 249. Striking a balance between low recombination and low resistance, Gan uses annealing to break the interfacial oxide “by a very small fracture.” *Id.* at Abstract. According to Gan, this break-up creates “additional highly conductive channels” “between the polysilicon and the substrate in the broken regions.” *Id.* at 249.

186. In other words, Foglietti teaches maintaining an interfacial oxide’s integrity to enable majority carrier tunneling, but Gan discloses breaking up the interfacial oxide to create different processes for the majority carriers to pass through. Thus, a POSITA would not have been motivated to combine the two incompatible references.

C. Claims 9-12 of the ’516 Patent Are Patentable Under Froitzheim and Gan (Ground 3)

187. Ground 3 of the Petition relies on Froitzheim in combination with Gan. Petition at 4. Ground 3 states that claims 9-12 are obvious based on Froitzheim and Gan. *Id.* The only independent claim at issue in this matter is claims 9. Therefore, if the combination of Froitzheim and Gan does not invalidate independent claim 9, then claims 10-12 are also not unpatentable.

188. In my opinion, a POSITA would not have been motivated to combine Froitzheim and Gan for at least two reasons. First, as recognized by both Gan and Kwark, Froitzheim’s temperature for dopant drive in would have led to

unacceptably high recombination in such combination, thereby negating Gan's purported benefit. Second, a POSITA would not have undertaken the combination because of failure of both Gan and Kwarik to teach or suggest a reliable, effective, and consistent method for growing the interfacial oxide layer at the precise thickness necessary between the crystalline substrate and the doped polysilicon layer formed on the back side of the substrate.

1. *Froitzheim's Anneal Temperature on Gan's Oxide Layer Would Have Led to High Resistivity and High Recombination*

As I discussed above in § XI.B, Gan shows the J_o increases too rapidly as the temperature increases above 900 degrees Celsius, although these higher temperatures are needed to achieve acceptably low ρ_c values. Anything above 900 degrees Celsius, however, produces a rapid increase in J_o , which is disastrous for solar cells.

189. Gan identifies polysilicon emitters with $J_o \leq 5 \times 10^{-14}$ A/cm²" and $\rho_c \sim 1 \times 10^{-5}$ Ω/cm² to be "quite useful for silicon concentrator solar cells." Ex.

1007, 249. CSI bases its motivation to combine on Gan's usefulness. Petition, 43 (citing Ex. 1007, 249). But the values of this useful polysilicon emitter "indicate that the interfacial oxide is only broken by a very small fraction." Ex. 1007, Abstract; *see also id.* at 248 ("[B]ecause the dominant recombination is likely at the oxide interface, it implies that the oxide must only be broken by very a small [*sic*] fraction.").

190. To achieve the desired values for J_o and ρ_c , Gan's device undergoes two anneals: a first-step anneal at 1050°C following polysilicon deposition, and a second-step anneal to drive-in dopants. *See, e.g.*, Ex. 1007, 246 (steps 4, 10). During the second-step anneal, Gan observed that " J_o increases with the temperature and time of the second-step anneal." Ex. 1007, 248.

191. Gan's measurements show that when the second-step anneal is conducted at higher than 900° C that a P-type polysilicon emitter incurs suboptimal ρ_c and J_o values. For example, at 900°C, both N and P-type polysilicon emitters have a ρ_c of 18 $\mu\Omega\text{-cm}^2$ (or $1.8 \times 10^{-5} \Omega/\text{cm}^2$), which is 80% higher than the value of $\rho_c \sim 1 \times 10^{-5} \Omega/\text{cm}^2$ that Gan deems "useful." Ex. 1007, 248 (Table 1).

192. To the extent CSI argues that Gan discloses its findings to be "useful for silicon solar cells" when ρ_c is lower than $5 \times 10^{-5} \Omega/\text{cm}^2$, Ex. 1007 at 249, Gan specifies at that ρ_c , "the potential drop across the contact is negligible as long as the current density is less than 100 A/cm²," *id.* CSI does not allege that its proposed Froitzheim-Gan combination would feature Gan's specified current density. Thus, in my opinion, a POSITA would not have found that ρ_c value to be relevant.

193. As shown below, annealing at 1000°C, even for 30 minutes, results in a value of J_o of $5 \times 10^{-14} \text{ A/cm}^2$ for N-type and $8 \times 10^{-14} \text{ A/cm}^2$ for P-type, both of which are higher than what Gan used in his simulation as "useful" for

concentrator cells of 2×10^{-14} A/cm² for N-type and 3.5×10^{-14} A/cm² for P-type.”

Table 1: The effect of the second-step anneal on $J_{o,e}$ and ρ_c .

	N-type		P-type	
	$J_{o,e}$ ($\times 10^{-14}$ A/cm ²)	ρ_c ($\mu\Omega\text{-cm}^2$)	$J_{o,e}$ ($\times 10^{-14}$ A/cm ²)	ρ_c ($\mu\Omega\text{-cm}^2$)
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

Ex. 1007, 248 (Table 1) (annotated).

194. The values of Gan’s P-type polysilicon emitter are relevant because CSI proposes replacing “Froitzheim’s rear P-type diffused *in-substrate* emitter with a rear P-type deposited *polysilicon* emitter plus the beneficial interfacial oxide layer.” Petition, 31 (emphasis in original).

195. CSI’s proposed combination adopts the dopant drive in anneal of Froitzheim and, accordingly, would undergo a second-step anneal to drive in the dopants at temperatures of least 900°C, and preferably 1000°C to 1100°C.

196. Froitzheim teaches “the wafer is treated in an atmosphere that contains oxygen at a temperature of 900 to 1200 degrees centigrade, preferably between **1000 and 1100** degree C, to generate an oxide layer and to drive in the dopant.” Ex. 1006, ¶42 (emphasis added). This step replaces Gan’s second-step anneal. Ex. 1007, 248 (“The first-step anneal, which serves to break the oxide, was performed at higher temperature than that for the second-step anneal which aims for the dopant drive-in.”).

197. Thus, at the lowest anneal temperature Froitzheim discloses, 900°C, the resulting Froitzheim-Gan combination would yield a value of ρ_c that is higher than what Gan finds “useful.” Further, at Froitzheim’s preferred temperatures of 1000°C to 1100°C the resulting Froitzheim-Gan combination would yield a value of J_o that is much higher than what Gan finds “useful.”

198. Further, the Gan Thesis discloses that a desirable value for J_o should be even lower: “cell efficiency . . . is hardly affected by the emitter recombination when J_o is below 1×10^{-14} A/cm²; however, it falls off rapidly as the J_o increases over 1×10^{-14} A/cm².” Ex. 2003, 3. He was never able to achieve J_o values this low.

199. At a minimum, a POSITA would have found no benefit in combining Froitzheim and Gan, and given Froitzheim’s preferred much higher drive-in temperature, would have rejected the combination. Thus, the Petition fails to establish a motivation to combine the references. Indeed, I believe this incompatibility in the drive in temperatures would be seen by a POSITA as teaching away from the proposed combination.

200. A POSITA that took the oxide and polysilicon (emitter in claim 9) components proposed by Gan and added it to the silicon wafer of Froitzheim and attempted to anneal the dopants into the Gan polysilicon at the temperatures suggested by Froitzheim would have a device that behaves no better, and likely

worse than, the system originally disclosed by Froitzheim. Gan was trying to identify a reliable balance between the recipe for forming a functional interfacial oxide and the processing temperature and was unsuccessful in doing so in a reproducible manner. A POSITA would not have adopted the extra steps required by Gan only to jeopardize reliability while yielding a device that would not outperform the original Froitzheim device.

2. *A POSITA Would Not Have Been Able to Consistently Grow Gan's Oxide Layer*

201. A POSITA would also not have any expectation of success in combining the polysilicon and interfacial oxide layer of Gan with the silicon wafer disclosed in Froitzheim because Gan proposes taking a standard tunnel oxide layer and then breaking it ever so slightly with critical precision in a reproducible manner. Gan did not reliably accomplish this goal and verified that failure in the Gan Thesis. Gan found it difficult to define a process to create and control a suitable tunnel oxide layer and, as noted in his thesis, documents frequent failures in the effort to do so.

202. The Gan Thesis stated “[i]n this chapter, we found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that **our thin-oxide growth recipe is not reliable**...In order to have **predictable** results, it appears that a precise control of the oxide thickness is necessary.” Ex. 2003, 135-136 (116-117

in original) (emphasis added). A POSITA would have concluded that Gan never achieved that “precise control.”

203. Gan Thesis was trying to get a low J_o of around $\sim 1 \times 10^{-14}$ A/cm². See, e.g., Ex. 2003, 8 (Abstract); *id.* at 22 (3 in original); *id.* at 41 (22 in original). This is understandable because Gan, Kwark, and the Gan Thesis are all striving to solve the same problem, namely a very small and consistent breakup of the interfacial oxide to achieve low J_o . In fact, Gan Thesis showed that there was no known method for achieving a precise oxide thickness reliably to obtain the sought after results. *Id.* at 138 (119 in original) (“It appears that the oxide breakup depends **critically** on the interfacial oxide thickness. **The thin-oxide growth recipe used in this work was not reliable**; the oxide thickness between 15 and 20 Å have been found with the same growth condition. As a result, this contributes to the **fluctuation** of the ρ_c results. **It is then clear that a more reliable way of growing the thin oxide is needed.**”) (emphasis added); *id.* at 126 (107 in original) (“Although a thermally grown interfacial oxide seems **essential** for a polysilicon emitter to have both low J_o and ρ_c , **the breakup process is still difficult to control**. On several occasions, we have encountered **reproducibility problems**. For example, we find that the ρ_c is quite different between two separate experiments **with identical processing conditions**. Even worse, **solar cells that were made in this study all suffered high contact resistance. The problem is**

primarily due to insufficient oxide breakup, and is caused by the fluctuation of the thickness of the interfacial oxide.”) (emphasis added); *id.* at 129 (110 in original) (“Later in the real solar cell runs, the **situation grew even worse**...Although the $(J_{on} + J_{op})$ measured from those cells are between 8×10^{-14} and 4×10^{-14} A/cm², **the cell efficiency is greatly degraded by such a high emitter resistance.**”); *id.* (“As shown in the figure, **the cell is in fact plagued by two things: the high surface recombination velocity ($S = 58$ cm/sec), and high emitter resistance ($\rho_{cm} + \rho_{cp} = 1 \times 10^{-3} \Omega\text{-cm}^2$).** . . . From the low emitter recombination and high emitter resistance, **it is clear that the interfacial oxide did not break as expected.**”) (emphasis added); *id.* at 130 (111 in original) (“Although these results can be attributed to many other reasons, the following experiment shows that **the effect of the oxide thickness cannot be ignored. This, combined with the non-reliable oxide-growth recipe gives rise to the mishap of our solar-cell runs.**”) (emphasis added); *id.* at 133 (114 in original) (“It becomes clear that the wide fluctuation of our results is mainly due to the poor control over the oxide thickness.”); *id.* at 133-136 (114-17 in original) (“[W]e found that a consistent result of ρ_c is difficult to reproduce for the polysilicon emitter with a thermally grown interfacial oxide. This is mainly attributed to the fact that **our thin-oxide recipe is not reliable.**”); *id.* at 75 (56 in original) (“With a window so

narrow, it is not possible to have good control over the characteristics of a polysilicon SIS emitter.”).

204. One thing is clear based on a thorough reading of the Gan Thesis. Gan thought that one day it might be possible to achieve his elusive results, as well as those in his presentation and in Kwark, such that they could be used in one sun solar cells, but clearly the path to those results was long and undefined.

205. A POSITA would read the Gan Thesis and determined that the experimental results discussed in the Gan reference were very unreliable, created “mishap[s],” had reproducibility problems, and the good results were only theoretical.

3. *A POSITA Would Not Have Been Motivated to Combine Froitzheim and Gan (Grounds 1 and 2)*

206. Because there is no expectation of success in combining Froitzheim with Gan to produce the claimed solar cell with a substrate, emitter, and oxide layer between the two as required by claim 9, a POSITA would not have been motivated to combine the references.

207. As I explained in § XII.C.1, a POSITA would not be motivated to combine the Gan reference with the Froitzheim reference because any advantages in J_o and ρ_c proposed by Gan would be unattainable as a consequence of the temperature range, including the preferred temperature range, disclosed by Froitzheim.

208. As I explained in § XII.C.2, a POSITA would not be motivated to combine the Gan reference with Froitzheim because the Gan Thesis, which discusses the work described in Gan (Ex. 1007) and tells the POSITA that the oxide layer required in the combination consistently fails, is unreliable, and at best remains a theoretical improvement.

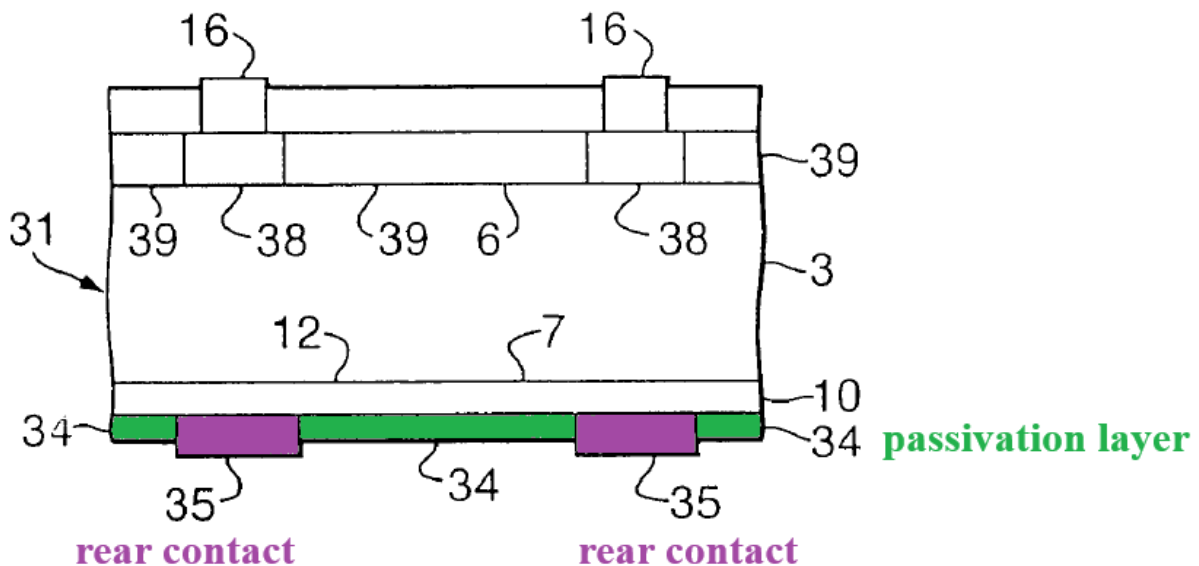
209. Finally, a POSITA would also not be motivated to combine Gan with Froitzheim because Gan is directed to concentrator solar cells. As I explain in ¶¶48-50 above, concentrator cells generate multiple times more free electrons than one sun solar cells requiring concentrator solar cells to have a much lower resistive path from the substrate to the emitter, through the metal contacts and gridlines, than in a one sun solar cell. But as I explain in ¶ 132 above, the high current levels taught in Gan Thesis indicate that the “modeling” referred to by Gan (Ex. 1007) were of silicon concentrator solar cells. Thus, a POSITA would not look to modifying the one sun solar cell manufacturing method of Froitzheim with the teachings of Gan relating to concentrator solar cells.

D. The Proposed Froitzheim-Gan Combination Does not Include a “Second Metal Contact” with “Silver Formed over a Layer of Silicon Dioxide” (Claim 12)

210. The Board should not consider CSI’s proposed Froitzheim-Gan combination under claim 12, which is based on an alternative embodiment of Froitzheim. Petition, 55-56 (citing and illustrating Ex. 1006, Fig. 3). This

alternative embodiment includes an additional passivation layer 34 and rear contacts 35 in a finger structure. Ex. 1006, ¶¶33.

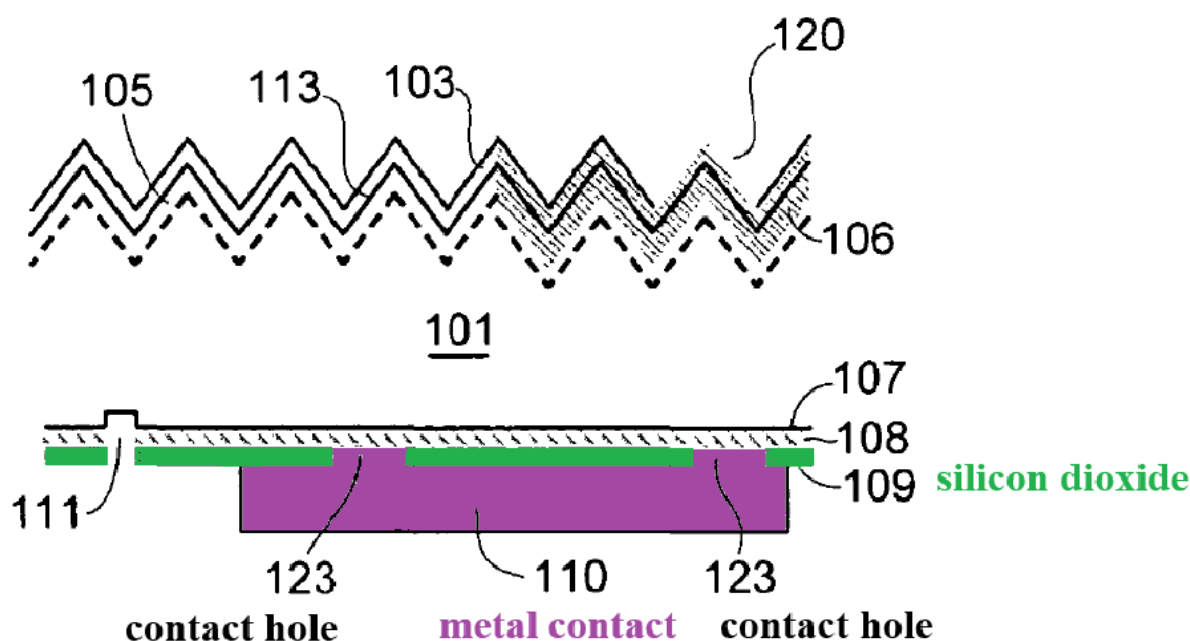
211. Further, CSI improperly equates Froitzheim’s disclosure of its rear contacts 35 forming *after* the passivation layer with the claim 12 limitation of “silver form[ing] over a layer of silicon dioxide.” Petition, 56-57 (citing Ex. 1006, ¶¶19, 33, 50). Froitzheim in fact discloses and illustrates that its passivation layer 34 is arranged *between* the rear contact 35 fingers. Ex. 1006, Fig. 3; *see also id.* at ¶¶33 (“Between the fingers a passivation layer 34 is arranged”). This is achieved by screen printing and firing squeegee paste “in order to make electrical contact with the p region.” *Id.* at [0049]. In the firing process, the squeegee paste pierces the passivation layer to reach the emitter layer 10 to form the electrical contact.



Ex. 1006, Fig. 3 (annotations added).

212. CSI fails to explain how this alternative embodiment would be modified with Gan, or whether a POSITA would have been motivated to perform such modifications. Thus, with regard to claim 12, the Board should not consider CSI's proposed Froitzheim-Gan combination using this alternative embodiment.

213. In contrast, in the '516 patent, the rear metal contact is formed *over* a layer of silicon dioxide because there are metal holes ensuring electrical contact. Specifically, the '516 patent describes that, first, "contact holes 120 and 123 are formed by removing exposed portions of the silicon nitride layer 103 and the silicon dioxide 109 in a contact etch step." Ex. 1001, 5:38-40. Next, "the metal contact 110 is formed *on* the silicon dioxide layer 109 to fill the contact holes 123 and make electrical connection to the polysilicon emitter 108." *Id.* at 5:48-50 (emphasis added).



Ex. 1001, Fig. 4L (annotated).

214. As shown, parts of the metal contact 110 overlap with the silicon dioxide layer 109. This overlap is not present in Froitzheim's Figure 3 or description thereof, and thus, the proposed alternative Froitzheim-Gan combination would not meet the limitation of claim 12.

E. A POSITA Would Not Have Expected a Reasonable Expectation of Success in the Combination of Froitzheim and Kwark (Ground 4)

215. Ground 4 of the Petition relies on Froitzheim in combination with Kwark. Petition, 4. Ground 4 states that claims 9-12 are obvious based on Froitzheim and Kwark. *Id.*

216. First, Kwark clearly teaches the use of a Chemox layer and that a Chemox layer only works if annealing is performed at low temperature. Ex. 1008, 742 ("In fact for devices annealed at 900°C/13 min, there is very little dependence on γ as seen in Fig. 2, although increasing the anneal temperature to 1000°C adversely affected J_{oe} ."), *id.* at 743 ("Fig. 4 displays the resulting J_{oe} as a function of annealing temperature for emitter B which has a Gaussian (3×10^{19} surface concentration, 1 micron depth into 5×10^{16} background) emitter diffused prior to the POLY deposition and emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction"), *id.* ("To this is added a component due to outdiffusion from the heavily doped POLY which becomes

increasingly significant for annealing temperatures above 900°C. This is apparent if one notes that the increase in J_{oe} for emitter B can be accounted for by the J_{oe} of emitter C at the same temperature. At 1000°C this outdiffusion is **severe** enough to dominate the J_{oe} which accounted for the lack of difference between emitters and C.”) (emphasis added).

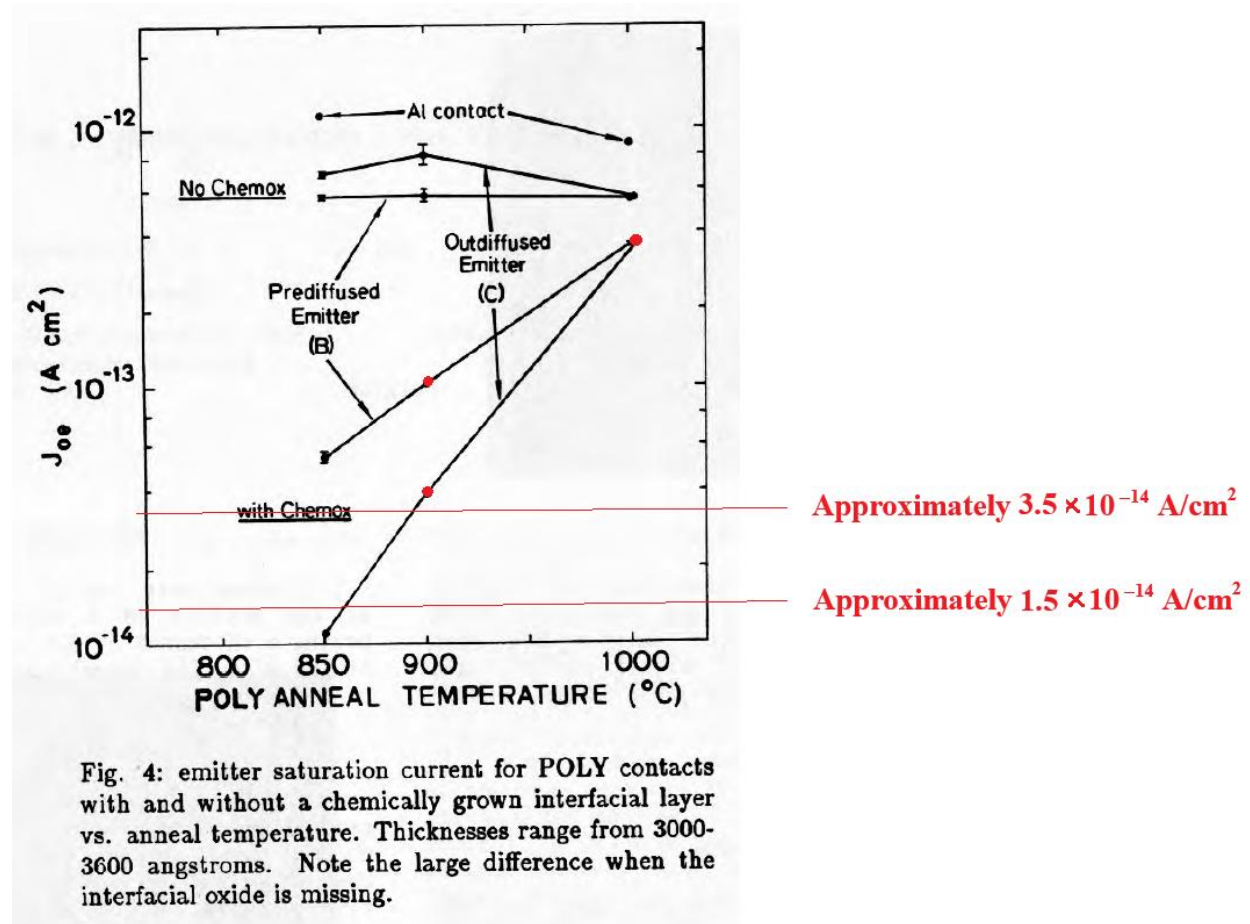
217. However, Froitzheim teaches “the wafer is treated in an atmosphere that contains oxygen at a temperature of 900 to 1200 degrees centigrade, preferably between 1000 and 1100 degree C, to generate an oxide layer and to drive in the dopant.” Ex. 1006, ¶42. In other words, at the temperatures Froitzheim says should be used to drive in the dopants, all of the benefits touted by Kwark would be lost.

218. Like Gan, Kwark examined emitter saturation current, J_{oe} , as a function of annealing temperature. Kwark’s J_{oe} and Gan’s J_o are the same; they both use the unit of current density Amperes per square centimeter. *See, e.g.*, Ex. 1007, Abstract (Gan disclosing “ $J_o \leq 5 \times 10^{-14}$ A/cm²”); Ex. 1008, Abstract (Kwark disclosing “ J_{oe} , values of 2×10^{-14} A/cm²”).

219. Similar to Gan, Kwark disclosed a desirable J_{oe} , value of 2×10^{-14} A/cm². Ex. 1008, Abstract; *see also id.* at 743 (discussing attaining “[e]mitter saturation currents of $1-2 \times 10^{-14}$ A/cm²” for “POLY with Chemox and for both

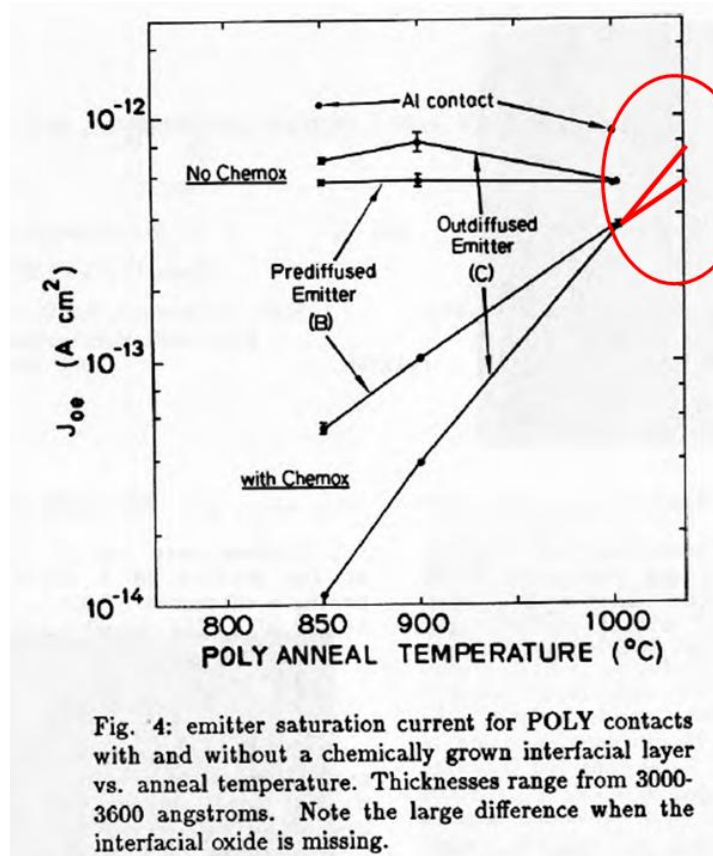
SIPOS contact structures.”). Kwark also discloses “a baseline J_{oe} of 5×10^{-14} A/cm²” for “[p]rediffused’ emitter B.” *Id.*

220. Further, like Gan, Kwark identified the undesirable, higher-than-desired J_{oe} values at anneal temperature of 900 C and above:



Ex. 1008, Fig. 4 (annotated); *see also id.* at 743 (“Fig. 4 displays the resulting J_{oe} as a function of annealing temperature for emitter B.”). Figure 4 of Kwark is relevant because CSI relies on it to argue motivation to combine Froitzheim with both Gan and with Kwark. *See e.g.*, Petition, 59.

221. Further, as can be seen below in red, if the emitter lines are extended into the temperature ranges disclosed as preferable in Froitzheim, all benefits of the Chemox are lost.



Ex. 1008, Fig. 4 (annotated).

222. Therefore, given the rapid breakup of the interfacial oxide layer at temperatures above 850°C, as taught by Kwark, and the much higher temperatures taught as being preferable by Froitzheim, a POSITA would not have a reasonable expectation of success in the combination of Froitzheim and Kwark. *See, e.g.*, ¶199 above. Also, a POSITA would not have chosen to form the interfacial

Chemox oxide layer and polysilicon layer disclosed by Kwark and on the surface

of the silicon substrate of Froitzheim, because Gan and the Gan Thesis both teach poor results would happen after the high anneal temperatures required by Froitzheim.

223. Further, Kwark proposes using Chemox. *See, e.g.*, Ex. 1008, Fig. 4. Chemox is a very crude form of creating silicon dioxide and this may be the reason Kwark had such a difficult time creating a uniform oxide layer and had such increases in J_o if processing temperatures exceeded 850°C. *See, e.g.*, ¶154 above (quoting Ex. 2003, 53 (34 in original)).

224. In fact, the Gan Thesis disparages the use of Chemox. The Gan Thesis tells us “[a]s mentioned previously, a very low J_o can be obtained (see Figure 3.6) for the N-type polysilicon SIS emitter with a chemically grown interfacial oxide. However, the corresponding ρ_c of such a device can be as high as $4 \times 10^{-4} \Omega\text{-cm}^2$ at the doping concentration of $1 \times 10^{20} \text{ cm}^{-3}$, which is the typical doping concentration of the emitter. This is four times higher than the value mentioned in the previous chapter as our goal, and the potential drop across the polysilicon emitter would be **intolerable**.” Ex. 2003, 58 (39 in original) (emphasis added). Therefore, a POSITA would not expect a reasonable expectation of success in using this Chemox layer, and for this reason would not be motivated to combine the Chemox and polysilicon layers of Kwark with Froitzheim.

225. However, most importantly, the Gan Thesis verifies that the results obtained by a Chemox layer as used in Kwark are not reproducible in a consistent manner in addition to disparaging the use of Chemox.

F. A POSITA Would Not Have Been Motivated to Combine Froitzheim and Kwark (Ground 4)

226. For the reasons discussed in the section above, a POSITA would not have a reasonable expectation of success in the Froitzheim and Kwark combination, and therefore, a POSITA would not have a motivation to combine the references.

227. Finally, a POSITA would not be motivated to combine Kwark with Froitzheim because the use of intentionally broken SiO₂ layers would be a significant cause of concern for long-term performance degradation. As noted above, the Gan Thesis points out, reproducibility using Chemox is very difficult. Moreover, like Gan, a POSITA would have seen the incompatibility in temperature ranges for driving in the dopants to indicate that the references, if combined, would yield no benefit over Froitzheim.

G. Claims 9-12 of the '516 Patent Are Patentable Under Froitzheim and Borden (Ground 5)

228. In my opinion, CSI proposes a Froitzheim-Borden combination using an interfacial oxide layer that Borden does not disclose. CSI also fails to show motivation to combine Froitzheim with any of Borden's oxide layers, or that there would be a reasonable expectation of success.

1. CSI Fails to Properly Define the Proposed Froitzheim-Borden Combination

229. In my opinion, CSI failed to properly define the proposed Froitzheim-Borden combination.

230. CSI misrepresents that “[l]ike Gan and Kwark, Borden taught the use of an interfacial oxide layer in between a polysilicon emitter and substrate;” Borden never mentions the term “interfacial oxide” once. Petition, 65. Rather, Borden discloses “forming a masking oxide layer on the front and back of the cell and then patterning holes in the masking oxide,” Ex. 1009, Abstract, and “insertion of a thin tunnel oxide.” *Id.*

231. As I explained in ¶86 above, a masking oxide layer and a thin tunnel oxide are not the same. A masking oxide layer is typically thicker than tunnel oxides, and a masking oxide can be produced by a wet oxidation process whereas an effective tunnel oxide is typically grown in a dry oxidation. CSI's proposed

Froitzheim-Borden combination featuring “interfacial oxide (green) based on Borden” is therefore undefined. Petition, 65, 67 (illustration).

2. *CSI Fails to Show Why a POSITA Would Have Been Motivation to Combine Froitzheim and Borden*

232. The proposed Froitzheim-Borden combination uses polysilicon emitters, but Borden’s purported benefits are not directed to polysilicon emitter cells, but to Heterojunction with Intrinsic Thin-layer (HIT) solar cells, which features amorphous silicon layers on both sides of a substrate. Petition, 65 (proposing a combination with polysilicon emitters); *id.* at 66 (citing Ex. 1009, Abstract) (alleging motivation to combine); *but see* Ex. 1009, ¶4 (disclosing the structure of a “typical HIT type solar cell”). Borden’s Abstract, when read in full, makes this clear:

Benefits of the invention include that it provides a controlled interface for the HIT cell through insertion of a thin tunnel oxide. Moreover, the tunnel oxide prevents epitaxial growth of amorphous silicon, allowing it to remain amorphous for the optimum band structure. Still further, it provides a layer to protect the surface from plasma damage during deposition of the a-Si layer.

Ex. 1009, Abstract (emphasis added).

233. Amorphous silicon (also referenced as “a-Si layer” in Borden) is a feature of “[a] typical HIT type solar cell.” Ex. 1009, ¶4; *see also id.* at Fig. 1B. Borden also expressly distinguishes HIT cells from polysilicon emitter cells

“[Polysilicon emitter solar cells] do not provide the heterojunction and its benefit of a higher cell voltage due to the higher bandgap of a-Si.” Ex. 1009, ¶16.

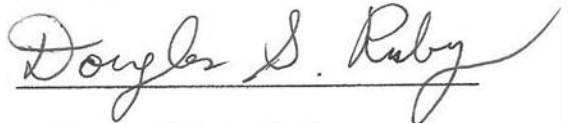
234. In other words, the purported benefit of the thin tunnel oxide is solely related to amorphous silicon, and amorphous silicon is not present in the proposed Froitzheim-Borden combination. Thus, in my opinion, a POSITA would not have been motivated to insert Borden’s tunnel oxide layer (unclear whether this is CSI’s proposed “interfacial oxide layer”) on Froitzheim because Borden’s purported benefits would not have been applicable to the proposed combination.

XIII. CONCLUSION

235. In my opinion, based on my review of the '516 patent, the materials referenced above, and my knowledge of what a POSITA would have known at the time of the invention, the Petition fails to show that any claim is unpatentable.

236. I declare that all statements made herein of my own knowledge are true, and that statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on April 8, 2025 in Holualoa, Hawaii.

A handwritten signature in cursive script, reading "Douglas S. Ruby", is written over a horizontal line.

Douglas Ruby, Ph.D.