PROCEEDINGS OF THE THIRD INTERNATIONAL SYMPOSIUM ON ULTRA LARGE SCALE INTEGRATION SCIENCE AND TECHNOLOGY

ULSI SCIENCE AND TECHNOLOGY / 1991

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SINGLE-WAFER RAPID THERMAL CVD TECHNOLOGY FOR FABRICATION OF MOS AND BIPOLAR DEVICES

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In fabrication of MOS, bipolar and BiCMOS integrated circuits, single-wafer rapid thermal chemical vapor deposition (RTCVD) can provide the foundation for a wide range of processes. In addition, a number of processing steps can be integrated to a central wafer handler to provide an application-specific tool. The applications include MOS gate dielectric, poly-emitter bipolar interface engineering, polysilicon deposition, and single or multi-layers of blanket or selective homo or hetero-epitaxy films. It is increasingly apparent, especially with the advanced generation technology employed for large substrates, that the level of control required can only be achieved when processing sequences are executed in a single-wafer mode under a controlled environment. A combination of low-temperature reduced-pressure wafer cleaning, dielectric engineering and polysilicon deposition will satisfy the requirements of this emerging concept of integrated, environmentally controlled front-end processing for the MOS gate and poly-emitter bipolar applications.

INTRODUCTION

For fabrication of small geometry ICs, reduced thermal budget processing is mandatory to restrict dopant movement for maintaining shallow junctions. Furthermore, for stability reasons, strained layer Si_xGe_{1-x} HBT structures can not be subjected to high-temperature processing [1]. For low-thermal budget processing, RTCVD was introduced to provide an alternative to conventional long-time, slow-response batch furnace technology. In this approach, thermal energy is provided by radiative heating in a cold-wall environment. Due to small thermal mass of the system, rapid changes in wafer temperature, both up and down, is made possible. In parallel, various dry low-temperature wafer cleaning techniques have been developed [2,3,4,5]. The key is to effectively clean the wafer at low temperatures (below 600°C) and to maintain surface cleanliness between various processing steps. Dry-phase, anhydrous HF cleaning at room temperature supplemented by UV/ozone treatment has been used to effectively remove the surface native oxide and hydrocarbon residues [6, 7]. This technique has attracted a lot of attention due to its simplicity, ease of integration and low cost. Furthermore, it can be applied to fabrication of both MOS and bipolar devices.

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INTEGRATED PROCESSING

For both the MOS gate electrode or the bipolar emitter contact applications, the polysilicon deposition immediately follows the most critical step in the process sequence, i.e. the gate oxidation in the MOS devices, and the preparation of the emitter contact in bipolars. Sequential processing of silicon wafers, gate oxidation followed by *in-situ* deposition of polysilicon electrode without exposing the wafers to atmospheric ambient, has been shown to improve the device yield [8]. The results of comparing the breakdown performance of in-situ and ex-situ deposited polysilicon electrodes for PMOS capacitors are shown in Figure 1. For these samples,

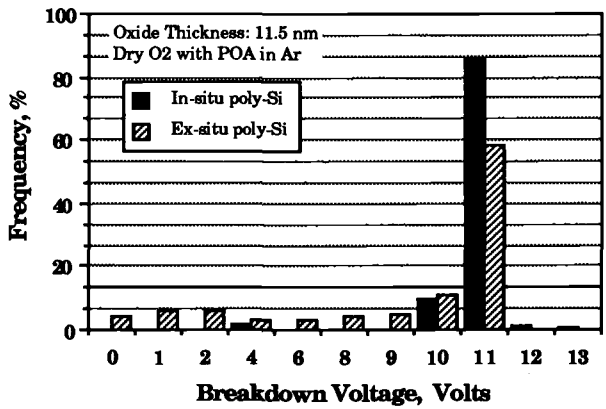

Figure 1. A comparison of intrinsic integrity of PMOS capacitors for in-situ vs. ex-situ deposited poly-Si electrodes on 115 Å of gate oxide.

the breakdown voltage was measured after the capacitors were ramped to 90 percent of the breakdown level once.

For bipolar devices with poly-emitter technology, control of the polysilicon / silicon substrate interface is the key parameter for performance repeatability. Conventionally, a thin oxide layer is chemically grown on the silicon substrate prior to polysilicon deposition. Chemical oxide films are silicon-rich and have a rough surface morphology. Due to the delay between their growth and polysilicon deposition, control of the oxide thickness is poor. Both native and chemical oxide films are thermally

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and chemically unstable and break down during the polysilicon deposition and emitter drive-in steps [9].

Ronsheim, et. al, [10] have reported on the correlation between the polysilicon / silicon interfacial oxygen content and the bipolar transistor performance. As expected, the transistor gain increases by the increasing amount of interfacial oxide thickness. The increase in the emitter resistance, however, becomes very severe at higher interfacial oxygen content. Tejwani, et. al, [11] have reported on the feasibility of improving the transistor gain without sacrificing the device speed, as evidenced by the value of the emitter resistance. An alternative approach to interfacial oxide growth and polysilicon deposition employs a bipolar poly-emitter integrated processing tool to clean, form and cap the interface [12]. Using the emitter resistance as a figure of merit, the effect of various wafer transfer media on poly-emitter interface characteristics is shown in Figure 2. The comparison is between hot and cold (100°C) conventional furnaces and single-wafer RTCVD. The RTCVD sample received an *in-situ* hydrogen clean prior to polysilicon deposition. This cleaning step completely removed the interfacial oxide, resulting in the lowest emitter resistance value. Depending on the device application, a controlled ultra-thin interfacial oxide film can be grown prior to the polysilicon deposition. For optimum performance, the thickness of the interfacial oxide must be controlled to balance the benefits of the higher transistor gain and the increase in the emitter resistance.

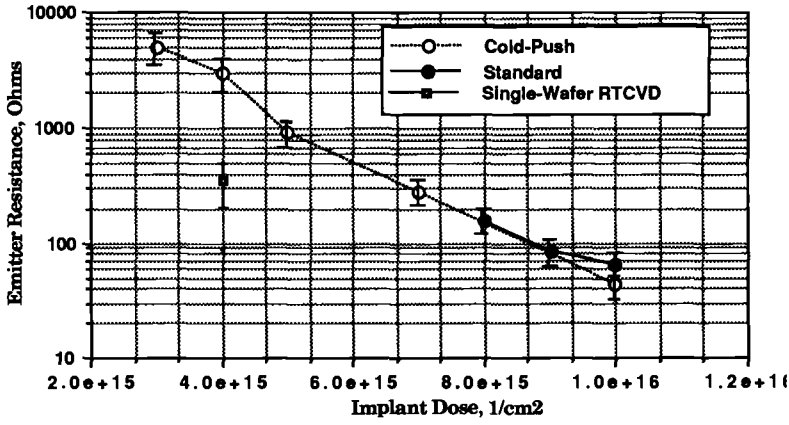

Figure 2. The effect of wafer transfer media on the emitter resistance, "standard" and "cold" furnace conditions are 625° and 100°C, respectively.

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MOS Gate Dielectric Engineering

One application of RTCVD is in engineering of sub 10 nm MOS gate dielectrics. It has been demonstrated that the annealed-nitrided oxides (ANO) films have superior electrical and diffusion barrier properties to pure oxides [13]. The immunity and electrical integrity of optimized ANO films to hot carriers, after injection of 0.5 C/cm^2 of charge, is shown in Figure 3. 80 Å thick oxide films were first grown at 1050°C in dry oxygen. Samples were then nitrided in diluted ammonia ambient and sequentially annealed in oxygen and argon. Hole trapping is observed in pure oxide films, while severe electron trapping is evident in the nitrided oxides. Properly engineered ANO films, however, exhibit excellent immunity against injected charge. Electron trapping behavior of the nitrided oxide films can be correlated to the nitridation conditions. Higher partial pressure of ammonia and nitridation temperature results in larger shifts in the flat band voltage. This is primarily due to higher concentration of nitrogen at the oxide/silicon interface and larger concentration of hydrogen related species in the oxide film [13]. The post nitridation anneal in oxygen

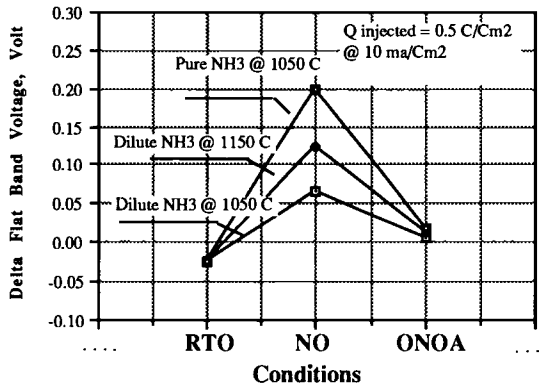

Figure 3. Hot carrier immunity of optimized ANO structures after injection of 0.5 C/cm^2 of charge at 10 mA/cm^2.

and argon is mandatory to remove the nitrogen and hydrogen species from the bulk of the oxide and silicon/oxide interface. The balance between the sequential oxygen and argon anneal is to minimize the oxide growth at the interface and to remove the electron trap sites.

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Bipolar Poly-emitter Interface Engineering

The interfacial oxide must be thicker than 10 Å to be thermally and chemically stable and, thin enough not block dopant atoms, approximately less than 30 Å. Furthermore, for best transistor performance, the interfacial oxide must have a near-SiO_2 stoichiometry. For this range of oxide thickness, the oxidation kinetics must be greatly reduced. This can be achieved by reducing the oxidation temperature, pressure and by lowering the partial pressure of oxygen. Using SIMS, the oxidation kinetics of ultra-thin oxide films expressed as total integrated dose of oxygen is shown in Figure 4. For these samples, upon completion of the oxidation step, polysilicon caps were *in-situ* deposited.

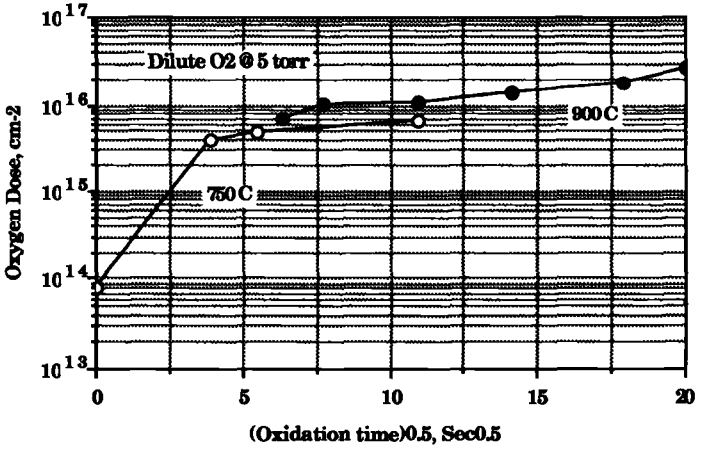

Figure 4. The oxidation kinetics of ultra-thin interfacial oxide films expressed as total integrated dose of oxygen, using SIMS.

Polysilicon deposition - RTCVD of polysilicon films is considered to be a complementary process for both integrated MOS gate and bipolar poly-emitter applications. Polysilicon films in production must have good thickness uniformity, smooth surface morphology, uniform grain size distribution and proper grain orientation. The throughput of a single-wafer system must be comparable to that of a conventional LPCVD tube furnace. This can be accomplished by increasing the deposition rate of polysilicon. The deposition kinetics of polysilicon at 5 torr pressure and 2% SiH_4/H_2 chemistry is shown in Figure 5. At higher pressures, homogeneous gas

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phase nucleation may result in severe particle problems. While increasing the temperature will increase film growth rate, it will also produce larger polysilicon grains and rough surface morphology. These effects are undesirable and can be prevented by a two step deposition process. An initial deposition at 580° to 630°C grows a fine grain nucleating layer while subsequent deposition at 680° to 780°C completes the stack. At the lower temperatures, the deposition rate is 100 to 200 Å/min. It rises to 1000 to 2000 Å/min in the higher temperature range. Based on TEM plan view results, the average grain size for the two-step deposited films is approximately 1.5 to 2 times larger than the conventional LPCVD polysilicon films.

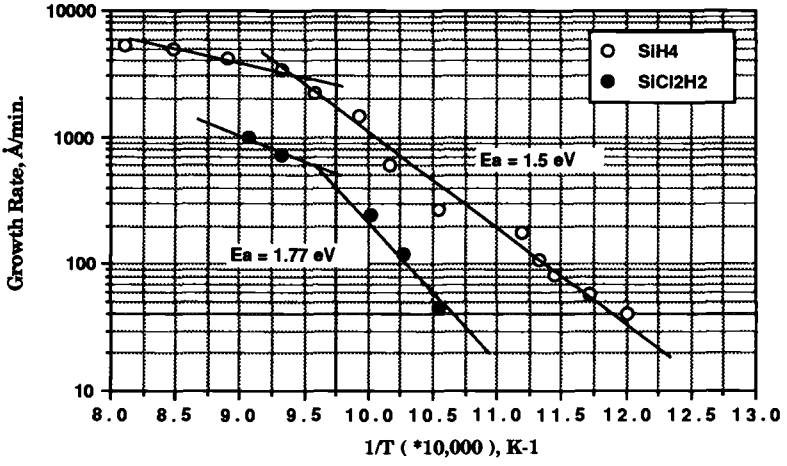

Figure 5. The growth kinetics of polysilicon at 5 torr pressure for silane/hydrogen and dichlorosilane/hydrogen chemistries.

SUMMARY

The applications of single-wafer RTCVD for fabrication of MOS and bipolar devices are discussed. For front-end processing, the MOS gate dielectric engineering and bipolar poly-emitter interface engineering are the most immediate applications. The same reactor technology may be used for gate oxidation and poly-emitter interfacial oxide growth. An integrated, environmentally controlled processing system that incorporates cleaning, oxidation, and RTCVD polysilicon modules would satisfy the processing requirements of both MOS and bipolar technologies.

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