84CH2099-0

# international ELECTRON DEVICES meeting

# 1984

## SAN FRANCISCO, CA

DECEMBER 9-12, 1984

TECHNICAL DIGEST

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*Late News!*
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Sponsored by Electron Devices Society of IEEE

# 1984 International Electron Devices Meeting
# TECHNICAL DIGEST

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Copies of available volumes of this Digest may be obtained from The Institute of Electrical & Electronics Engineers, Inc., 445 Hoes Lane, Piscataway, N.J.
Library of Congress Catalog Card Number: 78-20188.

IEEE Catalog Number: 84CH2099-0

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*Co-Chairmen:* P. H. Zimmerman
W. M. Scott

2:15 p.m.
**INTRODUCTION**

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**14.2 MONOLITHIC INTRINSIC NMOS HgCdTe IRCCDs WITH ON-CHIP SIGNAL PROCESSING,** T. Koch and J. Phillips, *Santa Barbara Research Center, Goleta, CA* 374

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**14.3 DEVELOPMENT OF AN IMPROVED 16 × 64 InSb CID Array,** C. Wei, H. Woodbury, and S. C-H. Wang, *General Electric Company, Schenectady, NY* 378

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**14.4 FULLY-INTEGRATED ZnO ON SILICON PYROELECTRIC INFRARED DETECTOR ARRAY,** D. Polla, R. Muller and R. White, *University of California, Berkeley, CA* 382

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**14.5 GROWTH AND CHARACTERIZATION OF AS GROWN p-n JUNCTIONS FABRICATED IN MULTILAYER LIQUID PHASE EPITAXIAL (Hg,Cd)Te,** P. Nayar, P. Ward, P. Colter, S. Hampton, I. Slawinski, L. Fishman, C. Callahan, and H. Vydyanath, *Aerojet Electrosystems Co., Azusa, CA* 385

4:25 p.m.
**14.6 SURFACE LEAKAGE CURRENT MECHANISMS IN HgCdTe GATE CONTROLLED PHOTODIODES,** J. Rosbeck and E. Blazejewski, *Santa Barbara Research Center, Goleta, CA* 389

4:50 p.m.
**14.7 Hg DIFFUSED $Hg_{1-x}Cd_xTe$ PHOTODIODES FOR LWIR DIRECT DETECTION APPLICATIONS,** R. Briggs and J. Shanley, *Honeywell, Inc., Lexington, MA* 393

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*Co-Chairmen:* R. W. Mauntel
J. Manoliu

2:15 p.m.
**INTRODUCTION**

2:20 p.m.
**15.1 CHARACTERIZATION AND MODELING OF A LATCH-UP FREE 1 MICRON CMOS TECHNOLOGY,** Y. Taur, W. Chang and R. Dennard, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY* 398

2:45 p.m.
**15.2 LATCHUP FREE CMOS USING GUARDED SCHOTTKY BARRIER PMOS,** S. Swirhun, E. Sangiorgi, R. Swanson, K. Saraswat and R. Dutton, *Stanford University, Stanford, CA,* and A. Weeks, *VLSI Technology, San Jose, CA* 402

3:10 p.m.
**15.3 A NEW METHOD FOR PREVENTING CMOS LATCH-UP,** K. Terrill, P. Byrne, H. Zappe, N. Cheung and C. Hu, *University of California, Berkeley, CA* 406

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**15.4 REDUCED $N^+/P^+$-SPACING WITH HIGH LATCHUP HARDNESS IN SELF-ALIGNED DOUBLE WELL CMOS TECHNOLOGY,** U. Schwabe, E. Jacobs and D. Takacs, *Siemens AG, Munich, FRG,* J. Winnerl and E. Lange, *Technical University Munich, Munich, FRG* 410

4:00 p.m.
**15.5 DEEP SUBMICRON MOSFET CHARACTERISTICS WITH 5 nm GATE OXIDE,** T. Kobayashi, S. Horiguchi and K. Kiuchi, *Nippon Telegraph and Telephone Public Corporation, Kanagawa, JAPAN* 414

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**15.6 A FINE-LINE CMOS TECHNOLOGY THAT USES P+ POLY-SILICON/SILICIDE GATES FOR NMOS AND PMOS DEVICES,** L. Parrillo, S. Hillenius, R. Field, E. Hu, W. Fichtner and M. L. Chen, *AT&T Bell Laboratories, Murray Hill, NJ* 418

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**15.7 HIGH PERFORMANCE SUBHALF-MICROMETER P-CHANNEL TRANSISTORS FOR CMOS VLSI,** A. Schmitz, P. Vasudev and J. Chen, *Hughes Research Laboratories, Malibu, CA* 423

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*Co-Chairmen:* D. L. Blackburn
M. Kurata

2:15 p.m.
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2:20 p.m.
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**16.2 A NEW TRIGGERED MODE FOR LIGHT TRIGGERING THYRISTORS,** Y. C. Kao and S. G. Leslie, *Westinghouse R&D Center, Pittsburgh, PA* 432

3:10 p.m.
**16.3 A VERY HIGH SENSITIVITY AND VERY HIGH SPEED LIGHT TRIGGERED AND LIGHT QUENCHED STATIC INDUCTION THYRISTOR (LTQSIThy),** J. Nishizawa and K. Nonaka, *Tohoku University, Sendai, JAPAN,* T. Tamamushi, *Semiconductor Research Institute, Sendai, JAPAN* 435

3:35 p.m.
**16.4 A HIGHLY INTERDIGITATED GTO POWER SWITCH WITH RECESSED GATE STRUCTURE,** P. Roggwiller, J. Gobrecht, J. Voboril and B. Broich, *Brown Boveri Research Center, Baden, SWITZERLAND* 439

4:00 p.m.
**16.5 NUMERICAL SIMULATION OF THE GTO THYRISTOR,** E. Palm and F. Van de Wiele, *Universite de Catholique de Louvain, Louvain-la-Neuve, BELGIUM* 443

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4:50 p.m.
**16.7 VHF HIGH POWER $VD^2$ MOSFET,** H. Yoshida, Y. Shibata and Y. Usunaga, *NEC Corp., Kawasaki City, Kanagawa, JAPAN* 451

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*Imperial Ballroom*

*Co-Chairmen:* D. C. Guterman
C. Hu

2:15 p.m.
**INTRODUCTION**

2:20 p.m.
**17.1 TECHNOLOGY REQUIREMENTS FOR MEGA BIT CMOS EPROMS,** K. Yoshikawa, M. Sato, S. Mori, Y. Mikata, T. Yanase, K. Kanzaki and H. Nozawa, *Toshiba Corporation, Kawasaki, JAPAN* 456

2:45 p.m.
**17.2 A HIGH PERFORMANCE CMOS PROCESS FOR THE NEXT GENERATION EPROM,** J. Lien, S. Longcor, K. Chang, L. Shen, P. Manos, D. Chan, T. Lee and S. Nallamothu, *Advanced Micro Devices, Sunnyvale, CA* 460

3:10 p.m.
**17.3 A NEW FLASH $E^2$ PROM CELL USING TRIPLE POLYSILICON TECHNOLOGY,** F. Masuoka, M. Asano, H. Iwahashi, T. Komuro and S. Tanaka, *Toshiba Corp., Kawasaki, JAPAN* 464

3:35 p.m.
**17.4 DESIGN OF AN $E^2$ PROM MEMORY CELL LESS THAN 100 SQUARE MICRONS USING 1 MICRON TECHNOLOGY,** S. Lai, Y. Hu, S. Tam, G. Lum and V. Dham, *Intel Corp., Santa Clara, CA* 468

4:00 p.m.
**17.5 A SHIELDED SUBSTRATE INJECTOR MOS (SSIMOS) EEPROM CELL,** R. Stewart, A. Ipri, L. Faraone, J. Cartwright and K. Schlesier, *RCA Laboratories, Princeton, NJ* 472

4:25 p.m.
**17.6 CONDUCTION IN THERMAL OXIDES GROWN ON POLYSILICON AND ITS INFLUENCE ON FLOATING GATE EEPROM DEGRADATION,** G. Groeseneken and H. Maes, *Katholieke Universiteit Leuven, Heverlee, BELGIUM* 476

4:50 p.m.
**17.7 ENDURANCE MODEL FOR TEXTURED POLY FLOATING GATE MEMORIES,** H. Wegener, *Xicor, Inc., Milpitas, CA* 480

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*Hilton Plaza*

*Co-Chairmen:* R. W. Herriott
R. Harper

2:15 p.m.
**INTRODUCTION**

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**18.1 SLOW-WAVE STRUCTURES IN MICROWAVE TUBES** (Invited Paper), B. Epsztein, *THOMSON-CSF, Boulogne Billancourt, FRANCE* 486

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**18.2 A HIGHLY EFFICIENT, LINEAR, HIGH POWER X-BAND COUPLED CAVITY TWT FOR ECM-RESISTANT AIR-BORNE RADAR,** K. Amboss, W. Harman and I. Tammaru, *Hughes Electron Dynamics Division, Torrance, CA* 490

3:10 p.m.
**18.3 RECENT PROGRESS IN MILLIMETER-WAVE TUNNELADDER TWT's,** D. Wilson, Jr., A. Jacquez and D. Andker, *Varian Associates, Palo Alto, CA* 494

4:00 p.m.
**18.4 BIPERIODIC FREE-LADDER MILLIMETER WAVE COMMUNICATION TWT,** K. [illegible] and M. [illegible], *Varian Canada, Inc., Georgetown, ONTARIO,* [illegible] and D. [illegible], *Varian Associates, Inc., Palo Alto, CA*

4:00 p.m.
**18.5 750W HELIX TWT FOR 14GHz EARTH STATIONS,** G. Fleury, D. Henry, J. Kuntzmann and S. LeFur *THOMSON-CSF, Boulogne Billancourt, FRANCE* 498

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4:50 p.m.
**18.6** **A 100 WATT, 44 GHz TRAVELLING WAVE TUBE,** S. Tip[illegible] G. Ball and [illegible] *Engl[illegible] Electric [illegible] Co. Ltd., Witham, Essex, ENGLAND*

4:50 p.m.
**18.7** **RECENT ADVANCES IN AN EHF HELIX TWTS,** R. Ohtomo, G. Wada, J. Benton and M. Pohlenz, *Hughes Aircraft Company, Torrance, CA* 502

5:15 p.m.
**18.8** **44 GHz HELIX TWT's FOR SATELLITE COMMUNICATION SYSTEMS,** A. Jacquez, *Varian Associates, Palo Alto, CA* 506

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*Franciscan Room*

*Co-Chairmen:* J. J. Coleman
L. Figueroa

2:15 p.m.
**INTRODUCTION**

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**19.1** **FREQUENCY CONTROL OF SEMICONDUCTORS LASERS** (Invited Paper), S. Wang, *University of California, Berkeley, CA* 510

**2:45 p.m.**
**19.2** **SINGLE LONGITUDINAL MODE DISTRIBUTED FEEDBACK DOUBLE CHANNEL PLANAR BURIED HETEROSTRUCTURE 1.55um IN GaAsP/InP LASERS,** D. Wilt, R. Yen, T. Wessel, P. Besomi, R. Brown, T. Cella, N. Dutta and P. Anthony, *AT&T Bell Laboratories, Murray Hill, NJ* 514

3:10 p.m.
**19.3** **IMPROVED HIGH POWER TWIN CHANNEL LASER WITH BLOCKING LAYER,** C. Morrison, L. Zinkiewicz, A. Burghard and L. Figueroa, *TRW, Inc., Redondo Beach, CA* 517

3:35 p.m.
**19.4** **MONOLITHIC INTEGRATION OF A QUANTUM-WELL LASER AND A DRIVER CIRCUIT ON A GaAs SUBSTRATE,** O. Wada, T. Sanada, S. Yamakoshi, H. Hamaguchi, T. Fujii, T. Horimatsu and T. Sakurai, *Fujitsu Limited, Atsugi, JAPAN* 520

4:00 p.m.
**19.5** **InGaAs/GaAs, STRAINED-LAYER SUPERLATTICE (SLS), JUNCTION PHOTODETECTORS, LED's, INJECTION LASERS's, AND FET's FOR OPTOELECTRONIC IC APPLICATIONS** (Invited Paper), T. Zipperian, L. Dawson, C. Barnes, J. Wiczer and G. Osbourn, *Sandia National Labs., Albuquerque, NM* 524

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**19.6** **AlAs/GaAs SUPERLATTICE BARRIER UNIPOLAR DIODE STRUCTURES,** T. Drummond and H. Hjalmarson, *Sanida National Labs., Albuquerque, NM;* P. Pearah, H. Morkoc, *Univ. of Illinois, Urbana, IL* 528

4:50 p.m.
**19.7** **CHARACTERIZATION OF DOUBLE HETEROJUNCTION GaAs/AlGaAs HOT ELECTRON TRANSISTORS,** N. Yokoyama, K. Imamura, T. Ohshima, H. Nishi, S. Muto, K. Kondo and S. Hiyamizu, *Fujitsu Limited, Atsugi, JAPAN* 532

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*Continental Ballroom 4*

*Panel Moderator:* Billy Crowder
IBM Corporation
East Fishkill, NY

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*Continental Ballroom 5*

*Panel Organizer:* John Shott
Stanford University
Stanford, CA

*Panel Moderator:* Brian Reid
Stanford University
Stanford, CA

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*Continental Ballroom 6*

*Panel Moderator:* David R. Myers
Sandia National Laboratories
Albuquerque, NM

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*Panel Moderator:* Robert K. Parker
Naval Research Laboratory
Washington, D.C.

**SESSION 24: Evening Panel Discussion** 545

Tuesday, December 11, 8:00 p.m.
*Imperial Ballroom*

*Panel Moderators:* John Barnes
Motorola, Inc.
Austin, TX

Wolfgang Fichtner
AT&T Bell Laboratories
Murray Hill, NJ

**SESSION 25: Detectors, Sensors and Displays—New Sensor Technologies and Characterization Methods** 547

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*Co-Chairmen:* W. E. Tennant
R. S. Muller

9:00 a.m.
**INTRODUCTION**

9:05 a.m.
**25.1** **HIGH-GAIN PHOTODETECTORS IN THIN-FILM TRANSISTORS FABRICATED FROM LASER-CRYSTALLIZED SILICON ON FUSED SILICA,** A. Chiang and N. Johnson, *Xerox Palo Alto Research Center, Palo Alto, CA* 548

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**25.2** **A HALF INCH SIZE CCD IMAGE SENSOR OVERLAID WITH A HYDROGENATED AMORPHOUS SILICON,** T. Chikamura, T. Komeda, D. Ishiko, M. Yoshino, M. Nakayama, K. Yano, Y. Aoki, A. Ueno, T. Yamada and T. Ishihara, *Matsushita Industrial Co. Ltd., Osaka, JAPAN* 552

9:55 a.m.
**25.3** **CHARACTERIZATION OF DARK CURRENT IN CCD IMAGERS,** G. Hawkins, L. Rivaud and J. Kyan, *Eastman Kodak Company, Rochester, NY* 556

10:20 a.m.
**25.4** **ELECTRON-BEAM INDUCED CURRENT MEASUREMENT OF HgCdTe HETEROJUNCTION INFRARED DETECTORS,** S. Price, *Santa Barbara Research Center, Goleta, CA* 560

10:45 a.m.
**25.5** **A.C. CHARACTERIZATION AND MODELING OF LATERAL BIPOLAR MAGNETOTRANSISTORS,** A. Andreou and C. Westgate, *The Johns Hopkins University, Baltimore, MD* 564

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11:10 a.m.
**25.6 SENSITIVITY AND NOISE OF A LATERAL BIPOLAR MAGNETOTRANSISTOR IN CMOS TECHNOLOGY,** R. S. Popovic, *LGZ Landis and Gyr Zug Corp., Zug, SWITZERLAND;* R. Widmer, *Swiss Federal Institut of Technology, Zurich, SWITZERLAND* 568

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*Co-Chairmen:* W. G. Oldham
T. Shibata

9:00 a.m.
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9:05 a.m.
**26.1 TRENCH ISOLATION PROSPECTS FOR APPLICATION IN CMOS VLSI,** (Invited Paper) R. Rung, *Hewlett Packard Co., Corvallis, OR* 574

9:30 a.m.
**26.2 A NEW TRENCH ISOLATION TECHNOLOGY AS A REPLACEMENT OF LOCOS,** H. Mikoshiba, T. Homma and K. Hamano, *NEC Corporation, Kanagawa, JAPAN* 578

9:55 a.m.
**26.3 NEW TECHNIQUE FOR ELIMINATION OF THE BIRD'S HEAD AND BIRD'S BEAK,** G. Burton, P. Tuntasood, F. Chien, R. Kovacs, and M. Vora, *Fairchild Research Center, Palo Alto, CA* 582

10:20 a.m.
**26.4 DEFECT GENERATION IN TRENCH ISOLATION,** C. Teng, C. Slawinski, and W. Hunter, *Texas Instruments Incorporated, Dallas, TX* 586

10:45 a.m.
**26.5 A FULLY SCALED SUBMICRON DIRECT WRITE E-BEAM CMOS TECHNOLOGY FOR ULSI DIGITAL APPLICATIONS,** R. Lutze, H. Vyas and J. Huang, *Honeywell Inc., Plymouth, MN* 590

11:10 a.m.
**26.6 APPLICATION OF SELECTIVE SILICON EPITAXIAL GROWTH FOR CMOS TECHNOLOGY,** S. Nagao, K. Higashitani, Y. Akasaka and H. Nakata, *Mitsubishi Electric Corp., Itami, JAPAN* 593

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*Co-Chairmen:* S. Diehl-Nagle
P. Sullivan

9:00 a.m.
**INTRODUCTION**

9:05 a.m.
**27.1 CRYOGENIC BEHAVIOR OF SCALED CMOS DEVICES,** J. Schrankler, J. Huang, R. Lutze, H. Vyas and G. Kirchner, *Honeywell Inc., Plymouth, MN* 598

9:30 a.m.
**27.2 1.5 MICRON GATE CMOS OPERATED AT 77°,** I. Kato, H. Oka, S. Hijiya and T. Nakamura, *Fijitsu Labs., Ltd., Atsugi, JAPAN* 601

9:55 a.m.
**27.3 EFFECTS OF SURFACE ROUGHNESS ON INVERSION LAYER TRANSPORT** (Invited Paper), D. Ferry, *Arizona State University, Tempe, AZ* 605

10:20 a.m.
**27.4 A NEW p-CHANNEL MOSFET STRUCTURE WITH SCHOTTKY-CLAMPED SOURCE AND DRAIN,** C. S. Oh, Y. Koh and C. Kim, *Institute of Science and Technology, Seoul, KOREA* 609

10:45 a.m.
**27.5 SCALING OF COMPENSATED MOSFETS TOWARDS SUBMICRON DIMENSIONS,** F. M. Klaassen, J. J. J. Bastiaens, W. Hes and M. Sprokel, *Phillips Research Laboratories, Eindhoven, THE NETHERLANDS* 613

11:10 a.m.
**27.6 A SMALL-SIGNAL HIGH-FREQUENCY MODEL FOR THE FOUR-TERMINAL INTRINSIC MOSFET VALID IN ALL REGIONS OF OPERATION,** M. Bagheri and Y. Tsividis, *Columbia University, New York, NY* 617

11:35 a.m.
**27.7 TWO-DIMENSIONAL MOSFET SIMULATION WITH ENERGY TRANSPORT PHENOMENA,** M. Fukuma and R. Uebbing, *NEC Corporation, Kawasaki, JAPAN* 621

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Wednesday, December 12, 9:00 a.m.
*Imperial Ballroom*

*Co-Chairmen:* J. T. Clemens
R. R. Troutman

9:00 a.m.
**INTRODUCTION**

9:30 a.m.
**28.2 PROCESS CONSIDERATIONS IN RESTRUCTURABLE VLSI FOR WAFER-SCALE INTEGRATION,** P. Wyatt, J. Raffel, G. Chapman, B. Mathur, J. Burns and T. Herndon, *MIT, Lincoln Lab., Lexington, MA* 626

9:55 a.m.
**28.3 SILICON NITRIDE FILMS BY PLASMA CVD FROM SiH4-N2 and SiF4-N2-H2 GAS MIXTURES,** S. Fujita, H. Toyoshima, T. Ohishi and A. Sasaki, *Kyoto University, Kyoto, JAPAN;* N. Zhou, *The Northwest Telecommunication Engineering Institute, Xi'an, THE PEOPLE'S REPUBLIC OF CHINA* 630

10:20 a.m.
**28.4 ELEVATED SOURCE/DRAIN MOSFET,** S. Wong, D. Bradbury, D. Chen and K. Y. Chiu, *Hewlett Packard Labs., Palo Alto, CA* 634

10:45 a.m.
**28.5 MULTIPLE SELF-ALIGNMENT MOS TECHNOLOGY MUSA/MOST,** H. Horie, T. Fukano, T. Ito and H. Ishikawa, *Fujitsu Laboratories Ltd., Atsugi, JAPAN* 638

11:10 a.m.
**28.6 N- and P-WELL PROCESS COMPATIBILITY IN A 1 MICRON CMOS TECHNOLOGY,** E. Jacobs, D. Takacs and U. Schwabe, *SIEMENS AG, Munich, FRG* 642

11:35 a.m.
**28.7 A HIGHLY RELIABLE N-MOS PROCESS FOR ONE MEGABIT DYNAMIC RANDOM ACCESS MEMORY,** T. Matsukawa, M. Inuishi, J. Mitsuhashi, M. Hirayama, K. Tsukamoto, S. Uoya, T. Yoshihara and H. Nakata, *Mitsubishi Electric Corporation, Hyogo, JAPAN* 647

## SESSION 29: Electron Tubes—Klystrons, Collectors, and Computations 651

Wednesday, December 12, 9:00 a.m.
*Hilton Plaza*

*Co-Chairmen:* A. Staprans
R. K. Parker

9:00 a.m.
**INTRODUCTION**

9:05 a.m.
**29.1 DEVELOPMENT OF 2 GHz, 1MW KLYSTRON FOR PLASMA HEATING,** S. Miyake, H. Ohno, H. Ishihara, S. Hosoi, and T. Okamoto, *Toshiba Corporation, Kawasaki-City, JAPAN;* T. Nagashima, K. Uehara, T. Imai, T. Fujii, K. Sakamoto, Y. Ikeda and M. Saigusa, *Japan Atomic Energy Research Institute, JAPAN* 652

9:30 a.m.
**29.2 A WIDEBAND 3 MW PEAK POWER S-BAND KLYSTRON,** A. Auberdiac, C. Bearzatto and G. Faillon, *THOMSON-CSF, Boulogne-Billancourt, FRANCE* 656

9:55 a.m.
**29.3 KLYSTRON UPDATE,** M. Shrader and D. Preist, *Varian EIMAC, San Carlos, CA* 660

10:20 a.m.
**29.4 AN EXPERIMENTAL TEST STATION FOR MULTISTAGE DEPRESSED COLLECTORS,** K. Moy and T. Grant, *Varian Associates, Inc., Palo Alto, CA* 665

10:45 a.m.
**29.5 LARGE SCALE SIMULATION OF ELECTRON DEVICES** (Invited Paper), A. Drobot, *Science Applications, Inc., McLean, VA* 668

11:10 a.m.
**29.6 COMPUTATIONS OF VSWR AND MODE CONVERSION FOR COMPLEX GYROTRON WINDOW GEOMETRIES,** A. Salop and M. Caplan, *Varian Associates, Palo Alto, CA* 672

11:35 a.m.
**29.7 A NUMERICAL METHOD FOR PREDICTING BRILLOUIN PLOTS OF COUPLED CAVITY CIRCUITS,** P. Prince, J. Baird and R. H. Jackson *Litton Systems, Inc., San Carlos, CA* 676

## SESSION 30: Integrated Circuits—Bipolar and Buried-Layer MOS Structures 681

Wednesday, December 12, 9:00 a.m.
*Pacific Room*

*Co-Chairmen:* I. Lagnado
Y. Okuto

9:00 a.m.
**INTRODUCTION**

9:05 a.m.
**30.1 A 1.6 GHz LOW POWER SILICON DUAL MODULUS PRESCALER IC,** H. Suzuki, T. Akiyama and K. Ueno, *Fujitsu Limited, Kawasaki, JAPAN* 682

9:30 a.m.
**30.2 AN 80ps ECL CIRCUIT WITH HIGH CURRENT DENSITY TRANSISTOR,** T. Tashiro, H. Takemura, T. Kamiya, F. Tokuyoshi, S. Ohi, H. Shiraki, M. Nakamae and T. Nakamura, *NEC Corporation, Kanagawa, JAPAN* 686

9:55 a.m.
**30.3 A 2 MICRON HIGH PERFORMANCE BIPOLAR 64K ECL STATIC RAM TECHNOLOGY WITH 200 SQUARE MICRONS CONTACTLESS MEMORY CELL,** M. Vora, F. Chien, G. Burton, Y. Koh, R. Brown, W. Herndon and R. Heald, *Fairchild Research Center, Palo Alto, CA* 690

10:20 a.m.
**30.4 PERFORMANCE AND STRUCTURES OF SCALED DOWN BIPOLAR DEVICES MERGED WITH CMOS FETs** (Invited Paper), H. Higuchi, G. Kitsukawa, N. Sasaki and K. Ogiue, *Hitachi, Tokyo, JAPAN;* T. Ikeda, Y. Nishio, *Hitachi, Ibaragi, JAPAN* 694

10:45 a.m.
**30.5 180V ANALOG-COMPATIBLE, HIGH-SPEED LOGIC UTILIZING SEMI-WELL ISOLATION TECHNOLOGY,** T. Okabe, M. Kimura and M. Nagata, *Hitachi Ltd., Tokyo, JAPAN;* I. Shimizu and Y. Nagai, *Hitachi Ltd., Gunma, JAPAN* 698

11:10 a.m.
**30.6 SOI-CMOS 4K SRAM WITH HIGH DOSE OXYGEN IMPLANTED SUBSTRATE,** C-E. Chen, T. Blake, L. Hite, S. Malhi, B. Mao and H. Lam, *Texas Instruments, Inc., Dallas, TX* 702

11:35 a.m.
**30.7 A P-TYPE BURIED LAYER FOR PROTECTION AGAINST SOFT ERRORS IN HIGH DENSITY CMOS STATIC RAMS,** H. Momose, T. Wada, I. Kamohara, M. Isobe, J. Matsunaga and H. Nozawa, *Toshiba Corporation, Kawasaki, JAPAN* 706

## SESSION 31: Quantum Electronics and Compound Semiconductor Devices—Photodetectors 711

Wednesday, December 12, 9:00 a.m.
*Franciscan Room*

*Co-Chairmen:* M. A. Pollack
V. Diadiuk

9:00 a.m.
**INTRODUCTION**

9:05 a.m.
**31.1 ULTRA-HIGH SPEED PHOTODETECTORS,** (Invited Paper), S. Y. Wang, *Hewlett-Packard Laboratories, Palo Alto, CA* 712

9:30 a.m.
**31.2 FAST InGaAs PHOTOCONDUCTIVE DETECTORS WITH SPEED ENHANCED BY BERYLLIUM ION BOMBARDMENT,** P. Downey and R. Martin, *AT&T Bell Laboratories, Holmdel, NJ;* R. Nahory, *Bell Communications Research, Murray Hill, NJ;* O. Lorimor, *AT&T Bell Laboratories, Murray Hill, NJ* 716

9:55 a.m.
**31.3 ION IMPLANTED LATERAL IN $_{.2}Ga_{.8}As$/GaAs STRAINED-LAYER SUPERLATTICE PHOTODETECTOR,** G. Bulman, D. Myers, J. Wiczer, L. Dawson, R. Biefeld and T. Zipperian, *Sandia National Laboratories, Albuquerque, NM* 719

10:20 a.m.
**31.4 NEW PSEUDO-QUANTERNARY GaInAsP SEMICONDUCTORS: A HIGH SPEED "HIGH-LOW" AVALANCHE PHOTODIODE WITH $Ga_{.47}In_{.53}As$/InP GRADED GAP SUPERLATTICE,** F. Capasso, A. Hutchinson and N. Olsson, *AT&T Bell Laboratories, Murray Hill, NJ;* H. Cox and S. Hummel, *Bell Communications Research, Murray Hill, NJ* 723

10:45 a.m.
**31.5 FULLY OPTICALLY AND ELECTRICALLY INTERFACED, MONOLITHIC 1×12 ARRAY of $In_{.53}Ga_{.47}As$/InP p-i-n PHOTODIODES,** M. Brown, S. Forrest, P. Hu, D. Kaplan, M. Koza, Y. Ota, J. Potopowicz, C. Seabury and M. Washington, *AT&T Bell Laboratories, Murray Hill, NJ* 727

11:10 a.m.
**31.6 GaInAs, AlInAs SCHOTTKY BARRIER DIODES AND GaInAs/AlInAs HETEROJUNCTION DIODE AS INTERNAL PHOTOEMISSION DETECTORS,** K. Hsieh, *Hughes Research Lab., Malibu, CA;* L. Eastman, *Cornell University, Ithaca, NY* 729

11:35 a.m.
**31.7 A HIGH SPEED, LOW VOLTAGE SILICON PHOTODIODE WITH BURIED ISOLATION REGION,** G. Chang, A. Hartman, M. Robinson, T. Riley and K. Lee, *AT&T Bell Laboratories, Murray Hill, NJ* 733

## SESSION 32: Device Technology—Advanced Bipolar Technology 737

Wednesday, December 12, 1:30 p.m.
*Continental Ballroom 4,5*

*Co-Chairmen:* J. Aitken
A. Wieder

1:30 p.m.
**INTRODUCTION**

1:35 p.m.
**32.1 CONDUCTION MECHANISM OF POLYSILICON EMITTERS WITH THIN INTERFACIAL OXIDE LAYERS,** H. Schaber, B. Benna, L. Treitinger and A. Wieder, *Siemens AG, Munchen, FRG* 738

2:00 p.m.
**32.2 SIPOS HETEROJUNCTION CONTRACTS TO SILICON,** Y. Kwark, R. Swanson and R. Sinton, *Stanford University, Stanford, CA* 742

2:25 p.m.
**32.3 A SILICON BIPOLAR TRANSISTOR WITH A HYDROGENATED AMORPHOUS EMITTER,** M. Ghannam, J. Nijs, R. DeKeersmaecker and R. Mertens, *Katholieke Universiteit Leuven, Heverlee, BELGIUM* 746

2:50 p.m.
**32.4 SELF-ALIGNED BIPOLAR TRANSISTORS WITH ENHANCED EFFICIENCY POLYSILICON EMITTERS,** A. Cuthbertson and P. Ashburn, *Southampton University, Southampton, Hampshire, ENGLAND* 749

3:15 p.m.
**32.5 NEW SELF-ALIGNED COMPLEMENTARY BIPOLAR TRANSISTORS USING SELECTIVE-OXIDATION MASK,** H. Sadamatsu, M. Inoue, A. Matsuzawa, A. Kanda and H. Shimoda, *Matsushita Electric Industrial Co., Ltd., Osaka, JAPAN* 753

3:40 p.m.
**32.6 MODELLING OF POLYSILICON DOPANT DIFFUSION FOR SHALLOW-JUNCTION BIPOLAR TECHNOLOGY,** G. Barbuscia, G. Chin and R. Dutton, *Stanford University, Stanford, CA;* T. Alvarez, *Motorola, Mesa, AZ;* L. Arledge, *Texas Instruments, Dallas, TX* 757

4:05 p.m.
**32.7 2 MICRON MERGED BIPOLAR-CMOS TECHNOLOGY,** A. Alvarez, P. Meller and B. Tien, *Motorola Inc., Mesa, AZ* 761

## SESSION 33: Solid State Devices—Lightly-Doped Drain MOSFETs 765

Wednesday, December 12, 1:30 p.m.
*Continental Ballroom 6,7,8,9*

*Co-Chairmen:* J. R. Sokel
G. Merkel

1:30 p.m.
**INTRODUCTION**

1:35 p.m.
**33.1 STATE-OF-THE-ART OF MOS MODELLING,** (Invited Paper), A. Schutz and C. Werner, *SIEMENS Research and Development Center, Munchen, WEST GERMANY* 766

2:00 p.m.
**33.2 OPTIMIZATION OF LIGHTLY DOPED DRAIN MOSFETS USING A NEW QUASIBALLISTIC SIMULATION TOOL,** C. Werner, R. Kuhnert and L. Risch, *Siemens AG, Munchen, FRG* 770

2:25 p.m.
**33.3 HOT CARRIER DEGRADATION MODES AND OPTIMIZATION OF LDD MOSFETs,** H. Katto, K. Okuyama, S. Meguro, R. Nagai and S. Ikeda, *Hitachi Ltd., Tokyo, JAPAN* 774

2:50 p.m.
**33.4 EFFECTS OF FIELD BORON DOSE ON SUBSTRATE CURRENT IN NARROW CHANNEL LDD MOSFETs,** S. Sawada, Y. Matsumoto, S. Shinozaki and O. Ozawa, *Toshiba Corporation, Kawasaki-city, JAPAN* 778

3:15 p.m.
**33.5 CHARACTERIZATION OF As-P DOUBLE DIFFUSED DRAIN STRUCTURE,** K. Balasubramanyan, M. Hargrove, M. Lin, D. Hoyniak, J. LaRue, and D. Thomas, *IBM, Essex Junction, VT;* H. Hanafi, *IBM, Yorktown Heights, NY* 782

3:40 p.m.
**33.6 MECHANISM OF HOT ELECTRON INDUCED DEGRADATION IN LDD NMOS-FET,** Y. Toyoshima, H. Nihira, M. Wada and K. Kanzaki, *Toshiba Corporation, Kawasaki, JAPAN* 786

## SESSION 34: Device Technology—SOI and 3-D Technologies 791

Wednesday, December 12, 1:30 p.m.
*Imperial Ballroom*

*Co-Chairmen:* D. Bartelink
S. Malhi

1:30 p.m.
**INTRODUCTION**

1:35 p.m.
**34.1 3-D SOI/CMOS** (Invited Paper), M. Nakano, *Fujitsu, Ltd., Kawasaki, JAPAN* 792

2:00 p.m.
**34.2 FABRICATION OF HIGH SPEED 1 MICRON FIPOS/CMOS,** K. Anzai, F. Otoi, M. Ohnishi and H. Kitabayashi, *OKI Electric Industry Co., Ltd., Tokyo, JAPAN* 796

2:25 p.m.
**34.3 ADVANCES IN OXIDIZED POROUS SILICON FOR SOI,** L. A. Nesbit, *IBM Corporation, Essex Junction, VT* 800

2:50 p.m.
**34.4 ELECTRICAL CHARACTERIZATION OF OXYGEN IMPLANTED SILICON SUBSTRATES,** D. Foster, A. Butler and P. Bolbot, *Plessey Research (Caswell) Ltd., Caswell, Towcester, Northants, U.K.* 804

3:15 p.m.
**34.5 DEVICE PERFORMANCES OF A SUBMICRON SOI TECHNOLOGY,** A. Auberton-Herve, J. Joly, J. Hode, J. Gautier and P. Jeuch, *LETI/Commissariat a l'Energie Atomique, Grenoble, FRANCE* 808

3:40 p.m.
**34.6 MERGED CMOS/BIPOLAR TECHNOLOGIES AND MICROWAVE MESFETS UTILIZING ZONE-MELTING-RECRYSTALLIZED SOI FILMS,** B. Tsaur, H. Choi, C. K. Chen, C. L. Chen, R. Mountain and J. Fan, *Massachusetts Institute of Technology, Lexington, MA* 812

4:05 p.m.
**34.7 PROMISING NEW FABRICATION PROCESS DEVELOPED FOR STACKED LSIs,** M. Yasumoto, H. Hayama and T. Enomoto, *NEC Corporation, Kawasaki, JAPAN* 816

## SESSION 35: Electron Tubes—Fast Wave Tubes 821

Wednesday, December 12, 1:30 p.m.
*Hilton Plaza*

*Co-Chairmen:* J. M. Baird
T. Kageyama

1:30 p.m.
**INTRODUCTION**

1:35 p.m.
**35.1 SURVEY OF PHYSICS RESEARCH IN MICROWAVE DEVICES** (Invited Paper), G. Bekefi, *Massachusetts Institute of Technology, Cambridge, MA* 822

2:00 p.m.
**35.2 A 60 GHz, 200 kW CW GYROTRON WITH HIGH OUTPUT MODE PURITY,** H. Jory, K. Felch, R. Bier, L. Fox, H. Huey, L. Ives, N. Lopez, J. Manca, J. Shively and S. Spang, *Varian Associates, Inc., Palo Alto, CA* 826

2:25 p.m.
**35.3 A 100 GHz, 500 kW GYROTRON OSCILLATOR,** W. DeHope, J. Eldridge, P. Ferguson, S. Hart, A. Krycuk, V. Matranga, J. Sandoval, M. Schmitt, J. Tancredi, C. Thorington and M. Wozniak, *Hughes Aircraft Co., Torrance, CA* 830

2:50 p.m.
**35.4 DESIGN CONSIDERATIONS FOR A 100 kW CW, 140 GHz GYROTRON OSCILLATOR,** K. Felch, R. Bier, L. Fox, H. Huey, L. Ives, H. Jory and S. Spang, *Varian Associates, Inc., Palo Alto, CA* 834

3:15 p.m.
**35.5 PERFORMANCE OF A THREE CAVITY GYROKLYSTRON,** W. Bollen and C. Sedlak, *Mission Research Corp., Alexandria, VA;* A. Ganguly, B. Arfin and R. Parker, *Naval Research Laboratory, Washington, DC* 838

3:40 p.m.
**35.6 FOURTH HARMONIC GYROMAGNETRON DEVELOPMENT,** L. Barnett, J. Baird, U. Shrivastava and R. Grow, *University of Utah, Salt Lake City, UT* 842

4:05 p.m.
**35.7 PENIOTRON AMPLIFIER RESULTS,** G. Döhler, D. Gallagher, C. Lowrie, R. Moats and F. Scafuri, *Northrop Corporation, Rolling Meadows, IL* 845

**NOTE: The following paper was not available at time of publication.**

9:05 a.m.
**28.1 X-RAY LITHOGRAPHY FOR HIGH RESOLUTION** (Invited Paper), A. Heuberger, *Fraunhofer-Institut fur Mikrostrukturtechnik, Berlin, FRG*

# SIPOS HETEROJUNCTION CONTACTS TO SILICON

Young H. Kwark, Ron Sinton, Richard M. Swanson

110 McCullough Building, Stanford Electronics Laboratories
Stanford, CA. 94305 (415)497-0503

Abstract: Using SIPOS films ($SiO_x$, x <2) as an emitter contact has been previously shown to reduce the emitter saturation current, $J_{oe}$, by at least a factor of fifty when compared to a conventional emitter structure with a metallic contact. Previous attempts to explain this $J_{oe}$ reduction have focused on the bulk properties of the SIPOS films. Experimental results of this study which attained $J_{oe}$ values of $2 \times 10^{-}14$ A/cm$^2$, suggest that an interfacial layer between the SIPOS and underlying silicon may play an important, if not dominant, role with the implication that the high oxygen concentrations previously used may not be essential for $J_{oe}$ reduction. This would permit the use of lower oxygen content SIPOS films whose lower bulk resistivities would allow utilization of these films in structures such as scaled VLSI bipolar devices and high concentration point contact solar cells where series resistance is detrimental to device performance.

Introduction: Deliberate introduction of controlled amounts of an oxygen bearing species such as nitrous oxide into the deposition ambient normally used for chemical vapor deposition of polysilicon produces SIPOS, a class of silicon oxides which exhibits a wide range of physical properties (1). It is possible to tailor film characteristics such as the refractive index, by altering the oxygen partial pressure in the deposition ambient. The addition of a dopant species converts these films from semi-insulating to a form that can be made sufficiently conductive after annealing to make them interesting for electronic applications (2). Incorporation of these films into the emitter structure of an NPN bipolar transistor had been found to reduce the emitter saturation current fifty fold (3); this translates into potential improvements of energy conversion efficiency for solar cells and enhanced high frequency performance of bipolar structures.

Matsushita (3) hypothesized that large amounts of oxygen in his SIPOS films produce a bandgap larger than for monocrystalline silicon. In N-type SIPOS emitter contacts the lining up of the equilibrium Fermi levels results in a barrier in the valence band which blocks hole transport and accounts for the reduction in $J_{oe}$. Simplified density of states calculations using small clusters of $SiO_x$ lend qualitative support to this scenario; namely the gap in the density of states increases in a continuous manner as the oxygen content in $SiO_x$ is increased (4). However, it is important to note that these clusters were constructed assuming a uniform and random distribution of oxygen throughout the film. While this may apply to films prepared at low temperatures (e.g. evaporation or sputtering), the CVD deposited SIPOS films used in these devices require a high temperature anneal in order to activate the dopant. A phase precipiation which results in a fine dispersion of silicon microcrystallites embedded in an oxygen rich matrix appears to be the result of such anneals (5). Such a heterogeneous structure would indicate that a model based on an effective bandgap and diffusion length may be oversimplified.

Experimental Results: Bipolar test structures and measurement techniques were refined to allow measurement of the emitter saturation current at these low levels; a sample Gummel plot showing the area related component from which $J_{oe}$, the emitter saturation current, was extracted is shown in Fig. 1. Devices with differing area/perimeter ratios were used in conjunction with the definition

$$I_{base} = Area * J_{area} + Perimeter * J_{peri}$$

to effect this separation. By utilizing various SIPOS emitter contact configurations, these measurements, after correcting to 300°K, allowed determination of which film parameters were relevant in determining the hole blocking action of the films.

The first set of experiments investigated the effect of varying the oxygen content on $J_{oe}$. These films were deposited in a hot wall APCVD reactor using nitrogen as the carrier gas. Varying $\gamma$, the ratio of nitrous oxide to silane in the deposition ambient, from $\gamma = 0$ (which should produce POLY) to $\gamma = 1.5$ (which should produce films comparable to ref. (3)) should display a monotonically decreasing $J_{oe}$ as hole transport is increasingly impeded by the increasing bandgap in the bulk SIPOS. In fact for devices annealed at 900°C/13 min, there is very little dependence on $\gamma$ as seen in Fig. 2, although increasing the anneal temperature to 1000°C adversly affected $J_{oe}$. That the $\gamma$=0 films produced such good results was surprising since POLY films of comparble thickness should yield a $J_{oe}$ an order of magnitude larger. In fact it was discovered that these $\gamma = 0$ films

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incorporated significant (several atomic %) amounts of oxygen as indicated from electron microprobe and the fact that they etched, albeit slowly, in buffered HF. This insensitivity to bulk film properties implies that other mechanisms, in this case the formation of an interfacial oxide layer as a result of the annealing process (Fig. 3), may be primarily responsible for the reduced hole currents. This conclusion suggests that the mechanism of hole suppression is akin to that for polysilicon SIS contacts, and that the distinguishing feature of SIPOS may be its built-in source of oxygen which aids in the formation and/or maintainence of this interfacial layer.

In order to establish unambiguous results for a relatively oxygen free film, POLY films doped insitu in an RF heated cold wall APCVD reactor using a hydrogen carrier were used in the next set of emitter contacts; these films did not etch in BHF. Fig. 4 displays the resulting $J_{oe}$ as a function of annealing temperature for emitter B which had a Gaussian ($3 \times 10^{19}$ surface concentration, 1 micron depth into $5 \times 10^{16}$ background) emitter diffused prior to the POLY deposition and emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction. For both structures, devices were prepared with and without a chemically grown oxide (chemox) by dipping half of the wafer which underwent a full RCA clean in dilute HF. The value for emitter B with a conventional aluminum contact is shown for reference. Addition of POLY without the chemox does not greatly impact $J_{oe}$ as would be expected since the heavily doped POLY acts essentially as an extension of the monocrystalline emitter. Addition of the chemox greatly decreases the $J_{oe}$ as has been previously reported (6). "Prediffused" emitter B displays a baseline $J_{oe}$ of $5 \times 10^{-14}$ A/cm$^2$ due to recombination in the bulk of the emitter. To this is added a component due to outdiffusion from the heavily doped POLY which becomes increasingly significant for annealing temperatures above 900°C. This is apparent if one notes that the increase in $J_{oe}$ for emitter B can be accounted for by the $J_{oe}$ of emitter C at the same temperature. At 1000°C, this outdiffusion is severe enough to dominate the $J_{oe}$ which accounted for the lack of difference between emitters B and C.

In Fig. 5, $J_{oe}$ for a $\gamma = 0$ SIPOS film (which recall has several at% oxygen) without the chemox is shown. The behavior above 850°C strongly resembles the POLY case with chemox. Addition of the chemox to the SIPOS contact structure does not greatly affect the lowest values of $J_{oe}$ attained. However, the increase in $J_{oe}$ at higher temperatures is not as severe as for the devices in Fig. 4 and 5. Furthermore, devices annealed at 850°C, while displaying the same $J_{oe}$ as the SIPOS devices without the chemox, also suffered from greatly increased series resistance.

Discussion: Emitter saturation currents of 1 - 2 $\times 10^{-14}$ A/cm$^2$ have been attained for POLY with chemox and for both SIPOS contact structures. That there was little difference in $J_{oe}$ between the SIPOS contacted emitters with and without the chemox would indicate that the interface between SIPOS and monocrystalline silicon is similar in both cases. Postulating the formation of a thin tunnelable interfacial oxide as a consequence of the high temperature annealing step is consistent with the observed similarities in $J_{oe}$. The smaller increase in $J_{oe}$ for the SIPOS device with chemox can be explained by assuming that the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step. This would act as a more robust diffusion barrier and would limit the extent of outdiffusion of dopants from the SIPOS thus reducing bulk recombination in the monocrystalline emitter region. This is also consistent with the increased series resistance which would arise from a thicker interfacial layer. The possibilty remains that a thin thermal oxide is growing during the thermal equilibration phase prior to deposition of the SIPOS films; although standard precautions were taken to minimze the presence of oxygen and water vapor in the deposition ambient, the apparatus currently available can not be used to rule out this possibility.

A key figure of merit which has not been discussed is the specific resistivity of the emitter contact structure. For the SIPOS films mentioned in ref. (3), a specific contact resistivity of $1 \times 10^{-3}$ ohm-cm$^2$ would result for a 1000 angstrom thick film. This is far too high to permit use in scaled bipolar or in high concentration point contact solar cells. If the hole barrier mechanism operative in SIPOS contacts is indeed associated with the formation of interfacial layers, then there is no apriori need for such high oxygen concentrations in the bulk of the films with their attendant high resistivity. The focus, in this case, would shift to the kinetics of the annealing process and to the morphology of the near interface region, much as is the case with POLY SIS structures. For the $\gamma = 0$ SIPOS contacts, an upper limit to the specific resistivity can be set at $1 \times 10^{-4}$ ohm-cm$^2$ from device Gummel plots; although the actual value is quite likely to be far below this, the presence of other parasitic resistances does not allow a more refined determination from the device data. The ability to directly measure the voltage drop at the interface is being incorporated into the next mask set.

References:


(1) D. Dong, E. Irene, et al "Preparation and Some Properties of CVD Si-rich $SiO_2$ and $Si_3N_4$ Films", J. Electrochemical Soc. 125(5), May 1978, p819

(2) H. Yamoto, N. Oh-uchi , et al "New Technology by the Use of Doped SIPOS Films", ECS Abstracts, #168, 1979

(3) T. Matsushita, "A Silicon Heterojunction Transistor," Appl. Phys. Lett., vol 35(7), p 549, 1979

(4) A. Bennet, L. Roth "Calculation of the Optical Properties of Amorphous $SiO_x$ Materials" Phys. Rev. B 4(8), Oct. 15, 1971, p 2686

(5) M. Hamasaki, "Crystallographic Study of SIPOS Doped with Oxygen Atoms,"J. Appl. Phys. 49(7), p 3987, 1978

(6) B. Soerowirdjo, P. Ashburn, et al "The Influence of Surface Treatments on the Electrical Characteristics of Polysilicon Emitter Bipolar Transistors" Tech. Digest IEDM, 1982, p 668





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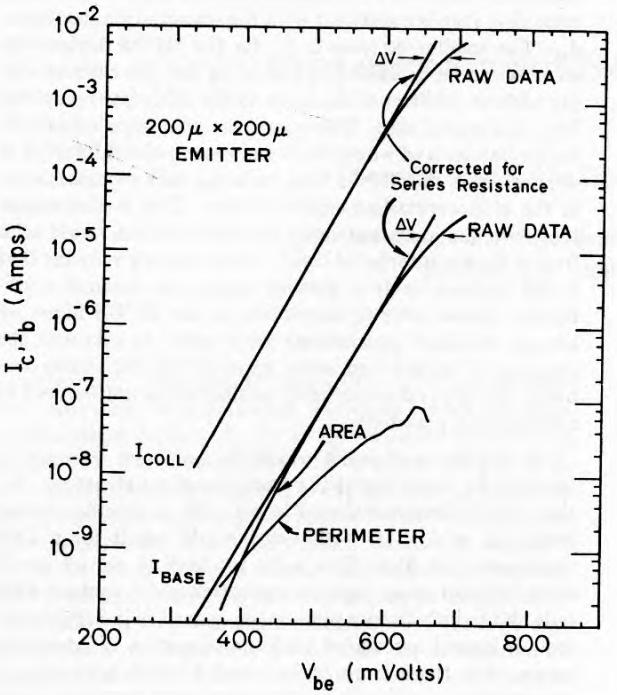


Fig. 1: Gummel plot of test bipolar structure showing area and perimeter related components.

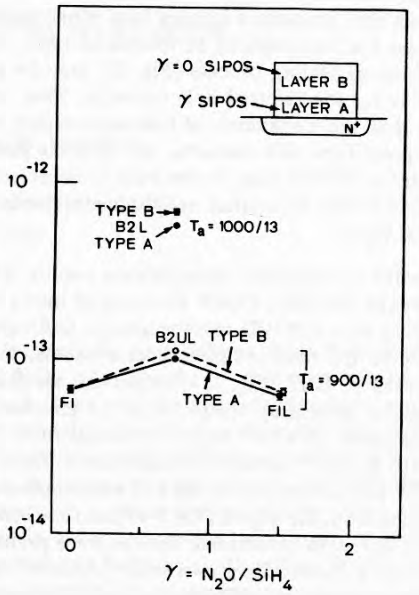


Fig.2: $\gamma$ is the ratio of nitrous oxide to silane in the SIPOS deposition ambient, $T_a$ is the anneal temperature (followed by a slash and anneal time in minutes). Layer B is a 2000 angstrom capping layer; layer A is the "active layer" ranging from 1000 to 1600 angstroms.

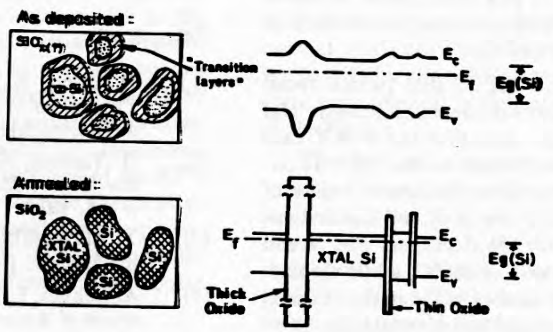


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the "oxide-like" regions become more $SiO_2$-like, accompanied by crystallization of the silicon crystallites.

32.2



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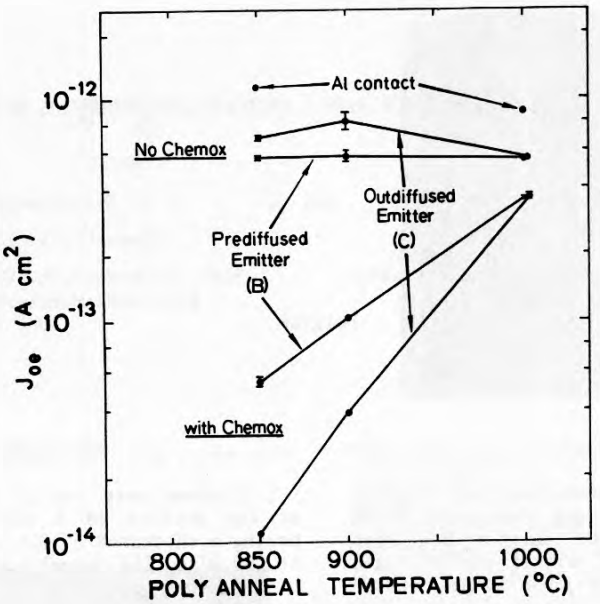


Fig. 4: emitter saturation current for POLY contacts with and without a chemically grown interfacial layer vs. anneal temperature. Thicknesses range from 3000-3600 angstroms. Note the large difference when the interfacial oxide is missing.

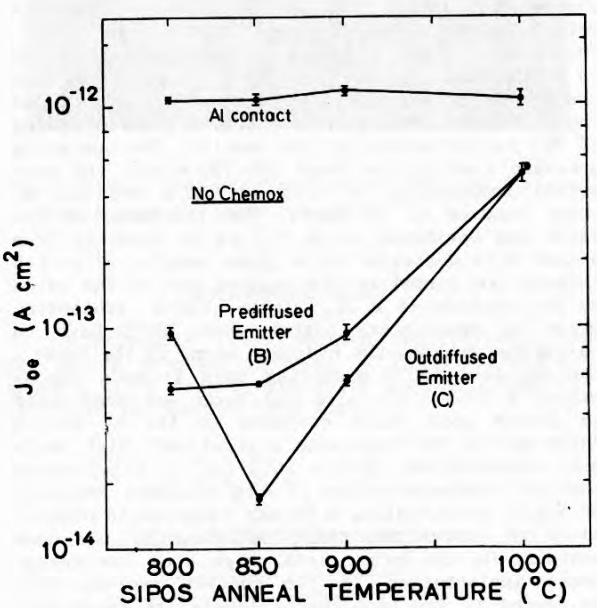


Fig. 5: emitter saturation current vs. anneal temperature for SIPOS contacts without a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

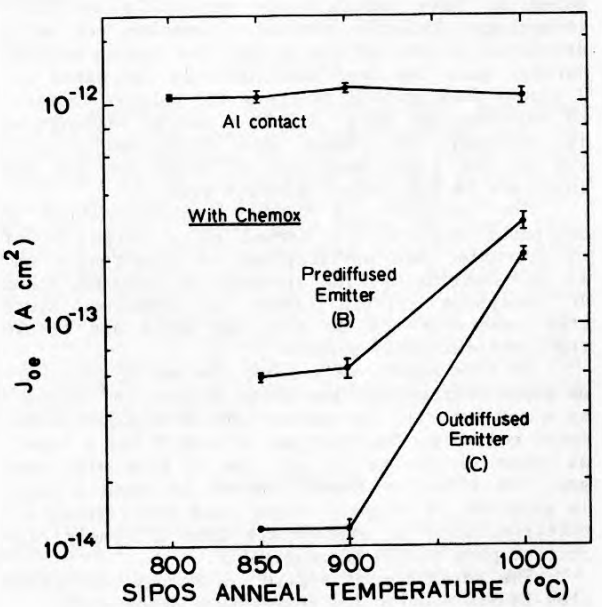


Fig. 6: emitter saturation current vs. anneal temperature for SIPOS contacts with a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.



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