A Study of n^+-SIPOS:p-Si Heterojunction Emitters

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Abstract—**We have found experimental conditions for the growth of n^+-SIPOS:p-Si heterojunction emitters with forward saturation current $J_0 = 10^{-14}$ Amps/cm^2 or equivalently "emitter Gummel number" $G_e = 3.3 \times 10^{15}$ s/cm^4. This outstanding figure of merit seems to rely upon the presence of a thin interfacial oxide between the SIPOS and the crystalline silicon. We invoke a model in which majority-carrier (electron) contact is made by microcrystalline grains which protrude into the interfacial oxide but minority-carrier (hole) recombination is inhibited by the small fractional area coverage of such contacts. The result is an emitter structure which is robust and relatively insensitive to variations in processing conditions.**

THERE have been a considerable number [1], [3] of reports recently on improved bipolar transistor emitters made of polycrystalline silicon or of SIPOS (a mixture of microcrystalline silicon and silicon dioxide). The improvement has come in the forward saturation current J_0, defined by $J \equiv J_0 \exp\{qV/kT\}$. For example, we have recently made SIPOS heterojunction emitters with $J_0 = 10^{-14}$ Amps/cm^2 which is about two orders of magnitude smaller than in a conventional homojunction emitter. An equivalent figure of merit [4] is the "emitter Gummel number" $G_e = 3.3 \times 10^{15}$ s/cm^4 where $G_e \equiv qn_i^2/J_0$ should be as large as possible. (Here q is the electronic charge and n_i is the intrinsic carrier density).

Such heterojunctions are valuable not only for emitter efficiency in bipolar transistors, but also for solar cells. A SIPOS:c-Si:SIPOS double heterostructure solar cell has recently [5] generated 720 mV at open circuit, which is a record for crystalline silicon.

There has been considerable uncertainty as to the mechanism of the improved saturation current, especially the role played by a thin interfacial oxide layer between the polycrystalline or SIPOS emitter and the underlying crystalline silicon substrate. In addition, there have been questions regarding the reproducibility and reliability of these types of high-performance emitters.

In this letter we will present the results of an extensive series of processing runs, in which the experimental conditions were widely varied, not only to optimize the process, but also to help determine the fundamental mechanism of the SIPOS:c-Si heterojunction. These results suggest a model in which the interfacial oxide plays a key role. An optimal process sequence is given in Table I.

Due to the large number of experimental process runs, it was desirable to have a quick diagnostic method which did not rely on the laborious fabrication of individual transistors and the measurement of I–V characteristics. Accordingly, we developed a contactless minority carrier lifetime [6] apparatus which directly and nondestructively measured the forward saturation current J_0 at the heterojunction emitter layer which had been deposited on both the front and back faces of a silicon wafer. The apparatus, shown in Fig. 1, monitors the decay of excess bulk minority carrier density n^b induced by the strobe lamp:

$$\frac{dn^b}{dt} = -\frac{n^b}{\tau_b} - \frac{2J}{qL} \tag{1}$$

where τ_b is the bulk recombination lifetime, the factor 2 accounts for the recombination current J at both front and back surfaces, and L is the sample thickness which should be small. The interfacial recombination velocity S may be defined by $J \equiv qS\,n^b$ in which case (1) becomes

$$\frac{dn^b}{dt} = -\left(\frac{1}{\tau_b} + \frac{2S}{L}\right) n^b. \tag{2}$$

The quantity in brackets is the experimentally measured decay constant which includes both the desired interfacial term S and the bulk term τ_b. We explicitly operate in a regime where n^b is spatially uniform. This will be true if L is much smaller than both $\sqrt{D\tau_b}$ and D/S where D is the minority carrier diffusion constant. In order to make the interfacial term S dominate the bulk term τ_b, then L should be as thin as possible, (which is step (1) of Table I) and τ_b should be as long as possible (step (2)). Accordingly we used Wacker 0.5 Ω·cm, p-type, <100> float zone silicon whose bulk lifetime τ_b was further improved to 450 μs by step (2). (The as-received material was only about half as good.) Due to the excellent bulk lifetime τ_b and the high injection levels $n^b \approx 10^{16}$/cm^3, recombination in the space charge region makes a negligible contribution to S which was independent of injection level as a result. These experiments

TABLE I
AN OPTIMAL PROCESSING SEQUENCE

1) Thin silicon wafers to 50 μm in aqueous KOH.
2) Getter in an oxidation furnace containing substantial chlorine.
3) Strip gettering oxide in HF acid.
4) Immediately load into cold APCVD furnace while purging with N_2.
5) Ramp up to 650°C while maintaining N_2 purge.
6) Oxidize for 5 min with 100 ppm O_2.
7) Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8) Ramp furnace to 900°C.
9) Anneal for 15 min.
10) Ramp furnace down to 450°C.
11) Anneal in Forming gas for 2 h.
12) Pull wafers from cold furnace.

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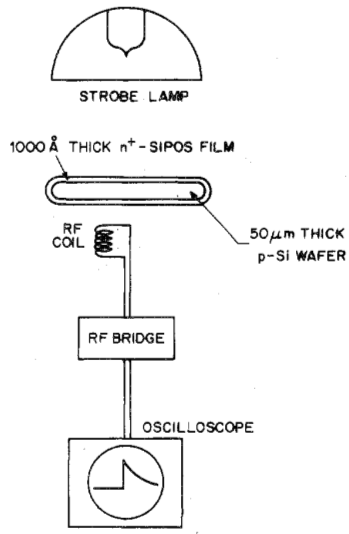

Fig. 1. The experimental apparatus which permitted a rapid and contactless determination of the forward saturation current J_0 of novel heterojunction emitters such as n^+-SIPOS.

which monitor interface quality could equally well have been performed on n-type wafers in which case the space charge region would be altogether absent.

Throughout all processing, we found that it was extremely valuable to monitor the bulk lifetime after each handling step. This could be done by using chemical fluorination [7] of the bare silicon surface to minimize or eliminate S in (2) thereby monitoring process induced changes in τ_b. In this manner, bulk minority lifetime τ_b could be maintained at a high value throughout all processing steps.

Substituting $n^b = (n_i^2/p^b) \exp \{qV'/kT\}$ into the definition of interface recombination velocity S we find that:

$$J = \frac{qSn_i^2}{p^b} \exp \{qV'/kT\} \tag{3}$$

where V' is the separation of quasi-Fermi levels. If we equate V' with V in the definition of forward leakage current J_0 we find $J_0 = q(Sn_i^2)/p^b$ where p^b is the bulk doping density. Equivalently $G_e = p^b/S$.

Using the apparatus in Fig. 1, the observed surface recombination velocity S can be determined in less than one minute. Therefore, J_0 and G_e can be diagnosed immediately after every process run and the information used to determine the conditions for the following run which could begin immediately. This enabled us to rapidly converge on an optimal set of process conditions as outlined in Table I.

Let us now discuss what we learned in the course of this iterative procedure. Step (6), the oxidation step, is of critical importance. In omitting that one step, G_e degrades by almost an order of magnitude. We found that purging with high-purity cylinder gas (0.5 ppm, O_2, and H_2O) helps to reproducibly control this oxidation step. In some published results [1], [3] on SIPOS heterojunction emitters and polysilicon emitters this step has been omitted, but we believe that oxidation frequently occurs inadvertently and is necessary toward achieving the most favorable figure of merit. Dewar nitrogen gas is notoriously unreliable in regard to oxygen concentration and was avoided. Likewise, it was helpful to load the silicon into a cold furnace to prevent inadvertent oxidation.

The annealing step (9) follows SIPOS deposition. This step is necessary to precipitate microcrystalline silicon grains within the material and to activate the phosphorus dopant. In addition, during this step the phosphorus diffuses about 20–50 Å into the silicon wafer as measured by secondary ion mass spectrometry. This produces a very shallow n^+ inversion layer which is transparent to minority carriers, i.e., the holes from the bulk "see" the Si–SiO_2 interface. Recent studies[8] of electron-hole recombination at thermally grown Si–SiO_2 interfaces have shown that under electron accumulation the recombination current is $\exp \{qV/kT\} \times 10^{-14}$ Amps/cm^2, which is consistent with the performance level achieved with the SIPOS emitter structure in Fig. 2.

Oxide thicknesses between 25 and 40 Å were found to be equally favorable with respect to the "emitter Gummel number." Therefore, differential tunneling between electrons and holes does not appear to be playing a major role because, over part of this range the oxide is too thick for even electron tunneling. We believe that majority carrier electrical contact is by individual microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 2, i.e., electrical contact is via thin spots and pinholes in the SiO_2.

The chemical mixture in step (7) of Table I results in a SIPOS formulation with only 5 percent oxygen incorporation as determined by X-ray fluorescence. At such low levels of oxygen concentration one might ask what distinguishes a SIPOS heterojunction from a polysilicon emitter. Indeed the resistivity of the n^+ – SIPOS ($\rho = 10^{-3}\ \Omega\cdot$cm) is similar to that of doped polysilicon. We believe the importance of the 5 percent oxygen concentration is metallurgical rather than electrical. The small concentration of oxygen inhibits grain growth and causes a microcrystalline structure with a significant surface density of individual grains protruding into the thin oxide layer. In polysilicon the grains are much larger, reducing the density of potential contacting points and causing reproducibility and repeatability problems. To maintain a low J_0, recombination at the contacting points should be minimized by making the contacted fraction f of the total area much smaller than 10^{-2}. The specific contact resistance R (in $\Omega\cdot$cm^2) can then be calculated from the spreading resistance [9] of all the point contacts in parallel:

$$R = \frac{\pi}{2} \frac{\rho\alpha}{f} \tag{4}$$

where α is the radius of each individual point contact. It is clear from the proportionality to α that it is better to have many small point contacts than a few large ones. That should result in superior reproducibility which appears to be the main advantage of SIPOS over polysilicon. For reasonable values of f and α the specific contact resistance can be much less than $10^{-6}\ \Omega\cdot$cm^2. Experiments on heterojunction bipolar transistors [10] yield an upper limit of $10^{-4}\ \Omega\cdot$cm^2.

As mentioned earlier, the recombination [8] at accumulated

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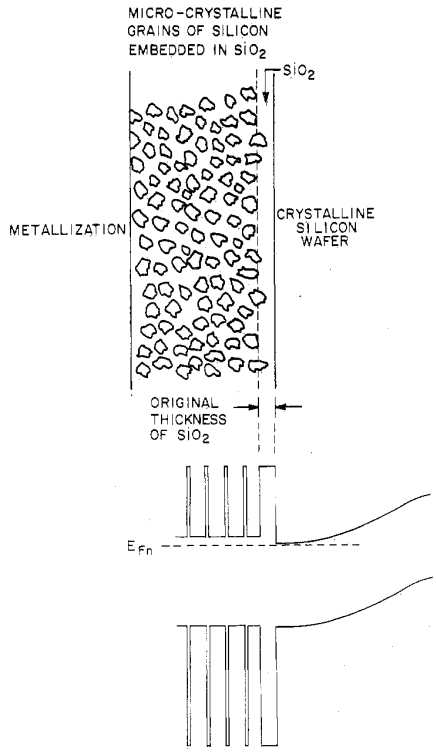

Fig. 2. A model for the metallurgical configuration of the SiPOS:Si heterojunction. Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.

Si–SiO_2 interfaces can be as low as exp $\{qV/kT\} \times 10^{-14}$ Amps/cm^2. To this should be added the diffusion current into the SIPOS at the contact points:

$$J_0^{\text{diff}} = qf \cdot p^s \sqrt{D_s/\tau_s} \tag{5}$$

where p^s, D_s, and τ_s are the SIPOS minority carrier concentration, diffusion constant, and lifetime, respectively. The combination of f, p^s, D_s, τ_s must be such as to result in a total $J_0 \lesssim 10^{-14}$ Amps/cm^2. For this to be the case the SIPOS cannot be a totally inactive material [11], it must have a finite minority carrier lifetime τ_s. In (5) we assumed one-dimensional diffusion. If $\alpha \ll \sqrt{D_s\tau_s}$, then the diffusion would be three-dimensional and (5) would have to be modified somewhat, but the conclusions would be the same.

We see then that the functioning of the n^+ – SIPOS heterojunction shown in Fig. 2 is complex. The individual contacts provide more than enough conductivity for majority carrier electrons, but the small fractional contact area f acts to block minority carrier holes from recombining in the SIPOS. Differential tunneling probability between electrons and holes is probably not playing a major role, since such a process would be very sensitive to oxide thickness contrary to what we observe.

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