



Europäisches Patentamt
European Patent Office
Office européen des brevets



Publication number : **0 457 522 A2**

(12)

EUROPEAN PATENT APPLICATION

(21) Application number : **91304259.4**

(51) Int. Cl.⁵ : **H04N 5/202**

(22) Date of filing : **13.05.91**

(30) Priority : **14.05.90 JP 121236/90**

(43) Date of publication of application :
21.11.91 Bulletin 91/47

(84) Designated Contracting States :
DE FR GB

(71) Applicant : **SONY CORPORATION**
7-35 Kitashinagawa 6-Chome Shinagawa-ku
Tokyo 141 (JP)

(72) Inventor : **Murayama, Hideaki, c/o Patents**
Division

Sony Corporation, 6-7-35, Kitashinagawa
Shinagawa-ku, Tokyo 141 (JP)

Inventor : **Yamamoto, Isamu, c/o Patents**
Division

Sony Corporation, 6-7-35, Kitashinagawa
Shinagawa-ku, Tokyo 141 (JP)

(74) Representative : **Cotter, Ivan John et al**
D. YOUNG & CO. 10 Staple Inn
London WC1V 7RD (GB)

(54) **Gamma correction circuits.**

(57) A gamma correction circuit, that can be used for a video camera having an image pick-up element for generating a video signal corresponding to an object image, and an analog-to-digital converter for converting the video signal generated from the image pick-up element to a corresponding digital video signal, comprises a memory (12) for storing slope data and intercept data of each portion of a polygonal line approximating a desired gamma correction characteristic, a converter (11) for converting the digital video signal to readout address data for the memory, a multiplier (13) for multiplying slope data read out from the memory in accordance with the readout address data by the digital video signal, and an adder (14) for adding intercept data read out from the memory, in accordance with the readout address data, to an output from the multiplier means to generate a gamma corrected output therefrom.

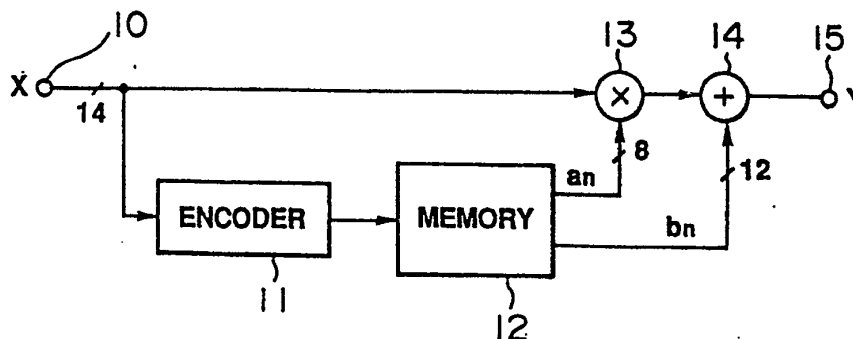


FIG. 3

EP 0 457 522 A2

This invention relates to gamma correction circuits.

The relationship between a grid signal voltage and a luminous output of a colour image receiving tube is not linear. The luminous output is proportional to, for example, 2.2-th power of an input signal applied to the grid. For this reason, if a signal from a video camera is applied to a colour image receiving tube without prior treatment, not only the luminance of an image on the screen, but also the hue and/or saturation, vary to a large degree. To prevent this, prior to applying it to the colour image receiving tube the input signal is passed through a gamma correction circuit having an input/output characteristic such that the output signal is equal to, for example, the 2.2-th power of the input signal, thereby to provide that the overall characteristic is linear. It is possible to position such a gamma correction circuit to process the signal immediately before it is applied to the grid of the colour image receiving tube. However, from the points of view of economy and stability, such a gamma correction circuit is generally not provided in association with a colour image receiver of a domestic electric apparatus. Instead, it is provided on the transmitting side, generally in a video camera.

In recent years, digital video signal processing technology for digitally processing a video signal has been widely used in video cameras, in which case the camera has been provided with a gamma correction circuit constructed as a digital circuit.

For example, it has been proposed to use a so-called mapping system in which a gamma correction characteristic prepared in advance is stored in memory and a gamma corrected digital video signal is read from the memory. More specifically, an output signal level of the input/output characteristic for the gamma correction is stored in advance in the memory and an output signal level is read from the memory by using an input signal level as a readout address for the memory to provide a gamma corrected output signal.

Further, as shown in Figure 1 of the accompanying drawings, for example, it has been proposed to use a gamma correction circuit designed to perform gamma correction using a polygonal line approximating to a desired gamma correction characteristic. More specifically, as shown in Figure 2, an approach is used in which characteristics of respective lines (line segments or portions) forming an approximation to a polygonal line are realised in respective operation circuits I_1 to I_n , comprising multiplier circuits and adder circuits, etc., and outputs from the respective operation circuits I_1 to I_n are compared with each other in a comparison circuit (comparator) 2 to select the minimum value, thereby to provide a gamma corrected digital video signal.

In the above-described gamma correction technique employing the mapping system, it is necessary to store all points on a curve ($Y=X^{1/n}$) representative

of the gamma correction characteristic. As a result, a memory of large capacity is required. A further problem is that, when an approach enabling realising of a high tone to increase the number of bits of a digital video signal is adopted, a memory of larger capacity is required. Particularly in the case of constructing the gamma correction circuit as an integrated circuit (IC), e.g. a so-called gate array, etc., the increased memory capacity is an obstruction. Further, the memory configuration generally employed is a configuration in which 8 bits are taken as one byte for carrying out writing and reading of bytes of data. Accordingly, if the number of bits per sample of a digital video signal is greater than 8, the use efficiency of the memory is poor.

Moreover, in the case of altering the gamma correction characteristic in correspondence with different gamma correction characteristics, for example for different broadcasting stations, the entirety of the memory contents must be rewritten. Since the capacity of the memory is large, it takes a great deal of time to prepare data, to write the prepared data into the memory, and the like.

Further, in the case of the gamma correction circuit as described with reference to Figures 1 and 2, if an attempt is made to increase the number of lines with a view to improving the precision of the polygonal line approximation, the number of operation circuits increases accordingly, resulting in the problem that the circuit scale becomes large. Furthermore, if the number of lines is above a certain value, it is difficult to realise a gamma correction circuit. In addition, it is necessary to alter characteristics (coefficients a_i , b_i : $i = 1$ to n) of all the operation circuits I_1 to I_n in order to vary the gamma correction characteristic. However, this is impossible from a practical point of view.

According to a first aspect of the invention there is provided a gamma correction circuit for a digital video signal, the circuit comprising:

memory means for storing slope data and intercept data of each of a plurality of portions of a polygonal line approximating to a desired gamma correction characteristic;

converter means for converting the digital video signal to readout address data for the memory means;

multiplier means for multiplying slope data, read out from the memory means in accordance with said readout address data, by the digital video signal; and

adder means for adding intercept data read out from the memory means in accordance with said readout address data to an output from the multiplier means to provide a gamma corrected output therefrom.

The gamma correction circuit according to the first aspect of the invention enables a desired gamma correction of a digital video signal to be carried out by

using slope data and intercept data of respective line segments or portions read out from the memory means.

According to a second aspect of the invention there is provided a gamma correction circuit for a digital video signal, the circuit comprising:

memory means for storing level data at each address corresponding to the level of the digital video signal, said level data representing a curve obtained by subtracting the level of said digital video signal from a desired gamma correction characteristic;

converter means for converting said digital video signal to readout address data for the memory means;

multiplier means for multiplying level data read out from the memory means by coefficient data; and

adder means for adding an output from the multiplier means to said digital video signal to generate a gamma corrected output therefrom.

The gamma correction circuit according to the second aspect of the invention allows the gamma correction characteristic to be changed by multiplying the level data read out from the memory means by different suitable coefficient data.

Preferred embodiments of the invention described in detail hereinbelow provide gamma correction circuits which permit the memory capacity to be smaller than that of the prior proposal described above, in carrying out gamma correction of a digital video signal by using a polygonal line approximating to a desired gamma correction characteristic, and thus permit the entire circuit scale to be smaller. Certain of the preferred embodiments permit changing of the gamma correction characteristic with a circuit scale smaller than that of the prior proposal described above.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which:

Figure 1 is a graphical representation of how an approximation to a polygonal line is achieved in a previously proposed gamma characteristic circuit;

Figure 2 is a block diagram of the previously proposed gamma correction circuit;

Figure 3 is a block diagram of a gamma correction circuit according to an embodiment of this invention;

Figure 4 is a graphical representation of a polygonal line achieved when a gamma correction characteristic is subjected to a 32 polygonal line approximation in the gamma correction circuit shown in Figure 3;

Figure 5 is a block diagram of a gamma correction circuit according to another embodiment of this invention;

Figure 6 is a graphical representation of a polygonal line achieved when a curve obtained by

drawing a line represented by $Y=X$ from a gamma correction characteristic is approximated by 32 polygonal lines in the gamma correction circuit shown in Figure 5;

Figure 7 is a block diagram of a gamma correction circuit according to a further embodiment of this invention;

Figure 8 is a graphical representation of a gamma correction characteristic and is used for explaining how gamma correction is achieved by the gamma correction circuit shown in Figure 7;

Figure 9 is a graphical representation of curves obtained by subtracting a line $Y=X$ from the gamma correction characteristic shown in Figure 8; and

Figure 10 is a graphical representation of a gamma correction characteristic when a coefficient K is changed in the gamma correction circuit shown in Figure 7.

Figure 3 shows the configuration of a gamma correction circuit according to an embodiment of the invention. In Figure 3, a digital video signal X provided by converting a video signal from a charge coupled device (CCD) image sensor (hereinafter referred to as a CCD) of, for example, a video camera to a digital signal is supplied to an encoder 11 and to a multiplier circuit 13 from an input terminal 10.

The encoder 11 converts the input digital video signal X to a readout address for a memory circuit 12.

The memory circuit 12 comprises, for example, a random access memory (RAM). In the memory circuit 12, slopes (hereinafter referred to as slope data a_n) and intercepts (hereinafter referred to as intercept data b_n) of respective line segments forming a polygonal line approximating to a gamma correction characteristic, that is a curve represented by $Y=X^{(1/\gamma)}$, are stored. The slope data a_n and the intercept data b_n stored in the memory circuit 12 are read out on the basis of a readout address from the encoder 11. The slope data a_n thus read out are supplied to the multiplier circuit 13, and the intercept data b_n thus read out are supplied to an adder circuit 14.

The multiplier circuit 13 multiplies the input digital video signal X supplied via the input terminal 10 by slope data a_n from the memory circuit 12 and supplies the multiplied result (product) to the adder circuit 14.

The adder circuit 14 adds the output from the multiplier circuit 13 and intercept data b_n from the memory circuit 12 to output the added result (sum), at an output terminal 15, as a gamma corrected digital video signal Y .

Thus, in this embodiment, the memory circuit 12 is used as memory means for storing slope data and intercept data of respective line segments, the encoder 11 is used as address conversion means for converting a level of an input signal to a readout address for the memory circuit 12, the multiplier circuit 13 is used as multiplier means for multiplying slope

data a_n , read out from the memory circuit 12 on the basis of an address from the encoder 11, by an input signal, and the adder circuit 14 is used as adder means for adding intercept data b_n , read out from the memory circuit 12 on the basis of an address from the encoder 11, and the multiplied value (product) from the multiplier circuit 13.

The operation of the gamma correction circuit of Figure 3 will now be described in more detail.

The memory circuit 12 stores, as mentioned above, slope data a_n and intercept data b_n of respective line segments of a polygonal line approximating to the gamma correction characteristic. In more precise terms, as shown in Figure 4, for example: when an input digital video signal X is less than 0% of a so-called reference white level, the gamma correction characteristic is approximated by 1 polygonal line; when that signal X is 0 to 15%, corresponding to the black area where an output signal varies to a large degree, the gamma correction characteristic is approximated by 16 polygonal lines; when that signal X is 15 to 120%, the gamma correction characteristic is approximated by 14 polygonal lines; and when that signal X is more than 120%, the gamma correction characteristic is approximated by 1 polygonal line. Then, slope data a_n (assumed to comprise, for example, 8 bits) and intercept data b_n (assumed to comprise, for example, 12 bits) are stored in the memory circuit 12. Thus, for example, in the case of the above-mentioned 32 polygonal line approximation, the capacity of the memory circuit 12 is equal to 640 (= (8+12) x 32) bits. (As another example, in the case of a 64 polygonal line approximation, the capacity of the memory circuit 12 is equal to 1280 (= (8+12) x 64) bits.)

The encoder 11 converts the input digital video signal X supplied via the input terminal 10 to a readout address for the memory circuit 12. In more precise terms, in the case of the above-mentioned 32 polygonal line approximation: when the input digital video signal X is less than 0% of the reference white level, the input digital video signal X of, for example, 14 bits is converted to one address; when that signal X is 0 to 15%, the input digital video signal X is converted to 16 addresses; when that signal X is 15 to 120%, the input digital video signal X is converted to 14 addresses; and when that signal X is more than 120%, the input digital video signal X is converted to one address. Namely, the input digital video signal X of 14 bits is converted to a readout address of 5 bits in correspondence with the 32 polygonal line approximation. Then, slope data a_n and intercept data b_n read out by using this readout address are supplied to the multiplier circuit 13 and the adder circuit 14, respectively.

The multiplier circuit 13 multiplies the input digital video signal X by the slope data a_n , and the adder circuit 14 adds the output from the multiplier circuit 13

and the intercept data b_n . Thus, a gamma corrected digital video signal Y is outputted from the output terminal 15, the signal Y being given by the equation:

$$Y = a_n \times X + b_n \quad (1).$$

As stated above, slope data a_n and intercept data b_n of respective line segments of a polygonal line approximating to a desired gamma correction characteristic are written in advance into the memory circuit 12. At the encoder 11, the input digital video signal X is converted to a readout address for the memory circuit 12 so that slope data a_n and intercept data b_n are read out from the memory circuit 12 on the basis of the readout address so that the operation expressed by Equation (1) above is performed by the multiplier circuit 13 and the adder circuit 14, thereby providing a gamma corrected digital video signal. In this case, it is unnecessary to store, in the memory circuit 12, data representing respective points on the polygonal line. Thus, for example, in the case of the 32 line polygonal approximation as described above, since it is sufficient to store 32 sets of slope data a_n and intercept data b_n , the capacity of the memory circuit 12 can be reduced. Further, the operation circuit can be constituted by the single multiplier circuit 13 and the single adder circuit 14. Thus, the gamma correction circuit can be realised on a circuit scale smaller than that of the previous proposal described above with reference to Figure 2.

A gamma correction circuit according to another embodiment of this invention is shown in Figure 5.

In Figure 5, an input digital video signal X is supplied to an encoder 21, and to adder circuits 23 and 27, from an input terminal 20.

The encoder 21 converts the input digital video signal X to a readout address for a memory circuit 22 in the same manner as in the embodiment of Figure 3.

The memory circuit 22 may, for example, comprise a RAM. The memory circuit 22 stores data described below for drawing a line represented by $Y=X$ from the gamma correction characteristic, that is the curve represented by $Y=X^{(1/\gamma)}$, to allow the curve thus provided to be subject to polygonal line approximation. Namely, slopes of respective line segments (hereinafter referred to as slope data a_m) of the polygonal line, levels of the input digital video signal X at respective bend points (hereinafter referred to as bend point data X_m), and levels of the polygonal line at the bend point data X_m (hereinafter referred to as intercept data b_m) are stored. The slope data a_m , the intercept data b_m , and the bend point data X_m stored in the memory circuit 22 are read out on the basis of the readout address from the encoder 21. The bend point data X_m thus read out are supplied to a subtraction terminal of the adder circuit 23, the slope data a_m thus read out are supplied to a multiplier circuit 24, and the intercept data b_m are supplied to an adder circuit 25.

The adder circuit 23 subtracts the bend point data X_m from the input digital video signal X supplied from the input terminal 20 and supplies the subtracted result to the multiplier circuit 24.

The multiplier circuit 24 multiplies an output from the adder circuit 23 by slope data a_m from the memory circuit 22 and supplies the multiplied result (product) to the adder circuit 25.

The adder circuit 25 adds an output from the multiplier circuit 24 and intercept data b_m from the memory circuit 22 and supplies the added result (sum) to a multiplier circuit 26.

The multiplier circuit 26 multiplies an output from the adder circuit 25 by a coefficient K for altering the gamma correction characteristic and supplies the multiplied result (product) to the adder circuit 27. The coefficient K is supplied to the multiplier circuit 28 via a terminal 28.

The adder circuit 27 adds an output from the multiplier circuit 26 and the input digital video signal X to output, at an output terminal 29, the added result (sum) as a gamma corrected digital video signal Z .

The operation of the gamma correction circuit of figure 5 will now be described in more detail.

The memory 22 stores, as mentioned above, data described below for drawing a line represented by $Y=X$ from a gamma correction characteristic to allow the curve thereby obtained to be subjected to polygonal line approximation. Namely, slope data a_m of respective line segments of the polygonal line, bend point data X_m of levels of an input digital video signal at respective bend points, and intercept data b_m at bend point data X_m , are stored. In more precise terms, a curve obtained by drawing a line represented by $Y=X$ from the gamma correction characteristic is approximated as shown in Figure 6, for example. Namely: when the input digital video signal X is less than 0% of the reference white level, the above-mentioned curve is approximated by 1 polygonal line; when that signal X is 0 to 15%, the above-mentioned curve is approximated by 16 polygonal lines; when that signal X is 15 to 120%, the above-mentioned curve is approximated by 14 polygonal lines; and when that signal X is more than 120%, the above-mentioned curve signal is approximated by 1 polygonal line. Then, slope data a_m of respective line segments or portions of 32 polygonal lines and assumed to comprise 8 bits, bend point data X_m assumed to comprise 14 bits, and intercept data b_m at respective levels X_m assumed to comprise 11 bits, are stored in the memory circuit 22.

The encoder 21 converts an input digital video signal X to a readout address for the memory circuit 22. In more precise terms, in the case of the 32 polygonal line approximation, an input digital video signal X of, for example, 14 bits is converted to a readout address of 5 bits in correspondence with the 32 polygonal approximation in the same manner as in the

embodiment of Figure 3. Then, bend point data X_m read out by using this readout address are supplied to the adder circuit 23, the slope data a_m similarly read out are supplied to the multiplier circuit 24, and the intercept data b_m similarly read out are supplied to the adder circuit 25.

The adder circuit 23 subtracts the bend point data X_m from the input digital video signal X , the multiplier circuit 24 multiplies an output from the adder circuit 23 by the slope data a_m , the adder circuit 25 adds an output from the multiplier circuit 24 to the intercept data b_m , the multiplier circuit 26 multiplies an output from the adder circuit 25 by the coefficient K supplied via the terminal 28, and the adder circuit 27 adds an output from the multiplier circuit 26 to the input digital video signal X . Thus, a gamma corrected digital video signal Z is outputted from the output terminal 29, the signal Z being given by the equation:

$$Z = (a_m \times (X - X_m) + b_m) \times K + X \quad (2).$$

At the points where the input digital video signal X is 0% and 100%, the value of the first term of Equation (2) becomes equal to zero. Thus, by varying the coefficient K , it is possible to vary the curve of the gamma correction characteristic without changing the gamma correction characteristic at the points where the input digital video signal X is 0% and 100%.

As stated above, slope data a_m , intercept data b_m , and bend point data X_m of respective line segments of a polygonal line approximating to a curve obtained by drawing a line represented by $Y=X$ from the gamma correction characteristic are written in advance in the memory circuit 22. At the encoder 21, the input digital video signal X is converted to a readout address for the memory circuit 22 so that the slope data a_m , the intercept data b_m , and the bend point data X_m are read out from the memory circuit 22 on the basis of this readout address so that the operation expressed by Equation (2) is carried out by the circuits 23 to 27, thereby providing a gamma corrected digital video signal Z . In this case, it is unnecessary to store data representing respective points on the polygonal line in the memory circuit 22. Thus, for example, in the case of the 32 polygonal line approximation as described above, since it is sufficient to store 32 sets of slope data a_m , intercept data b_m , and bend point data X_m , the capacity of the memory circuit 22 can be reduced. Further, the operation circuit can be constituted by the two multiplier circuits 24 and 26 and the three adder circuits 23, 25 and 27. Thus, the gamma correction circuit can be constituted on a circuit scale smaller than that of the prior proposal described above. In addition, the gamma correction characteristic can be altered by altering the coefficient K supplied via the terminal 28.

Further, by subtracting bend point data X_m from the input digital video signal X at the adder circuit 23, the number of bits multiplied at the multiplier circuit 24 can be smaller than that of the embodiment of Figure

3. In addition, since the maximum value of the intercept data b_m of this embodiment is smaller than the maximum value of the intercept data b_n of the embodiment of Figure 3, the number of bits can be smaller than that of the embodiment of Figure 3.

As described above, the gamma correction circuit according to the above embodiments employs an approach of storing advance slope data and intercept data of respective line segments of a polygonal line approximating a desired gamma correction characteristic in a memory means, converting a level of an input signal to a readout address for the memory means in address conversion means, and reading out the slope data and intercept data from the memory means on the basis of this readout address to perform a processing operation at multiplier means and adder means, thereby to provide a gamma corrected digital video signal. Thus, it is unnecessary to write data representing respective points on the polygonal line into the memory means, whereby it is possible to reduce the capacity of the memory means. Further, the circuitry for carrying out the above-mentioned operation can be simply constituted. Thus, the gamma correction circuit can be realised on a circuit scale smaller than that of the prior proposal described above. In other words, it becomes easy to construct the gamma correction circuit as an IC, and the power consumption can be smaller than that of the prior proposal. As a result, the number of line segments forming a polygonal line can be larger than that of the prior proposal, so that it is possible for the precision of the approximation to be high. In addition, by changing values of the slope data and the intercept data stored into the memory means, it is possible to readily cope with diverse gamma correction characteristics, for example in dependence upon broadcasting stations.

A gamma correction circuit according to a further embodiment of this invention is shown in Figure 7.

In Figure 7, a digital video signal X provided by converting a video signal, for example a video signal from a CCD image sensor (hereinafter simply referred to as a CCD) of a video camera, to a digital signal is supplied to a memory circuit 31 and to an adder circuit 33 from an input terminal 30.

The memory circuit 31 comprises, for example, a RAM or a read only memory (ROM). In the memory circuit 31, as shown in Figure 8, values (hereinafter referred to as reference data Δy) on a curve obtained by drawing a line represented by $Y=X$ from a gamma correction characteristic, that is a curve represented by $Y=X^{(1/M)}$, are stored by using the input digital video signal X as a readout address as in the curve indicated by a solid line in Figure 9. Each piece of reference data Δy stored in the memory circuit 31 is read out on the basis of the input digital video signal X. The reference data Δy thus read out are supplied to a multiplier circuit 32.

The multiplier circuit 32 multiplies the reference

data supplied thereto by a coefficient K for altering a gamma correction characteristic and supplies the multiplied result (product) to the adder circuit 33. The coefficient K is supplied to the multiplier circuit 32 via a terminal 34.

The adder circuit 33 adds an output from the multiplier circuit 32 to the input digital video signal X to output, at an output terminal 35, the added result (sum) as a gamma corrected digital video signal Y.

Thus, in this embodiment, the memory circuit 31 is used as memory means for storing each value on the curve obtained by subtracting the line $Y=X$ from the gamma correction characteristic by using the level of an input signal as an address, the multiplier circuit 32 is used as multiplier means for multiplying a value read out from the memory 31 on the basis of the level of the input signal by the coefficient K, and the adder circuit 33 is used as adder means for adding an output from the multiplier circuit 32 to the input signal.

The principle of operation of the gamma correction circuit of Figure 7 will now be described in more detail.

Reference data Δy read out from the memory circuit 31 are zero at the points where the input digital video signal X is 0% and 100%. Thus, by changing the coefficient K supplied via the terminal 34, an output from the multiplier circuit 32 is unchanged at the points where the input digital video signal X is 0% and 100%, and is equal to a value K times larger than the reference data Δy at points except for the above, as indicated by broken line curves in Figure 9. Accordingly, the gamma correction circuit of this embodiment can vary the curve of the gamma correction characteristic without changing the gamma correction characteristic at the points where the input digital video signal X is 0% and 100%, as shown in Figure 10.

As described above, the gamma correction circuit of this embodiment employs an approach of storing, in the memory circuit 31, each value on the curve obtained by subtracting the line $Y=X$ from the gamma correction circuit, that is reference data Δy , multiplying reference data Δy read out from the memory circuit 31 on the basis of the input digital video signal X by the coefficient K in the multiplier circuit 32, and adding an output from the multiplier circuit 32 to the input digital video signal X in the adder circuit 33, thereby permitting changing of the gamma correction characteristic. In addition, since the operation circuit can be constituted by the single multiplier circuit 32 and the signal adder circuit 33, a gamma correction circuit capable of varying the gamma correction characteristic can be constructed on a circuit scale smaller than that of the prior proposal described above.

In other words, the gamma correction circuit according to this embodiment employs an approach of storing, in memory means, each value on the curve

obtained by subtracting the line $Y=X$ from the gamma correction characteristic by using the level of an input signal as an address, multiplying the value read out from the memory means on the basis of the level of the input signal by the coefficient K in multiplier means, and adding an output from the multiplier means to the input signal, thereby permitting changing of the gamma correction characteristic. Moreover, it is sufficient to store in the memory means only one gamma correction characteristic serving as a reference. As a result, the capacity of the memory means can be reduced, and circuitry for carrying out the above-mentioned operation can be simply constituted. Thus, a gamma correction circuit capable of varying the gamma correction characteristic can be realised on a circuit scale smaller than that of the above-described prior proposal. The gamma correction circuit can thus be easily implemented as an IC, and the power consumption can be smaller than that of the prior proposal. Further, by changing the coefficient K , it is possible readily to cope with diverse gamma correction characteristics, for example in dependence upon broadcasting stations.

In addition, polygonal line approximation is implemented by a curve obtained by drawing a line $Y=X$ from the gamma correction characteristic, thereby making it possible further to reduce the capacity of the memory.

Claims

1. A gamma correction circuit for a digital video signal, the circuit comprising:
 - memory means (12; 22) for storing slope data and intercept data of each of a plurality of portions of a polygonal line approximating to a desired gamma correction characteristic;
 - converter means (11; 21) for converting the digital video signal to readout address data for the memory means (12; 22);
 - multiplier means (13; 24) for multiplying slope data, read out from the memory means (12; 22) in accordance with said readout address data, by the digital video signal; and
 - adders means (14; 25) for adding intercept data read out from the memory means (12; 22) in accordance with said readout address data to an output from the multiplier means (13; 24) to provide a gamma corrected output therefrom.
2. A gamma correction circuit according to claim 1, where the memory means (12) stores slope data and intercept data of each portion of 32 polygonal lines, the circuit being so operative that approximation by said 32 polygonal lines is carried out such that: the gamma correction characteristic for an input video signal of less than 0% with respect

to a reference white level is approximated by one polygonal line: the gamma correction characteristic for an input video signal of 0 to 15% with respect to said reference white level is approximated by 16 polygonal lines: the gamma correction characteristic for an input video signal of 15 to 120% with respect to said reference white level is approximated by 14 polygonal lines: and the gamma correction characteristic for an input video signal of more than 120% with respect to said reference white level is approximated by one polygonal line.

3. A gamma correction circuit according to claim 1, wherein slope data, intercept data and bend point data of respective line segments of a polygonal line approximating a correction curve obtained by subtracting the level of a video signal which is not yet gamma-corrected from said gamma correction characteristic are stored in the memory means (22), and wherein the gamma correction circuit comprises subtractor means (23) for subtracting, from said digital video signal, bend point data read out from the memory means (22) in accordance with said readout address data, and supplying the subtracted output to the multiplier means (24), and second adder means (27) for adding the output of the first-mentioned adder means (25) to said digital video signal to output a gamma corrected digital video signal.
4. A gamma correction circuit according to claim 3, which comprises second multiplier means (26) for multiplying the output of the first-mentioned adder means (25) by a coefficient (K) and supplying a multiplied output to the second adder means (27).
5. A gamma correction circuit according to claim 3 or claim 4, wherein the memory means (22) stores slope data, intercept data and bend point data of each portion of 32 polygonal lines, the circuit being so operative that approximation by said 32 polygonal lines is carried out such that: the correction curve for an input video signal of less than 0% with respect to the reference white level is approximated by one polygonal line; the correction curve for an input video signal of 0 to 15% with respect to said reference white level is approximated by 16 polygonal lines; the correction curve for an input video signal of 15 to 120% with respect to said reference white level is approximated by 14 polygonal lines; and the correction curve for an input video signal of more than 120% with respect to said reference white level is approximated by one polygonal line.
6. A gamma correction circuit for a digital video signal, the circuit comprising:

memory means (31) for storing level data at each address corresponding to the level of the digital video signal, said level data representing a curve obtained by subtracting the level of said digital video signal from a desired gamma correction characteristic; 5

converter means for converting said digital video signal to readout address data for the memory means (31);

multiplier means (32) for multiplying level data read out from the memory means (31) by coefficient data; and 10

adder means (33) for adding an output from the multiplier means (32) to said digital video signal to generate a gamma corrected output therefrom. 15

7. A gamma correction circuit for a digital video signal, the circuit comprising:

memory means (31) for storing level data at each address corresponding to the level of the digital video signal, said level data representing a curve obtained by subtracting the level of said digital video signal from a desired gamma correction characteristic; 20 25

multiplier means (32) for multiplying level data read out from the memory means (31) by coefficient data; and

adder means (33) for adding an output from the multiplier means (32) to said digital video signal to generate a gamma corrected output therefrom. 30

8. A gamma correction circuit according to any one of the preceding claims, which is incorporated in a digital video camera having an image pick-up means for generating a video signal corresponding to an object image and analog-to-digital converter means for converting the generated video signal to said digital video signal. 35 40

45

50

55

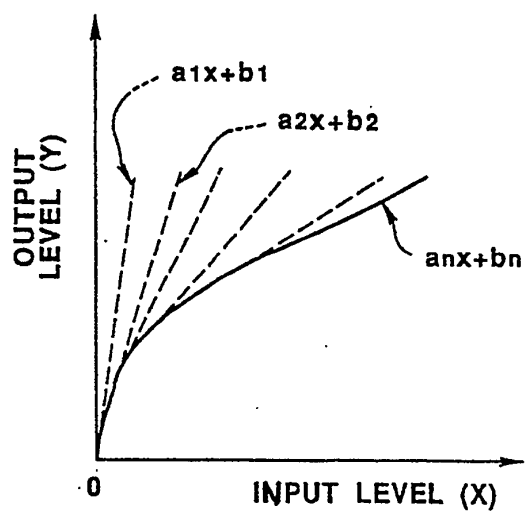


FIG.1

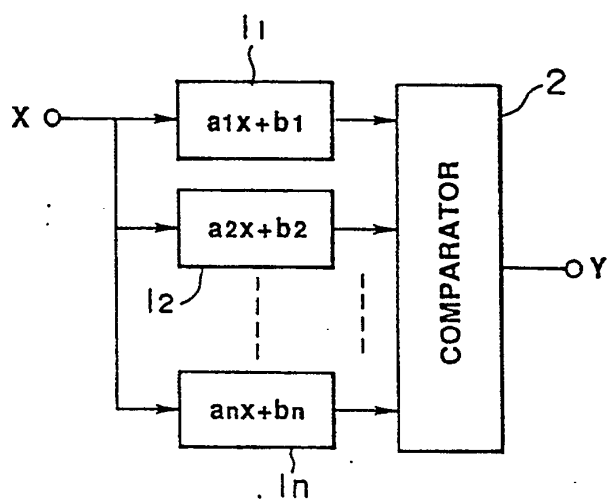


FIG.2

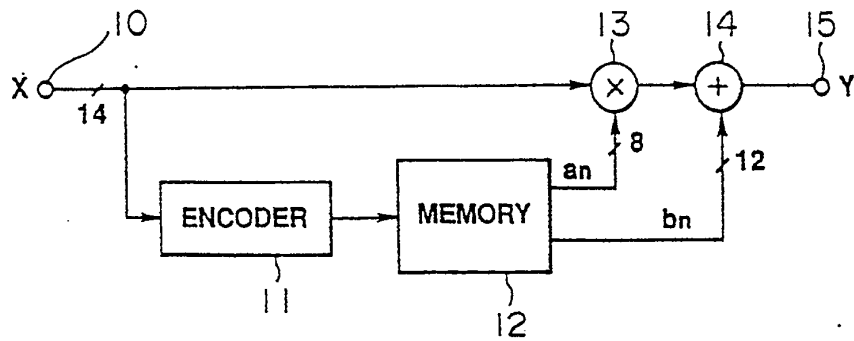


FIG. 3

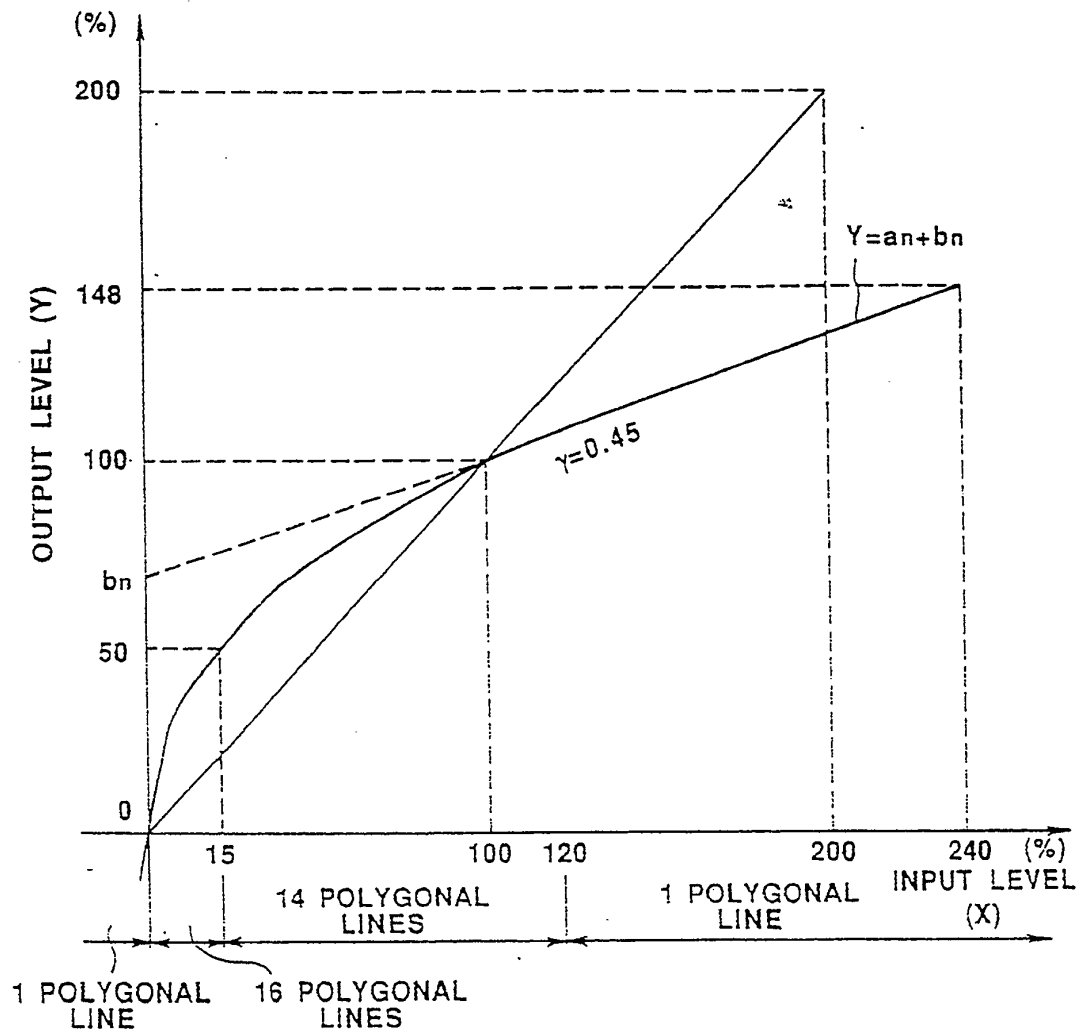


FIG. 4

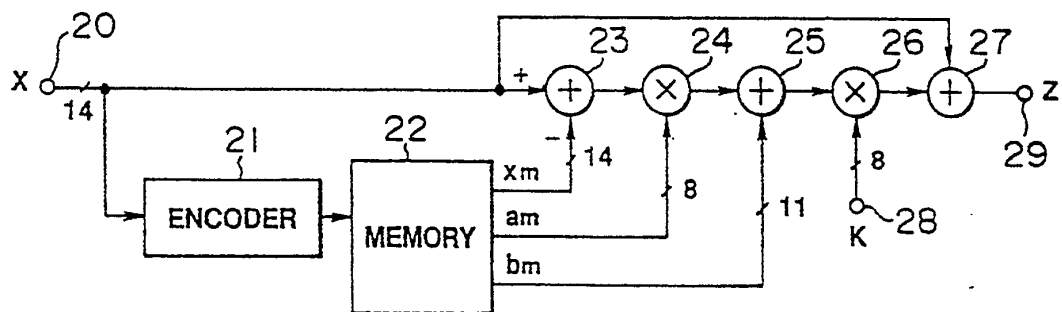


FIG. 5

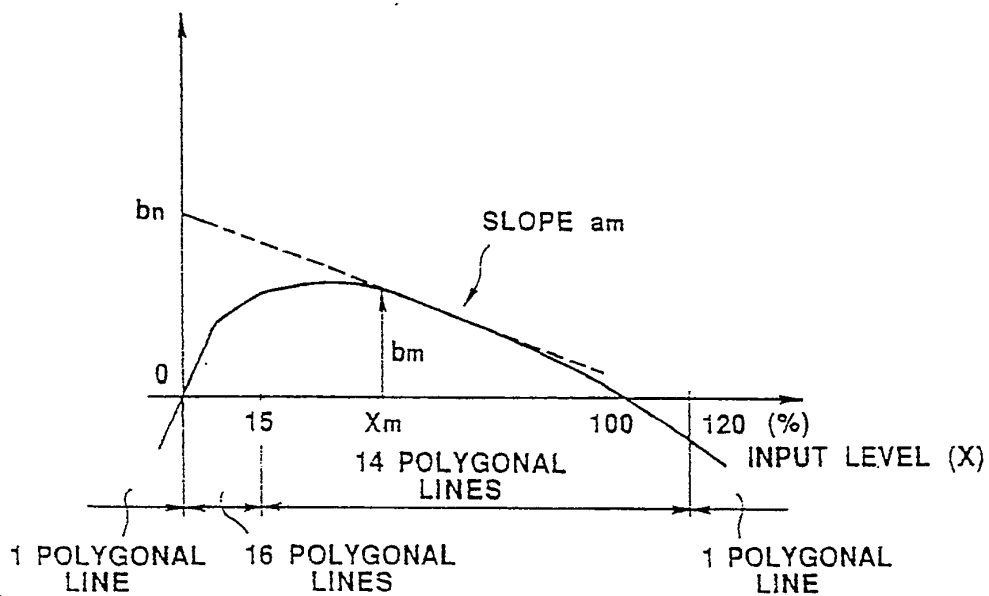


FIG. 6

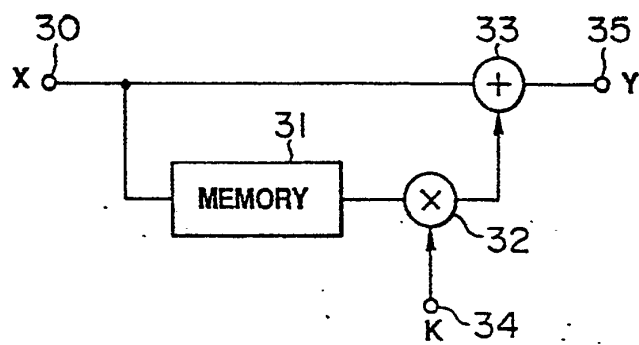


FIG. 7

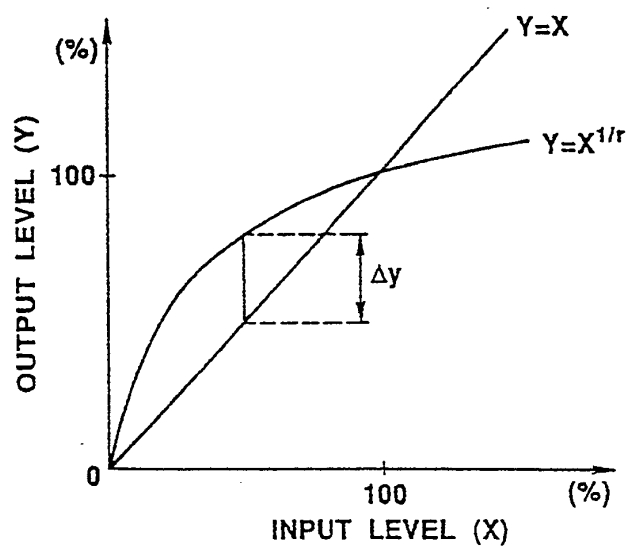


FIG. 8

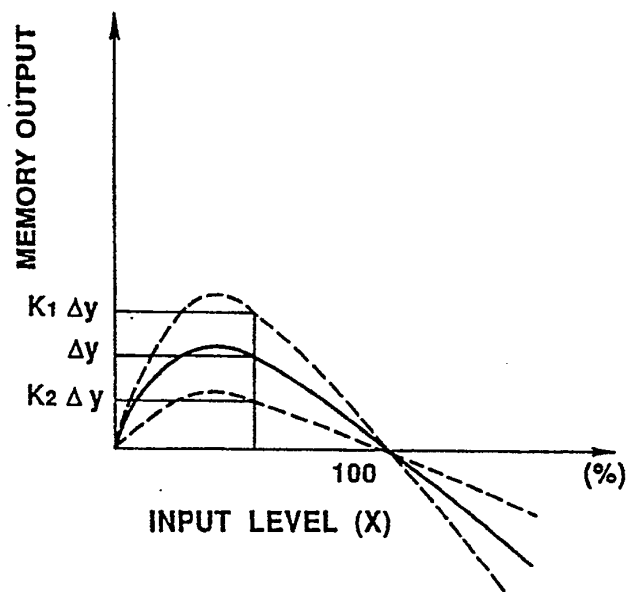


FIG. 9

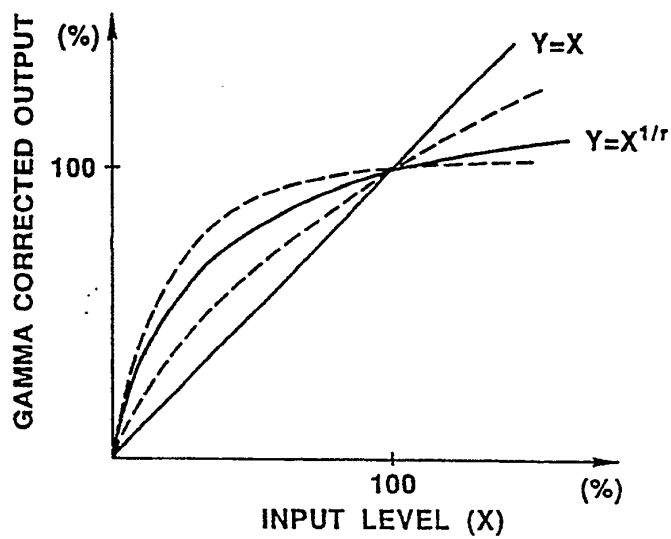


FIG.10