

Digital Subscriber Line technology heralds the age of digital communication, providing a faster, more efficient method of transmitting data over regular telephone lines. The widespread adoption of DSL technology increases the demand for subject-specific, in-depth knowledge of this breakthrough in digital communication. *DSL: Simulation Techniques and Standards Development for Digital Subscriber Line Systems* arms the communications and networking engineer with the quintessential information for implementing DSL systems, including:

- Vital telephone subscriber loop plant structure and engineering conventions
- Detailed analysis of the twisted-pair loop as a broadband communication channel, associated AWG, NEXT, and FEXT noise environments, and corresponding transmission potential known as the channel capacity
- Essential structural analysis and calculations of the analog front-end dynamic range, hybrid circuits, and echo path models
- Reliable simulations for ensuring precision with the analog front end, channel equalization, echo cancellation, error correction coding, and Trellis coded modulation

With this detailed, subject-specific, hard-to-find information from a leader in the DSL industry, the communications and networking engineer will be able to approach DSL system implementation with confidence and professional assurance. *DSL: Simulation Techniques and Standards Development for Digital Subscriber Line Systems* provides field-tested calculations and simulations for the following DSL systems:

- HDSL (High-Bit-Rate Digital Subscriber Lines)
- ADSL (Asymmetrical Digital Subscriber Lines)
- SHDSL (Single-Pair High-Bit-Rate Digital Subscriber Lines)
- VDSL (Very-High-Bit-Rate Digital Subscriber Lines)

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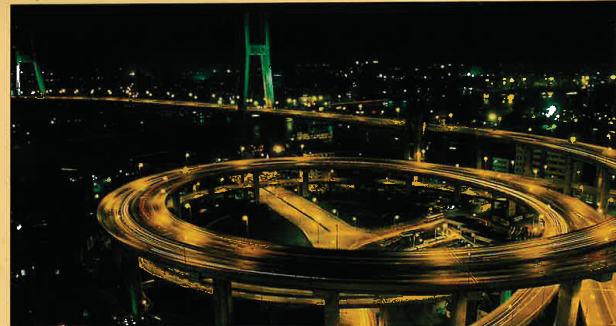
DSL

*Simulation Techniques and Standards
Development for Digital Subscriber
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Dr. Walter Y. Chen

DSL: Simulation Techniques and Standards Development for Digital Subscriber Line Systems

By Dr. Walter Y. Chen

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Dr. Walter Y. Chen was born in Shanghai, China, on September 8, 1956. He received a B.S. (summa cum laude) degree in electrical engineering from the Polytechnic Institute of New York, Brooklyn, in 1982, an M.S. degree in electrical engineering from California Institute of Technology, Pasadena, in 1983, and a Ph.D. in electrical engineering from Polytechnic University of New York in 1989.

From 1982 to 1987, he was a Member of Technical Staff at AT&T Bell Laboratories, where he worked on PBX systems engineering and voice band modem VLSI chip design. From 1987 to 1989, he was a Member of Technical Staff at NYNEX Science and Technology, where he conducted computer network traffic and adaptive signal processing simulation studies. From 1989 to 1995, he was a research scientist at Bellcore, where he was involved with HDSL, ADSL, and HFC modem simulation studies and standards development. From 1995 to 1997, he was a research branch manager at the DSPS R&D Center of Texas Instruments, Inc., for the development of DSL technologies and High-throughput Digital Home Networks.

Dr. Chen is currently with the Information Systems Group of Motorola working on next-generation DSL and Digital Home Network technologies. Since 1989, he has made more than 40 technical contributions at T1E1.4, ADSL Forum, and IEEE 802.14 standards committees. His main research interest is the application of circuit and system theories to the area of advanced digital communication. He holds four U.S. patents and has several others pending.

Dedication

To Aaron and Brian, and to Nancy and our parents.

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Introduction

When telecommunication was first invented as a telegraph, letters were coded in binary form: a combination of dots and dashes, as specified by the Morse code. In some sense, early telegraph was a digital system. The later invention of the telephone made the most popular telecommunication means into the analog format. Today, most telephone subscriber loops are still in analog format for the sole purpose of carrying analog telephone services.

Nonetheless, the *Public Switched Telephone Network* (PSTN) is dominated by digital technologies. High-speed digital transmission links between different telephone Central Offices (COs) are capable of multiplexing and concentrating local traffic according to the digital hierarchy with a minimum number of physical cable connections. A flexible digital network also is efficient at carrying new feature services, delivering information other than voice signals.

With the advanced development of computer and consumer electronics, traditional telephone subscribers are ready for new services based on digital technologies. There is a lot of useful information, such as news, weather, and stock prices, on the Internet. As a result of this new information channel, there will be a stronger need by consumers to access the Internet for telecommunication, shopping, and "infotainment." There are some digital information appliances, such as PCs, satellite receivers, and digital audio/video recorders, in the home already. When the digital television technology becomes a reality, the average household will be more digitally oriented.

Along with the digitization of public and private information and of consumer electronics, the amount of information associated with their applications has been drastically increased. First-generation PCs had a RAM size of 256KB and a hard disk drive of 20MB. Now, a consumer-grade PC has 16MB of RAM and a hard disk drive of 1GB. During the last 15

years, the PC memory and storage size increase factors have been about 62.5 and 50, respectively; however, the increase of transmission throughput for a voice band modem, which has become a popular PC communication device, is only about a factor of 14–33.4 kbps vs. 2.4 kbps.

With a much more powerful PC processing lots of information, the capability of a voice band modem, which is limited by the 3.3 kHz voice channel, becomes a limiting factor in integrating consumers to the evolving high-speed digital communication network. The drawback of a voice band modem can be overcome with the *Digital Subscriber Line* (DSL) technology. By bypassing the *Plain Old Telephone Set* (POTS) interface at a local CO, a DSL system can utilize the full potential of a copper telephone subscriber loop to deliver a transmission throughput of up to a few hundred times that of a voice band modem.

1.1 Digital Access Methods Through POTS Loops

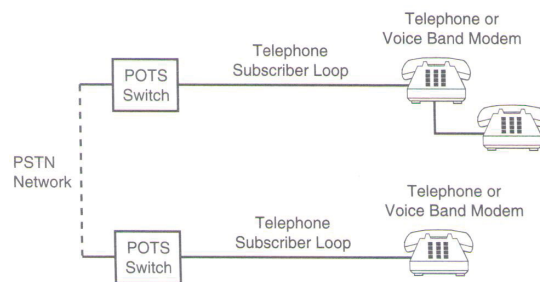
Currently, there are three ways to provide digital access through a telephone subscriber loop:

- Analog voice channel
- Digital switches
- POTS splitters

1.1.1 Digital Access Through Analog Voice Channels

Figure 1.1 shows the first approach of providing digital transmission through the existing POTS switch and PSTN network.

Figure 1.1 Digital Access Through an Analog Voice Channel



1.4.5 VDSL System Standards

To meet the demand of future all-purpose multimedia applications, Very-high-bit-rate Digital Subscriber Line (VDSL) has been under study since late 1995 for transmission throughputs of 13, 26, and 52 Mbps. The VDSL service range is expected to be between 1.5 to 4.5 kft. VDSL customers will be connected by short-distance copper twisted-pair loops to nearby *Optical Network Units* (ONUs) that are linked to a CO with fiber optical cables.

The VDSL transmit spectrum can occupy a bandwidth of up to 15 MHz where the Radio Frequency Interference (RFI), both ingress and egress, has become a chief concern. Under such a high transmission throughput, the requirement of delivering desired analog and digital semiconductor capabilities under a consumer product cost constraint becomes an incentive for VDSL system developers.

1.5 Chapter-by-Chapter Overview

This book is a collection of simulation/implementation techniques and reference materials for the design and development of DSL systems. It is intended for practicing engineers working in DSL and related fields. Many techniques developed for DSLs can be very useful also for next-generation communication systems, such as a high-throughput home digital network. This book also can be used as a reference for graduate students to aid in their research studies in digital communication systems.

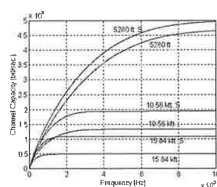
Note

Past technical contributions of the T1E1.4 working group can be obtained from Creative Communications Consulting, P.O. Box 15189, Durham, NC 27704; telephone: 732-842-6250.

This book is divided into two parts: Part I, "Fundamentals: Transmission Environment and Signal Processing," and Part II, "DSL Systems: System and Transceiver Architectures." Part I deals with twisted-pair telephone loop channel modeling, DSL system performance simulation, and the general implementation of digital signal processing techniques. The transmission performance potential of telephone subscriber loops are examined through the calculation of channel capacity. Adaptive channel equalization, adaptive echo cancellation, and coding techniques are addressed with an emphasis on DSL-specific implementation details.

Part II deals with the specifics of developed and developing DSL systems. For each developed DSL system, initial and major standard development activities, general system performance characteristics, and key features of standard documents are discussed. The general features and related issues for developing DSL systems also are discussed. ANSI T1D1.3 and T1E1.4 working group contributions are extensively referenced.

Figure 5.13 NEXT Channel Capacity with 6 dB Noise Margin



Therefore, the channel capacities of a 5280 ft. 26-gauge simplified channel model are equivalent to those of a 8448 ft. 22-gauge simplified channel model. Similarly, you have

$$d_{24} = d_{26} \frac{k_{1,26}}{k_{1,24}} = d_{26} \frac{4.8}{3.8} = 1.26 d_{26}$$

in which the simplified channel models are as follows for 26-gauge and 24-gauge twisted-pair cables, respectively:

$$H(d, f) = e^{-d(k_{1,26}\sqrt{f} + k_{2,26}f)}$$

$$H(d, f) = e^{-d(k_{1,24}\sqrt{f} + k_{2,24}f)}$$

This means that the channel capacities of a 5280 ft. 26-gauge simplified channel model is equivalent to those of a 6669 ft. 24-gauge simplified channel model.

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CHAPTER

6

Hybrid Circuits

For half-duplex telegraphs of early days, transmission was carried out only in one direction over one pair of two-wire cables at a given time. The transmission direction can be regulated through some handshake protocol whenever a transceiver at one end has data to transmit. The transmission direction can also be time divided: transceivers at both ends are synchronized and take turns transmitting. This is sometimes called *Time Division Multiplex* (TDM) or *Time Division Duplex* (TDD), respectively. For a telephone conversation, a real-time, full-duplex system, in which telephone subscribers at both ends can talk and listen simultaneously, is preferred to emulate a more natural situation.

Real-time, full-duplex transmission of voice signals can be accomplished using a hybrid circuit, which connects a microphone and an earphone to a two-wire telephone subscriber loop. A hybrid circuit is basically an electrical bridge. There is little signal from the transmit path coming back to the receiving path when the electrical bridge is balanced. The balance condition, however, requires the impedance match to the telephone subscriber loop. This condition cannot really be satisfied because the input impedance of a telephone loop is not exactly fixed, due to bridged taps and temperature variation.

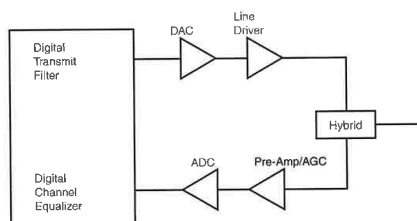
This small amount of impedance mismatch is tolerable for voice applications. In fact, the echo, which is caused by impedance mismatch of a hybrid circuit, of someone's own talk is usually perceived as an "alive" indication for a telephone connection.

For real-time, full-duplex data transmission applications, the amount of hybrid echo should be minimized; otherwise, the echo could interfere with the received signal. Although some telephone set hybrid circuits rely on voltage parities from different windings of one or two magnetic cores to cancel the transmit signal, hybrid circuits used for DSL systems are based on the balance of resistive networks to minimize the amount of echo.

DSL transceivers typically consist of both a single-ended and a differential hybrid circuit. Both circuits can be simplified to some resistive networks. DSL hybrid circuits also usually have a coupling transformer, which is mainly used for the purpose of longitudinal signal isolation and surge protection. Both wires of a telephone loop can pick up some substantial noises through the open electromagnetic field; however, the only difference between these two longitudinal signals appears after a transformer. A coupling transformer can also reduce the severity of some longitudinal surge voltage or current.

Because a hybrid is an analog circuit, it is connected to the rest of a DSL transceiver through a *Digital to Analog Converter* (DAC) in the transmitting path and an *Analog to Digital Converter* (ADC) in the receiving path. Figure 6.1 shows the typical structure of an *Analog Front End* (AFE) that connects the digital portion of a DSL transceiver to the telephone subscriber.

Figure 6.1 The General Structure of an Analog Front End



The transmit signal to a DAC is usually coming from digital transmit shaping filters, and the received signal from an ADC usually goes to channel equalizers. A hybrid circuit can provide some limited amount of transmission loss from the transmitting path to the receiving path, depending on the impedance balance condition. There is usually a line drive between the DAC and the hybrid circuit for supplying sufficient voltage and current onto the twisted-pair loop with certain line impedance.

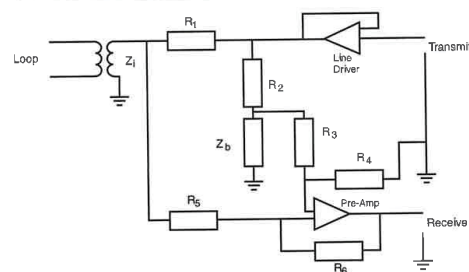
There is usually also a pre-amplifier with automatic gain control between the hybrid circuit and the ADC to raise the received signal level to that suitable for the input dynamic range of the ADC. There are typically two types of hybrid circuits used for Digital Subscriber Line (DSL) transceivers: single-ended hybrid circuits and differential hybrid circuits. This chapter explains the structure, functionality, and components of these two types of hybrid circuits and related concepts, as follows:

- **Single-ended hybrid circuits.** Single-ended hybrid circuits can be simplified into a classical electrical bridge with four branches. The transmitting path and the receiving path are connected at two diagonal ports, while the twisted-pair telephone loop is used as one of these branches through the coupling transformer.
- **Differential hybrid circuits.** Differential hybrid circuits can be simplified into a balance circuit of six resistors with six joints. The transmitting path, the receiving path, and the twisted-pair telephone loop are cross-connected through a coupling transformer to six joints of this balance network. A differential hybrid circuit is suitable for using a differential line driver.
- **Transformer equivalent circuits.** A line coupling transformer can be represented with a T-equivalent circuit for transformer design and system performance analysis. The ABCD parameters of the transformer equivalent circuit are also derived to be used in conjunction with ABCD parameters of the twisted-pair telephone subscriber loop.
- **Echo path model.** A realistic echo path model can be obtained by combining the equivalent circuit of the line coupling transformer, the balance network, and the input impedance of the loop. The echo path model can be used to assess the echo level and as a reference for the design of an echo canceller.

6.1 Single-Ended Hybrid Circuits

Figure 6.2 shows a single-ended hybrid circuit.

Figure 6.2 Single-Ended Hybrid Circuit



Channel Equalization

The usable bandwidth of a twisted-pair telephone subscriber loop is much wider than the voice band telephony channel; however, the channel distortion is also more severe for using the full available bandwidth. Specifically, amplitude attenuation and phase delay could be very different at different frequency regions within the available bandwidth. A transmitting signal could become unrecognizable after going through a telephone subscriber loop because of the amplitude and phase distortion. The channel capacity estimation in the frequency domain only indicates the transmission potential of the telephone subscriber loop—but does not reveal any method of achieving that.

An information bit stream is usually converted into a sequence of data symbols. The transmission throughput is the product of the symbol rate and the number of bits carried by every data symbol. The faster the symbol rate, the higher the transmission throughput; however, the symbol rate is limited by the channel amplitude and phase distortion. Specifically, the channel distortion causes the data symbols to spread. Therefore, there are certain limitations to how close symbols can be lined up next to each other without the use of any channel distortion compensation technique.

The effect of channel distortion can be minimized using a channel equalizer, which can be used to control the spread of the data symbol after going through the channel. Dividing the available bandwidth into many smaller frequency regions where channel distortion becomes relatively insignificant also can minimize the effect of channel distortion. A channel equalizer also can be very useful even for the bandwidth divided DSL systems.

In theory, an equalizer should have a frequency response that is the inverse of the channel. In practice, a channel equalizer is normally implemented with a digital adaptive filter. An adaptive channel equalizer can be further categorized as linear or decision feedback, baud

rate or fractionally spaced, baseband or passband (depending on performance requirement), signal processing capability, and system architecture.

The development of the adaptive channel equalization technique has helped the evolution of the voice band modem technology. The adaptive channel equalization technique has also been successfully used for DSL systems to realize the transmission throughput potential available over the telephone subscriber loops. Equalizer coefficients and equalizer output signal-to-noise ratio (SNR) can characterize the implementation requirement and the effectiveness of an adaptive channel equalizer. Equalizer coefficients and output SNR can be obtained iteratively through the simulation of the adaptation process or directly through some matrix calculation in conjunction with channel and noise models.

This chapter addresses issues related to the determination of equalizer coefficients and equalizer output SNR, based on the matrix calculation method. Detailed results are derived for the following equalizer configurations:

- *Adaptive Linear Channel Equalizer*. Concepts of channel equalization and adaptive filtering are discussed. Baud rate and fractionally spaced linear equalizer coefficients and equalizer output SNRs are calculated. The issue of noise enhancement is also addressed.
- *Decision Feedback Channel Equalizer (DFE)*. DFE equalizer coefficients and equalizer output SNRs are calculated for baud rate and fractionally spaced *feed forward filters* (FFF). The Tomlinson/Harashima precoding method is also introduced.
- *Passband Equalizer and Carrierless AM/PM (CAP)*. Equalizer coefficients and output SNRs are calculated for the passband *Quadrature Amplitude Modulation* (QAM) system. A linear equalizer or the FFF of a DFE can be placed before or after the demodulation process. Linear equalizer and DFE structures for a CAP system are derived. Equalizer coefficients and equalizer output SNRs are also calculated for a CAP system.
- *Equalizer for Discrete MultiTone (DMT) Systems*. The concept of *intersymbol interference* for a DMT system is introduced. Equalizer coefficients and equalizer output SNRs are calculated for a DMT system based on the *Minimum Mean Square Error* (MMSE) criteria.

8.1 Adaptive Linear Channel Equalization

A channel equalizer can be used to minimize the effect of channel distortion; however, every twisted-pair loop has its own unique transmission characteristics due to the composition and the configuration of that particular loop. Furthermore, the transmission characteristics of a twisted-pair loop is slightly time varying and temperature dependent.

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ADSL (Asymmetrical Digital Subscriber Lines)

The desire for the further advancement of telephone subscriber loop-based DSL technology was very strong after the initial definition of the dual-duplex HDSL as a repeaterless T1 technology. The performance improvement of HDSL was partially due to its broader signaling bandwidth compared with that of DSL. Therefore, the next DSL technology after HDSL should utilize more bandwidth than that used by HDSL.

On the other hand, the NEXT noise could have made the telephone subscriber loop channel useless beyond the frequency band of HDSL even at CSA range. The only possibility to further expand the usable bandwidth is to avoid the NEXT noise by adopting one directional transmission among all telephone subscriber loops.

Consumer broadband services that could benefit from DSL technologies had been considered video oriented. Video telephony was a candidate, but its market potential was questionable based on previous attempts. The video-on-demand service had been considered as a telephone company's response to video rental and cable television pay-per-view markets. The video-on-demand service can be provided through a T1 rate (1.544 Mbps) DSL system in conjunction with a digital video compression technique, such as MPEG1 from a CO to a telephone subscriber. In the reverse direction, only a lower throughput channel is necessary to send ordering information as well as real-time control commands similar to that of a VCR.

Asymmetrical Digital Subscriber Lines (ADSL) were originally developed for such a video-on-demand service with a downstream (from a CO to a subscriber) transmission throughput of 1.544 Mbps and an upstream (from a subscriber to a CO) transmission throughput of between 16 and 64 kbps. With ADSL, one compressed video channel can be provided to all consumers connected with nonloaded telephone subscriber loops. At CSA range, up to four

compressed video channels can be provided. Meanwhile, Trellis and forward error correction coding techniques had been introduced in conjunction with the Discrete MultiTone (DMT) line code to improve the transmission performance under the crosstalk and impulse noise environment.

Most recently, ADSL has been considered as the next-generation transmission technology for high-speed data access applications. The ever increasing population of home PCs and the widespread use of the Internet create a demand for a higher access speed than what a voice band modem can provide. Because of the random nature of data communication and corresponding transmission protocol, some ADSL transmission overhead designed for multiple video channels can be simplified. The adoption of an ATM-oriented transmission interface is another flexible approach to make ADSL technology suitable for different applications.

This chapter covers development activities, line codes, transmission performances, and interface standards of Asymmetrical Digital Subscriber Lines, including the following:

- *Development of ADSL technology.* Technical discussions leading to the development of ADSL are reviewed. Early performance measurements on prototype ADSL systems and in conjunction with a POTS service are presented.
- *ADSL transceiver structures and line codes.* For the ADSL standard defined by T1.413, the general ADSL transceiver architecture and issues, such as TEQ, FEQ, and sub-carrier SNR, are discussed. Transmission parameters for both downstream and upstream directions are summarized. ADSL specific techniques including Trellis coding, Reed-Solomon coding, interleaving, and asymmetric echo cancellation are reviewed. Implementation strategy, requirement, and complexity are addressed with respect to digital interface, digital signal processing, and analog interface functional blocks for both CO and subscriber side transceivers. Transceiver structures, transmission parameters, specifics of transmit filter and equalizer coefficients, and possible implementation approaches are also discussed for CAP line code ADSL.
- *ADSL performance objectives.* An additional six ADSL mid-CSA test loop configurations and corresponding transfer functions as well as three noise models with combined NEXT, FEXT, and AWG noises are presented. DMT ADSL transmission performances are simulated for three different ranges of test loops with associated noise conditions. Transmission performances of CAP ADSL are also estimated.
- *ADSL network and premises interfaces.* ADSL network interface at a CO or a RT for providing video on demand services is discussed. Associated ADSL multi-channel specifications are reviewed. ADSL network interface for providing data access services is also

discussed. The function and the design of POTS splitter is addressed. Possible approaches of POTS splitter installation in conjunction with existing telephone in-house wiring are presented.

- *ADSL standards.* Key features of ADSL defined by ANSI T1.413, such as frame/super-frame structure, channelization, bit-to-constellation mapping, and initialization procedures, are discussed.

13.1 Development of ADSL Technology

The development of HDSL is relatively straightforward. Based on experience gained from DSL development, people involved felt that the same signal processing and *Very-Large-Scale Integrated circuit* (VLSI) technologies could be enhanced for a higher transmission throughput. The next logical step of higher throughput is the T1 rate: 24 B channels at a rate of 1.544 Mbps. Computer performance simulation studies indicated that two pairs of cables were required.

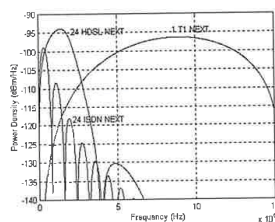
After the demonstration of the prototype VLSI chip, the echo cancellation-based 2B1Q line code was selected for HDSL. HDSL then found an application as the dual-duplex repeater-less T1 technology. To avoid the lengthy standardization process experience of DSL, it was decided that a technical report by the T1E1.4 working group would be sufficient to guide HDSL vendors for the compliance of interoperability.

During these performance studies, two other line codes—Carrierless AM/PM (CAP) and Discrete MultiTone (DMT)—were also proposed as alternatives. Due to the lack of understanding of these alternative line codes by the majority of standards activity participants, these line codes were not favored for HDSL. Due to persistent efforts of their proponents as well as the availability of corresponding tutorial material, however, the T1E1.4 working group recognized the potential of using CAP and DMT line codes for the next generation of higher throughput DSL systems. The early market acceptance of HDSL by the business community further enhanced the desire for the development of a higher throughput digital subscriber line system for the mass consumer market.

HDSL is somewhat restrictive for residential services.¹ The need for two pairs and the CSA range limitation may prove prohibitive in certain areas where a significant portion of customers are beyond 12 kft or where the number of pairs-per-living unit are less than two. Thus, the genesis for the next generation of high throughput DSL systems was to design a new transport access capability to provide economic wideband services directly to the residential customer. Objectives are to cover most of the nonloaded loop plant out to 18 kft, as is the case for Basic Rate Access. In addition, it is highly desirable to reduce the number of pairs required because pairs-per-living unit ratios can be as low as 1.3 in some areas.

Although intended for the residential market, the higher throughput DSL system under consideration then needed to co-exist with early developed DSL and HDSL systems. To be conservative, the co-existence with T1 lines using the traditional transceiver technology also needed to be considered. In other words, the system under consideration then needed to operate with DSL, HDSL, and T1 NEXT. The level of crosstalk noise depends on the number of disturbers. A point of contention is that in a residential environment, the number of deployed HDSLs might be smaller. According to Figure 13.1, the new system under development could have a transmit spectrum above that of HDSL to realize the full potential of the available bandwidth of the copper loop plant.

Figure 13.1 Noise Environment with DSL, HDSL, and T1



Observing that many services needed greater transmission rates from the central office to the customer than in the other direction, Dr. Joseph Lechleider proposed the idea of asymmetrical DSLs (ADSL).² Adding asymmetry to a DSL system opened a new dimension to be considered with system configuration. Lechleider mainly considered 18 kft range, 2B+D full duplex, and 1.544 Mbps downstream; CSA range, 2B+D full duplex, and 3.088 Mbps downstream; and 5 kft range, 1.544 Mbps upstream, and 6.176 Mbps downstream single pair as well as a few other dual-pair ADSL options.

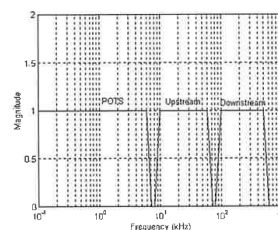
For the first two options, Lechleider assumed a unilateral downstream channel occupying a frequency band above 75 kHz in addition to DSL. For the third option, Lechleider assumed a unilateral downstream channel occupying a frequency band above 425 kHz in addition to a double baud rate HDSL. The higher transmission throughput of unilateral channels are possible because they are limited only by effect of Far End Crosstalk (FEXT).

This concept of ADSL fits the concept of a video-on-demand service provided through the existing copper loop plant very well. The CCITT H.261 recommendation and the ISO Moving Picture Experts Group (MPEG) recommendation both provide full-motion video at rates of around 1.3 Mbps. The video, an audio channel, and associated overhead can be transmitted within a 1.5 Mbps signal. Users could signal the network, scan archives of programming, and receive video-on-demand. For this service, only a low transmission throughput upstream control channel is necessary to send back control signals for interactive commands, such as Pause and Play.

The concept of ADSL also fits applications, such as network computing where software and database records could be stored on network servers and retrieved at a speed equivalent to the CD-ROM and tele-education where a specialist can be shared with a large student population through downstream channels and individual feedback can be provided through upstream channels. It was realized that for residential applications, a POTS service—with which the traditional telephone service can be provided regardless of whether the ADSL was on or off—was more practical than the ISDN service.

After sharing ideas among Bellcore, regional Bell operating companies, and other industry and academic leading ADSL proponents, ADSL was proposed as having the traditional duplex POTS channels, occupying the frequency band between 300 Hz and 4 kHz, an upstream control channel of 16–64 kbps, occupying the frequency band between 10 kHz to 50 kHz, and a downstream channel of 1.544 Mbps, occupying the frequency band of 100 kHz–500 kHz. Figure 13.2 shows the initial frequency spectra for ADSL technology.

Figure 13.2 Initial ADSL Frequency Spectra



13.1.1 Convergence of Initial Ideas on ADSL

The discussion about ADSL at T1E1.4 working group was not started until after the proposal of a new study project about ADSL by U.S. West during the May 1991 meeting.³ During the August 1991 T1E1.4 meeting, the performance of a QAM ADSL was studied in conjunction with DSL NEXT,^{4,5} 18 test loops were proposed for ADSL,⁶ the effect of impulse noise was examined,⁷ and the performance of a multi-carrier system, DMT, was compared with that of a single-carrier system, QAM.⁸

During the November 1991 T1E1.4 meeting, performance of DMT was further discussed,^{9,10,11} the nature of burst error was discussed,¹² the forward error correction code was proposed for ADSL,^{13,14} the feasibility of an ADSL control channel was discussed,¹⁵ and the use of Trellis code for ADSL was discussed.¹⁶

During the February 1992 T1E1.4 meeting, the similarity between CAP and QAM was explored,¹⁷ and the performances of DMT and QAM were further studied.^{18,19,20,21} During the May 1992 T1E1.4 meeting, ADSL system issues—ranging from interfaces to frame format—were discussed,^{22,23,24,25,26,27,28} a QAM ADSL including a control channel was discussed for spectrum compatibility with other DSLs,^{29,30} the ADSL Radio Frequency Interference (RFI) was discussed,³¹ the POTS-generated impulse noise was discussed,³² a performance test plan for ADSL “Olympics,” was presented,³³ and the A/D precision issue was discussed.³⁴ The possibility of having an ADSL standard project was also discussed.^{35,36}

During the August 1992 T1E1.4 meeting, the possibility of a baseband ADSL was discussed,³⁷ the idea of asymmetrical echo cancellation was discussed,³⁸ the idea of impulse noise cancellation was discussed,³⁹ the design issues of a CAP ADSL were discussed,^{40,41} milestones of the ADSL standard were proposed,⁴² possible ADSL interfaces were discussed,⁴³ the ADSL “Olympic” test plan was further discussed in more detail,^{44,45,46} ADSL spectral compatibility was further discussed in more detail,^{47,48} the possibility of an ADSL with embedded ISDN was discussed,⁴⁹ and ADSL coding and interleaving issues were further discussed.^{50, 51,52,53}

During the December 1992 T1E1.4 meeting, test plans were further discussed,^{54,55} Trellis coding and forward error correction coding for ADSL were discussed,^{56,57,58,59} the issue of impulse noise was discussed,^{60,61,62} the idea of an analytical testbed was proposed,⁶³ the design of a DMT transceiver was discussed,⁶⁴ the possibility of providing multiple 1.544 Mbps rates was discussed,^{65,66,67} the DMT echo canceller structure was discussed,⁶⁸ the spectrum compatibility between ADSL and other DSLs was examined,^{69,70} ADSL frame structure and maintenance issues were further discussed,^{71,72} and possibilities of including POTS and ISDN were discussed.⁷³

During the March 1993 T1E1.4 meeting, the issue of selecting forward error correction code was further discussed,^{74,75,76} implementation details of the DMT ADSL were discussed,^{77,78,79,80} inclusion and alternatives of providing 6 Mbps were discussed,^{81,82} the effect of ADSL spectrum on T1 performance was discussed,⁸³ and performance measurements of ADSL prototypes were reported by Northern Telecom, Inc.⁸⁴ and Bellcore.^{85,86,87,88} NTI measurements showed positive performance margins for self-FEXT (see Figure 13.3), 49-disturber ISDN NEXT (see Figure 13.4), and 24-disturber HDSL NEXT (see Figure 13.5). No error was observed when a POTS operation was performed on the same test loop.

Figure 13.3 NTI Self-FEXT Margin

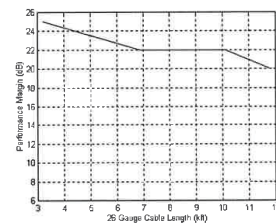


Figure 13.4 NTI 49 ISDN NEXT Margin

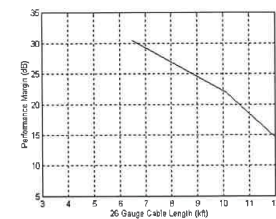
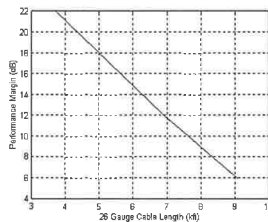


Figure 13.5 NTI 24 HDSL NEXT Margin



Bellcore ADSL "Olympic" test measurements, summarized in Table 13.1, showed Amati's ADSL prototype in the first place, Reliance/Bellcore's ADSL prototype in the second, and AT&T Paradyne's ADSL prototype in the third. The operation of the POTS sharing the same test loop also was verified for Reliance/Bellcore and Amati prototypes. Little disturbance was observed. Amati's ADSL prototype had forward error correction code. Based on these test measurements, DMT line code was selected as the ADSL standard also based on the fact that Amati's prototype could operate at 6 Mbps in addition to 1.5 Mbps.

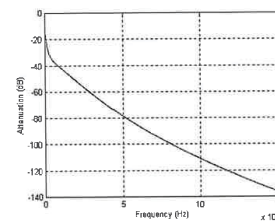
Table 13.1 Bellcore ADSL "Olympic" Test Results

Loop Number	Disturbers	Reliance/Bellcore	Amati 21 dBm	Amati 16 dBm	AT&T
ADSL #4	24-DSL	-6	8	4	Not work
ADSL #6	24-DSL	<-8	7	3	Not work
ADSL #9	24-DSL	7	>16	>16	Not work
ADSL #17	24-DSL	1	15	10	Not work
CSA #2	24-HDSL	>11	>11	>11	<-8
CSA #6	24-HDSL	5	>11	>11	-8
CSA #7	24-HDSL	>11	>11	>11	-1
CSA #2	1-T1	7	>10	>10	<0
CSA #6	1-T1	2	>10	8	<0
CSA #7	1-T1	8	>10	>10	-2

13.1.2 Concerns for POTS Interference

The feasibility of ADSL with a POTS service was established by the aforementioned prototype efforts and verified by laboratory measurements. The most obvious transmission challenge associated with the ADSL was the high level of signal loss at the extreme range of the nonloaded loop plant. Figure 13.6 shows the attenuation of an 18 kft, 24-gauge loop.

Figure 13.6 Attenuation of an 18 kft, 24-Gauge Loop



To fully realize the potential of a twisted-pair loop, the electronics front-end noise should be a few dBs below that of the twisted-pair loop plant. For an assumed twisted-pair loop plant noise power density level of -140 dBm/Hz, the RMS noise voltage for a bandwidth of 500 kHz is about 700 μ V as calculated by the following expressions:

$$P = 10^{\frac{-140}{10}} \times 5 \times 10^5 = 5 \times 10^{-9} \text{ Watts}$$

$$0 \quad k \quad \mu V$$

P is the total noise power in a bandwidth of 500 kHz, and V_{rms} is the corresponding voltage level. Within a single ADSL system itself, there is the potential for interference between the three derived channels:

- The POTS channel
- The high throughput downstream channel
- The low throughput upstream channel

The POTS channel is separated by a POTS splitter, which consists of a lowpass filter and a highpass filter. The POTS splitter design and implementation are very challenging. Ringing voltage applied at the Central Office is 86 Vrms superimposed on -48 Vdc with a two

seconds on/four seconds off pattern. When ringing is interrupted due to a telephone handset going off-hook (referred to as *ring trip*), a considerable transient can be induced in the line.

Other lower level transients are produced by dial pulsing and on-off hooks. Upstream and downstream channels can be separated by either frequency division using highpass and low-pass filters, echo cancellation, or a combination of frequency division and echo cancellation. Due to the combination of heavy channel attenuation and light echo path attenuation, a filter stop band attenuation or echo cancellation level of more than 60 dB is expected.

13.1.3 The Convergence of ADSL Standards

The first issue of ADSL standard, T1.413, was released during 1995 by the T1E1 committee. The concept of ADSL was also heavily promoted by professional technical conferences and the formation and activities of the ADSL Forum. The ADSL technology has been in technical and market trials since early 1994. The purpose of the technical trial was to verify the performance of ADSL technology in the real field. The purpose of the market trial was to get user feedback about the technology and its potential applications. Technical trials have established the viability of the ADSL technology. Market trials have likewise indicated strong user interest. Most recently, ADSL has been considered as an ideal vehicle for Internet access and telecommunicating applications.

13.2 Transceiver Structures and Line Codes

The DMT line code is a multi-carrier system. The spectrum of a DMT signal consists of many narrow bandwidth QAM-like carriers with different and equally distributed carrier frequencies. Information is attached in the transmitter and recovered in the receiver from these carriers through discrete versions of Fourier Transforms. The CAP line code, similar to QAM, is a single carrier system. Information is attached to and recovered from the single carrier through transmit filters and receiver channel equalizers. One similarity between DMT and CAP line codes is that there is no carrier modulation and demodulation required.

13.2.1 DMT Line Code

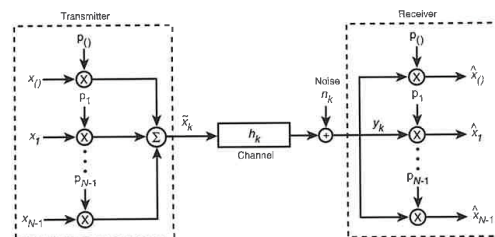
We can envision the DMT ADSL as a group of 256 voice band modems with their carrier frequencies ranging from a few kHz to near 1 MHz and with no guardband in between adjacent carriers. The need of guardband is eliminated due to the *orthogonality* between all carriers. Similar to the voice band situation, each modem in this group can fall back to lower data rates by changing its constellation size. The capability of variable constellation size for each subcarrier is the DMT approach of dealing with a random channel with different Signal

On the other hand, because frequency responses of all subchannels of this modem group are relatively flat, equalizers of the group of voice band modems are all omitted. The use of Trellis coding can still be applied. Because all the modems in this group can be synchronized, the transmit and receive filter functions can be combined and performed by an IFFT (Inverse Fast Fourier Transform) for all transmit filters, and an FFT (Fast Fourier Transform) for all receive filters.

On the line after the ADSL transmitter, we can imagine 256 different but synchronized signals each of which has its distinguishable carrier frequency and constellation size. The number of 256 subchannels corresponding to an IFFT/FFT size of 512 was chosen to maximize ADSL transceiver hardware efficiency while maintaining a tolerable IFFT/FFT processing delay time. A 512 real-to-complex FFT and a 512 complex-to-real IFFT were actually used.

Figure 13.7⁸⁹ shows a simplified DMT system. The major function of a DMT transmitter is the N (for which $N=512$) dimensional IFFT. The major function of a DMT receiver is the N -dimensional FFT.

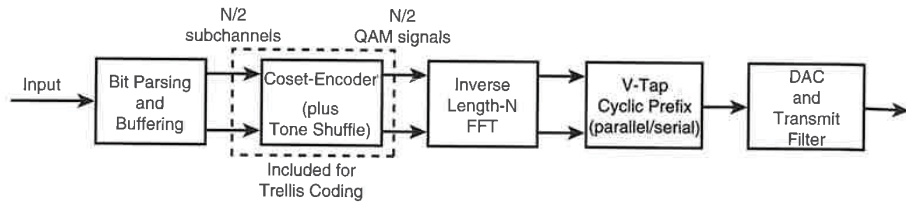
Figure 13.7 Simplified Illustration of DMT Transceiver and Channel



DMT ADSL Transmitters

The general transmitter illustrated in Figure 13.8 consists of bit parsing, buffering, coset-encoder, IFFT, cyclic prefix, parallel to serial conversion, Digital to Analog Conversion, (DAC), transmitter filter, and line interface functions.

Figure 13.8 Block Diagram of a DMT Transmitter



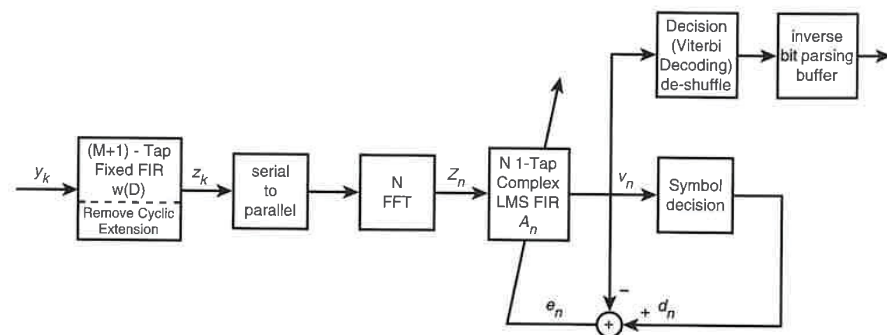
The serial bit stream is first converted into parallel data in the transmitter. The N -dimensional parallel data is then mapped into $N/2$ multibit subchannels according to a bit allocation algorithm. The coset-encoder implements the bit allocation algorithm. To achieve an efficient DFT implementation we need $N=2^i$, where i is a positive integer.

Each multibit subchannel can use a QAM signal constellation. The parallel time domain data after the IDFT is converted back to serial. A guard period stuffed with cyclic prefixes is introduced before the DAC function. The cyclic prefix is defined as the partial duplication and addition of the last v points in front of the N original data points, resulting in a total number of $v+N$ cyclic prefixed data points.

DMT ADSL Receivers

Figure 13.9 shows the general structure of a DMT receiver. The general receiver consists of a line interface, Analog to Digital Conversion (ADC), Time-Domain Equalizer (TEQ), serial to parallel conversion, FFT, Frequency-Domain Equalizer (FEQ), symbol decision, bit decision, and inverse bit parsing functions.

Figure 13.9 Block Diagram of a DMT Receiver



After ADC, the received signal is first filtered by the TEQ (the $(M+1)$ tap fixed FIR filter, as illustrated in Figure 13.9. The samples corresponding to the guard period cyclic prefix are simply ignored. The rest of the samples are converted into parallel data for input to the DFT process. The FEQ (the $N/4$ -tap complex FIR filter in Figure 13.9) is implemented by inverse target channel scaling. The target channel is the combination of channel and TEQ. FEQ is necessary to correct both magnitude and phase distortion of the equalized channel when using a single decision device for all subchannels.

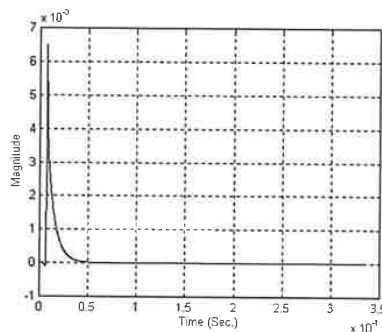
Note

It is worthwhile to mention that the purpose of the TEQ is to contain the amount of channel distortion in the time domain. The use of guard periods is to avoid the residual inter-baud-symbol interference. Residual channel distortion, in the form of different magnitude attenuation and phase delay for each subcarrier, however, still exists for each baud symbol.

Combating Channel Distortion

In theory, the channel distortion can be avoided by a DMT system through the fine division of the available bandwidth into many subcarriers such that each subchannel is almost distortion free. The finer division in frequency domain is equivalent to further extension of the signaling baud period. The channel distortion can be considered negligible if the channel impulse response tail caused by channel distortion is negligible compared with the signaling baud period. Figure 13.10 shows the channel impulse response of the 9 kft, 26-gauge loop.

Figure 13.10 Channel Impulse Response of a 9 kft, 26-Gauge Loop



The tail length is about 2.77 microseconds at 1 percent of the peak amplitude. The signaling baud length can be chosen as 277 microseconds for a factor of 100 of the tail length. The baud rate is then 3.61 kHz. On the other hand, the overall delay time, which is about three times the baud length, should also be constrained according to the system requirement.

The channel distortion could cause inter-subchannel interference. The inter-subchannel interference is caused by amplitude attenuation and phase delay differences between subchannels. The total inter-subchannel interference for a particular subchannel can be calculated as follows:

$$10 \log_{10} \sum_{\substack{k=1 \\ k \neq i}}^N \int_0^T \cos\left(2\pi i \frac{t}{T} - \theta_i\right) \cdot \frac{1 - \Delta A_k}{1 - \Delta A_i} \left(\cos\left(2\pi k \frac{t}{T} - \theta_k\right) + \sin\left(2\pi k \frac{t}{T} - \theta_k\right) \right) dt$$

The values are as follows:

ΔA_i and ΔA_k are the subchannel and interfering subchannel amplitude attenuations, respectively.

θ_i and θ_k are the subchannel and interfering subchannel phase delays, respectively.

The inter-subchannel interference can be minimized by selecting a lower baud rate or by using a channel equalizer.

Although the effect of the channel impulse response tail is minimized through the selection of a slow baud rate, the tail of one baud will extend to the next adjacent baud. This inter-baud interference is the DMT inter-symbol interference. The effect of DMT inter-symbol interference can be minimized by using a guard period or a cyclic prefix.⁹⁰ The length of a cyclic prefix is chosen such that the tail portion of one baud will die out before the next adjacent baud starts. The cyclic prefix repeats the last ν time domain serial data points before the first serial data point, in which ν is the length of the guard period. The length of the cyclic prefix can also be minimized by using a channel equalizer.

We have the following:

$$\nu = T_g f_s, N = T f_s, \text{ or } f_s = \frac{N}{T} = \frac{\nu}{T_g}$$

The value f_s is the sampling frequency, and T_g is the guard period. The sampling frequency should be higher than twice that of the usable channel bandwidth.

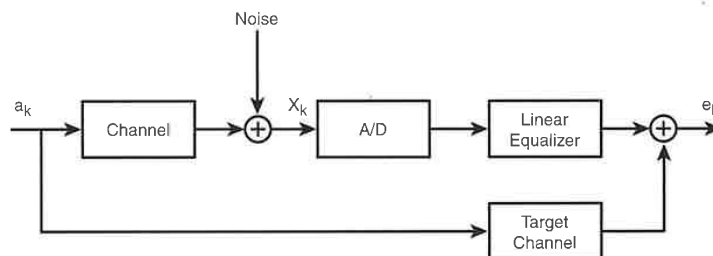
A time domain channel equalizer is necessary for the DMT receiver to reduce the amount of channel distortion present in the subscriber loop environment. The channel equalizer reduces the length of the cyclic prefix.

Note

In theory, a linear equalizer can reduce the cyclic prefix to zero length; however, a linear equalizer operating on the sampling rate to reach that goal might not be practical to implement in hardware. Furthermore, such a linear equalizer could cause excessive noise enhancement.

A linear equalizer with a small number of taps can reduce the cyclic prefix length to less than 30 sampling points. The conventional channel equalizer optimizes the desired signal to noise ratio at a particular decision point; however, the channel equalizer in general can modify the channel response according to particular needs just as what an FIR filter is capable of. A DMT Time Domain Equalizer can modify the loop channel response to the target channel response, as shown in Figure 13.11. The desired target channel response has the minimum mean square error when compared with any other equalized channel response.

Figure 13.11 Analysis of DMT Time-Domain Equalizer



The pair of DMT Time-Domain Equalizers and the target channel is similar to the pair of feedforward and feedback filters of a Decision Feedback channel Equalizer (DFE), except the impulse response of the target channel does not have to be causal. The optimal DMT Time-Domain Equalizer coefficients can be calculated using the same matrix operation method used for the calculation for those of a DFE, but in several iterations. The target channel impulse response is calculated only for evaluation, but not for real-time filtering. In practice, DMT Time-Domain Equalizer coefficients are identified iteratively in real-time in frequency or time domain.^{91,92}

To complete the received signal detection, a Frequency-Domain Equalizer is also required. Although the inter-symbol interference has been mainly avoided by utilizing a cyclic prefix, amplitude attenuation and phase delay differences still exist for different subchannels. We can imagine each DMT baud pulse consisting of 256 sinusoids of different frequencies. At the transmit side, all these sinusoids are synchronized by the IFFT operation; however, these sinusoids are not synchronized in phase after the FFT operation at the receiver due to the channel distortion.

The purpose of the Frequency-Domain Equalizer (FEQ) is to correct phase and amplitude distortion of each subchannel such that a unified symbol detection mechanism can be applied to all subchannels. The FEQ has one complex tap for each subchannel resulting to an N /two-dimensional equalizer coefficient vector. The FEQ coefficient vector has the inverse frequency response of the equivalent channel, including transmit and receiver filters and the Time-Domain Equalizer. FEQ is performed by multiplying the FFT output with the FEQ coefficient vector.

Bit Loading Algorithm

Based on the Signal to Noise Ratio (SNR) of each subchannel, the number of bits that can be transmitted through each subchannel for certain error probability can be calculated as follows:

$$b_j = \log_2 \left(1 + \frac{SNR_j}{\Gamma} \right)$$

The SNR_j is expressed in power ratio. Γ for an error rate of 10^{-7} is 9.8 dB or 9.55 in terms of power ratio. Γ of 9.8 dB is the reference point for uncoded system with 0 dB performance margin. To achieve an additional SNR performance margin, the value of Γ should be adjusted accordingly. For the same error rate, but with a 6 dB performance margin, the value of Γ would be increased to 15.8 dB or 38.02 in terms of power ratio. The value of Γ should be adjusted accordingly if any coding gain is to be considered. To add a coding gain of 3 dB, Γ will be reduced to 12.8 dB or 19.05 in terms of power ratio.

Note

It should be noted that Γ is only used here for analytical purpose—not as a design parameter.

The computation for the number of bits that can be transmitted through each subchannel will result in a fractional number of bits for each subchannel. An integer number of bits for up to 11 bits per subchannel is expected if a simple two-dimensional QAM-like constellation is to be implemented; however, the use of an integer number of bits could reduce the transmission efficiency.

One way to improve the transmission efficiency with integer number of bits is to assign a different signal power for each subchannel. The other way to improve transmission efficiency is to use a multidimensional signal constellation.⁹³ Up to 1 dB of performance improvement can be achieved by using these advanced loading algorithms.

The overall transceiver throughput is the sum of the number of bits for all subchannels times the modified baud rate, that is, the inverse of the baud period plus the guard period.

The computation of the performance margin for a target throughput can be achieved using the following expression in several iterations:

$$R = \sum_{j=1}^{256} b_j \frac{1}{T + T_g}$$

In other words, we first choose a particular SNR margin and calculate corresponding transmission throughput. We then adjust the value of the SNR margin and repeat the transmission throughput calculation until the desired transmission throughput is obtained.

Pilot Tone for Timing Recovery

The clock synchronization between a DMT transmitter and a DMT receiver is maintained through a timing recovery circuit in at least one transmission direction. This synchronization is based on the configuration where the transmitter and the receiver at one end of an ADSL system use their own clock source, and the transmitter and receiver at the other end use the recovered clock.

The timing recovery circuit of a DMT system involves the transmission of a pilot tone at the clock source end and the recovery of the pilot tone at the other end. The pilot tone could have periodic phase shift to reduce its interference with other tones. The transmit power of the pilot tone is usually a little lower than other information bearing subcarriers. The recovered pilot tone is usually filtered with a phase locked loop to increase its stability. The transmit power of the pilot tone may actually be more than the nominal transmit power of the information bearing subcarriers, especially for longer loops.

Note

A pilot tone is a subcarrier dedicated only for the purpose of timing recovery. A pilot tone has a fixed amplitude and fixed or alternating phases.

DMT ADSL Transceiver Parameters

The transceiver parameters⁹⁴ of a DMT system are summarized in Table 13.2 for the downstream channel.

Table 13.2 DMT Downstream Parameters

Symbol rate	4 kHz
FFT size	512 samples
Cyclic prefix	32 samples
Synchronization	Average 8 samples/symbol
Sampling rate	2.208 MHz
Transmit power	20 dBm
Time-Domain Equalizer	16 taps
Highpass filter (without echo cancellation)	6th order elliptic, passband corner frequency 62.5 kHz, 1 dB passband ripple

With the parameters in Table 13.2, the downstream DMT subcarriers are spaced at 4.3125 kHz intervals. The lowest carrier available is at 64.6875 kHz or 12.938 kHz with echo cancellation. The highest carrier available is at 1099.6875 kHz. The transceiver parameters of a DMT system are summarized in Table 13.3 for the upstream channel.

Table 13.3 DMT Upstream Parameters

Symbol rate	4 kHz
FFT size	64 samples
Cyclic prefix	4 samples
Synchronization	Average 1 sample/symbol
Sampling rate	276 kHz
Transmit power	7 dBm
Time-Domain Equalizer	32 taps
Lowpass filter	6th order elliptic, passband corner frequency 43.875 kHz, 1 dB passband ripple

With the parameters in Table 13.3, the upstream DMT subcarriers are also spaced at 4.3125 kHz intervals (identical to the downstream direction). The lowest carrier available is at 11.25 kHz (leaving below 10 kHz for POTS), the highest carrier available is at 42.75 kHz or 271.6875 kHz with echo cancellation. In addition, we need to meet an error rate of 10^{-7} and have a POTS highpass filter with a corner frequency of higher than 4 kHz. The performance should be examined with a background noise level of -140 dBm/Hz as well as NEXT and FEXT noise.

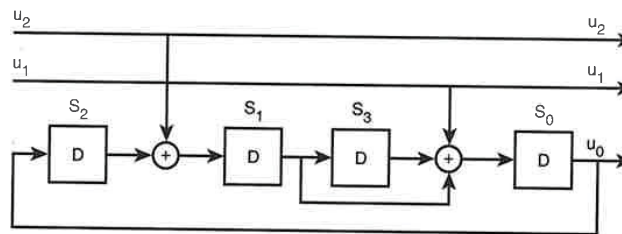
DMT ADSL Trellis Coding

The use of Trellis-Coded Modulation (TCM) is an option for ADSL to either meet performance margin requirements for long loops or increase the transmission throughput under a certain performance margin. Wei's 16-state 4D code, which has emerged from ten years of study and development, was proposed for ADSL.⁹⁵ This code has a theoretical gain of 4.5 dB and a practical gain of 4.2 dB against background and crosstalk noise.

In the TCM decoder, maximum-likelihood decoding using the Viterbi algorithm is employed to estimate the transmitted sequence. The use of a four-dimensional code (compared with a two-dimensional code) has the advantage of a smaller constellation expansion, and hence a smaller peak-to-average power ratio. As a result, it is more immune to nonlinear distortion. With the same decoding complexity, the four-dimensional codes also give higher coding gains.

The proposed Wei's code uses a rate $2/3$ (2 bit/3 bit) convolutional code with parity check matrix (D^3+D^2, D, D^4+1) . The number of bits in a four-dimensional symbol increases from the uncoded case of b bits to the coded case of $b+1$ bits. The 2^{b+1} points are partitioned into eight cosets. Two of the b message bits are fed into the convolutional encoder. The three output bits from the convolutional encoder are used to specify the coset. The other $b-2$ message bits determine which point in the coset should be transmitted. Figure 13.12 shows the structure of the convolutional encoder.

Figure 13.12 Structure of the Convolution Encoder



The minimum square Euclidean distance between points in the same coset is 4, with 24 neighbors. The minimum square Euclidean distance between coded coset sequences is 6. The fundamental coding gain of the code is determined by the smaller of the two, and is equal to

$$10 \log_{10} 4 - \frac{1}{2} 10 \log_{10} 2 = 4.52 \text{ dB}$$

The term $\frac{1}{2} 10 \log_{10} 2$ is for the adjustment of constellation expansion per two dimensions. In the uncoded case, there are only eight nearest neighbors for each four-dimensional symbol. The factor of 3 increase in the number of nearest neighbors causes the coding gain to decrease from 4.52 dB to an effective value of 4.2 dB. Trellis coding and decoding are applied to each subcarrier individually.

DMT ADSL Forward Error Correction (FEC) Coding

To accommodate maximum flexibility for the providers and end users of ADSL services, it was recommended that FEC be selectively applied to 32 kbps increments of the composite data streams to, or from, the Central Office.⁹⁶ This permits FEC to be included or excluded selectively both on a call-by-call basis and within portions of the composite data stream.

As an example of mixed requirements for FEC in an ADSL service, consider transmitting a one-way DS1 stream from the Central Office to the remote terminal (CO to RT) along with a bi-directional basic rate ISDN channel. The end user may require high reliability on the one-way channel because the one-way channel might contain highly compressed data with no possibility for request for retransmission. For this portion of the ADSL signal, FEC is necessary. Voice services and duplex data services with their own embedded protocols will require minimum latency on the embedded ISDN channel. For this portion of the ADSL signal, FEC is optional.

FEC of ADSL employs Reed-Solomon codes based on symbols of 8 bits=1 byte (that is, a code over $GF(2^8)$). The maximum codeword length for such codes is 255, with varying error correction capabilities. Relatively long codeword lengths for a minimal redundancy of 8–10 percent were used. The redundancy and interleave depths chosen accomplish the following: correct for error bursts of up to $\frac{1}{2}$ ms of transmitted data and reduce the background bit error rate (BER) from 10^{-7} to 10^{-10} .

Tables 13.4–13.6 summarize the chosen encoding system. Table 13.4 specifies interleave depths (the number of codewords in the interleave matrix) and codeword lengths (specified in ms) for uncoded data rates ranging from 32 kbps to 7584 kbps. Table 13.4 aids in the calculation of the number of message bytes in a codeword for any uncoded data rate. Note that the interleave depth times the codeword length, which equals the interleave latency, is kept constant at 16 ms.

Table 13.4 Interleave Depth and Codeword Length Parameters

Data Rate (kbps)	Interleave Depth (codewords)	Codeword Length (ms)
32–64	1	16
96–224	2	8
256–448	4	4
480–928	8	2
960–1888	16	1
1920–3776	32	0.5
3808–7584	64	0.25

Table 13.5 and Table 13.6 specify the number of check bytes in a codeword for data rates below and at or above 256 kbps, respectively. For the flexibility offered, very few parameters must be stored in the ADSL unit to implement selectable FEC.

Table 13.5 Message Bytes and Check Bytes (Data Rates < 224 kbps)

Data Rate (kbps)	Message Length (bytes)	Redundancy Length (bytes)
32	64	8
64	128	16
96–128	96–128	12
160–192	160–192	16
224	224	20

Table 13.6 Message Bytes and Check Bytes (Data Rates > 224 kbps)

Message Length (bytes)	Redundancy Length (bytes)
128–147	12
148–175	14
176–207	16
208–237	18

As a simple example in the use of Tables 13.4–13.6, consider adding FEC to an uncoded data rate of 1568 kbps. Using Table 13.4, we see one codeword contains $(1568 \text{ kbits/sec}) \times (1 \text{ msec/codeword}) \times (1 \text{ byte/8 bits}) = 196$ message bytes. Using Table 13.6, we find

that for a codeword of length 196 bytes, we need to add 16 check bytes to form a codeword of 212 bytes. The coded data rate, or line rate, is calculated as $(212 \text{ bytes/codeword}) \times (1 \text{ codeword/1 msec}) \times (8 \text{ bits/byte}) = 1696 \text{ kbps}$.

Interleaving for Reed-Solomon Coding

The combination of Reed-Solomon code with interleaving is effective at correcting errors caused by impulse noise in the subscriber loop plant. Some studies indicate that a burst error correction capability of 500 microseconds (μs) = $1/2 \text{ ms}$ should provide sufficient protection against the effects of nearly all impulses encountered for a well-designed ADSL system.⁹⁷ On average, the time between impulses was found to be 67 ms.⁹⁸ For redundancies in the range of 7–9 percent, the required end-to-end latency is about 16 ms to correct for 500 μs of data with errors. To correct for 1000 μs of data with errors would require double the latency or double the redundancy.⁹⁹

Consider an uncoded transmission rate of 1600 kbps = 200 kbyte/s. Adding 7 percent redundancy, at this data rate equal to 14 kbytes/s, results in a coded transmission rate of 214 kbytes/s. The impulse causes a burst of $1/2 \text{ ms} = 107 \text{ bytes}$ coded data destroyed. Using a $t = 7 \text{ byte}$ ($2t = 14 \text{ check bytes}$) error correction capability FEC code would require an interleave depth of at least 16 codewords to correct this burst of 107 bytes of data with errors.

At a coded data rate of 214 kbytes/s, a codeword of length 214 bytes would last 1 ms. The latency for an interleave depth of 16 codewords is thus 16 ms. Conventional block interleaving would require 16 ms for interleaving at the encoder and an additional 16 ms for deinterleaving at the decoder, but convolutional interleaving, as described later in this section, reduces the total delay to 16 ms.

Using a fixed latency of 16 ms for any data rate, you can achieve the same burst error correction capability with smaller codewords and proportionally larger interleave depths. For example, relatively short constituent codewords are used in the concatenated Reed-Solomon codes for compact discs. Longer codewords, however, allow for additional redundancy to be added for random bit error protection with little additional cost. Increasing the number of check bytes in the previous example from the minimum $2t = 14$ to $2t = 16$ adds only 1 percent additional redundancy and results in a background bit error rate (BER) improvement from 10^{-7} to 10^{-10} . This last result is found using the following formula. Assume the following parameters:

- A burst error destroys x bytes per codeword
- A background random bit error rate (not due to the burst) of p

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bytes/code-

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the following

- A codeword length of N
- A redundancy of $2t$ bytes per codeword

The bit error rate¹⁰⁰ after burst and random error correction is given approximately by

$$\frac{1}{2} \left(\frac{N-x}{t-x+1} \right) \frac{t+1}{N} (8p)^{t+1} \frac{1}{2} \left(\frac{n-x}{t-x+1} \right) \frac{t+1}{n} (8p)^{t+1}$$

Adding one byte error correction capability to that needed for burst error correction, we chose $t=x+1$. Substituting $p=10^{-7}$, you can confirm the background bit error rate is reduced to the order of 10^{-10} for the codeword lengths chosen.

Convolutional interleaving reduces the end-to-end latency incurred for burst error correction to half the latency incurred by block interleaving. This reduction is achieved by alternately reading and writing to the interleave matrix for each encoded byte. First, consider block interleaving. Figure 13.13 illustrates the block interleave matrix for a codeword length of $N=8$ bytes and an interleave depth $d=5$ codewords.⁹⁶

Figure 13.13 Block Interleave/Deinterleave Matrix

Interleave Depth
(Intlv Read/Deintlv Write Direction)

→

0	1	2	3	4
0	8	16	24	32
5	6	7	8	9
1	9	17	25	33
10	11	12	13	14
2	10	18	26	34
15	16	17	18	19
3	11	19	27	35
20	21	22	23	24
4	12	20	28	36
25	26	27	28	29
5	13	21	29	37
30	31	32	33	34
6	14	22	30	38
35	36	37	38	39
7	15	23	31	39

Codeword Length
(Intlv Write/Deintlv Read Direction)

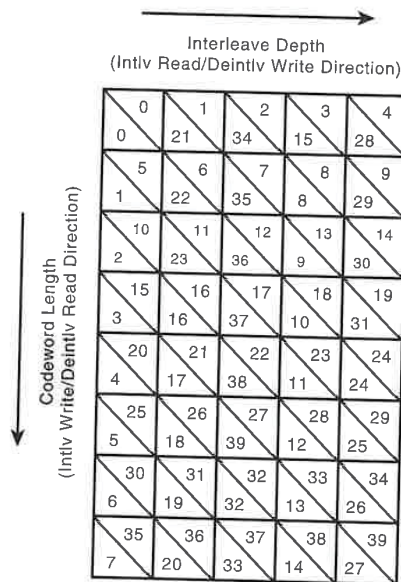
↓

Block interleaving requires writing all positions in an entire interleave matrix prior to the first byte being read. The lower-left number x in each square in the matrix indicates the *time* index when writing into that location. The upper-right number y in each square in the matrix indicates the time index when reading from that location. Of course the entire matrix is written prior to any byte being read. Therefore, in actual implementation, two separate interleave matrices are used: one from which the current byte is read and one into which the current byte is written.

The same matrix describes deinterleaving, except the lower-left number in a square indicates the time index when reading from that location, while the upper-right number in a square indicates the time index when writing to that location. Deinterleaving adds a delay of $40+x-y$ bytes at the decoder end. The end-to-end delay with block interleaving for this example is thus 80 bytes. Note also that for correct decoding, the block deinterleaver must know the position of the beginning of the interleave matrix.

Now consider convolutional interleaving. As shown in Figure 13.14, in convolutional interleaving, after writing a byte into the interleave matrix, a previously written byte is read from the same interleave matrix. Only one interleave matrix is used for both reading and writing, so convolutional interleaving requires half the memory space of block interleaving.

Figure 13.14 Convolutional Interleave/Deinterleave Matrix



While the interleave matrix is read sequentially horizontally as with block interleaving, the matrix is written in a more complex manner, as shown by the numbers in the matrix. In **general**, the byte at the beginning of a codeword is written to, and read from, the same location. The remaining bytes in a codeword are written sequentially vertically within the same column as the first byte. For example, the first byte in a codeword experiences no delay (written and then read immediately thereafter).

At the decoder end, the same matrix describes deinterleaving except the bytes are now written sequentially horizontally and are now read in the more complex manner vertically. Thus, the first byte in a codeword incurs the minimum delay in the interleave matrix, but incurs maximum delay in the deinterleave matrix. The end-to-end total delay for this example is 40 bytes—exactly half the delay incurred by block interleaving.

Upon examining the interleave matrix, you should also note that the convolutional deinterleaver must know only the position of the beginning of a codeword to deinterleave correctly. Thus with convolutional interleaving, FEC synchronization need only search through a codeword depth rather than the entire interleave matrix. Note that for the entire interleave matrix to be used, the codeword length and interleave depth must be coprime. For ADSL, the interleave depths chosen are all powers of 2. Any odd codeword length will then be coprime to the interleave depth.

Convolutional interleaving incurs half the latency, requires half the memory, and needs less time for resynchronization compared with block interleaving. For this savings, convolutional interleaving requires a more complicated addressing scheme, needs alternate reading and writing of the interleave matrix, and requires an interleaving/deinterleaving codeword length coprime to the interleave depth. The convolution interleaving was selected for DMT ADSL.

DMT Asymmetrical Echo Cancellation

The asymmetrical echo cancellation technique can be used to improve the performance of an ADSL system. Although the upstream/downstream overlapped spectrum created by echo cancellation is NEXT limited, it still can provide a high enough SNR to be useful for transmission in both upstream and downstream directions. At the ADSL data rates, traditional time-domain and frequency-domain LMS echo cancellers can be prohibitively expensive to implement.

Mixed frequency and time-domain techniques are proposed to achieve low-complexity echo cancellation. The use of these techniques can achieve the required 70 dB of echo cancellation level.

A time-domain echo canceller needs to complete the discrete convolution process in the scale of the echo impulse response during every sampling interval. The echo impulse response could be as long as a few hundred sample points. For a sampling rate of about 1 MHz, a time-domain echo canceller would need a few hundred million multiplications and addition operations per second. On the other hand, if the echo cancellation is implemented in the frequency domain, assuming both echo path and data vectors are available in the frequency domain, the operations need to be completed only during each DMT baud interval. For 256 subcarriers and a baud rate of 4 kHz, the required operations are only a few million complex multiplication and addition operations per second.

For the mixed frequency and time-domain approach, most of the echo emulation is performed in the frequency domain. Because data vectors and therefore the echoes are not periodic, the time-domain convolution cannot be exactly duplicated in the frequency domain as a block multiplication. The circular nature of an echo block can be reinstated by *tail cancellation* and *cyclic reconstruction*.^{101,102}

Note

The **tail cancellation** is the subtraction of the tail caused by the previous data block, and the **cyclic reconstruction** is the replacement of a cyclic prefix corresponding to the current data block.

The combined process involves the convolution of an estimated echo path impulse response with portions of the current and the previous echo blocks.

Due to the asymmetrical transmission throughput nature, the sampling frequencies of transmission and receiving paths are different. Thus, a decimation, in the *Asymmetrical Terminal Unit-Central Office* (ATU-C), or an interpolation, in the ATU-R, process is necessary to match the rate of an analog to digital converter (ADC) to that of a digital to analog converter (DAC). Figure 13.15 shows a functional block diagram for an ATU-C DMT echo canceller. Figure 13.16 shows a functional block diagram for an ATU-R DMT echo canceller.

In the ATU-C, as illustrated in Figure 13.15, the ADSL upstream receiver has an FFT size of N . The ratio between the downstream DAC sampling rate and the upstream ADC sampling rate is k . Therefore, the ADSL downstream transmitter has an FFT size of kN . The echo has a tail of M sampling points in the transmitter sampling rate. The last $M-1$ previous and current data block points are combined through subtraction and used for tail cancellation and cyclic construction.

Figure 13.15 ATU-C DMT Echo Cancellation

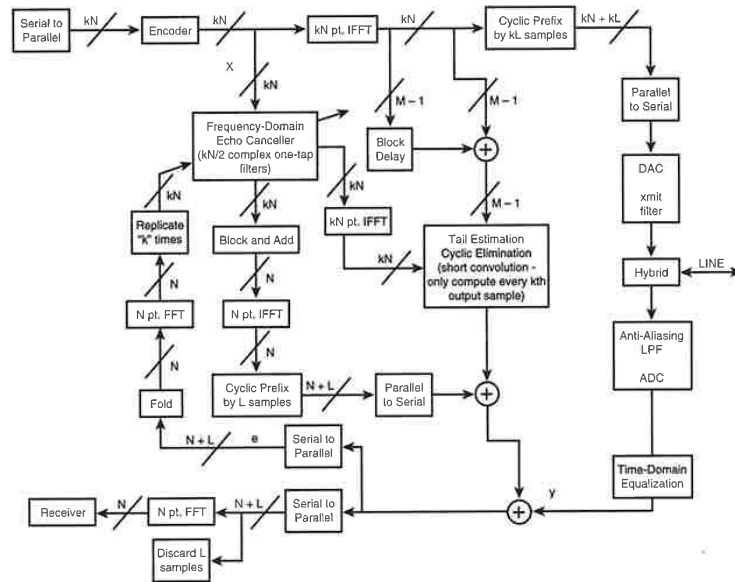
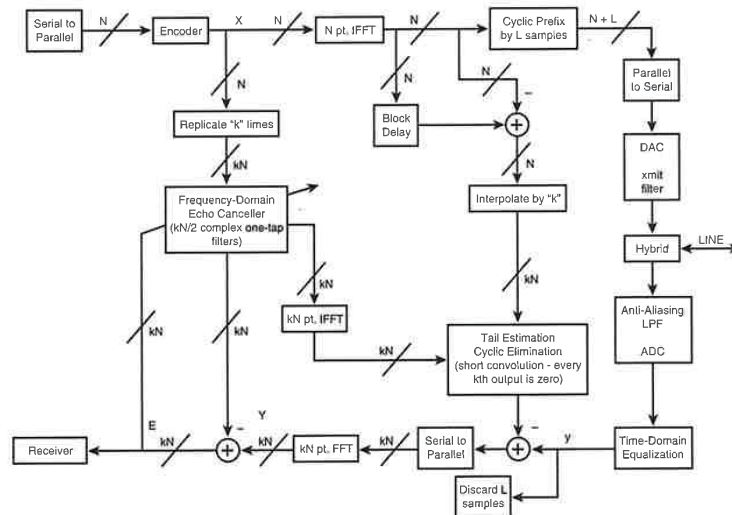


Figure 13.16 ATU-R DMT Echo Cancellation



The estimated frequency-domain echo path is also transformed into time domain for the tail cancellation and cyclic construction purpose. The convolution output for tail cancellation and cyclic construction is only needed at the receiver sampling rate. The main echo duplication is generated in the frequency domain, decimated by a factor of k , and converted into time domain for echo cancellation. The main echo replica is generated in the frequency domain, but used in the time domain to avoid the out-of-band aliasing effect.

In ATU-R, transmitting data in both the frequency domain and the time domain is interpreted to the receiver sampling rate. The interpolated frequency-domain data is used for main frequency-domain echo replica generation. The interpolated previous and current data block points in time domain are combined through subtraction and used for tail cancellation and cyclic construction. The estimated frequency-domain echo path is transformed into time domain for the tail cancellation and cyclic construction purpose. The main echo replica is generated in the frequency domain and combined with FFT transformed received data for direct frequency-domain echo cancellation.

DMT ADSL Transceiver Implementation

As for other DSL systems, only if a transceiver can be implemented with a low-cost VLSI (Very-Large-Scale-Integrated) circuits solution will ADSL find its broad acceptance. Major functions that an ADSL transceiver needs to accomplish in the real time include complex FFT/IFFT, Time-Domain Equalizer, Frequency-Domain Equalizer, echo canceller, Reed-Solomon forward error correction, Trellis coding, timing recovery, digital interfaces of up to seven channels, and OAM.

ATU-C/ATU-R Transceivers

ATU-C and ATU-R transceivers can be divided into three major functional blocks: *Digital Interfaces* (DI), *Digital Signal Processing* (DSP), and *Analog Interfaces* (AI).¹⁰³ Figure 13.17 shows such a decomposition for ATU-C. Figure 13.18 shows such a decomposition for ATU-R.

Figure 13.17 ATU-C Functional Blocks

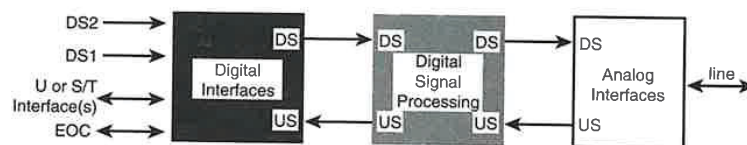
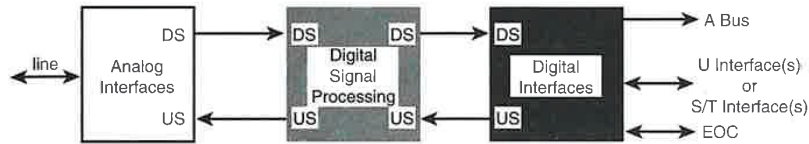
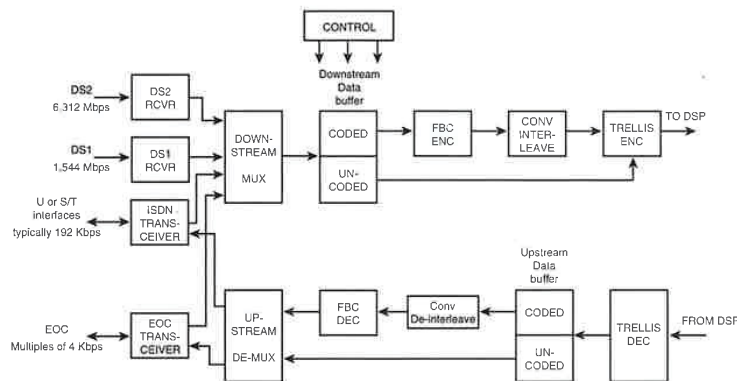


Figure 13.18 ATU-R Functional Blocks



The DI includes the acquisition and generation of data and clocks that interface the Central-Office switch or remote-terminal applications module. The DI essentially formats and unformats data for convenient processing by the DSP. Modulation and demodulation of data from and to the discrete time modulated transmission signals is performed in the DSP Subsection. The digital signals are converted and conditioned to and from the line in the AI. Figure 13.19 shows the functional blocks of ATU-C DI.

Figure 13.19 ATU-C DI Functional Blocks



In the downstream direction, high-speed primary data at DS1 (1.544 Mbps) or DS2 (6.312 Mbps) rates, low-speed secondary data at multiples of 16 Kbps (typically 192 Kbps), and EOC data at small multiples of 4 Kbps are received, processed, and transferred to the DSP. The processing includes multiplexing the various received data streams into one data stream, which is then buffered and separated into two types. The first type of data will be FEC coded and interleaved for error protection. The second type of data will not be interleaved but might be FEC encoded because of its sensitivity to extra latency. The coded, interleaved data, together with the non-interleaved data, is then Trellis encoded before they are passed to the DSP.

In the upstream direction, only the secondary data and the EOC data are present. The data from the DSP is first Trellis decoded, then separated into FEC coded and uncoded data through the upstream buffer. The FEC coded data is then deinterleaved and FEC decoded. This decoded data, together with the uncoded data, are demultiplexed into the secondary data and the EOC data, which are then transferred to the transceivers. Table 13.7 summarizes the detailed semiconductor requirements:.

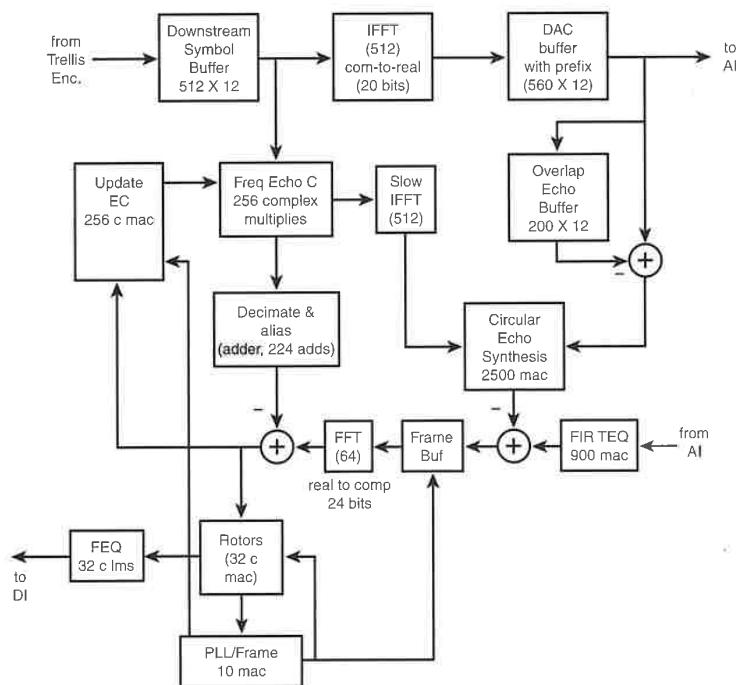
Table 13.7 DI Complexity Estimates

Functional Block	Random Logic	RAM	ROM
DS1 receiver	2000	N/A	N/A
DS2 receiver	2000	N/A	N/A
ISDN transceiver	2000	N/A	N/A
EOC transceiver	2000	N/A	N/A
Downstream multiplexer	1000	16	N/A
Downstream buffer	1000	512	N/A
FEC encoder	2000	18	128
Convolutional interleaver	1000	16 K	N/A
Trellis encoder	3000	192	1 K
Trellis decoder	15000	904	800
Upstream buffer	1000	512	N/A
Convolutional deinterleaver	1000	512	N/A
FEC decoder	7000	256	N/A
Upstream demultiplexer	1000	256	N/A
Control	8000	N/A	4 K×8
Total	49000	20 K	6 K

Figure 13.20 illustrates the ATU-C DSP functional blocks.

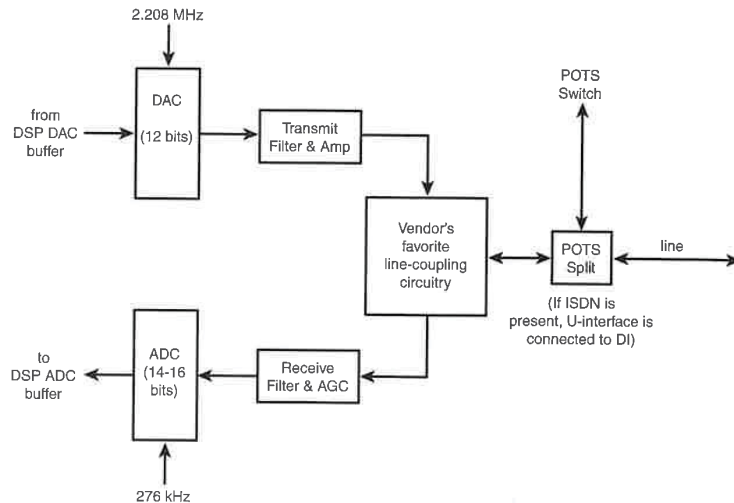
ATU-C DSP Functional Blocks Data symbols for each subchannel input are supplied by the Trellis encoder of the DI in 6-bit real and 6-bit imaginary parts. The downstream data symbols are modulated digitally by the 512 complex-to-real IFFT, and a 32-sample prefix is added to each block of time-domain samples at the DAC buffer, which is output to the AI at 2.208 Msamples/s.

Figure 13.20 ATU-C DSP Functional Blocks



The echo canceller uses an overlap method to make the echo appear periodic so that a simple 1-tap per subchannel echo canceller will provide excellent cancellation range. The upstream ADC samples at 276 kHz are filtered by an FIR TEQ and followed by the circular echo adjustment, frame buffering, and demodulation by the 64-point real-to-complex FFT. A decimated frequency-domain echo is subtracted, timing is digitally interpolated in the frequency domain to the remote clock, and a 1-tap LMS gain/phase adjustment (FEQ) is made to each subchannel so that common decision boundaries can be used by the Trellis decoder in the DI. The ATU-C DSP requires about 67,000 gates, 12 K RAM, 6 K ROM, and 67 MIPS (Millions of Instructions Per Second). Figure 13.21 illustrates the ATU-C AI functional blocks.

Figure 13.21 ATU-C AI Functional Blocks



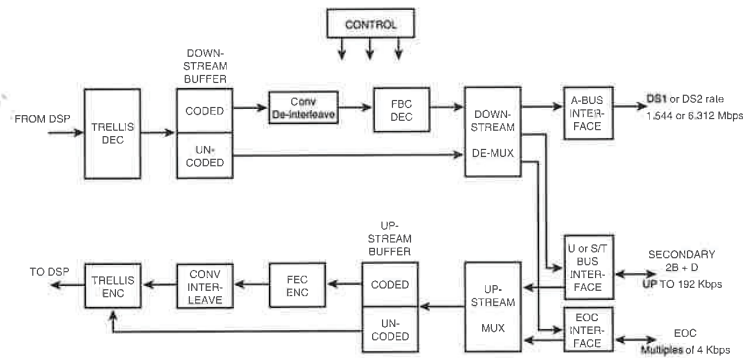
DAC precision is 12 bits at a sampling rate of 2.208 MHz, while ADC precision is 14–16 bits (good hybrids require 14, less sophisticated hybrids require 16) at a sampling rate of 276 kHz. The ADC clock is exactly eight times slower than the DAC clock, and both are run asynchronously with the CO clocks at a stable jitter-free crystal oscillator frequency. The jitter-free clocks are required for proper operation of the echo canceller in the DSP section. Interpolation and elastic queues in the DSP and DI sections realign clocks.

The ATU-R DI is very similar to the ATU-C DI. The main difference is that the decoder portion now runs at the downstream high data rate, while the encoder portion runs at the upstream low data rate. To save design effort, the basic computation modules (FEC encoder, FEC decoder, Trellis encoder, and Trellis decoder) are designed for both ATU-C and ATU-R DIs.

Figure 13.22 illustrates the functional blocks of an ATU-R DI.

In the upstream, low-speed secondary data at multiples of 16 Kbps (192 Kbps for example), and EOC data at small multiples of 4 Kbps are received, processed, and transferred to the Digital Signal Processor. The secondary data and EOC data are multiplexed, buffered, and separated into two types. The first type of data will be FEC coded and interleaved for error protection. The second type of data will not be interleaved because of its sensitivity to extra latency. The coded, interleaved data, together with the uncoded data, is then Trellis coded before they are passed to the DSP.

Figure 13.22 ATU-R DI Functional Blocks



In the downstream direction, in addition to the secondary and EOC data, primary data at DS1 (1.544 Mbps) or DS2 (6.312 Mbps) rates are also present. The data from the DSP is first Trellis decoded, then separated into FEC coded and uncoded data through the downstream buffer. The FEC coded data is then deinterleaved and FEC decoded. This decoded data, together with the uncoded data, are demultiplexed into the primary and secondary data and the EOC data. The ATU-R DI also requires about 49,000 gates, 20 K RAM, and 6 K ROM. Figure 13.23 illustrates the functional blocks of an ATU-R DSP.

Data symbols for each subchannel input are supplied by the Trellis encoder of the DI in 6-bit real and 6-bit imaginary parts. The upstream data symbols are modulated digitally by the 64 complex-to-real IFFT and a 4-sample prefix is added to each block of time-domain samples at the DAC buffer, which is output to the AI at 276 ksamples/s. The echo canceller uses an overlap method to make the echo appear periodic so that a simple 1-tap per sub-channel echo canceller will provide an excellent cancellation range.

The downstream ADC samples at 2.208 MHz are filtered by a 16-tap FIR TEQ and followed by the circular echo adjustment, frame buffering, and demodulation by the 512-point real-to-complex FFT. An interpolated polyphase frequency-domain echo is subtracted, timing is digitally interpolated in the frequency domain to the Central Office clock, and a 1-tap LMS gain/phase adjustment (FEQ) is made to each subchannel so that common decision boundaries can be used by the Trellis decoder in the DI. The ATU-R DSP requires about 72,000 gates, 12 K RAM, 4 K ROM, and 132 MIPS. Figure 13.24 illustrates the functional blocks of an ATU-R AI.

Figure 13.23 ATU-R Digital Signal Processing Functional Blocks

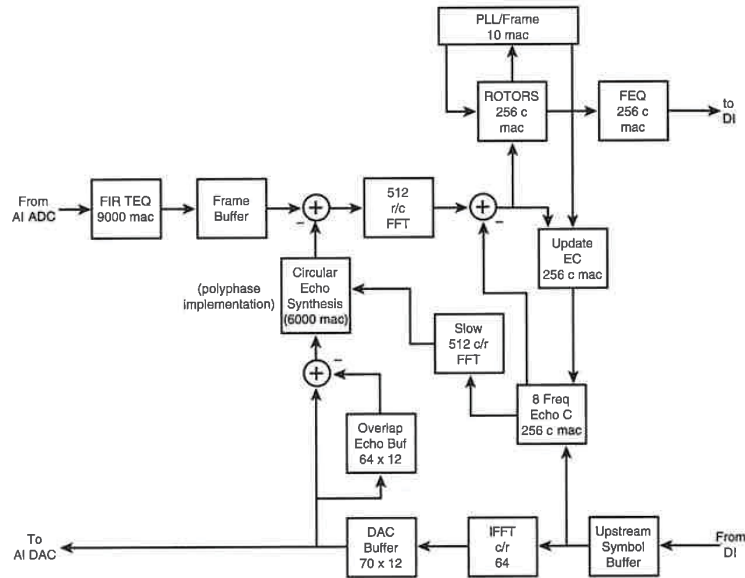
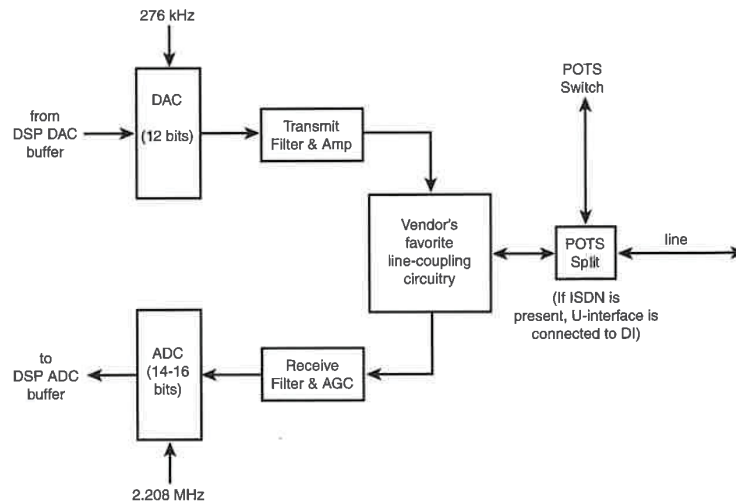


Figure 13.24 ATU-R AI Functional Blocks



DAC precision is 12 bits at 276 kHz, while ADC precision is 14–16 bits (good hybrids require 14, less sophisticated hybrids require 16) at 2.208 MHz. The ADC clock is exactly eight times faster than the DAC clock and both are run asynchronously with the ATU-R data clocks at a stable jitter-free crystal oscillator frequency. The jitter-free clocks are required for proper operation of the echo canceller in the DSP section. Interpolation and elastic queues in the DSP and DI sections realign clocks.

13.2.2 CAP Line Code

A CAP (Carrierless AM/PM) ADSL system consists of an upstream channel and a downstream channel. There is a transmitter and receiver pair for each channel and for each transceiver. A CO-side CAP transceiver, ATU-C, has a downstream transmitter and an upstream receiver. A residential or remote side transceiver, ATU-R, has an upstream transmitter and a downstream receiver.

CAP Transmitter Structure and Functionality

A CAP transmitter should have a scrambler, an encoder, a pair of transmitter filters, a Digital to Analog converter (DAC), and a lowpass filter.¹⁰⁴ The encoder converts the scrambled data into an in-phase channel data and a quadrature channel data. The transmitter filters convert the data streams into passband line signal. The DAC puts the filtered signal into analog format. The lowpass after the DAC removes harmonic images of the transmit signal. The encoded signal arrives at the baud rate.

The filters operate three to four times the baud rate. The DAC usually has a higher internal operating rate. The lowpass filter could be in analog format. A transmitter clock, locked to network incoming data or to recovered data by the receiver, should be available to functional blocks of the transmitter. Figure 13.25 shows the structure of a CAP ADSL transmitter.

Figure 13.25 A CAP Transmitter

