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Liu et al.

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(54) **FORWARD COMPATIBLE AND EXPANDABLE HIGH SPEED COMMUNICATIONS SYSTEM AND METHOD OF OPERATION**

(75) Inventors: **Young Way Liu**, La Mirada; **Ming-Kang Liu**, Cupertino; **Steve Chen**, San Jose, all of CA (US)

(73) Assignee: **Integrated Telecom Express, Inc.**, Santa Clara, CA (US)

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(51) **Int. Cl.**[7] **H04B 1/38**

(52) **U.S. Cl.** **375/219**; 375/220

(58) **Field of Search** 375/219, 220, 375/222, 260, 316, 354; 364/705.05; 370/94.2; 395/200.63; 455/522

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Primary Examiner—Stephen Chin
Assistant Examiner—Chieh M. Fan
(74) *Attorney, Agent, or Firm*—Law+

(57) **ABSTRACT**

A high speed communications system is provided which uses a selectable, desirable portion of the total available bandwidth of a transmission channel. In a preferred embodiment, the invention is an ADSL compatible modem which selects a sub-set of the available downstream DMT sub-channels based on an evaluation of such sub-channels by appropriate signal processing circuitry. An analog front end (AFE) contains sub-band filtering causes an upstream transceiver to use only this selected number of available sub-channels for downstream data transmission. This reduces hardware costs and complexity while still preserving compatibility with applicable ADSL standards and providing a high speed data link. The target data rate of the modem can be further enhanced to the point of achieving full protocol capability by increasing or upgrading the AFEs, and/or the signal processing circuitry in order to increase the number of processable transmitted downstream sub-channels.

67 Claims, 10 Drawing Sheets

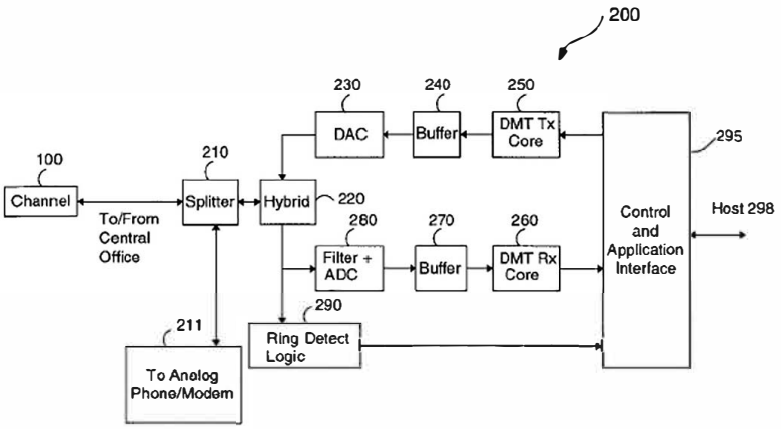

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FIGURE 1

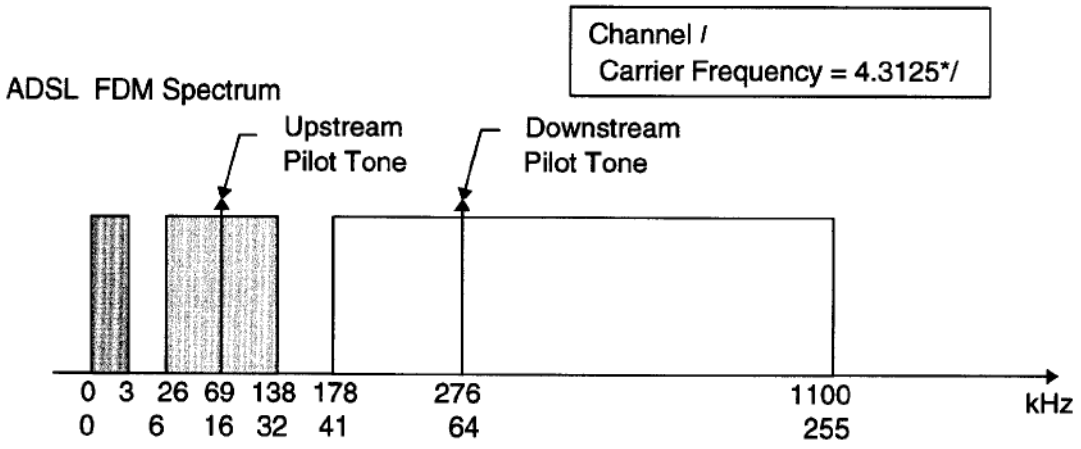


FIGURE 1B

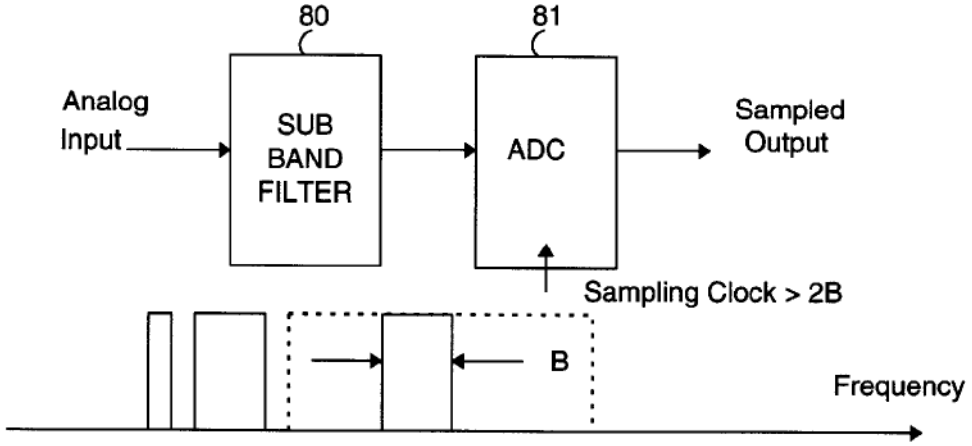


FIGURE 1C

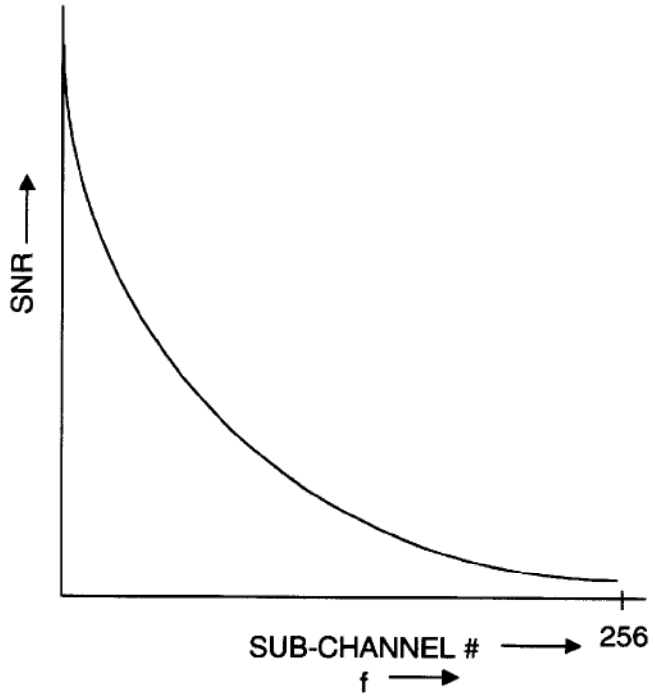
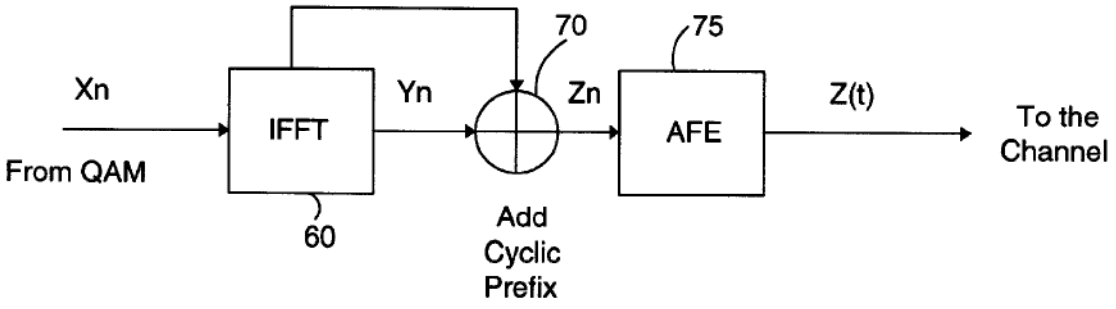


FIGURE 1D



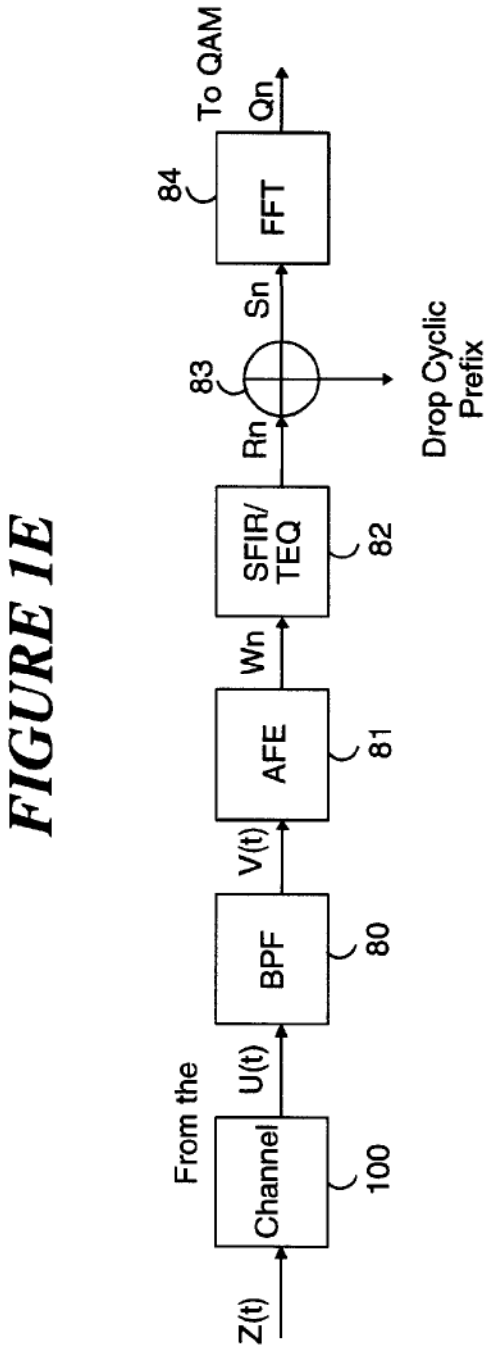


FIGURE 1E

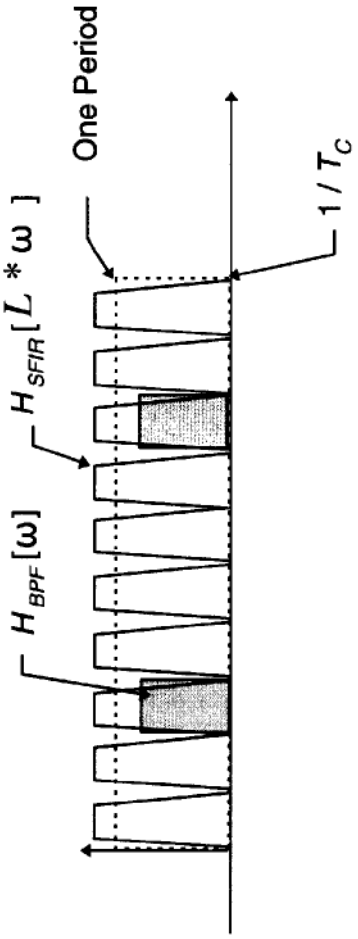
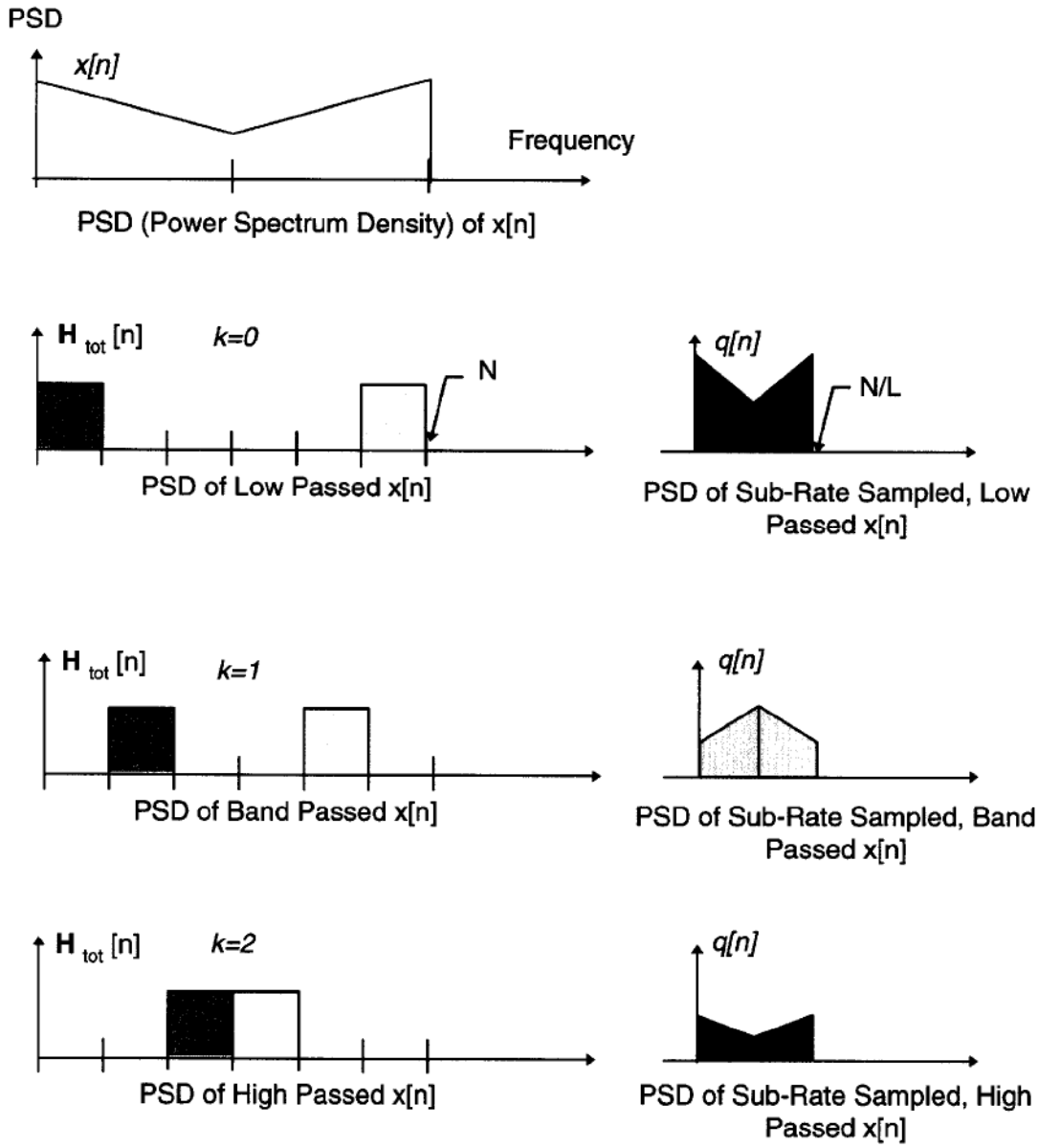


FIGURE 1F

FIGURE 1G


PSD
x[n]
Frequency
PSD (Power Spectrum Density) of x[n]
H tot [n]
k=0
N
PSD of Low Passed x[n]
q[n]
N/L
PSD of Sub-Rate Sampled, Low Passed x[n]
H tot [n]
k=1
PSD of Band Passed x[n]
q[n]
PSD of Sub-Rate Sampled, Band Passed x[n]
H tot [n]
k=2
PSD of High Passed x[n]
q[n]
PSD of Sub-Rate Sampled, High Passed x[n]

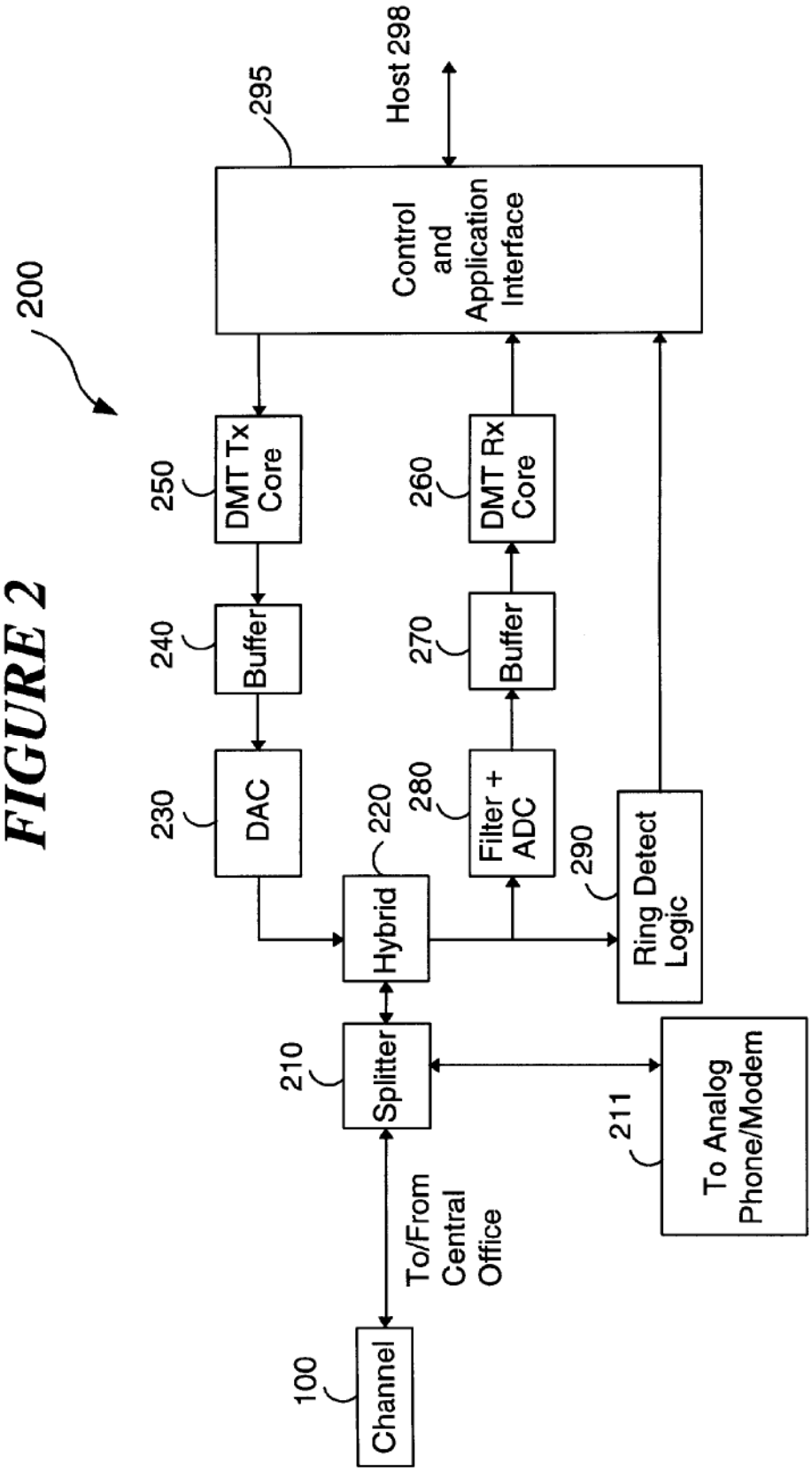

200
295
Host 298
Control and Application Interface
250
DMT Tx Core
240
Buffer
230
DAC
260
DMT Rx Core
270
Buffer
280
Filter + ADC
220
Hybrid
290
Ring Detect Logic
210
Splitter
211
To Analog Phone/Modem
To/From Central Office
100
Channel

FIGURE 2

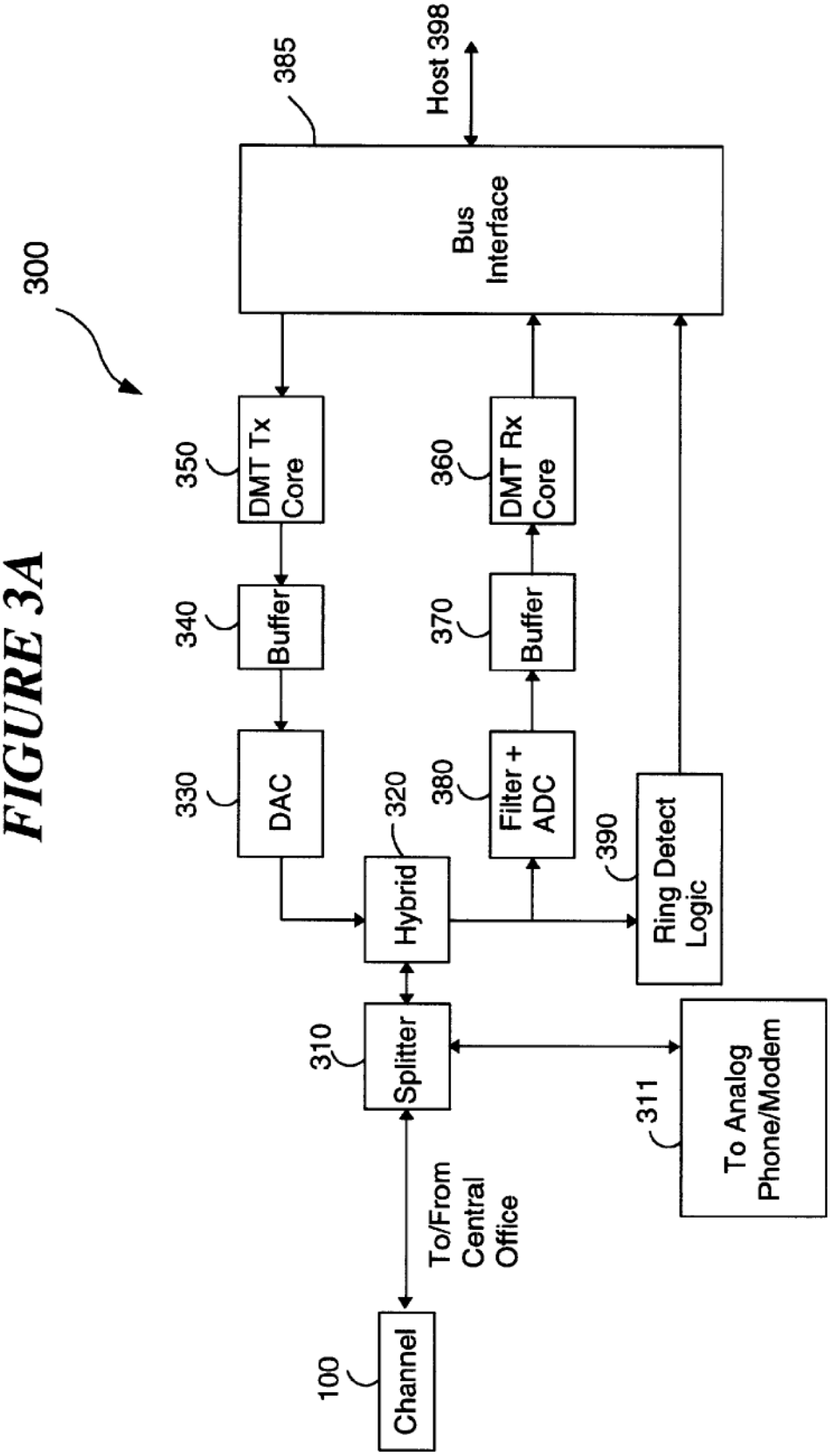

300
385
Host 398
Bus Interface
350
DMT Tx Core
360
DMT Rx Core
340
Buffer
370
Buffer
330
DAC
320
Hybrid
380
Filter + ADC
390
Ring Detect Logic
310
Splitter
311
To Analog Phone/Modem
To/From Central Office
100
Channel

FIGURE 3A

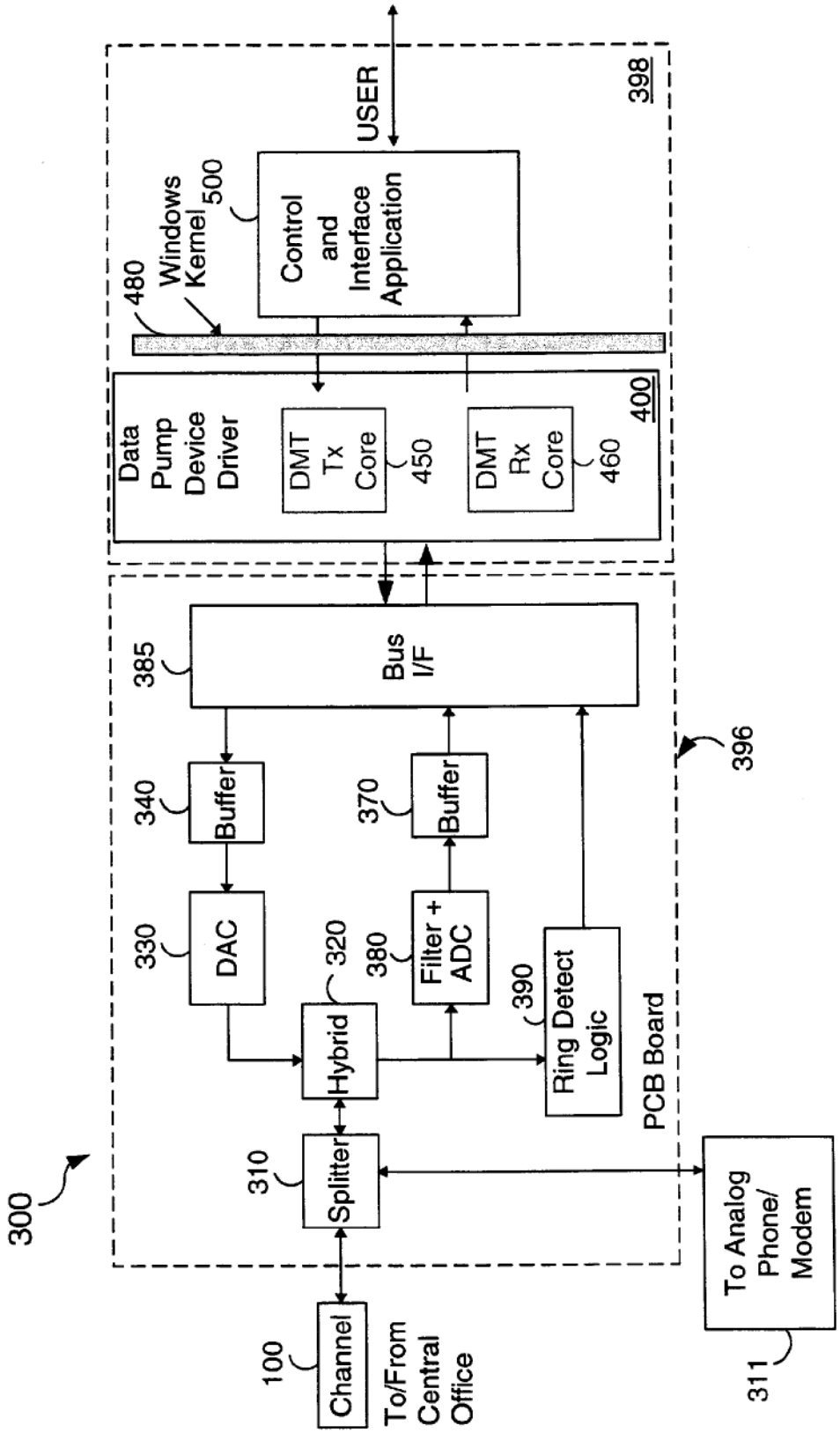

USER
398
Windows Kernel
500
480
Control and Interface Application
Data Pump Device Driver
DMT Tx Core
450
DMT Rx Core
460
400
385
Bus I/F
396
340
Buffer
370
Buffer
330
DAC
320
380
Filter + ADC
390
Ring Detect Logic
Hybrid
PCB Board
300
310
Splitter
To Analog Phone/ Modem
100
Channel
To/From Central Office
311

FIGURE 3B

FIGURE 4

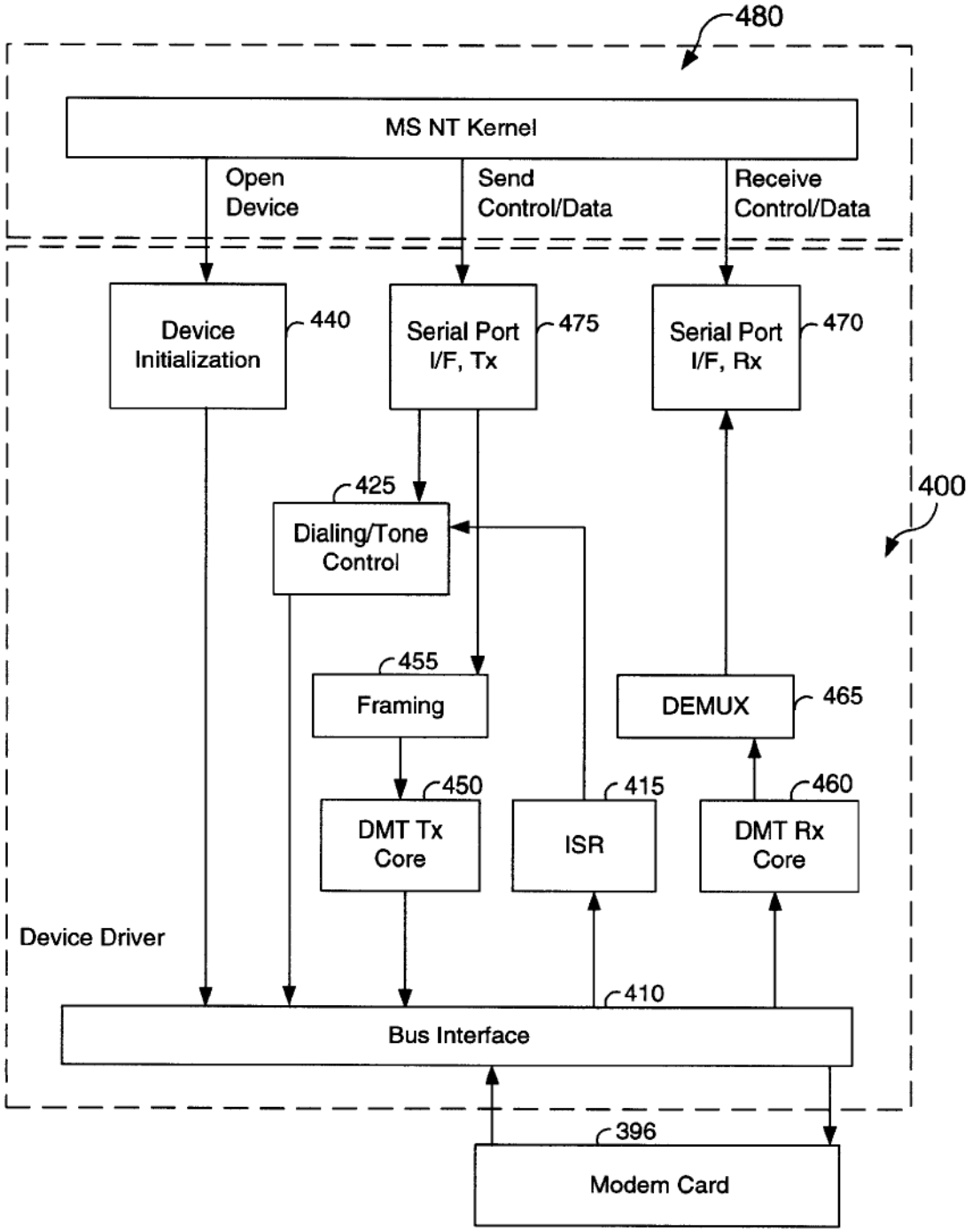
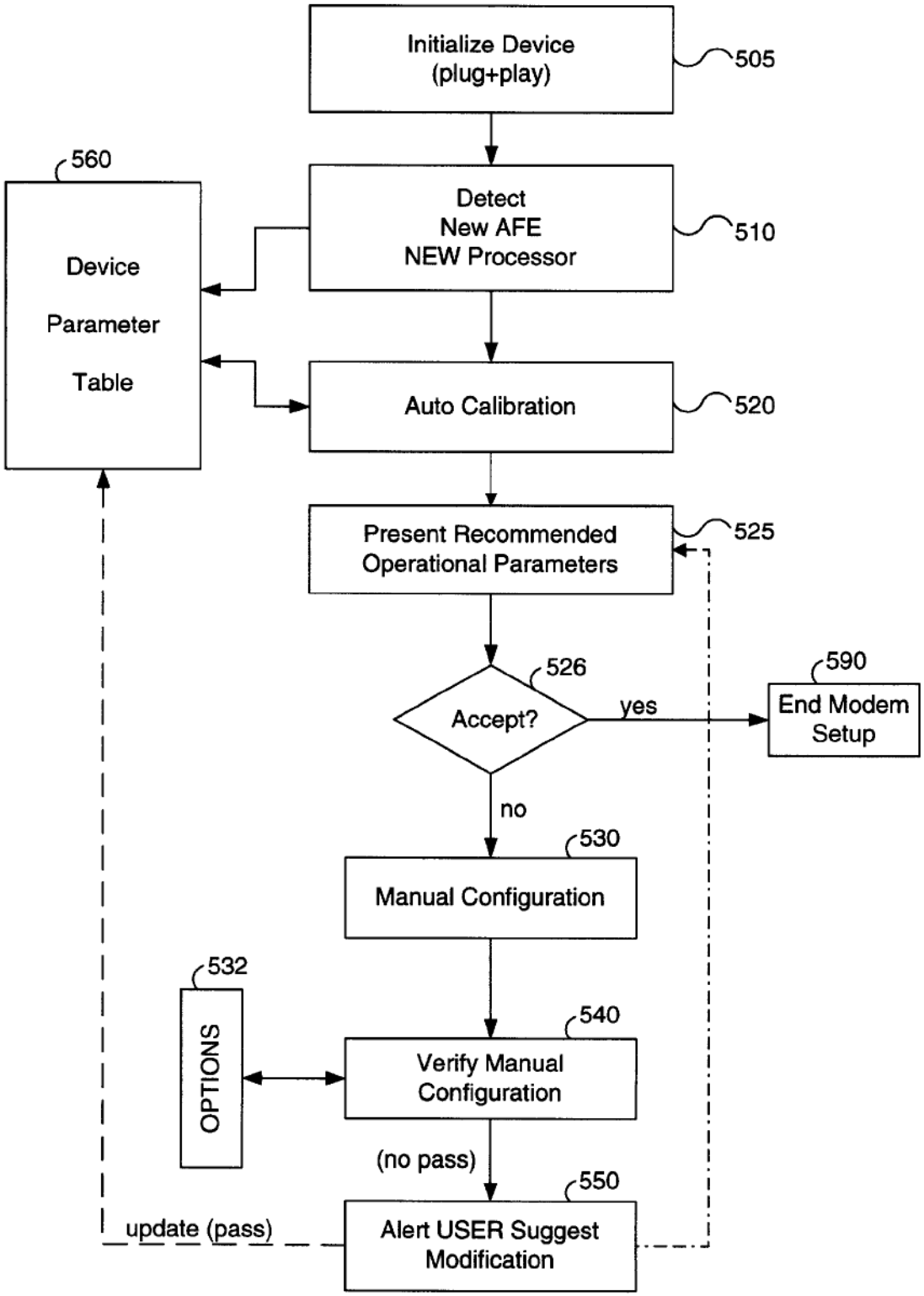

480
MS NT Kernel
Open Device
Send Control/Data
Receive Control/Data
Device Initialization
440
Serial Port I/F, Tx
475
Serial Port I/F, Rx
470
425
Dialing/Tone Control
400
455
Framing
DEMUX
465
450
415
460
DMT Tx Core
ISR
DMT Rx Core
Device Driver
410
Bus Interface
396
Modem Card

FIGURE 5


Initialize Device
(plug+play)
505
560
Device
Parameter
Table
Detect
New AFE
NEW Processor
510
Auto Calibration
520
Present Recommended
Operational Parameters
525
526
Accept?
yes
590
End Modem
Setup
no
530
Manual Configuration
532
OPTIONS
540
Verify Manual
Configuration
(no pass)
550
update (pass)
Alert USER Suggest
Modification

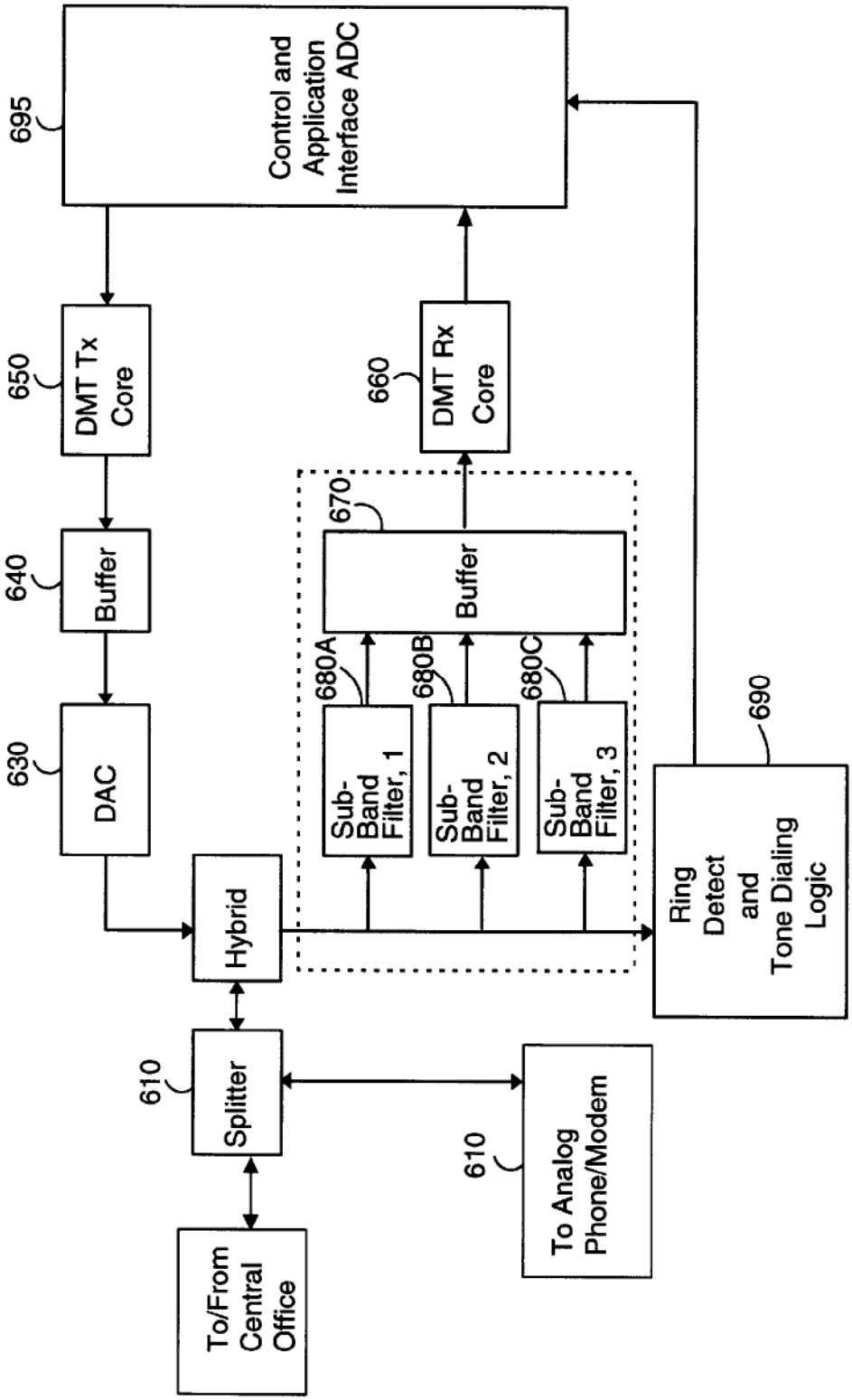

695
Control and Application Interface ADC
650
DMT Tx Core
660
DMT Rx Core
640
Buffer
670
Buffer
630
DAC
680A
680B
680C
Sub-Band Filter, 1
Sub-Band Filter, 2
Sub-Band Filter, 3
690
Ring Detect and Tone Dialing Logic
Hybrid
610
Splitter
610
To Analog Phone/Modem
To/From Central Office

FIGURE 6

FORWARD COMPATIBLE AND EXPANDABLE HIGH SPEED COMMUNICATIONS SYSTEM AND METHOD OF OPERATION

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is related to the following additional applications, all of which are being filed concurrently herewith:

Ser. No. 08/884,979, now U.S. Pat. No. 6,092,122, entitled "xDSL DMT Modem Using Sub-channel Selection to Achieve Scaleable Data Rate Based on Available Signal Processig Resources."

Ser. No. 08/884,957, now U.S. Pat. No. 6,128,335, entitled "Software Rate Adaptable Modem With Forward Compatible and Expandable Functionality & Method of Operation."

Ser. No. 08/884,958, now U.S. Pat. No. 6,065,060, entitled "Modular Multiplicative Data Rate Modem & Method of Operation."

Ser. No. 08/884,956, entitled "Device Driver For Rate Adaptable Modem With Forward Compatible and Expandable Functionality."

Ser. No. 08/884,959, now U.S. Pat. No. 6,073,179, entitled "Program for Controlling DMT Based Modem Using Sub-channel Selection to Achieve Scaleable Data Rate Based on Available Signal Processing Resources."

FIELD OF THE INVENTION

The invention relates generally to an improved high-speed communications system which establishes a data link using only a selectable portion of the total available bandwidth of a channel. The present invention has particular applicability to systems which use rate adaptable techniques such as the discrete multi-tone modulation (DNM technique and CAP for transmitting data in Digital Subscriber Lines and similar environments. By limiting the data throughput of the link to some adjustable fraction of the total available data rate, the present invention significantly reduces hardware costs and allows a downstream user to configure a data link whose performance is directly controllable by the processing power available to such user. In this manner, the system is completely forward compatible and expandable in functionality, and permits a user to increase throughput to the point of achieving full potential of the available channel bandwidth .

BACKGROUND OF THE INVENTION

Remote access and retrieval of data and information are becoming more desirable and common in both consumer and business environments. As data and information transfer is becoming more and more voluminous and complex, using traditional data links such as voice-band modems is too slow in speed. For example, the use of the Internet to locate and access information is increasing daily, but the retrieval of typical graphics, video, audio, and other complex data forms is generally unsatisfyingly slow using conventional voice-band modems. In fact, the slow rate of existing dial -up analog modems frustrates users, and commerce and interaction using the Internet would have been even higher were it not for the unacceptable delays associated with present day access technology. The ability to provide such desired services as video on demand, television (including HDTV), video catalogs, remote CD -ROMs, high-speed LAN access, electronic library viewing, etc., are similarly impeded by the lack of high speed connections.

Since the alternatives to copper line technology have proven unsatisfactory, solutions to the high speed access problem have been focused on improving the performance of voice band modems. Voice band modems operate at the subscriber premises end over a 3 kHz voice band lines and transmit signals through the core switching network; the phone company network treats them exactly like voice signals. These modems presently transmit up to 33.6 kbps over a 2-wire telephone line, even though the practical speed only twenty years ago was 1.2 kbps. The improvement in voice band modems over the past 20 years has resulted from significant advances in algorithms, digital signal processing, and semiconductor technology. Because such modems are limited to voice bandwidth (3.0 kHz), the rate is bound by the Shannon limit, around 30 kbps. A V.34 modem, for example, achieves 10 bits per Hertz of bandwidth, a figure that approaches the theoretical Shannon limits.

There is a considerable amount of bandwidth available in copper lines, however, that has gone unused by voice band modems, and this is why a proposal known as Asymmetric Digital Subscriber Line (ADSL) was suggested in the industry as a high-speed protocol/connection alternative. The practical limits on data rate in conventional telephone line lengths (of 24 gauge twisted pair) vary from 1.544 Mbps for an 18,000 foot connection, to 51.840 Mbps for a 1,000 foot connection. Since a large proportion of current telephone subscribers fall within the 18,000 foot coverage range, ADSL can make the current copper wire act like a much "bigger pipe" for sending computer bits and digital information (like movies and TV channels), while still carrying the voice traffic. For example, an ADSL modem can carry information 200 times faster than the typical voice band modem used today.

ADSL is "asymmetric" in that more data goes downstream (to the subscriber) than upstream (back from the subscriber). The reason for this is a combination of cost, demand, and performance. For example, twisted pair wiring coupling increases with the frequency of the signal. If symmetric signals in many pairs are used within a cable, the data rate and line length become significantly limited by the coupling noise. Since the preponderance of target applications for digital subscriber services is asymmetric, asymmetric bit rate is not perceived to be a serious limitation at this time. Therefore, the ADSL standard proposes up to 6 Mbps for downstream, and up to 640 kbps for upstream. For example, video on demand, home shopping, Internet access, remote LAN access, multimedia access, and specialized PC services all feature high data rate demands downstream, to the subscriber, but relatively low data rates demands upstream. The principal advantage is that all of the high speed data operations take place in a frequency band above the voice band, leaving Plain Old Telephone Service (POTS) service independent and undisturbed, even if an ADSL modem fails. ADSL further provides an economical solution for transmission of high bandwidth information over existing copper line infrastructures.

Specifically, the proposed standard for ADSL divides the available transmission bandwidth into two parts. At the lower 4 kHz band, ordinary (POTS) is provided. The bulk of the rest bandwidth in the range from 4 kHz to about 1 MHz is for data transmission in the downstream direction, which is defined to be from the exchange to the subscriber. The upstream control channel uses a 160 kHz band in between. The signals in each channel can be extracted with an appropriate band -pass filter.

A DMT implementation of ADSL uses the entire available 1 MHz range of a copper phone line. It merely splits the signal into 255 separate channels, and each 4 kHz channel can be made to provide a bit rate up to the best present day voice band (33.6 kbs) modems. This results essentially in overall performance which is equivalent to around two hundred V.34 modems used in parallel on the same line. Because each channel can be configured to a different bit rate according to the channel characteristics, it can be seen that DMT is inherently "rate-adaptive" and extremely flexible for interfacing with different subscriber equipment and line conditions. A number of problems arise, however, in attempting to implement a full scale ADSL transceiver cost-effectively.

First, to achieve this high bit rate transmission over existing telephone subscriber loops, advanced analog front end (AFE) devices, complicated digital signal processing techniques, and high speed complex digital designs are required. As a result, this pushes current technology limits and imposes both high cost and power consumption. For example, AFE devices in modem applications provide the interface between analog wave forms and digital samples for digital hardware/software processing. In high speed modem technologies such as ADSL, AFE devices need to operate at a very high sampling rate and high accuracy. For example, the DMT technology has a spectrum of 1 MHz and requires sampling above 50 MHz if a sigma-delta analog-to-digital (ADC) method is used. This thus requires the state-of-art ADC technology and imposes a high cost for end users.

Second, the time domain signal in ADSL/DMT transmissions is a summation of a large number of carriers modulated by quadrature amplitude modulation (QAM). This typically results in a large peak-to-peak deviation. As a result, even though a high speed AFE is made possible, a large dynamic range and high resolution AFE is required at the same time to minimize quantization errors.

Third, in addition to the high sampling rate and resolution requirement for ADSL AFEs, the other hardware and software in ADSL environment also needs to operate at a much higher speed than current conventional modem counterparts. For example, to implement the DMT technology in software, a custom and dedicated digital signal process (DSP) of a power of several hundred MIPS (millions instructions per second) is required to process many components such as error encoding and decoding, spectrum transforms, timing synchronization, etc. As with the AFE part of the system, this high speed requirement for the signal processing portion of ADSL also results in less flexible, high component costs.

Fourth, requiring a communications device (such as a modem) to filly support the total throughput of a standard such as ADSL may be inefficient in some cases, since many prospective users of high-speed data links may not need to use all the available bandwidth provided by such standards. It is generally more preferable therefore to permit users to throttle or scale the data throughput in a manner they can control, based on their particular application needs, hardware cost budget, etc. For example, a full-scale ADSL system may have the performance level of 200 times conventional V.34 modems, but it is apparent that even a performance improvement of 10–20 times than present day available analog modems would be sufficient for many consumer applications, such as Internet access and similar uses. Thus, unlike conventional analog modems, which are available in various speeds varying generally from 14.4 to 56 Kbps, there are no known ADSL modems which offer scalable performance levels to users.

Fifth, in addition to the implementation challenge, the T1E1.4 ADSL standard does not specify the system interface and user model. Although various high level interface to support T1/E1, ATM, etc. have been described, system integration with high level protocols such as TCP/IP and interface with computer operating systems have not yet been defined. As a result, there is uncertainty how existing and future modem-based applications can work with the ADSL technology. For example, when users run an Internet application which sends and receives data to and from an Internet service provider [SP), a mutually agreed protocol is required to set up a call and transfer data. Possible protocols available at various levels include ATM (asynchronous transfer mode), TCP/IP, ISDN, and current modem AT commands. Either one of these or a possibly new protocol needs to be defined to facilitate the adoption of ADSL technology.

SUMMARY OF THE INVENTION

An object of the present invention therefore is to provide a communications system which is fully compatible with high speed, rate adaptable protocols such as are used with ADSL, but which system is nevertheless implementable with simpler analog front end receiving/transmitting circuitry and is thus reduced in cost and complexity;

A further object of the present invention is to provide a communications system which is fully compatible with high speed, rate adaptable modulation protocols such as used with ADSL, but which system is nevertheless implementable with simpler digital signal processing circuitry and is thus reduced in cost and complexity;

Another objective of the present invention is to provide a method for transmitting data within a fractional, desirable portion of available bandwidth in a channel by modulating only a limited number of desirable sub-channel data carriers, so that a high speed data link can be achieved that is faster, and has reduced computation and hardware demands;

Yet a further objective of the present invention is to provide a communications system with smaller peak-to-peak deviation in the sub-channels signals, so as to reduce the dynamic range required for the front end ADC, and to minimize quantization errors.

Another objective of the present invention is to provide a high speed communications system having a data throughput that is easily controllable and expandable, so that the performance range of such system can be configured to any fractional percentage of total bandwidth available in a transmission channel, up to and including full bandwidth use of the channel;

A related objective of the present invention is to provide a high speed communications system that is modular so that forward compatible and expandable functionality can be incorporated flexibly and with a minimum of effort on the part of a user of such system;

Yet a further objective is to provide a system that is compatible with high speed protocols used in ADSI, but which is also easily adaptable to support preexisting high level data protocols, including those presently used for controlling high speed voice band modems;

A further object of the present invention is to provide a high speed communications system that self-calibrates its own performance level, based on the processing power available to such system;

Another objective of the present invention is to provide a high speed communications system that permits a user to configure the performance parameters of such system using

conventional personal computer hardware, software and operating systems;

A further object of the present invention is to provide an interface between a host operating system and a high speed communications system that provide forward compatible and expandable functionality;

An additional aim of the present invention is to provide an improved system for concurrent control of conventional voice data traffic on a POTS channel, and upstream/downstream communications on separate sub-channels; These objects and others are accomplished by providing a communications system that permits a host processing device to receive selected data within a narrow bandwidth from an upstream transciever which can and normally transmits a large bandwidth analog data transmission signal through a connected channel. A channel interface circuit AFE samples the received analog signal to generate a digital signal. Only a limited portion of the bandwidth may be sampled, thus reducing front end complexity. A digital signal processing circuit then extracts the selected data from this limited digital signal, which is significantly easier to process than a full bandwidth digital signal. Feedback information is provided back to the upstream transmitter which causes the upstream transmitter to transmit downstream data thereafter only using the limited bandwidth of the front end, and not the full bandwidth. This feedback information contains information about the channel that suggests to the upstream transmitter that the other bandwidth in the channel is unusable. In this manner, the upstream transceiver is trained to accommodate the lower rate downstream transceiver in a manner that nevertheless preserves protocol integrity.

In a preferred embodiment, the large bandwidth analog data transmission signal is comprised of a number of DMT modulated sub-channels, and an anti-aliasing filter on the front end of the the downstream transceiver ensures that only a limited number of such sub-channels are processed by a DMT signal processing core. The feedback information consists of non-zero SNR information for the selected sub-channels, and a sub-channel blackout "mask" to eliminate the potential use of other sub-channels. The feedback information is sent by way of a front end transmitting circuit which transmits an upstream data transmission using a second frequency range different from the downstream transmission.

One implementation of the aforementioned high speed system is in a personal computer, so that the signal processing can be accomplished using a processor within such computer, which in a preferred embodiment is an X86 compatible processor. Another implementation of the aforementioned high speed system uses a dedicated signal processor for demodulating the selected sub-channels. This cuts down on processing overhead requirements for a host processing system incorporating the system. In such implementations the portion of the downstream data transmission to be processed for data extraction can be configured by a user of such systems, or alternatively, it can be dynamically determined based on an evaluation by the digital signal processing circuit of performance characteristics of different portions of the frequency spectrum within the bandwidth potential of the upstream transceiver.

In another variation, the data rate of a system such as described above can be increased by processing data from an additional second limited frequency bandwidth portion of the total available downstream bandwidth. In a preferred embodiment, this can be done by including a number of anti-aliasing filters in a modular bank as part of the analog front end section, each of which passes a different frequency bandwidth portion. By making the analog front end modular, the data rate of the overall system can be scaled in a controllable and cost-effective fashion. At the same time, each analog front end portion can be operated at a slower sampling clock and smaller dynamic range. This results in a more relaxed speed requirement and smaller quantization noise at a given number of bits per sample.

The present disclosure also includes an interface to an operating system, to facilitate controlling the high speed communications system when it is incorporated in a personal computer system. This interface ensures that the operating system treats such communications system essentially the same as other prior art voice band modems, and in a preferred embodiment, is a device driver for the Windows NT operating shell. Finally, the present disclosure also describes an applications program which permits a user of a personal computer to control the performance characteristics of the high speed communications system by setting certain system parameters when such system is incorporated in a personal computer system. This program includes an auto calibration routine for setting such system parameters, or alternatively a user of such program can tailor the settings subject to confirmation of the efficacy of such settings based on an evaluation of the processing power available to such user.

Although the inventions are described below in a preferred embodiment implementing the ADSL standard, it will be apparent to those skilled in the art the present invention would be beneficially used in any high speed rate-adaptable applications.

It should be noted that while some prior art devices also have limited mechanisms for achieving a reduction of nominal or peak transmission speed in a channel, they only activate or implement such mechanisms as a failback response to a failure in the channel, or because of a transmission rate reduction in the upstream transceiver. Unlike the present invention, such prior art modems, during an initialization process, attempt to establish the highest possible transmission rate achievable by the channel and the upstream transciever. In other words, any rate reduction imposed by the downstream modem is typically considered an unintended and undesirable side effect of bad channel characteristics, and not a desirable and intentional design target as set forth in the present invention. In addition, the data rate reduction in such modems is accomplished primarily by varying the number of bits per baud (hertz) at a fixed frequency, and not by controlling the overall frequency spectrum of the downstream data transmission. Moreover, in such prior art systems, no effort is made to measure, identify or use an optimal portion of the usable bandwidth or set of transmission sub-channels. Instead, such prior art systems typically use whatever available bandwidth or sub-channels happen to be usable at that instant in time.

Similarly, while a fixed 300 baud rate downstream modem can work with an upstream 33 kbs rate modem this arrangement is also unlike the present invention. This is because, again, the bandwidth reduction in such prior art device is so large that it is considered commercially unusable by today's standards. Furthermore, the smaller bandwidth modem is not compatible with, and does not support, the higher protocols of the higher bandwidth modem, which is also undesirable from an implementation standpoint. Stated another way, unlike the present invention, the lower end modem limitations of prior art system force the data link to be set up using a low level protocol that does not take advantage of the full capabilities of more advanced protocols.

Finally, there is no mechanism for users of either of the prior art systems noted above to expand the functionality of such modems in a controlled, flexible, and modular manner.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a pictorial depiction of the ADSL/DMT bandwidth allocation for upstream and downstream data in a channel based on frequency division multiplexing (FDM) configuration.

FIG. **1**B shows the relationship between a sub -band filter and an analog to digital converter that can be used in an analog front end (AFE) of the present invention;

FIG. **1**C is a pictorial depiction of a SNR curve for a typical subscriber loop channel using sub-channel modulation;

FIGS. **1**D–**1**G are mathematical modellings and charts that further explain the underlying physical premises of the present invention based on DMT;

FIG. **2** is a block diagram of a general implementation of a communications system employing the present invention, adapted for use in an ADSL environment;

FIG. **3**A is a block diagram of a dedicated hardware implementation of a communications system employing the present invention, also adapted for use in an ADSL environment;

FIG. **3**B is a block diagram of a mixed hardware an d software based implementation of a communications system employing the present invention, also adapted for use in an ADSL environment;

FIG. **4** is a block diagram depicting the general structure of the data pump device driver used in the mixed implementation shown in FIG. **3**;

FIG. **5** is a flowchart depicting the general operation of the control and application interface used in the mixed implementation shown in FIG. **3**

FIG. **6** is a block diagram of an implementation of a communications system employing the present invention, also adapted for use in an ADSL environment, in which it is depicted how a user can modularly expand throughput capability by adding additional AFE stages to process a greater percentage of the available bandwidth in the channel.

DETAILED DESCRIPTION OF THE INVENTION

While some of the concepts set forth immediately below are well-known, a brief explanation of ADSL technology is provided with reference to FIG. **1** to facilitate an understanding of the present invention. As explained above, it is well-known in the art to use DMT to effectuate the ADSL standard. In contrast to most modulation schemes, such as AM/FM transmissions that use one carrier, DMT uses multiple carriers to transmit data bits. Specifically, T1E1.4 ADSL standards specify an up to 255 channels for downstream transmission from the central office to subscribers and up to 31 channels for upstream transmission from subscribers to the central office. As shown in FIG. **1**, each carrier has a bandwidth of 4.3125 kHz. The total bandwidth is 1.1 MHz for a total of 255 channels. In the upstream direction, a "pilot" tone in the approximate range of 69 kHz, is used for maintaining timing synchronization. A similar pilot tone is transmitted in the downstream direction in the vicinity of 276 kHz.

Since upstream and downstream transmissions are over the same 2-pair twisted wire, they need to be separated by either echo cancellation (EC) or frequency division multiplexing (FDM). Echo cancellation allows simultaneous transmissions in both directions but requires a complex echo canceler implementation. On the other hand, FDM uses two different frequency bands for separate downstream and upstream transmissions. As shown in FIG. **1**, the upstream transmission uses subchannels from channel number 6 to 31, and the downstream transmission uses subchannels from channel number 41 to 255. While the remainder of the discussion below focuses on an system employing FDM, it will be appreciated by those skilled in the art that the present invention is adaptable and can be used beneficially with echo-cancellation approaches as well.

As with most communication environments, the transmission bit rates for both upstream and downstream communications in ADSL are not fixed but instead are determined by the quality of the channel. In the present invention, a number of well-known techniques can be used advantageously for setting up the initial data link. In general, these techniques work as follows: during initialization, the channel quality is measured and a certain data rate (typically a number of bits) is assigned for each DMT sub-channel; thereafter, a "handshaking" process is used to dynamically and adaptively change the bit loadings (and energy levels). The latter is often necessary because (among other things) changes may occur in the overall channel characteristics, changes in the target bit rate may be needed, or new bit distributions in the sub-channels may be required because of degradations in one of the sub-channels. The quality of the sub-channel response can be measured by the received signal to noise (SNR) ratio. According to the Shannon theorem, the upper limit of the number of bits per unit Hz that can be transmitted is $\log_2(^1 + \text{SNR})$. Therefore, by measuring the received SNR at the receiver end, one can determine the number of bits allocated for each sub-channel modulation. The total data throughput rate achieved by the system, therefore, is simply the sum of all the data rates of all the usable subchannels.

According to the T1E1.4 ADSL standards, data bits are grouped and processed every 250 μsec. The number of bits that can be processed over one such time frame is the summation of the bits allocated for each subchannel determined from the previous channel response measurement. For a given number of bits assigned to a certain subchannel, quadrature amplitude modulation (QAM) is used to convert bits to a complex value, which is then modulated by the subchannel carrier at the corresponding frequency.

The above is a merely a brief summary of the general operation of a typical DMT/ADSL communications system. The general circuits used in prior art ADSL systems, the specifics of the bit/energy loading process for the subchannels, the bit fine tuning process, and the details of the modulation of the sub-channels, are well-known in the art, and will not be discussed at length herein except where such structures or procedures have been modified in accordance with the teachings herein.

The full downstream data throughput of a typical prior art ADSL standard transceiver approaches 6 Mbps, which is more than 200 times the speed of conventional analog modem technology. This requirement was imposed since a large part of the initial motivation to implement ADSL was to achieve high speed multimedia communications and video teleconferencing. Nevertheless, a large number of potential users do not want or need to have such wide bandwidth capability. For example, many potential users of ADSL (or similar high speed loops), including many who are intending to use such links primarily for Internet access, only need to achieve downstream transmission speeds that

are in the hundreds of kilobits per second range. This data rate is in fact achievable using only a fraction of the available bandwidth of ADSL. By processing only a fraction of the available bandwidth of the ADSL standard, the present invention permits a limited but extremely useful ADSL modem to be implemented with significantly less expense and complexity than previously possible. At the same time, because the present invention has modular characteristics, the proposed implementation of the present invention affords users an easy path to forward and upward expansion of the overall functionality of their system. The principle behind this aspect of the present invention is as follows: As shown in FIG. **1**B, if the transmission in the channel is restricted to a smaller bandwidth by an anti-aliasing filter **80**, according to the Nyquist sampling theorem, the sampling rate of AFE devices (such as ADC **81**) that perform analog to digital conversion can be significantly reduced. Specifically, if the total downstream bandwidth is limited to some fractional total B Hz (in a preferred embodiment using DMT in an ADSL environment, B=20 DMT channels or about 86 kHz) as shown below, we can limit the Nyquist sampling rate to around 180 kHz. This is achievable with ADCs having greatly simplified hardware and reduced performance requirements, in contrast to the full ADSL bandwidth approach, which processes 200 DMT channels or 900 kHz in the case of full ADSL implementation.

The total accumulated bit rate of an ADSL communications system using the present invention can be calculated as follows. Suppose a total number of k subchannels (out of a total of M possible) are to be supported and each channel is allocated bk bits for transmission. The total accumulated bit rate (R) is:

$$R=(\Sigma_{i=1,k}bi)*4 \text{ kHz (bits/sec)}$$

where 4 kHz is the framing rate defined by T1E1.4 ADSL standards. If k=20 channels and the average number of bits per channel is 6, then total bit rate (R) is approximately 480 kbits/sec. It can be seen that this fractional use of the ADSL bandwidth nevertheless provides about 9 times the performance of a conventional analog 56 kbits/sec digital modem. The benefits of this approach of the present invention are apparent. The overall performance and cost of a high speed communications system can be scaled and controlled in direct relationship to the particular needs of particular users. In general, the data rate supportable by (and the relative cost of) any particular implementation of the present invention is generally determined by two factors: (1) the capacity of the AFE; and (2) the capacity of the hardware performing the DMT.

The capacity of an AFE is generally measured by the maximum sampling speed it can achieve. As explained above, the sampling speed in turn determines the upper limit of the frequency band B (in kHz) that can be obtained. At the defined channel separation of 4.3125 kHz for ADSL, the total number of subchannels that can be supported is less than or equal to B/4.1325. A suitable ADC can be selected, therefore, based on the particular data rate and cost requirements of any particular user.

The other factor that limits the number of subchannels (and achievable data rate) is the processing power available for DMT modulation and demodulation routines. For example, a variety of performance levels (achievable data rates) are possible with well-known dedicated signal processing hardware, such as digital signal processors, as discussed in more detail below with reference to FIG. **2**. Alternatively, as shown in FIG. **3**, if such routines are implemented primarily by software and run by a host CPU, the required processing power (MPS) generally increases directly as function of the number of subchannels that need to be processed. This is because, in general, most of the processings are done in serial, or a channel by channel basis. As discussed below in more detail, the present invention makes use of a "calibration" routine for estimating the total available processing power of a user's computing system in order to set an upper limit of the total subchannels that can be supported.

Irrespective of the selection of the particular AFE or signal processing technique used, however, another useful (but not essential) aspect of the present invention is that the sub-channels with the largest signal to noise ratio (SNR) within the passband are selected for data transmission. In other words, in the preferred embodiment of the present invention, those k subchannels within the passband that support the largest number of bits are used for processing. As seen in FIG. **1**C, for example, a standard two-wire subscriber line typically has a SNR curve that exhibits extensive attenuation with higher frequencies. It can be seen roughly in this figure that while there are more than 200 sub-channels provided for downstream transmission in ADSL, it is typically the case that 50% of the maximum data rate can be accomplished using only a much smaller percentage (than 50%) of the subchannels. This fact is especially useful in considering some of the shared/ multi-channel bandwidth embodiments discussed further below.

The present invention, therefore, permits an implementation for a high speed data communications system that makes use of the best portion of the channel, while still being upwardly compatible and forward expandable. By these terms, it is meant that a system constructed in accordance with the teachings herein is completely compatible with a fully implemented version ADSL DMT modem. Moreover, it will be apparent to those skilled in the art that appropriate modifications specific to the channel and data link protocols and standards can be made so that the present invention can be advantageously employed in non-ADSL environments as well. Upward compatibility and forward expandability refer to the fact that systems constructed with the present teachings can have data rates that are easily upgraded while still preserving and maintaining compatibility with existing standards. For example, lower end users desiring less bandwidth can achieve a satisfactory performance with a minimum of cost, and can then upgrade the performance levels of their systems at later time by suitable (and preferably modular) upgrades of the AFE and signal processing hardware/ software.

A system constructed in accordance with the present teachings is completely compatible with the full ADSL standard because of the following two aspects: According to the rate adaptation feature specified by the T1E1.4 ADSL standards, the bit rate for each sub-channel is determined initially (and preferably dynamically on an ongoing basis) by the sub-channel SNR analysis. Specifically, an ADSL downstream receiver can inform an upstream ADSL transmitter about the quality of the transmission; the receiver can also decide the bit rate for each sub-channel. Therefore, a downstream, partial-channel bandwidth receiver using the present invention can (based on the speed and passband of such receiver) supply an upstream, full-standard ADSL transmitter with information or control signals to effectuate a transmission only in selected sub-channels. In particular, in a preferred embodiment, the upstream ADSL transmitter is provided with SNR information for sub-channels outside the passband that is artificially contrived so as to suggest to the upstream transmitter that these sub-channels are not usable.

In this manner, the downstream transmission is limited to a certain number of subchannels within the AFE and signal processing capabilities of the receiver. It can be seen, nevertheless, that this scheme is completely transparent to the transmitter, thereby permitting a system built in accordance with the present teachings to be fully compatible with the ADSL standard. While not possible at this time within the ADSL standard, it is apparent that other high-speed data protocols may use a control signal, instead, to provide for express limiting and control of the identity of the sub-channels transmitting information.

As the technology improves for AFE devices and DMT implementation, the number of subchannels supported by a system using the present invention can increase. As a result, such systems can upgrade completely to a full T1E1.4 ADSL implementation using a single higher end modular replacement AFE devices, or alternatively, a number of lower end modular AFE devices.

General Embodiment of Present Invention

The basic structure of the present invention is depicted generally in FIG. **2**. In general, the present invention can be embodied in different combinations of hardware and software. The primary difference between these embodiments is the specific implementation of the DMT core. These specific embodiments are described in more detail below with reference to FIGS. **3**A and **3**B.

The structure and operation of ADSL transceivers is well-known in the art, and for that reason the present description primarily details those aspects of such transceivers which are necessary to an understanding of the inventions herein. As seen in FIG. **2**, a channel **100** is made of a regular copper wire "loop", and each such loop may have differing electrical properties, transmission lengths (sizes), varying attenuation characteristics, and a number of impairments or interferences. Splitter **210**, a conventional and well-known circuit, separates a DMT signal occupying more than **200** sub-channels from a lower end 4 kHz POTS analog signal. The latter can be used for simultaneous voice or conventional analog modem. Hybrid circuit **220** is also well-known in the art, and consists primarily of conventional transformers and isolation circuitry used in a wide variety of high-speed devices interfacing to standard telephone lines. A ring detect logic circuit **290** can also be implemented using accepted techniques, to alert a Control Interface **295** to the existence of a transmission signal originating from an upstream transceiver (not shown).

The full bandwidth signal is either low passed or bandpass limited to a frequency width B by suitable, well-known techniques as it passes through bandpass Filter and Analog/Digital Converter **280**, so that only a fraction of the signal in the frequency domain is passed on to Buffer and DMT Receive Core **260**. Again, the only important consideration for Subband Filter **280** is that it must constrain the bandwidth of the incoming signal to be $\leqq$B, where the sampling rate of the Analog/Digital Converter is $\geqq$2B. This can be accomplished by using well-known filter designs. By suitable selection of circuitry for Filter and ADC **280**, the overall system cost and performance can be scaled accordingly. In a preferred embodiment, the signal passed through Filter and ADC **280** occupies a spectrum between approximately 200 and 400 kHz. This selection is based primarily on an expected average performance of a typical two-wire line. It will be apparent to those skilled in the art that different bandpass widths and regions may be more suitable or optimal for other kinds of data links, or other kinds of multi-carrier modulation schemes. Moreover, in some instances, while it is somewhat more expensive to implement, an adaptive or tunable filter may be substituted, such that the target frequencies of the passband are adjustable uniquely for each new data link. In such cases, the bandpass can be configured to coincide with the sub-channels having the highest achievable SNR, including the subchannels that must be supported for protocol or other system overhead reasons. Also, in some applications, the analog-to-digital conversion may be performed by a digital signal processor, or by the host computer and therefore, the sampling rate can be dynamically controlled and matched to the bandpass target frequency and frequency breadth. This feature, in turn, would assist dynamic scaling of the data throughput based on system computing power and overhead requirements.

Furthermore, in this preferred embodiment, using a multi-carrier approach implementation for ADSL, a pilot tone at 276 kHz must be allowed within the passband. It is apparent that other protocols may require similar pilot tones, and the design of comparable filters to achieve the functionality of Filter and ADC **280** is well within the ordinary skill of one in the art. DMT Receiver Core **260** is generally responsible for monitoring and measuring the SNR of the sub-channels falling within the frequency range passed by FILTER and ADC **280**, and for extracting the original data stream from the numerous sub-carriers. In a preferred embodiment, Control Interface **295** receives system configuration information from a host **298**. This information may contain such parameters as target throughput rate R, target error rate, target center frequencies F for FILTER and ADC **280**, target frequency width B, etc. By evaluating the SNR and bit capacities of the sub-channels computed by DMT Receiver Core **260**, and taking into consideration the target data rate R, Control Interface **295** can select a number k of sub-channels up to and including the total available number M of sub-channels to carry the data stream from the upstream transmitter (not shown). The number of sub-channels that can be used for carrying data is directly related to the bandpass frequency B as described above. In a preferred embodiment, M=200+(ADSL) and Control Interface 295 will usually configure k=20.

For every sub-channel other than the selected k sub-channels, a "mask" or blackout control/feedback signal is generated and transmitted by DMT Tx Core **250**, Buffer **240** and DAC **230** to the upstream transceiver. This ensures that any subsequent data transmissions by the upstream transceiver only use the selected k sub-channels. This feedback information is provided, therefore, irrespective of the transmitting capacity of the upstream transceiver, and even during times when the channel **100** is capable of supporting more than k sub-channels. In this manner, the present system is perceived by upstream transceiver to be compatible with protocols and performance characteristics of the upstream transceiver, because the upstream transmitter receives feedback information indicating merely that the two systems are connected through a channel with substantial signal attenuation characteristics for data signals outside the k sub-channels. Based on the inherent rate adaptiveness of ADSL and other similar protocols, the upstream transceiver will automatically train itself to use only the k sub-channels predetermined by the downstream transceiver. It should be noted that the DAC **230** and Buffer **240** in the front end transmitting circuit preferably transmit any upstream data transmissions using a second frequency bandwidth different from that of the downstream data transmission. However, this is not necessary in systems using echo-cancellation. Furthermore, in ADSL applications, the size of this band-

width is considerably smaller, and uses only L sub-channels, where L<M. In other xDSL applications, L may be on the same order or larger than M.

Again, while the ADSL standard fixes the data error rate to be 10^{--7}, it is conceivable that other applications of the present invention may tolerate a reduced error rate. For example, if maximum data throughput is required (i.e., the margin is less constrained) then the largest bit capacity sub-channels within B can be selected. Alternatively, if the system is error-performance driven and has more relaxed throughput requirements, than the subchannels with the best margin are selected. A suitable combination of sub-channels can be selected by one skilled in the art based on the particular system requirements which may vary from application to application. Moreover, Controller Interface **295** may optimize the desired sub-channel mix dynamically depending on the type of data transmitted in channel **100**. For example, streaming audio or video, or pictorial graphics, may require less integrity and error performance than other kinds of data used by n applications programs running on host **298**. The specifics of the structure, operations and techniques used by Controller Interface **295** are not constrained by any requirements of the present invention, and can be implemented in various ways well-known to those skilled in the art.

The operation of the remainder of the circuitry shown in FIG. **2** is also relatively straightforward and not unlike a typical multi-carrier modulation system. Control Interface **295** ensures that DMT Transmit Core **250** performs bit and energy loading only for those sub-carriers necessary to effectuate a selected host throughput rate/error rate combination. As with the circuitry used for Filter ADC **280**, the circuitry for performing the functions of DAC **230** can be implemented in programmable form to allow for greater flexibility. Finally, while not presently supported in ADSL protocols, it is nevertheless possible that the filter in block **280** can be eliminated entirely in some applications when the subchannel or downstream transmission frequencies can be configured through appropriate handshaking or similar procedures. In other words, if the upstream transmitter can be configured to transmit using only a portion of the bandwidth available in the channel, the advantages of the present invention can still be realized, because the ADC portion of block **280** can still be relatively less complex, since it will be processing at a much slower sampling rate than that required for a full spectrum implementation. Moreover, such an implementation would also yield the same commensurate savings in the DMT processing core, and reduced quantization errors.

Some special features of the present invention include the fact that:

(i) unlike hardware architectures implementing a fill T1E1.4 ADSL standard, the present invention uses a filter in the front end. As mentioned earlier, the use of this filter is to allow low speed sampling by the ADC. If suitable handshaking between the upstream and downstream transcievers can be effectuated to generate a reduced downtstream transmission, the filter can be eliminated.

(ii) standard ring detection logic is incorporated to support existing modem features;

(iii) DMT Rx core **260** is basically implemented the same way as specified by T1E1.4, but with some important differences, specifically:

[a] due to subband filtering and lower speed sampling, the frequency channels at the output of FFA (not shown) in the DMT Rx Core have a frequency shift

[b] Since not all 256 subchannels are necessarily supported by the DMT Rx Core **260**, actual FFT implementation can be smaller, simpler and more cost-effective;

(iv) Control logic 295 permits the system to behave essentially like a conventional analog modem, and is used to support necessary setup tasks such as dialing and handshaking;

(v) The use of limited bandwidth from the downstream channel reduces the need for echo-cancellation circuitry, because there is less need for overlap between the upstream and downstream transmissions, and this further reduces system complexity and cost;

(vi) Because a smaller portion of the spectrum is processed by the present invention, the peak-to-peak deviation of the downstream signal is reduced, and this helps to minimize quantization errors.

Dedicated Hardware Based Embodiment

FIG. **3**A illustrates an embodiment of the present invention that can be generally described as a dedicated hardware implementation. For the present discussion of FIG. **3**A, it can be assumed that those circuits having like numbered references are the same and/or perform the same function as their counterpart in FIG. **2**. For example, unless otherwise indicated, there is no material difference between Splitter **210** (FIG. **2**) and Splitter **310** (FIG. **3**A).

In this embodiment, the DMT sub-channel modulation core is implemented completely in dedicated processing hardware. For this application, DMT Receiver Core **260** typically includes a digital signal processor (DSP) (not shown) and including on-board program ROM (or other suitable memory) for storing executable microcode routines for performing bit, energy and SNR measurements of the carriers in the sub-channels. In such an embodiment, due to the power of the DSP, there is typically no need for processing assistance from a user's host processor **398**. This embodiment therefore may be advantageously employed where host processing power limitations are a consideration.

A user of a system shown in FIG. **3**A can expand the functionality (i.e., data throughput rate and modem features) of such system by upgrading the DMT Receiver Core **260**, and where necessary, the AFE **280** as well. The system of FIG. **3**A can be incorporated on a typical printed circuit board. By mounting or packaging the circuits used in such blocks in an accessible fashion, they can be replaced or supplemented much in the same way present users of personal computers can upgrade their motherboards to include additional DRAM. One practical alternative, for example, would be to have multiple available slots to accommodate new subband pass filters for passing a greater portion of the downstream transmission to be processed by the DMT core logic. Other practical and simple variations of this approach will be apparent to those skilled in the art.

Partial Software Based Embodiment

In the above dedicated hardware embodiment, the overall speed (data throughput) can be maximized but with less flexibility for upgrades. This is because upgrades to such a system must take the form of hardware replacements, which can be more costly and difficult for the user to incorporate. On the other hand, as depicted in FIG. **3**B, a number of important functions of a communications system can be completely implemented in software, in an analogous fashion to what is commonly described in the art as a "software" modem. In this case, the overall speed of the system depends on the user's processor power available at host **398**, and only the AFE portion need be implemented in hardware.

The primary differences between the embodiments of FIGS. **3**A and **3**B are the following: (1) implementation of

DMT modulation; (2) implementation of the control and handshaking functions; and (3) implementation of the control interface. As seen in FIG. 3B, DMT Receive Core **460** and DMT Transmit Core **450** are implemented in a data pump device driver by the host system **398**. In a preferred embodiment, host system **398** includes some form of multipurpose microprocessor (such as an x86 type processor) running a suitable operating system (such as Windows by Microsoft), and is capable of executing suitable low level drivers for the DMT modulation (FIG. 4), as well as high level application software for implementing Control Interface **500** (FIG. **5**). Host processor system **398** communicates over a standard bus interface **385** (i.e., a PCI bus) to Front End circuitry **396** for implementing a high speed modem. As with the circuitry in conventional analog modems, this circuitry of the present invention can be effectively incorporated on a PC motherboard (i.e., Bus Interface **385** and Front End Circuitry **396** can be merged so that they are essentially part of host system **398**) or on a separate printed circuit board, or as a stand-alone unit physically separated from host **398**. While this approach may not provide as much throughput performance, it has the advantage of being less expensive than the pure hardware approach of FIG. **2**, and much easier to upgrade.

In the "software" modem implementation of FIG. **3** using a typical PC running Windows, the DMT Tx core **450**, Rx Core **460** and Control/Handshaking logic are implemented as a Windows Data Pump Device Driver **400**, which consist of DMT routines, associated control and handshaking codes, and an interface to kernel **480**.

A more detailed characterization of a portion of host processing system **398** is depicted in FIG. **4**, which illustrates a preferred embodiment of a device driver **400** as it would be constituted for a computer operating system shell **480**. In the present embodiment, Microsoft Windows NT is considered, but it is understood that other comparable environments may be used, including UNIX, Windows 95, etc. As is well-known, operating system **480** is responsible for supervising and controlling the operation of processing system **398** and all of its associated peripheral devices. Operating system **480** also includes various interactive control and graphical application interfaces (FIG. **5**) for permitting a user of processing system **398** to run various applications programs, and to set up, control, configure, monitor and utilize peripheral devices such as disk drives, printers, monitors, modems and the like.

To assist operating system **480** to interact and control such peripheral devices, it is also well-known to use device drivers, which are essentially low-level hardware routines executed by a host processor and operating system. A device driver is a memory image file or executable file that contains all the code necessary to instruct a host processor to interface and drive a particular device within a computing system. Device driver **400** acts as an interface between an operating system 480 (in this case, Microsoft Windows NT) and hardware **396**. In this case, for example, device driver **400** supports hardware **396** (see FIG. 3B), which is embodied in a typical printed circuit board (or external device). The teachings herein therefore provide for a new device driver that in combination with hardware **396** operates as a "software" modem. In this manner, operating system 480 classifies this combination as an ADSL modem, or in other words, another typical personal computer peripheral device, analogous to conventional voice-band modems.

Generally speaking, device driver **400** works as follows: a user of processing system **398** desiring to establish a data link to a remote site for transmitting/receiving data initiates such link through an application program (FIG. **5**). Operating system **480** (FIG. **4**) interprets and services this request by passing control of this task to device driver **400**, which first generates appropriate instructions for a Device Initialization **440**. In a preferred embodiment, Modem card **396** is initialized through Bus Interface **410** using conventional voice band modem control commands, so that the present invention is compatible with preexisting applications programs written for controlling modems using operating system **480**. Similarly, therefore, control and data signals are interpreted and transmitted by operating system **480** to a Serial Port Interface **475** so that conventional modem dialing instructions and handshaking signals can be imparted to Modem Card **396** to establish a link through channel **100** to an upstream conventional ADSL transciever (not shown). As explained above, after suitable handshaking protocols have been completed, the upstream fully compatible ADSL transceiver will begin transmitting data on all available M usable subchannels. This downstream data is filtered by FILTER/ADC **380** and at this time, information for only N subchannels (N<=M) is temporarily held in Buffer **370**. At or before this same time, an interrupt is generated by bus interface **385** and passed through device driver bus interface **410** to alert Interrupt Service Router **415** to the existence of downstream data requiring processing. Thereafter, DMT Receive Core **460** begins processing the downstream data stream in response to control information from ISR **415**.

A demultiplexer **465** extracts and correlates the data in the various sub-channels before passing it on to Serial Port Interface **470**, and back to Operating System **480**. In this manner, Device Driver **400** coordinates with Modem card **396** to effectuate a sofware modem whose performance is directly correlated to the computing power of a processor contained within the host processing device.

As mentioned earlier, Device Driver **400** also contains control information for configuring the number and selection of sub-channels to be used in the particular data link established through channel **100** with the upstream transciever during an initialization process. As also mentioned above, this control information may be self-determined by a user of host processing system **398**, or alternatively, automatically sensed and monitored by such processing system, based on a computing performance rating for such system determined in a calibration routine. In either event, during the initialization process (and at all times subsequent) the upstream transceiver is induced to use such sub-channels only for the ensuing data transmission. This is accomplished by transmitting SNR information that is interpreted by the upstream transceiver as zero for all but K<N of the sub-channels of the driver selection. This data is passed under control of Operating System **480** through Serial Port **475**, Framing control **455** and DMT Transmit Core **450** before being sent out to Modem Card **396** and channel **100**.

It is understood, of course, that ADSL Modem **396** can also respond to a request from a remote modem for initiating the data link. The process for initializing the link, nevertheless, is essentially the same as that described above. Device driver **400** can also contain control logic for supporting typical dial-up modem operations and control codes from conventional modem application programs typically implemented in voice-band modems, such as setting up Originate/Answer modes, monitoring call progress, performing modem diagnostics, configuring receive/transmit buffer sizes, supporting facsimile transmissions, as well as performing enhanced error control, data compression and flow control between Modem Card **396** and Operating System **480**. Device Driver **400** can also support other

conventional "always-on" data link connections as desired, such as may be found in typical ethernet network connections, and other dedicated applications.

Given the teachings of the present invention, the general design of the above Data Pump Device Driver **400** is a routine task well within the abilities of one skilled in the art. The specifics of such implementation are not critical or essential to the present inventions, and will vary from application to application according to system designer requirements, so they are not included here. Again, while this embodiment of the present invention is set out in the context of a PC based host processor running Windows, it will be apparent to those skilled in the art that above description is merely an exemplary implementation. The referenced DMT routines, associated control and handshaking codes can be employed in numerous host processing/operating system environments, and in a variety of different coding organizations (high level or low level processing forms) well-known in the art.

In the preferred embodiment implemented using a standard PC running Windows, Control/Application interface **500** includes Win32 codes which provide standard modem utility functions and interface with Data Pump Device Driver **400**. In FIG. **5**, a flowchart of the operation of the Control/Application Interface **500** can be seen, which interface is discussed in more detail below.

Another particularly beneficial aspect of the embodiment of FIG. **3**B is the provision of a self-determining "performance" or calibration rating that can be used to determine an optimal or maximum data throughput rate. In other words, the system of FIG. **3**B can automatically and adaptively configure a host system **398** to a particular throughput rate based on an evaluation of the available computing power. In a preferred embodiment, the performance rating is determined based on a calibration routine executed by Data Pump Device Driver **400**. This routine sets a timer, and counts how many DMT frames can be processed within the given time; this gives a relative figure of merit for the particular host system in question. For each sub-channel to be added, one DMT frame needs to be processed within a small fraction of 250 μs. Therefore, by incrementally increasing the subchannel count, the overall effect on total system processing overhead can be determined. Control/Application Interface 500 provides the user with control to set a threshold of available host power for implementing the high speed link. Based on this threshold of available power (which can be nominally set to 20%) the number of subchannels that can be supported can be gleaned very quickly.

In view of current technology, when DMT processing is implemented in software, the host processing power is more likely to be the limiting factor than the frequency band of the subband filter **80** in FIG. **1**B. Nevertheless, because host processors (and especially microprocessors) are evolving in performance at a fairly rapid rate, the present invention affords users an opportunity to realize a high speed data link with performance that is controllable, and which improves whenever there is an upgrade in the host processing system. Since many typical present day personal computer systems have easily accessible and replaceable host processors, users of the present invention can easily and flexibly expand and enhance the throughput and functionality of an ADSL modem.

An example of the flow chart for an ADSL modem application/control program **500** designed in accordance with the present teachings is shown in FIG. **5**. With the teachings herein, a user of host processing system **398** can, for the first time, dynamically control a forward compatible and expandable modem, such as an ADSL modem, using modem-control applications software that is analogous to that only previously available for voice band modems. In a preferred embodiment, ADSL Modem Card **396** is automatically detected by Operating System **480** and set up by initialization routine **505** by Modem Device Driver **400**. A separate detection routine **510** determines whether or not ADSL Modem Card **396** has been upgraded with an additional AFE (as described generally with reference to FIG. **6** below), or alternatively whether a processor used in a host system has changed.

The purpose of this step is primarily to determine whether entries in a Device Parameters Table **560** need to be updated because of changes in computing power, front end capabilities or other parameters that may necessitate a modification of the data throughput characterization of the overall system when used in a communications mode. A calibration routine **520** is then executed to determine the nominal setup parameters for the overall system in the manner described earlier. The results from this operation are stored in Device Paramater Table **560** where they then become accessible to various application programs that may make use of ADSL Modem Card **396** and Device Driver **400**. The information stored in table **560** can include any or all of the following: (a) measurements of the computing power available to the host processor; (b) measurements of the number of frames processable by the system within a particular time period; (c) estimations of the expected loading on the processing system based on demands of other applications programs and peripheral devices; (d) minimum and maximum data throughput estimations and/or targets; (e) data identifying the type of host processor; (1) data identifying the number and type of AFEs in ADSL Modem card **396**; (g) estimations and/or target system loading rates available for a datalink (i.e., maximum available processing time to be used by the system during data transmission); (h) data transmit and receive buffer sizes; (i) interrupt or similar priority data for the modem card; (j) estimations and/or target system subchannel utilization; (k) estimations and/or target system sub-channel bit capacity information; etc. It will be apparent to skilled artisans that the above are just examples of the types of information that may be pertinent to the performance of a high speed communications system, and that other parameters may be considered depending on the environment, application, etc. in which the present invention is used.

After performing Auto Calibration routine **520**, the results of the same are presented to the user for acceptance and verification at step **525**. At this point, the user can accept the predetermined configuration data at step **526** (i.e., such as proposed maximum and minimum throughput rates, loading rates, etc.) and this would otherwise invoke an end of modem setup routine **590**. Should the user not want to accept the recommended parameters, a Manual Configuration routine **530** is executed. At this juncture, various system performance data can be presented to the user for review, along with a list of modifiable system options **532**. If for example, the user elects to increase the desired throughput rate, a Verification routine **540** is then executed to determine whether such rate is reasonably sustainable within the other parameters of the system. If the new proposed configuration data is otherwise acceptable, then the Device Parameter Table **560** is updated, and the setup routine again ends. Otherwise, the user is alerted by a Notification/Suggestion routine **550**, which points out the failure of the proposed configuration, and, if possible, makes suggestions to the user

for modifying the system options **532** so that overall compliance can be achieved within the performance capability of the host processing system. The program then loops back to Acceptance routine **525**, and thereafter the process is repeated until an acceptable configuration has been achieved, and any changes have been incorporated into Device Parameter Table **560**.

While some of the operational steps above are described as implemented solely by Operating system **480** and Device Driver **400**, it is understood that such operations occur under direction of modem applications program **500**, or in some cases, based on initialization routines executed by the host processing system. Moreover, to simplify the presentation of the present invention, only some of the features that may be implemented are described above, and many other well-known operational steps normally associated with setting up or monitoring modems are omitted.

As with the design of the above Data Pump Device Driver **400**, the general design of the Control/Application Interface **500** required to accomplish the above functions is a routine task well within the abilities of one skilled in the art given the teachings herein. The specifics of such implementation are not critical or essential to the present inventions, and will vary from application to application according to system designer requirements, so they are not included here. Again, while this embodiment of the present invention is set Out in the context of a PC based host processor running Windows, it will be apparent to those skilled in the art that above description is merely an exemplary implementation. The referenced Control/Application Interface can be employed in numerous host processing/operating system environments, and in a variety of different coding organizations (high level or low level processing forms) well-known in the art.

Multiple AFE and Lower Sampling Speed Embodiment

FIG. **6** illustrates an example of the present invention wherein a user can achieve significantly increased data throughput using multiple low cost, low sampling speed AFEs, generally designated **680**A, **680**B, **680**C, etc. As described above, these AFEs may be in separate, modular form and configured in a bank form so that they can be incorporated conveniently on a printed circuit board (or similar mounting) or integrated in a single IC chip. Each AFE can be implemented in a fixed hardware configuration, or individually programmed/controlled to pass a certain portion of the downstream data transmission. Assuming suitable processing power is available for DMT modulation/demodulation (either through a dedicated or software implementation as described above in connection with FIGS. **3**A and **3**B) a user of such system can achieve substantially expanded functionality by upgrades having performance characteristics and costs of their choice.

Underlying Theory of Present Invention for ADSL/DMT Applications

A discussion of the underlying theory supporting the premise of the present invention now follows. In particular, this section shows the mathematical foundation for the use of multiple low speed AFE's to sample a full bandwidth ADSL/DMT signal. It will be apparent to those skilled in the art, after reading this discussion, that the present inventions can be advantageously used in a number of rate adaptable communications environments, including CAP implementations of ADSL.

DMT Transmitter

To simplify the present discussion, only a subset of the DMT transmitter is considered, as shown in FIGS. **1**D and **1**E. The combined model that includes the channel response and the DMT receiver is shown below, where only one branch of band-pass filtering and sampling is shown for simplicity. To further simplify, the channel response and the SFIR are combined together.

In this subsection, we analyze the signal over one band pass filtering process. The result shows that the DMT signals within the band pass can be recovered with the same use of impulse response shortening technique. With use of multiple AFE's that cover different frequency bands, all DMT sub-channels can be recovered.

In an ADSL environment as shown in FIG. **1**D, N (N=512) frequency domain variables are transformed into the time domain by IFFT block **60**

$$y_n = \sum_{i=0}^{N-1} x_n e^{j2\pi in/N}$$

Cyclic Prefix

c time domain variables at the end are added to the prefix of the sequence as shown in FIG. **1**D by block **70**

$$\{z_n\}=\{z_{-c}, z_{-c+1}, \ldots, z_{-1}, z_0, z_1, \ldots, z_{N-1}\}=\{y_{N-c}, \ldots, y_{NN-1}, y_0, y_{N-1}\}$$

AFE/DAC

Discrete time domain sequence are converted by AFE **75** to the continuous time domain waveform as follows:

$$z(t) = \sum_{n=-\infty}^{\infty} z_n p_{TX}(t - nT_c),$$

where p_{TX} (t) is the transmitter pulse of the AFE/DAC used, and T_c is the transmitter DAC clock period and equal to

$$T_c = \frac{250\,\mu\text{sec}}{N + c}$$

according to the DMT ADSL specifications.

Channel

With reference now to FIG. **1**E, if the channel impulse response is $h_c(t)$, we have

$$u(t) = \sum_{n=-\infty}^{\infty} z_n p_{RX}(t - nT_c) \quad \text{where} \quad p_{RX}(t) = p_{TX}(t) \otimes h_c(t).$$

Bandpass Filtering

If the bandpass filter **80** has an impulse response of hBPF(t),

$$v(t) = \sum_{n=-\infty}^{\infty} z_n p_{BPF}(t - nT_c)$$

where PBPF (t)=P_{RX}(t)\⊗h_{BPF}(t).

AFE/ADC

Let the sampling dock be $T_s=T_c\times L$. This means a slower sampling by a factor of L for AFE **81**. Thus,

$$w_k = \sum_{n=-\infty}^{\infty} z_n p_{BPF}(kT_s - nT_c) = \sum_{n=-\infty}^{\infty} z_n p_{BPF}([kL-n]T_c)$$

For causal pulse PBPF(t),we have

$$w_k = \sum_{n=-\infty}^{\infty} z_n p_{BPF}((kL-n)T_c) = \sum_{n=0}^{\infty} z_{kL-n} p_{BPF}(nT_c)$$

Shortening FIR (SFIR)

After AFE discrete time sampling, a time domain equalizer (TEQ) called SFIR **82** is used to reduce the combined discrete time impulse response to a duration smaller than c. If the SFIR response is $h_{SFIR}[n]$, we have

$$\begin{aligned} r_k &= \sum_{i=0}^{\infty} w_{k-i} h_{SFIR}[i] \\ &= \sum_{i=0}^{\infty} \left[\sum_{n=-\infty}^{\infty} z_n p_{BPF}([kL-n-iL]T_c) \right] h_{SFIR}[i] \\ &= \sum_{n=-\infty}^{\infty} z_n h_{tot}[kL-n] \\ &= \sum_{n=0}^{\infty} z_{kL-n} h_{tot}[n] \end{aligned}$$

where

$$h_{tot}[kL-n] = \sum_{i=0}^{\infty} h_{SFIR}[i] p_{BPF}([kL-n-iL]T_c)$$

Physical Meaning of $h_{tot}[n]$

If we perform discrete Fourier transform at block **84** for $h_{tot}[n]$, we obtain $H_{tot}[\omega]=H_{SFIR}[L\omega]H_{BPF}[\omega]$ where $H_{SFIR}[L\omega]$ and $H_{BPF}[\omega]$ are the DFT's with period $1/(LT_c)$ and $1/T_c$, respectively. Their spectra can be illustrated as shown in FIG. **1**F for L=5.

Dropping Cyclic Prefix

By dropping the cyclic prefix of length c/L, at block **83** we consider only $s_k=r_k$, k=0, . . . , N_1-1, where $N_1=N/L$.

FFT

Performing FFT at block **84** for s_k, k=0, . . . ,(N/L)−1,one obtains:

$$\begin{aligned} q_n &= \sum_{l=0}^{N_1-1} s_l e^{-j2\pi nl/N_1} \\ &= \sum_{k=0}^{N_1-1} r_k e^{-j2\pi nk/N_1} \\ &= \sum_{k=0}^{N_1-1} \left(\sum_{i=0}^{\infty} z_{kL-i} h_{tot}[i] \right) e^{-j2\pi nk/N_1} \\ &= \sum_{k=0}^{N_1-1} \sum_{i=0}^{\infty} z_{kL-i} h_{tot}[i] e^{-j2\pi n(kL-i)/N_1} e^{-j2\pi ni/N_1} \\ &= \sum_{i=0}^{\infty} \sum_{k=0}^{N_1-1} z_{kL-i} e^{-j2\pi n(kL-i)/N_1} h_{tot}[i] e^{-j2\pi ni/N_1} \\ &= \sum_{i=0}^{c} \sum_{k=0}^{N_1-1} z_{kL-i} e^{-j2\pi n(kL-i)/N_1} h_{tot}[i] e^{-j2\pi ni/N_1} \end{aligned}$$

-continued

$$= \sum_{i=0}^{c} \sum_{k=0}^{N_1-1} y_{kL-i} e^{-j2\pi n(kL-i)/N_1} h_{tot}[i] e^{-j2\pi ni/N_1}$$

where we assume $h_{tot}[i]$ is only nonzero for i=0, . . . , c. For a given i, let us define $l'=\lceil i/L \rceil$; We can then define $i'=l'L-i$, where i'=0, . . . , L−1. Therefore, $i=l'L-i'$From the above definitions, we have

$$\begin{aligned} \sum_{k=0}^{N_1-1} y_{kL-i} e^{-j2\pi n(kL-i)/N_1} &= \sum_{k=0}^{l'-1} y_{kL-i} e^{-j2\pi n(kL-i)/N_1} + \\ &\quad \sum_{k=l'}^{N_1-1} y_{kL-i} e^{-j2\pi n(kL-i)/N_1} \\ &= \sum_{k=0}^{l'-1} y_{(k-l')L+i'} e^{-j2\pi n([k-l']L+i')/N_1} + \\ &\quad \sum_{k=l'}^{N_1-1} y_{(k-l')L+i} e^{-j2\pi n([k-l']L+i')/N_1} \\ &= \sum_{k=0}^{l'-1} y_{(k-l'+N_1)L+i'} e^{-j2\pi n([k-l'+N_1]L+i')/N_1} + \\ &\quad \sum_{k=0}^{N_1-1-l'} y_{kL+i'} e^{-j2\pi n(kL+i')/N_1} \\ &= \sum_{k=N_1-l'}^{N_1-1} y_{kL+i'} e^{-j2\pi n(kL+i')/N_1} + \\ &\quad \sum_{k=0}^{N_1-1-l'} y_{kL+i'} e^{-j2\pi n(kL+i')/N_1} \\ &= \sum_{k=0}^{N_1-1} y_{kL+i'} e^{-j2\pi n(kL+i')/N_1} \end{aligned}$$

Therefore,

$$\begin{aligned} q_n &= \sum_{i=0}^{c} \sum_{k=0}^{N_1-1} y_{kL-i} e^{-j2\pi n(kL-i)/N_1} h_{tot}[i] e^{-j2\pi ni/N_1} \\ &= \sum_{i=0}^{c} \left[\sum_{k=0}^{N_1-1} y_{kL+i'} e^{-j2\pi n(kL+i')/N_1} \right] h_{tot}[i] e^{-j2\pi ni/N_1} \\ &= \sum_{i=0}^{c} \left[\sum_{k=0}^{N_1-1} \left(\sum_{l=0}^{N-1} x_l e^{j2\pi(kL+i')l/N} \right) e^{-j2\pi n(kL+i')/N_1} \right] \\ &\quad h_{tot}[i] e^{-j2\pi ni/N_1} \\ &= \sum_{i=0}^{c} \left[\sum_{k=0}^{N_1-1} \sum_{l=0}^{N-1} x_l e^{j2\pi(kL+i')(l-n)/N} \right] h_{tot}[i] e^{-j2\pi ni/N_1} \\ &= \sum_{i=0}^{c} \left[\sum_{l=0}^{N-1} x_l \sum_{k=0}^{N_1-1} e^{j2\pi(kL+i')(l-n)/N} \right] h_{tot}[i] e^{-j2\pi ni/N_1} \end{aligned}$$

Since

$$\sum_{k=0}^{N_1-1} e^{j2\pi(kL+i')(l-n)/N} = 0$$

when $(l-n)\neq mN_1$, we have

$$q_n = N_1 \sum_{i=0}^{c} \left[\sum_{m=0}^{L-1} x_{mN_1+n} e^{j2\pi i' m/L} \right] h_{tot}[i] e^{-j2\pi ni/N_1}$$

Knowing that $h_{tot}[i]$ is zero for $i<0$ and $i>c$ we have

$$\begin{aligned} q_n &= N_1 \sum_{i=0}^{c} \left[\sum_{m=0}^{L-1} x_{mN_1+n} e^{j2\pi i' m/L} \right] h_{tot}[i] e^{-j2\pi ni/N_1} \\ &= N_1 \sum_{i=-\infty}^{\infty} \left[\sum_{m=0}^{L-1} x_{mN_1+n} e^{j2\pi i' m/L} \right] h_{tot}[i] e^{-j2\pi ni/N_1} \\ &= N_1 \sum_{l=-\infty}^{\infty} \sum_{i'=0}^{L-1} \left[\sum_{m=0}^{L-1} x_{mN_1+n} e^{j2\pi i' m/L} \right] h_{tot}[lL-i'] e^{-j2\pi n(lL-i')/N} \\ &= N_1 \sum_{m=0}^{L-1} x_{mN_1+n} \sum_{i'=0}^{L-1} e^{j2\pi i' m/L} \sum_{l=-\infty}^{\infty} h_{tot}[lL-i'] e^{-j2\pi n(lL-i')/N} \end{aligned}$$

Since

$$\begin{aligned} \sum_{l=-\infty}^{\infty} h_{tot}[lL-i'] e^{-j2\pi n(lL-i')/N} &= \sum_{l=-\infty}^{\infty} h_{tot}[lL-i'] e^{-j\omega(lL-i')T_c} \Big|_{\omega=2\pi n/NT_c} \\ &= F\left\{ h_{tot}(t) \sum_l \delta(t-[lL-i']T_c) \right\} \Big|_{\omega=2\pi n/NT_c} \\ &= \frac{1}{2\pi} C_{tot}(\omega) \otimes \left[\frac{2\pi}{LT_c} \sum_l \delta\left(\omega - \frac{2\pi l}{LT_c}\right) e^{j2\pi li'/L} \right] \Big|_{\omega=2\pi n/NT_c} \\ &= \frac{1}{LT_c} \sum_l C_{tot}\left(\frac{2\pi n}{NT_c} - \frac{2\pi l}{LT_c}\right) e^{j2\pi li'/L} \end{aligned}$$

we have

$$\begin{aligned} q_n &= N_1 \sum_{m=0}^{L-1} x_{mN_1+n} \sum_{i'=0}^{L-1} e^{j2\pi i' m/L} \sum_{l=-\infty}^{\infty} h_{tot}[lL-i'] e^{-j2\pi n(lL-i')/N} \\ &= N_1 \sum_{m=0}^{L-1} x_{mN_1+n} \sum_{i'=0}^{L-1} e^{j2\pi i' m/L} \frac{1}{LT_c} \sum_l H_{tot}\left(\frac{2\pi n}{NT_c} - \frac{2\pi l}{LT_c}\right) e^{j2\pi li'/L} \\ &= \frac{N_1}{LT_c} \sum_{m=0}^{L-1} x_{mN_1+n} \sum_l H_{tot}\left(\frac{2\pi n}{NT_c} - \frac{2\pi l}{LT_c}\right) \sum_{i'=0}^{L-1} e^{j2\pi(l+m)i'/L} \\ &= \frac{N_1}{T_c} \sum_{m=0}^{L-1} x_{mN_1+n} H_{tot}\left(\frac{2\pi n}{NT_c} + \frac{2\pi m}{LT_c}\right) \\ &= \frac{N_1}{T_c} \sum_{m=0}^{L-1} x_{mN_1+n} H_{tot}\left(\frac{2\pi}{NT_c}[mN_1+n]\right), n = 0, \ldots, N_1-1 \\ &= N_1 \sum_{m=0}^{L-1} x_{mN_1+n} H_{tot}[mN_1+n], n = 0, \ldots, N_1-1 \end{aligned}$$

where

$$H_{tot}[n] = \frac{1}{T_c} H_{tot}\left(\frac{2\pi}{NT_c} n\right), \quad \text{for } 0 \le n < N$$

Relationship between q_n and x_n

As shown in FIG. **1G** if $\overline{H}_{tot}[n]$ is a bandpass filter and nonzero only in the intervals $[k(N/2L), (k+1)(N/2L)]$ and $[(2L-k-1)(N/2L), (2L-k)(N/2L)]$, where $0 \leqq k \leqq L$, the possible values of m that $H_{tot}[m(N/L)+n]$ is nonzero for $0 \leqq n \leqq (N/L)$ are as follows.

Even k

If k is even, we can have $m=k/2$ and $0 \leqq n < (N/2L)$ so that $H_{tot}[m(N/L)+n]$ is nonzero over the interval $[k(N/2L), (k+1)(N/2L)]$, and $m=(L-1)-k/2$ and $(N/2L) \leqq n < (N/L)$ so that $H_{tot}[m(N/L)+n]$ is nonzero over the interval $[(2L-k-1)(N/2L), (2L-k)(N/2L)]$.

Odd k

If k is odd, we can have $m=(k-1)/2$ and $(N/2L) \leqq n \leqq (N/L)$ so that $H_{tot}m(N/L)+n]$ is nonzero over the interval $[k(N/2L), (k+1)(N/2L)]$, and $m=L-(k-1)/2$ and $0 \leqq n < (N/2L)$so that $H_{tot}[m(N/L)+n]$ is nonzero over the interval $[(2L-k-1)(N/2L), (2L-k)(N/2L)]$. The above discussion is illustrated in FIG. **1G** for L=3.

In another variation that can be used in the present invention, similar advantages to those obtained by limiting bandwidth in the received signal in the downstream transceiver can be obtained by also optionally limiting the upstream data rate of the transceiver as well. In other words, the ADSL standard provides for 31 channels in the upstream direction, but many applications do not require this amount of bandwidth. The constraints, requirements and costs associated with the DMT modulation signal processing, and DAC **330** also can be significantly reduced by transmitting only a sub-set of the available 31 sub-channels. The determination of the appropriate sub-channels would be accomplished in essentially the same manner as set forth above, except that the information on upstream sub-channel SNR usually must be determined by the upstream transceiver, and then fed back to the downstream transceiver. To save time and overhead complexity, and given the fact that there is less variation in bit capacity in sub-channels in this frequency band, one approach also would be to simply select a fixed sub-set of such sub-channels without regard to their actual performance characteristics. In a software modem environment, Control/Application software 500 would provide a user with selectable control to effectuate a restricted upstream transmission on limited sub-channels. Again, with respect to the ADSL standard, the only requirement in this

respect is that the upstream pilot tone must also be transmitted to establish a valid data link. An optional limited "upstream" transmission can be effectuated in a variety of ways by the circuitry already described above in connection with FIGS. **2** and **3**. The exact details of such implementation will be apparent to those of skill in the art given the present teachings.

Although the present invention has been described in terms of a preferred ADSL embodiment, it will be apparent to those skilled in the art that many alterations and modifications may be made to such embodiments without departing from the teachings of the present invention. For example, it is apparent that the present invention would be beneficial used in any xDSL or high speed multi-carrier application environment. Other types of VLSI and ULSI components beyond those illustrated in the foregoing detailed description can be used suitably with the present invention. Accordingly, it is intended that the all such alterations and modifications be included within the scope and spirit of the invention as defined by the following claims.

What is claimed is:

1. A high speed communications system capable of supporting a downstream data transmission from an upstream transceiver using an analog signal consisting of M data carrying signals contained within a bandwidth F, said system comprising:

a channel interface circuit for coupling to and receiving said analog signal; and

a front end receiving circuit for processing the analog signal and converting it to a digital signal;

a processing circuit for performing signal processing operations on N of said M data carrying signals (N<M) from the digital signal using a first frequency portion f1 of the digital signal (f1<F) and for extracting selected data from said N data carrying signals; and

wherein said selected data can be varied by varying resources available to said processing circuit, and said processing circuit does not process data carrying signals from the downstream data transmission outside of said first frequency portion f1.

2. The system of claim **1**, wherein the N data carrying signals are selected by the processing circuit so as to reduce the amount of processing required to extract the selected data from the digital signal as compared to an amount of processing required to extract the selected data if it were carried by a different set of N data carrying signals.

3. The system of claim **2**, wherein the N data carrying signals can be selected during an initialization process setting up a data link to the upstream transceiver.

4. The system of claim **3**, wherein M data carrying signals can be sent by the upstream transmitter during an initialization process, and thereafter, only N data carrying signals are sent.

5. The system of claim **1**, wherein the front end circuit includes: (i) a sub-band filter for passing the first frequency bandwidth portion f_1 of said bandwidth F; (ii) and an analog to digital converter.

6. The system of claim **1**, wherein the selected data can be augmented to further include data obtained from an additional second frequency bandwidth portion f2 of said bandwidth F, when resources available to said processing circuit are also augmented so that an additional number of data carrying signals P from the M data carrying signals (N+P<M) can be processed.

7. The system of claim **6**, further including one or more sub-band filters for passing the first frequency bandwidth portion f1 and second frequency bandwidth portion f2 of said bandwidth F and an analog to digital converter.

8. The system of claim **7**, wherein a target data rate of the system can be increased by processing an additional number of data carrying signals P from the M data carrying signals, where N+P<M.

9. The system of claim **1**, wherein the selected data to be extracted from the digital signal can be controlled by a user of such system.

10. The system of claim **9**, wherein a user of such system can increase a target data rate of the system by modularly augmenting the front end circuit to include additional bandwidth and analog to digital conversion capacity such that an additional number of data carrying signals P from the M data carrying signals (N+P<M) can be processed.

11. The system of claim **1**, further including a front end transmitting circuit for transmitting control information to cause said upstream transceiver to transmit downstream data only using the N data carrying signals.

12. The system of claim **11**, wherein the control information transmitted to the upstream transceiver includes feedback information indicating that only N of the M data carrying signals are desirable for downstream data transmission, even during times when said channel is capable of supporting more than N data carrying signals.

13. The system of claim **1**, further including a front end transmitting circuit for transmitting an upstream data signal using a second frequency bandwidth F2 different from F, and L data carrying signals, and where L<M.

14. A high speed communications system capable of supporting a downstream data transmission from an upstream transceiver using an analog signal consisting of M data carrying signals contained within a bandwidth F, said system comprising:

a channel interface circuit for coupling to and receiving said analog signal; and

a front end receiving circuit for processing the analog signal and converting it to a digital signal;

a processing circuit for extracting N data carrying signals (N<M) from the digital signal using a first frequency portion f1 of the digital signal (f1<F); and

a front end transmitting circuit for transmitting control information to cause said upstream transceiver to transmit downstream data only using the N data carrying signals; and

wherein the control information transmitted to the upstream transceiver includes feedback information indicating that only N of the M data carrying signals are desirable for downstream data transmission, even during times when said channel is capable of supporting more than N data carrying signals and

further wherein the control information transmitted to the upstream transceiver further includes feedback information indicating that: (i) the system can support any data protocols used by said upstream transceiver; and (ii) that they are connected through a channel with substantial signal attenuation characteristics for data signals other than the N data carrying signals.

15. A scalable high speed communications system capable of supporting an upstream transceiver which can transmit M modulated sub-channels using an analog signal through a channel to said system, said system comprising:

a channel interface circuit for coupling to and receiving said analog signal from the channel;

an analog front end circuit for processing the analog signal and converting it to a digital signal, the front end

circuit including a sub-band filter and an analog to digital converter:

a processing circuit for extracting data from the digital signal, the digital signal including data from a first number N of said sub-channels, where N<M/k where k is a scaling factor, and said processing circuit can accommodate any integer value for k>=1, and;

wherein said N sub-channels can be varied based on resources available to said processing circuit, and said processing circuit extracts data only from said N sub-channels, regardless of whether additional ones of said M sub-channels can be used for transmitting data between the system and said upstream transceiver; and

further wherein the N sub-channels are selected so as to reduce the amount of processing required to extract the selected data from the digital signal, as compared to an amount of processing required to extract the selected data if it were carried by a different set of N sub-channels.

16. The system of claim **15**, wherein the front end circuit includes: (i) a sub-band filter for passing only the N sub-channels; (ii) and an analog to digital converter.

17. The system of claim **15**, wherein the selected data further includes data obtained from an additional second number of sub-channels P, so that an additional number of sub-channels (N+P<M) can be processed.

18. The system of claim **17**, further including one or more sub-band filters for passing the first number N and second number P of said sub-channels and an analog to digital converter.

19. The system of claim **18**, wherein a target data rate of the system can be increased by processing an additional number of sub-channels P from the M sub-channels, and where N+P<M.

20. The system of claim **15**, wherein the selected data to be extracted is taken from bandpassed data passed through said sub-band filter, and which selected data can be controlled by a user of such system.

21. The system of claim **15**, wherein the upstream transceiver uses discrete multi-tone (DMI) modulation for generating the M modulated sub-channels, and the channel supports asymmetric digital subscriber loop (ADSL) transmission standards.

22. The system of claim **15**, further including a front end transmitting circuit for transmitting an upstream data signal using a second set of sub-channels L separate from M, where L<M.

23. A scalable high speed communications system capable of supporting an upstream transceiver which can transmit M modulated sub-channels using an analog signal through a channel to said system, said system comprising:

a channel interface circuit for coupling to and receiving said analog signal from the channel;

an analog front end circuit for processing the analog signal and converting it to a digital signal, the front end circuit including a sub-band filter and an analog to digital converter;

a processing circuit for extracting data from the digital signal the digital signal including data from a first number N of said sub-channels, where N≦M/k, where k is a scaling factor, and said processing circuit can accommodate any integer value for k>=1, and;

wherein said N sub-channels can be varied based on resources available to said processing circuit, and said processing circuit extracts data only from said N sub-channels, regardless of whether additional ones of said M sub-channels can be used for transmitting data between the system and said upstream transceiver; and

further wherein the N sub-channels are selected so as to reduce the amount of processing required to extract the selected data from the digital signal, as compared to an amount of processing required to extract the selected data if it were carried by a different set of N sub-channels;

further wherein the N sub-channels can be selected by an initialization process to set up a data link to the upstream transceiver.

24. A scalable high speed communications system capable of supporting an upstream transceiver which can transmit M modulated sub-channels using an analog signal through a channel to said system, said system comprising:

a channel interface circuit for coupling to and receiving said analog signal from the channel:

an analog front end circuit for processing the analog signal and converting it to a digital signal, the front end circuit including a sub-band filter and an analog to digital converter;

a processing circuit for extracting data from the digital signal, the digital signal including data from a first number N of said sub-channels, where N≦M/k, where k is a scaling factor, and said processing circuit can accommodate any integer value for k>=1, and;

wherein said N sub-channels can be varied based on resources available to said processing circuit, and said processing circuit extracts data only from said N sub-channels, regardless of whether additional ones of said M sub-channels can be used for transmitting data between the system and said upstream transceiver; and

further wherein the N sub-channels are selectable by an initialization process to set up a data link with the remote transceiver, and are selected so as to reduce the amount of processing required to extract the selected data from the digital signal, as compared to an amount of processing required to extract the selected data if it were carried by a different set of N sub-channels;

further wherein the M sub-channels can be received from the upstream transmitter during said initialization process, and thereafter, only N sub-channels are received.

25. A scalable high speed communications system capable of supporting an upstream transceiver which can transmit M modulated sub-channels using an analog signal through a channel to said system, said system comprising:

a channel interface circuit for coupling to and receiving said analog signal from the channel;

an analog front end circuit for processing the analog signal and converting it to a digital signal, the front end circuit including a sub-band filter adapted to bandpass said analog signal under control of a user of such system, and an analog to digital converter;

a processing circuit for extracting data from the digital signal, the digital signal including data from a first number N of said sub-channels bandpassed by said sub-band filter under control of said user, where N<M/k, and where k is a scaling factor and said processing circuit can accommodate any integer value for k>=1 and;

wherein said N sub-channels can be varied based on resources available to said processing circuit, and said processing circuit extracts data only from said N sub-channels, regardless of whether additional ones of said

M sub-channels can be used for transmitting data between the system and said upstream transceiver; and

further wherein said user of such system can increase a target data rate of the system by modularly augmenting the front end circuit to include additional bandwidth and analog to digital conversion capacity such that an additional second number of sub-channels P from the M sub-channels (N+P<M) can be processed.

26. A scalable high speed communications system capable of supporting an upstream transceiver which can transmit M modulated sub-channels using an analog signal through a channel to said system, said system comprising:

a channel interface circuit for coupling to and receiving said analog signal from the channel,

an analog front end circuit for processing the analog signal and converting it to a digital signal, the front end circuit including a sub-band filter adapted to bandpass said analog signal under control of a user of such system, and an analog to digital converter;

a processing circuit for extracting data from the digital signal, the digital signal including data from a first number N of said sub-channels bandpassed by said sub-band filter under control of said user, where $N \leqq M/k$, and where k is a scaling factor, and said processing circuit can accommodate any integer value for k >=1, and;

wherein said N sub-channels can be varied based on resources available to said processing circuit, and said processing circuit extracts data only from said N sub-channels regardless of whether additional ones of said M sub-channels can be used for transmitting data between the system and said upstream transceiver; and

further wherein said user of such system can increase a target data rate of the system by modularly augmenting the front end circuit to include additional bandwidth and analog to digital conversion capacity such that an additional second number of sub-channels P from the M sub-channels (N+P<M) can be processed; and

a front end transmitting circuit for transmitting control information to cause said upstream transceiver to transmit downstream data only using the N sub-channels.

27. A scalable high speed communications system capable of supporting an upstream transceiver which can transmit M modulated sub-channels using an analog signal through a channel to said system, said system comprising:

a channel interface circuit for coupling to and receiving said analog signal from the channel;

an analog front end circuit for processing the analog signal and converting it to a digital signal, the front end circuit including a sub-band filter adapted to bandpass said analog signal under control of a user of such system, and an analog to digital converter;

a processing circuit for extracting data from the digital signal the digital signal including data from a first number N of said sub-channels bandpassed by said sub-band filter under control of said user, where $N \leqq M/k$ and where k is a scaling factor, and said processing circuit can accommodate any integer value for k>=1, and,

a front end transmitting circuit for transmitting control information to cause said upstream transceiver to transmit downstream data only using the N sub-channels; and

wherein said N sub-channels can be varied based on resources available to said processing circuit, and said processing circuit extracts data only from said N sub-channels, regardless of whether additional ones of said M sub-channels can be used for transmitting data between the system and said upstream transceiver; and

further wherein said user of such system can increase a target data rate of the system by modularly augmenting the front end circuit to include additional bandwidth and analog to digital conversion capacity such that an additional second number of sub-channels P from the M sub-channels (N+P<M) can be processed; and

further wherein said control information transmitted to the upstream transceiver includes feedback information indicating that only N of the M sub-channels are usable for downstream data transmission, even during times when said channel is capable of supporting more than N sub-channels.

28. A high speed communications system capable of supporting an upstream transceiver which can transmit M modulated sub-channels using an analog signal through a channel to said system, said system comprising

a channel interface circuit for coupling to and receiving said analog signal from the channel;

an analog front end circuit for processing the analog signal and converting it to a digital signal, the front end circuit including a sub-band filter and an analog to digital converter;

a processing circuit for extracting data from the digital signal, the digital signal including data from a first number N of said subchannels, where N<M;

a front end transmitting circuit for transmitting control information to cause said upstream transceiver to transmit downstream data only using the N sub-channels; and wherein the control information transmitted to the upstream transceiver includes feedback information indicating that only N of the M sub-channels are usable for downstream data transmission, even during times when said channel is capable of supporting more than N sub-channels; and

further wherein the control information transmitted to the upstream transceiver further includes feedback information indicating that: (i) the system can support any data protocols used by said upstream transceiver; and (ii) that the system and upstream transceiver are connected through a channel with substantial signal attenuation characteristics for sub-channels other than the N sub-channels.

29. A high speed communications system for processing an analog data signal from a channel capable of supporting a downstream data transmission using a bandwidth F from a remote transciever also capable of using a bandwidth F, said system comprising:

a channel interface circuit for coupling to and receiving said analog data signal from the channel, and

a front end receiving circuit for processing the analog data signal and converting it to a digital signal;

a processing circuit for extracting selected data from the digital signal, the digital signal including data from a first frequency bandwidth portion f1 of said bandwidth and for generating feedback information indicating to the remote transceiver that the bandwidth other than f1 is unsuitable for data transmission even when said channel can support said bandwidth F;

wherein the feedback information contains intentionally altered channel characteristic information.

30. A high speed communications system for processing an analog data signal from a channel capable of supporting

a downstream data transmission using a bandwidth F from a remote transciever also capable of using a bandwidth F, said system comprising:

a channel interface circuit for coupling to and receiving said analog data signal from the channel; and

a front end receiving circuit for processing the analog data signal and converting it to a digital signal;

a processing circuit for extracting selected data from the digital signal, the digital signal including data from a first frequency bandwidth portion f1 of said bandwidth and for generating feedback information indicating to the remote transceiver that the bandwidth other than f1 is unsuitable for data transmission even when said channel can support said bandwidth F, said feedback information containing intentionally altered channel characteristic information;

wherein the feedback information, including the size and center of first frequency bandwidth portion f1, can be controlled by a user of such system.

31. A high speed communications system for processing an analog data signal from a channel capable of supporting a downstream data transmission using a bandwidth F from a remote transciever also capable of using a bandwidth F, said system comprising:

a channel interface circuit for coupling to and receiving said analog data signal from the channel; and

a front end receiving circuit for processing the analog data signal and converting it to a digital signal;

a processing circuit for extracting selected data from the digital signal, the digital signal including data from a first frequency bandwidth portion f1 of said bandwidth and for generating feedback information indicating to the remote transceiver that the bandwidth other than f1 is unsuitable for data transmission even when said channel can support said bandwidth F, said feedback information containing intentionally altered channel characteristic information;

wherein the feedback information, including the size and center of first frequency bandwidth portion f1, can be controlled by a user of such system; and

further wherein the ratio of f1 to F is approximately 0.5 or less, and this ratio can be increased through modular additions to the front end receiving circuit.

32. A high speed communications system for transmitting digital information in a channel capable of supporting a transmission bandwidth F, said system comprising:

an upstream data transceiver capable of modulating the digital information to generate an analog data signal data transmission using said transmission bandwidth F; and

a downstream data transceiver channel interface circuit for coupling to and receiving said analog data signal from the upstream data transciever through said channel, the downstream data transceiver including

(i) a front end receiving circuit for processing the analog data signal and converting it to a digital signal; and

(ii) a processing circuit for demodulating the digital signal, the digital signal including data from a first frequency bandwidth portion f1 of said bandwidth and for generating feedback information indicating to the upstream transceiver that the bandwidth other than f1 is unsuitable for data transmission; and

(iii) a front end transmitting circuit for transmitting the feedback information using a second frequency bandwidth portion f2 to cause said upstream transceiver to transmit downstream data only using the first frequency portion fl;

wherein the feedback information contains intentionally altered channel characteristic information.

33. The system of claim **32**, wherein the ratio of f1 to F is approximately 0.5 and this ratio can be increased through modular additions and/or changes to thefront end receiving circuit.

34. The system of claim **33**, wherein the feedback information, including the size and location of first frequency portion f1, can be controlled by a user of such system.

35. A method of operating a high speed communications system that is coupled to a remote transceiver through a channel capable of supporting an analog data transmission having a bandwidth F, said method comprising:

(a) receiving said analog data signal from the remote transceiver through the channel;

and

(b) generating a digital signal based on sampling a portion of the analog data transmission signal corresponding to a first frequency bandwidth portion fl; and

(c) processing the digital signal to extract data from the digital signal; and

(d) generating feedback information indicating to the remote transceiver that the bandwidth other than f1 should not be used for data transmission, even if an analog data signal with bandwidth>f1 is supportable in the channel and by the remote transceiver; and

(e) determining an optimal size and location of first frequency bandpass portion f1 so as to minimize the amount of processing required to extract the data from the digital signal, as compared to some other size and location for said first frequency bandpass portion f1.

36. The method of claim **35**, further including a step prior to step (a): receiving a control signal from a user of such system for determining size and location of first frequency bandwidth portion f1.

37. The method of claim **35**, wherein the system transmits feedback information containing intentionally altered channel characteristic information.

38. A method of operating a high speed communications system that is coupled to a remote transceiver through a channel capable of supporting an analog data transmission having a bandwidth F, said method comprising:

(a) receiving said analog data signal from the remote transceiver through the channel;

and

(b) generating a digital signal based on sampling a portion of the analog data transmission signal corresponding to a first frequency bandwidth portion f1; and

(c) processing the digital signal to extract data from the digital signal; and

generating feedback information indicating to the remote transceiver that the bandwidth other than f1 should not be used for data transmission, even if an analog data signal with bandwidth >f1 is supportable in the channel and by the remote transceiver; and

wherein step (a) occurs during an initialization period, and said received analog transmission signal is generated by the remote transceiver to have a bandwidth >f1; and

after said initialization period the remote transceiver only transmits an analog data signal within first frequency bandwidth portion f1.

39. A method of operating a high speed communications system that is coupled to a remote transceiver through a

channel capable of supporting an analog data transmission signal including M modulated sub-channels, said method comprising:

(a) receiving said analog data transmission signal from the remote transceiver through the channel; and

(b) generating a digital signal based on sampling a portion of the analog data transmission signal corresponding to a first frequency bandwidth portion f1; and

(c) processing the digital signal to extract data from N of the sub-channels, where N<M; and

(d) generating feedback information indicating to the remote transceiver that the sub-channels other than the N sub-channels should not be used for data transmission, even if said channel and/or the remote transceiver is capable of supporting more than N sub-channels; and

(e) determining an optimal set of N sub-channels so as to minimize the amount of processing required to extract the data from the digital signal.

40. The method of claim **39**, further including a step prior to step (a): receiving a control signal from a user of such system for determining the identity of the N sub-channels.

41. A method of operating a high speed communications system that is coupled to a remote transceiver through a channel capable of supporting an analog data transmission signal including M modulated sub-channels, said method comprising:

(a) receiving said analog data transmission signal from the remote transceiver through the channel; and

(b) generating a digital signal based on sampling a portion of the analog data transmission signal corresponding to a first frequency bandwidth portion f1; and

(c) processing the digital signal to extract data from N of the sub-channels, where N<M; and

(d) generating feedback information indicating to the remote transceiver that the sub-channels other than the N sub-channels should not be used for data transmission, even if said channel and/or the remote transceiver is capable of supporting more than N sub-channels; and

wherein:

step (a) occurs during an initialization period, and said received analog transmission signal can be generated by said remote transceiver to include data for M sub-channels; and

after step (d) the remote transceiver only transmits an analog data signal using the N sub-channels.

42. A method of operating a high speed communications system that is coupled to a remote transceiver through a channel capable of supporting an analog data transmission signal including M modulated sub-channels, said method comprising:

(a) receiving said analog data transmission signal from the remote transceiver through the channel, and

(b) generating a digital signal based on sampling a portion of the analog data transmission signal corresponding to a first frequency bandwidth portion f1; and

(c) processing the digital signal to extract data from N of the sub-channels where N<M: and

(d) generating feedback information indicating to the remote transceiver that the sub-channels other than the N sub-channels should not be used for data transmission even if said channel and/or the remote transceiver is capable of supporting more than N sub-channels; and

wherein the system transmits feedback information containing intentionally altered channel characteristic information.

43. A method of operating a high speed communications system that is coupled through a channel to a remote transceiver operating at a maximum data rate Y using a bandwidth F, said method comprising:

(a) receiving an analog initialization signal from the remote transceiver through the channel; and

(b) generating a digital signal based on sampling a portion of the analog data transmission signal corresponding to a first frequency bandwidth portion fl, where f1<F; and

(c) processing the digital signal to extract data from the digital signal such that an effective receiving rate X (where X<Y) is achieved by the system;

(d) generating feedback information pertaining to the channel transmission characteristics indicating to the remote transceiver that data rates higher than X should not be used;

(e) thereafter receiving an analog data signal transmitted by the remote transceiver to have a bandwidth fl;

(f) repeating steps (b) and (c);

(g) determining an optimal location and size of bandwidth portion f1 so as to minimize the amount of processing required to extract the data from the digital signal at the receiving rate X, as compared to an amount of processing required to extract the data from the digital signal at the receiving rate X from a different bandwidth portion f1.

44. The method of claim **43**, further including a step prior to step (a): receiving a control signal from a user of such system for determining the effective receiving rate X.

45. A high speed communications data receiver for communicating through a channel with a remote transmitter that is capable of transmitting a data signal with a particular frame rate T and data rate Y, the receiver comprising:

a channel interface circuit for coupling to and receiving said data signal; and

an analog front end circuit for sampling the data signal and converting it to a digital signal; and

a processing circuit that: (i) is configurable for processing the digital signal at a data rate<=X and using said frame rate T, where X is determined for such processing circuit prior to initialization of a data transmission and X<Y/2; (ii) generates a transmission control signal for causing said remote transmitter to transmit at a data rate no greater than X during a data transmission; (iii) is configurable to support said data transmission at least in part with assistance from resources from a host processing device;

wherein signal processing requirements for the processing circuit are reduced from that otherwise required to support data rate Y because processing resources sufficient to support a fractional rate of the available data rate Y are used to support said data rate X; and

further wherein X is determined by evaluating signal processing capabilities available to said processing circuit prior to said data transmission, including resources of said host processing device.

46. The system of claim **45**, further including a front end transmitting circuit for transmitting the transmission control signal from the processing circuit to cause said remote transceiver to transmit downstream data only at said data rate X.

47. The system of claim **45**, wherein the control information transmitted to the remote transceiver includes feedback information indicating that the maximum downstream data transmission data rate is X, even during times when said channel is capable of supporting more than said data rate X.

48. The system of claim **45**, wherein the feedback information including the data rate X can be controlled by a user of such system.

49. The system of claim **45**, wherein the ratio of X to Y is approximately 0.2 or less.

50. A high speed communications data receiver for communicating through a channel at a controllable data rate X with a remote transceiver capable of transmitting a data signal at a frame rate T, and a data rate Y, where X/Y<½, the receiver comprising:

a channel interface circuit for coupling to and receiving an analog data signal from the remote transceiver; and

an analog front end circuit for data sampling the analog signal and converting it to a digital signal; and

a processing circuit for determining said rate X based on processing capabilities available for extracting data from the digital signal, and for generating a transmission control signal for causing said remote transceiver to transmit using said frame rate T, and a data rate substantially equal to said data rate X during a data transmission, and said processing circuit being implemented at least in part by signal processing software executed by a host processing device coupled to the data receiver.

51. The receiver of claim **50**, wherein said rate X is determined during a calibration routine.

52. The receiver of claim **51**, wherein said calibration routine is executed by said processing device to determine the capabilities of such processing circuit.

53. The receiver of claim **50**, wherein said rate X is configurable by a user of such receiver based on controlling resources to be made available to said host processing device.

54. The receiver of claim **50**, wherein X/Y is approximately 0.2 or less.

55. A method for communicating through a channel with a remote transceiver that is capable of transmitting a data signal at a frame rate T, and a data rate Y, the method comprising the steps of:

receiving said data signal at a local transceiver; and

sampling the data signal and converting it to a digital signal at said local transceiver; and

processing the digital signal at a data rate<=X and using said frame rate T at said local transceiver, where X is determined for said local transceiver prior to initialization of a data transmission and X<Y/2; and

generating a transmission control signal for causing said remote transceiver to transmit at a data rate no greater than X during a data transmission; and

transmitting data in the channel at a data rate that is intentionally reduced from that supportable by said remote transceiver and by the channel, so that said local transceiver can: (1) support such data transmission with data signal sampling resources and digital signal processing resources that are reduced from that required to support data rate Y; (2) adjust said data rate in response to changes in said data signal sampling resources and digital signal processing resources.

56. The method of claim **55**, wherein said transmission control signal, including the data rate X can be controlled by a user of such system.

57. The method of claim **55**, wherein the ratio of X to Y is approximately 0.2 or less.

58. A method for communicating through a channel at a controllable data rate X with an upstream transmitter capable of transmitting a data signal at a frame rate T, and a data rate Y, where X/Y <½, the method comprising the steps of:

receiving said data signal; and

sampling the data signal and converting it to a digital signal; and

determining said rate X based on processing capabilities available f or extracting data from the digital signal; and

generating a transmission control signal for causing said upstream transmitter to transmit at said frame rate T and a data rate substantially equal to said data rate X during a data transmission

transmitting data in the channel at a data rate that is intentionally reduced from that supportable by the channel, such that said said data transmission can be supported with data signal sampling resources and digital signal processing resources that are reduced from that required to support data rate Y, and said data rate is adjustable in response to changes in said data signal sampling resources and digital signal processing resources.

59. The method of claim **58**, wherein said rate X is determined during a calibration routine.

60. The method of claim **59**, wherein said calibration routine is executed by a host data processor to determine the capabilities of such processor.

61. The method of claim **58**, wherein said rate X is configurable by a user of such receiver based on performance characteristics of a host processor comprising a portion of the processing circuit.

62. The method of claim **58**, wherein X/Y is approximately 0.2 or less.

63. A method for communicating through a channel between a local and a remote transceiver, which remote transceiver supports up to a first maximum number M modulated sub-channels, the method comprising the steps of:

(a) determining a second maximum number N of modulated sub-channels supportable by signal processing resources at the local transceiver; and

(b) transmitting data transmission control signals for causing the remote transceiver to transmit using at most said N modulated sub-channels, where N<=M;

(c) transmitting data between the local and remote transceiver during a data transmission using at most said N modulated sub-channels; and

(d) dynamically adjusting a number of, or a data loading for, said N modulated sub-channels in response to changes in said signal processing resources.

64. The method of claim **63**, wherein said signal processing resources are based on a software signal processing routine executed by a microprocessor coupled to the local transceiver.

65. The method of claim **63**, wherein said data transmission control signals include T1.413 initialization protocol signals.

66. The method of claim **63**, wherein the local and remote transceivers can be configured to support either a full data rate transmission in the channel using said first maximum number M modulated sub-channels, or a reduced data rate transmission using said second maximum number N modulated sub-channels.

67. The method of claim **63**, further including a step (d): adjusting said second maximum number N of modulated sub-channels in response to changes in said signal processing resources.

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