

Claim Chart For Infringement of U.S. Patent No. 7,865,177 by NXP Chips

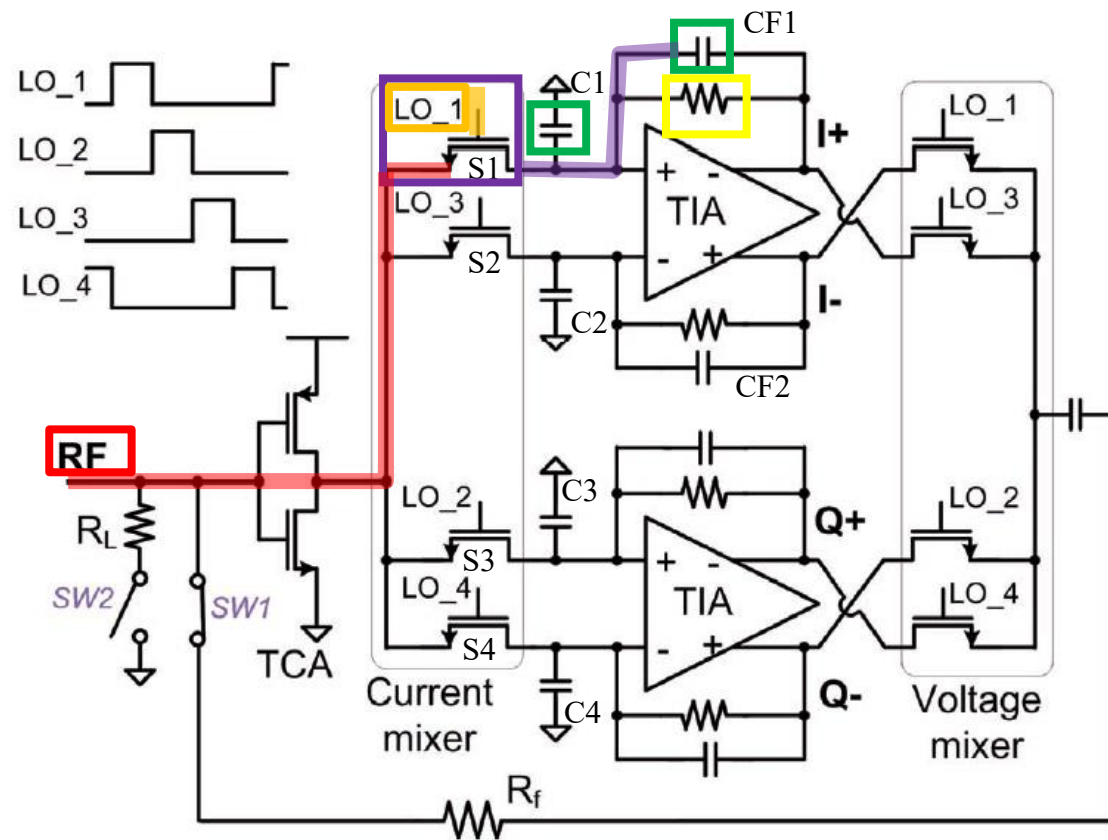
Claim 14	NXP Wireless Chips
A method for down-converting an electromagnetic signal, comprising:	NXP directly infringes (literally and/or under the doctrine of equivalents) the '177 patent by making, using, selling, offering for sale, and/or importing in/into the United States products covered by at least claim 14 of the '177 patent. NXP products that infringe claim 14 of the '177 patent include NXP wireless chips (e.g., Wi-Fi and/or Bluetooth chips) including, without limitation, NXP part nos. TEF510x series, IW620 series, IW416 series, 88W9098 series, 88W9097 series, 88W9068 series, 88W9064 series, 88W8997 series, 88W8987 series, 88W8977 series, 88W8897 series, 88W8887 series, 88W8801 series, 88W8787 series, 88W8786 series, 88W8766 series, 88W8764 series, 88W8688 series, 88Q9098 series, 88MW3xx series, and any other NXP chip (collectively, “NXP Chips”) that is capable of down-converting an electromagnetic signal as claimed in the '177 patent. On information and belief, each NXP Chip includes at least one or more switches/transistors that sample a carrier signal, one or more capacitors that store non-negligible amounts of energy from a carrier signal, and one or more resistors providing a low impedance load(s). On information and belief, the structure, function, and operation of NXP Chips are substantially similar to one another with respect to the claims at issue. On information and belief, the NXP Chips are described, in part, in the IEEE paper entitled, “A Compact SAW-less Multiband WCDMA/GPS Receiver Front-End with Translational Loop for Input Matching” by X. He and H. Kundur, 2011 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 2011, pp. 372-374 (hereinafter referred to as 2011 IEEE paper). On information and belief, each NXP Chip performs a method for down-converting an electromagnetic signal (e.g., high frequency RF signal) to a lower frequency signal (e.g., baseband signal). The method is performed on the receiver side of each NXP chip. For example, NXP’s 88W8977 “is a highly integrated single-chip solution that incorporates both Wi-Fi (2.4/5 GHz) and Bluetooth technology. The IEEE 802.11n compliant dual-band system-on-chip offers Wi-Fi data rates up to MCS 7 (150 Mbit/s). The SoC is specifically designed to support the speed, reliability, and quality requirements of devices such as wearables, Internet of Things (IoT) and smart home applications. The Combo solution provides both

	simultaneous and independent operation of the IEEE 802.11n compliant 1x1 spatial stream and Bluetooth 5.2 with high speeds and mesh networking for increased Internet of Things (IoT) functionality.”¹ Accordingly, each NXP Chip is configured to receive an electromagnetic signal (e.g., high frequency RF signal). In order to process such a signal, each NXP Chip must necessarily down-convert the electromagnetic signal to a baseband signal.
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¹ <https://www.nxp.com/products/wireless-connectivity/wi-fi-plus-bluetooth-plus-802-15-4/2-4-5-ghz-dual-band-1x1-wi-fi-4-802-11n-plus-bluetooth-5-2-solution:88W8977>; *see also, e.g.*, <https://www.nxp.com/products/wireless-connectivity/dsrc-safety-modem/v2x-rf-transceiver:TEF5100>; <https://www.nxp.com/products/wireless-connectivity/wi-fi-plus-bluetooth-plus-802-15-4/2-4-5-ghz-dual-band-2x2-wi-fi-6-802-11ax-plus-bluetooth-5-1-solution:IW620>; <https://www.nxp.com/products/wireless-connectivity/wi-fi-plus-bluetooth-plus-802-15-4/2-4-5-ghz-dual-band-2x2-wi-fi-6-802-11ax-plus-bluetooth-5-3:88W9098>; <https://www.nxp.com/products/wireless-connectivity/wi-fi-plus-bluetooth-plus-802-15-4/2-4-5-ghz-dual-band-2x2-wi-fi-5-802-11ac-plus-bluetooth-5-3-solution:88W8997>.

receiving an input signal at a first matched filtering/correlating module;

Each NXP Chip receives an input signal (e.g., RF, shown in the red box) at a first matched filtering/correlating module (e.g., linear time-variant circuit, including a switch S1 (shown in the purple box), capacitor(s) C1, CF1 (shown in the green boxes), and low impedance load (e.g., feedback resistor(s), shown in the yellow box), shown along the purple path).

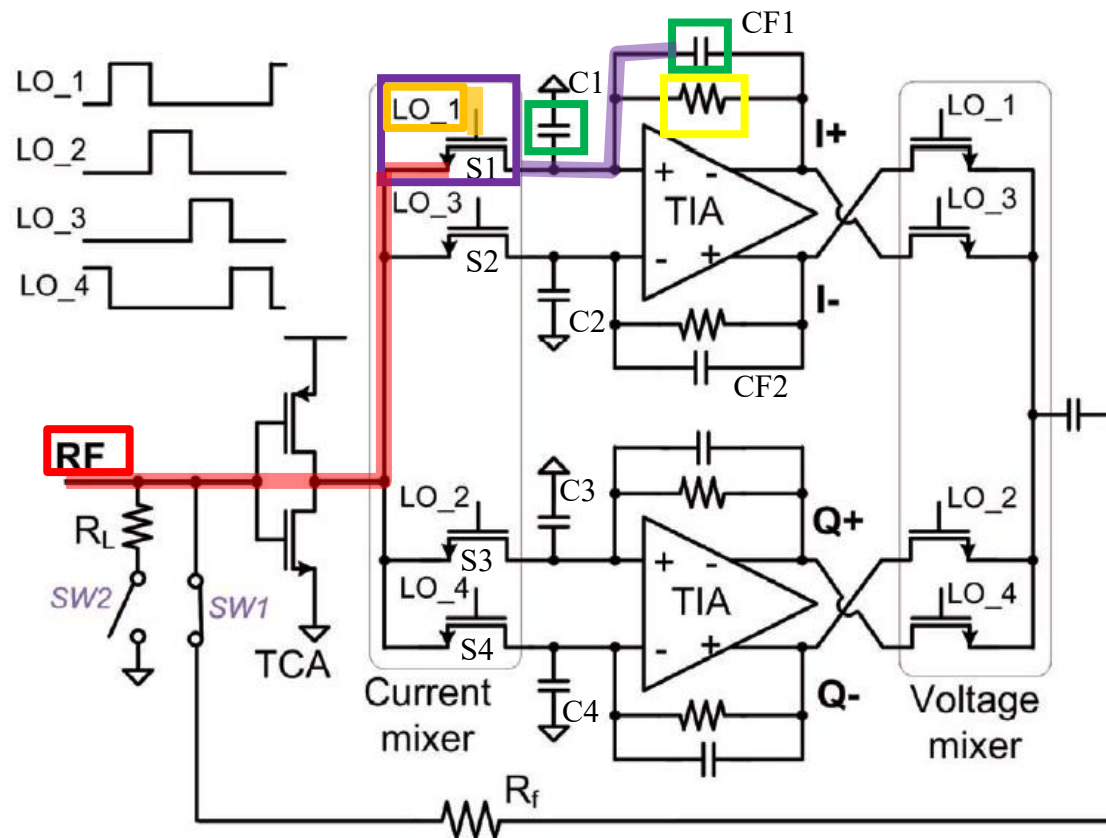


2011 IEEE paper, Figure 21.5.2.

The first matched filtering/correlating module receives the input signal RF along the red path.

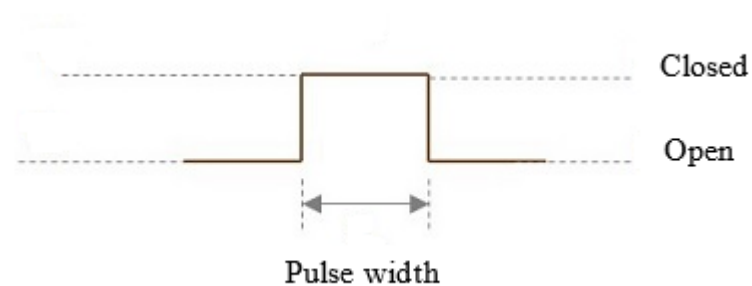
down converting said input signal at said first matched filtering/correlating module according to a first control signal and outputting a first down-converted signal;

Each NXP Chip down-converts the input signal (e.g., RF, shown in the red box) at the first matched filtering/correlating module (e.g., linear time-variant circuit, including a switch S1 (shown in the purple box), capacitor(s) C1, CF1 (shown in the green boxes), and low impedance load (e.g., feedback resistor(s), shown in the yellow box), shown along the purple path) according to a first control signal (e.g., LO_1, shown in the orange box) and outputs a first down-converted signal (e.g., I+).



2011 IEEE paper, Figure 21.5.2.

Switch S1 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_1 (orange box). In particular, switch S1 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red box) in the circuit. The time period for which switch S1 (purple box) is open/closed is determined by LO_1 (orange box). Specifically, LO_1 (orange box) enables (i.e., closes) switch S1 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_1.



When switch S1 (purple box) is ON (closed), current can pass through the switch S1; when the switch is OFF (opened), current is blocked from passing through the switch. The switch S1 is turned ON (closed) by sending control signal LO_1 to the switch at an independent control input. The switch is kept ON (kept closed) for the duration of the signal pulse (i.e., during a sampling aperture of the pulse).

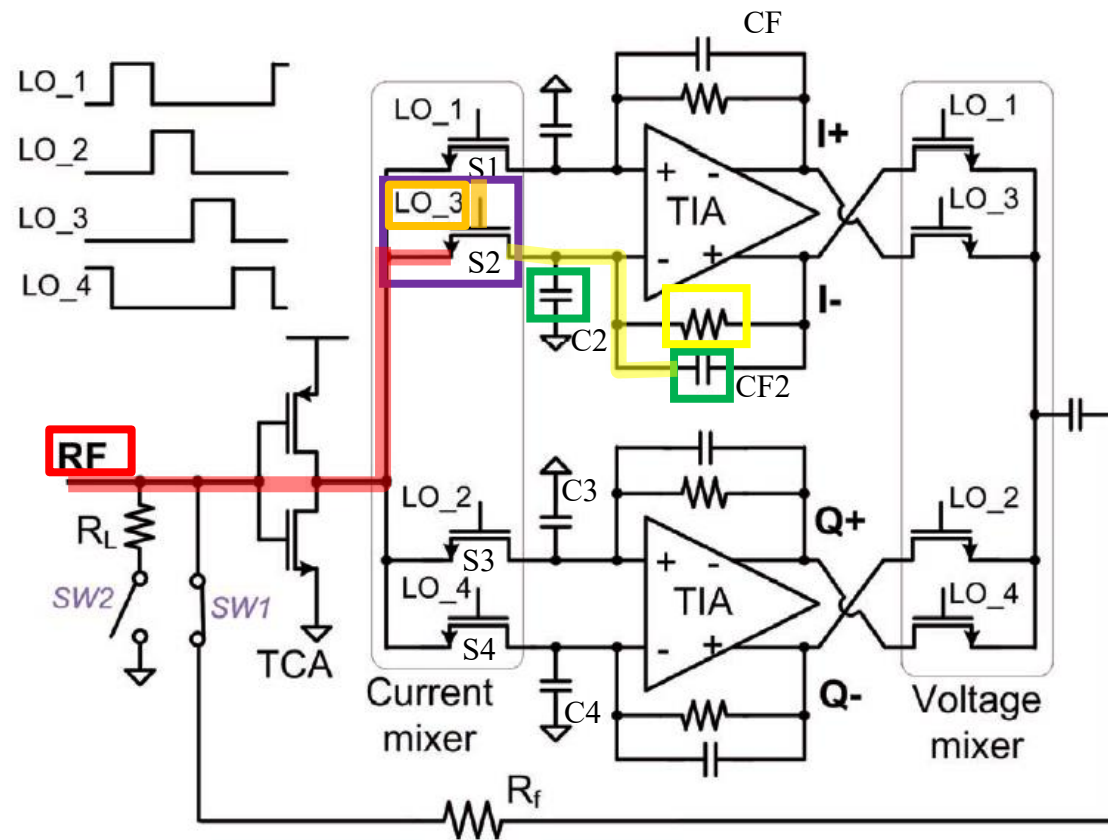
On information and belief, the pulses of control signal LO_1 have a non-negligible, periodic aperture (e.g., nominal 25% duty cycle). Successive pulses of LO_1 (orange box) therefore recursively close/open switch S1 (purple box), which samples the RF signal (red box). The recursive closing/opening of switch S1 (purple box) periodically couples the RF signal (red box) to capacitor(s) C1, CF1 (green boxes). During an aperture of LO_1 (orange box), for example, switch S1 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C1, CF1 (green boxes) and load circuitry (e.g., feedback resistor(s), yellow box). On information and belief, non-negligible amounts of energy from the input signal are accumulated (e.g., in one or more capacitors) and transferred to a low impedance load (e.g., one or more feedback resistors) during an aperture period (e.g., when the switch is closed (ON)). Between apertures of LO_1 (orange box), switch S1 (purple box) remains open, preventing the flow of energy through the switch and consequently discharging energy stored in capacitor(s) C1, CF1 (green boxes) to load circuitry. In this way, real power

	from the input signal is transferred to the low impedance load and produces a down-converted signal with enhanced signal-to-noise power ratio. The sampling, charging, and discharging process outputs the first down-converted signal (e.g., I+).
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	Each NXP Chip meets wireless telecommunication standards including, but not limited to, IEEE 802.11a, 802.11b, 802.11g, 802.11n, 802.11p, and ARIB STD-T55/STD-T75. See, e.g., https://www.nxp.com/products/wireless/dsrc-safety-modem/v2x-rf-transceiver:TEF5100.
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receiving said input signal at a second matched filtering/correlating module;

Each NXP Chip receives the input signal (e.g., RF, shown in the red box), at a second matched filtering/correlating module (e.g., linear time-variant circuit, including a switch S2 (shown in the purple box), capacitor(s) C2, CF2 (shown in the green boxes), and low impedance load (e.g., feedback resistor(s), shown in the yellow box), shown along the yellow path).

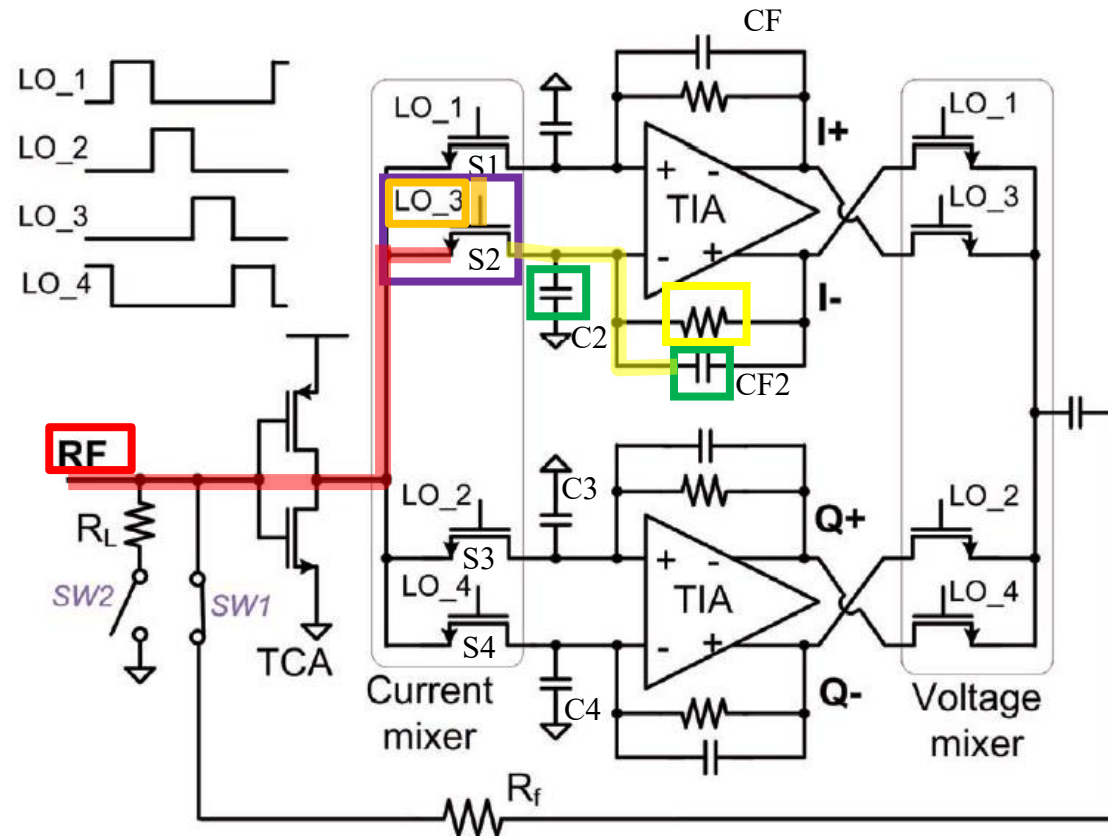


2011 IEEE paper, Figure 21.5.2.

The second matched filtering/correlating module receives the input signal RF along the red path.

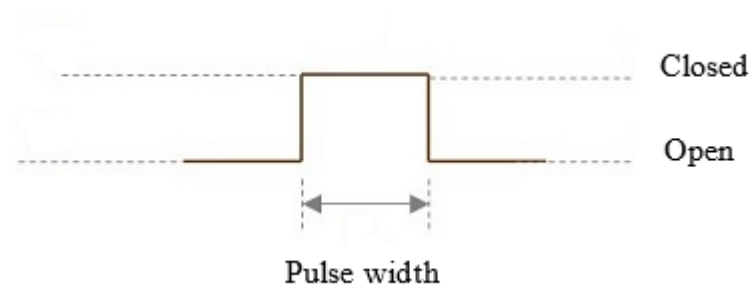
down-converting said input signal at said second matched filtering/correlating module according to a second control signal and outputting a second down-converted signal; and

Each NXP Chip down-converts the input signal (e.g., RF, shown in the red box) at the second matched filtering/correlating module (e.g., linear time-variant circuit, including a switch S2 (shown in the purple box), capacitor(s) C2, CF2 (shown in the green boxes), and low impedance load (e.g., feedback resistor(s), shown in the yellow box), shown along the yellow path) according to a second control signal (e.g., LO_3, shown in the orange box) and outputs a second down-converted signal (e.g., I-).



2011 IEEE paper, Figure 21.5.2.

Switch S2 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_3 (orange box). In particular, switch S2 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red box) in the circuit. The time period for which switch S2 (purple box) is open/closed is determined by LO_3 (orange box). Specifically, LO_3 (orange box) enables (i.e., closes) switch S2 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_3.



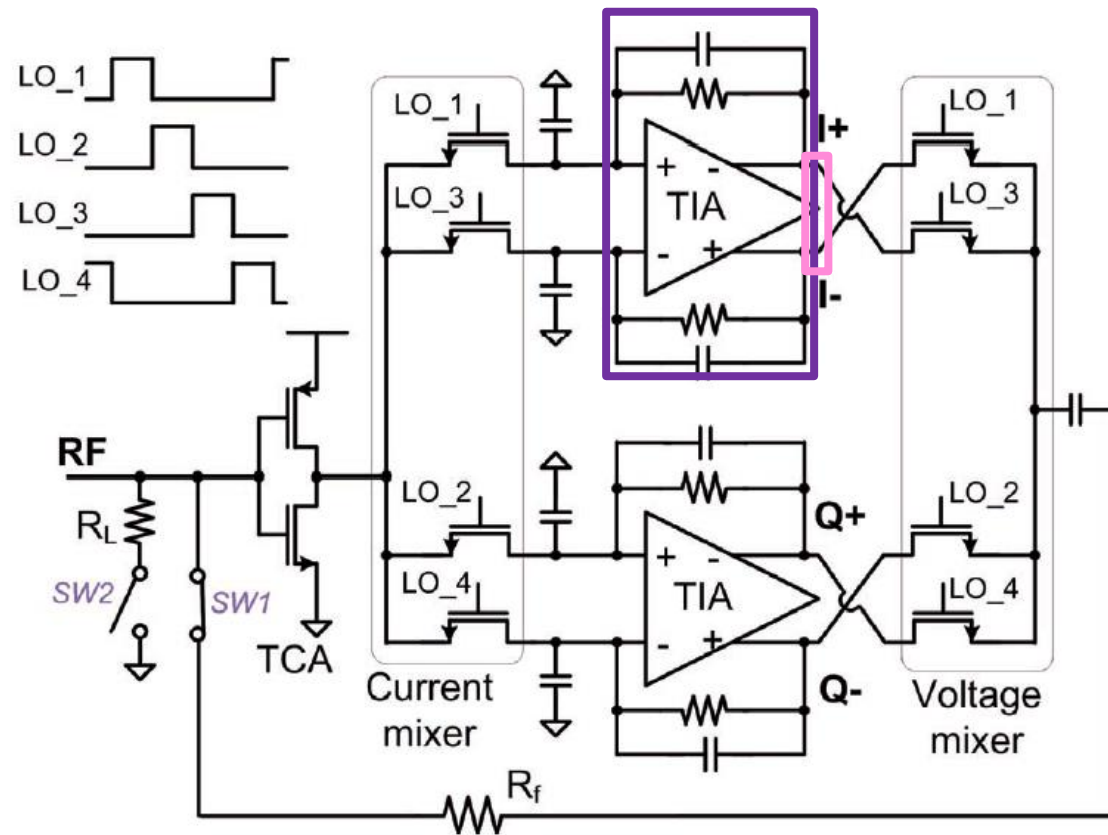
When switch S2 (purple box) is ON (closed), current can pass through the switch S2; when the switch is OFF (opened), current is blocked from passing through the switch. The switch S2 is turned ON (closed) by sending control signal LO_3 to the switch at an independent control input. The switch is kept ON (kept closed) for the duration of the signal pulse (i.e., during a sampling aperture of the pulse).

On information and belief, the pulses of control signal LO_3 have a non-negligible, periodic aperture (e.g., nominal 25% duty cycle). Successive pulses of LO_3 (orange box) therefore recursively close/open switch S2 (purple box), which samples the RF signal (red box). The recursive closing/opening of switch S2 (purple box) periodically couples the RF signal (red box) to capacitor(s) C2, CF2 (green boxes). During an aperture of LO_3 (orange box), for example, switch S2 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C2, CF2 (green boxes) and load circuitry (e.g., feedback resistor(s), yellow box). On information and belief, non-negligible amounts of energy from the input signal are accumulated (e.g., in one or more capacitors) and transferred to a low impedance load (e.g., one or more feedback resistors) during an aperture period (e.g., when the switch is closed (ON)). Between apertures of LO_3 (orange box), switch S2 (purple box) remains open, preventing the flow of energy through the switch and consequently discharging energy stored in capacitor(s) C2, CF2 (green boxes) to load circuitry. In this way, real power

	from the input signal is transferred to the low impedance load and produces a down-converted signal with enhanced signal-to-noise power ratio. The sampling, charging, and discharging process outputs the second down-converted signal (e.g., I-). Each NXP Chip meets wireless telecommunication standards including, but not limited to, IEEE 802.11a, 802.11b, 802.11g, 802.11n, 802.11p, and ARIB STD-T55/STD-T75. See, e.g., https://www.nxp.com/products/wireless/dsrc-safety-modem/v2x-rf-transceiver:TEF5100.
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combining said second down-converted signal and said first down-converted signal to output a first channel down-converted signal.

Each NXP Chip uses a differential amplifier circuit (e.g., differential amplifier circuit including operational amplifier (op-amp) with resistor-capacitor feedback, shown in the purple box) to combine the second down-converted signal (e.g., I-) and the first down-converted signal (e.g., I+) to output a first channel down-converted signal (e.g., shown in the pink box).



2011 IEEE paper, Figure 21.5.2.

The differential amplifier circuit (purple box) receives two inputs, the first down-converted signal (e.g., I+) and the second down-converted signal (e.g., I-), and outputs a down-converted signal (e.g., shown in the pink box), which is a function of the difference between the inputs. In particular, the differential amplifier circuit combines the first down-converted signal (I+) with the second down-converted signal (I-) and outputs a down-converted signal (e.g., shown in the pink box) that is a function of the combination of the first and second down-converted signals.

10.1.2 Differential Signals

Let us return to the circuit of Fig. 10.2(a) and recall that the duplicate stage consisting of Q_2 and R_{C2} remains "idle," thereby "wasting" current. We may therefore wonder if this stage can provide signal amplification in addition to establishing a reference point for V_{out} . In our first attempt, we directly apply the input signal to the base of Q_2 [Fig. 10.3(a)]. Unfortunately, the signal components at X and Y are in phase, canceling each other as they appear in $v_X - v_Y$:

$$v_X = A_v v_{in} + v_r \quad (10.5)$$

$$v_Y = A_v v_{in} + v_r \quad (10.6)$$

$$\Rightarrow v_X - v_Y = 0. \quad (10.7)$$

For the signal components to *enhance* each other at the output, we can *invert* one of the input phases as shown in Fig. 10.3(b), obtaining

$$v_X = A_v v_{in} + v_r \quad (10.8)$$

$$v_Y = -A_v v_{in} + v_r \quad (10.9)$$

and hence

$$v_X - v_Y = 2A_v v_{in}. \quad (10.10)$$

B. Razavi, *Fundamentals of Microelectronics* at p. 439

Energy, power, current, voltage, resistance/impedance, and time relationships can be expressed as follows:

Energy Power Current Voltage Resistance Impedance Time Relationships

$$E = \left(\frac{J}{\Delta t} \right) \cdot \Delta t$$

$$P = \left(\frac{J}{\Delta t} \right)$$

$$E = P \cdot \Delta t$$

Where:

E is Energy in Joules

P is Power in Watts*

t is Time in Seconds

I is Current in Amperes

V is Voltage in Volts

R is Resistance or Impedance (Z) in Ohms

*Power is the rate of energy transfer

$$P = V \cdot I$$

$$P = \left(\frac{V^2}{R} \right)$$

$$P = I^2 \cdot R$$

$$E = V \cdot I \cdot \Delta t$$

$$E = \left(\frac{V^2}{R} \right) \cdot \Delta t$$

$$E = I^2 \cdot R \cdot \Delta t$$

$$V = \left(\frac{E}{I \cdot \Delta t} \right)$$

$$V = \sqrt{\left(\frac{E \cdot R}{\Delta t} \right)}$$

$$I = \sqrt{\left(\frac{E}{R \cdot \Delta t} \right)}$$

$$I = \left(\frac{E}{V \cdot \Delta t} \right)$$