

Claim Chart For Infringement of U.S. Patent No. 9,118,528 by NXP Wireless Chips

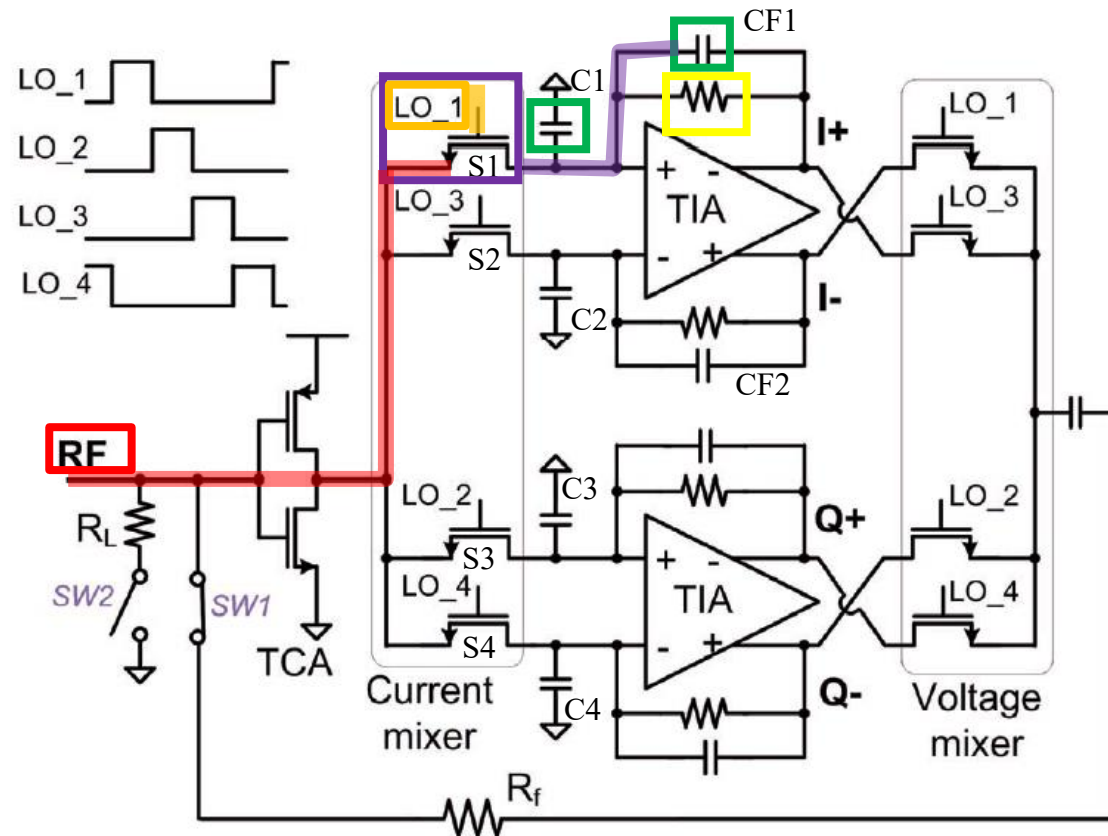
Claim 1	NXP Wireless Chips
A system for frequency down-converting a modulated carrier signal to a baseband signal, comprising:	NXP directly infringes (literally and/or under the doctrine of equivalents) the '528 patent by making, using, selling, offering for sale, and/or importing in/into the United States products covered by at least claims 1-5, 8, 9, 11-23, 26, 27, and 29-36 of the '528 patent. NXP products that infringe claims 1-5, 8, 9, 11-23, 26, 27, and 29-36 of the '528 patent include NXP wireless chips (e.g., Wi-Fi and/or Bluetooth chips) including, without limitation, NXP part nos. TEF510x series, IW620 series, IW416 series, 88W9098 series, 88W9097 series, 88W9068 series, 88W9064 series, 88W8997 series, 88W8987 series, 88W8977 series, 88W8897 series, 88W8887 series, 88W8801 series, 88W8787 series, 88W8786 series, 88W8766 series, 88W8764 series, 88W8688 series, 88Q9098 series, 88MW3xx series, and any other NXP chip (collectively, "NXP Chips") that is capable of down-converting a modulated carrier signal to a baseband signal as claimed in the '528 patent. On information and belief, each NXP Chip includes at least one or more switches/transistors that sample a carrier signal, one or more capacitors that store non-negligible amounts of energy from a carrier signal, and one or more resistors providing a low impedance load(s). On information and belief, the structure, function, and operation of NXP Chips are substantially similar to one another with respect to the claims at issue. On information and belief, the NXP Chips are described, in part, in the IEEE paper entitled, "A Compact SAW-less Multiband WCDMA/GPS Receiver Front-End with Translational Loop for Input Matching" by X. He and H. Kundur, 2011 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 2011, pp. 372-374 (hereinafter referred to as 2011 IEEE paper). On information and belief, each NXP Chip is/includes a system for frequency down-converting a modulated carrier signal (e.g., high frequency RF signal) to a baseband signal. For example, NXP's 88W8977 "is a highly integrated single-chip solution that incorporates both Wi-Fi (2.4/5 GHz) and Bluetooth technology. The IEEE 802.11n compliant dual-band system-on-chip offers Wi-Fi data rates up to MCS 7 (150 Mbit/s). The SoC is specifically designed to support the speed, reliability, and quality requirements of devices such as wearables, Internet of Things (IoT) and smart home applications. The Combo solution provides both

	simultaneous and independent operation of the IEEE 802.11n compliant 1x1 spatial stream and Bluetooth 5.2 with high speeds and mesh networking for increased Internet of Things (IoT) functionality.”¹ Accordingly, each NXP Chip is configured to receive a modulated carrier signal (e.g., high frequency RF signal). In order to process such a signal, the each NXP Chip must necessarily down-convert the modulated carrier signal to a baseband signal.
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¹ <https://www.nxp.com/products/wireless-connectivity/wi-fi-plus-bluetooth-plus-802-15-4/2-4-5-ghz-dual-band-1x1-wi-fi-4-802-11n-plus-bluetooth-5-2-solution:88W8977>; *see also, e.g.*, <https://www.nxp.com/products/wireless-connectivity/dsrc-safety-modem/v2x-rf-transceiver:TEF5100>; <https://www.nxp.com/products/wireless-connectivity/wi-fi-plus-bluetooth-plus-802-15-4/2-4-5-ghz-dual-band-2x2-wi-fi-6-802-11ax-plus-bluetooth-5-1-solution:IW620>; <https://www.nxp.com/products/wireless-connectivity/wi-fi-plus-bluetooth-plus-802-15-4/2-4-5-ghz-dual-band-2x2-wi-fi-6-802-11ax-plus-bluetooth-5-3:88W9098>; <https://www.nxp.com/products/wireless-connectivity/wi-fi-plus-bluetooth-plus-802-15-4/2-4-5-ghz-dual-band-2x2-wi-fi-5-802-11ac-plus-bluetooth-5-3-solution:88W8997>.

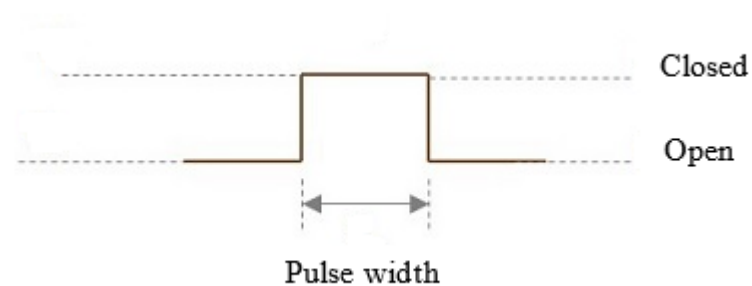
a first switch coupled to a first control signal which comprises a sampling aperture with a specified frequency, wherein the first switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said first switch during the sampling aperture of the first control signal;

Each NXP Chip includes a first switch (e.g., switch S1, shown in the purple box) coupled to a first control signal (e.g., LO_1, shown in the orange box) which comprises a sampling aperture with a specified frequency, wherein the first switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal (e.g., RF, shown in the red box) as an output of the first switch during the sampling aperture of the first control signal.



2011 IEEE paper, Figure 21.5.2.

Switch S1 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_1 (orange box). In particular, switch S1 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red box) in the circuit. The time period for which switch S1 (purple box) is open/closed is determined by LO_1 (orange box). Specifically, LO_1 (orange box) enables (i.e., closes) switch S1 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_1.

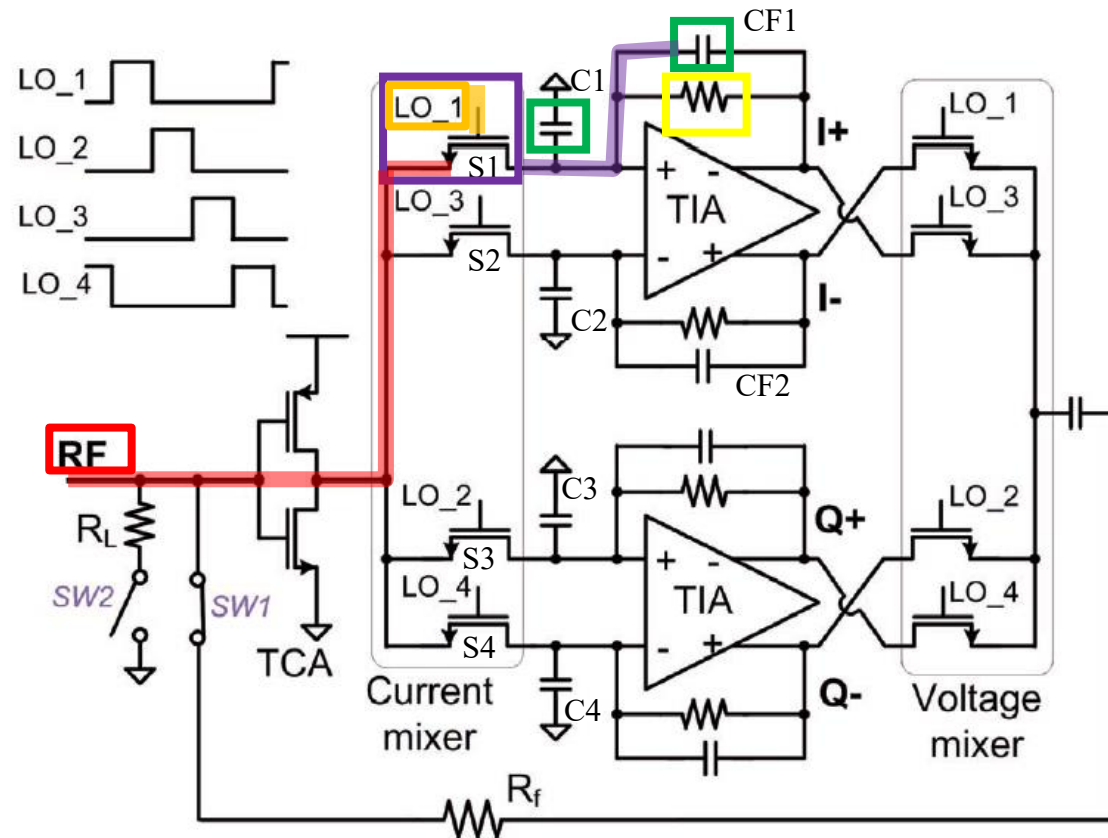


When switch S1 (purple box) is ON (closed), current can pass through the switch S1; when the switch is OFF (opened), current is blocked from passing through the switch. The switch S1 is turned ON (closed) by sending control signal LO_1 to the switch at an independent control input. The switch is kept ON (kept closed) for the duration of the signal pulse (i.e., during a sampling aperture of the pulse).

On information and belief, the pulses of control signal LO_1 have a non-negligible, periodic aperture (e.g., nominal 25% duty cycle). As such, switch S1 (purple box) is closed during an aperture of LO_1 (orange box) and remains open between apertures of LO_1. During an aperture of LO_1 (orange box), energy from RF (red box) that is distinguishable from noise is transferred across the switch to an output of switch S1 (purple box).

a first energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted in-phase baseband signal portion of said modulated carrier signal;

Each NXP Chip includes a first energy storage element (e.g., capacitors C1, CF1, shown in the green boxes) that stores the transferred energy from the modulated carrier signal (e.g., RF, shown in the red box) and outputs a down-converted in-phase baseband signal portion (e.g., I+) of the modulated carrier signal.



2011 IEEE paper, Figure 21.5.2.

As explained above, control signal LO_1 (orange box) enables (i.e., closes) switch S1 (purple box) during an aperture thereof. Successive pulses of LO_1 (orange box) therefore recursively close/open switch S1 (purple box). The recursive closing/opening of switch S1 (purple box) periodically couples the input signal RF (red box) to capacitor(s) C1, CF1 (green boxes). During an aperture of LO_1 (orange box), for example, switch S1 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C1, CF1 (green boxes) along the purple path. Between apertures of LO_1 (orange box), switch S1 (purple box) remains open, preventing the flow of energy through the switch and consequently discharging energy stored in capacitor(s) C1, CF1 (green boxes) to load circuitry (e.g., feedback resistor(s), yellow box). Accordingly, capacitor(s) C1, CF1 (green boxes) discharges stored energy, thereby outputting a down-converted in-phase baseband signal portion I+ (pink box) of the modulated carrier signal.

Each NXP Chip meets wireless telecommunication standards including, but not limited to, IEEE 802.11a, 802.11b, 802.11g, 802.11n, 802.11p, and ARIB STD-T55/STD-T75. See, e.g., <https://www.nxp.com/products/wireless/dsrc-safety-modem/v2x-rf-transceiver:TEF5100>.

Stored Energy

The power delivered to a circuit element is the product of the current and the voltage (provided that the references have the passive configuration):

$$p(t) = v(t)i(t) \quad (3.9)$$

Using Equation 3.3 to substitute for the current, we have

$$p(t) = Cv \frac{dv}{dt} \quad (3.10)$$

Suppose we have a capacitor that initially has $v(t_0) = 0$. Then the initial stored electrical energy is zero, and we say that the capacitor is uncharged. Furthermore, suppose that between time t_0 and some later time t the voltage changes from 0 to $v(t)$ volts. As the voltage magnitude increases, energy is delivered to the capacitor, where it is stored in the electric field between the plates.

If we integrate the power delivered from t_0 to t , we find the energy delivered:

$$w(t) = \int_{t_0}^t p(t) dt \quad (3.11)$$

Using Equation 3.10 to substitute for power, we find that

$$w(t) = \int_{t_0}^t Cv \frac{dv}{dt} dt \quad (3.12)$$

Canceling differential time and changing the limits to the corresponding voltages, we have

$$w(t) = \int_0^{v(t)} Cv dv \quad (3.13)$$

Integrating and evaluating, we get

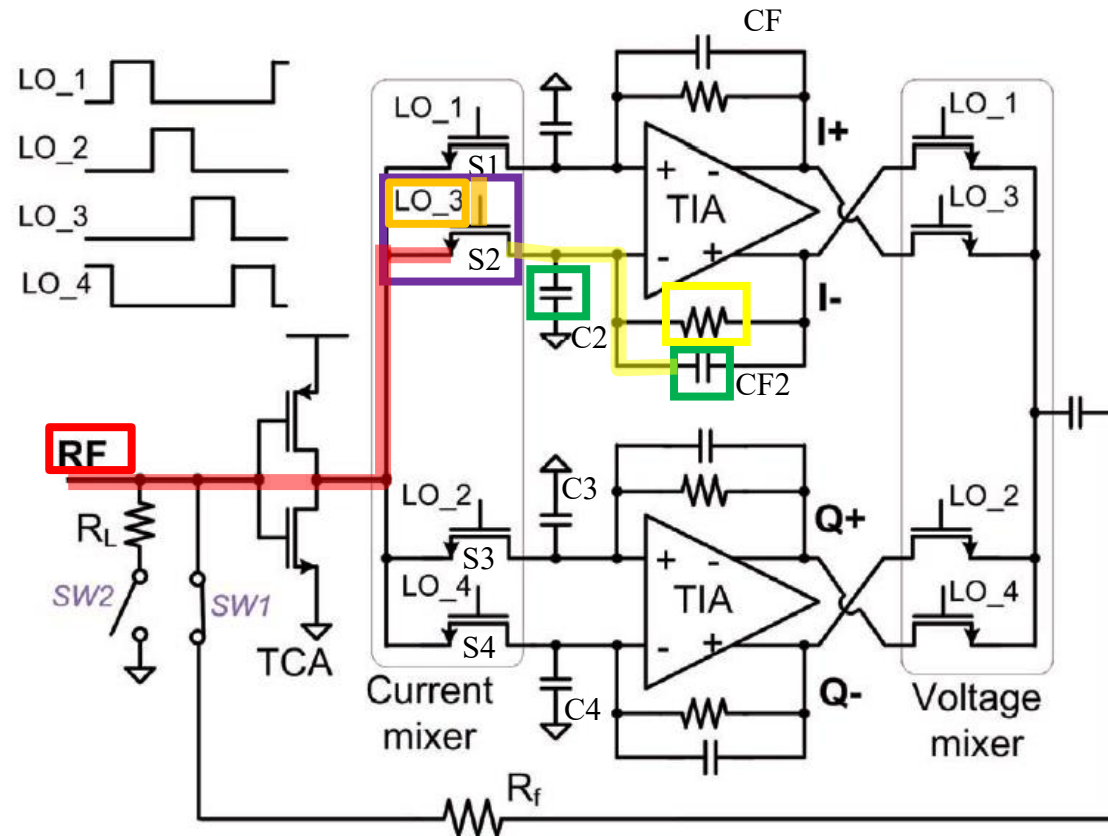
$$w(t) = \frac{1}{2} Cv^2(t) \quad (3.14)$$

This represents energy stored in the capacitance that can be returned to the circuit.

See Hambley, *Electrical Engineering Principles and Applications*, 6th Ed., Prentice Hall, 2014, p. 129 -130.

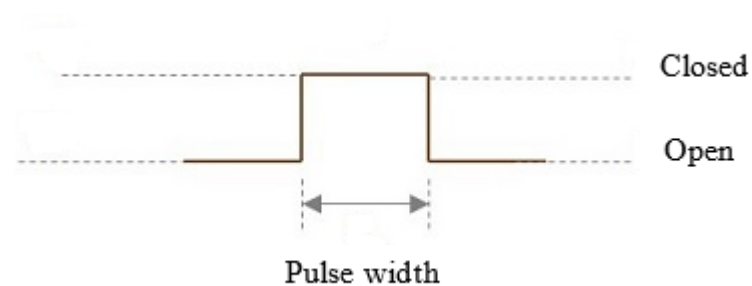
a second switch coupled to a second control signal which comprises a sampling aperture with a specified frequency, wherein the second switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said second switch during the sampling aperture of the second control signal;

Each NXP Chip includes a second switch (e.g., switch S2, shown in the purple box) coupled to a second control signal (e.g., LO_3, shown in the orange box) which comprises a sampling aperture with a specified frequency, wherein the second switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal (e.g., RF, shown in the red box) as an output of the second switch during the sampling aperture of the second control signal.



2011 IEEE paper, Figure 21.5.2.

Switch S2 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_3 (orange box). In particular, switch S2 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red box) in the circuit. The time period for which switch S2 (purple box) is open/closed is determined by control signal LO_3 (orange box). Specifically, control signal LO_3 (orange box) enables (i.e., closes) switch S2 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_3.

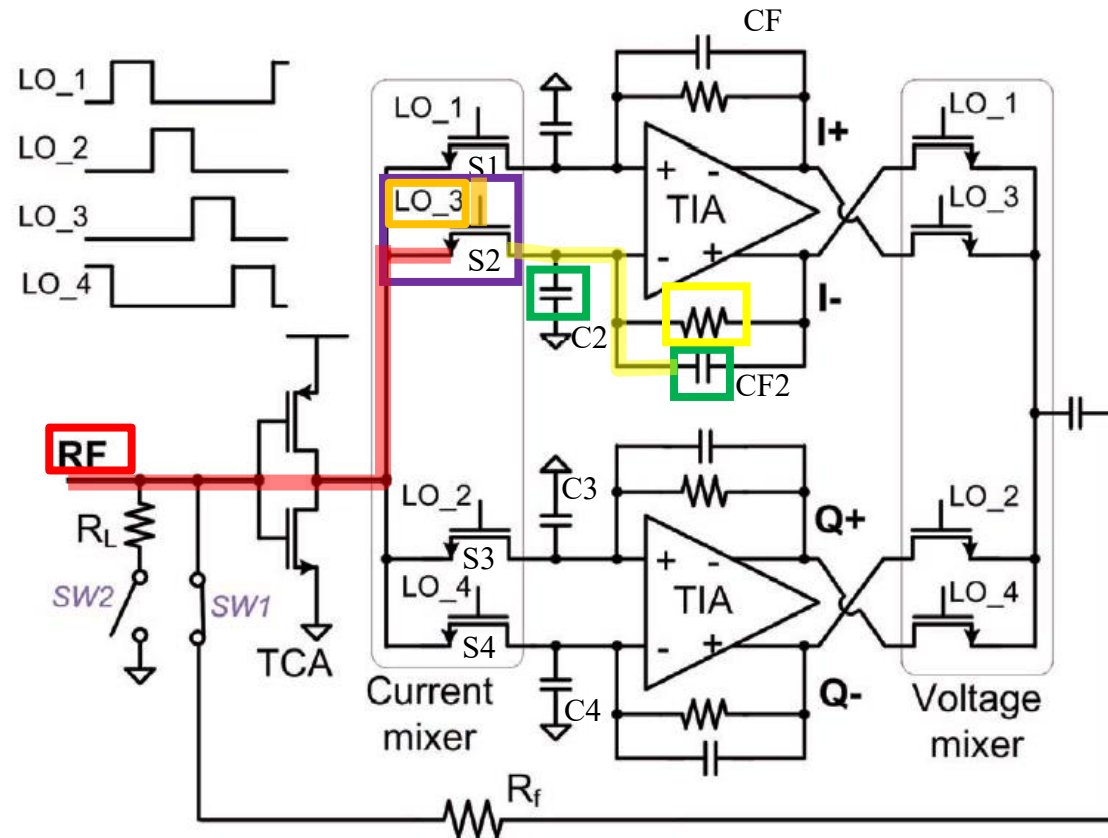


When switch S2 (purple box) is ON (closed), current can pass through the switch S2; when the switch is OFF (opened), current is blocked from passing through the switch. The switch S2 is turned ON (closed) by sending control signal LO_3 to the switch at an independent control input. The switch is kept ON (kept closed) for the duration of the signal pulse (i.e., during a sampling aperture of the pulse).

On information and belief, the pulses of control signal LO_3 have a non-negligible, periodic aperture (e.g., nominal 25% duty cycle). As such, switch S2 (purple box) is closed during an aperture of LO_3 (orange box) and remains open between apertures of LO_3. During an aperture of LO_3 (orange box), energy from RF (red box) that is distinguishable from noise is transferred across the switch to an output of switch S2 (purple box).

a second energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted inverted in-phase baseband signal portion of said modulated carrier signal;

Each NXP Chip includes a second energy storage element (e.g., capacitor(s) C2, CF2 shown in the green boxes) that stores the transferred energy from the modulated carrier signal (e.g., RF, shown in the red box) and outputs a down-converted inverted in-phase baseband signal portion (e.g., I-) of the modulated carrier signal.



2011 IEEE paper, Figure 21.5.2.

As explained above, control signal LO_3 (orange box) enables (i.e., closes) switch S2 during an aperture thereof. Successive pulses of LO_3 (orange box) therefore recursively close/open switch S2 (purple box). The recursive closing/opening of switch S2 (purple box) periodically couples the input signal RF (red box) to the capacitor(s) C2, CF2 (green boxes). During an aperture of LO_3 (orange box), for example, switch S2 (purple box) closes and energy LO_3 (orange box), switch S2 (purple box) remains open, preventing the flow of energy through the switch and consequently discharging energy stored in capacitor(s) C2, CF2 (green boxes) to load circuitry (e.g., feedback resistor(s), yellow box). Accordingly, capacitor(s) C2, CF2 (green boxes) discharges stored energy, thereby outputting a down-converted inverted in-phase baseband signal portion I- of the modulated carrier signal.

Each NXP Chip meets wireless telecommunication standards including, but not limited to, IEEE 802.11a, 802.11b, 802.11g, 802.11n, 802.11p, and ARIB STD-T55/STD-T75. See, e.g., <https://www.nxp.com/products/wireless/dsrc-safety-modem/v2x-rf-transceiver:TEF5100>.

Stored Energy

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Using Equation 3.3 to substitute for the current, we have

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Suppose we have a capacitor that initially has $v(t_0) = 0$. Then the initial stored electrical energy is zero, and we say that the capacitor is uncharged. Furthermore, suppose that between time t_0 and some later time t the voltage changes from 0 to $v(t)$ volts. As the voltage magnitude increases, energy is delivered to the capacitor, where it is stored in the electric field between the plates.

If we integrate the power delivered from t_0 to t , we find the energy delivered:

$$w(t) = \int_{t_0}^t p(t) dt \quad (3.11)$$

Using Equation 3.10 to substitute for power, we find that

$$w(t) = \int_{t_0}^t Cv \frac{dv}{dt} dt \quad (3.12)$$

Canceling differential time and changing the limits to the corresponding voltages, we have

$$w(t) = \int_0^{v(t)} Cv dv \quad (3.13)$$

Integrating and evaluating, we get

$$w(t) = \frac{1}{2} Cv^2(t) \quad (3.14)$$

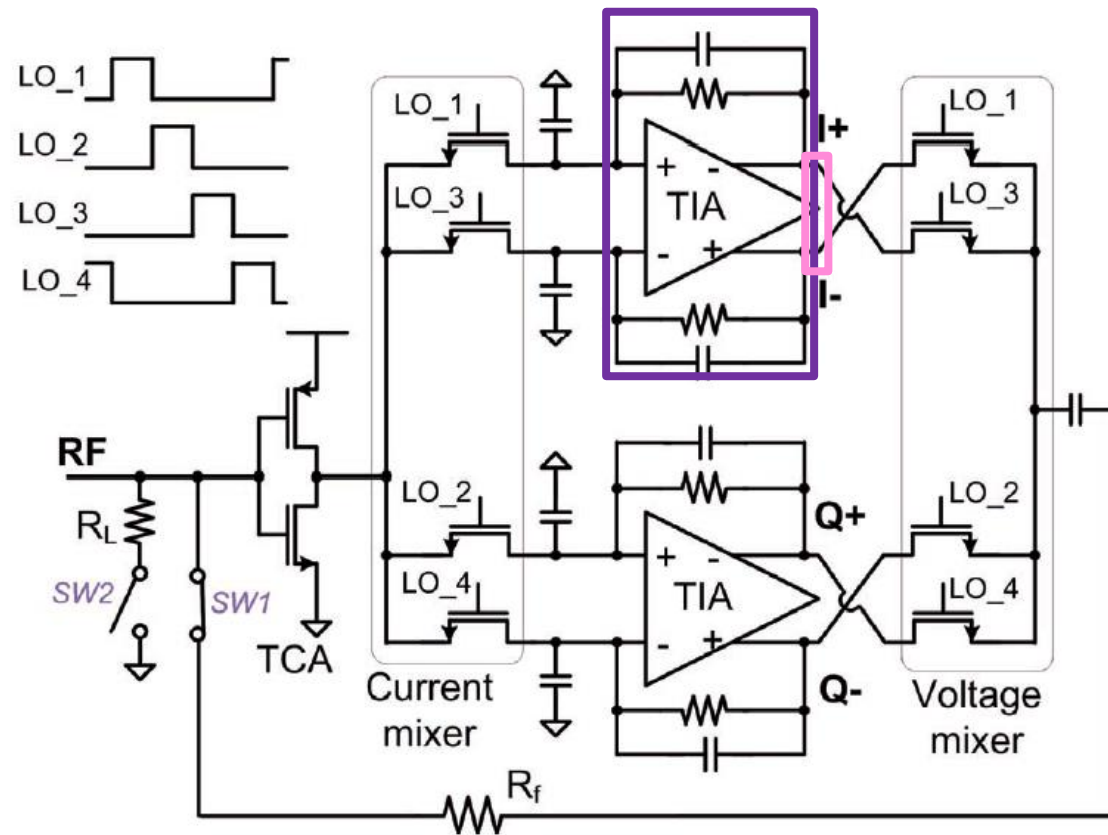
This represents energy stored in the capacitance that can be returned to the circuit.

See Hambley, *Electrical Engineering Principles and Applications*, 6th Ed., Prentice Hall, 2014, p. 129 -130.

wherein the portions of transferred energy from each of the first and second switch are integrated over time to accumulate said portions of transferred energy from which said down-converted in-phase baseband signal portion and said down-converted inverted in-phase baseband signal portion are derived; and	Each NXP Chip is/includes a system wherein portions of transferred energy from each of the first and second switch (e.g., switch S1 and switch S2, respectively) are integrated over time to accumulate the portions of transferred energy from which the down-converted in-phase baseband signal portion (e.g., I+) and the down-converted inverted in-phase baseband signal portion (e.g., I-) are derived. In particular, capacitors C1/CF1 and C2/CF2 accumulate the portions of transferred energy (i.e., energy portions passing through enabled switches S1 and S2, respectively), thereby integrating the portions of transferred energy over time. See Hambley, <i>Electrical Engineering Principles and Applications</i>, 6th Ed., Prentice Hall, 2014, p. 129-130 (above). During an aperture of LO_1 (orange box), for example, switch S1 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C1, CF1 (green boxes) along the purple path. The closing of switch S1 (purple box), therefore, results in capacitor(s) C1, CF1 (green boxes) integrating energy (i.e., during apertures of the LO_1 signal). Between each aperture of control signal LO_1, switch S1 remains open (i.e., RF signal is prevented from passing through the switch). Accordingly, capacitor(s) C1, CF1 discharges a portion of the transferred energy to the load circuitry (e.g., feedback resistor(s), yellow box). The energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle. Accordingly, the capacitor(s) integrate the energy over the aperture periods. Likewise, during an aperture of LO_3 (orange box), switch S2 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C2, CF2 (green boxes) along the yellow path. The closing of switch S2 (purple box), therefore, results in capacitor(s) C2, CF2 (green boxes) integrating energy (i.e., during apertures of the LO_3 signal). Between each aperture of control signal LO_3, switch S2 remains open (i.e., RF signal is prevented from passing through the switch). Accordingly, capacitor(s) C2, CF2 discharges a portion of the transferred energy to the load circuitry (e.g., feedback resistor(s), yellow box). The energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle. Accordingly, the capacitor(s) integrate the energy over the aperture periods.
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a first differential amplifier circuit that combines said down-converted in-phase baseband signal portion with said down-converted inverted in-phase baseband signal portion and outputs a first channel down-converted differential in-phase baseband signal.

On information and belief, each NXP Chip includes a first differential amplifier circuit (e.g., differential amplifier circuit including operational amplifier (op-amp) with resistor-capacitor feedback, shown in the purple box) that combines the down-converted in-phase signal portion (e.g., I+) with the inverted in-phase signal portion (e.g., I-) and outputs a first channel down-converted differential in-phase signal (e.g., shown in the pink box).



2011 IEEE paper, Figure 21.5.2.

The differential amplifier circuit (purple box) receives two inputs, down-converted in-phase signal portion I+ and down-converted inverted in-phase signal portion I- , and outputs a first channel down-converted differential in-phase signal (shown in the pink box), which is a function of the difference between the inputs. In particular, differential amplifier circuit combines the first down-converted signal portion (I+) with the second down-converted signal portion (I-) and outputs a single channel down-converted signal (e.g., shown in the pink box) that is a function of the combination of the first and second down-converted signal portions.

10.1.2 Differential Signals

Let us return to the circuit of Fig. 10.2(a) and recall that the duplicate stage consisting of Q_2 and R_{C2} remains "idle," thereby "wasting" current. We may therefore wonder if this stage can provide signal amplification in addition to establishing a reference point for V_{out} . In our first attempt, we directly apply the input signal to the base of Q_2 [Fig. 10.3(a)]. Unfortunately, the signal components at X and Y are in phase, canceling each other as they appear in $v_X - v_Y$:

$$v_X = A_v v_{in} + v_p \quad (10.5)$$

$$v_Y = A_v v_{in} + v_p \quad (10.6)$$

$$\Rightarrow v_X - v_Y = 0. \quad (10.7)$$

For the signal components to *enhance* each other at the output, we can *invert* one of the input phases as shown in Fig. 10.3(b), obtaining

$$v_X = A_v v_{in} + v_p \quad (10.8)$$

$$v_Y = -A_v v_{in} + v_p \quad (10.9)$$

and hence

$$v_X - v_Y = 2A_v v_{in}. \quad (10.10)$$

B. Razavi, *Fundamentals of Microelectronics* at p. 439

Energy, power, current, voltage, resistance/impedance, and time relationships can be expressed as follows:

Energy Power Current Voltage Resistance Impedance Time Relationships

$$E = \left(\frac{J}{\Delta t} \right) \cdot \Delta t$$

$$P = \left(\frac{J}{\Delta t} \right)$$

$$E = P \cdot \Delta t$$

Where:

E is Energy in Joules

P is Power in Watts*

t is Time in Seconds

I is Current in Amperes

V is Voltage in Volts

R is Resistance or Impedance (Z) in Ohms

*Power is the rate of energy transfer

$$P = V \cdot I$$

$$P = \left(\frac{V^2}{R} \right)$$

$$P = I^2 \cdot R$$

$$E = V \cdot I \cdot \Delta t$$

$$E = \left(\frac{V^2}{R} \right) \cdot \Delta t$$

$$E = I^2 \cdot R \cdot \Delta t$$

$$V = \left(\frac{E}{I \cdot \Delta t} \right)$$

$$V = \sqrt{\left(\frac{E \cdot R}{\Delta t} \right)}$$

$$I = \sqrt{\left(\frac{E}{R \cdot \Delta t} \right)}$$

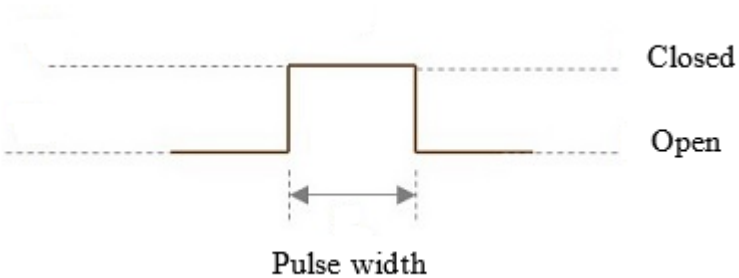
$$I = \left(\frac{E}{V \cdot \Delta t} \right)$$

Claim 2	NXP Wireless Chips
The system of claim 1, wherein said modulated carrier signal includes an amplitude variation.	Each NXP Chip is/includes a system wherein the modulated carrier signal (e.g., RF) includes an amplitude variation. Each NXP Chip meets wireless telecommunication standards including, but not limited to, IEEE 802.11a, 802.11b, 802.11g, 802.11n, 802.11p, and ARIB STD-T55/STD-T75. <i>See, e.g.,</i> https://www.nxp.com/products/wireless/dsrc-safety-modem/v2x-rf-transceiver:TEF5100 . Chipsets using IEEE 802.11 technology include support for various modulation schemes such as QAM (quadrature amplitude modulation) and QPSK (quadrature phase shift keying).
Claim 3	NXP Wireless Chips
The system of claim 1, wherein said modulated carrier signal includes a phase variation.	See claim 2.
Claim 4	NXP Wireless Chips
The system of claim 1, wherein said modulated carrier signal includes a combination of amplitude variation and phase variation.	See claim 2.

Claim 5	NXP Wireless Chips
The system of claim 1, wherein the first switch is on for less than one-half cycle of the modulated carrier signal.	Each NXP Chip is/includes a system wherein the first switch (e.g., switch S1) is on for less than one-half cycle of the modulated carrier signal (e.g., RF). Switch S1 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_1 (orange box). In particular, switch S1 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red box) in the circuit. The time period for which switch S1 (purple box) is open/closed is determined by control signal LO_1 (orange box). Specifically, control signal LO_1 (orange box) enables (i.e., closes) switch S1 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_1. The diagram illustrates a square wave pulse representing the control signal LO_1. The pulse transitions from a low state (labeled 'Open') to a high state (labeled 'Closed') and back to the low state. The duration of the high state is indicated by a horizontal double-headed arrow and labeled 'Pulse width'. An aperture of the control signal (e.g., LO_1) therefore possesses a time duration or duty cycle with respect to an LO rate. The duty cycle of the aperture controlled by the control signal (e.g., LO_1) is the percentage of time during a cycle in the switch is closed. On information and belief, the frequency of control signal LO_1 is substantially similar to the frequency of the RF signal. On information and belief, the control signal (e.g., LO_1) has a sampling aperture with a nominal 25% duty cycle. Accordingly, switch S1 is on for less than one-half cycle of RF.

Claim 8	NXP Wireless Chips
The system of claim 1, wherein the first and second control signals each control a charging and discharging cycle of their respective energy storage element by respectively controlling the first and second switching devices so that for each switching device said portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device when the switching device is off.	Each NXP Chip is/includes a system wherein the first and second control signals (e.g., LO_1, LO_3, respectively) each control a charging and discharging cycle of their respective energy storage element (e.g., capacitor(s) C1/CF1, capacitor(s) C2/CF2, respectively) by respectively controlling the first and second switching devices (e.g., switch S1, switch S2, respectively) so that for each switching device said portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device when the switching device is off. As explained above, the recursive closing/opening of the switch S1 (purple box) periodically couples the RF signal (red box) to a capacitor(s) C1, CF1 (green boxes) according to control signal LO_1 (orange box). During a sampling aperture of control signal LO_1, switch S1 closes and energy from the RF signal is directed to capacitor(s) C1, CF1 along the purple path. Between each sampling aperture of LO_1, switch S1 remains open (i.e., RF signal is prevented from passing through the switch). Accordingly, capacitor(s) C1, CF1 discharges a portion of the transferred energy to a load (e.g., feedback resistor(s), yellow box). Likewise, the recursive closing/opening of the switch S2 (purple box) periodically couples the RF signal (red box) to a capacitor(s) C2, CF2 (green boxes) according to control signal LO_3 (orange box). During a sampling aperture of control signal LO_3, switch S2 closes and energy from the RF signal is directed to capacitor(s) C2, CF2 along the yellow path. Between each sampling aperture of LO_3, switch S2 remains open (i.e., RF signal is prevented from passing through the switch). Accordingly, capacitor(s) C2, CF2 discharges a portion of the transferred energy to a load (e.g., feedback resistor(s), yellow box).

Claim 9	NXP Wireless Chips
The system of claim 8, wherein for each respective storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.	Each NXP Chip is/includes a system wherein for each respective storage element (e.g., capacitor(s) C1/CF1, capacitor(s) C2/CF2), the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle. The first and second control signals (e.g., LO_1 and LO_3, respectively) each control a charging and discharging cycle of their respective energy storage element (e.g., capacitor(s) C1/CF1 and capacitor(s) C2/CF2, respectively) by respectively controlling the first and second switching devices (e.g., switch S1, switch S2, respectively) so that for each switching device the portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device when the switching device is off. The first energy storage element (e.g., capacitor(s) C1, CF1) charges when the first switch (switch S1) is closed (“ON”) and partially discharges when the first switch is open (“OFF”). On information and belief, capacitor(s) C1, CF1 does not completely discharge after the first charging cycle, which means that there is energy available from the previous charging cycle. Thus, the energy discharged by the first energy storage element during any given discharge cycle is not fully discharged with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle of the first energy storage element. Likewise, the second energy storage element (e.g., capacitor(s) C2, CF2) charges when the second switch (switch S2) is closed (“ON”) and partially discharges when the second switch is open (“OFF”). On information and belief, capacitor(s) C2, CF2 does not completely discharge after the charging cycle, which means that there is energy available from the previous charging cycle. Thus, the energy discharged by the second energy storage element during any given discharge cycle is not fully discharged with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle of the second energy storage element.

Claim 11	NXP Wireless Chips
The system of claim 1, wherein the frequencies of the first and second apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.	On information and belief, each NXP Chip is/includes a system wherein the frequencies of the first and second apertures have periods that are two (2) percent or greater of the modulated carrier signal's (e.g., RF) period. The period of the modulated carrier signal is defined as the amount of time required to complete one full cycle. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of an aperture signal (e.g., LO_1, LO_3).  Apertures of the first and second control signals (e.g., LO_1, LO_3) possess a time duration or duty cycle with respect to an LO rate. The duty cycle is the percentage of time during a cycle in which the signal is active (switch is closed). On information and belief, the frequency of the control signals is substantially similar to the frequency of the modulated carrier signal (e.g., RF signal). On information and belief, the control signals (e.g., LO_1, LO_3) have a sampling aperture with a nominal 25% duty cycle. Accordingly, the frequencies of the first and second apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.

Claim 12	NXP Wireless Chips
The system of claim 1, wherein the frequencies of the first and second apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.	On information and belief, each NXP Chip is/includes a system wherein the frequencies of the first and second apertures have periods that are five (5) percent or greater of the modulated carrier signal's (e.g., RF) period. See claim 11.
Claim 13	NXP Wireless Chips
The system of claim 1, wherein the frequencies of the first and second apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.	On information and belief, each NXP Chip is/includes a system wherein the frequencies of the first and second apertures have periods that are ten (10) percent or greater of the modulated carrier signal's (e.g., RF) period. See claim 11.
Claim 14	NXP Wireless Chips
The system of claim 1, wherein the frequencies of the first and second apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal's period.	On information and belief, each NXP Chip is/includes a system wherein the frequencies of the first and second apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal's period. See claim 11.

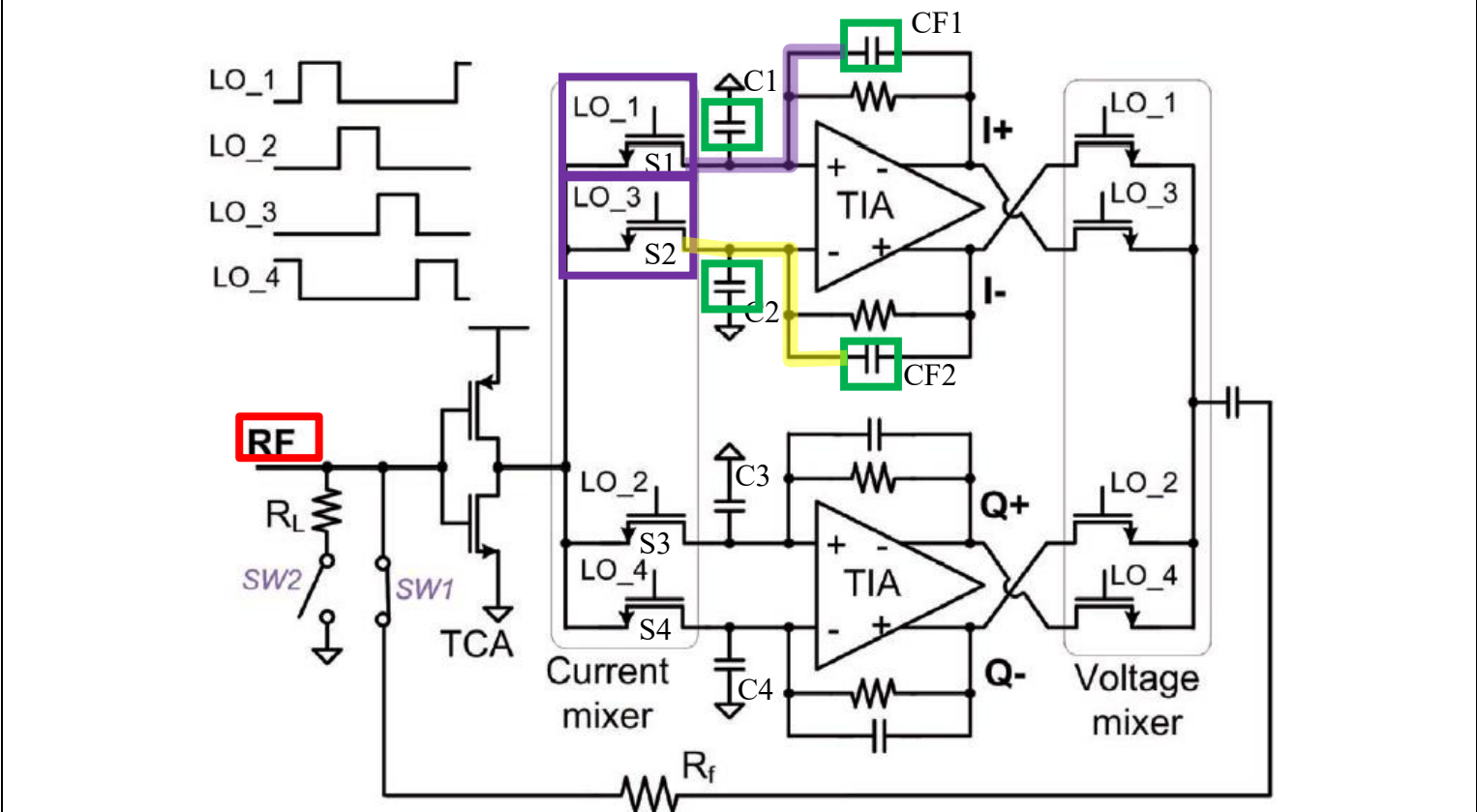
Claim 15	NXP Wireless Chips
The system of claim 1, further comprising: a first filter that filters said down-converted in-phase baseband signal portion; and a second filter that filters said down-converted inverted in-phase baseband signal portion.	On information and belief, each NXP Chip is/includes a system further comprising: a first filter that filters the down-converted in-phase signal portion (e.g., I+); and a second filter that filters the down-converted inverted in-phase signal portion (e.g., I-).
Claim 16	NXP Wireless Chips
The system of claim 15, wherein the first and second filters each comprise a low-pass filter.	On information and belief, each NXP Chip is/includes a system wherein the first and second filters each comprise a low-pass filter. See claim 15.

Claim 17

The system of claim 1, wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first and second switch.

NXP Wireless Chips

Each NXP Chip is/includes a system wherein the portions of transferred energy from each of the first and second switch (e.g., switch S1, switch S2, respectively) which are integrated over time to accumulate the portions of transferred energy are integrated by a separate integration module (e.g., capacitors C1, capacitive feedback CF1, capacitors C2, capacitive feedback CF2, shown in the green boxes) coupled to the output of each the first and second switch.



2011 IEEE paper, Figure 21.5.2.

	The recursive closing/opening of switch S1 (purple box) periodically couples the RF signal (red box) to capacitor(s) C1, CF1 (green boxes). During an aperture of LO_1 (orange box), for example, switch S1 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C1, CF1 (green boxes) along the purple path. Likewise, the recursive closing/opening of switch S2 (purple box) periodically couples the RF signal (red box) to capacitor(s) C2, CF2 (green boxes). During an aperture of LO_3 (orange box), for example, switch S2 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C2, CF2 (green boxes) along the yellow path. Accordingly, capacitors C1, CF1, C2, CF2 (green boxes) accumulate portions of transferred energy from each of the first and second switch (switch S1, switch S2, respectively), thereby integrating the portion of transferred energy over time.
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Stored Energy

The power delivered to a circuit element is the product of the current and the voltage (provided that the references have the passive configuration):

$$p(t) = v(t)i(t) \quad (3.9)$$

Using Equation 3.3 to substitute for the current, we have

$$p(t) = Cv \frac{dv}{dt} \quad (3.10)$$

Suppose we have a capacitor that initially has $v(t_0) = 0$. Then the initial stored electrical energy is zero, and we say that the capacitor is uncharged. Furthermore, suppose that between time t_0 and some later time t the voltage changes from 0 to $v(t)$ volts. As the voltage magnitude increases, energy is delivered to the capacitor, where it is stored in the electric field between the plates.

If we integrate the power delivered from t_0 to t , we find the energy delivered:

$$w(t) = \int_{t_0}^t p(t) dt \quad (3.11)$$

Using Equation 3.10 to substitute for power, we find that

$$w(t) = \int_{t_0}^t Cv \frac{dv}{dt} dt \quad (3.12)$$

Canceling differential time and changing the limits to the corresponding voltages, we have

$$w(t) = \int_0^{v(t)} Cv dv \quad (3.13)$$

Integrating and evaluating, we get

$$w(t) = \frac{1}{2} Cv^2(t) \quad (3.14)$$

This represents energy stored in the capacitance that can be returned to the circuit.

See Hambley, *Electrical Engineering Principles and Applications*, 6th Ed., Prentice Hall, 2014, p. 129 -130.

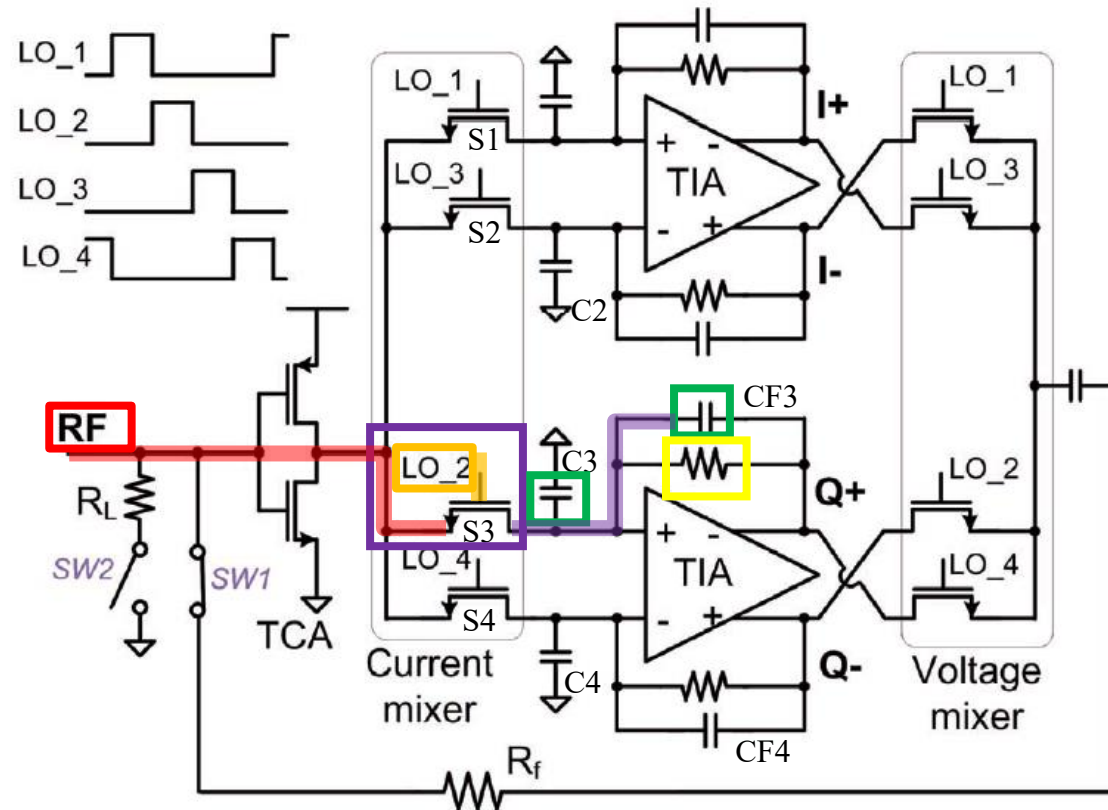
Claim 18	NXP Wireless Chips
The system of claim 1, wherein said first and second storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first and second switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling apertures.	Each NXP Chip is/includes a system wherein the first and second storage elements (e.g., capacitor(s) C1/CF1 and C2/CF2, respectively) are capacitive storage circuits, and wherein the portions of transferred energy from each of the first and second switch which are integrated over time to accumulate the portions of transferred energy are integrated by the capacitive storage circuits as they accumulate charge during successive sampling apertures. <i>See claim 17.</i>

Claim 19

The system of claim 1, further comprising: a third switch coupled to a third control signal which comprises a sampling aperture with a specified frequency, wherein the third switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said third switch during the sampling aperture of the third control signal;

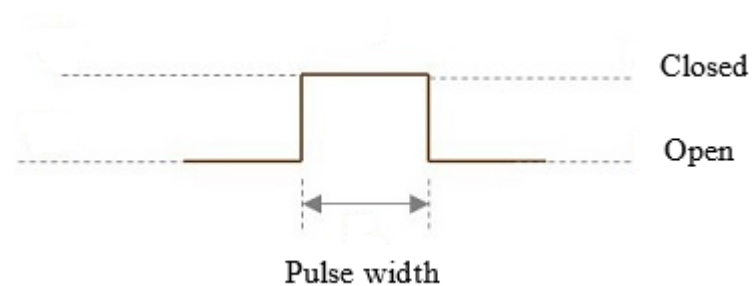
NXP Wireless Chips

Each NXP Chip includes a third switch (e.g., switch S3, shown in the purple box) coupled to a third control signal (e.g., LO_2, shown in the orange box) which comprises a sampling aperture with a specified frequency, wherein the third switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal (e.g., RF, shown in the red box) as an output of the third switch during the sampling aperture of the third control signal.



2011 IEEE paper, Figure 21.5.2.

Switch S3 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_2 (orange box). In particular, switch S3 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red box) in the circuit. The time period for which switch S3 (purple box) is open/closed is determined by LO_2 (orange box). Specifically, LO_2 (orange box) enables (i.e., closes) switch S3 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_2.

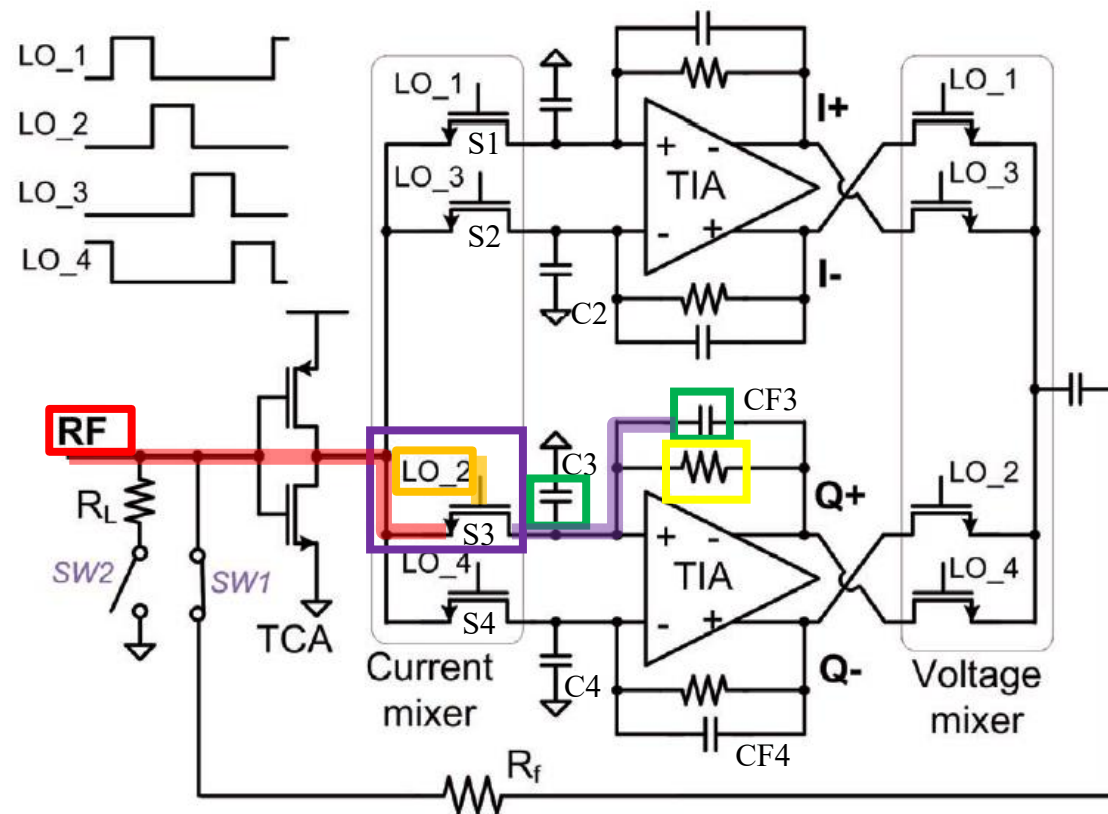


When switch S3 (purple box) is ON (closed), current can pass through the switch S3; when the switch is OFF (opened), current is blocked from passing through the switch. The switch S3 is turned ON (closed) by sending control signal LO_2 to the switch at an independent control input. The switch is kept ON (kept closed) for the duration of the signal pulse (i.e., during a sampling aperture of the pulse).

On information and belief, the pulses of control signal LO_2 have a non-negligible, periodic aperture (e.g., nominal 25% duty cycle). As such, switch S3 (purple box) is closed during an aperture of LO_2 (orange box) and remains open between apertures of LO_2. During an aperture of LO_2 (orange box), energy from RF (red box) that is distinguishable from noise is transferred across the switch to an output of switch S3 (purple box).

a third energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted quadrature-phase baseband signal portion of said modulated carrier signal;

Each NXP Chip includes a third energy storage element (e.g., capacitor(s) C3, CF3, shown in the green boxes) that stores the transferred energy from the modulated carrier signal (e.g., RF, shown in the red box) and outputs a down-converted quadrature-phase baseband signal portion (e.g., Q+) of the modulated carrier signal.



2011 IEEE paper, Figure 21.5.2.

As explained above, control signal LO_2 (orange box) enables (i.e., closes) switch S3 (purple box) during an aperture thereof. Successive pulses of LO_2 (orange box) therefore recursively close/open switch S3 (purple box). The recursive closing/opening of switch S3 (purple box) periodically couples the input signal RF (red box) to capacitor(s) C3, CF3 (green boxes). During an aperture of LO_2 (orange box), for example, switch S3 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C3, CF3 (green boxes) along the purple path. Between apertures of LO_2 (orange box), switch S3 (purple box) remains open, preventing the flow of energy through the switch and consequently discharging energy stored in capacitor(s) C3, CF3 (green boxes) to load circuitry (e.g., feedback resistor(s), yellow box). Accordingly, capacitor(s) C3, CF3 (green boxes) discharges stored energy, thereby outputting a down-converted quadrature-phase baseband signal portion Q+ of the modulated carrier signal.

Each NXP Chip meets wireless telecommunication standards including, but not limited to, IEEE 802.11a, 802.11b, 802.11g, 802.11n, 802.11p, and ARIB STD-T55/STD-T75. See, e.g., <https://www.nxp.com/products/wireless/dsrc-safety-modem/v2x-rf-transceiver:TEF5100>.

Stored Energy

The power delivered to a circuit element is the product of the current and the voltage (provided that the references have the passive configuration):

$$p(t) = v(t)i(t) \quad (3.9)$$

Using Equation 3.3 to substitute for the current, we have

$$p(t) = Cv \frac{dv}{dt} \quad (3.10)$$

Suppose we have a capacitor that initially has $v(t_0) = 0$. Then the initial stored electrical energy is zero, and we say that the capacitor is uncharged. Furthermore, suppose that between time t_0 and some later time t the voltage changes from 0 to $v(t)$ volts. As the voltage magnitude increases, energy is delivered to the capacitor, where it is stored in the electric field between the plates.

If we integrate the power delivered from t_0 to t , we find the energy delivered:

$$w(t) = \int_{t_0}^t p(t) dt \quad (3.11)$$

Using Equation 3.10 to substitute for power, we find that

$$w(t) = \int_{t_0}^t Cv \frac{dv}{dt} dt \quad (3.12)$$

Canceling differential time and changing the limits to the corresponding voltages, we have

$$w(t) = \int_0^{v(t)} Cv dv \quad (3.13)$$

Integrating and evaluating, we get

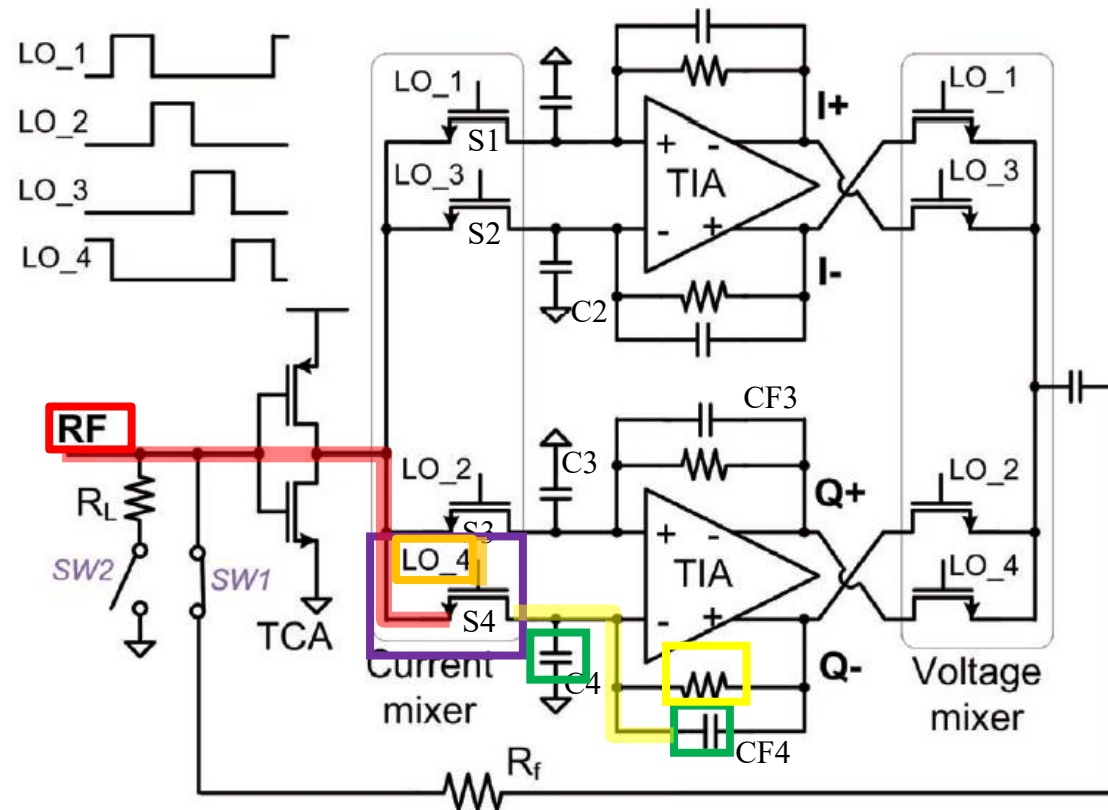
$$w(t) = \frac{1}{2} Cv^2(t) \quad (3.14)$$

This represents energy stored in the capacitance that can be returned to the circuit.

See Hambley, *Electrical Engineering Principles and Applications*, 6th Ed., Prentice Hall, 2014, p. 129 -130.

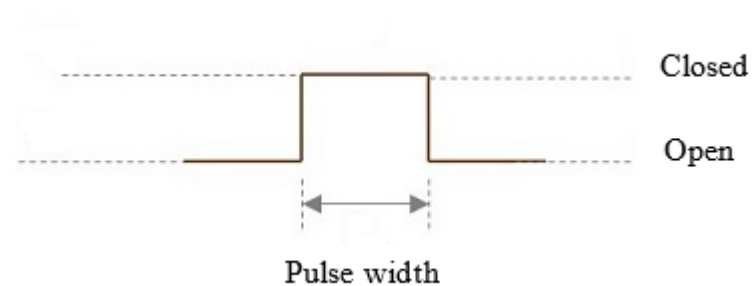
a fourth switch coupled to a fourth control signal which comprises a sampling aperture with a specified frequency, wherein the fourth switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal as an output of said fourth switch during the sampling aperture of the fourth control signal;

Each NXP Chip includes a fourth switch (e.g., switch S4, shown in the purple box) coupled to a fourth control signal (e.g., LO_4, shown in the orange box) which comprises a sampling aperture with a specified frequency, wherein the fourth switch is on and a portion of energy that is distinguishable from noise is transferred from the modulated carrier signal (e.g., RF, shown in the red box) as an output of the fourth switch during the sampling aperture of the fourth control signal.



2011 IEEE paper, Figure 21.5.2.

Switch S4 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO_4 (orange box). In particular, switch S4 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red box) in the circuit. The time period for which switch S4 (purple box) is open/closed is determined by control signal LO_4 (orange box). Specifically, control signal LO_4 (orange box) enables (i.e., closes) switch S4 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO_4.

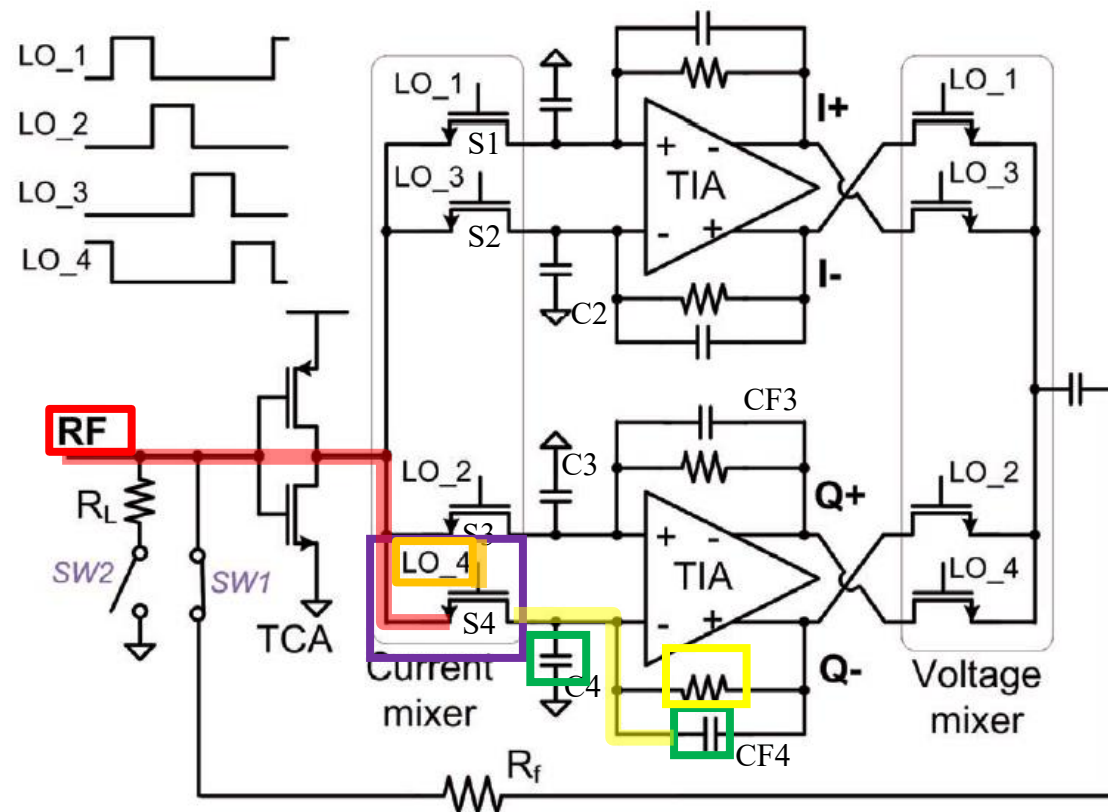


When switch S4 (purple box) is ON (closed), current can pass through the switch S4; when the switch is OFF (opened), current is blocked from passing through the switch. The switch S4 is turned ON (closed) by sending control signal LO_4 to the switch at an independent control input. The switch is kept ON (kept closed) for the duration of the signal pulse (i.e., during a sampling aperture of the pulse).

On information and belief, the pulses of control signal LO_4 have a non-negligible, periodic aperture (e.g., nominal 25% duty cycle). As such, switch S4 (purple box) is closed during an aperture of LO_4 (orange box) and remains open between apertures of LO_4. During an aperture of LO_4 (orange box), energy from RF (red box) that is distinguishable from noise is transferred across the switch to an output of switch S4 (purple box).

a fourth energy storage element that stores the transferred energy from the modulated carrier signal and outputs a down-converted differential quadrature-phase baseband signal portion of said modulated carrier signal;

Each NXP Chip includes a fourth energy storage element (e.g., capacitor(s) C4, CF4, shown in the green boxes) that stores the transferred energy from the modulated carrier signal (e.g., RF, shown in the red box) and outputs a down-converted inverted quadrature-phase baseband signal portion (e.g., Q+) of the modulated carrier signal.



2011 IEEE paper, Figure 21.5.2.

As explained above, control signal LO_4 (orange box) enables (i.e., closes) switch S4 during an aperture thereof. Successive pulses of LO_4 (orange box) therefore recursively close/open switch S4 (purple box). The recursive closing/opening of switch S4 (purple box) periodically couples the input signal RF (red box) to the capacitor(s) C4, CF4 (green boxes). During an aperture of LO_4 (orange box), for example, switch S4 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C4, CF4 (green boxes) along the yellow path. Between apertures of LO_4 (orange box), switch S4 (purple box) remains open, preventing the flow of energy through the switch and consequently discharging energy stored in capacitor(s) C4, CF4 (green boxes) to load circuitry (e.g., feedback resistor(s), yellow box). Accordingly, capacitor(s) C4, CF4 (green boxes) discharges stored energy, thereby outputting a down-converted inverted quadrature-phase baseband signal portion Q- of the modulated carrier signal.

Each NXP Chip meets wireless telecommunication standards including, but not limited to, IEEE 802.11a, 802.11b, 802.11g, 802.11n, 802.11p, and ARIB STD-T55/STD-T75. See, e.g., <https://www.nxp.com/products/wireless/dsrc-safety-modem/v2x-rf-transceiver:TEF5100>.

Stored Energy

The power delivered to a circuit element is the product of the current and the voltage (provided that the references have the passive configuration):

$$p(t) = v(t)i(t) \quad (3.9)$$

Using Equation 3.3 to substitute for the current, we have

$$p(t) = Cv \frac{dv}{dt} \quad (3.10)$$

Suppose we have a capacitor that initially has $v(t_0) = 0$. Then the initial stored electrical energy is zero, and we say that the capacitor is uncharged. Furthermore, suppose that between time t_0 and some later time t the voltage changes from 0 to $v(t)$ volts. As the voltage magnitude increases, energy is delivered to the capacitor, where it is stored in the electric field between the plates.

If we integrate the power delivered from t_0 to t , we find the energy delivered:

$$w(t) = \int_{t_0}^t p(t) dt \quad (3.11)$$

Using Equation 3.10 to substitute for power, we find that

$$w(t) = \int_{t_0}^t Cv \frac{dv}{dt} dt \quad (3.12)$$

Canceling differential time and changing the limits to the corresponding voltages, we have

$$w(t) = \int_0^{v(t)} Cv dv \quad (3.13)$$

Integrating and evaluating, we get

$$w(t) = \frac{1}{2} Cv^2(t) \quad (3.14)$$

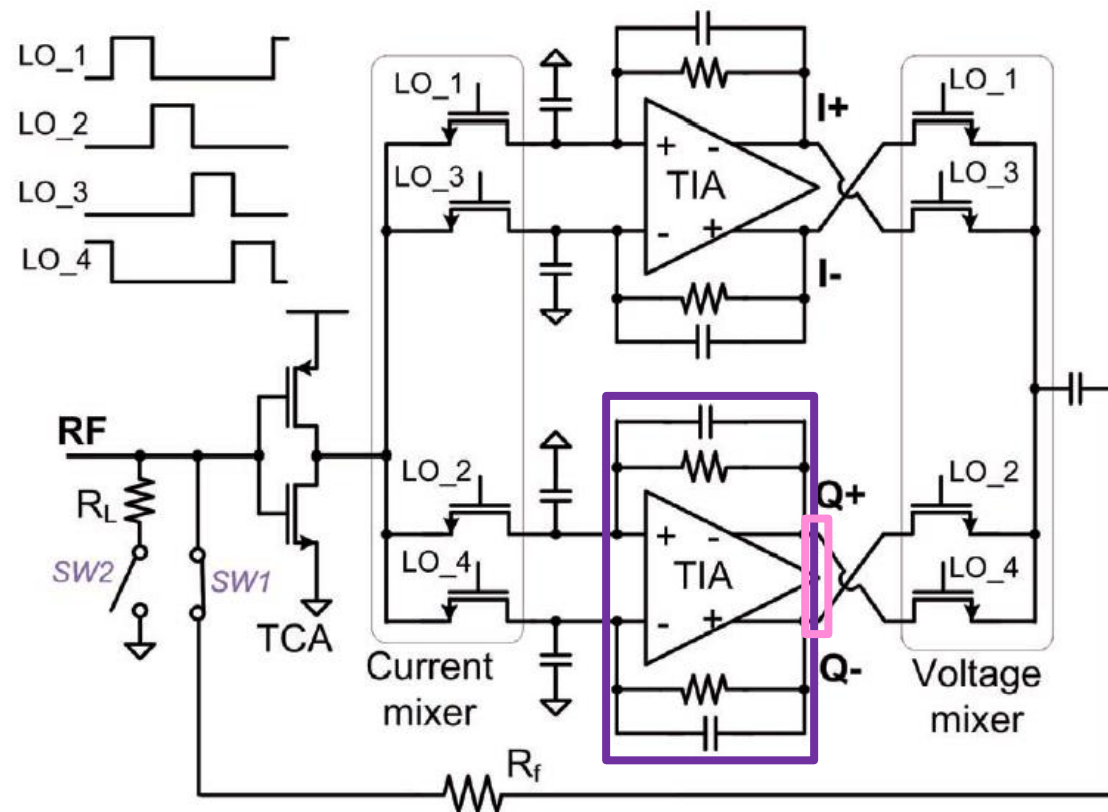
This represents energy stored in the capacitance that can be returned to the circuit.

See Hambley, *Electrical Engineering Principles and Applications*, 6th Ed., Prentice Hall, 2014, p. 129 -130.

wherein the portions of transferred energy from each of the third and fourth switch are integrated over time to accumulate said portions of transferred energy from which said down-converted quadrature-phase baseband signal portion and said down-converted differential quadrature-phase baseband signal portion are derived; and	Each NXP Chip is/includes a system wherein portions of transferred energy from each of the third and fourth switch (e.g., switch S3 and switch S4, respectively) are integrated over time to accumulate the portions of transferred energy from which the down-converted quadrature-phase baseband signal portion (e.g., Q+) and the down-converted inverted quadrature-phase baseband signal portion (e.g., Q-) are derived. In particular, capacitors C3/CF3 and C4/CF4 accumulate the portions of transferred energy (i.e., energy portions passing through enabled switches S3 and S4, respectively), thereby integrating the portions of transferred energy over time. <i>See Hambley, Electrical Engineering Principles and Applications</i>, 6th Ed., Prentice Hall, 2014, p. 129 -130 (above). During an aperture of LO_2 (orange box), for example, switch S3 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C3, CF3 (green boxes) along the purple path. The closing of switch S3 (purple box), therefore, results in capacitor(s) C3, CF3 (green boxes) integrating energy (i.e., during apertures of the LO_2 signal). Between each aperture of control signal LO_2, switch S3 remains open (i.e., RF signal is prevented from passing through the switch). Accordingly, capacitor(s) C3, CF3 discharges a portion of the transferred energy to the load circuitry (e.g., feedback resistor(s), yellow box). The energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle. Accordingly, the capacitor(s) integrate the energy over the aperture periods. Likewise, during an aperture of LO_4 (orange box), switch S4 (purple box) closes and energy from RF (red box) is directed to capacitor(s) C4, CF4 (green boxes) along the yellow path. The closing of switch S4 (purple box), therefore, results in capacitor(s) C4, CF4 (green boxes) integrating energy (i.e., during apertures of the LO_4 signal). Between each aperture of control signal LO_4, switch S4 remains open (i.e., RF signal is prevented from passing through the switch). Accordingly, capacitor(s) C4, CF4 discharges a portion of the transferred energy to the load circuitry (e.g., feedback resistor(s), yellow box). The energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle. Accordingly, the capacitor(s) integrate the energy over the aperture periods.
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a second differential amplifier circuit that combines said down-converted quadrature-phase baseband signal portion with said down-converted differential quadrature-phase baseband signal portion and outputs a second channel down-converted differential quadrature-phase baseband signal.

Each NXP Chip includes a second differential amplifier circuit (e.g., differential amplifier circuit including operational amplifier (op-amp) with parallel resistor-capacitor feedback, shown in the purple box) that combines the down-converted quadrature-phase signal portion (e.g., Q+) with the inverted quadrature-phase signal portion (e.g., Q-) and outputs a second channel down-converted differential quadrature-phase signal (e.g., shown in the pink box).



2011 IEEE paper, Figure 21.5.2.

The differential amplifier circuit (purple box) receives two inputs, down-converted quadrature-phase signal portion Q+ and down-converted inverted quadrature-phase signal portion Q-, and outputs a second channel down-converted differential in-phase signal (e.g., shown in the pink box), which is a function of the difference between the inputs. In particular, differential amplifier circuit combines the first down-converted signal portion (Q+) with the second down-converted signal portion (Q-) and outputs a second channel down-converted signal (e.g., shown in the pink box) that is a function of the combination of the first and second down-converted signal portions.

10.1.2 Differential Signals

Let us return to the circuit of Fig. 10.2(a) and recall that the duplicate stage consisting of Q_2 and R_{C2} remains "idle," thereby "wasting" current. We may therefore wonder if this stage can provide signal amplification in addition to establishing a reference point for V_{out} . In our first attempt, we directly apply the input signal to the base of Q_2 [Fig. 10.3(a)]. Unfortunately, the signal components at X and Y are in phase, canceling each other as they appear in $v_X - v_Y$:

$$v_X = A_v v_{in} + v_p \quad (10.5)$$

$$v_Y = A_v v_{in} + v_p \quad (10.6)$$

$$\Rightarrow v_X - v_Y = 0. \quad (10.7)$$

For the signal components to *enhance* each other at the output, we can *invert* one of the input phases as shown in Fig. 10.3(b), obtaining

$$v_X = A_v v_{in} + v_p \quad (10.8)$$

$$v_Y = -A_v v_{in} + v_p \quad (10.9)$$

and hence

$$v_X - v_Y = 2A_v v_{in}. \quad (10.10)$$

B. Razavi, *Fundamentals of Microelectronics* at p. 439

Energy, power, current, voltage, resistance/impedance, and time relationships can be expressed as follows:

Energy Power Current Voltage Resistance Impedance Time Relationships

$$E = \left(\frac{J}{\Delta t} \right) \cdot \Delta t$$

$$P = \left(\frac{J}{\Delta t} \right)$$

$$E = P \cdot \Delta t$$

Where:

E is Energy in Joules

P is Power in Watts*

t is Time in Seconds

I is Current in Amperes

V is Voltage in Volts

R is Resistance or Impedance (Z) in Ohms

*Power is the rate of energy transfer

$$P = V \cdot I$$

$$P = \left(\frac{V^2}{R} \right)$$

$$P = I^2 \cdot R$$

$$E = V \cdot I \cdot \Delta t$$

$$E = \left(\frac{V^2}{R} \right) \cdot \Delta t$$

$$E = I^2 \cdot R \cdot \Delta t$$

$$V = \left(\frac{E}{I \cdot \Delta t} \right)$$

$$V = \sqrt{\left(\frac{E \cdot R}{\Delta t} \right)}$$

$$I = \sqrt{\left(\frac{E}{R \cdot \Delta t} \right)}$$

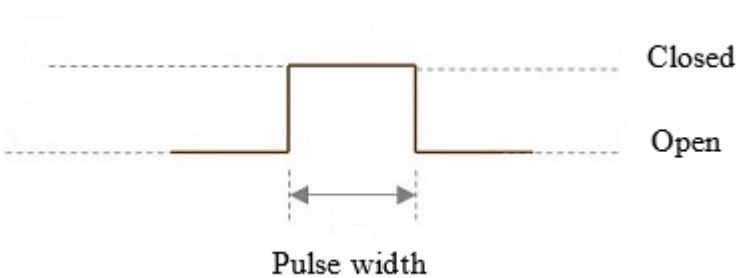
$$I = \left(\frac{E}{V \cdot \Delta t} \right)$$

Claim 20	NXP Wireless Chips
The system of claim 19, wherein said modulated carrier signal includes an amplitude variation.	Each NXP Chip is/includes a system wherein the modulated carrier signal (e.g., RF) includes an amplitude variation. <i>See claim 2.</i>
Claim 21	NXP Wireless Chips
The system of claim 19, wherein said modulated carrier signal includes a phase variation.	Each NXP Chip is/includes a system wherein the modulated carrier signal (e.g., RF) includes a phase variation. <i>See claim 2.</i>
Claim 22	NXP Wireless Chips
The system of claim 19, wherein said modulated carrier signal includes a combination of amplitude variation and phase variation.	Each NXP Chip is/includes a system wherein the modulated carrier signal (e.g., RF) includes a combination of amplitude variation and phase variation. <i>See claim 2.</i>

Claim 23	NXP Wireless Chips
The system of claim 19, wherein the third switch is on for less than one-half cycle of the modulated carrier signal.	Each NXP Chip is/includes a system wherein the third switch (e.g., switch S3) is on for less than one-half cycle of the modulated carrier signal (e.g., RF). Switch S3 (purple box) includes transistors that operate as a switch with switching frequency and duty cycles controlled by LO₂ (orange box). In particular, switch S3 (purple box) periodically opens and closes, thereby controlling the current flow of RF (red box) in the circuit. The time period for which switch S3 (purple box) is open/closed is determined by control signal LO₂ (orange box). Specifically, control signal LO₂ (orange box) enables (i.e., closes) switch S3 (purple box) during an aperture thereof. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of control signal LO₂. The diagram illustrates a square wave pulse representing the control signal LO₂. The pulse is shown as a horizontal line that rises to a high level and then falls back to a low level. The duration of the high level is indicated by a double-headed arrow and labeled 'Pulse width'. To the right of the pulse, the high level is labeled 'Closed' and the low level is labeled 'Open'. An aperture of the control signal (e.g., LO₂) therefore possesses a time duration or duty cycle with respect to an LO rate. The duty cycle of the aperture controlled by the control signal (e.g., LO₂) is the percentage of time during a cycle in the switch is closed. On information and belief, the frequency of control signal LO₂ is substantially similar to the frequency of the RF signal. On information and belief, the control signal (e.g., LO₂) has a sampling aperture with a nominal 25% duty cycle. Accordingly, switch S3 is on for less than one-half cycle of RF.

Claim 26	NXP Wireless Chips
The system of claim 19, wherein the third and fourth control signals each control a charging and discharging cycle of their respective third and fourth energy storage element by respectively controlling the third and fourth switching devices so that for each third and fourth switching device a portion of energy that is distinguishable from noise is transferred to the respective third and fourth storage element when the respective switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective third and fourth switching device when the respective switching device is off.	Each NXP Chip is/includes a system wherein the third and fourth control signals (e.g., LO_2, LO_4 respectively) each control a charging and discharging cycle of their respective energy storage element (e.g., capacitor(s) C3/CF3, capacitor(s) C4/CF4, respectively) by respectively controlling the third and fourth switching devices (e.g., switch S3, switch S4, respectively) so that for each switching device the portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device when the switching device is off. As explained above, the recursive closing/opening of the switch S3 (purple box) periodically couples the RF signal (red box) to a capacitor(s) C3, CF3 (green boxes) according to control signal LO_2 (orange box). During a sampling aperture of control signal LO_2, switch S3 closes and energy from the RF signal is directed to capacitor(s) C3, CF3 along the purple path. Between each sampling aperture of LO_2, switch S3 remains open (i.e., RF signal is prevented from passing through the switch). Accordingly, capacitor(s) C3, CF3 discharges a portion of the transferred energy to a load (e.g., feedback resistor(s), yellow box). Likewise, the recursive closing/opening of the switch S4 (purple box) periodically couples the RF signal (red box) to a capacitor(s) C4, CF4 (green boxes) according to control signal LO_4 (orange box). During a sampling aperture of control signal LO_4, switch S4 closes and energy from the RF signal is directed to capacitor(s) C4, CF4 along the yellow path. Between each sampling aperture of LO_4, switch S4 remains open (i.e., RF signal is prevented from passing through the switch). Accordingly, capacitor(s) C4, CF4 discharges a portion of the transferred energy to a load (e.g., feedback resistor(s), yellow box).

Claim 27	NXP Wireless Chips
The system of claim 26, wherein for each respective energy storage element, the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle.	Each NXP Chip is/includes a system wherein for each respective storage element (e.g., capacitor(s) C3/CF3, capacitor(s) C4/CF4), the energy discharged during any given discharge cycle is not completely discharged, with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle. The third and fourth control signals (e.g., LO_2 and LO_4, respectively) each control a charging and discharging cycle of their respective energy storage element (e.g., capacitor(s) C3/CF3 and capacitor(s) C4/CF4, respectively) by respectively controlling the third and fourth switching devices (e.g., switch S3, switch S4, respectively) so that for each switching device the portion of energy that is distinguishable from noise is transferred to the respective storage element when the switch is on during the charging cycle, and a portion of the transferred energy is discharged during the discharging part of the cycle for each respective switching device when the switching device is off. The third energy storage element (e.g., capacitor(s) C3, CF3) charges when the third switch (switch S3) is closed (“ON”) and partially discharges when the third switch is open (“OFF”). On information and belief, capacitor(s) C3, CF3 does not completely discharge after the charging cycle, which means that there is energy available from the previous charging cycle. Thus, the energy discharged by the third energy storage element during any given discharge cycle is not fully discharged with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle of the third energy storage element. Likewise, the fourth energy storage element (e.g., capacitor(s) C4, CF4) charges when the fourth switch (switch S4) is closed (“ON”) and partially discharges when the fourth switch is open (“OFF”). On information and belief, capacitor(s) C4, CF4 does not completely discharge after the charging cycle, which means that there is energy available from the previous charging cycle. Thus, the energy discharged by the fourth energy storage element during any given discharge cycle is not fully discharged with the remaining undischarged energy from the given discharge cycle becoming an initial condition for the next charging cycle of the fourth energy storage element.

Claim 29	NXP Wireless Chips
The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.	On information and belief, each NXP Chip is/includes a system wherein the frequencies of the third and fourth apertures have periods that are two (2) percent or greater of the modulated carrier signal's (e.g., RF) period. The period of the modulated carrier signal is defined as the amount of time required to complete one full cycle. An aperture describes the pulse width of the control signal (i.e., the length of activation within the signal) when the switch is closed. The diagram below represents an exemplary waveform of an aperture signal (e.g., LO_2, LO_4).  Apertures of the third and fourth control signals (e.g., LO_2, LO_4) possess a time duration or duty cycle with respect to an LO rate. The duty cycle is the percentage of time during a cycle in which the signal is active (switch is closed). On information and belief, the frequency of the control signals is substantially similar to the frequency of the modulated carrier signal (e.g., RF signal). On information and belief, the control signals (e.g., LO_2, LO_4) have a sampling aperture with a nominal 25% duty cycle. Accordingly, the frequencies of the third and fourth apertures have periods that are two (2) percent or greater of the modulated carrier signal's period.

Claim 30	NXP Wireless Chips
The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are five (5) percent or greater of the modulated carrier signal's period.	On information and belief, each NXP Chip is/includes a system wherein the frequencies of the third and fourth apertures have periods that are five (5) percent or greater of the modulated carrier signal's (e.g., RF) period. See claim 29.
Claim 31	NXP Wireless Chips
The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are ten (10) percent or greater of the modulated carrier signal's period.	On information and belief, each NXP Chip is/includes a system wherein the frequencies of the third and fourth apertures have periods that are ten (10) percent or greater of the modulated carrier signal's (e.g., RF) period. See claim 29.
Claim 32	NXP Wireless Chips
The system of claim 19, wherein the frequencies of the third and fourth apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal's period.	On information and belief, each NXP Chip is/includes a system wherein the frequencies of the third and fourth apertures have periods that are twelve and a half (12.5) percent or greater of the modulated carrier signal's (e.g., RF) period. See claim 29.

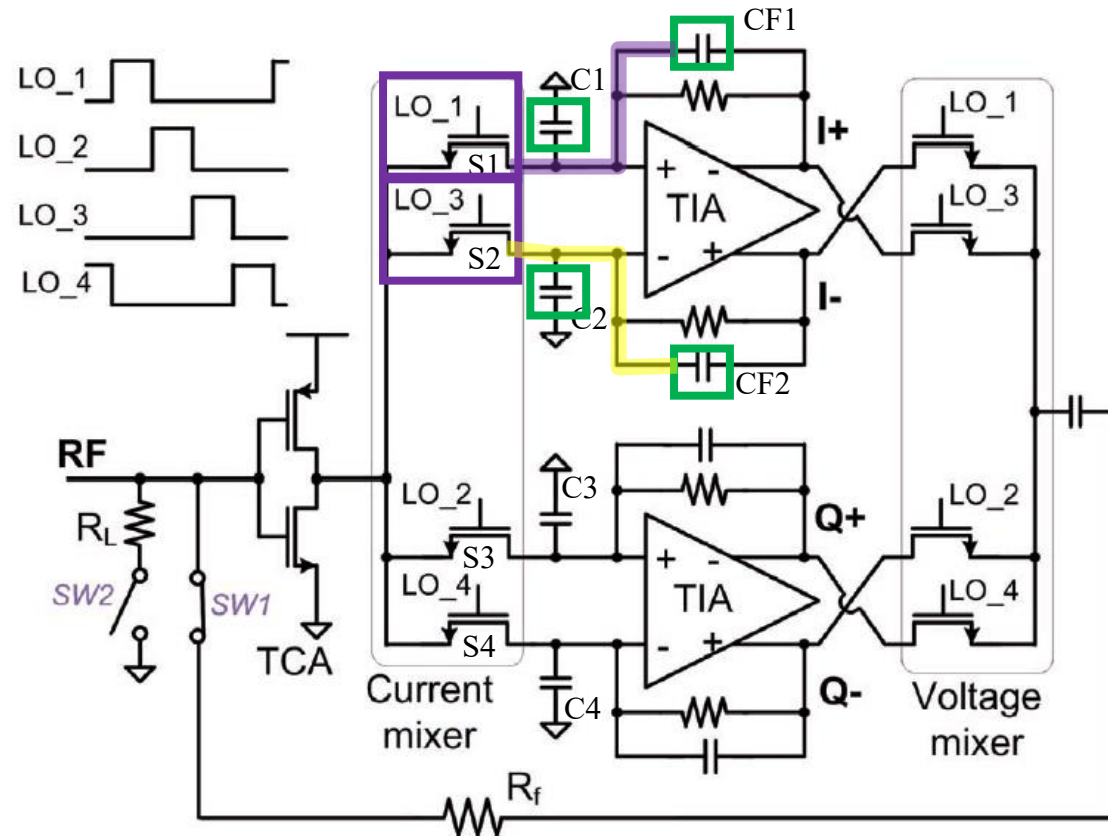
Claim 33	NXP Wireless Chips
The system of claim 19, further comprising: a first filter that filters said down-converted in-phase baseband signal portion; a second filter that filters said down-converted inverted in-phase baseband signal portion; a third filter that filters said down-converted quadrature-phase baseband signal portion; a fourth filter that filters said down-converted inverted quadrature-phase baseband signal portion.	On information and belief, each NXP Chip is/includes a system further comprising: a first filter that filters the down-converted in-phase signal portion (e.g., I+)); and a second filter that filters the down-converted inverted in-phase signal portion (e.g., I-). On information and belief, the first and second filters have the same circuit configuration as the third and fourth filters. As such, on information and belief, each NXP Chip also includes a third filter that filters the down-converted quadrature-phase signal portion (e.g., Q+); and a fourth filter that filters the down-converted inverted quadrature-phase signal portion (e.g., Q-).
Claim 34	NXP Wireless Chips
The system of claim 33, wherein the first, second, third, and fourth filters each comprise a low-pass filter.	On information and belief, each NXP Chip is/includes a system wherein the first, second, third, and fourth filters each comprise a low-pass filter. <i>See claim 33 above.</i>

Claim 35

The system of claim 19, wherein said portions of transferred energy from each of the first, second, third and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by a separate integration module coupled to the output of each said first, second, third and fourth switch respectively.

NXP Wireless Chips

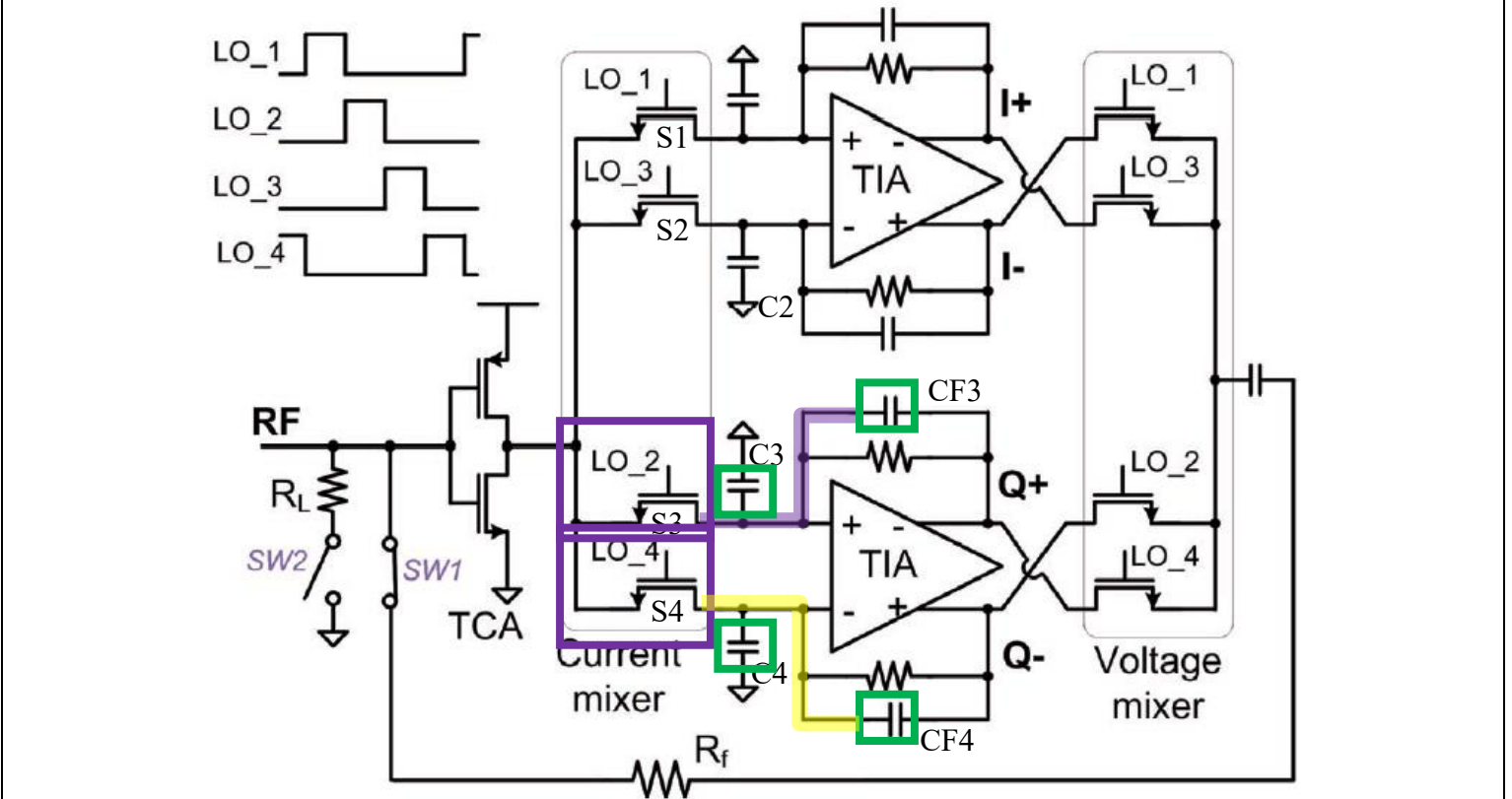
Each NXP Chip is/include a system wherein the portions of transferred energy from each of the first and second switch (e.g., switch S1, switch S2, respectively) which are integrated over time to accumulate the portions of transferred energy are integrated by a separate integration module (e.g., capacitors C1, capacitive feedback CF1, capacitors C2, capacitive feedback CF2, shown in the green boxes) coupled to the output of each the first and second switch.



2011 IEEE paper, Figure 21.5.2.

	The recursive closing/opening of switch S1 (purple box) periodically couples the RF signal to capacitor(s) C1, CF1 (green boxes). During an aperture of LO_1 (orange box), for example, switch S1 (purple box) closes and energy from RF is directed to capacitor(s) C1, CF1 (green boxes) along the purple path. Likewise, the recursive closing/opening of switch S2 (purple box) periodically couples the RF signal to capacitor(s) C2, CF2 (green boxes). During an aperture of LO_3 (orange box), for example, switch S2 (purple box) closes and energy from RF is directed to capacitor(s) C2, CF2 (green boxes) along the yellow path. Accordingly, capacitors C1/CF1, C2/CF2 (green boxes) accumulate portions of transferred energy from each of the first and second switch (switch S1, switch S2, respectively), thereby integrating the portion of transferred energy over time.
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2011 IEEE paper, Figure 21.5.2.

	The recursive closing/opening of switch S3 (purple box) periodically couples the RF signal to capacitor(s) C3, CF3 (green boxes). During an aperture of LO_2 (orange box), for example, switch S3 (purple box) closes and energy from RF is directed to capacitor(s) C3, CF3 (green boxes) along the purple path. Likewise, the recursive closing/opening of switch S4 (purple box) periodically couples the RF signal to capacitor(s) C4, CF4 (green box). During an aperture of LO_4 (orange box), for example, switch S4 (purple box) closes and energy from RF is directed to capacitor(s) C4, CF4 (green boxes) along the yellow path. Accordingly, capacitors C3/CF3, C4/CF4 (green boxes) accumulate portions of transferred energy from each of the third and fourth switch (switch S3, switch S4, respectively), thereby integrating the portion of transferred energy over time.
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Stored Energy

The power delivered to a circuit element is the product of the current and the voltage (provided that the references have the passive configuration):

$$p(t) = v(t)i(t) \quad (3.9)$$

Using Equation 3.3 to substitute for the current, we have

$$p(t) = Cv \frac{dv}{dt} \quad (3.10)$$

Suppose we have a capacitor that initially has $v(t_0) = 0$. Then the initial stored electrical energy is zero, and we say that the capacitor is uncharged. Furthermore, suppose that between time t_0 and some later time t the voltage changes from 0 to $v(t)$ volts. As the voltage magnitude increases, energy is delivered to the capacitor, where it is stored in the electric field between the plates.

If we integrate the power delivered from t_0 to t , we find the energy delivered:

$$w(t) = \int_{t_0}^t p(t) dt \quad (3.11)$$

Using Equation 3.10 to substitute for power, we find that

$$w(t) = \int_{t_0}^t Cv \frac{dv}{dt} dt \quad (3.12)$$

Canceling differential time and changing the limits to the corresponding voltages, we have

$$w(t) = \int_0^{v(t)} Cv dv \quad (3.13)$$

Integrating and evaluating, we get

$$w(t) = \frac{1}{2} Cv^2(t) \quad (3.14)$$

This represents energy stored in the capacitance that can be returned to the circuit.

See Hambley, *Electrical Engineering Principles and Applications*, 6th Ed., Prentice Hall, 2014, p. 129 -130.

Claim 36	NXP Wireless Chips
The system of claim 19, wherein said first, second, third and fourth storage elements are capacitive storage circuits, and wherein said portions of transferred energy from each of the first, second, third and fourth switch which are integrated over time to accumulate said portions of transferred energy are integrated by the capacitive storage circuits of the respective first, second, third and fourth storage elements as they accumulate charge during successive sampling apertures.	Each NXP Chip is/includes a system wherein the first, second, third, and fourth storage elements (e.g., capacitors C1/CF1, C2/CF2, C3/CF3, C4/CF4, respectively) are capacitive storage circuits, and wherein the portions of transferred energy from each of the first, second, third and fourth switch which are integrated over time to accumulate the portions of transferred energy are integrated by the capacitive storage circuits of the respective first, second, third and fourth storage elements as they accumulate charge during successive sampling apertures. See claim 35.