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Networks on Chip

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Editors: [Axel Jantsch](#), [Hannu Tenhunen](#)

6517 Accesses | 492 Citations | 3 Altmetric

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About this book

As the number of processor cores and IP blocks integrated on a single chip is steadily growing, a systematic approach to design the communication infrastructure becomes necessary. Different variants of packed switched on-chip networks have been proposed by several groups during the past two years. This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces. It also provides a guideline and vision about the direction this field is moving to. Moreover, the book outlines the consequences of adopting design platforms based on packet switched network. The consequences may in fact be far reaching because many of the topics of distributed systems, distributed real-time systems, fault tolerant systems, parallel computer architecture, parallel programming as well as traditional system-on-chip issues will appear relevant but within the constraints of a single chip VLSI implementation.

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Keywords

VLSI **architecture** **computer** **computer architecture**

distributed systems **operating system** **processor**

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Reviews

From the reviews:

"This edited book is concerned with the fundamentals of Networks-on-Chip design. ... Overall, the various authors have done an excellent job in covering their material, and the book is well edited. The authors' objectives were that of providing an in-depth, up-to-date, unified and comprehensive treatment These are difficult objectives ... and they have done a creditable job of attaining them. In summary, this book is a welcome addition to the literature on networks on chip design" (Mile Stojcev, Microelectronics Reliability, Vol. 44, 2004)

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Editors and Affiliations

Royal Institute of Technology, Stockholm

Axel Jantsch, Hannu Tenhunen

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Bibliographic Information

Book Title

Networks on Chip

EditorsAxel Jantsch, Hannu
Tenhunen**DOI**<https://doi.org/10.1007/b105353>**Publisher**

Springer New York, NY

eBook Packages[Springer Book Archive](#)**Copyright Information**Springer Science+Business
Media New York 2003**Hardcover ISBN**

978-1-4020-7392-2

Published: 31 January 2003

Softcover ISBN

978-1-4419-5344-5

Published: 05 November
2010**eBook ISBN**

978-0-306-48727-9

Published: 08 May 2007

Edition Number

1

Number of Pages

VIII, 303

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Implementation, Processor
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Aided Engineering \(CAD,
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