ERIK CHMELAR

(650) 533-7952 | echmelar@yahoo.com

Subject matter expert in semiconductor hardware and software with over two decades of experience developing, implementing, and protecting advanced technologies including digital and mixed-signal systems, high-speed serial communications, 5G/wireless telecommunications, and smart medical devices.

CREDENTIALS

EDUCATION —

- **JD, Intellectual Property**, Univ. Michigan Law School, Ann Arbor, MI 2015-2017
- **MBA, Management**, Western Michigan Univ., Kalamazoo, MI 2012-2013
- **BS, Chemical Physics**, Saginaw Valley State Univ., University Center, MI 2008-2011
- **PhD, Electrical Engineering**, Stanford Univ., Stanford, CA 2002-2004
  Dissertation: "Test and Diagnosis of Field-programmable Gate Arrays."
- **MS, Electrical Engineering**, Stanford Univ., Stanford, CA 2000-2001
- **BS, Electrical Engineering**, Michigan Technological Univ., Houghton, MI 1997-2000

LICENSES AND CERTIFICATIONS —

- **Agile Certified Practitioner** (PMI-ACP, PMI) 2015-pres.
- **Certified Project Management Professional** (PMP, PMI) 2014-pres.
- **Licensed Professional Engineer** (PE, State of Michigan LARA) 2010-pres.
- **Licensed Patent Agent/Attorney** (State Bar of Michigan, USPTO) 2007-pres.

EXPERIENCE

Technical Expert, **Semiconductor Hardware/Software**, Midland, MI 08/2007-pres.

- Serve as a technical expert witness for litigation in court and inter partes review (IPRs)
- Mine and analyze patent portfolios and develop assertion strategies for non-practicing entities (NPEs)
- Recent technology areas include memory, programmable hardware, microcontrollers, and AI devices

Senior Counsel, Young Basile Hanlon & MacFarlane, PC, Troy, MI 06/2023-pres.

- Draft and prosecute patent applications in a variety of semiconductor, software, and related arts
- Draft legal opinions for non-infringement, invalidity, and freedom-to-operate (FTO)
- Interview inventors, harvest inventions, and manage patent portfolios

Senior Associate, Dilworth IP, New Haven, CT 10/2020-06/2023

- Drafted and prosecuted patent applications in a variety of semiconductor, software, and related arts
- Drafted legal opinions for non-infringement, invalidity, freedom-to-operate (FTO), and export controls
- Interview inventors, harvest inventions, manage patent portfolios, and create technology landscapes

Senior Associate, Murphy, Bilak & Homiller, PLLC., Cary, NC 01/2020-06/2020

- Prosecuted patent applications for industry-leading wireless and semiconductor corporations
- Drafted approx. 100 office-action responses for complex 5G technologies
- Routinely referenced ETSI 3GPP specifications for prosecution of standard essential patents (SEPs)

Senior Manager, Innovation Partners, InterDigital, Inc., Wilmington, DE 09/2015-10/2018

- Created patent portfolios for 5G, IoT, connected/autonomous vehicles, and augmented/virtual reality
- Managed scientists and engineers to create over 100 new invention disclosures / patent applications
- Forged research partnerships with commercial and academic organizations to develop patent portfolios

Co-founder, Managing Member, Dera Industries LLC., Midland, MI 05/2016-07/2017
- Developed and productized the award-winning One-Tie™ re-usable tie strap consumer product
- Achieved $1 million in annual sales prior to licensing the intellectual property

Senior Principal Engineer, Adv. Dev., Stryker Corp., Kalamazoo, MI 02/2012-03/2015
- Supervised R&D of disruptive medical instruments and surgical technologies
- Formalized new business opportunities, developed budgets and timelines, and staffed project teams
- Collaborated with several top-tier universities to bring necessary expertise into the organization
- Delivered working prototypes for biophotonic devices and boundary-constraint surgical robotics

Staff SW Engineer, Adv. Tech. Dev., LSI Corp. (Broadcom)**,** Milpitas, CA 07/2004-01/2012
- Conducted R&D for very large scale integrated (VLSI) and serializer-deserializer (SerDes) circuits
- Granted approx. 20 patents for physical (PHY) interfaces, SerDes, and VLSI test architectures
- Made cutting-edge contributions in SerDes and test that were implemented in customer designs

Adjunct Professor, ECE Dept., SVSU, University Center, MI 01/2009-01/2012
- Taught courses in digital circuits, computer architecture and organization, and data communications

Consulting Assistant Professor, EE/CS Dept., Stanford University, Stanford, CA 09/2006-08/2008
- Advised PhD students on the test and reliability of VLSI circuits
- Created and taught a PhD-level course on clock and data recovery (CDR) for digital communications

Product Test Engineer, Xilinx, Inc., Los Gatos, CA (PhD. Intern, two summers) 06/2002-09/2003
- Engineered tools to detect and diagnose defects in FPGAs, which reduced diagnosis time by 75%

Manufacturing Engineer, Cisco Systems, Inc., San Jose, CA 11/1999-04/2002
- Oversaw functional testing of layer-2/3 network switches and determined root-cause failures

SERVICE AND MENTORING

Admissions Representative, Univ. Michigan Law School, Ann Arbor, MI 2018
- Advised prospective law students at 30 law fairs and forums

Instructor, National Science Foundation, Western Michigan Univ. I-Corps, Kalamazoo, MI 2015
- Taught Lean Startup and Business Canvas fundamentals to a cohort of 30 entrepreneurs

Engineering Program Evaluator, Accred. Board of Eng. & Tech. (ABET), Baltimore, MD 2013-2014
- Evaluated electrical engineering and computer engineering university educational programs

Industry Mentor, National Science Foundation, Univ. Michigan I-Corps, Ann Arbor, MI 2013
- Mentored teams of medical-device entrepreneurs participating in the I-Corps program

Industry Mentor, Western Michigan Univ., Starting Gate Accelerator, Kalamazoo, MI 2013
- Mentored entrepreneurs participating in the university startup-accelerator program

SELECT PROFICIENCIES

- Hardware – Verilog, VHDL, ASICs, FPGAs
- Engineering – COMSOL, ANSYS
- Software – C/C++, Perl, Java, MatLab
- CAD – SolidWorks, AutoCAD, Blender

Select US Patents

US11446109B2, “Metal detection system for use with medical waste container,” issued 2022-09-23.

US11389556B2, “Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized,” issued 2022-07-19.

US11357877B2, “Sterilization enclosure for surgical instruments,” issued 2022-06-14.

US11225996B1, “Dual hook clasp,” issued 2022-01-18.

US11002308B2, “Hook device with opposing jaws,” issued 2021-05-11.

US11000341B2, “Metal detection system for use with medical waste container,” issued 2021-05-11.

US10994906B2, “Easy-to-remove cable tie,” issued 2021-05-04.

US10731698B2, “Hook device with rotatable opposing jaws,” issued 2020-08-04.

US10604317B2, “Reusable tie strap with multiple apertures,” issued 2020-03-31.

US10258706B2, “Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized,” issued 2019-04-16.

US10010636B2, “Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized,” issued 2018-07-03.

US9292644B2, “Row based analog standard cell layout design and methodology,” issued 2016-03-22.

US9087157B2, “Low-loss transmission line TDM communication link and system,” issued 2015-07-21.

US9014313B2, “Error signature analysis for data and clock recovery in a communication system,” issued 2015-04-21.

US8982941B2, “Predictive selection in a fully unrolled decision feedback equalizer,” issued 2015-03-17.

US8929497B2, “Dynamic deskew for bang-bang timing recovery in a communication system,” issued 2015-01-06.

US8923382B2, “Tap adaptation with a fully unrolled decision feedback equalizer,” issued 2014-12-30.

US8615062B2, “Adaptation using error signature analysis in a communication system,” issued 2013-12-24.

US8527912B2, “Digitally obtaining contours of fabricated polygons,” issued 2013-09-03.

US8432250B2, “Process variation based microchip identification,” issued 2013-04-30.

US8121186B2, “Systems and methods for speculative signal equalization,” issued 2012-02-21.

US7956790B2, “Systems and methods for synchronous, retimed analog to digital conversion,” issued 2011-07-05.

US7973692B2, “Systems and methods for synchronous, retimed analog to digital conversion,” issued 2011-06-07.

US7779320B2, “Low power scan shifting with random-like test patterns,” issued 2010-08-17.

US7696915B2, “Analog-to-digital converter having reduced number of activated comparators,” issued 2010-04-13.

US7656340B2, “Systems and methods for pipelined analog to digital conversion,” issued 2010-02-02.

US7656339B2, “Systems and methods for analog to digital conversion,” issued 2010-02-02.

US7328386B2, “Methods for using checksums in X-tolerant test response compaction in scan-based testing of integrated circuits,” issued 2008-02-05.

US7293312B2, “Multipurpose skateboard tool,” issued 2007-11-13.

US7210083B2, “System and method for implementing postponed quasi-masking test output compression in integrated circuit,” issued 2007-04-24.

US7206983B2, “Segmented addressable scan architecture and method for implementing scan-based testing of integrated circuits,” issued 2007-04-17.

US7093842B2, “Skateboard truck assembly, “issued 2006-08-22.

US6979142B1, “Retractable tip mechanical pencil assembly,” issued 2005-12-27.

US6920621B1, “Methods of testing for shorts in programmable logic devices using relative quiescent current measurements,” issued 2005-07-19.

Select Publications

E. Chmelar, "Error signature analysis (ESA) receiver architecture for data communication," DesignCon, 2012.

E. Chmelar and C. Ito, "Mostly digital SerDes (MDS): a comprehensive low power receiver architecture," DesignCon, 2012.

I. Park, D. Lee, E. Chmelar, and E. McCluskey, "Inconsistent fails due to limited tester timing accuracy," Proc. 26th VLSI Test Symp., 2008.

A. Al-Yamani, N. Devta-Prasanna, E. Chmelar, M. Grinchuk, and A. Gunda, "Scan test cost and power reduction through systematic scan reconfiguration," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 26, pp. 907–918, 2007.

A. Al-Yamani, E. Chmelar, and M. Grinchuk, "Segmented addressable scan architecture," Proc. 23rd VLSI Test Symp., 2005.

E. Chmelar, "Minimizing the number of test configurations for FPGAs," Int. Conf. Computer Aided Design, 2004.

E. Chmelar, "The test and diagnosis of FPGAs," Ph.D. thesis, Stanford University, 2004.

E. Chmelar and S. Toutounchi, "FPGA bridging fault detection and location via differential IDDQ," Proc. 22nd VLSI Test Symp., 2004.

E. Chmelar, "Subframe multiplexing: FPGA manufacturing test time reduction," CRC TR-04-01, 2004.

E. Chmelar, "Subframe multiplexing for FPGA manufacturing test," Proc. Int. Symp. FPGAs, 2004.

E. Chmelar, "FPGA interconnect delay fault testing," Proc. Int. Test Conf., pp. 1239–1247, 2003.

Select Professional Organizations

State Bar of Michigan
Member (2018-pres.)

Project Management Institute
Certified Agile Practitioner (2014-pres.)
Certified Project Management Professional (2015-pres.)

Association for Computing Machinery
Member (2018-2019)

Accreditation Board of Engineering and Technology
Program Evaluator (2013-2018)

Institute of Electrical & Electronic Engineers
Senior Member (2004-2018)

American Chemical Society
Member (2013-2016)

National Science Foundation I-Corps
Instructor (2015)
Industry Mentor (2013)

American Society of Mechanical Engineers
Member (2014-2015)

International Society of Optics & Photonics
Member (2015)