IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

NETWORK SYSTEM TECHNOLOGIES, LLC,	)	
	)	
Plaintiff,	)	
	)	
v.	)	Civil Action No. 1:22-cv-1331-DAE
	)	
QUALCOMM INCORPORATED;	)	
QUALCOMM TECHNOLOGIES, INC.;	)	
ARTERIS, INC.,	)	
	)	
Defendants.	)	

NETWORK SYSTEM TECHNOLOGIES, LLC'S RESPONSE TO DEFENDANTS' JOINT OPENING CLAIM CONSTRUCTION BRIEF

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I. Introduction

Pursuant to the Court's Amended Scheduling Order (Dkt. 80), Plaintiff Network System Technologies, LLC ("NST") respectfully submits this brief in response to Qualcomm, Inc.'s, Qualcomm Technologies, Inc.'s and Arteris, Inc.'s (hereinafter "Defendants") Joint Opening Claim Construction Brief (Dkt. 77, hereinafter "Br.").

Through its proposed constructions, Defendants seek to unduly and unfairly limit the scope of the disputed claim terms by: 1) improperly importing limitations from the patent specifications, a "cardinal sin" of patent law; 2) seeking to construe plainly structural claim terms under 35 U.S.C. § 112, ¶ 6; or 3) limiting the claims based on alleged prosecution history disclaimers that are far from the "clear and unmistakable" threshold required by the law and are, in fact, nonexistent. NST's constructions, on the other hand, faithfully hew to the language of the claims and the patent specifications, which are the primary sources of claim construction evidence.

Defendants' proposed constructions should be rejected in favor of NST's constructions, as demonstrated below.

II. Brief Technical Background[1]

The Asserted Patents—U.S. 7,366,818 ("'818 Patent," attached hereto as Exhibit 1); U.S. 7,373,449 ("'449 Patent," Exhibit 2); U.S. 7,594,052 ("'052 Patent," Exhibit 3); U.S. 7,769,893 ("'9893 Patent," Exhibit 4); U.S. 8,072,893 ("'2893 Patent," Exhibit 5); and U.S. 8,086,800 ("'800 Patent," Exhibit 6)—all generally relate to integrated circuits having a plurality of circuitry modules that are communicatively interconnected via network-on-chip ("NoC") interconnects.

System-on-chip ("SoC") technology is widely used in consumer electronics and computing

[1] NST respectfully directs the Court to its forthcoming Technical Tutorial, to be served on December 18, 2023, (*see* Dkt. 80), for further background of the technology and the Asserted Patents.

devices, including smartphones, laptops, and embedded systems such as vehicle infotainment and advanced driver assistance systems. Dkt. 57 ¶ 204. As the adoption of SoCs in electronic devices grew over time, and as microchip manufacturing technology advanced, more processing cores and other circuitry modules were incorporated into SoCs. *Id.* ¶ 205. In early SoC designs, these circuitry modules were directly connected, first by point-to-point interconnects, and later by shared buses, both of which resulted in large SoCs with poor interconnect efficiency. *Id.*; *see also* Declaration of Dr. Erik Chmelar ("Chmelar Decl." attached hereto as Exhibit 7), ¶¶ 29-32. Though more efficient than point-to-point interconnects, buses suffered from a critical limitation insofar as only one module can send data to the bus at a time and the others must wait their turn. '818 Patent at 1:33-34. Thus, as the number of circuitry modules increased, buses became a bottleneck limiting the number of circuitry modules that could be practicably interconnected—and therefore, limited the potential power and capability of SoCs. *Id*.

To eliminate this bottleneck, the inventors of the Asserted Patents at Philips Semiconductor developed advanced network-on-chip ("NoC") technologies. An NoC is a substantially different interconnection paradigm for on-chip communication that leverages certain aspects of traditional computer networks, such as network interfaces for connecting modules to an on-chip network, packetized data for breaking messages up into smaller units for transmission by the on-chip network, and routers for switching of data packets along various routes. Chmelar Decl. ¶¶ 32. In an NoC, a message transmitted from one module to another may be divided into smaller packets by a network interface and those packets may travel across the NoC using different routes determined by the routers in the NoC. *Id.* Each interconnection between routers may be called a "hop," such that the NoC is a "multi-hop" interconnection between modules separated by routers, or network nodes. *Id.* ¶¶ 32, 34. Accordingly, an NoC is an "indirect" interconnection between

modules. *Id.* ¶¶ 135, 143. This is distinctly different from a shared bus, where data transmitted from one module to another always takes the same route, and is therefore a "direct" interconnection between modules. *Id.* ¶ 29, 32.

Besides overcoming the bottleneck of shared buses, NoCs have other advantages over prior, direct, interconnections. Because NoCs can utilize interconnects more efficiently than shared buses, fewer interconnects are required. *Id.* ¶¶ 32-36. This reduces the area and power consumption of the on-chip interconnects of an SoC compared to shared buses. *Id.* ¶¶ 82, 110, 195. Additionally, by moving the communications logic of a circuitry module to a dedicated network interface that connects the module to the NoC, the modules can be simpler and more modular, which enables even higher levels of integration at lower design costs. '818 Patent at 1:67–2:16;'449 Patent at 1:66–2:15; '052 Patent at 1:64–2:12; '9893 Patent at 1:65–2:11; '800 Patent at 1:64–2:2.

Although NoCs leverage certain aspects of traditional computer networks, the on-chip environment of NoCs introduces several constraints and challenges not present in the off-chip environment. '818 Patent at 1:62-2:6. For example, there is substantially less memory and computational resources in the on-chip environment that can be dedicated to network processing. *Id.* at 2:44-50, 3:7-22, 3:31-35. The Asserted Patents address these challenges.

III. <u>Legal Standard</u>

A. Plain and Ordinary Meaning

The "words of a claim" are understood according to their plain and ordinary meaning in the context of the surrounding claim limitations, the specification, and the prosecution history. *Thorner v. Sony Computer Entertainment America LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). However, "we must look at the ordinary meaning in the context of the written description and the prosecution history," since importing limitations is one of the "cardinal sins of patent law." *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005).

The "words of a claim" are not given their plain meaning only when the patentee "acts as his own lexicographer" or "disavows the full scope of a claim term either in the specification or during prosecution." *Thorner*, 669 F.3d at 1365. The standard for lexicography is exacting. *Id.* at 1365-67. "To act as its own lexicographer, a patentee must clearly set forth a definition of the disputed claim term other than its plain and ordinary meaning," and occurs only when the patentee explicitly discloses that a term "means" a particular definition or "is defined." *Id*. The "standard for disavowal of claim scope is similarly exacting." *Id*. The intrinsic evidence must provide "expressions of manifest exclusion or restriction," clarifying that the invention does not include a particular feature. *Id*. "Where the alleged disavowal is ambiguous," courts do not apply the doctrine of prosecution history disclaimer. *Avid Tech., Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1045 (Fed. Cir. 2016).

B. Means-Plus-Function

"In determining whether a claim term invokes § 112, ¶ 6, the essential inquiry is not merely the presence or absence of the word 'means' but whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Skky, Inc. v. MindGeek s.a.r.l.*, 859 F.3d 1014, 1019 (Fed. Cir 2017) (internal quotations and citations omitted). While the word "means" triggers a presumption that § 112, ¶ 6 applies, this can be rebutted by a preponderance of the evidence when "consider[ing] the limitations as a whole" according to the "understanding of one of ordinary skill in the art." *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1374 (Fed. Cir. 2003) (internal quotations, citations, and modifications omitted). "[W]hen a claim uses the term 'means,' the focus is on whether the claim term recites no function corresponding to the means or recites sufficient structure or material for performing that function." *Id*. at 1372 (internal quotations omitted). To further "hold that a claim containing a means-plus-function limitation lacks a disclosure of structure" "requires [an additional] finding,

by clear and convincing evidence, that the specification lacks disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the recited function." *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376-77 (Fed. Cir. 2001).

C. Definiteness

Definiteness is evaluated from the perspective of someone "skilled in the relevant art." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 909 (2014). "[T]he certainty which the law requires in patents is not greater than is reasonable, having regard to their subject-matter." *Id*. at 910 (quoting *Minerals Separation, Ltd. v. Hyde*, 242 U.S. 261, 270 (1916)). Terms of degree are not "inherently indefinite," and "absolute or mathematical precision is not required." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014).

Indefiniteness requires a showing of "clear and convincing evidence that a skilled artisan could not discern the boundaries of the claim based on the claim language, the specification, and the prosecution history, as well as her knowledge of the relevant art area." *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249-50 (Fed. Cir. 2008); 35 U.S.C. § 282.

IV. Level of Ordinary Skill in the Art

NST's expert, Dr. Chmelar, opines that a person of ordinary skill in the art ("POSITA") at the time of the invention of the Asserted Patents is an individual having at least: a Bachelor of Science (or equivalent) degree in electrical engineering, computer engineering, or a related field, and 2-3 years of work experience in very large-scale integrated ("VLSI") systems, such as application-specific integrated circuits ("ASICs"), application-specific standard parts ("ASSPs"), system-on-chip ("SoC"), or field-programmable gate arrays ("FPGAs"), and has an understanding of on-chip interconnection networks. Chmelar Decl. ¶ 26.

Defendants' expert, Dr. Hassoun, posits an even higher skill level: at least either a Master's degree in Electrical Engineering, or related field, as well as at least three years of work experience

in the field of SoC design, or a Bachelor's degree in Electrical Engineering, or related field, as well as at least five years of work experience in the field of SoC design.

Neither expert has opined that this discrepancy would have an impact on their conclusions as to the constructions of the various terms.

V. Disputed Terms

A. Common Term – "connection"

Claim Term	NST's Construction	Defendants' Construction
"connection" '818 Patent, Claim 1 '449 Patent, Claims 10, 13-16 '052 Patent, Claim 6 '9893 Patent, Claims 4-10 '800 Patent, Claim 12	"one or more communication channels"	"one or more channels, each having a set of connection properties, between a first module and at least one second module, that are created before use and closed after use"

Consistent with the Parties' agreement that "connection" should be afforded the same meaning across all five patents containing the term, NST's construction as "one or more communication channels" reflects the understanding of a POSITA in light of the specifications of all five patents. Chmelar Decl. ¶ 53. Defendants' construction, on the other hand, improperly seeks to import an additional *functional* limitation that the connections "are created before use and closed after use," which is neither required by the claims nor mentioned in any patent's specification.[2] *Id.* ¶ 54. Importing limitations from a patent's specification is prohibited; importing them from *another* patent's specification is unheard of. Defendants' construction must be rejected.

Instead, NST's proposed construction of "connection" as "one or more communication

[2] As Defendants acknowledge, the sole specification passage they rely upon for the "created before use and closed after use" portion of their construction is only present in three of the patents with a "substantively identical statement" in the fourth. (Br. at 7, n.5.) Implicit is an admission that there is no such statement in the fifth patent containing the term "connection." *See id.*; *see also* Chmelar Decl. ¶ 54 (discussing '800 Patent's lack of support for Defendants' additional limitations).

channels" is supported by the specifications of *all five* Asserted Patents containing the term. Chmelar Decl. ¶ 53 (citing ʾ818 Patent at 6:36-38; ʾ449 Patent at 8:17-18; ʾ052 Patent at 4:53-55; ʾ9893 Patent at 4:56-58; ʾ800 Patent at 5:16-18).[3] In light of this intrinsic evidence, a POSITA would understand that "connection" means "one or more communication channels." *Id.* ¶¶ 52-53.

Defendants' proposed construction imports functional limitations that are not found in the claims. While the specifications for *a subset of* the Asserted Patents indicate that connections may be created or closed,[4] the claims themselves do not recite these additional *functional* steps. *Id.* ¶¶ 53-54; ʾ818 Patent, Claims 1-3, 5-7; ʾ449 Patent, Claims 10-16; ʾ052 Patent, Claim 6; ʾ9893 Patent, Claims 4-11; ʾ800 Patent, Claim 12. It is well-settled that "the *claims*, not the written description, [] define the scope of the patent right." *Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1347 (Fed. Cir. 1998) (emphasis in original); *AllVoice Computing PLC v. Nuance Comms., Inc.*, 504 F.3d 1236, 1248 (Fed. Cir. 2007) ("every claim need not contain every feature taught in the specification"). Of the patents that contain the term "connection," only Claim 10 of the '449 Patent includes a limitation related to the establishment of a connection: "the target connection between the first and second module being established based on the available properties of said

[3] Each of these cited passages make clear that the "communication channels" included in NST's construction require "connection properties" (which are an agreed term, *see* Brief at 6). *See* Chmelar Decl. ¶¶ 38-39. Thus, Defendants' strawman attack on NST's construction, asserting that it "requires nothing more than a wire," fails. *Id.* ¶¶ 38-39; *see also id.* ¶¶ 57-58 (explaining communication channels). Defendants' attack on NST's construction also incorrectly conflate "connection-based" with "connection." *Id.* ¶¶ 55-56. As Dr. Chmelar explains, and as the intrinsic record confirms, a system can use "connections" without being "connection based." *Id.*

[4] As Defendants concede, the specification passages that indicate the that connections ***may*** (rather than "must") be opened or closed. Opening Br. at 8-9 (citing ʾ449 Patent at 7:64-65 ("a connection requiring some properties ***is opened or not*** depending on the availability of these resources"); ʾ449 Patent at 10:55-61 ("the communication manger CM issues a request to said resource manager RM to reset the connection ***or the connection properties***); ʾ449 Patent at 6:63-7:1 ("[t]o avoid buffer overflow connections ***can*** be used); ʾ449 Patent at 16:32-45 ("[a] connection ***could be opened*** as follows"); ʾ9893 Patent at 9:56-60 ("[c]onnections ***can*** be configured independently").

communication channels of said connection." '449 Patent, Claim 10. But this limitation says nothing of Defendants' proposed construction that the connection be "created before use and closed after use." If the inventors intended to limit the claims in this manner, they would have added language to that effect. Intentional omission of language must be given effect; claims cannot be rewritten to add unrecited limitations. *Thorner*, 669 F.3d at 1366 ("We do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that.").

It is a fundamental error of claim construction to import limitations from the specification into the claims. *CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1231 (Fed. Cir. 2005) ("[i]n examining the specification for proper context, however, this court will not at any time import limitations from the specification into the claims"); *King Pharms., Inc. v. Eon Labs, Inc.*, 616 F.3d 1267, 1275 (Fed. Cir. 2010) ("[i]t would be improper to limit the broad terms used in the […] patent's claims to the specific […] conditions disclosed in the written description.").

Even worse, Defendants' proposed construction impermissibly imports a ***functional* limitation** into a ***structural* term**, "connection." However, the law is clear that "[a]n invention claimed in purely structural terms generally resists functional limitation." *Toro Co. v. White Cons. Indus., Inc.*, 266 F.3d 1367, 1371 (Fed. Cir. 2001); *see also Ecolab v. Envirochem,* 264 F.3d 1358, 1367 (Fed. Cir. 2001) ("Where the function is not recited in the claim itself by the patentee, we do not import such a limitation."); *Jeneric/Pentron Inc. v. Dillon Co.,* 205 F.3d 1377, 1382, 54 USPQ2d 1086, 1090 (Fed. Cir. 2000); *Transmatic, Inc. v. Gulton Indus.,* 53 F.3d 1270, 1278, 35 USPQ2d 1035, 1041 (Fed. Cir. 1995) (holding that the district court erred by importing functional limitations into a structural claim element because functions that are not recited in a claim are not legally relevant to the literal language of the claim).

Because Defendants' proposed construction improperly imports unwarranted functional

limitations into the claims, NST's construction should be adopted.

B. '818 Patent Term – "dropping means . . . "

Claim Term	NST's Construction	Defendants' Construction
"dropping means (DM) for dropping data exchanged by said first and second module (M, S) / a first dropping means (DM) for dropping data / said dropping means (DM)" '818 Patent, Claim 1	"dropping means" means "circuit configured to drop messages," the remaining language should be afforded their plain and ordinary meaning (not subject to §112 ¶ 6). If the Court holds that §112 ¶ 6 applies, NST proposes: **Function (claim 1)**: "drop data exchanged by said first and second module" **Function (claim 3)**: claim 1 function + "create an error message if data is dropped" **Function (claim 5)**: claim 3 function + "send said error message to said first module" **Structure**: "circuit"	"dropping means" subject to §112 ¶ 6. **Function (claim 1)**: "dropping data exchanged by said first and second module (M, S)" **Function (claim 3)**: claim 1 function + "creating an error message if data is dropped" **Function (claim 5)**: claim 3 function + "sending said error message to said first module (M)" **Structure**: Indefinite (no structure disclosed)

A POSITA understands that the "dropping means" in the '818 Patent is a "circuit configured to drop messages [or data],"[5] which as a "circuit" is sufficiently structural in the field of integrated circuitry to overcome any §112 ¶ 6 presumption. Chmelar Decl. ¶ 63. However, if the Court determines § 112 ¶ 6 applies, then the structure disclosed in the specification is a "circuit," namely, a "circuit configured to drop messages [or data, *see* footnote 6, *supra*]." *Id.* ¶ 72.

Though the word "means" creates a presumption that a term should be interpreted under § 112 ¶ 6, this is rebutted where the phrase describes structure. *Skky, Inc.*, 859 F.3d at 1019 (finding "'wireless device means' does not invoke 112 ¶ 6 because its clause recites sufficient structure").

[5] Defendants take issue with NST's construction as reciting "dropping messages" rather than "dropping data." (Br. at n.6.) While NST believes its original construction is correct, to remove a point of dispute, NST is willing to adapt its construction to: "a circuit configured to drop data."

Here, a POSITA understands that the "dropping means" is sufficiently structural to overcome that presumption in the field of integrated circuitry. *See* Chmelar Decl. ¶ 72.

The preamble of claim 1, which the Parties agree is a claim limitation, (*see* Br. at 5), recites that the "dropping means" is a constituent of an "integrated circuit." '818 Patent at 12:5-9. The Parties have stipulated that "integrated circuit" means "interconnected circuitry on a chip." (*See* Br. at 6.) This interconnected circuitry is a physical structure with millions (even billions) of microscopic transistors, logic gates, flip-flops, multiplexers, and other circuitry elements that interact with electrons representing data as they move through the chip. Chmelar Decl. ¶¶ 63-69. The "integrated circuit" of claim 1 of the '818 Patent includes hardware "network on chip" ("NoC") circuitry having physical network interfaces called "interface means (ANIP, PNIP)" that include physical "dropping means (DM)" in them. '818 Patent at 12:10-23;[6] *see also id.* at 5:27-28, 5:37-41 ("integrated circuit comprising at least one interface means" that "comprises a first dropping means"). These physical hardware structures are shown schematically in Figure 2 of the '818 Patent. In one embodiment, the hardware "dropping means (DM)" (aka, "dropping manager (DM)")[7] is physically located within the hardware network interface. '818 Patent at 7:45-54. In other embodiments, "the dropping means as described above may be implemented in some of the routers of the network, so that these routers are allowed to drop data." *Id*. at 11:23-25.

Notably, Defendants do not argue that "interface means (ANIP, PNIP)," which is also

[6] All emphasis herein added unless noted otherwise.

[7] The specification of the '818 Patent uses the terms "dropping means (DM)" and "dropping manager (DM)" interchangeably and defines both with the acronym "DM." *See*, *e.g.*, '818 Patent at 5:21-30, 7:48-50. Such interchangeable use equates the two terms by definition. *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1329 (Fed. Cir. 2009) ("the specification consistently uses the words 'graft' and 'intraluminal graft' interchangeably. It states that 'an intraluminal graft as defined above' is carried through a catheter 'until the graft extends into the vessel.' . . . The interchangeable use of the two terms is akin to a definition equating the two").

recited as a constituent of Claim 1's "integrated circuit" and is the part of that overall circuit that contains the "dropping means," is either governed by § 112 ¶ 6 or indefinite. Thus, the dropping means/manager (as well as the non-disputed "interface means") are disclosed as physical hardware structures with defined locations in the overall hardware structure.

According to Dr. Chmelar, the NoC circuitry is application-specific; its purpose is to physically move electrons, representing data, across the chip. Chmelar Decl. ¶ 70. This movement of data is determined by the physical interaction of electrons with microscopic circuitry elements. *Id.* ¶ 69 The NoC is purpose-built machinery that physically moves data according to its physical structures; it does not execute software or instructions (in contrast to, for example, the "master (M)" disclosed in the '818 Patent, which may be a microprocessor that executes software). *Id.* ¶ 70. Nowhere does the '818 Patent disclose that either the NoC circuitry, or the dropping means contained therein, are implemented in software, firmware, or in anything other than physical hardware structures of the integrated circuit. *Id.* Rather, in a passage immediately preceding Claim 1, the specification reads: "[i]n the device claim enumerating several **means**, several of ***these means* can be embodied by one and the same item of *hardware***," where hardware in this context means physical circuitry. '818 Patent at 11:41-43; Chmelar Decl. ¶ 66.

Thus, a POSITA knowledgeable of the integrated circuitry field appreciates that the '818 Patent's disclosure of a "dropping means" sufficiently describes structure in the form of an arrangement of microscopic circuitry physically located within the NoC network interfaces that is configured to drop messages or data. For this reason, §112 ¶ 6 does not apply. *Id.* ¶ 71.

This conclusion is supported by the Federal Circuit's recognition that "[w]e have previously held on several occasions that the term 'circuit' connotes structure." *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1364 (Fed. Cir. 2013); *see*

also Linear Tech. Corp. v. Impala Linear Corp., 379 F.3d 1311, 1320-21 (Fed. Cir. 2004) (holding that the term "circuit" is not a means-plus-function limitation when the patent provides "a recitation of the respective circuit's operation in sufficient detail to suggest structure to persons of ordinary skill in the art").[8]

Defendants contend that "dropping means" is indefinite and offer no construction for the § 112 ¶ 6 structure.[9] Br. at 12. Defendants' burden to demonstrate indefiniteness is high: they must show "by clear and convincing evidence that a skilled artisan could not discern the boundaries of the claim based on the claim language, the specification, and the prosecution history, as well as her knowledge of the relevant art area." *Halliburton*, 514 F.3d at 1249-50; 35 U.S.C. § 282.

Rather than meet this exacting standard, Defendants ignore the disclosures of the '818 Patent and feign ignorance as to the knowledge of a POSITA familiar with integrated circuitry. As shown above, the '818 Patent unambiguously links and discloses the structure of the "dropping means" as a hardware "integrated circuit" (indeed, "circuit" or "integrated circuit" appear roughly 27 times in the patent, including in the title and preamble of each claim), and yet, Defendants incorrectly argue that the "dropping means" is a "black box" that is not linked to the disclosed hardware circuitry and rely upon a collection of **non-chip** cases involving nontangible system and

[8] Ample Federal Circuit authority is in accord. *See, e.g.*, *Apex Inc.*, 325 F.3d at 1373 (Fed. Cir. 2003) ("[T]he term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies some structural meaning to one of ordinary skill in the art."); *Mass. Inst. Of Tech. v. Abacus Software*, 462 F.3d 1344, 1356 (Fed. Cir. 2006) ("The claim language here too does not merely describe a circuit; it adds further structure by describing the operation of the circuit."); *Lighting World, Inc. v. Birchwood Lighting, Inc.*, 382 F.3d 1354, 1359-60 (Fed. Cir. 2004) ("In considering whether a claim term recites sufficient structure to avoid application of § 112 ¶ 6, we have not required the claim term to denote a specific structure. Instead, we have held that it is sufficient if the claim term is used in common parlance or by persons of skill in the pertinent art to designate structure, even if the term covers a broad class of structures and even if the term identifies the structures by their function") (overturned on other grounds).

[9] Thus, if the Court disagrees that the term is indefinite, it should adopt NST's construction.

software inventions (misleadingly characterized by Defendants as "computer-related").[10] Br. at 13-14. Defendants also ignore the Federal Circuit precedent cited above that makes clear in the context of **chip** cases that a "circuit" is sufficiently structural. And Defendants' argument that claims must "recite the 'certain cases' in which dropping occurs," (*id.* at 15), runs afoul of the Federal Circuit's holding that it is error to "incorporat[e] unrecited functional limitations into the claims." *Micro Chem., Inc. v. Great Plains Chem. Co*., 194 F.3d 1250, 1258 (Fed. Cir. 1999). Finally, as noted above, it is telling that Defendants do not assert that the "interface means (ANIP, PNIP)," which is the portion of Claim 1's "integrated circuit" that contains the "dropping means," is either governed by § 112 ¶ 6 or indefinite, even though the (rebuttable) "means" presumption would have applied and the identical (yet incorrect) "black box" arguments could have been made.

Because Defendants have not met their high burden of establishing indefiniteness, and because NST has rebutted the § 112 ¶ 6 presumption, the Court should adopt NST's proposed construction, which is consistent with intrinsic evidence and the understanding of a POSITA. Alternatively, if § 112 ¶ 6 applies, the Court should adopt NST's proposed structure, "circuit."

C. '449 Patent Terms – "resource manager…" and "communication manager"

Claim Term	NST's Construction	Defendants' Construction
"resource manager determining whether a	"Resource manager" means "circuit that manages network	"resource manager determining whether a connection between

[10] *WSOU Investments LLC v. Google LLC*, Appeal No. 2022-1066, 2023 WL 6210607 (Fed. Cir. Sept. 25, 2023) ("means for issuing an alert" software feature indefinite in non-chip invention); *Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371 (Fed. Cir. 2009) ("means for assigning" software feature indefinite in non-chip invention); *Noah Sys. Inc. v. Intuit Inc*., 675 F.3d 1302 (Fed. Cir. 2012) ("access means" software indefinite in non-chip accounting system invention); *Optimum Processing Solutions LLC v. Advanced Micro Devices, Inc*., No. 1:09-cv-1098-TCB, 2012 WL 13001400 (N.D. Ga. July 10, 2012) ("processor selection logic" software executed by general purpose computer indefinite in non-chip invention); *Fiber, LLC v. Ciena Corp.*, 792 Fed. Appx. 789 (Fed. Cir. 2019) ("control" indefinite in non-chip invention where patentee unsuccessfully attempted to analogize the non-tangible "control" to circuitry); *Maurice Mitchell Innovations, L.P. v. Intel Corp*., 249 Fed. Appx 184 (Fed. Cir. 2007) ("means for causing" software executed by general purpose computer indefinite in non-chip invention).

target connection with the desired connection properties is available" '449 Patent, Claim 10	resources," and the remaining language should be afforded their plain and ordinary meanings.	modules with desired properties is available to be opened and is not an arbiter prioritizing which port of a switching device is to be utilized."
"communication manager" '449 Patent, Claim 10	"circuit that manages communication between modules" If the Court holds that § 112 ¶ 6 applies, NST proposes the following construction: **Function**: "forward a request for a connection to the resource manager" **Structure**: "circuit"	Subject to § 112 ¶ 6 **Function**: "receiving a request for a connection from the first module, forwarding the request to a resource manager, and receiving the availability of the target connection from the resource manager" **Structure**: Indefinite (insufficient structure disclosed)

Claim 10 of the '449 Patent describes the interaction between two circuits that are constituents of a larger "integrated circuit": a "resource manager" and "communication manager." While NST construes these circuits according to a POSITA's understanding of these terms in light of the specification, Defendants treat them inconsistently: wrongly asserting that "manager" in "communication manager" renders it subject to § 112 ¶ 6 and indefinite, while correctly contending that "resource manager" is sufficiently structural to be definite and not subject to § 112 ¶ 6.

1. "resource manager" and "communication manager" are physical circuitry elements and therefore structural

Both "resource manager" and "communication manager" are consistently described throughout the claim and specification as constituents of an "integrated circuit," which as noted above the Parties have stipulated means "interconnected circuitry on a chip." *See* '449 Patent at Claim 10 ("Method for exchanging messages in an **integrated circuit** comprising…"); *see also* Chmelar Decl. ¶¶ 82-84,110-112 (citing '449 Patent at Fig 3; 1:15-35; 9:66-10:3 ("FIG. 3 shows a system **on chip** [that] comprises a **communication manager CM** and a **resource manager**

RM."); 7:35-39 ("said **integrated circuit** comprises at least one **communication managing means CM** for managing the communication between different modules; **and at least one resource managing means RM** for managing the resources of the network N")). The '449 Patent also discloses that the "resource manager" and "communication manager" are arranged in a network or a network interface means, which are both comprised in integrated circuits. *Id.* ¶ 86, 114 (citing '449 Patent at Abstract; 1:7-11; 7:15-18; 8:7-11; 9:17-21; 9:66-10:6).

As discussed above in the context of "dropping means," an "integrated circuit" is physical hardware, and so too are the constituent circuitry elements that make up the integrated circuit, including the "resource manager" and "communication manager." *See* § V.B., *supra*. And as also discussed above, Defendants' argument that the "dropping means" or "communication manager" are mere "black boxes" that may be implemented as software is incorrect in light of the '449 Patent's disclosing these as structural circuitry elements, not software stored in memory or executed by general purpose computers. *See id.*; *see also* Chmelar Decl. ¶¶ 89, 117.

Defendants argue that "communication ***manager***" is indefinite and lacks structure for using the word "manager,"[11] Br. at 18-20, yet separately concede that "resource ***manager***" is not

[11] None of Defendants' cited authority supports this argument. The term "manager" is not discussed in *Welker* – the *Welker* court determined that "mechanism," "means," "element," and "device" are not sufficiently structural. *Welker Bearing Co. v. PHD, Inc.*, 550 F.3d 1090, 1096 (Fed. Cir. 2008). In *Synchronoss Techs., Inc. v. Dropbox Inc.*, the court, despite finding the term "synchronization manager" subject to § 112 ¶ 6, found "synchronization manager" is sufficiently structural and definite. No. 16-cv-00119, 2017 U.S. Dist. LEXIS 201981, at *30-33 (N.D. Cal. Dec. 7, 2017). Moreover, courts have repeatedly found that the term "manager" is "clearly not a nonce word that might typically fail to connote sufficient structure and overcome the presumption against § 112(6) treatment." *SFA Sys., LLC v. 1-800-Flowers.com, Inc.*, No. 6:09-CV-340, 2011 WL 3476462, at *13 (E.D. Tex. Aug. 8, 2011) (finding "event manager" structural because "the specification treats the event manager as structural: 'the system also includes an event manager coupled to…'"); *Capella Photonics, Inc. v. Fujitsu Network Commc'ns, Inc.*, No. 2:20-CV-00076-JRG, 2021 WL 465430, at *25 (E.D. Tex. Feb. 9, 2021) (finding "Defendants have not overcome the presumption against applying § 112, ¶ 6" because "'power management system' refers to a well-known class of structures").

indefinite and has sufficient structure by offering a construction for that term. *Id.* at 16-18. And, as explained in the last paragraph, the '449 Patent discloses the structure of both the "resource manager" and "communication manager" in parallel.[12] Therefore, because both are described as structural circuits, Defendants' inconsistent treatment of these terms is unwarranted, and their assertion that "communication" manager is subject to § 112 ¶ 6 and indefinite should be rejected.

2. "resource manager" is a "circuit that manages network resources" and no prosecution disclaimer applies

The intrinsic record makes clear that the "resource manager" is a circuit that "manages network resources," consistent with NST's construction. Chmelar Decl. ¶ 91 (quoting '449 Patent at 7:38-39 ("at least one resource managing means RM for managing the resources of the network"); *see also id.* ¶¶ 92-95, 99 (explaining that the '449 Patent passages at 7:46-51, 10:19-26, 10:34-40, 10:41-46, and 10:55-61 summarize the functions of the resource manager, which are all examples of "managing network resources").

Therefore, NST's construction reflects what a POSITA would have understood this term to mean as used in the '449 Patent. The rest of the claim phrase "determining whether a target connection with the desired connection properties is available" should be afforded its plain and ordinary meaning. Indeed, Defendants ascribe no particular meaning to this language at all, other than grafting an unexplained, unsupported "to be opened" requirement. Chmelar Decl. ¶ 100. This insertion is an improper attempt to add additional functional steps and should be rejected for the same reasons noted above regarding Defendants' construction of "connection."

[12] Indeed, just as the '449 Patent uses the terms "communication manager" and "communication managing means" interchangeably, it does likewise with "resource manager" and "resource managing means." Chmelar Decl. ¶¶ 88, 116. Therefore, based on Defendants' concession that "resource manager" is not indefinite and has sufficient structure, Defendants' argument that this interchangeable use warrants a finding of indefiniteness lacks merit. *See* Br. at 19.

Meanwhile, the rest of Defendants' proposed construction inappropriately seeks to add language *negatively* defining the "resource manager" as "***not*** an arbiter prioritizing which port of a switching device is to be utilized," a carve-out that is found nowhere in the specification but that Defendants nevertheless argue is necessitated by alleged prosecution disclaimer. Br. at 16-18.

The bar for prosecution disclaimer is high. There must be an "exacting" disavowal that is "clear and unmistakable." *Thorner*, 669 F.3d at 1365–67 ("The standard for disavowal of claim scope is … exacting."); *MIT v. Shire Pharmaceuticals, Inc.*, 839 F.3d 1111, 1119 (Fed. Cir. 2016) (prosecution history disclaimer must be "clear and unmistakable" such that where disavowal is ambiguous or amenable to multiple interpretations, prosecution history disclaimer does not attach). If there is any ambiguity, there is no disavowal. *Avid Tech.*, 812 F.3d at 1045 ("Where the alleged disavowal is ambiguous," courts do not apply the doctrine of prosecution history disclaimer).

Defendants point to no such "exacting" or "clear and unmistakable disavowal." Indeed, NST's expert analyzed the prosecution passages that Defendants cite and has concluded that there is nothing in the prosecution history concerning whether the resource manager "is not an arbiter prioritizing which port of a switching device is to be utilized." Chmelar Decl. ¶¶ 101-04.

While the Applicant amended claim 10 of the '449 Patent, the functional limitations added had nothing to do with whether the resource manager was an arbiter. Rather, the amendments concerned *features* of the resource manager: 1) receiving a request from the communication manager comprising desired connection properties associated with the sets of communication channels; 2) determining whether a target connection with the desired connection properties is available; and 3) responding with the availability of the target connection to the communication manager (*see id.* ¶ 102), and distinguished the cited Emerson reference based on the fact that Emerson's arbiter does not have those features (*see id.* ¶ 101). The Applicant made no clear and

unmistakable concession regarding whether the resource manager "is not an arbiter prioritizing which port of a switching device is to be utilized." *See id.* ¶ 104. Indeed, the Examiner explained in the reason for allowance that the claim was allowable over the prior art (including Emerson) because it "do[es] not teach wherein the resource manager determines whether the at least one connection with the communication channels is available based on the connection properties being available," which is a limitation already in claim 10. *Id.* ¶ 103 (quoting prosecution history).

3. "communication manager" is a "circuit that managers communication between modules" and not subject to 112 ¶ 6

As Defendants acknowledged, there is a presumption that "communication manager" is not subject to §112 ¶ 6. Br. at 18-19. Defendants fail to cite sufficient evidence to overcome this presumption. And, as set forth above, there is ample support in the specification (as well as Defendants' concession that both "resource manager" and "communication manager" are structural and not indefinite) that compels the conclusion that "communication manager" is sufficiently structural to neither be subject to § 112 ¶ 6 nor indefinite.

NST's construction of a "communication manager" as a "circuit that manages communication between modules" reflects what a POSITA would have understood this term to mean as used in the Asserted Patents. Chmelar Decl. ¶¶ 108, 121. As noted above, the "communication manager" is a circuit that "manages communication between modules. *See id.* ¶¶ 109-121. Since NST is the only party to have offered a construction of "communication manager," its construction should be adopted if it is neither subject to § 112 ¶ 6 nor indefinite.

If the Court determines that § 112 ¶ 6 applies, Defendants' proposed structure and function for "communication manager" are wrong. Rather, the structure would be an "integrated circuit" and the function "forward a request for a connection to a resource manager." *See id*. ¶¶ 123-125.

Regarding function, Defendants' assert that "[t]he functions of the 'communication

manager' are provided in the claim language," but Defendants impermissibly attempt to import functions not found in said claim language. Br. at 20. The only express function performed by the communication manager is: "forward[] the request [for a connection] to a resource manager." '449 Patent, claim 10; Chmelar Decl. ¶ 125. Defendants attempts to add functions to the communication manager not explicitly unrecited in the claim is improper. *See In re Teles AG Informationstechnologien*, 747 F.3d 1357, 1367–68 (Fed. Cir. 2014) ("When construing functional claims under § 112 ¶ 6, [t]he statute does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim") (internal citations omitted); *see also Budde*, 250 F.3d at 1378 (Fed. Cir. 2001) (vacating claim construction ruling because district court improperly held that an "electronic sensing means for determining when the ignition system of the engine delivers an electronic pulse" required "direct detection of those pulses" and reasoning that "[s]uch a determination can be done indirectly").

Regarding structure, Defendants' arguments that "the specification discloses no structure for performing any of these functions," Br. at 20, should be rejected because, as established above, the '449 Patent discloses ample structure. *See* § V.C.1, *supra*.

D. '052 Patent Term – "interconnect means"

Claim Term	NST's Construction	Defendants' Construction
"interconnect means" '052 Patent, Claim 6	"Multi-hop interconnection between modules separated by one or more network nodes." NST disagrees that this term is governed by § 112 ¶ 6, but proposes the following if the Court holds otherwise: **Function** "coupling said plurality of processing modules (M, S)." **Structure**: "circuit"	Subject to § 112 ¶ 6. **Function**: coupling said plurality of processing modules (M, S). **Structure**: bus, switch, point-to-point wire, or network.

As an initial matter, the Parties have already agreed to construe "network" as a "multi-hop

interconnection between modules separated by one or more network nodes." Br. at 6. This is relevant to the construction of "interconnect means" because the '052 Patent uses the terms "an interconnect means (N)" and "a network N" interchangeably. *Compare* '052 Patent at 5:12-31 ("Each module M, S is connected to a ***network N*** via its associated network interface NI") *with* 10:19-20 ("coupling said plurality of processing modules (M,S) by an ***interconnect means (N)***") *and* 10:25-26 ("interconnect means (N) by at least one network interface (NI)"). According to the Federal Circuit, the "interchangeable use of the two terms is akin to a definition equating the two." *Edwards Lifesciences*, 582 F.3d at 1329. Thus, the Parties' agreed upon construction for "network" should be adopted for "interconnect means."

Intrinsic evidence demonstrates that a POSITA would have understood the term "interconnect means" to mean a "[m]ulti-hop interconnection between modules separated by one or more network nodes" as a "network" (*i.e.*, an indirect interconnection) rather than a shared bus (*i.e.*, a ***direct interconnection***). *See* Chmelar Decl. ¶¶ 130-135. For instance, the '052 Patent ascribes the exact same functionalities to an "interconnect means (N)" as it does a "network N." *See* Chmelar Decl. ¶¶ 139-142 (citing '052 Patent at Abstract, Fig. 1, Fig. 4, 1:7-8, 3:18-22, 3:51-54, 4:1-4, 5:24-31). What's more, Claim 6 specifies that the "interconnect means (N)" is connected "by at least one **network interface** (NI)," confirming the "interconnect means" is a network. '052 Patent at Claim 6. A POSITA would also understand "interconnect means" to describe a "network" comprising indirect interconnections between modules, not a direct interconnection between modules as typically found in a bus architecture. Chmelar Decl. ¶¶ 143-144. Thus, a POSITA would understand that the "network N" and the "interconnect means (N)" to be the same thing. *Id.*

Defendants do not propose an alternative construction for interconnect means. Instead, they argue that "interconnect means" should be governed by § 112 ¶ 6. This is unavailing. As noted

above, the '052 Patent discloses that the "interconnect means" is part of an "integrated circuit," which is intrinsically structural according to Federal Circuit precedent. *See* § V.B., *supra* (collecting cases). For instance, the '052 Patent's Abstract expressly discloses that the "interconnect means" is part of an "integrated circuit": "[t]he invention relates to ***an integrated circuit*** having a plurality of processing modules ***and an interconnect means.***" *See* '052 Patent at Abstract. Claim 6 further supports the fact that the "interconnect means" is part of an "integrated circuit" by reciting a "[m]ethod of communication service mapping ***in an integrated circuit***." '052 Patent at 3:7-8, 3:45-46. Each step is performed ***in an integrated circuit***, including "coupling said plurality of processing modules (M,S) ***by an interconnect means (N)***" and "controlling the communication between said at least one first of said plurality of processing modules (M) and said ***interconnect means (N)***." '052 Patent at 10:19-25. To remove any doubt, Claim 1 makes it abundantly clear by reciting an "***[i]ntegrated circuit***, comprising . . . ***an interconnect means (N)*** for coupling said plurality of processing modules (M, S)." '052 Patent at Claim 1; *see also id.* at Claim 6 ("**integrated circuit**, having a plurality of processing modules (M,S)…coupling said plurality of processing modules **by an interconnect means (N)**"). Thus, applying the same analysis as "dropping means," *see* § V.B., *supra*, an "interconnect means" is intrinsically structural for being part of an integrated circuit.

Nevertheless, if the Court finds that § 112 ¶ 6 applies, NST's proposed structure of a "circuit" should be adopted since it best reflects the fact that the '052 Patent discloses the "interconnect means" as part of an integrated circuit, and Defendants' proposed structure of a "bus, switch, point-to-point wire, or network" rejected for being in direct conflict with the '052 Patent's specification, which, as Defendants admit, repeatedly distinguishes the patented Network on Chip technology from "buses, switches, or point-to-point wires." *See* Br. at 23 (citing '052 Patent at

1:50-54 ("in contrast to existing on-chip interconnects ***(e.g., buses, switches, or point-to-point wires),*** where the communicating modules are directly connected, in a NoC the modules communicate remotely via network nodes.")); *id.* (citing '052 Patent at 2:31-33 ("Introducing networks as on-chip interconnects radically changes the communication when ***compared to direct interconnects, such as buses or switches***.")); *id.* (citing '052 Patent at 2:36-38 ("This is in contrast with the prevalent existing interconnects ***(i.e., buses)***")); *id.* (citing '052 Patent at 4:46-50 ("The interconnect is embodied as a network on chip NOC, allowing communication between all aforementioned modules. The network on chip may include wires, bus, time-division multiplexing, switches, and/or routers within a network."); *id.* (citing '052 Patent at 1:25-27 ("In conventional processing systems the systems modules usually communicate to each other via a bus.")). It is incorrect to read the "interconnect means" of the '052 Patent to cover these distinguished and disparaged structures. *Openwave Sys. v. Apple Inc*., 808 F.3d 509, 517 (Fed. Cir. 2015) ("it is difficult to envisage how, in light of the repeated disparagement of mobile devices with 'computer modules' discussed above, one could read the claims of the patents-in-suit to cover such devices); *SciMed Life Sys. v. Advanced Cardiovascular Sys*., 242 F.3d 1337, 1343 (Fed. Cir. 2001) ("Thus, the SciMed patents distinguish the prior art on the basis of the use of dual lumens and point out the advantages of the coaxial lumens used in the catheters that are the subjects of the SciMed patents. That discussion in the written description supports the district court's conclusion that the claims should not be read so broadly as to encompass the distinguished prior art structure.").

E. '9893 Patent Term – "arranging … the first and second information . . . "

Claim Term	NST's Construction	Defendants' Construction
"arranging … the first and second information comprising said issued message as a single address" '9893 Patent, Claim 4	"Arranging … the first and second information comprised in said issued message as a single address"	Indefinite.

A POSITA would understand that the claim and the specification recite that "the first and second information" is "comprised in said issued message." Chmelar Decl. ¶ 149-151. Specifically, Claim 4 recites that "a ***message*** issued by an addressing module M ***comprises***: ***first information*** … and ***second information***." Chmelar Decl. ¶ 149; '9893 Patent at Claim 4. The specification confirms this reading. Chmelar Decl. ¶ 150; '9893 Patent at 3:16-22 ("the ***message comprises first information*** indicative for the location of the addressed module(s) within the network. ***The message*** may further ***include second information*** indicative for a particular location within the module, such as a memory, or a register address").

NST's proposed plain and ordinary meaning construction reflects a POSITA's understanding of this term (*see* Chmelar Decl. ¶ 148), and because the intrinsic evidence does not depart from the language of the claim. *See Johnson Worldwide Assocs., Inc. v. Zebco Corp.*, 175 F.3d 985, 989 (Fed. Cir. 1999) (there is a "heavy presumption in favor of the ordinary meaning of claim language"); *Chrimar Sys., Inc. v. Alcatel-Lucent, Inc.*, No. 6:13-CV-880-JDL, 2015 WL 11549073, at *7 (E.D. Tex. Jan. 16, 2015) ("constru[ing] 'arranging impedance within the at least one path' to have its plain meaning"); *Brocade Commc'ns Sys., Inc. v. A10 Networks, Inc.*, No. 10-CV-03428-LHK, 2012 WL 33251, at *15 (N.D. Cal. Jan. 6, 2012) (construing "arranging a list of virtual addresses" to have its plain and ordinary meaning).

NST's construction appropriately affords the true meaning to a term containing an obvious "clerical or typographical mistake," which is "clearly evident from the specification, drawings, and prosecution history." Br. at 24 (citing *Superior Fireplace Co. v. Majestic Prods. Co.*, 270 F.3d 1358, 1376 (Fed. Cir. 2001)). The claim and specification consistently disclose that the message "comprises" the first information and the second information. '9893 Patent, Claim 4, 3:16-22; Chmelar Decl. ¶ 150. "[C]laims must be construed so as to be consistent with the specification, of

which they are a part." *Merck & Co. v. Teva Pharms. USA, Inc.*, 347 F.3d 1367, 1371 (Fed. Cir. 2003) ("[a] fundamental rule of claim construction is that terms in a patent document are construed with the meaning with which they are presented in the patent document."). NST's proposed construction corrects a clear typographical error in the claims to allow the term to be construed consistent with its usage in the specification.

Defendants wrongly argue that a "POSITA would not know what the term means by 'arranging' two pieces of information into 'a single address.'" Br. at 24. But as noted above, Defendants' expert proposes an exceptionally well-credentialed POSITA who would immediately understand this. *See* § IV., *supra.* The specification provides that "[a] transaction address will therefore have two parts: (a) a destination identifier, and (b) an internal address at the destination." '9893 Patent at 5:50-52. A person of ordinary skill would understand that "to arrange" means, for example, "to combine," "to order," to group," or "to assemble." Chmelar Decl. ¶ 154. A POSITA would also understand that the first and second information would be truncated, added, concatenated, multiplied, or otherwise manipulated into a single address to comport with the addressing scheme of the integrated circuit. *Id.*. Thus, a POSITA would determine with reasonable certainty what it means to "arrange" the first and second information into a "single address." *Supra* § V.B.

For these reasons, the Court should adopt NST's plain and ordinary meaning construction.

F. '2893 Patent Terms

1. "each data package comprising N data elements"

Claim Term	NST's Construction	Defendants' Construction
"each data package comprising N data elements" '2893 Patent, Claim 10	NST incorporates its definition for the term "data package," "data elements" are groups of data, and the remaining language should be afforded their plain and ordinary meanings.	"every data package communicated by the network stations has a fixed size of N data elements"

The main dispute between the Parties appears to be over the meaning of "a ***fixed size*** of N data elements." NST's position is that a "fixed size of N data elements" refers to the fact that the number of data elements in a given data package must remain fixed (*i.e.*, constant) throughout the course of each communication. While the number of data elements can vary between one data package and the next, the number for any given data package cannot fluctuate (*i.e.*, must remain "fixed"). Conversely, Defendants' argument seeks to inject a limitation that is not supported by the claims or the specification. Br. at 25-29. Namely, Defendants argue that the '2893 Patent requires all (*i.e.*, "every") data packages ever communicated across an integrated circuit to contain the same exact same number of data elements. *Id.* at 25. Thus, Defendants' construction might as well read: "[each and] every data package [ever] communicated by the network stations [must have the same] fixed size of N data elements." This is not what the '2893 Patent teaches.

NST's construction also best reflects the language actually used in the claims and the specification itself. For instance, Defendants seek to substitute the word "each" for "every" in the claims. However, the word "every" is never used to describe "data package comprising N data elements" anywhere in the '2893 Patent. Instead, the claims and the specification repeatedly disclose "***each*** data package." '2893 Patent at Abstract, 2:3, 3:40, and 4:52. The difference between "each data package" and "every data package" is enormous. Whereas "each" means every one "***individually***," the word "every" means "***all possible***." *Compare* THE AMERICAN HERITAGE DICTIONARY (2022), https://www.ahdictionary.com/word/search.html?q=each *with id.,* https://www.ahdictionary.com/word/search.html?q=every. Put simply, if adopted, Defendants' construction would profoundly alter the meaning of the disputed term from "***each*** data package ***individually***" to "***all possible*** data packages ***collectively***." This must be rejected.

As for the rest of NST's construction, Defendants do not appear to dispute NST's proposal

that the data elements be construed as "groups of data." Br. at 25-29. For instance, a person of ordinary skill would understand Figure 3 to show that data elements are grouped into respective data packages. Chmelar Decl. ¶ 164, 168-169. This grouping is also shown in other figures, including Figure 4 below, where the individual data elements "h," "d0," and "d1" in each row are grouped together in separate data packages. '2893 Patent at 7:58-61 ("a data package consisting of data elements h, d0 and d1"). Consistent with this interpretation, the specification further discloses that data elements are "sent" together as part of a "data package." *See, e.g.*, '2893 Patent at 7:58-61 ("a data package consisting of data elements h, d0 and d1 is sent from data router 120 to data router 140."). A person of ordinary skill would understand this to mean that individual "data elements" are grouped together and sent as a "data package." Chmelar Decl. ¶ 170.

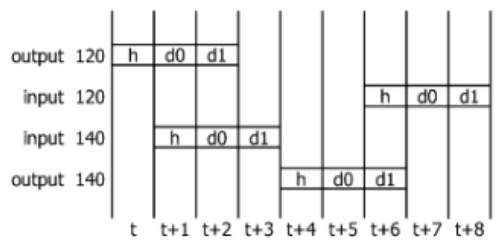

FIG. 4

2. "data package"

Claim Term	NST's Construction	Defendants' Construction
"data package" '2893 Patent, Claim 10	"fixed-size arrangement of data"	See Defendants' construction of "each data package comprising N data elements" above.

Almost all of Defendants' section on "data package" is comprised of cross-references to arguments raised in their "each data package comprising N data elements" section. The only new content offered is a single, unsupported sentence that reads: "NST's construction should be rejected because it introduces the concept of the 'arrangement' of the data, which is ambiguous and something not contemplated by the claim language "data package." Br. at 30. Such a hollow

statement offered without any evidence, argument, or explanation must be rejected outright.

Contrary to Defendants' opinion, NST's proposed construction draws on language in the '2893 Patent. For instance, Figures 2 and 4 show data elements in different data packages being arranged in a particular way, wherein the first data element is identified as "h," the second "d0," and the third "d1." '2893 Patent at FIGS. 2 and 4. The specification also discloses a specific arrangement of these data elements, wherein the "first data element h of a data package" comprises header information. *See* '2893 Patent at 6:35-40; *see also id.* at 2:24-25 ("the first data element (i.e. a header)"), 5:29-32, 6:47-53, 6:62-63, 7:3-6, 8:4-6, FIG 2, FIG 4. After the header, the data are arranged by way of "subsequent data elements d0 and d1." *Id.* at 6:38-40 ("The subsequent data elements d0 and d1 of this data package are received by the data router 120 at respective clock cycles t+1 and t-i-2."), 7:58-61, 8:7-18, FIG 2, FIG 4. These data are not presented in a random, arbitrary order. A person of ordinary skill would understand these data elements as being presented in a particular arrangement. Chmelar Decl. ¶ 174-179.

In short, NST's proposed construction for "data package" should be adopted because it accurately reflects what is disclosed in the specification, and because Defendants' have chosen to forgo briefing any actual opposition.

3. "data storage elements"

Claim Term	NST's Construction	Defendants' Construction
"data storage elements" '2893 Patent, Claim 10	"Array of one or more elements that store data."	"each being a structure that stores one data element"

Defendants' construction seeks to inject a limitation that is directly contrary to the specification. Namely, Defendants argue that "data storage elements" can only store one data element at a time. Br. at 31-32. Not true. For instance, the specification clearly discloses that while header data can have "a fixed position in the data package, *e.g.* ***the first data element*** (i.e. a

header)," it is also possible that "***other data elements*** [(*i.e.*, d0 or d1)] may (also) contain such information." '2893 Patent at 2:22-26. Chmelar Decl. ¶¶ 167, 177.

Defendants' argument that data storage elements with multiple data elements would mean that the "mathematical relationship [(M*N)] would be lost" is likewise baseless. In fact, the specification repeatedly discloses data storage elements (*i.e.*, "(M*N)") with data element values (*i.e.*, "N") that are greater than one. *See* '2893 Patent at 6:1-2 ("slow communication channel 150 is also extended with ***N=3 data storage elements***"), 5:63-64 ("The network 100 shown in FIG. 1 is arranged to communicate ***data packages with size N=3***."), 6:60-61 ("due to the presence of ***N=3 data storage elements*** 160"), and 7:11-12 ("In FIG. 3, M=1, ***N=3***, A=1 and B=2"). Changing the number of data elements (*i.e.*, "N") does not destroy the mathematical relationship (M*N) at all. To the contrary, it a person of ordinary skill would understand that these examples show how the equation (M*N) is meant to work with more than one data element. Chmelar Decl. ¶¶ 187-190.

Finally, Defendants fail to explain how the word "array" is in anyway "ambiguous" or "potentially overbroad." An "array" is just "a group of elements forming a complete unit." MERRIAM-WEBSTER DICTIONARY (2023), https://www.merriam-webster.com/dictionary/array. This is what the '2893 Patent discloses.

G. '800 Patent Terms

1. "optimal amount of data"

Claim Term	NST's Construction	Defendants' Construction
"optimal amount of data" '800 Patent, Claim 12	Plain and ordinary meaning	Indefinite

Intrinsic evidence confirms that "optimal amount" should be afforded its plain and ordinary meaning. As Dr. Chmelar observes, the '800 Patent discloses that the "object of the invention" is to provide "improved interconnect utilization," where the improvement is achieved by buffering

data until conditions for an optimal transfer (i.e., the "connection properties") are satisfied. Chmelar Decl. ¶ 194 (citing '800 Patent at 3:35-37, 4:18-28, 4:49-57, 5:27-35, 6:15-17,6:22-30, 6:31-36, 6:47-53, 7:23-28, 7:44-51). From these passages, Dr. Chmelar concludes: (1) buffering of data improves and/or optimizes interconnect utilization; (2) the optimal amount of data to be buffered can be based on communication properties of a communication and (3) the optimal amount of data to be buffered can be specific to a particular interconnect. *Id.* ¶ 195. As Dr. Chmelar concludes, the "optimal amount of data" is not a fixed quantifier but based on certain conditions such as communication properties and/or interconnect characteristics. *Id.* Thus, a POSITA would understand that a "first optimal amount of data to be buffered" equates to the amount of data that is optimal under certain conditions. *Id.*

Affording this term its plain and ordinary meaning is also supported by case law affording the term "optimal" its plain and ordinary meaning. *See, e.g.*, *Bitmicro LLC v. Kioxia America, Inc., et al.*, Case 6:22-cv-00331, Dkt. 54, at *30 (W.D. Texas Feb. 16, 2023) (finding that "***optimized*** memory operations" is "not indefinite and should be construed according to its plain-and-ordinary meaning"). Likewise, a POSITA would understand that the '800 Patent uses the term "optimal amount" in its plain and ordinary sense, *i.e.*, optimal amount of data to be buffered based on certain conditions, which is supported by dictionary definitions of the time that define "optimal" as the "[m]ost favorable or desirable; optimum" and "optimum," which further means "[t]he point at which the condition, degree, or amount of something is the most favorable." Ex. 8, American Heritage Dictionary (4th ed. 2000).

Defendants have not met their "high burden" of proving indefiniteness "by clear and convincing evidence." *Halliburton*, 514 F.3d at 1249-50; *Traxcell Techs., LLC v. Cellco P'ship*, No. 6:20-CV-01175-ADA, 2023 WL 2415583, at *4 (W.D. Tex. Mar. 8, 2023); 35 U.S.C. § 282.

The ’800 Patent relates to optimizing interconnect utilization in a network (Chmelar Decl. ¶ 194) by buffering data until optimal transfer conditions are satisfied. *Id.* (citing ’800 Patent at 4:49-57) (“buffer data until the buffered data is sufficiently large to be transferred optimally over an interconnect means in a packet.”); *see also id.* (“[t]he larger a packet is, the smaller is the amount of packet headers and therefore the overhead is reduced and the interconnect is utilized more efficiently.”). The data are only transferred when sufficient data have been buffered to provide the optimal packet size. *Id.* Thus, a POSITA would not consider this term to be indefinite. *Id*. ¶ 198.

Defendants’ argument that the “optimal amount of data” is indefinite because it “lacks objective bounds,” (Br. at 32-33), is unavailing as it ignores the fact that any POSITA would understand that the goal of integrated circuit design is to send as much data in the fewest a number of transmissions as possible. *Id.* ¶¶ 195-196. Thus, the “optimal amount of data” is the maximum amount of data that can be transmitted at a given moment across an integrated circuit. *Id.* ¶ 197. The objective upper bounds can be calculated using the physical attributes baked into the integrated circuit, the availability of network resources at the time of the transmission, and the objective communication properties that were established when the integrated circuit was first fabricated.

As an example, a latency guarantee is a fixed value that is baked into various elements of an integrated circuit to ensure that data is transmitted at least as quickly as the specified amount of time. *Id.*¶ 197. An integrated circuit might be fabricated with a latency guarantee value of 1/10 of a millisecond to ensure that real-time video communications do not experience “jittering” effects. *Id*. This value is hardwired into the integrated circuit at fabrication. Thus, objectively calculating the “optimal amount of data” simply involves determining the maximum amount of data that can be buffered in 1/10th of a millisecond or less. *Id.*

For this reason, the cases cited in Defendants' brief are inapposite. Br. at 32. For instance, in *Akamai Techs., Inc. v. MediaPointe, Inc.*, the claims did not recite an "optimal" number that could be objectively quantified. Instead, the claim explicitly recited the "optimal/***best*** [delivery] route[s]," a subjective factor that was left to a user's discretion. No. 2:22-cv-06233-MCS (AFMx), 2023 WL 7386057, *6-7 (C.D. Cal. July 7, 2023). Here, "optimal" as used in the term "optimal amount" is not a subjective preference left to "user discretion." It is an objective value that can be calculated based on objective attributes that are baked into an integrated circuit during fabrication. Similarly, *Intellectual Ventures* involved subjective, software quality of service requirements that were "entirely subjective and user-defined" by each user based on how the user wanted different software programs to perform. *Intell. Ventures I LLC v. T-Mobile USA, Inc.*, 902 F.3d 1372, 1374 and 1381 (Fed. Cir. 2018). Here, the communication properties are objective and pertain to physical attributes baked into integrated circuit hardware components. Lastly, in *Optimum Processing Solutions*, the term "optimized" was found to be indefinite for failing to disclose what "***optimized*** to perform certain logical sequences employed in executing [said] instructions" meant. *Optimum Processing Solutions v. Advanced Micro Devices*, Civil Action No. 1:09-CV-1098-TCB, 2012 WL 13001400, at *11-13 (N.D. Ga. July 10, 2012). The Court found the term to be indefinite because plaintiff had failed to "identify the performance index" that was to be optimized.[13] Here, the '800 Patent not only discloses what is optimized (i.e., the "optimal ***amount of data***"), it also discloses how to determine this value objectively. The '800 Patent discloses objective criteria (i.e., communication properties) that are used to determine both how and when optimal transfer conditions are satisfied. *See* Chmelar Decl. ¶ 194; *see also* '800 Patent at 4:18-28; 4:49-57; 6:15-

[13] Tellingly, the court also suggested, albeit in dicta, that the outcome might have been different had "optimized" meant "***maximize*** or minimize a performance index." *Id.* This is exactly how "optimal" is used in the '800 Patent.

17; 6:22-30; 6:31-36; 7:23-28; 7:44-51. The '800 Patent relates to optimizing interconnect utilization in a network (*id*. ¶ 194) by buffering data until optimal transfer conditions are satisfied. *Id.* (citing '800 Patent at 4:49-57 ("buffer data until the buffered data is sufficiently large to be transferred optimally over an interconnect means in a packet.")); *see also id.* ("[t]he larger a packet is, the smaller is the amount of packet headers and therefore the overhead is reduced and the interconnect is utilized more efficiently."). For these reasons, Defendants' indefiniteness arguments must be rejected.

2. "optimal moment for sending the data . . ."

Claim Term	NST's Construction	Defendants' Construction
"optimal moment for sending the data in said first wrapper or said second wrapper" '800 Patent, Claim 12	NST incorporates its definition for the term "wrapper," and the remaining language should be afforded their plain and ordinary meanings.	Indefinite

The "optimal moment" term relates to sending data between a master and a slave. Claim 12 of the '800 Patent recites:

> at least one of the first determination unit and the second determination unit is further **configured to determine an optimal moment for sending the data** in said first wrapper or said second wrapper **according to communication properties of the communication between the master and the slave**.

'800 Patent at 12:16-21. NST incorporates its proposed construction for "wrapper," *infra*. The rest of the "optimal moment" term requires no construction beyond its plain and ordinary meaning. *See, e.g.*, *Bitmicro LLC v. Kioxia America, Inc., et al.*, Case 6:22-cv-00331 (W.D. Texas Feb. 16, 2023) (affording "optimal" a plain and ordinary meaning).

Defendants' position that this term is indefinite under § 112 is incorrect, as the term is readily understandable to a POSITA in light of the intrinsic and extrinsic evidence. As Dr. Chmelar opines, a POSITA would understand "optimal moment" to relate to the "transmission moment"

(*i.e.*, when transmission occurs) whereas the "transmission" would refer to the "data to be transmitted." Chmelar Decl. ¶ 203 (citing '800 Patent at 3:14, 7:4-6). The "transmission moment" is not an arbitrary moment in time. A person of ordinary skill would understand that in an integrated circuit, the "transmission moment" is simply the next possible moment when network resources become physically available so that its physically possible to transmit the data. Chmelar Decl. ¶ 205. The specification further confirms that a POSITA would understand "transmission moment" to sufficiently disclose the "optimal moment." For example, the specification discloses:

> . . . the **transmission moment may be determined in a similar way** by the first and second determination means BLDU1, BLDU2. **For a guaranteed throughput GT connection, data should wait for one of the slots reserved for its connection.** Using a "flush"-like signal/flag may force the sending of the data in advance. Alternatively, **for a best effort BE connection, a round robin arbitration across connections in the NI can be used.**

'800 Patent at 7:4-14.

For instance, as recited in claim 12, throughput is one of the connection properties that is used to determine the "optimal moment" for transmitting data. *See id.*; *see also* '800 Patent at 12:16-32 ("wherein the communication properties include . . . throughput where a lower bound on throughput is guaranteed"). A guaranteed throughput equates to a guarantee that a component of an integrated circuit was designed to ensure that a specified amount of data can be transmitted across it in at least the specified amount of time. (*e.g.*, Mbps). Chmelar Decl. ¶ 197. Throughput is a communication property that encompasses guaranteed throughput (GT) as a lower bound whereas best effort (BE) does not. Chmelar Decl. ¶ 204. The guaranteed throughput is an attribute of an integrated circuit's design, which is hardwired during a circuit's fabrication. Chmelar Decl. ¶¶ 199, 204-207. Guaranteed throughputs are particularly useful for high demand applications, like real-time video conferencing, that depend on the transmission of large amounts of data in short periods of time. Chmelar Decl. ¶ 195. In this context, a POSITA would understand that the

optimum moment to send data is whenever a "slot" becomes available to squeeze in at least as much data to meet the throughput value. By way of example, if the guaranteed throughput value is 5 Mbps, a POSITA would understand that the "optimal moment to send data" is simply the next available moment when network resources permit at least 5 megabits of data to be transmitted across the link in 1 millisecond or less. *See* Chmelar Decl. ¶¶ 201-07.

Extrinsic evidence further supports a plain and ordinary meaning construction. A dictionary definition of "optimal" is "[m]ost favorable or desirable; optimum" and "optimum," which further means "[t]he point at which the condition, degree, or amount of something is the most favorable." Ex. 8, American Heritage Dictionary (4th ed. 2000). A plain and ordinary meaning is appropriate because claim 12 recites that the optimal moment is determined under a particular set of circumstances (*i.e.*, "according to communication properties"). Accordingly, extrinsic evidence supports a plain and ordinary meaning construction.

Defendants improperly suggest that the connection properties are irreconcilable by arguing that "[i]t is not clear to a POSITA which of these (optimal amount of data versus optimal moment) is controlling." Br. at 37. Not true. The '800 Patent explicitly discloses the fact that the data must be buffered *before* it can be transmitted. *See* '800 Patent at 5:60-65 ("two wrapper means WM1, WM2 buffer data coming from the master M or the slave S, respectively, until a certain amount of data is buffered. Thereafter, the buffered data is transferred over the network N."); *see also id*. at Claim 12 (reciting the limitation that the "optimal amount of data" is determined *before* the limitation that the "optimal moment" is determined). Thus, before an optimal moment can be determined, the data must be buffered, which requires calculating the optimal amount of data to buffer in the first place. Chmelar Decl. ¶ 205.

Similarly, Defendants' argument that it is impossible to reconcile the "data correctness"

communication property with the optimal moment is equally unavailing. "Data correctness" is not a user-defined property. Like "latency" and "throughput," it is an objective attribute that is baked into an integrated circuit. Chmelar Decl. ¶¶ 38, 142, 197, 199, 205-06. Accordingly, the optimal moment is simply the next available moment when data can be transmitted across a link while ensuring the "data correctness" threshold value.

Finally, Defendants mischaracterize Claim 12 as reciting "an optimal moment ***based on . . .***" (*i.e.*, "derived from"). Br. at 36. This is not what Claim 12 recites. Instead, Claim 12 recites an "optimal moment ***according to . . .***" (*i.e.*, "in conformity with"). *See Oilfield Equip. Mktg., Inc. v. New Tech Sys., Inc.*, No. CIV.A. MO-02-CA-183, 2005 WL 6258387, at *6 (W.D. Tex. Sept. 2, 2005), *aff'd*, 227 F. App'x 925 (Fed. Cir. 2007) (finding that the plain and ordinary meaning of "according to" to be "in conformity with"). Defendants fail to justify why the phrase "according to," which is explicitly recited in Claim 12 and disclosed in the specification, should be removed and replaced with Defendants' phrase "based on," which appears in neither. *See* '800 Patent at 4:19-27, 6:49-53, 12:15-21.

For these reasons, the Court should afford this term its plain and ordinary meaning and reject Defendants' indefiniteness argument.

3. "according to communication properties . . . "

Claim Term	NST's Construction	Defendants' Construction
"according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is	according to communication properties of the communication between the master and the slave, wherein the communication properties include: ordering of data transport; flow control, including: when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is	Requires use of all the communication properties identified after "include."

available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery" '800 Patent, Claim 12	available for the produced data at the remote buffer; throughput, where a lower bound on throughput is guaranteed; latency, where an upper bound for latency is guaranteed; lossiness, including dropping of data; transmission termination; transaction completion; data correctness; priority, and data delivery	

Defendants do not dispute the text that NST has proposed in its construction. Br. at n.6. Rather, Defendants seek to construe the word "include" in Claim 12 to mean "all of the listed communication properties" recited in the claim, and that all of these communication properties "must be ***used***" to determine (*i.e.*, to calculate) the optimal moment. Br. at 38. Defendants' positions are unavailing.

First, Defendants have failed to justify deviating from the plain and ordinary meaning of the term "include." Defendants do not dispute that the term "include" would be clear and readily understandable to a finder of fact. *See, e.g.*, *Sybase, Inc. v. Vertica Systems, Inc.*, Case NO. 6:08-cv-0024 at 19 (E.D. Tex. May 13, 2010) (finding the term "includes a selective one of [list of items]" to be "clear and understandable to the fact finder and thus does not require construction."). Nor do Defendants argue that the plain and ordinary meaning of the term is "inadequate" because it "has more than one 'ordinary' meaning" or because "reliance on a term's 'ordinary' meaning does not resolve the parties' dispute." *See O2 Micro, Ltd. v. Beyond Innovation Tech. Co.,* 521 F. 3d 1351, 1361 (Fed. Cir. 2008). In fact, Defendants' proposal appears to be that "include" should mean "all the communication properties identified," which comports both with this term's plain and ordinary meaning and NST's position.

Second, Defendants' argument that the communication properties "must be ***used***" to

determine (*i.e.*, "to calculate") the optimal moment is not supported by the specification or Claim 12, which actually recites "determine an optimal moment for sending the data . . . ***according to*** communication properties." '800 Patent at 12:16-31. The difference between "must be used" and "according to" (i.e., "in conformity with") is significant. *See Oilfield Equip. Mktg., Inc. v. New Tech Sys., Inc.*, No. CIV.A. MO-02-CA-183, 2005 WL 6258387, at *6 (W.D. Tex. Sept. 2, 2005), *aff'd*, 227 F. App'x 925 (Fed. Cir. 2007).

Collectively, Defendants' construction would have the effect of rewriting the term from the recited language "determine an optimal moment for sending the data . . . ***according to*** the communication properties" to "the communication properties ***must be used*** to determine an optimal moment." Br. at 38 – 40. This is not how Claim 12 was drafted. Nor do Defendants provide support in the specification or Claim 12 that supports such an extreme reinterpretation of the claim language. Tellingly, the phrase "must be used" does not appear a single time anywhere in the '800 Patent. For these reasons, Defendants' proposal must be rejected.

Defendants cannot distort the prosecution history to support of their position. While it is true that the Examiner used the word "using" in the phrase "optimal time to send data over a communication line ***using all of the listed conditions/requirements***," additional context from the Notice of Allowance shows that the Examiner was not using the term "using" in the way Defendants suggest. There, the Examiner wrote that "prior art found alone or in combination does not teach or suggest the communication properties of the communication between the master and slave used to determine the optimal moment for sending data, ***incorporating the claimed list of communication properties to make that determination***." Dkt. 77-20, Notice of Allowability at 2. The Examiner's use of the phrase "***incorporating the claimed list*** of communication properties to make that determination" is consistent with the phrase "according to" (*i.e.*, in conformity with)

that is actually recited in Claim 12, not the "must be used" phrase that Defendants now propose.

4. "first determination unit" / "second determination unit"

Claim Term	NST's Construction	Defendants' Construction
"first determination unit" / "second determination unit" '800 Patent, Claim 12	Not subject to § 112 ¶ 6. "determination unit" means a "circuit that makes determinations based on stored or received information." The remaining should be afforded plain and ordinary meaning. If the Court holds that § 112 ¶ 6 governs, NST proposes the following in the alternative: **Functions**: the function for "first determination unit" is "determine a first optimal amount of data to be buffered by the first memory," the function of the "second determination unit" is "determine a second optimal amount of data to be buffered by the second memory," and the function for at least one of the first determination unit and the second determination unit: "determine an optimal moment for sending the data in said first wrapper or said second wrapper" **Structure**: circuit	Subject to § 112 ¶ 6. Function: "determining a first/second optimal amount of data to be buffered by the first/second memory" and for at least one of the first determination unit and the second determination unit "determining an optimal moment for sending data" Structure: indefinite

NST's construction of "determination unit" as a "circuit that makes determinations based on stored or received information" reflects what a POSITA would have understood the term to mean as used in the '800 Patent. Defendants, by contrast, have not met their burden of proving by clear and convincing evidence that this term is indefinite and have not overcome the presumption that § 112 ¶ 6 does not apply.

Applying the same analysis as "dropping means," *see* § V.B., *supra*, the '800 Patent expressly discloses a machine: a "systems on chip, i.e. a plurality of modules on the same chip (including e.g. system in a package, multi-die modules) or on different chips, communicate with each other via some kind of interconnect. The interconnect is embodied as a network on chip NOC." '800 Patent at 5:7-11. Moreover, the '800 Patent is also directed to hardware circuitry; nowhere does the Asserted Patent disclose or claim intangible software or firmware. Chmelar Decl. ¶ 221. This is consistent with the Parties' agreed construction of "integrated circuit" as "[i]nterconnected circuitry on a chip" and that is recited in the disputed claim's preamble. Br. at 6; '800 Patent at Claim 12.

This is also consistent with the '800 Patent's disclosure of "[t]he determination of the optimal burst length may be performed based on information ***stored in*** the determination units BDLU [sic] 1, 2 or on information received from the network N or IP blocks," '800 Patent at 6:62-65, since information ***can be stored only in*** storage circuitry, such as latches, flip-flops, registers, or memory cells. Chmelar Decl. ¶ 222. In another embodiment, the "determination units" (BLDU) are physically located, or "arranged[,] in the network interfaces NI associated to the slave S and master M, respectively." '800 Patent at 6:47-49, FIG 2. Because the determination unit is housed within the network interfaces NI, "data is [therefore] buffered in the network interface NI, i.e. the interconnect surface, such that the master M or slave S, which may constitute intellectual property block [that] are not involved in the actual communication or the communication protocol for communicating over the interconnect or network." *Id*. at 7:34-40. Further still, in another embodiment, the "wrapper means comprise a determination unit BLDU for determining the optimal first or second amount of data to be buffered." *Id*. at 4:18-24. Again, information cannot be buffered except with storage *circuitry*, which, as discussed previously, the Federal Circuit has

held is inherently structural. *See* § V.B., *supra* (collecting cases).

In further alternative embodiments, the "determination unit" itself is the network interface or wrapper, as applicable. '800 Patent at 8:34-36 ("In the device claim enumerating several means, several of these means can be embodied by one and the same item of ***hardware***"). Notably, Defendants do not dispute that such network interface NI is not subject to § 112 ¶ 6. Construing "determination unit" to be non-structural and subject to § 112 ¶ 6 where there is no dispute that network interface NI is a known structure is irreconcilable to the patent's disclosure that the determination unit and the network interface NI are embodied by the same hardware. But to be sure, the "communication properties" provide additional structure for the "determination unit." A person of ordinary skill would understand that the general goal of integrated circuitry is to transmit data as soon as possible, and the optimal moment is the soonest available transmission window that exists that is in accordance with the communication properties. Chmelar Decl. ¶¶ 224-225.

Defendants provide no compelling reason—let alone one meeting the clear and convincing standard required to invalidate this term—to depart from these disclosures of the determination unit's disclosed structure, such as the least two expressly recited structures in the disputed claim (integrated circuit and wrapper) and at least three structures disclosed in the specification (integrated circuit, network interface, and wrapper). Defendants correctly acknowledge "the failure to use the word 'means' creates a presumption that § 112, ¶ 6 does not apply." *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 703–04 (Fed. Cir. 1998); Br. at 41. This presumption is only "rebutted if the evidence intrinsic to the patent and any relevant extrinsic evidence so warrant," and that "[i]n deciding whether either presumption has been rebutted, the focus remains on whether the claim as properly construed recites sufficiently definite structure to avoid the ambit of § 112, ¶ 6." *Id.* Defendants have failed to do so.

Defendants lead with the argument that "unit" is a purportedly well-recognized nonce word. Br. at 41. But Defendants cited cases all relate to systems and software that are not inherently structural, like integrated circuits. *Compare* Br. at 41 *with* § V.B. ("dropping means"), *supra*. Defendants then observe that the specification interchangeably refers to determination units, as disputed in the limitation, with determination means, and concludes that § 112 ¶ 6 automatically applies. However, this glosses over Defendants' admission that the presumption that § 112, ¶ 6 does not apply because the disputed claim recites "determination unit" rather than "determination means." '800 Patent at Cl. 1. Defendants further incorrectly conclude that "the specification states that optimal burst length 'may be' performed based on information stored and received (i.e., it is optional)." Br. at 43. But this reading is not faithful to the disclosure, which states, as discussed above: "[t]he determination of the optimal burst length may be performed based on information stored in the determination units BDLU [sic] 1, 2." '800 at 6:62-64. Contrary to Defendants' misreading, the Asserted Patent's disclosure is express that information is stored in the determination units, and, instead, what is optional is that the optimal burst length may be based (i) on the information stored in the determination units, or (ii) information from other sources.

Defendants' remaining points repeat their arguments with respect to "dropping means," and such arguments also miss the mark here. *Compare* Br. at 42–43 *with, generally, supra*, § V.B. ("dropping means"). Defendants argue that that the "determination unit" is linked to a "black box abstraction." Br. at 42. But as discussed above, the "determination unit" has storage circuitry is embodied by at least the network interface NI structure. Defendants next argue that the specification makes no mention of a circuit as it relates to the "determination unit," nor does the circuit appear in the Description of the Preferred Embodiments. Br. at 43. However, as discussed above, that the "determination unit" stores information indicates that it is at least storage circuit

and/or network interface NI. More so, the Asserted Patent regularly references "circuits" in at least the title, abstract, field of the invention, background of the invention, and claims. *See*, *generally*, '800 Patent. Defendants then argue that the determination units may be implemented as software or firmware or implemented without using stored information. Br. at 43. But this invites extrinsic evidence to supplant intrinsic evidence. Neither software nor firmware can store information (Chmelar Decl. ¶ 221), and reading out this preferred embodiment violates the canons of claim construction. More so, the '800 Patent also does not contemplate software of firmware, as discussed in § V.B. ("dropping means"), *supra*.

Nevertheless, if § 112 ¶ 6 applies, NST's proposed structure of a "circuit" should be adopted for the reasons set forth above. Meanwhile, NST's proposed function should be adopted over Defendants' because NST's function tracks the language in Claim 12. '800 Patent at 11:66-12:8, 12:16-21. Conversely, Defendants' proposed function departs from the claim language by adding "and for at least one of the first determination unit and the second determination unit," which is not recited in Claim 12 or disclosed anywhere in the specification. Br. at 40-43.

Defendants have not produced clear and convincing evidence that "determination unit" is both (i) subject to § 112 ¶ 6, overcoming the presumption against such conclusion, and (ii) lacking a disclosed structure to conclude that it is indefinite. Thus, NST's construction should be adopted, which is consistent with intrinsic evidence and the understanding of a POSITA.

5. "wrapper"

Claim Term	NST's Construction	Defendants' Construction
"wrapper" '800 Patent, Claim 12	"memory"	Indefinite

NST's proposed construction of "wrapper" as a "memory" reflects what a person of ordinary skill would understand the term to mean. The '800 Patent discloses that the wrapper is a

physical part of an integrated circuit with a specific location in the network interface. '800 Patent at Fig. 1, Fig. 2, 5:58-60. Applying the same analysis as "dropping means," and consistent with Federal Circuit precedent, the wrapper's being a physical component of a circuit (*i.e.*, an integrated circuit) provides sufficient, definitive structure. *See* § V.B., *supra* (collecting cases).

The '800 Patent discloses that the wrapper is a memory circuit because it is "responsible for ***buffering*** data sent from the master M and the salve S over the network N." *Id.* at 5:60-62, 3:41-43 ("A first wrapper means associated to said second processing module buffers data"), 3:54-56 ("second wrapper means is associated to the first processing module for buffering data"). A person of ordinary skill in the art would understand that buffering data is synonymous with storing data, which can only be achieved with storage (*i.e.*, memory) circuitry (*e.g.,* latches, flip-flops, registers, memory cells, etc.). Chmelar Decl. ¶¶ 222, 240. Numerous courts throughout the country have found the term "buffer" to be synonymous with "memory." *See, e.g.*, *Tivi, Inc. v. AT&T, et al*., Case No. 2:09-cv-259 (E.D. Tex. Oct. 11, 2011) (construing "buffer" to mean "memory where data can be temporarily stored for transfer."); *3Com Corp. v. D-Link Systems, Inc*., Case No. 03-cv-2177 (N.D. Cal. Feb. 6, 2007) (construing "buffer" as "a memory for temporary storage of data"); *Crossroads Systems, Inc. v. 3Par, Inc*., Case No. A-10-CA-652-SS (E.D. Tex. Nov. 8, 2011) (construing "buffer" as a "memory device that is utilized to temporarily hold data."); *In Re Papst Licensing Gmbh & Co. Kg Litigation*, Case 1:07-mc-00493-RMC at 5 (D.C. Dist. Nov. 24, 2009) (construing "buffer" as "memory used to store data . . .").

Defendants do not raise separate indefiniteness arguments for the term "wrapper" in isolation. Rather, Defendants argue that the term "wrapper" is indefinite for the same reasons presented for their brief regarding the term "said first wrapper" / "said second wrapper." Br. at 45. However, as explained in the next section, Defendants have failed to meet their "high burden" of

providing by "clear and convincing evidence" that this term is indefinite.

6. "said first wrapper" / "said second wrapper"

Claim Term	NST's Construction	Defendants' Construction
"said first wrapper" / "said second wrapper" '800 Patent, Claim 12	"said first memory" / "said second memory"	Indefinite

Defendants' have once again presented inconsistent positions. By separately arguing that "said first/second wrapper" means "said first/second memory" in their proposed function for "determination unit," Defendants cannot credibly suggest that it is unclear whether "said first/second wrapper" is meant to refer back to the previously-recited "first/second memory." *Compare* Br. at 40-41 with 44. Indeed, Defendants actually outline a compelling case for why this term is definite in their brief. Defendants readily admit that these "terms could be referring to the previously-recited 'first memory' and 'second memory,'" which "***would be consistent with the specification's teaching that the wrapper may 'buffer data***.'" Br. at 44. Defendants further admit that the "buffering function in claim 12 is performed ***by the 'first memory' and the 'second memory***.'" *Id.* (citing '800 Patent at 11:63-66; 12:1-3). Indeed, Defendants also admit not only that "[t]hese structures ***store data*,"** and but also that "claim 12 recites that ***there is 'data in said first wrapper or said second wrapper***.'" *Id.*

NST agrees with this rationale, and notes that it is further supported by even more sections of the '800 Patent that were not included in Defendants' brief. *See* '800 Patent at 3:41-43 "A first wrapper means associated to said second processing module buffers data"); *id.* at 3:54-56 ("second wrapper means is associated to the first processing module for buffering data").

While Defendants offer a compelling case for this term being definite, their two indefiniteness scenarios are neither clear nor convincing. Perplexingly, after previously arguing

that "wrapper" means "memory," Defendants now suggest that it is unclear because "said first/second wrapper" "could be referring to the previously-recited 'first interconnect module' and 'second interconnect module.'" Br. at 44. Defendants' position is undermined by their position on "wrapper," and language in the specification that discloses that the ***interconnect means***—not the wrapper—is responsible for transferring data. *See* '800 Patent at 3:54-57 ("wrapper means is associated to the first processing module for buffering data from said first processing module ***to be transferred over the interconnect means***").

Defendants' final scenario departs even further from reason by relying on the supposed presence of a mysterious "***unrecited structure***." Tellingly, rather than identify a discrete structure, Defendants refer only to a supposed "interface." Br. at 45. To be clear, "interface" ***is not*** recited in Claim 12. '800 Patent at 11:44-12:32. In fact, the word "interface" does not appear once in the claim at all. *Id.* Defendants have manufactured this supposed structure from thin air. To suggest that a person of ordinary skill would somehow think that "said first/second wrapper," which Defendants admit means "first/second memory," refers back to a mysterious "unrecited structure" instead of the explicitly recited "first/second memory" is not credible and must be rejected outright.

VI. Conclusion

For the reasons set forth above, Defendants' proposed constructions should be rejected in favor of NST's constructions. Whereas NST's constructions are firmly grounded in the understandings of a POSITA informed by the patent claims and specifications, Defendants' intent to unduly limit the scope of the claims by any improper means is unmistakable and Defendant's constructions would result in numerous claim construction errors. Therefore, NST respectfully requests that its proposed claim constructions be adopted.

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Respectfully submitted,

/s/ *Daniel S. Stringfield w/ permission William E. Davis, III*
William E. Davis, III
Texas Bar No. 24047416
DAVIS FIRM PC
213 N. Fredonia Street, Suite 230
Longview, TX 75601
(903) 230-9090
bdavis@davisfirm.com

Daniel S. Stringfield
Peter C. Krusiewicz
Allison E. Strong
NIXON PEABODY LLP
70 West Madison St., Suite 5200
Chicago, IL 60602
(312) 977-4130
nst@nixonpeabody.com
dstringfield@nixonpeabody.com
pkrusiewicz@nixonpeabody.com
astrong@nixonpeabody.com

Erica J. Van Loon
Vincent C. Capati
NIXON PEABODY LLP
300 S. Grand Avenue, Suite 4100
Los Angeles, CA 90071
(213) 629-6000
evanloon@nixonpeabody.com
vcapati@nixonpeabody.com

Attorneys for Plaintiff Network System Technologies, LLC

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was served via electronic mail on November 17, 2023, to all opposing counsel of record.

/s/ J. William E. Davis, III
William E. Davis, III