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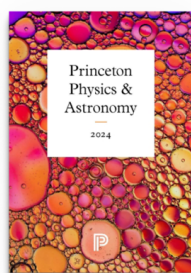


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Efficient tristable resistive memory based on single layer graphene/insulating polymer multi-stacking layer

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Tristable resistive memories based on single layer graphene (SLG)/insulating polymer multi-stacking layer were fabricated. By using the traditional transfer method, the chemical vapor deposition-synthesized SLG serving as charging layers were combined with poly(methyl methacrylate) (PMMA) layers and polystyrene (PS) layers to form charge traps with various depth. Based on the PS/SLG/PMMA/SLG/PMMA multi-stacking layer, the devices exhibited efficient tristable memory performances. The ratios as large as 10^4 between different resistive states were maintained for a retention time of more than 10^4 s. The operation mechanisms of stepping-charging in the multi-stacking layer for the tristable resistive switching were proposed on the basis of the current-voltage analysis. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4875596>]

As the demands for high density integration and high performance memory in portable electronic devices are continuously increasing, the semiconductor industry has long been seeking a high-density, high-speed, and low-power consumption storage technology. Among the various candidates for the next-generation memory, the resistive memory which is based on resistance change modulated by electrical stimulus, has recently inspired scientific and commercial interests given its high-density integration, high operation speed, and simple structure.^{1–4} However, owing to the lithography limit scaling down the area size to further obtain high-density storage will become more and more challenging. It is believed that multilevel storage technology is the practical way to increase the storage density of resistive memory.^{5,6} The multilevel tunability of resistance offers a unique opportunity to store more than 2-bits in a single cell, thereby achieving a high density memory with minimized downscaling. Hence, the research of the possibility of multilevel resistive memory devices has attracted extensive attentions. Recently, Kim *et al.* demonstrated a flexible three-level resistive memory device with B- and N-doped carbon nanotubes as charge traps.⁷ Park *et al.* reported a four-level nonvolatile small-molecule memory cell, which was embedded with Ni nanocrystals surrounded by a NiO tunneling barrier.⁸ A highly reproducible multilevel resistive memory device utilizing graphene oxide sheets/polyimide hybrid nanocomposite has been developed.⁹ Moreover, Cu-doped HfO₂ films, TiO₂ thin films, and TaO_x films have also exhibited multi-level memory effect.^{10–12} However, the reported ratios of different resistive states in the multilevel memory devices were smaller than 10^2 . The stable operation of multilevel resistive memory generally requires a long retention time and a large ratio of different resistive states to avoid misreading.

Recently, the organic memory devices with larger on/off ratio have been reported employing the structures of polymer/multilayer graphene/polymer stacking layer in which the multilayer graphene acts as charge traps.^{13–15} For

obtaining multi-level resistive memory effect, it is important to tune the depth of charge traps.⁷ It is generally considered that the workfunction of chemical vapor deposition-synthesize graphene is difficult to modify. Nevertheless, the depth of charge traps can be systematically tuned by employing insulating polymer layers with different energy band structure.¹⁶

In this work, poly(methyl methacrylate) (PMMA) layer and polystyrene (PS) layer were used as charge blocking layers and single layer graphene (SLG) was used as charge trapping layers to form charge traps with different depth. Memory device using PS/SLG/PMMA/SLG/PMMA multi-stacking layer as active medium was presented, which presented tristable resistive memory effect and excellent ratio of over 10^4 between different resistive states. The memory performances were investigated systematically. The memory mechanisms were discussed on the basis of the *I*–*V* results.

Figure 1 shows fabrication process of the resistive memory device using SLG/insulating polymer multi-stacking layer as active medium. The SLG used as interlayer in the insulating polymer layers was synthesized on 25 μ m-thick Cu foil by CVD technique.¹⁷ Cu foil (1.5 cm $\times$ 1.5 cm) was placed into a 2 in. quartz tube of the CVD chamber. H₂ of 28 standard cubic centimeters per minute (SCCM) was introduced into the chamber, and the temperature of the chamber was brought up to 1035 °C in 30 min. Then, CH₄ of 19 SCCM was introduced for graphene growth at a pressure of 140 Pa. After reaction for 10 min, the chamber was cooled down to room temperature with flow of 28 sccm H₂. The fabrication method of the active medium was similar to the previously reported graphene transfer method.¹⁷ A PMMA layer (50 nm) was spin-coated on the SLG/Cu substrate (Figure 1(b)). Subsequently, the SLG/PMMA stacking layer was separated from Cu foil by dissolving Cu in ferric chloride solution (Figure 1(c)), followed by rinsing with de-ionized water. Clean ITO glass substrate was spin-coated with 50 nm-thick PS layer (Figures 1(d) and 1(e)), and the PMMA/graphene stacking layer was transferred onto the ITO/PS substrate forming ITO/PS/SLG/PMMA structure (Figure 1(f)). After drying the device at 300 K for 24 h,

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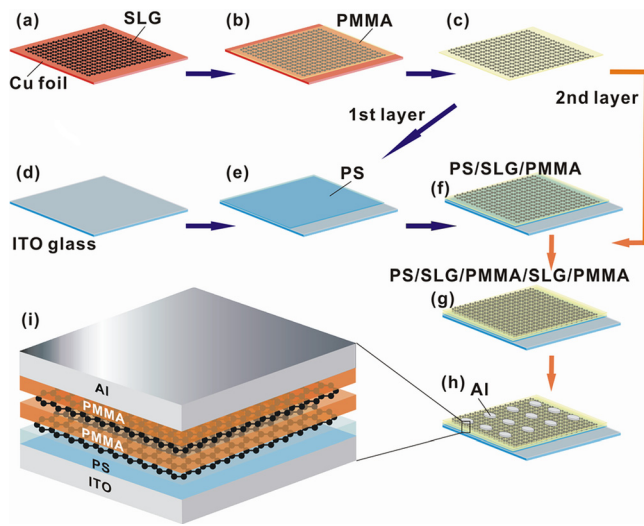


FIG. 1. Schematic of fabrication process for ITO/PS/SLG/PMMA/SLG/PMMA/Al device: (a) growth of SLG on Cu foil; (b) deposition of PMMA layer on SLG/Cu substrate by spin-coating; (c) separation of PMMA/SLG stacking layer from Cu foil by dissolving Cu foil; (d) clean ITO-coated glass substrate; (e) deposition of PS layer on ITO-coated glass substrate by spin-coating; (f) formation of ITO/PS/SLG/PMMA structure by transferring PMMA/SLG on glass/ITO/PS; (g) formation of ITO/PS/SLG/PMMA/SLG/PMMA structure by transferring PMMA/SLG on ITO/PS/SLG/PMMA; (h) deposition of Al top electrodes by using thermal evaporation process; (i) the magnifying schematic structure of the ITO/PS/SLG/PMMA/SLG/PMMA/Al memory unit cell.

another SLG/PMMA stacking layer was sequentially transferred onto the PMMA surface forming ITO/PS/SLG/PMMA/SLG/PMMA structure (Figure 1(g)). After drying the device at 300 K for 24 h, the top circular Ag electrodes with a diameter of 0.5 mm were deposited onto the active film by thermal evaporation, as shown in Figure 1(h). Figure 1(i) shows the magnifying schematic structure of the ITO/PS/SLG/PMMA/SLG/PMMA/Al memory cell in which the SLG was used as charge trapping layer. For comparison, the device with ITO/PMMA/SLG/PMMA/SLG/PMMA/Al structure was also fabricated. The as-synthesized SLG was characterized by scanning electron microscopy (SEM, HITACHI S-3000N), Raman spectrum (Renishaw inVia), and Atomic Force Microscope (AFM, Agilent 5500AFM/SPM). All electrical measurements of the devices were performed by using semiconductor characterization system (Keithley 4200-SCS) at 300 K in air.

The morphology of SLG synthesized on Cu foil was measured by SEM, as shown in inset of Figure 2(a). For the growing time of 10 min, the Cu surface was fully covered with continuous graphene film in which the wrinkles were associated with the thermal expansion coefficient difference between Cu and graphene.¹⁷ Figure 2(a) shows Raman spectrum of the sample with typical peaks for graphene, including a 2D-band located at 2644 cm^{-1} and a G-band located at 1588 cm^{-1} . The intensity of D-band at 1350 cm^{-1} , a measure of defects in the graphene was below the equipment detection limit. It indicated typical features of high quality single layer graphene, e.g., ~ 0.5 G-to-2D intensity ratio, and undetectable D-band.¹⁸ The thickness of the as-fabricated graphene sheets on Si substrate was further directly measured by AFM, as shown in Figure 2(b). The inset line scan profile showed that the thickness of the graphene sheets was smaller

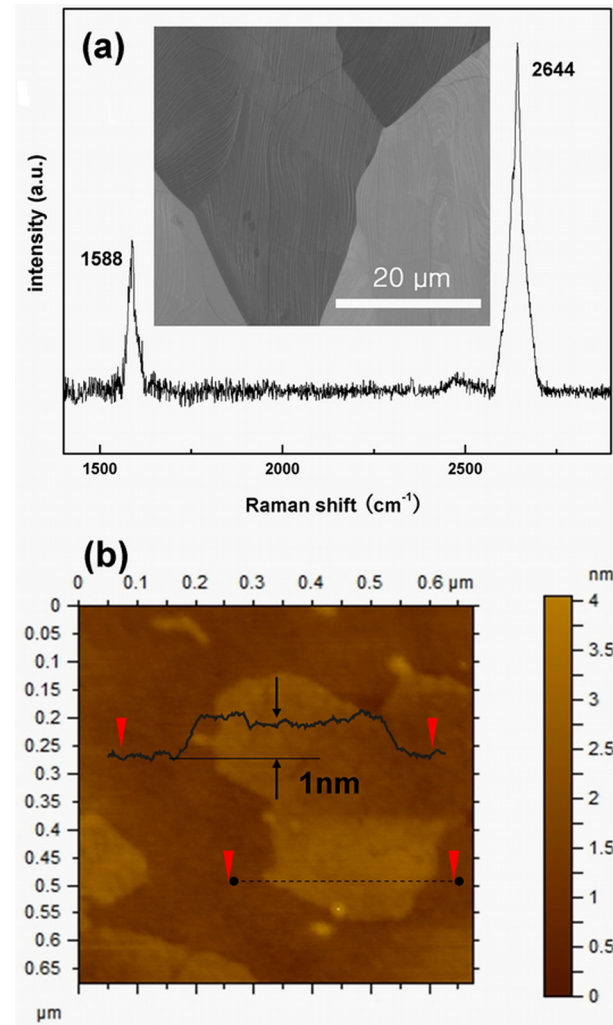


FIG. 2. (a) Raman spectra of single layer graphene, and SEM image of single layer graphene on Cu foil (inset). (b) AFM image of a single layer graphene on Si substrate.

than 1 nm. The results indicated that the high quality single layer graphene sheets were obtained in our experiments.

Figure 3 shows I - V curves for ITO/PS/SLG/PMMA/SLG/PMMA/Al device. In the measurement, the top Al

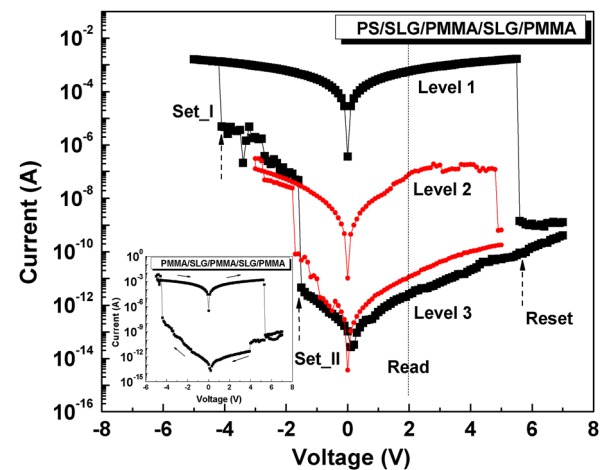


FIG. 3. I - V curves of ITO/PS/SLG/PMMA/SLG/PMMA/Al device and I - V curve of ITO/PMMA/SLG/PMMA/SLG/PMMA/Al device (inset).

electrodes were grounded and the bias was applied to the bottom ITO electrode. The applied voltage was swept with a step of 0.1 V in a cycle from 7 to -5 V and then from -5 to 7 V. The device clearly showed electrical hysteresis behaviors, an essential feature of resistive memory device. In the voltage sweep from 0 to -5 V, the current increased gradually in the beginning but increased abruptly above a voltage of ~ -2.0 V (defined as Set_II). This corresponded to the transition from low current state to intermediate current state. The further increase of bias led to the second-time current abrupt increase from intermediate current state to high current state above voltage of ~ -4 V (defined as Set_I). In the following sweep from -5 to 0 V, the device sustained the high current state. During the sweep from 0 to 5 V, the current abruptly decreased to low current state at a higher voltage of ~ 6 V. As shown in the red dot curve of Figure 3, after transfer from low current state to intermediate current state the device could return to the low current state at voltage of ~ 5 V. Three distinct conducting states are observed: high current state (defined as level 1), intermediate current state (defined as level 2), and low current state (defined as level 3). The distinct tristable states in the voltage range of 0–5 V allows a voltage (e.g., 2 V) to read the various signal of the memory device. The current ratio between level 1 and level 2 at 2 V bias is as large as more than 10^4 , and the current ratio between level 2 and level 3 is more than 10^4 , which are enough to decrease the probability of misreading.

The inset of Figure 3 is the I - V curve of ITO/PMMA/SLG/PMMA/SLG/PMMA/Al device, which exhibited the similar electrical hysteresis behaviors as the ITO/PS/SLG/PMMA/SLG/PMMA/Al device with large current ratio. However, for ITO/PMMA/SLG/PMMA/SLG/PMMA/Al device, the low current state was switched to high current state at ~ 4.5 V directly without the existence of an intermediate current state. This clearly proved that the tristable resistive of the ITO/PS/SLG/PMMA/SLG/PMMA/Al device was due to the presence of the bottom PS layer. To further examine charge conduction in the organic device, the I - V characteristics

of ITO/PS/SLG/PMMA/SLG/PMMA/Al device in negative bias regions depicted in double-log plot is shown Figure 4(a). The data at low voltage up to -0.5 V could be well fitted with the TE conduction mechanism, as shown in the inset of Figure 4(a), where $\ln(I)$ is plotted against $V^{1/2}$.¹⁹ This phenomenon was due to the thermally generated free carriers at the interface between the electrode and the organic layers. In the voltage region (from -0.5 to -1.5 V) of the low current state, the slope of the fitting line was ~ 2 ($I \sim V^2$), which could be explained by the space-charge-limited current (SCLC) conduction based on trap model.²⁰ In higher voltage region (from -1.6 V to -4.1 V), the device was switched to intermediate current state, and the I - V characteristics showed a large linear slope of ~ 5 . The large slope value of the fitting line indicates that the traps in the stacking layer are exponentially distributed over energy in the organic materials band gap.²¹ This revealed that the number of carriers injected into the stacking layer was significantly higher in this voltage range and the response followed a strong space charge limited current, which was known as a trap charge limited current with full trapping models ($\alpha \gg 2$).¹⁵ After the state transition to high current state at -4.2 V, the I - V curve can be fitted well by using the Ohmic current model with linear slope of 1. The carrier transport due to the Ohmic current in the high current state is not affected by the direction of the current.

Figure 4(b) shows schematic diagram of the energy band structures for ITO/PS/SLG/PMMA/SLG/PMMA/Al devices under zero-bias. The LUMO and the HOMO represent the energy levels of the lowest unoccupied molecular orbital and the highest occupied molecular orbital, respectively. The wide energy gap of the PS and PMMA layer suggests that the PS and PMMA layer can act as charge blocking material.^{13,22} The single layer graphene films between the insulating polymer layers act as charge-trapping sites.²³ Thus, in the PS/SLG/PMMA/SLG/PMMA stacking structure two energy wells are formed. The relative small LUMO of PS leads to the relative shallow energy well for PS/SLG/PMMA structure,

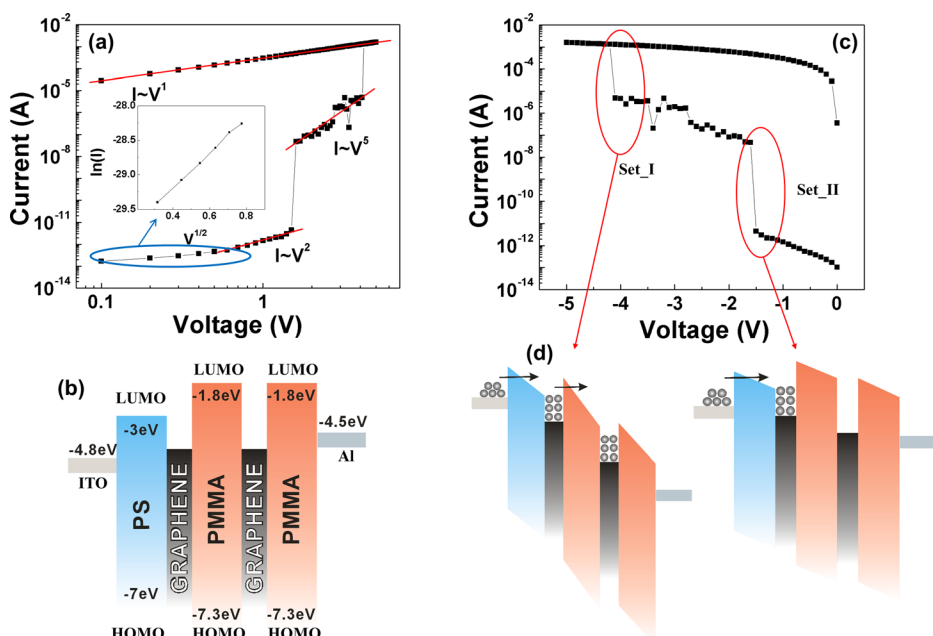


FIG. 4. (a) Electrical behavior analysis of ITO/PS/SLG/PMMA/SLG/PMMA/Al device based on I - V curves. (b) Schematic energy band structures of the ITO/PS/SLG/PMMA/SLG/PMMA/Al device under zero-bias. (c) I - V curve of the device under Set_I bias and Set_II bias. (d) Schematic energy band structures corresponding to the electron transport under Set_I bias (left) and Set_II bias (right).

which may play the key role in the tristable resistive memory effect of ITO/PS/SLG/PMMA/SLG/PMMA/Al device. Figures 4(c) and 4(d) show the I - V curve and schematic diagrams of the energy band structures for ITO/PS/SLG/PMMA/SLG/PMMA/Al devices under Set_I and Set_II bias, respectively. It is considered that the stepping-charging process in the multi-stacking layer is contributed to the tristable memory effect. When the applied voltage increases above the Set_II bias, the injected electrons exponentially increase through the tunneling process due to the relative low energy barrier between ITO and PS. The electrons existing at the LUMO level of PS are transported through the tunneling mechanism among the PS molecules. The electrons can be trapped in the single layer graphene layer because of the difference of potential between PS and graphene, as shown in bottom right of Figure 4(c). As a result, the device switches from low current state to intermediate current state, and the trapped charge-limit current mechanism documented the conduction at intermediate current state. However, due to the relative large energy barrier between graphene and PMMA, the electrons are only captured in one of the graphene layer, which cannot generate sufficient internal field to form conducting filaments. When the applied voltage increases further above Set_I bias, the external electric field is large enough to make electrons tunnel through PMMA layer and capped by the second graphene layer, as shown in bottom left of Figure 4(c). Therefore, the almost complete occupation by electrons in the two graphene layers are sufficient to generate a higher enough internal field to form the conducting filament in the stacking layer, which results in the Ohmic current in the high current state.^{13,24,25} It should be noted that for ITO/PMMA/SLG/PMMA/SLG/PMMA/Al device the relative large energy barriers between ITO and PMMA results in the larger bias for conduction switch. The two graphene layers may be occupied by injected electrons at the same time under large external electric field, and the tristable states were not obtained, as shown in inset of Figure 3.

The memory performances of ITO/PS/SLG/PMMA/SLG/PMMA/Al devices, including operation voltage distribution, current responses during voltage cycles, and retention characteristics, were investigated. The Set_I and Set_II voltage distributions extracted from I - V plots are shown in Figure 5(a). The distribution of the Set_I voltage was between -3.5 V and -4.7 V, and the distribution of the Set_II voltage was between -1 V and -2.8 V. Thus, for ITO/PS/SLG/PMMA/SLG/PMMA/Al device the Set_I and

Set_II voltage can be set as -5 V and -3 V, respectively. Set-Reset sequence test were performed in order to investigate the switching characteristics of the tristable resistive memories for which the three-value storage could be achieved. The current-time response of the device during the “Reset(7 V)-Read(2 V)-Set_I(-5 V)-Read-Reset(7 V)-Read-Set_II(-3 V)-Read” cycles is shown in Figure 5(b). The reset pulse of 7 V was applied to turn the device to the low current state (state 3), the Set_I pulse was applied to turn the device to the high current state (state 1), and the Set_II pulse was applied to turn the device to the intermediate current state (state 2). Then, the reading pulse was applied to distinguish different conduction states of the device. After the reset pulse was applied, the current at the next reading pulse was approximate 10^{-12} A, indicative of the low current state (state 3). The reading current following the Set_I pulse was approximate 10^{-4} A, indicative of the high current state (state 3). Subsequently, the reading current following the Set_II pulse was approximate 10^{-8} A, indicative of the intermediate current state (state 2). The retention ability was tested by keeping the device in the various conduction states under ambient conditions. Figure 5(c) shows the currents as functions of the retention time for 10^4 s. The device stably sustained the initial current values of level 1, level 2, and level 3 for 10^4 s under a constant reading voltage (2 V), indicative of the nonvolatile and long-time stability of the tristable resistive memory device. The memory performances indicate that the ITO/PS/SLG/PMMA/SLG/PMMA/Al cells are applicable in three-value-storage memory devices for high-density storage. Moreover, three-value logic for high-speed compute can be achieved by employing the ITO/PS/SLG/PMMA/SLG/PMMA/Al cells.

In summary, a tristable resistive memory based on PS/SLG/PMMA/SLG/PMMA multi-stacking layer was presented. By using insulating polymer (PS and PMMA) as charge blocking materials and using SLG as charging material, the depth of charge traps with polymer/SLG/polymer structure could be tuned, which was considered as the key role for the tristable resistive memory. The stepping-charging process in the multi-stacking layer due to the different charge traps depth was proposed. As large as 10^4 ratios between the three resistive states can be achieved even after retention time more than 10^4 s. The efficient tristable resistive memories hold promising application in high-density storage and three-value logic for high-speed compute.

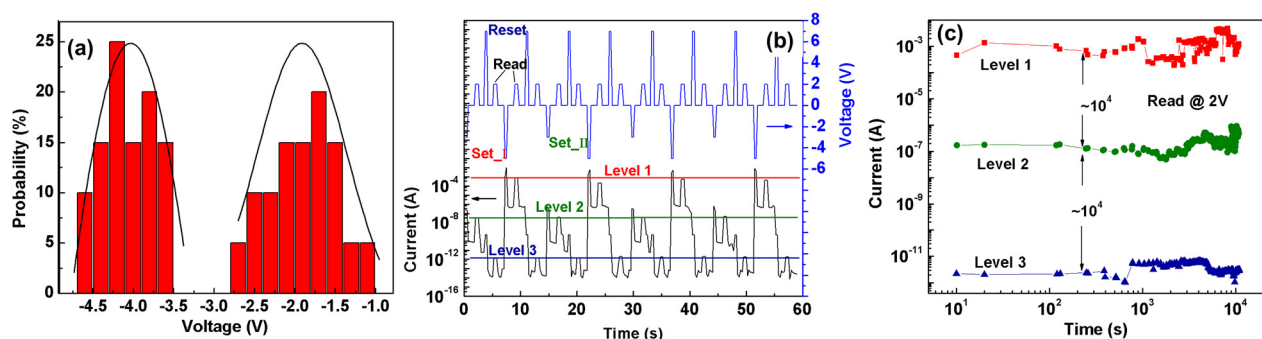


FIG. 5. (a) Distributions of Set_I and Set_II voltage. (b) Current response of the device during the voltage cycles. (c) Retention test of the device.

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