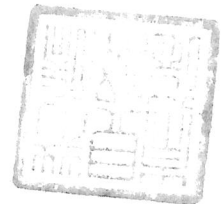

VLSI TECHNOLOGY

Second Edition

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Murray Hill, New Jersey*



McGraw-Hill Book Company

New York St. Louis San Francisco Auckland Bogotá Caracas Colorado Springs
Hamburg Lisbon London Madrid Mexico Milan Montreal New Delhi
Oklahoma City Panama Paris San Juan São Paulo Singapore Sydney Tokyo Toronto

This book was set in Times Roman by Publication Services.
 The editor was Alar E. Elken;
 the designer was Albert M. Cetta;
 the production supervisor was Salvador Gonzales.
 Drawings were done by Bell Laboratories, Inc.
 Project supervision was done by Publication Services.
 Arcata Graphics/Halliday was printer and binder.

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1 2 3 4 5 6 7 8 9 0 HALHAL 8 9 3 2 1 0 9 8

ISBN 0-07-062735-5

Library of Congress Cataloging-in-Publication Data

VLSI technology.

(McGraw-Hill series in electrical engineering.
 Electronics and electronic circuits)
 Includes index.

1. Integrated circuits—Very large scale integration.
 I. Sze, S. M., 1936— . II. Series.
 TK7874.V566 1988 621.381'73 87-22803

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1	Cry C. W 1.1 1.2 1.3 1.4 1.5 1.6
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CHAPTER 11

VLSI PROCESS INTEGRATION

S. J. HILLENIUS

11.1 INTRODUCTION

It was first recognized by G. W. A. Dummar in 1952 that electronic equipment could be made from a single block of layers of insulating, conducting, rectifying, and amplifying materials with the electrical functions being connected by cutting out areas of the various layers.¹ This was the first description of an integrated circuit, but it was not until 1958 that J. S. Kilby invented and demonstrated an integrated circuit (IC). These first demonstration circuits were germanium transistors, resistors, and capacitors formed on a wafer by selectively etching the germanium by applying black wax to mask the active regions. The first circuits formed this way were phase shift oscillators and a flip-flop. From that primitive start, the mass production of semiconductor ICs developed in the early 1960s and has continued to grow exponentially. Today, ICs are complex devices with millions of individual components that are manufactured on a single silicon crystal and interconnected by tiny wires that are microns wide. The process of forming these devices out of a single piece of silicon crystal will be described in this chapter.

Integrated circuits consist of layers of insulating, semiconducting, and conducting regions. These layers are assembled in such a way as to form transistors that are interconnected to produce a certain desired electrical function. The individual transistors come in a variety of types. Each type of transistor has particular attributes that make it more or less desirable for particular types of electrical functions. Each type of transistor will also have different needs when it

comes to processing. The major IC technologies that are used today are n-channel metal-oxide-semiconductor (NMOS), complementary metal-oxide-semiconductor (CMOS), bipolar, and integrated-injection-logic bipolar (I²L). The order in which these technologies are presented is the order of increasing complexity of the processing. Table 1 shows the relative attributes of each of the IC technologies from the point of view of circuit characteristics.²

The purpose of this chapter is to present the fundamentals of integrating silicon processing steps to create silicon devices. The basic principles of operation of these devices will not be discussed, and it will be assumed that the reader is familiar with these fundamentals. These principles of operation will be referenced wherever it is necessary to include them to understand the processing constraints and particular features of each technology. Detailed explanations of the operation of these devices can be found in texts on device physics, such as those by Sze,^{3,4} Grove,⁵ and Muller and Kamins.⁶

11.2 FUNDAMENTAL CONSIDERATIONS FOR IC PROCESSING

The process of building devices in a single piece of silicon crystal is a process of building successive layers of insulating, conducting, and semiconducting

TABLE 1
Characteristics of integrated transistors²

	NMOS	CMOS	Bipolar	
			n-p-n	I ² L
1. General				
Supply voltage range	+	++	—	+
Power	+	++	—	+
Speed	+	+	++	+
Transconductance	—	—	++	++
Circuit density	++	+	—	+
Drive capability	—	+	++	+
2. Digital				
Switching speed	++	++	++	+
Power	+	++	—	+
Noise margins	+	++	—	—
Logic swing	—	++	—	—
3. Analog				
Gain per stage	—	+	++	
Bandwidth	—	—	++	
Input impedance	++	++	—	
Power	++	++	—	
Output swing	—	+	++	
Linearity	—	+	++	
Analog switches	+	++	—	
Precision elements	++	++	+	

The symbols represent moderate (—), good (+), and superior (++) behavior.

material. Each layer is patterned to give a distinct function and relationship with surrounding areas and subsequent layers. The layers are produced and patterned by using the techniques described in the first 10 chapters of this book.

11.2.1 Building Individual Layers

Figure 1 depicts some of the more important ways to create a layer in or on the silicon crystal. The layers are formed by oxidation, implantation, deposition, or epitaxial growth of silicon. Each one of these layers can be formed uniformly, as shown in the left side of Fig. 1, or selectively, as shown in the right side of the figure. The patterning of the layers for selective formation would be achieved by using the photolithography and etching procedures described in Chapters 4 and 5, as would any subsequent patterning of the layers.

The various techniques for forming individual layers have their own usefulness for particular applications. For example, if an insulating layer is needed, the oxidation of silicon described in Chapter 3 forms a layer of SiO_2 , which is an excellent insulator and can be formed with a high degree of uniformity. However, the formation of the SiO_2 layer consumes silicon and may require relatively long thermal cycles for thicker layers. Therefore, if a thick insulating oxide is needed,

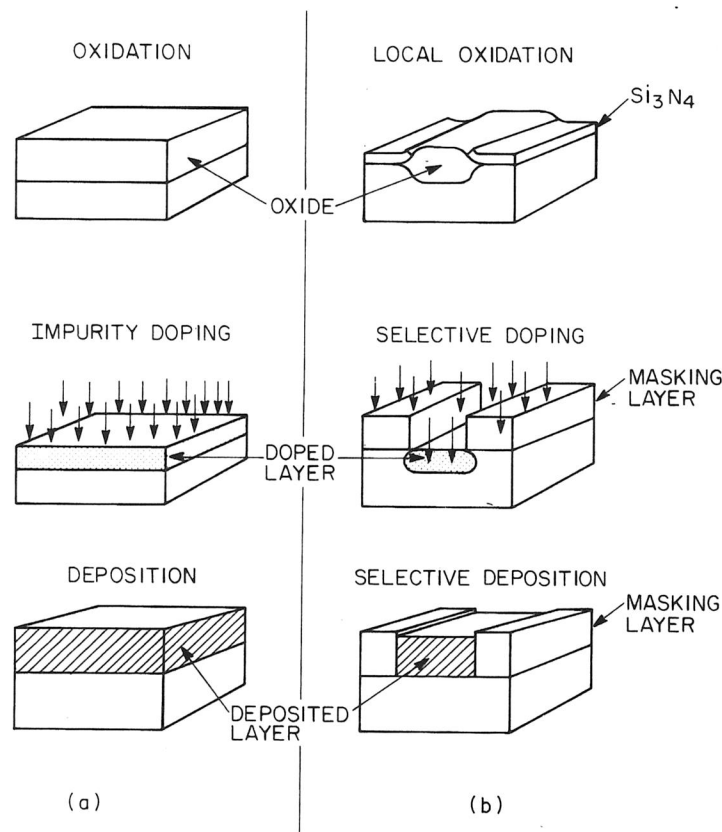


FIGURE 1

Schematic representations of forming layers in silicon: (a) uniform, (b) selective.

it might require an oxide deposition as described in Chapter 6. The deposited oxide in general has a poorer uniformity than the thermally grown oxide but can be deposited at much lower temperatures. This kind of analysis must be made at each step in the process development to determine which type of layer will give the desired results without adversely affecting previous layers. Oxidation and deposition are the most common ways of forming a dielectric layer. The oxidation can be made selective by depositing and patterning Si_3N_4 before oxidation, which allows the oxide to form only wherever the Si_3N_4 is removed, since the Si_3N_4 blocks the oxidation. This technique is sometimes called “local oxidation.”

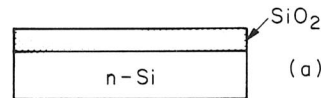
The junctions formed by n-type and p-type regions are the fundamental components of all transistors. The doping levels and depths of these doped regions will determine the characteristics of the devices. Ion implantation is the most important doping technique in modern ICs. The techniques and theory presented in Chapter 8, along with the diffusion of the dopants as described in Chapter 7, will determine the doping profiles. In designing a process sequence it must always be remembered that the doping profiles will change with every subsequent thermal cycle, and the total thermal cycle that impurities undergo must be taken into account. Selective doping, as shown in the middle of Fig. 1b, can be achieved using a variety of masking layers such as photoresist, polysilicon, or SiO_2 . The deposition of materials can be achieved through the CVD methods described in Chapter 6 or the physical deposition techniques covered in Chapter 9. The choice of material will be determined by the particular application and function, the most common materials being silicon oxides, polysilicon, aluminum, and silicon nitride. Some deposited materials can be deposited selectively, as shown in the bottom of Fig. 1b, which may give an advantage for some applications. The epitaxial growth of single-crystal silicon can also be deposited uniformly or selectively. Selective epitaxial growth is not used commonly in ICs but has many advantages that may be useful for future devices.

11.2.2 Integrating the Process Steps

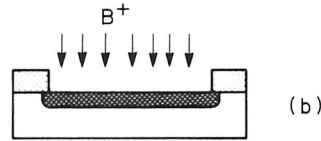
The process of building a succession of layers described in the previous section requires careful consideration of each layer's relative position to the others. A simple example of this process of building layers is shown in Fig. 2, which illustrates the sequence of forming a simple MOS capacitor out of four successive layers. The initial oxidation (Fig. 2a) forms an insulating layer between the final aluminum layer and the substrate. The oxide is then patterned and etched to form the active region of the capacitor. The active region of the capacitor consists of a boron-doped p-type region of the silicon, formed by ion-implanting boron into the silicon exposed by the etching of the oxide, as shown in Fig. 2b. The oxide acts as an implant mask in this step, effectively blocking the boron from doping the silicon under the oxide. The implant energy must be carefully chosen to ensure that the range of the ions in the oxide is not sufficient to penetrate to the silicon. An important feature of this particular step is that the implant is self-aligned to the oxide that serves as the isolation region of the final device. This self-aligned

MOS CAPACITOR

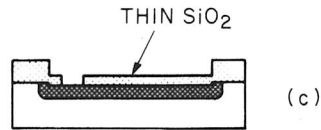
GROW 4000Å OXIDE ON
N-TYPE SILICON MATERIAL



PATTERN AND ETCH OXIDE, THEN
ION IMPLANT 50 KeV BORON
TO FORM P⁺ REGION.



GROW THIN OXIDE (200Å),
PATTERN AND ETCH OXIDE TO
FORM CONTACT.



DEPOSIT 5000Å ALUMINUM,
PATTERN AND ETCH ALUMINUM.

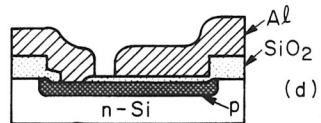


FIGURE 2.

Steps to form an MOS capacitor.

feature is very important when device miniaturization is considered, and it will be covered in more detail with some of the VLSI technologies discussed later in this chapter.

The subsequent steps of growing and patterning a thin oxide, shown in Fig. 2c, and depositing and patterning aluminum (Fig. 2d) illustrates another important consideration of integrating layers—alignment. The capacitor that results from this sequence of steps will only work properly if the individual layers are isolated from each other except where an intentional contact is made. Therefore, if the aluminum over the thin oxide is misaligned so that it makes an electrical contact to the p region, the device will not function. This alignment consideration is one of the limiting factors in any device miniaturization and will be covered in detail in the next section.

11.2.3 Miniaturizing VLSI Circuits

In this section we will discuss some of the limitations to the efforts to reduce the size of ICs. The discussion will be restricted to some basic guides for reducing feature sizes and increasing density. Another aspect of miniaturization involves the way individual transistor characteristics change as the dimensions change. This topic will be covered in later sections, after the particular technologies are introduced.