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(54) ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE AND FABRICATION METHOD THEREOF

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(57) **ABSTRACT**

An organic light emitting diode (OLED) display device and a fabrication method thereof are provided. In the OLED display device, when an existing power wiring using a metal used for a data wiring is divided based on a common electrode marginal region as a boundary so as to be used as a wiring as well as as the power wiring, the reduced width of the wiring is compensated for by increasing the thickness of the wiring by using a metal for an anode or a cathode, thus reducing the left and right bezel widths.

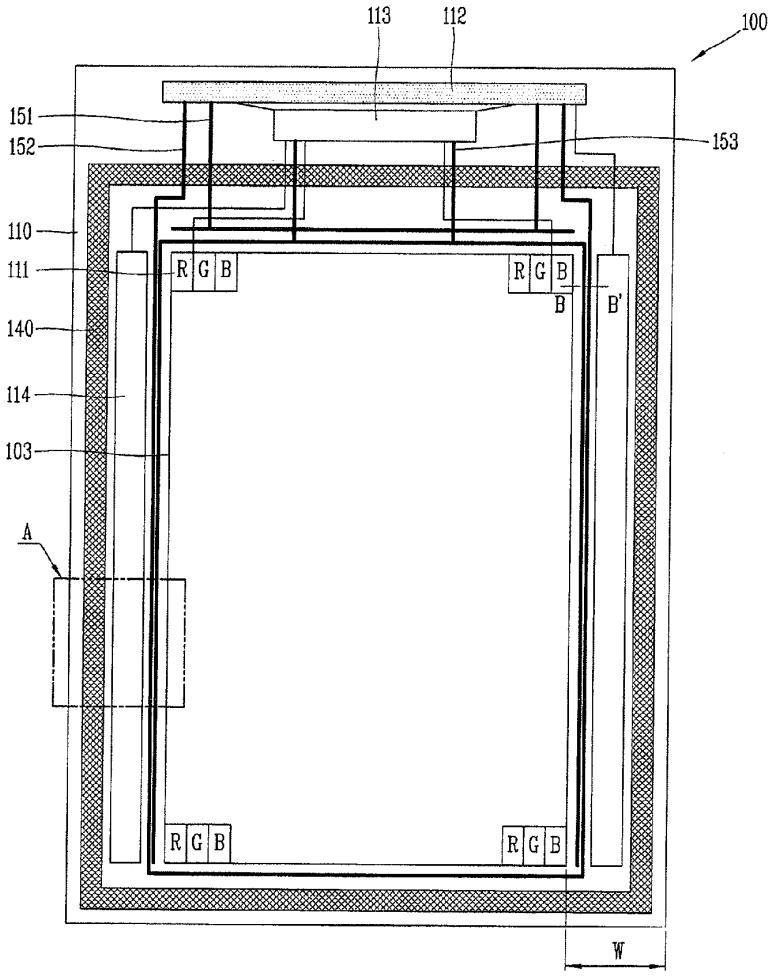


FIG. 1
RELATED ART

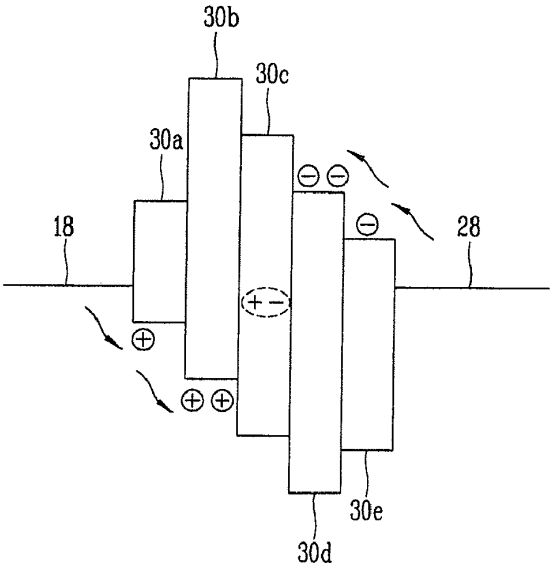



FIG. 2
RELATED ART

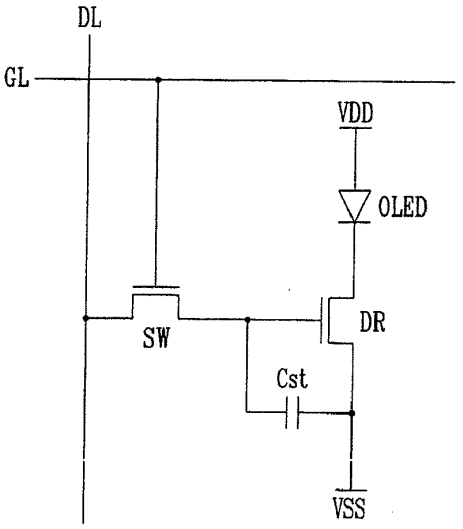


FIG. 3
RELATED ART

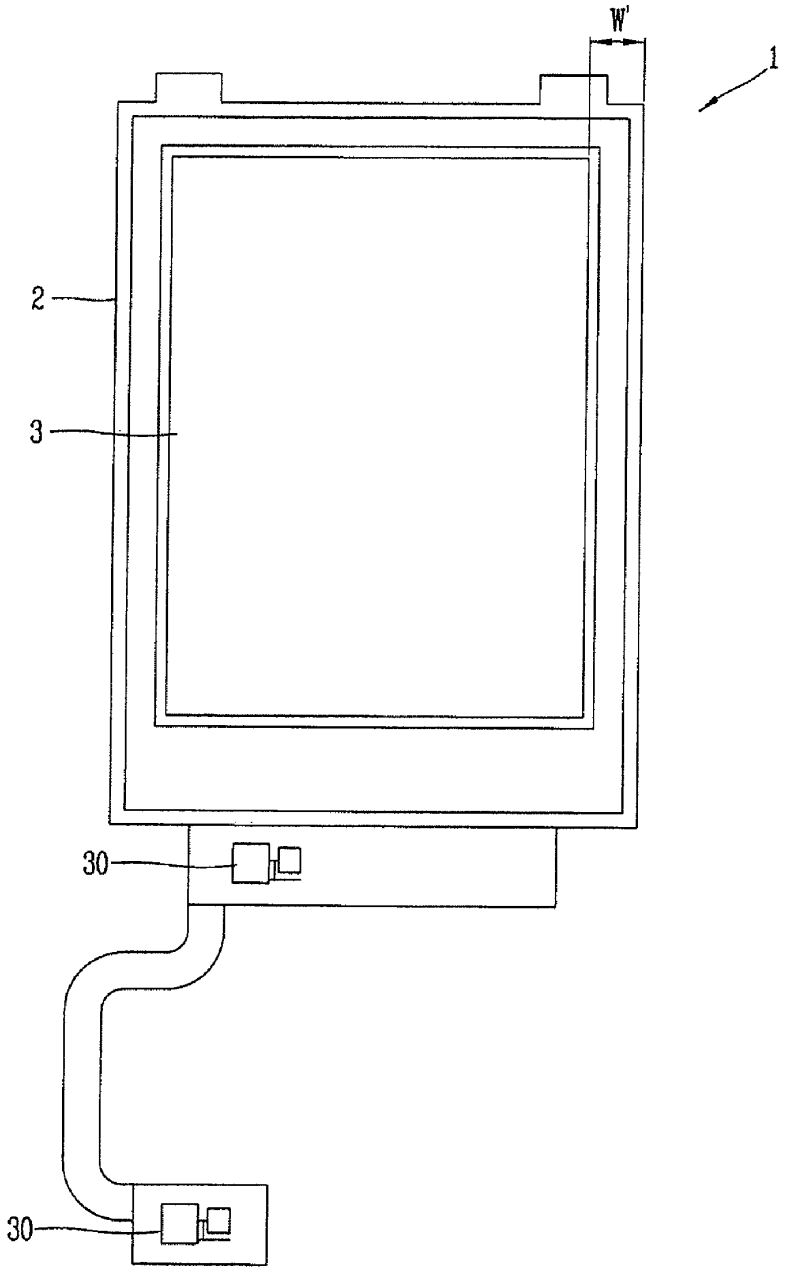


FIG. 4
RELATED ART

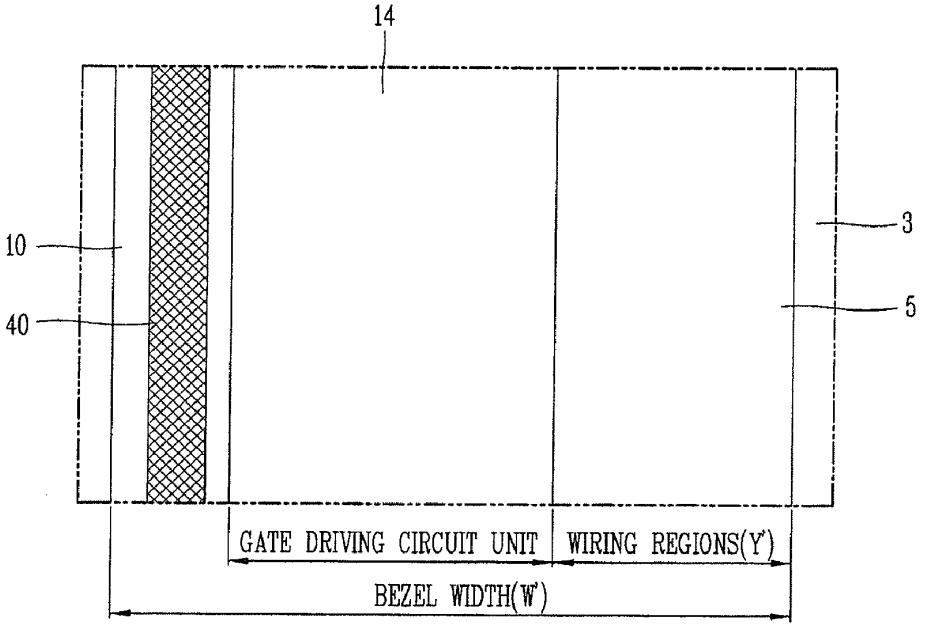


FIG. 5

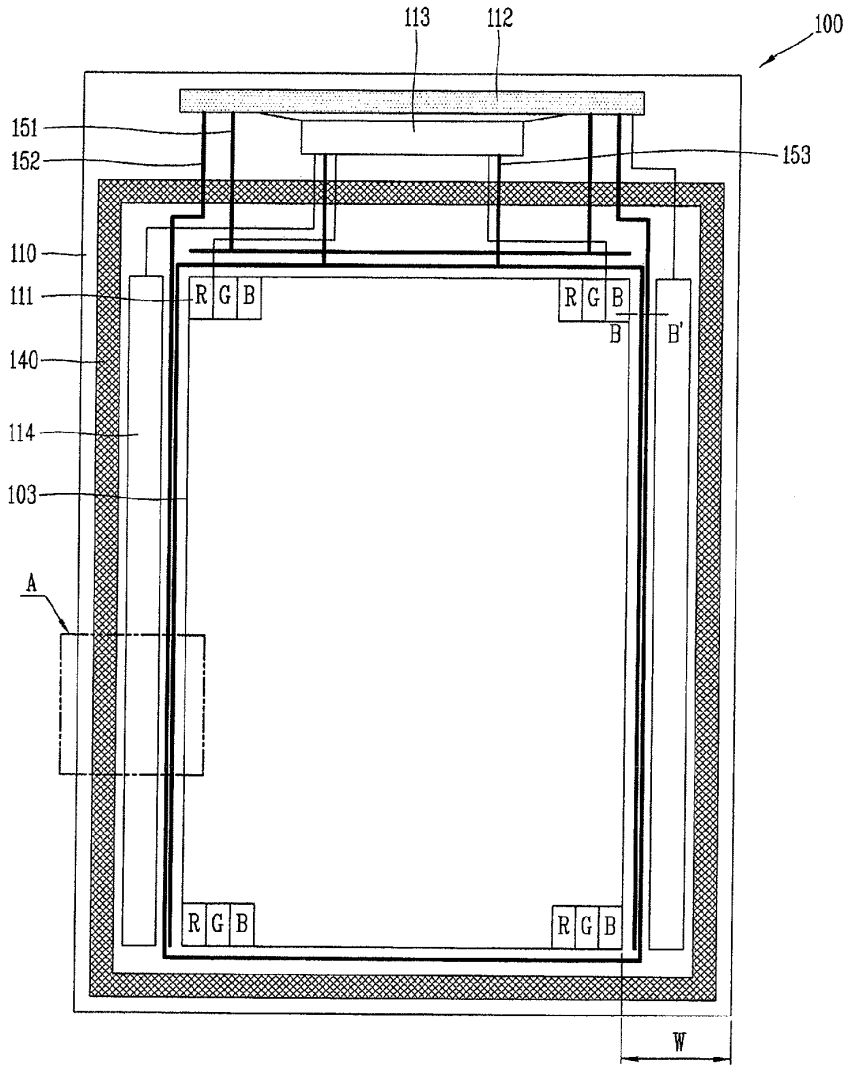


FIG. 6

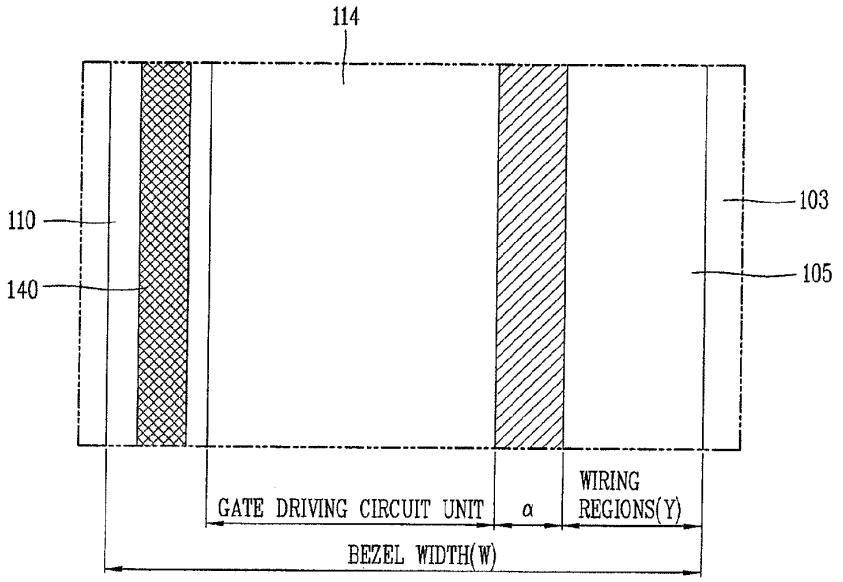

114
110
140
103
105
GATE DRIVING CIRCUIT UNIT
α
WIRING
REGIONS(Y)
BEZEL WIDTH(W)

FIG. 7

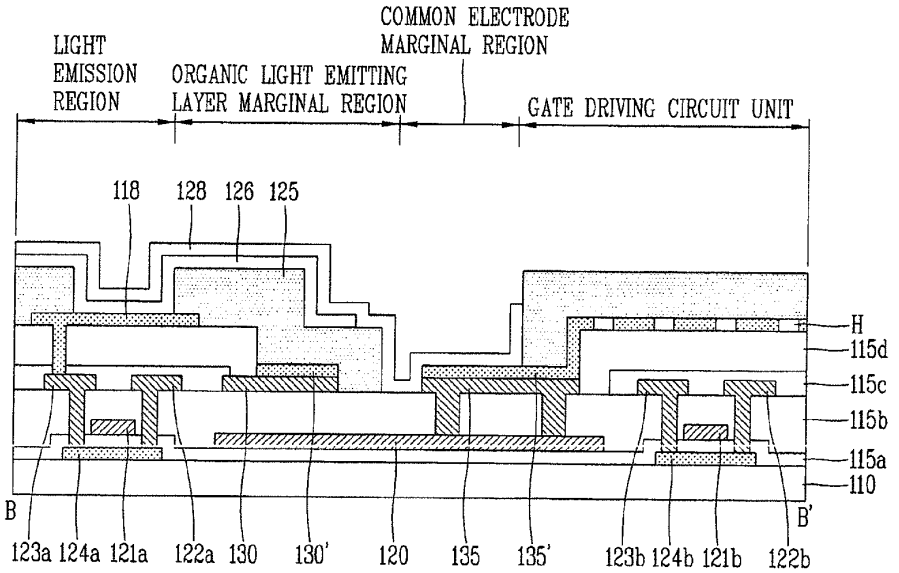

LIGHT
EMISSION
REGION
ORGANIC LIGHT EMITTING
LAYER MARGINAL REGION
COMMON ELECTRODE
MARGINAL REGION
GATE DRIVING CIRCUIT UNIT
118
128
126
125
H
115d
115c
115b
115a
110
B
B'
123a
124a
121a
122a
130
130'
120
135
135'
123b
124b
121b
122b

FIG. 8A

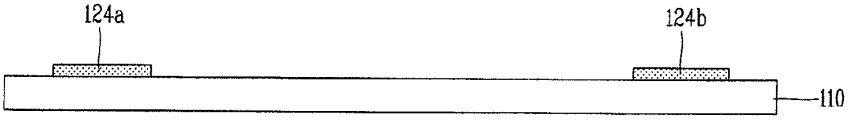



FIG. 8B

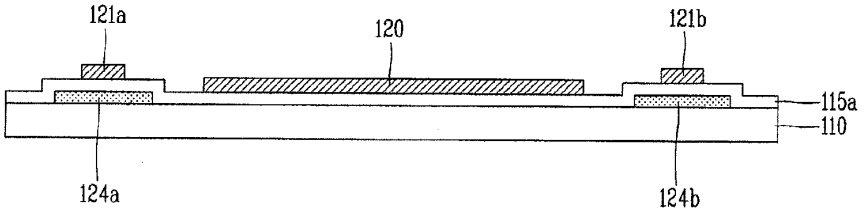



FIG. 8C

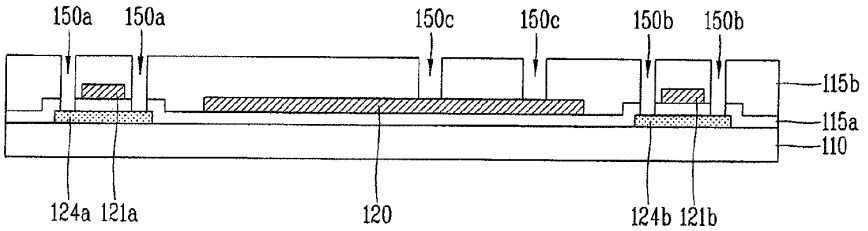



FIG. 8D

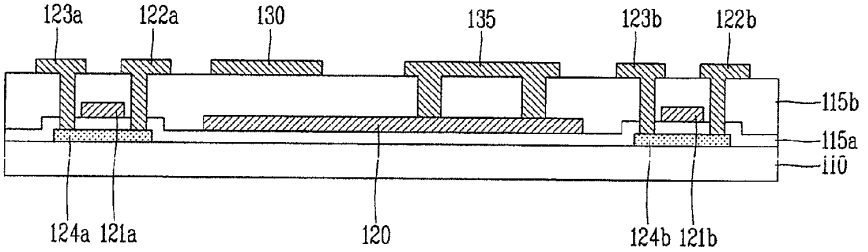


FIG. 8E

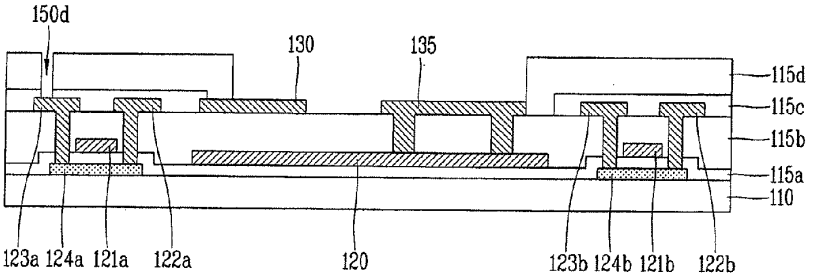



FIG. 8F

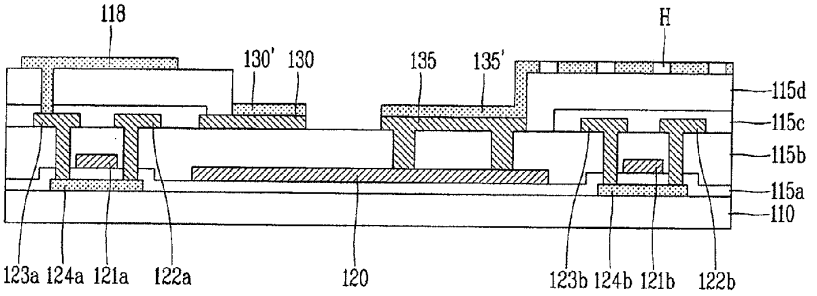



FIG. 8G

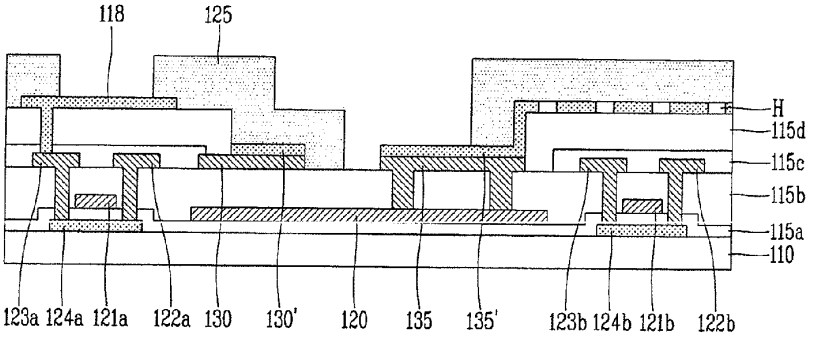


FIG. 8H

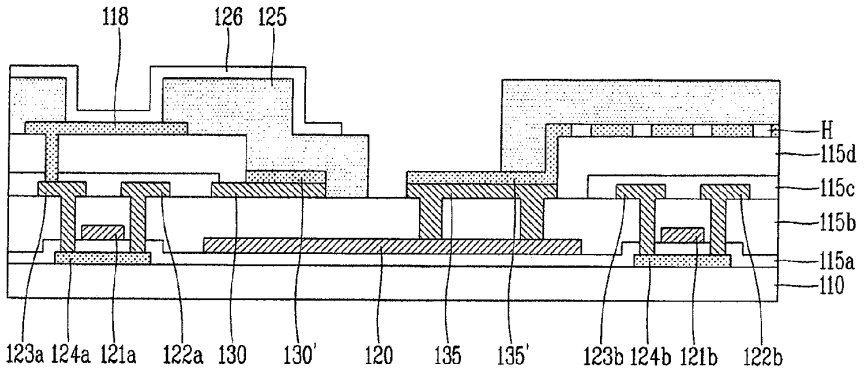
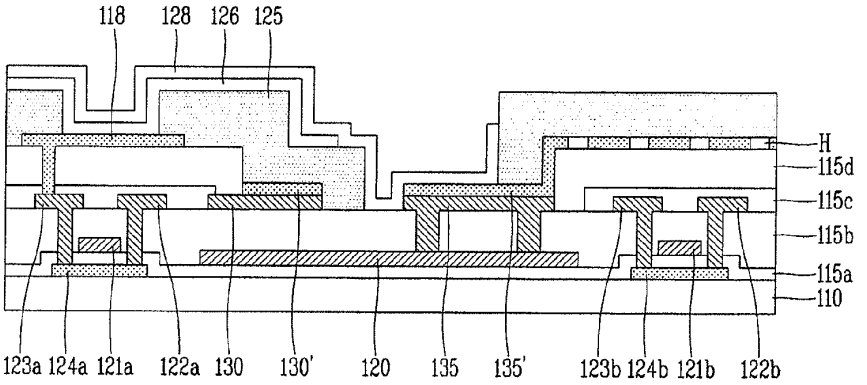

118
126
125
H
115d
115c
115b
115a
110
123a
124a
121a
122a
130
130'
120
135
135'
123b
124b
121b
122b

FIG. 8I


118
128
126
125
H
115d
115c
115b
115a
110
123a
124a
121a
122a
130
130'
120
135
135'
123b
124b
121b
122b

# ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE AND FABRICATION METHOD THEREOF

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims the benefit of earlier filing data and right of priority to Korean Patent Application No. 10-2010-0134890, filed on Dec. 24, 2010, the contents of which is hereby incorporated by reference for all purposes as if fully set forth herein in its entirety.

## BACKGROUND OF THE INVENTION

**[0002]** 1. Field of the Invention

**[0003]** The present invention relates to an organic light emitting diode (OLED) display device and a fabrication method thereof and, more particularly, to an OLED display device capable of reducing a bezel width therein and a fabrication method thereof.

**[0004]** 2. Description of the Related Art

**[0005]** As the consumer's interest in information displays is growing and the demand for portable (mobile) information devices is increasing, research into and commercialization of light and thin flat panel displays ("FPD"), which substitute cathode ray tubes (CRTs), the conventional display devices, has been actively ongoing.

**[0006]** In the FPD field, a liquid crystal display (LCD), which is lighter and consumes less power, has come to prominence so far. However, the LCD is a light receiving device, rather than a light emitting device, having shortcomings in terms of brightness, a contrast ratio, a viewing angle, and the like, so a novel display device that may be able to overcome such shortcomings has been actively developed.

**[0007]** An organic light emitting diode (OLED) display device, one of novel display devices, is self-emissive, having excellent viewing angle and contrast ratio, and since it does not require a backlight, the OLED display device is lighter and thinner and is advantageous in terms of power consumption. In addition, the OLED display device has advantages in that it is available for DC low voltage driving and has a faster response speed, and also is advantageous in terms of fabrication costs.

**[0008]** Unlike the LCD or a plasma display panel (PDP), a fabrication process of the OLED display device includes only a deposition and encapsulation process, which is, thus, simple. Also, when the OLED display device is driven according to an active matrix scheme having a thin film transistor (TFT) as a switching element in each pixel, although a low current is applied, the same luminance can be obtained, so the LED display device has an advantage in that it can consume less power and high precision and resolution, and can be increased in size.

**[0009]** A basic structure and operational characteristics of the OLED display device will be described in detail with reference to the accompanying drawings.

**[0010]** FIG. **1** is a diagram explaining a light emission principle of a related art OLED display device.

**[0011]** As shown in FIG. **1**, the related art OLED display device includes an OLED. The OLED includes organic compound layers **30***a*, **30***b*, **30***c*, **30***d*, and **30***e* formed between an anode **18** as a pixel electrode and a cathode **28** as a common electrode.

**[0012]** The organic compound layers **30***a*, **30***b*, **30***c*, **30***d*, and **30***e* include a hole injection layer **30***a*, a hole transport layer **30***b*, an emitting layer **30***c*, an electron transport layer **30***d*, and an electron injection layer **30***e*.

**[0013]** When a driving voltage is applied to the anode **18** and the cathode **28**, holes which have passed through the hole transport layer **30***b* and electrons which have passed through the electron transport layer **30***d* move to the emission layer **30***c* to form excitors, and as a result, the emission layer **30***c* emits visible rays.

**[0014]** In the OLED display device, pixels having the OLED having the foregoing structure, are arranged in a matrix form and selectively controlled by a data voltage and a scan voltage, thus displaying an image.

**[0015]** The OLED display device is divided into a passive matrix display device and an active matrix display device using TFTs as switching elements. Among them, in the active matrix display device, the TFTs are selectively turned on to select pixels and emission of pixels is maintained by the voltage maintained in a storage capacitor.

**[0016]** FIG. **2** is an equivalent circuit diagram of a single pixel in the related art OLED display device. Specifically, FIG. **2** is an equivalent circuit diagram of a related art 2T1C pixel (including two transistors and one capacitor) in the active matrix OLED display device.

**[0017]** With reference to FIG. **2**, the pixel of the active matrix OLED display device includes an OLED, a data line DL and a gate line GL which cross each other, a switching TFT SW, a driving TFT DR, and a storage capacitor Cst.

**[0018]** Here, the switching TFT SW is turned on in response to a scan pulse from the gate line GL, thus electrically connecting a current path between a source electrode and a drain electrode thereof. During an ON-time period of the switching TFT SW, a data voltage from the data line DL is applied to a gate electrode of the driving TFT DR and the gate storage capacitor Cst through a source electrode and a drain electrode of the switching TFT SW.

**[0019]** Here, the driving TFT DR controls a current flowing through the OLED according to the data voltage applied to the gate electrode thereof. The storage capacitor Cst stores the voltage between the data voltage and a low potential power source voltage VSS, and then, uniformly maintains during one frame period.

**[0020]** FIG. **3** is a view showing an example of a usage state of the related art OLED display device.

**[0021]** With reference to FIG. **3**, a related art OLED display device **1** includes a light emission region **3** including an OLED and a circuit unit **30** electrically connected to a printed circuit board (PCB) and transferring a signal transferred from the PCB to the light emission region **3**.

**[0022]** The light emission region **3** outputs a display image according to a signal received from the PCB through the circuit unit **30**.

**[0023]** The related art OLED display device **1** includes an external appearance glass **2** attached on a front surface thereof so as to be used in a mobile communication terminal or an information terminal such as a digital TV, a computer, or the like, and in general, a space between an outer side of the external appearance glass **2** and the light emission region **3** is called a bezel width W'.

**[0024]** FIG. **4** is a plan view schematically showing the bezel region in the OLED display device illustrated in FIG. **3**.

**[0025]** With reference to FIG. **4**, in the related art OLED display device, the light emission region **3** displaying display information is formed on a substrate **10**, and a plurality of pixels (not shown) of an OLED are formed in the light emission region **3**.

**[0026]** Here, a gate driving circuit unit **14** is positioned on the side of the light emission region **3** and electrically connected to the PCB (not shown0 to receive an external signal.

**[0027]** A sealant **40** is formed at an outer side of the gate driving circuit unit **14** to protect the gate driving circuit unit **14** and the light emission region **3** against impurities such as external moisture, oxygen, and the like.

**[0028]** A wiring region **5** in which a power (GND) wiring (not shown), an ON/OFF switch wiring (not shown), a reference wiring (not shown), or the like, are disposed is positioned between the gate driving circuit unit **14** and the light emission region **3**.

**[0029]** As mentioned above, the space between an outer side of the substrate **10** and the light emission region **3** is called the bezel width W', and when the bezel width W' is large, dead spaces of the information terminal such as a mobile phone, or the like, is increased, defiling the outer appearance or design.

**[0030]** In particular, when the OLED display device is fabricated, a horizontal power wiring is led into the light emission region **3** by using portions of the left and right bezels. Here, in case of configuring a power source led in the horizontal direction using the left and right bezels, the additionally wiring region **5** is required in the bezel region in order to supply power, resulting in an increase in the bezel width W'.

**[0031]** Namely, as the OLED display device is advancing toward high resolution, layout of the power wiring such that the power wiring is led into the light emission region **3** in a vertical direction is not possible, so the power wiring is required to be designed in a horizontal direction within the pixel. Here, however, when the power wiring led into the light emission region **3** is horizontally disposed, the power wiring should be designed in the left and right wiring regions **5** by using a metal for a data wiring or a gate wiring, increasing the width Y' of the wiring regions **5**, namely, the bezel width W'.

## SUMMARY OF THE INVENTION

**[0032]** An aspect of the present invention provides an organic light emitting diode (OLED) display device having a reduced bezel width and a fabrication method thereof.

**[0033]** According to an aspect of the present invention, there is provided an organic light emitting diode (OLED) display device including: a light emission region displaying display information; a plurality of pixels formed in the light emission region; a data driving circuit unit formed on at least one side of the light emission region and a gate driving circuit unit formed on at least one side of the light emission region; a wiring region placed between the gate driving circuit unit and the light emission region and having a plurality of wirings disposed therein; first and second power wirings disposed in the wiring region and made of a metal used for a data wiring; and a first power wiring pattern made of a metal used for an anode and connected to the first power wiring and a second power wiring pattern made of the metal used for an anode and connected to the second power wiring.

**[0034]** The first power wiring pattern may be positioned on the first power wiring, and the second power wiring pattern may be positioned on the second power wiring.

**[0035]** The wirings formed in the wiring region may include a power wring, an ON/OFF switch wiring or a reference wiring, and supply a signal or power to the pixels of the light emission region.

**[0036]** The organic light emitting diode (OLED) display device may further include: a dummy wiring disposed in the wiring region and made of a metal used for a gate wiring.

**[0037]** The dummy wiring may be electrically connected to the first power wiring or the second power wiring.

**[0038]** According to another aspect of the present invention, there is provided a method for an organic light emitting diode (OLED) display device including: providing a substrate divided into a light emission region outputting an image and a wiring region positioned at an outer side of the light emission region and having a plurality of wirings formed therein; forming a thin film transistor (TFT) on the substrate; forming first and second power wirings with metal used for a data wiring on the substrate of the wiring region; forming a planarization film on the substrate with the TFT and the first and second power wirings formed thereon; forming an anode on the planarization film, forming a first power wiring pattern on the first power wiring by using a metal used for the anode such that the first power wiring pattern is connected to the first power wiring, and forming a second power wiring pattern on the second power wiring by using the metal used for the anode such that the second power wiring pattern is connected to the second power wiring; forming a barrier rib demarcating a pixel region on the substrate with the anode, the first power wiring pattern and the second power wiring pattern formed thereon; forming an organic light emitting layer on the substrate with the barrier rib formed thereon; and forming a cathode on the organic light emitting layer.

**[0039]** The wirings formed in the wiring region may include a power wring, an ON/OFF switch wiring or a reference wiring, and supply a signal or power to the pixels of the light emission region.

**[0040]** The method may further include: forming a dummy wiring with a metal used for a gate wiring on the substrate of the wiring region.

**[0041]** The dummy wiring may be electrically connected to the first power wiring or the second power wiring.

**[0042]** The barrier rib may be formed to cover the first power wiring pattern and expose the second power wiring pattern.

**[0043]** The metal used for the cathode may be formed to be connected to the exposed second power wiring pattern.

**[0044]** According to embodiments of the present invention, in the OLED display device and the fabrication method thereof, when the existing power wiring using the metal for a data wiring is divided based on a common electrode marginal region as a boundary so as to be used as a wiring as well as as the power wiring, and here, the reduced width of the wiring is compensated for by increasing the thickness of the wiring by using a metal for an anode or a cathode, thus reducing the left and right bezel widths. Thus, since the bezel widths are reduced, the use of an unnecessary space is reduced without defiling the outer appearance or design.

**[0045]** The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0046]** FIG. **1** is a diagram explaining a light emission principle of a related art organic light emitting diode (OLED) display device.

**[0047]** FIG. **2** is an equivalent circuit diagram of a single pixel in the related art OLED display device.

**[0048]** FIG. **3** is a view showing an example of a usage state of the related art OLED display device.

**[0049]** FIG. **4** is a plan view schematically showing a bezel region in the OLED display device illustrated in FIG. **3**.

**[0050]** FIG. **5** is a plan view schematically showing an internal configuration of an OLED display device according to an embodiment of the present invention.

**[0051]** FIG. **6** is a plan view schematically showing a bezel region in the OLED display device illustrated in FIG. **5**.

**[0052]** FIG. **7** is a sectional view taken along line B-B' in the OLED display device illustrated in FIG. **5**.

**[0053]** FIGS. **8**A through **8**I are sectional views sequentially showing a method for fabricating the OLED display device illustrated in FIG. **7**.

## DETAILED DESCRIPTION OF THE INVENTION

**[0054]** An OLED display device and a fabrication method according to embodiments of the present invention will be described in detail with reference to the accompanying drawings.

**[0055]** FIG. **5** is a plan view schematically showing an internal configuration of an OLED display device according to an embodiment of the present invention.

**[0056]** FIG. **6** is a plan view schematically showing a bezel region in the OLED display device illustrated in FIG. **5**. Specifically, FIG. **6** is an enlarged view of portion 'A'.

**[0057]** With reference to FIGS. **5** and **6**, the OLED display device **100** according to an embodiment of the present invention includes a light emission region **103** formed on a certain substrate **110** to display display information on, and a plurality of pixels **111** of an OLED are formed in the light emission region **103**.

**[0058]** Here, a data driving circuit unit **113** is formed at an upper side of the light emission region **103**, and gate driving units **114** are formed at left and right sides. The data driving circuit unit **113** and the gate driving circuit units **114** are electrically connected to a PCB **112** to receive external signal.

**[0059]** A sealant **140** is formed at an outer side of the gate driving circuit unit **114** to protect the gate driving circuit units **114** and the light emission region **103** from impurities such as external moisture, oxygen, or the like.

**[0060]** A wiring region **105** is positioned between the gate driving circuit unit **114** and the light emission region **103**. A power wiring **151**, an ON/OFF switch wiring (not shown), a reference wiring **153**, and the like, are disposed on the wiring region **105**.

**[0061]** Here, the power wiring **151** is a wiring connected to a reference voltage of a panel, and the ON/OFF switch wiring serves to turn on or turn off the switching TFT in changing scanning during driving.

**[0062]** Also, the reference wiring **153** is a wiring connected to a reference voltage of an input data signal, and reference numeral **152** denotes a data wiring.

**[0063]** As mentioned above, the space between an outer side of the substrate **110** and the light emission region **103** is called a bezel width (W), and when the bezel width W is large, dead spaces of the information terminal such as a mobile phone, or the like, is increased, defiling the outer appearance or design.

**[0064]** As the OLED display device **100** is advancing toward high resolution, layout of the power wiring led into the light emission region **3** in a vertical direction is not possible, so the power wiring is required to be designed in a horizontal direction within the pixel. Here, in the related art, when the power wiring led into the light emission region **3** is horizontally applied, the power wiring should be designed in the left and right wiring regions **5** by using a metal used for a data wiring or a gate wiring, increasing the bezel width W. In an embodiment of the present invention, the existing power wiring **151** is divided based on a common electrode marginal region as a boundary so as to be used as a wiring (not shown) as well as as the power wiring, and here, the reduced width of the wiring is compensated for by increasing the thickness of the wiring by using a metal used for an anode or a cathode, thus reducing the left and right bezel widths.

**[0065]** Namely, in the OLED display device **100**, the wiring disposed in the bezel region is used as a power source for operating the pixels **111** within the light emission region **103**, and in this case, when the metal for a data wiring or a gate wiring below the anode is used, the metal fixedly occupies the bezel region.

**[0066]** Thus, in an embodiment of the present invention, the existing power wiring **151** is divided based on the common electrode marginal region as a boundary so as to be used as a wiring as well as as the power wiring, and here, the reduced width of the wiring is compensated for by increasing the thickness of the wiring by using a metal used for an anode or a cathode formed in the bezel region, thus reducing the width Y of the wiring region **105**, namely, the bezel width W. In this case, since power of the divided wirings is open to each other (namely, each power is not connected) by the common electrode based on the common electrode marginal region as a boundary, the separated power can be used. Thus, power used in the light emission region **103** can be supplied without having to add a bezel region for a power wiring.

**[0067]** FIG. **7** is a sectional view taken along line B-B' in the OLED display device illustrated in FIG. **5**. In FIG. **7**, the light emission region, the organic light emitting layer marginal region, the common electrode marginal region, and the gate driving circuit unit are sequentially illustrated from the left of the drawing.

**[0068]** As shown in FIG. **7**, in the OLED display device according to an embodiment of the present invention, a first active layer **124***a* and a second active layer **124***b*, each being made of polycrystalline silicon, are formed on the substrate **110** made of an insulating material such as transparent glass, plastic, or the like.

**[0069]** Here, for the sake of explanation, it is assumed that a switching TFT and a driving TFT are formed in the light emission region and a gate driving TFT is formed in the gate driving circuit unit. Namely, for example, the first active layer **124***a* is formed on the substrate **110** of the light emission region and the second active layer **124***b* is formed on the substrate **110** of the gate driving circuit unit.

**[0070]** Here, in the embodiment of the present invention, the case in which the first active layer **124***a* and the second active layer **124***b* are made of polycrystalline silicon is taken as an example, but the present invention is not limited thereto, and the first active layer **124***a* and the second active layer **124***b* may be made of hydrogenated amorphous silicon or oxide semiconductor.

**[0071]** A gate insulating layer **115***a* made of silicon nitride (SiNx), silicon oxide ($SiO_2$), or the like, is formed on the substrate **110** including the first active layer **124***a* and the second active layer **124***b*, and a first gate electrode **121***a*, a gate line (not shown), a storage electrode (not shown), and a second gate electrode **121***b* (hereinafter, the first electrode **121***a*, the gate line, the storage electrode, and the second gate electrode **121***b* will be collectively called a 'gate wiring') are formed on the gate insulating layer **115***a*.

**[0072]** Here, the first gate electrode **121***a* and the second gate electrode **121***b* are positioned at an upper side of the first active layer **124***a* and the second active layer **124***b*, respectively.

**[0073]** A dummy wiring **120** made of the metal for a gate wiring may be formed in the organic light emitting layer marginal region and the common electrode marginal region. For reference, the organic light emitting layer marginal region and the common electrode marginal region refer to a wiring region.

**[0074]** A first passivation layer **115***b* made of silicon nitride, silicon oxide, or the like, is formed on the substrate **110** on which the first gate electrode **121***a*, the gate line, the storage electrode, and the second gate electrode **121***b* have been formed, and a data line (not shown), a driving voltage line (not shown), first source and drain electrodes **122***a* and **123***a*, and second source and drain electrodes **122***b* and **123***b* (hereinafter, the data line, the driving voltage line, the first source and drain electrodes **122***a* and **123***a*, and the second source and drain electrodes **122***b* and **123***b* will be collectively called a 'data wiring') are formed on the first passivation layer **115***b*.

**[0075]** Here, the first source electrode **122***a* and the drain electrode **123***a* face each other based on the first gate electrode **121***a*, and the second source electrode **122***b* and the second drain electrode **123***b* face each other based on the second gate electrode **121***b*.

**[0076]** Also, the first source and drain electrodes **122***a* and **123***a* are electrically connected to source and drain regions of the first active layer **124***a* through first contact holes, respectively, and the second source and drain electrodes **122***b* and **123***b* are electrically connected to the source and drain regions of the second active layer **124***b* through second contact holes.

**[0077]** Here, a first power wiring **130** and a second power wiring **135**, each being made of metal for a data wiring, may be formed in the organic light emitting layer marginal region and the common electrode marginal region, respectively. The second power wiring **135** may be a reference wiring and may be electrically connected to an underlying dummy wiring **120** through a third contact hole, However, the present invention is not limited thereto and the first power wiring **130** and the dummy wiring **120** may be electrically connected through the third contact hole.

**[0078]** A second passivation film **115***c* made of silicon nitride, silicon oxide, or the like, is formed on the substrate **110** on which the data line, the driving voltage line, the first source and drain electrodes **122***a* and **123***a*, and the second source and drain electrodes **122***b* and **123***b* have been formed, and a planarization film **115***d* made of an organic insulating material such as photoacryl, or the like, is formed on the second passivation film **115***c*.

**[0079]** Here, a fourth contact hole exposing the first drain electrode **123***a* is formed in the planarization film **115***d* and the second passivation film **115***c*, and portions of the planarization film **115***d* and the second passivation film **115***c* in the organic light emitting layer marginal region and the common electrode marginal region are selectively removed to expose the first power wiring **130** and the second power wiring **135**.

**[0080]** A pixel electrode **118** and a connecting electrode (not shown) are formed on the planarization film **115***d*. The pixel electrode **118** and the connecting electrode are made of a transparent conductive material such as indium-tin-oxide (ITO), indium-zinc-oxide (IZO), or the like, or a reflective conductive material such as aluminum, silver, an alloy thereof, or the like.

**[0081]** Here, the pixel electrode **118** as an anode is electrically connected to the first drain electrode **123***a* through the fourth contact hole.

**[0082]** Here, a power wiring pattern **130'** is formed on the first power wiring **130** by using the metal for an anode and a second power wiring pattern **135'** is formed on the second power wiring **135**.

**[0083]** As mentioned above, when a horizontal wiring is led into the light emission region and used, a gap must be present between the first power wiring pattern **130'** and the second power wiring pattern **135'** to separate them.

**[0084]** In this manner, the first power wiring pattern **130'** is formed on the first power wiring **130** and connected to the first power wiring **130**, obtaining an effect that the thickness of the first power wiring **130** is substantially increased. Thus, the width of the wirings can be reduced in case of having the same wiring resistance.

**[0085]** Also, the second power wiring pattern **135'** is formed on the second power wiring **135** and the dummy wiring **120** is formed at a lower side thereof and connected to the second power wiring **135**, obtaining an effect that the thickness of the second power wiring **135** is substantially increased. Thus, the width of the wirings can be reduced in case of having the same wiring resistance.

**[0086]** Here, reference letter H denotes anode holes, and a barrier rib **125** is formed on the substrate **110** on which the pixel electrode **118**, the first power wiring pattern **130'**, and the second power wiring pattern **135'** have been formed.

**[0087]** Here, the barrier rib **125** surrounds the peripheral portions of the pixel electrode **118** like a bank to define an opening, and is made of an organic insulating material or an inorganic insulating material. The barrier **125** may also be made of a photosensitizer including black pigment, and in this case, the barrier rib **125** serves as a light blocking member.

**[0088]** The barrier rib **125** according to an embodiment of the present invention covers the first power wiring pattern **130'** formed in the organic light emitting marginal region and exposes a portion of the second power wiring pattern **135'** formed in the common electrode marginal region, but the present invention is not limited thereto.

**[0089]** A certain organic light emitting layer **126** is formed on the substrate **110** on which the barrier rib **125** has been formed.

**[0090]** Here, the organic light emitting layer **126** may have a multi-layered structure including a light emitting layer emitting light and an auxiliary layer for improving luminous efficiency of the light emitting layer. The auxiliary layer may include an electron transport layer and a hole transport layer for balancing electrons and holes and an electron injection layer and a hole injection layer for strengthening injection of electrons and holes.

**[0091]** A common electrode **128** as a cathode is formed on the organic light emitting layer. Here, the common electrode **128** receives a common voltage and may be made of a reflective conductive material including calcium (Ca), barium (Ba), magnesium (Mg), aluminum (Al), silver (Ag), and the like, or a transparent conductive material such as ITO, IZO, or the like.

**[0092]** A metal for a cathode constituting the common electrode **128** is connected to the exposed portion of the second power wiring pattern **135'**.

**[0093]** In this manner, it is noted that, when the dummy electrodes such as the dummy wiring **120**, the first power wiring pattern **130'**, the second power wiring pattern **135'**, and the like, are used, an effect that the thickness of the power wirings **130** and **135** is substantially increased can be obtained, so the wiring resistance is reduced.

**[0094]** Here, since the wiring resistance is reduced, the width of the power wirings **130** and **135** may be reduced, and a different signal line or wiring may be additionally formed by the reduced width (i.e., 'a' in FIG. **6**).

**[0095]** For example, when the dummy electrodes are used, lateral resistance can be reduced to be about 1/13 in comparison to the case in which the dummy electrodes are not used, and when the dummy electrodes are not used, a wiring region having a width of about 600 μm is required, but when the dummy electrodes are used, only a wiring region having a width of about 550 μm is required. As a result, the remaining 50 μm can be used for a signal line or wiring in a different region.

**[0096]** A method for fabricating the OLED display device according to an embodiment of the present invention configured as described above will be described in detail with reference to the accompanying drawings.

**[0097]** FIGS. **8**A through **8**I are sectional views sequentially showing a method for fabricating the OLED display device illustrated in FIG. **7**. In FIGS. **8**A through **8**I show a case of a method for fabricating the light emission region, the organic light emitting layer marginal region, the common electrode marginal region, and the gate driving circuit unit in order from the left in the drawings, as an example.

**[0098]** As shown in FIG. **8**A, a buffer layer (not shown) and a silicon film are formed on the substrate **110** made of an insulating material such as transparent glass, plastic, or the like.

**[0099]** Here, the buffer layer serves to prevent impurities such as natrium (Na), or the like, present within the substrate **110** from infiltrating into an upper layer during the process.

**[0100]** The silicon film may be made of an amorphous silicon or polycrystalline silicon, but in an embodiment of the present invention, the case in which a TFT is formed by using polycrystalline silicon is taken as an example. Here, the polycrystalline silicon may be formed by depositing amorphous silicon on the substrate **110** and then performing various crystallization methods. This will be described as follows.

**[0101]** First, the amorphous silicon can be deposited according to various methods. Typical methods of depositing the amorphous silicon include a low pressure chemical vapor deposition (LPCVD) and a plasma enhanced chemical vapor deposition (PECVD).

**[0102]** Methods for crystallizing the amorphous silicon include a solid phase crystallization (SPC) method which thermally treats amorphous silicon in a high temperature furnace and an eximer laser annealing (ELA) method using a laser.

**[0103]** As the laser crystallization, the ELA using laser having a pulse form is commonly used, and recently, a sequential lateral solidification (SLS) which remarkably improves the crystallization characteristics by growing grains in a horizontal direction has been studied.

**[0104]** Thereafter, the silicon film is selectively removed through a photolithography process to form the first active layer **124***a* and the second active layer **124***b* made of the polycrystalline silicon.

**[0105]** Here, for the sake of explanation, it is assumed that the switching TFT and the driving TFT are formed in the light emission region and the gate driving TFT is formed in gate driving circuit unit. Namely, for example, the first active layer **124***a* is formed on the substrate **110** of the light emitting region and the second active layer **124***b* is formed on the substrate **110** of the gate driving circuit unit.

**[0106]** Here, as mentioned above, in an embodiment of the present invention, the case in which the first active layer **124***a* and the second active layer **124***b* are made of polycrystalline silicon is taken as an example, but the present invention is not limited thereto and the first active layer **124***a* and the second active layer **124***b* may be made of hydrogenated amorphous silicon or oxide semiconductor.

**[0107]** Meanwhile, when the first active layer **124***a* and the second active layer **124***b* are made of hydrogenated amorphous silicon, n+ amorphous silicon may be deposited along with amorphous silicon and patterned to form a resistive contact member, and in this case, a TFT may be formed to have a top gate structure, instead of a coplanar structure. In this manner, the present invention can be applicable regardless of the material constituting the first active layer **124***a* and the second active layer **124***b* and the corresponding structure of the TFT.

**[0108]** Next, as shown in FIG. **8**B, the gate insulating layer **115***a* made of silicon nitride, silicon oxide, or the like, is formed on the substrate **110** with the first active layer **124***a* and the second active layer **124***b* formed thereon to form the first gate electrode **121***a*, a gate line (not shown), a storage electrode (not shown), and the second gate electrode **121***b* on the gate insulating layer **115***a*.

**[0109]** Here, the first gate electrode **121***a*, the gate line, the storage electrode, and the second gate electrode are formed by depositing a first conductive film on the entire surface of the substrate **110** and selectively patterning the first conductive film through a photolithography process.

**[0110]** Here, the first conductive film may be made of a low-resistivity opaque conductive material such as aluminum-based metal such as aluminum (Al), an aluminum alloy, etc., silver-based metal such as silver (Ag), a silver alloy, etc., a copper-based metal such as copper (Cu), a copper alloy, etc., molybdenum-based metal such as molybdenum (Mo), a molybdenum alloy, etc., chromium (Cr), tantalum (Ta), titanium (Ti), and the like. Also, the first conductive film may have a multilayered structure including two conductive films each having different physical qualities. When the first conductive film has a multilayered structure, one conductive film may be made of metal of low resistivity, for example, aluminum-based metal, silver-based metal, copper-based metal, or the like, capable of reducing signal delay or a voltage drop, and the other conductive film may be made of a different material, which has excellent physical, and chemical electrical contact characteristics with ITO and IZO, e.g., molybdenum-based metal, chromium, titanium, tantalum, or the like.

**[0111]** A lateral face (or the side) of each of the first gate electrode **121***a*, the gate line, the storage electrode, and the second gate electrode **121***b* may be sloped toward the surface of the substrate **110**, and in this case, the slope angle may range from 30° to 80°.

**[0112]** The first gate electrode **121***a* and the second gate electrode **121***b* are disposed on the first active layer **124***a* and the second active layer **124***b*, respectively.

**[0113]** Here, as mentioned above, the dummy wiring **120** made of the metal for a gate wiring may be formed in the organic light emitting layer marginal region and the common electrode marginal region.

**[0114]** Next, as shown in FIG. **8**C, the first passivation film **115***b* made of silicon nitride, silicon oxide, or the like, is formed on the entire surface of the substrate **110** with the first gate electrode **121***a*, the gate line, the storage electrode, and the second gate electrode **121***b* formed thereon, and the first passivation film **115***b* and the gate insulating film **115***a* are selectively removed through a photolithography process to form the first contact hole **150***a* exposing the source and drain regions of the first active layer **124***a* and the second contact hole **150***b* exposing the source and drain regions of the second active layer **124***b*.

**[0115]** Also, the first passivation film **115***b* is selectively removed through the photolithography process to form the third contact hole **150***c* exposing the dummy wiring **120**.

**[0116]** And then, as shown in FIG. **8**D, a second conductive film is formed on the entire surface of the substrate **110** with the first passivation film **115***b* formed thereon, and then, selectively removed through a photolithography process to form the data line (not shown) formed of the second conductive film, the driving voltage line (not shown), the first source and drain electrodes **122***a* and **123***a*, and the second source and drain electrodes **122***b* and **123***b*.

**[0117]** Here, the first source electrode **122***a* and the first drain electrode **123***a* face each other based on the first gate electrode **121***a*, and the second source electrode **122***b* and the second drain electrode **123***b* face each other based on the second gate electrode **121***b*.

**[0118]** Also, the first source and drain electrodes **122***a* and **123***a* are electrically connected to the source and drain regions of the first active layer **124***a* through the first contact hole, and the second source and drain electrodes **122***b* and **123***b* are electrically connected to the source and drain regions of the second active layer **124***b* through the second contact hole.

**[0119]** Here, the first power wiring **130** and the second power wiring **135**, each being made of the metal for a data wiring, may be formed in the organic light emitting layer marginal region and the common electrode marginal region, respectively. The second power wiring **135** may be a reference wiring and may be electrically connected to the underlying dummy wiring **120** through the third contact hole. However, the present invention is not limited thereto, and the first power wiring **130** may be electrically connected to the dummy wiring **120** through the third contact hole.

**[0120]** Here, the second conductive film may be made of a low-resistivity opaque conductive material such as aluminum-based metal such as aluminum (Al), an aluminum alloy, etc., silver-based metal such as silver (Ag), a silver alloy, etc., a copper-based metal such as copper (Cu), a copper alloy, etc., molybdenum-based metal such as molybdenum (Mo), a molybdenum alloy, etc., chromium (Cr), tantalum (Ta), titanium (Ti), and the like. Also, the first conductive film may have a multilayered structure including two conductive films each having different physical qualities. When the first conductive film has a multilayered structure, one conductive film may be made of metal of low resistivity, for example, aluminum-based metal, silver-based metal, copper-based metal, or the like, capable of reducing signal delay or a voltage drop, and the other conductive film may be made of a different material, which has excellent physical, and chemical electrical contact characteristics with ITO and IZO, e.g., molybdenum-based metal, chromium, titanium, tantalum, or the like.

**[0121]** The lateral face of each of the data line, the driving voltage line, the first source and drain electrodes **122***a* and **123***a*, and the second source and drain electrodes **122***b* and **123***b* may be sloped to the surface of the substrate **110** at about 30° to 80°.

**[0122]** Thereafter, as shown in FIG. **8**E, the second passivation film **115***c* made of silicon nitride, silicon oxide, or the like, is formed on the entire surface of the substrate **110** with the data line, the driving voltage line, the first source and drain electrodes **122***a* and **123***a*, the second source and drain electrodes **122***b* and **123***b*, and the first power wiring **130** and the second power wiring **135** formed thereon, and then, the polarization film **115***d* made of an organic insulating material such as photo acryl is formed on the second passivation film **115***c*.

**[0123]** Thereafter, the planarization film **115***d* and the second passivation film **115***c* are selectively removed through a photolithography process to form a fourth contact hole **150***d*, and, meanwhile, the planarization film **115***d* and the second passivation film **115***c* in the organic light emitting layer marginal region and the common electrode marginal region are selectively removed to expose the first power wiring **130** and the second power wiring **135**.

**[0124]** And then, as shown in FIG. **8**F, a third conductive film is deposited on the entire surface of the substrate **110** with the polarization film **115***d* formed thereon, and then, selectively removed through a photolithography to form the pixel electrode **118** and the connection electrode (not shown) formed of the third conductive film.

**[0125]** Here, the third conductive film may be made of a transparent conductive material such as ITO, IZO, or the like.

**[0126]** Also, the pixel electrode **118** as an anode is electrically connected to the first drain electrode **123***a* through the fourth contact hole.

**[0127]** Here, the first power wiring pattern **130'** is formed on the first power wiring **130** by using the metal for an anode, and the second power wiring pattern **135'** is formed on the second power wiring **135**.

**[0128]** As mentioned above, when the horizontal wiring is led into the light emission region and used, the first power wiring pattern **130'** and the second power wiring pattern **135'** have a certain gap therebetween.

**[0129]** In this manner, since the first power wiring pattern **130'** is formed on the first power wiring **130** and connected to the first power wiring **130**, the effect of substantially increasing the thickness of the first power wiring **130** can be obtained, so the width of the wiring can be reduced in case of having the same wiring resistance.

**[0130]** Also, since the second power wiring pattern **135'** is formed on the second power wiring **135** and dummy wiring **120** are formed under the second power wiring **135** and connected to the second power wiring **135**, the effect of substantially increasing the thickness of the second power wiring **135** can be obtained, so the width of the wiring can be reduced in case of having the same wiring resistance.

**[0131]** Next, as shown in FIG. **8**G, the barrier rib **125** demarcating the sub-pixels is formed on the substrate **110** with the pixel electrode **118**, the connection electrode, the first power wiring pattern **130'**, and the second power wiring pattern **135'** formed thereon.

**[0132]** Here, the barrier rib **125** surrounds the peripheral portions of the pixel electrode **118** like a bank to define an opening, and is made of an organic insulating material or an inorganic insulating material. The barrier **125** may also be made of a photosensitizer including black pigment, and in this case, the barrier rib **125** serves as a light blocking member.

**[0133]** The barrier rib **125** according to an embodiment of the present invention covers the first power wiring pattern **130'** formed in the organic light emitting marginal region and exposes a portion of the second power wiring pattern **135'** formed in the common electrode marginal region, but the present invention is not limited thereto.

**[0134]** And, as shown in FIG. **8**H, the organic light emitting layer **126** is formed on the substrate **110** on which the barrier rib **125** has been formed.

**[0135]** As mentioned above, the organic light emitting layer **126** may have a multi-layered structure including a light emitting layer emitting light and an auxiliary layer for improving luminous efficiency of the light emitting layer. The auxiliary layer may include an electron transport layer and a hole transport layer for balancing electrons and holes and an electron injection layer and a hole injection layer for strengthening injection of electrons and holes.

**[0136]** As shown in FIG. **8**I, the common electrode **128** as a cathode is formed on substrate **110** with the organic light emitting layer formed thereon.

**[0137]** Here, the common electrode **128** receives a common voltage and may be made of a reflective conductive material including calcium (Ca), barium (Ba), magnesium (Mg), aluminum (Al), silver (Ag), and the like, or a transparent conductive material such as ITO, IZO, or the like.

**[0138]** A metal for a cathode constituting the common electrode **128** is connected to the exposed portion of the second power wiring pattern **135'**.

**[0139]** In this manner, it is noted that, when the dummy electrodes such as the dummy wiring **120**, the first power wiring pattern **130'**, the second power wiring pattern **135'**, and the like, are used, an effect that the thickness of the power wirings **130** and **135** is substantially increased can be obtained, so the wiring resistance is reduced.

**[0140]** Here, since the wiring resistance is reduced, the width of the power wirings **130** and **135** may be reduced, and a different signal line or wiring may be additionally formed by the reduced width.

**[0141]** As the present invention may be embodied in several forms without departing from the characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its scope as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds of the claims, or equivalents of such metes and bounds are therefore intended to be embraced by the appended claims.

What is claimed is:

**1**. A method for an organic light emitting diode (OLED) display device comprising:

providing a substrate divided into a light emission region outputting an image and a wiring region positioned at an outer side of the light emission region and having a plurality of wirings formed therein;

forming a thin film transistor (TFT) on the substrate;

forming first and second power wirings with metal used for a data wiring on the substrate of the wiring region;

forming a planarization film on the substrate with the TFT and the first and second power wirings formed thereon;

forming an anode on the planarization film, forming a first power wiring pattern on the first power wiring by using a metal used for the anode such that the first power wiring pattern is connected to the first power wiring, and forming a second power wiring pattern on the second power by using the metal used for the anode wiring such that the second power wiring pattern is connected to the second power wiring;

forming a barrier rib demarcating a pixel region on the substrate with the anode, the first power wiring pattern and the second power wiring pattern formed thereon;

forming an organic light emitting layer on the substrate with the barrier rib formed thereon; and

forming a cathode on the organic light emitting layer.

**2**. The method of claim **1**, wherein the wirings formed in the wiring region include a power wring, an ON/OFF switch wiring or a reference wiring, and supply a signal or power to the pixels of the light emission region.

**3**. The method of claim **1**, further comprising:

forming a dummy wiring with a metal used for a gate wiring on the substrate of the wiring region.

**4**. The method of claim **3**, wherein the dummy wiring is electrically connected to the first power wiring or the second power wiring.

**5**. The method of claim **1**, wherein the barrier rib is formed to cover the first power wiring pattern and expose the second power wiring pattern.

**6**. The method of claim **5**, wherein the metal used for the cathode is formed to be connected to the exposed second power wiring pattern.

**7**. An organic light emitting diode (OLED) display device comprising:

a light emission region displaying display information;

a plurality of pixels formed in the light emission region;

a data driving circuit unit formed on at least one side of the light emission region and a gate driving circuit unit formed on at least one side of the light emission region;

a wiring region placed between the gate driving circuit unit and the light emission region and having a plurality of wirings disposed therein;

first and second power wirings disposed in the wiring region and made of a metal used for a data wiring; and

a first power wiring pattern made of a metal used for an anode and connected to the first power wiring and a second power wiring pattern made of the metal used for an anode and connected to the second power wiring.

**8**. The display device of claim **7**, wherein the first power wiring pattern is positioned on the first power wiring, and the second power wiring pattern is positioned on the second power wiring.

**9**. The display device of claim **7**, wherein the wirings formed in the wiring region include a power wring, an ON/OFF switch wiring or a reference wiring, and supply a signal or power to the pixels of the light emission region.

**10**. The display device of claim **7**, further comprising:

a dummy wiring disposed in the wiring region and made of a metal used for a gate wiring.

**11**. The display device of claim **10**, wherein the dummy wiring is electrically connected to the first power wiring or the second power wiring.

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