

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., Ltd.
Petitioner

v.

Optronic Sciences LLC
Patent Owner

Inter Partes Review No.: IPR2024-01132

**PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO.
7,586,121 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-100, ET SEQ**

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INDEX OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 7,586,121 (121 Patent)
1002	Declaration of Dean Neikirk in Support of Petition for Inter Partes Review of U.S. Patent 7,586,121 (121 Patent)
1003	U.S. Patent No. 7,330,168 (“Anzai”)
1004	U.S. Patent No. 6,992,332 (“Yamazaki”)
1005	File History of U.S. Patent No. 7,586,121
1006	Polysilicon TFT Technology for Active Matrix OLED Display by Mark Stewart, et. al., (“Stewart”)
1007	U.S. Patent Publication No. 2003/0067266 (“Kim”)
1008	U.S. Patent Publication No. 2006/0208979 (“Fish”)
1009	PCT Publication No. WO 2003/71511 (“Choi”)
1010	U.S. Patent No. 6,476,419 (“Yasuda”)

CHART OF CLAIMS
[1pre] An electroluminescence (EL) device, comprising:
[1a] a substrate; and
[1b] a plurality of pixels formed on the substrate, each pixel being in a respective pixel area, each pixel area including at least a first area, a second area, and a third area, wherein each pixel includes:
[1c] at least a first capacitor and a second capacitor in the first area, the first capacitor including a first conductive layer formed over a first gate oxide layer, a first dielectric layer over the first conductive layer, and a second conductive layer over the first dielectric layer, and the second capacitor including the second conductive layer, a second dielectric layer over the second conductive layer, and a third conductive layer over the second dielectric layer;
[1d] a transistor in the second area, the transistor including a first semiconductor layer formed on the substrate, the first gate oxide layer over the first semiconductor layer, and a fourth conductive layer over the first gate oxide layer, wherein the fourth conductive layer is formed of the same conductive film as the first conductive layer, and wherein both the first conductive layer and the fourth conductive layer are directly formed on the gate oxide layer; and
[1e] a light emitting device in the third area, the light emitting device including a fifth conductive layer, a first organic layer over the fifth conductive layer, and a sixth conductive layer over the first organic layer, wherein the sixth conductive layer is formed of the same conductive film as the third conductive layer.
[2] The device of claim 1, each pixel further comprising a seventh conductive layer in the second area for providing contact to the first semiconductor layer.
[3] The device of claim 1, wherein the second dielectric layer comprises a passivation layer and a capping layer.
[4] The device of claim 3, wherein at least one of the passivation layer and the capping layer comprises silicon nitride.
[5] The device of claim 1, wherein the second conductive layer and the fifth conductive layer both comprise indium tin oxide (ITO).
[6] The device of claim 1, wherein the second dielectric layer comprises a layer of passivation silicon nitride and a second organic layer formed on the layer of passivation silicon nitride, the second organic layer comprising the same material as the first organic layer.
[7] The device of claim 1, wherein the second dielectric layer comprises a passivation layer, a capping layer on the passivation layer and a second organic layer formed on the capping layer, at least one of the passivation layer and the capping layer comprising silicon nitride, and the second organic layer comprising the same material as the first organic layer.

I. INTRODUCTION

BOE Technology Group Co. LTD. (“Petitioner”) requests *inter partes* review of claims 1-7 (“Challenged Claims”) of U.S. Patent No. 7,586,121 (“121 patent,” EX1001), owned by Optronic Sciences LLC (“PO”).

This petition relies upon the declaration of Dean Neikirk (EX1002), and copies large portions of that declaration herein.

II. STATEMENT OF PRECISE RELIEF REQUESTED

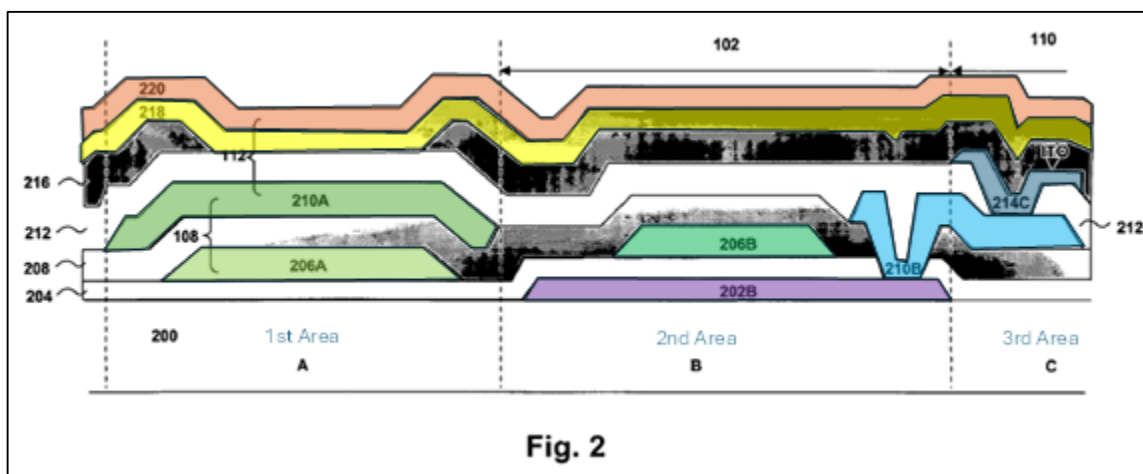
In accordance with 35 U.S.C. § 311, Petitioner requests cancelation of claims 1-5 of the 121 patent in view of the following grounds:

Ground	Claims	Stat. Basis	Prior Art
1	1-3 and 5	35 U.S.C. §102	Anzai
2	4	35 U.S.C. §103	Anzai in view of Yamazaki
3	1-7	35 U.S.C. §103	Yamazaki in view of Anzai

III. THE 121 PATENT

A. Overview of the 121 Patent

The 121 Patent was filed on December 7, 2004, published on June 8, 2006, and issued on September 8, 2009. EX1001, Face of Patent.



The 121 Patent, as seen in Figure 2 above (with coloring added), is directed to an OLED device with a plurality of pixels where each pixel (100) comprises three areas formed on a substrate 200. EX1001, Abstract. In the first area, area A, a first capacitor 108 and a second capacitor 112 are formed vertically stacked above each other, where the two storage capacitors share the second conductive layer 210A to increase the storage capacitance without increasing chip area or additional masks. *Id.*, Abstract, 5:5-6:49.

Here, in the first area, area A, the first storage capacitor 108 comprises a first metal pattern 206A (light green), the interlayer dielectric 208, and the second metal pattern 210A (light green). The second storage capacitor 112 comprises the second metal pattern 210A, the passivation SiN layer 212 and the capping silicon nitride 216, organic layer 218 (yellow), and the third metal layer 220 (i.e., cathode) (orange). *Id.*, 5:47-6:35. The two storage capacitors 108 and 112 share a common electrode (second metal pattern 210A); this configuration is commonly referred to

in the art as a tri-plate capacitor. EX1002, ¶27. The 121 Patent discloses that the first metal pattern 206A may be formed using an existing mask for the first metal pattern 206B and the same for second metal patterns 210A and 210B, thus reducing the number of masks needed to form the capacitors. EX1001, 5:47-6:35. In addition, capacitors 108 and 112 are coupled in parallel to each other and may be collectively viewed as the storage capacitor of pixel 100 "whose capacitance is equal to the sum of the capacitance of both capacitors 108 and 112" such that capacitor 112, is coupled between the gate of transistor 102 and the cathode 220 of the OLED element 110. *Id.*, 4:66-5:11.

In the second area, area B, the 121 Patent discloses a first metal pattern 206B, which serves as the gate of the transistor 102, and is formed over a polysilicon pattern 202B (i.e., semiconductor layer) (purple), which serves as the source and drain of transistor 102, with a gate oxide layer 204 in between. EX1001, 5:22-58; Fig. 2. The source of transistor 102 is coupled to power supply voltage V_{DD} and the drain is connected to drive the OLED element 110. *Id.*, 4:36-63. Second metal pattern 210B (blue) provides contact between polysilicon pattern 202B to the indium tin oxide ("ITO") pattern 214C of the OLED element 110 (see below). *Id.*, Fig. 2. Second metal pattern 210B is formed by depositing a layer of metal over ILD 208 and patterned, where the second metal pattern 210B contacts

polysilicon pattern 202B through a via hole in ILD 208 and gate oxide 204. *Id.*, 5:29-34; Fig. 2.

In the third area, area C, the 121 Patent discloses an OLED element 110 that includes an indium tin oxide ("ITO") pattern 214C (i.e., the anode) formed under a capping layer SiN 216 (black), which is formed under an organic layer 218 (yellow), which is formed under a third metal layer 220 (i.e., the cathode) (orange). EX1001, 4:58-65; 5:22-58.

The 121 Patent includes various embodiments where the first storage capacitor 108 and the second storage capacitor 112 comprise different combinations of insulation layer(s) between the conductive layers. *Id.*, Figs. 3-9, 11.

B. Overview of the 121 patent's File History

The '121 Patent was issued on September 8, 2009, from U.S. Patent Application No. 11/005,648, which was filed on December 7, 2004. Ex. 1001, Patent Face. During prosecution, the initially filed claims went through two rounds of restrictions and elections, after which the pending claims were initially rejected under section 112 for lack of written support and indefiniteness based on the submitted specification. EX1005, Office Action dated May 04, 2007, pp. 2-3. The claims were further rejected under § 102 as anticipated by Yamazaki (U.S. 2002/0104995) and under § 103 as rendered obvious by Yamazaki in view of

Murade (6,610,997). *Id.*, pp. 3-12. After the Final Rejection on March 25, 2008, the Applicant filed a Request for Continued Examination (RCE) and amended claims on June 12, 2008, where the language of claim 1 was entirely replaced and other claims were amended. *Id.*, Amendment and Response to Final Office Action with RCE, pp. 2-3.

After the Non-Final Office Action on August 15, 2008, where the Examiner made similar 112, 102, and 103 rejections as before, the Applicant conducted an interview with the Examiner and filed a response on November 17, 2008, adopting the Examiner's suggestion of amending claim 1 to include that the "first conductive layer is formed over the first gate oxide layer" in the first area, and in the second area "both the first conductive layer and the fourth conductive layer are directly formed on the gate oxide layer." *Id.*, Amendment and Response to Non-Final Office Action, pp. 2-3. The application was then allowed.

C. Person of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the 121 patent (December 7, 2004) would have had a Bachelors' degree in electrical engineering or a comparable field of study, plus approximately two to three years of professional experience with electronic and optoelectronic device design. Additional graduate education could substitute for professional

experience, and significant experience in the field could substitute for formal education. EX1002, ¶23.

D. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

The Challenged Claims are interpreted using the same claim construction standard that is used to construe the claim in a civil action in federal district court. 37 C.F.R. § 42.100(b).

Because the prior art asserted herein discloses the preferred embodiment within the indisputable scope of the claims, the Board need not construe the outer bounds of the claims as part of these proceedings. The district court may have to address other bounds of the claims in addressing infringement. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)) (providing that only those terms that are in controversy need be construed, and only to the extent necessary to resolve the controversy).

All the claim terms should be construed according to their plain and ordinary meaning to a POSITA at the time of the 121 patent.

IV. OVERVIEW OF THE PRIOR ART REFERENCES

A. EX1003 – Anzai

U.S. Patent 7,330,168 (“Anzai”) was filed on April 30, 2003, issued February 12, 2008, and claims priority to Japanese Patent Application 2002-

128008, filed on April 30, 2002. EX1003, Face of the Patent. Anzai qualifies as prior art to the 121 Patent under at least pre-AIA 35 U.S.C. § 102 (e).

B. EX1004 – Yamazaki

U.S. Patent 6,992,332 (“Yamazaki”) was filed on May 5, 2003, issued on January 31, 2006, and claims priority to Japanese patent application 2002-13994. EX1004, Face of the Patent. Yamazaki qualifies as prior art to the 121 Patent under at least pre-AIA 35 U.S.C. § 102 (e).

V. GROUND 1: CLAIMS 1-3 AND 5 ARE ANTICIPATED BY ANZAI

A. Claim 1

1. [1pre]

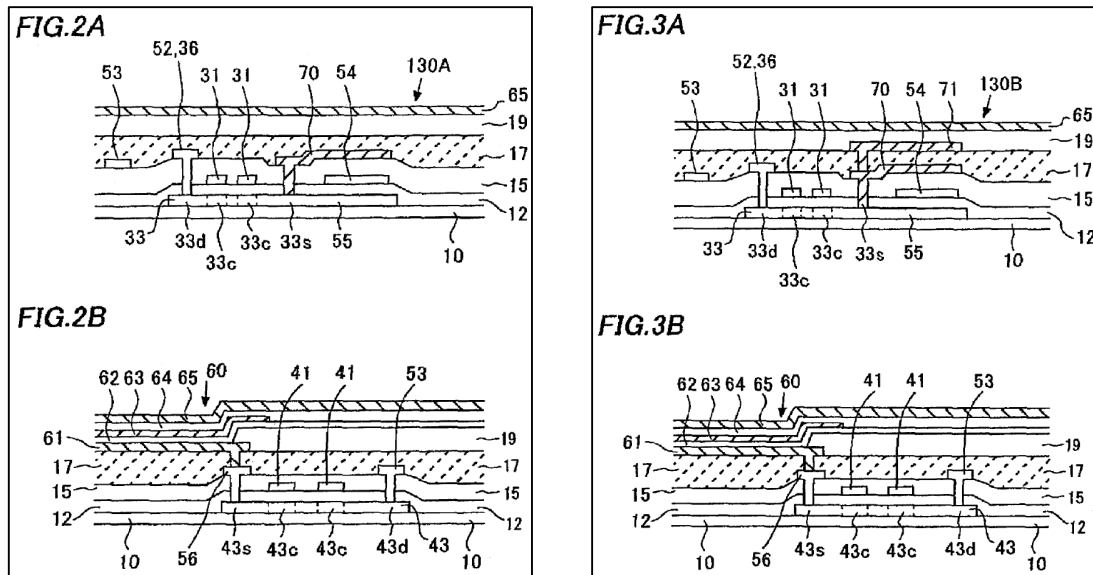
To the extent that the preamble is limiting, Anzai teaches “[a]n electroluminescence (EL) device (Anzai’s electroluminescent display device).” EX1002, ¶38-39.

Anzai is directed to electroluminescent (“EL”) display devices. EX1003, 1:6-17. More particularly, Anzai is directed to reducing the forming area of a storage capacitor for holding the video signal supplied to a transistor to improve the display quality of an electroluminescent display device with a storage capacitance element for holding a video signal supplied to the gate of a driving transistor (TFT) for an organic EL element. *Id.*, Abstract.

2. [1a]

Anzai teaches the use of “a substrate (Anzai substrate 10).” EX1002, ¶40-41.

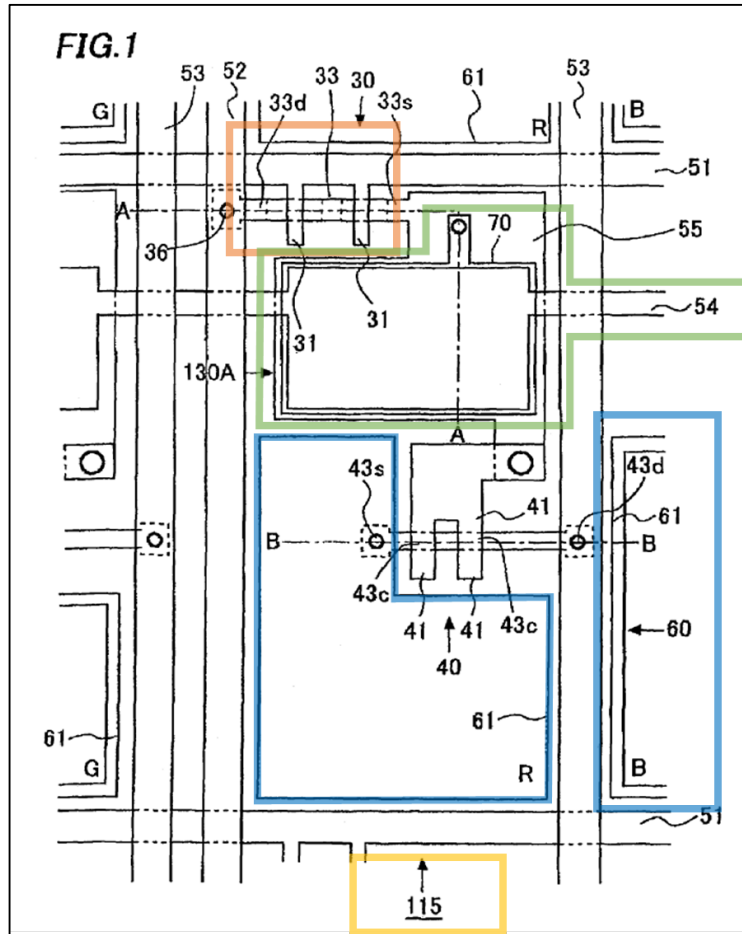
Anzai discloses “an insulating substrate 10, which is either a substrate made of a glass, a synthetic resin, a conductive material or a semiconductor.” EX1003, 3:57-61; Figs. 2A-2B and 3A-3B.



3. [1b]

Anzai discloses “a plurality of OLED pixels (RGB OLED pixels), formed on the substrate (10), each pixel being in a respective pixel area (115), each pixel area including at least a first area (Capacitor Area), a second area (Transistor Area), and a third area (OLED Area), wherein each pixel includes (*see* [1c]-[1e]).” EX1002, ¶42-43.

Anzai discloses a plurality of pixel portions 115, disposed in a matrix configuration forming a display region. EX1003, 3:28-31; Fig. 1.



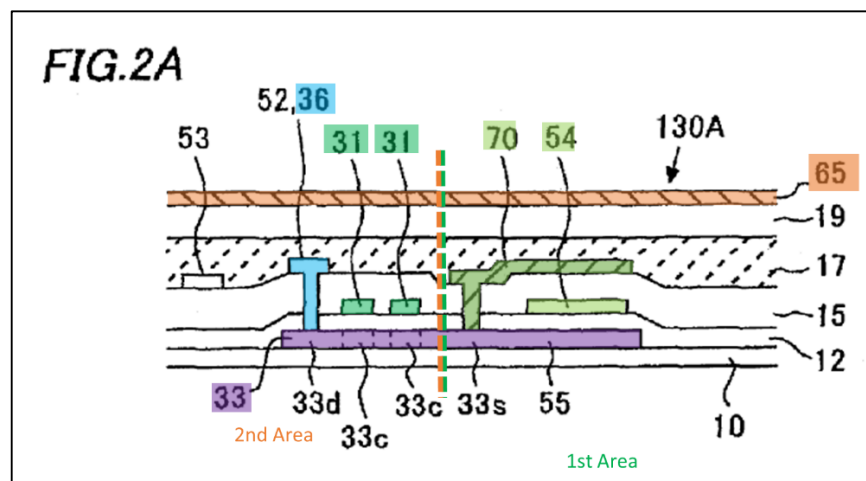
Each pixel portion 115 then comprises capacitors 130A (shown), 130B (not shown) in the first area (Capacitor Area) (see [1c]) a driving transistor 40 in the second area (Transistor Area) (see [1d]) and organic EL element 60 in the third area (OLED Area) (see [1e]). *Id.*, 3:32-40; EX1002, ¶43.

4. [1c]

Anzai discloses “at least a first capacitor (layers 54, 15, 70, 71) and a second capacitor (layers 70, 71, 17, 19, 65) in the first area, the first capacitor including a first conductive layer (electrode layer 54) formed over a first gate oxide layer (gate insulating film 12), a first dielectric layer (interlayer insulating film 15) over the

first conductive layer (electrode layer 54), and a second conductive layer (electrode layer 70 or 70/71) over the first dielectric layer (interlayer insulating film 15), and the second capacitor including the second conductive layer (electrode layer 70 or 70/71), a second dielectric layer (first 17 and second 19 planarization films) over the second conductive layer, and a third conductive layer (cathode layer 65) over the second dielectric layer.” EX1002, ¶44-49.

As seen in Fig. 2A below, Anzai discloses a first embodiment having the first capacitor within the first area that includes electrode layer 54 and electrode layer 70 with insulating film 15 sandwiched in between. EX1003, Fig. 2A, 4:25-47. Electrode layer 54 is formed over gate insulating film 12, which Anzai discloses can be made from “a SiO₂ film” (i.e., an oxide layer). *Id.*, 3:61-67; Fig. 2A.



The fact that Anzai additionally discloses electrode layer 55 providing additional capacitance storage relative to electrode layer 54 is not relevant to claim 1.

EX1002, ¶45. Claim 1 is an open ended “comprising” claim to “at least” a first and second capacitor, and the capacitors themselves are recited as “including” the recited layers. EX1001, claim 1. Thus, a device with the claimed capacitors including the claimed layers practices the claims even if the device includes additional capacitors and the capacitor includes additional layers. EX1002, ¶45.

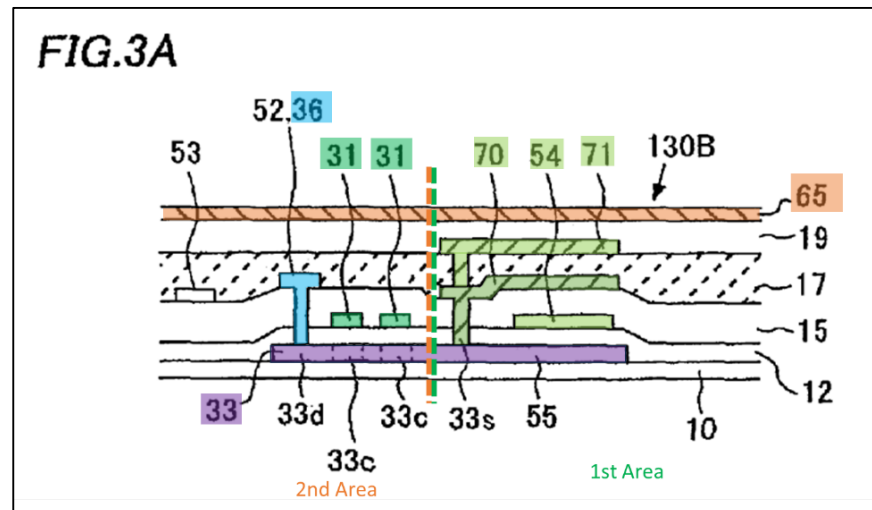
The second capacitor is formed between **electrode layer 70** and **cathode layer 65** with an insulating layer comprising first and second planarization films 17 and 19. *Id.*, Fig. 2A, 4:48-51, 5:62-67 (“In the first embodiment, a capacitance is formed between the third capacitance electrode layer 70 and the cathode layer 65 when the cathode electrode is used as a fourth capacitance electrode layer. Both the first planarization film 17 and the second planarization film 19 function as the capacitance insulating film in this configuration.”).

Anzai discloses that each of the above identified first and second capacitors functions as a capacitor. EX1003, 4:30-47 (first capacitor), 4:48-51 and 5:58-65 (second capacitor). Anzai further discloses that interlayer insulating film 15 is formed of a SiO₂ film, a SiN film and a SiO₂ film, sequentially deposited. *Id.*, 4:60-63. Both the first planarization film 17 and second planarization film 19 “function as the capacitance insulating film.” *Id.*, 5:65-67. A POSITA would have understood the first and second capacitors share a “second conductive layer” as

recited in claim 1 since the **electrode layer 70** is common to both capacitors.

EX1002, ¶47.

In addition, Anzai discloses a second embodiment (Fig. 3A) that also satisfies this limitation. EX1002, ¶48. The embodiment of Fig. 3A is that same as that of Fig. 2A except for the capacitance electrode structure that adds electrode layer 71. EX1003, 5:39-41. As seen in Figure 3A below, the formation of the first capacitor within the first area is between **electrode layer 54** stacked below the **combined electrode layer 70/71** with a gate insulating film 15 sandwiched in between. EX1003, Fig. 3A, 5:34-57.



The second capacitor is formed between the **combined electrode layer 70/71** and the **cathode layer 65**, with second planarization layer 19 sandwiched in between. *Id.*, 5:52-61 and 5:67-6:3. Here, a POSITA would have understood the first and second capacitors share a “second conductive layer” as recited in claim 1 since the

electrode layer 71 extends over and is electrically connected to electrode layer 70 (i.e., electrode layers 70 and 71 form a U-shaped conductive layer that is shared between the first and second capacitors). EX1002, ¶48. As with the first embodiment, the fact that Anzai additionally discloses an additional electrode layer 55 is not relevant. *Id.*

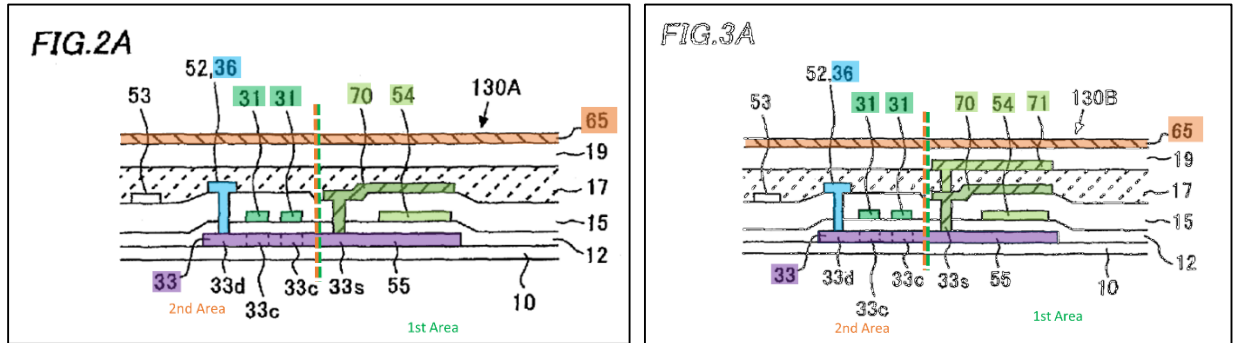
Anzai discloses the second embodiment (Figs. 3A-3B) is identical to the first embodiment (Figs. 2A-2B) other than the addition of electrode layer 71 for the capacitor. EX1003, 5:34-43. Thus, all references herein to Anzai to either embodiment apply equally to both embodiments, except where explicitly stated otherwise.

5. [1d]

Anzai discloses “a transistor (pixel selecting TFT 30) in the second area (Transistor Area), the transistor including a first semiconductor layer (active layer 33) formed on the substrate (substrate 10), the first gate oxide layer (gate insulating film 12) over the first semiconductor layer (active layer 33), and a fourth conductive layer (gate electrode 31) over the first gate oxide layer (gate insulating film 12), wherein the fourth conductive layer (gate electrode 31) is formed of the same conductive film as the first conductive layer (first electrode layer 54), and wherein both the first conductive layer (first electrode layer 54) and the fourth

conductive layer (gate electrode 31) are directly formed on the gate oxide layer (gate insulating film 12).” EX1002, ¶¶50-53.

Anzai teaches that in the second, Transistor Area, as seen in Fig. 1 (see [1a]) and in Figs. 2A and 3A annotated below (e.g., on the left side of the orange dashed line), pixel selecting TFT 30 is formed by gate electrode 31 above an active layer 33 with a gate insulating film 12 in between. EX1003, Figs. 2A and 3A; 4:1-25 and 37-40.

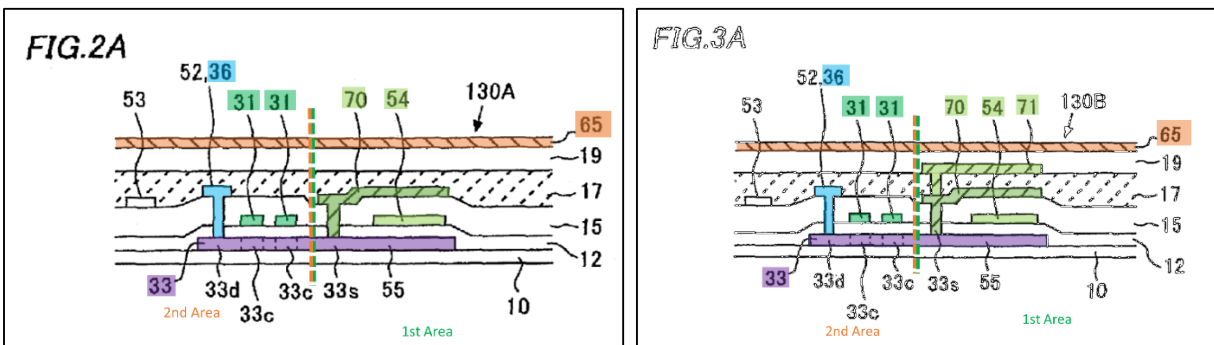


Drain electrode 36 is connected to the drain 33d, and the third capacitance electrode layer 70 is connected to the source 33s, of the TFT 30. *Id.*

Anzai discloses the device is fabricated using sequentially deposited layers. *Id.* Anzai discloses depositing on substrate 10 an amorphous silicon film, which is re-crystallized to form a polycrystalline silicon film that functions as the active layer 33. *Id.*, 4:1-7. A single or multiple layers of SiO₂ and SiN are formed on layer 33 to serve as the gate insulating film 12. *Id.*, 4:8-10. A gate signal line 51 also working as the gate electrode 31 is disposed on gate insulating film 12. *Id.*, 4:11-14; Figs. 2A and 3A. A POSITA would have understood the active layer 33

to be the first semiconductor layer, the insulating film 12 to be the gate oxide layer that is deposited over the first semiconductor layer, and the **gate electrode 31** to be the fourth conductive layer. EX1002, ¶52.

Anzai discloses that **gate electrode 31** (the fourth conductive layer) is formed of the same conductive film as the **first electrode layer 54** (the first conductive layer) because each is disclosed as being formed directly on the same underlying structure (i.e., gate insulating layer 12), they are formed by the same process, and they are formed of the same material. EX1003, Figs. 2A, 3A, 4:25-40 (“The second capacitance electrode layer 54 is made of Cr or Mo, and formed in the same layer as the gate electrode 31 and by the same process as the gate electrode 31.”)



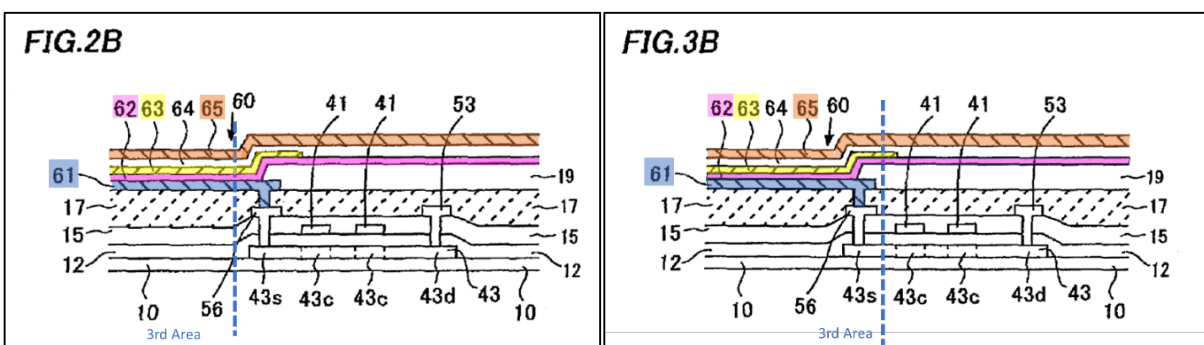
A POSITA would understand that forming electrode layers in the same layer, by the same process, with the same material, would mean these two electrode layers are formed of the same conductive film. EX1002, ¶53.

6. [1e]

Anzai teaches “a light emitting device (organic EL element 60) in the third area (OLED Area), the light emitting device including a fifth conductive layer

(anode layer 61), a first organic layer (emissive layer 63) over the fifth conductive layer (anode layer 61), and a sixth conductive layer (cathode layer 65) over the first organic layer (emissive layer 63), wherein the sixth conductive layer (cathode layer 65) is formed of the same conductive film as the third conductive layer (cathode layer 65).” EX1002, ¶54-57.

Anzai discloses, in the third OLED Area (see [1a]) and as seen in Figs. 2B and 3B below (e.g., the left side of the blue dashed line), an EL element is formed with an anode layer 61 (that is connected to the active layer source 43s through source electrode 56), an emissive layer 63 over anode layer 61, and a cathode layer 65 over the emissive layer 63. EX1003, 5:3-33; Figs. 2B, 3B.



Anzai provides the following details of the organic EL element 60:

“The organic EL element 60 includes the anode layer 61 made of the transparent electrode such as ITO (Indium Tin Oxide), a hole transportation layer 62 having a first hole transportation layer made of MTDATA (4,4-bis(3-methylphenylphenylamino)biphenyl) and a second hole transportation layer made of TPD (4,4,4-tris (3-methylphenylphenylamino)triphenylamine), an emissive layer 63 made

of Bebq2 (bis(10-hydroxybenzohquinolino)beryllium) including quinacridone derivative, an electron transportation layer 64 made of Bebq2, and the **cathode layer 65** made of either magnesium-indium alloy, aluminum or aluminum alloy.” *Id.*, 5:14-25.

A POSITA would understand that **emissive layer 63** is an organic layer because Anzai explains that during operation, organic molecules in the emissive layer are activated. *Id.*, 5:26-29; EX1002, ¶56. A POSITA would also have understood that intervening layers 62 and 64 in the organic EL element 60 do not change the relative positioning of the layers as called for in claim 1, namely, that the **emissive layer 63** is over the **anode layer 61**, and the **cathode layer 65** is over the **emissive layer 63**. EX1002, ¶56.

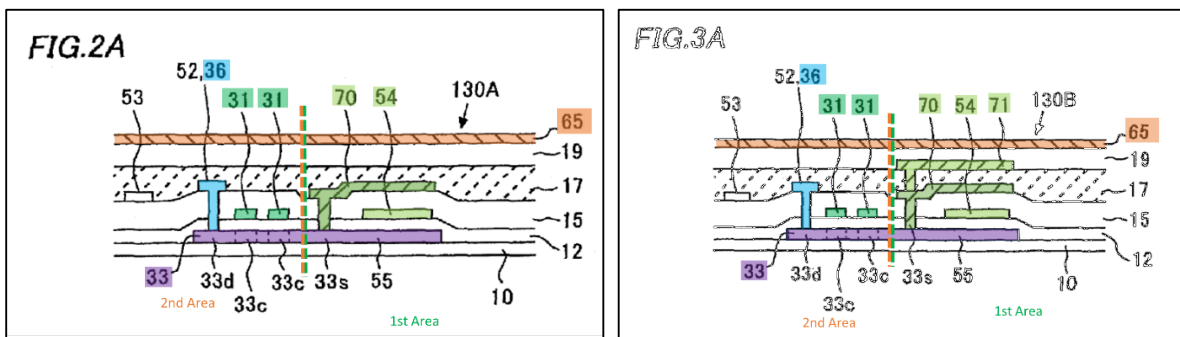
Finally, a POSITA would have further understood that the sixth conductive layer (i.e., **cathode layer 65**) of the light emitting device of Anzai is formed from the same conductive film as the third conductive layer of the second capacitor of Anzai because as shown above in section [1c], the same film (i.e., **cathode layer 65**) that serves as third conductive layer also serves as the sixth conductive layer (see above). Thus, the third and sixth conductive layers are literally the same layer in Anzai (i.e., **cathode layer 65**). *Id.*, ¶57.

B. Claim 2

Anzai discloses “the device of claim 1 (*see* claim 1), each pixel further comprising a seventh conductive layer (**drain electrode 36**) in the second area

(Transistor Area) for providing contact to the first semiconductor layer (active layer 33).” EX1002, ¶58-59.

Anzai discloses that drain electrode 36 is formed by filling a contact hole formed at the location corresponding to the drain 33d. EX1003, 4:20-24. Figs. 2A and 3A show drain electrode to be in the Transistor Area and in contact with the drain portion 33d of active layer 33.



A POSITA would have also understood drain electrode 36 to be a layer that provides contact to the active layer 33. EX1002, ¶59. The sole example of the seventh conductive layer in the 121 patent is metal pattern 210B (which provides contact to the first semiconductor layer (i.e., polysilicon pattern 202B)). EX1001, 5:29-34; Fig. 2. The 121 patent teaches that metal pattern 210B is formed by depositing a layer of metal over ILD 208 and patterned to form metal pattern 210B over both areas B and C, “wherein second metal pattern 210B contacts polysilicon pattern 202B through a via hole (not numbered) in ILD 208 and gate oxide 204.” *Id.* Therefore, Anzai teaches forming its seventh conductive layer (drain electrode

36) in the same manner as the 121 patent forms its seventh conductive layer (metal pattern 210B), namely, by filling a hole with conductive material. EX1002, ¶59.

C. Claim 3

Anzai also discloses “the device of claim 1 (*see* claim 1), wherein the second dielectric layer (first and second planarization layers 17 and 19) comprises a passivation layer (first planarization layer 17) and a capping layer (second planarization layer 19).” EX1002, ¶60-65.

The 121 patent provides no meanings for “passivation layer” and “capping layer.” In fact, the 121 patent discloses silicon nitride (SiN) as the sole example for both layers. For the passivation layer of the second dielectric layer, the 121 patent states: “A layer of passivation silicon nitride (SiN) 212 is formed over ILD208 and second metal patterns 210A and 210B.” EX1001, 5:34-36. For the capping layer of the second dielectric layer, the 121 patent states: “A layer of capping SiN 216 is disposed to cover passivation SiN 212 and ITO pattern 214C.” *Id.*, 5:40-42. A POSITA would understand from the 121 patent that there is no special meaning ascribed to passivation layer and capping layer other than they are two separate layers of insulation material. EX1002, ¶61. Moreover, given that the sole example given in the 121 patent is SiN for both layers, a POSITA would understand these two layers need not be made of different insulation materials. *Id.*

Anzai discloses that planarization layer 17 may be made of an organic resin for flattening the surface. EX1003, 4:20-24. While Anzai does not disclose the material for planarization layer 19, it must be made of an insulation material because in the embodiment of Fig. 3A, it is the sole layer between **electrode layer 71** and **cathode layer 65** forming the second capacitor. *Id.*, 6:3-8; Fig. 3A; EX1002, ¶62. Moreover, Anzai discloses that the first planarization film 17 and the second planarization film 19 for the first embodiment “function as the capacitance insulating film for this configuration.” EX1003, 5:62-67.

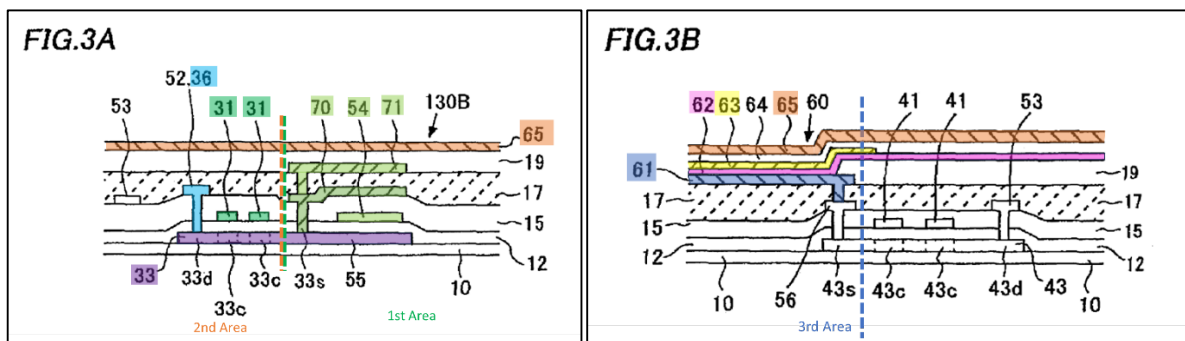
A POSITA would have understood that when the first and planarization layers 17 and 19 are used as the insulating film, one of the layers can be understood as a passivation layer while the other layer is a capping layer. EX1003, 5:44-6:9; EX1002, ¶63. The first planarization film 17 is formed over the entire surface for flattening, which will protect the semiconductor surface from the surrounding environment (for passivation). EX1003, 4:17-24, 5:3-13. The POSITA would further understand that the second planarization film 19 is then further disposed on the first planarization film 17 (capping the passivation layer). EX1002, ¶63; EX1001, 5:3-13; Figs. 2A-B, 3A-B.

As such, a POSITA would understand that Anzai’s planarization film 17 is a passivation layer and Anzai’s planarization film 19 is a capping layer. EX1002, ¶64.

D. Claim 5

Anzai discloses “the device of claim 1 (*see* claim 1 – second embodiment (Figs. 3A, 3B)), wherein the second conductive layer (**combined electrode layer 70/71**) and the fifth conductive layer (**anode layer 61**) both comprise indium tin oxide (ITO).” EX1002, ¶66-68.

For the second embodiment in Figures 3A and B, Anzai explicitly discloses **anode layer 61** (i.e., the fifth conductive layer) is made of a transparent electrode such as ITO (Indium Tin Oxide). EX1003, 5:14-25; Figs. 3A-3B.



Anzai further discloses that “**electrode layer 71** is in the same layer as and formed by the same process as **anode layer 61**.” *Id.*, 5:55-57.

Accordingly, a POSITA would have understood that Anzai discloses the **anode layer 61** comprises ITO, as does the **combined electrode layer 70/71**. EX1002, ¶68.

VI. GROUND 2: CLAIM 4 RENDERED OBVIOUS BY ANZAI IN VIEW OF YAMAZAKI

A. Claim 4

The combination of Anzai and Yamazaki renders obvious “the device of claim 3 (*see* claim 3 above) wherein at least one of the passivation layer (Anzai’s planarization film 17) and the capping layer (Anzai’s planarization film 19) comprises silicon nitride.” EX1002, ¶69-79.

The 121 patent provides no meanings for “passivation layer” and “capping layer.” In fact, the 121 patent discloses silicon nitride (SiN) as the sole example for both layers. For the passivation layer of the second dielectric layer, the 121 patent states: “A layer of passivation silicon nitride (SiN) 212 is formed over ILD208 and second metal patterns 210A and 210B.” EX1001, 5:34-36. For the capping layer of the second dielectric layer, the 121 patent states: “A layer of capping SiN 216 is disposed to cover passivation SiN 212 and ITO pattern 214C.” *Id.*, 5:40-42. A POSITA would understand from the 121 patent that there is no special meaning ascribed to passivation layer and capping layer other than they are two separate layers of insulation material. EX1002, ¶70. Moreover, given that the sole example given in the 121 patent is SiN for both layers, a POSITA would understand these two layers need not be made of different insulation materials. *Id.*

Anzai discloses that the second dielectric layer (first and second planarization layers 17 and 19) comprises a passivation layer (first planarization

layer 17) and a capping layer (second planarization layer 19). See claim 3, §V.C.

Anzai does not explicitly state what material(s) are used to form planarization layers 17 and 19 (other than an organic resin for layer 17). EX1003, 4:20-24.

However, Anzai discloses that those layers function as the capacitance insulating film. *Id.*, 5:62-6:9. Anzai further expressly discloses that silicon nitride (SiN) can be used in the interlayer insulating film 15 that is between second capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitance element 130, and in the gate insulating film 12 between first and second capacitance electrode layers 55 and 54. *Id.*, 4:8-10, 4:17-24 and 4:40-47.

Yamazaki discloses an active-matrix type light emitting device with organic compound light emitting element, that includes pixel parts 2. EX1004, Abstract, 8:56-67, Fig. 2.

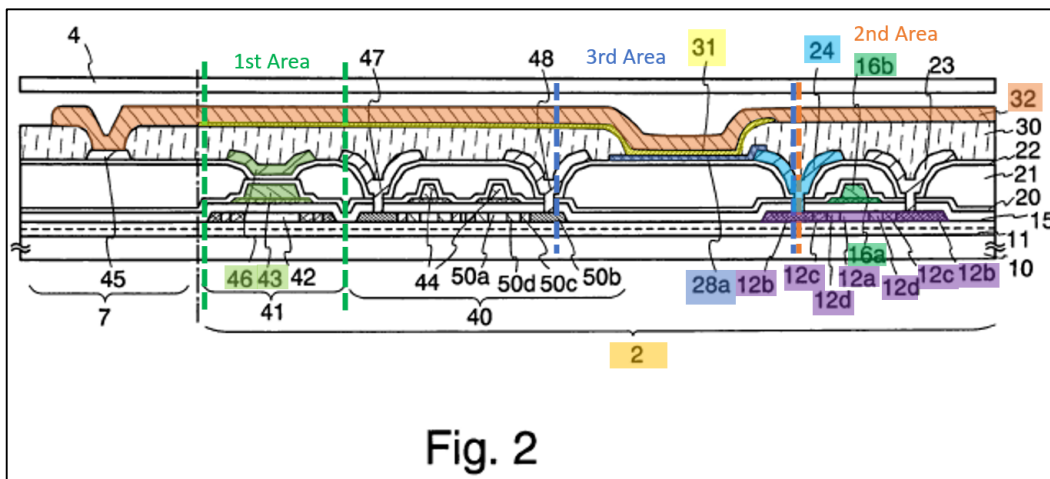


Fig. 2

Each pixel part 2 includes a first area that contains capacitors¹, a second area that contains a transistor and a third area that contains a light emitting element. *Id.*, 9:47-12:20, Fig. 2. The first area (Capacitor Area) includes a first capacitor formed between electrode 43 and electrode 46 with interlay insulating films 22 and 20 disposed in between, and a second capacitor formed electrode 46 and 2nd electrode 32 (e.g., cathode of the EL device) with an insulating material 30 and EL layer 31 disposed in between. EX1004, 9:65-12:20, Fig. 2. The second area (TFT Area) includes a transistor (e.g., current-controlling TFT) formed by gate electrodes 16a/16b disposed on top of regions 12a-12d on top of substrate 10. *Id.*, 9:47-64, Fig. 2. The third area includes a light emitting element formed by a 2nd electrode 32 disposed above an EL layer 31 which is disposed above 1st electrode 28a (e.g., anode of the EL device). *Id.*, 11:22-12:20, Fig. 2.

Insulation layer 30 is disposed between cathode electrode layer 32 and the electrodes 46, 47, 48, 24, 23 underneath (similar to Anzai's layers 17, 19 disposed

¹ Yamazaki refers to “a capacity 41”, and “a holding capacity is formed using an electrode 46 and an electrode 43,” and “a holding capacity is also formed using the electrode 43 and a semiconductor film 42.” EX1004, 9:65-10:15. A POSITA would have understood that “capacity” refers to a “capacitor” given the structure at issue (two electrodes separated by insulation). EX1002, ¶72.

between cathode 65 and electrodes 53, 52, 70). EX1004, Fig. 2. The top surface of insulation layer 30 is flattened relative to the topology underneath that includes electrodes 46, 47, 48, 24, 23 and insulation film 21 (similar to Anzai's layers 17, 19). *Id.* Yamazaki teaches that silicon nitride is a suitable material for insulation layer 30. *Id.*, 11:45-50. Yamazaki also teaches that the flat top surface of insulation layer 30 can be achieved by CMP (chemical mechanical polish), which can be performed after the formation of insulating material 30. *Id.*, 20:17-24.

It would have been obvious to a POSITA to combine the teachings of Anzai and Yamazaki to use silicon nitride as the material for at least one of the planarization films 17 or 19 of Anzai. EX1002, ¶76.

Anzai and Yamazaki are analogous prior art to the 121 patent, as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third area containing a light emitting device having an organic layer between two electrode layers. EX1002, ¶77.

A POSITA would have understood the issue involved, namely what material(s) can be used to form the first and second planarization layers 17 and 19 for the second capacitor of Anzai. EX1002, ¶78. To address this issue, a POSITA would have investigated what insulator material(s) would be appropriate. *Id.* A POSITA would have been motivated to use silicon nitride to form at least one of

the first and second planarization layers 17 and 19 of Anzai because (1) Yamazaki teaches using silicon nitride as the insulating layer 30 under its cathode layer (EX1004, 11:45-50), (2) Yamazaki teaches using silicon nitride for use as a planarization film for flattening the surface (compare upper and lower surfaces of insulation layer 30 (*Id.*, 11:22-12:20), and (3) Anzai teaches using silicon nitride in the interlayer insulating film 15 between second and third capacitance electrode layers 54 and 70, and in the gate insulating film 12 between first and second capacitance electrode layers 55 and 54 (EX1003, Fig. 2A, 4:8-10 and 17-24 and EX1004, 11:22-12:52, 20:17-39, Fig. 2). EX1002, ¶78.

Additionally, Anzai discloses that both films 17 and 19 are used as the capacitance insulating film. EX1003, 5:65-67. A POSITA would have known that organic materials usually have lower dielectric constants than inorganic materials such as SiN, and a higher dielectric constant is desirable for the insulator in a capacitor since that leads to a higher capacitance per unit area. EX1002, ¶78. That then allows a reduced area storage capacitance element, one of the objectives of Anzai. EX1003, Abstract (“The forming area of the storage capacitance element for holding the video signal supplied to the gate of the driving transistor can be thus reduced, improving display quality as well as extending life span of the organic El element.”). Therefore, a POSITA would have been motivated to

consider using an inorganic material such as SiN for the films 17 and 19. EX1002, ¶78.

The modification to Anzai would simply involve selecting an appropriate insulation material for the first and second planarization layers 17 and 19.

EX1002, ¶79. A POSITA would have had a reasonable expectation of success in combining Anzai and Yamazaki, as both references disclose forming capacitors for use with organic electroluminescent devices, and both references teach insulator films for such capacitors that comprise silicon nitride. *Id.* Moreover, because combining the teachings of Anzai and Yamazaki would involve known methods, it would have yielded predictable results. *Id.*

VII. GROUND 3: CLAIMS 1-7 RENDERED OBVIOUS BY YAMAZAKI IN VIEW OF ANZAI

A. Claim 1

1. [1pre]

To the extent that the preamble is limiting, the combination of Yamazaki and Anzai renders obvious “[a]n electroluminescence (EL) device (Yamazaki’s light emitting device).” EX1002, ¶80-81.

Yamazaki is directed to a light emitting device. EX1004, Abstract. In particular, Yamazaki is directed to a light emitting display device (“EL element”) in which a light emitting element arranged in a matrix configuration has a layer

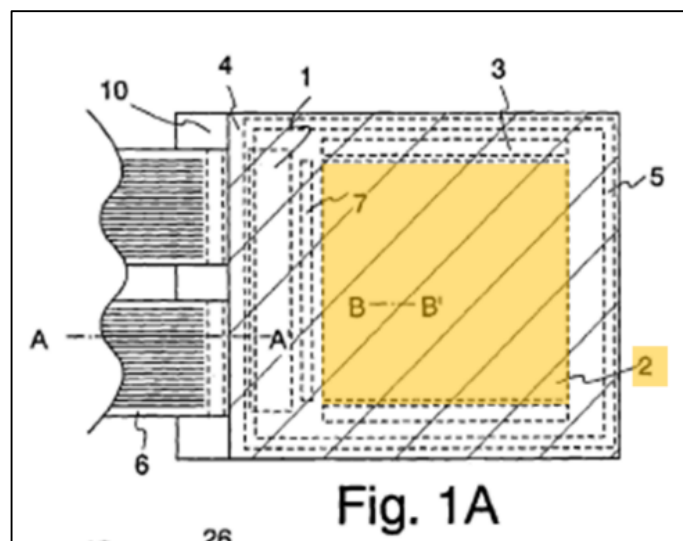
The combination of Yamazaki and Anzai renders obvious “a substrate (Yamazaki’s substrate 10).” EX1002, ¶82-83.

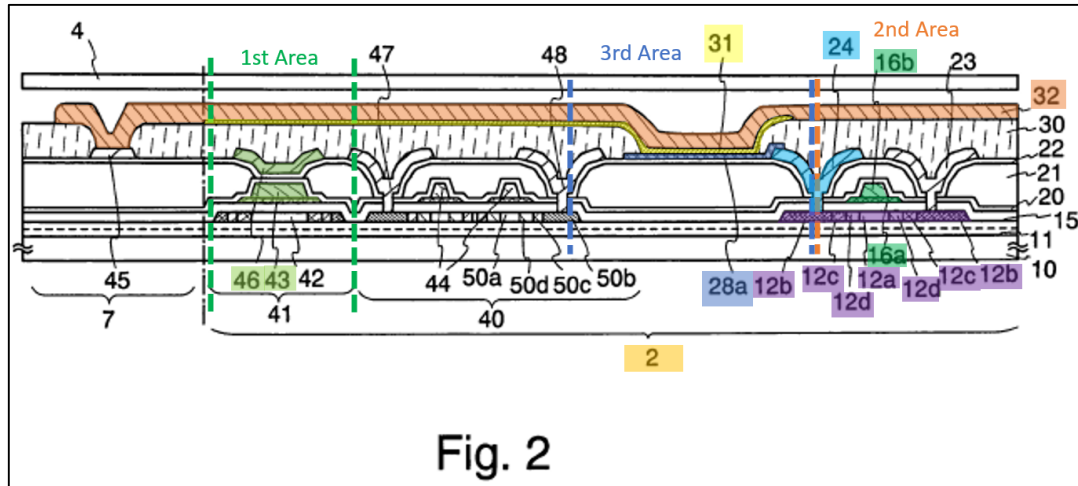


3. [1b]

The combination of Yamazaki and Anzai renders obvious “a plurality of OLED pixels (Yamazaki’s plurality of pixels), formed on the substrate (Yamazaki’s substrate 10), each pixel being in a respective pixel area (Yamazaki’s pixel part 2), each pixel area including at least a first area (Yamazaki’s Capacitor Area), a second area (Yamazaki’s TFT Area), and a third area (Yamazaki’s EL element), wherein each pixel includes (*see* [1c]-[1e]).” EX1002, ¶84-85.

Yamazaki discloses that pixel part 2 comprises a plurality of pixels within an active-matrix type light emitting device. EX1004, 2:37-64, 8:63-9:4, 9:47-64, Figs. 1A, 2. Each pixel part 2 comprises a capacity 41 (i.e., capacitors) in the first area (Capacitor Area) (*see* 1[c]), a current-controlling TFT in the second area (TFT Area) (*see* 1[d]) and an EL element in the third area (EL Area) (*see* 1[e]). *Id.*, 9:47-10:55, 11:22-12:13, 20:3-21:7; Fig. 2. EX1002, ¶85.





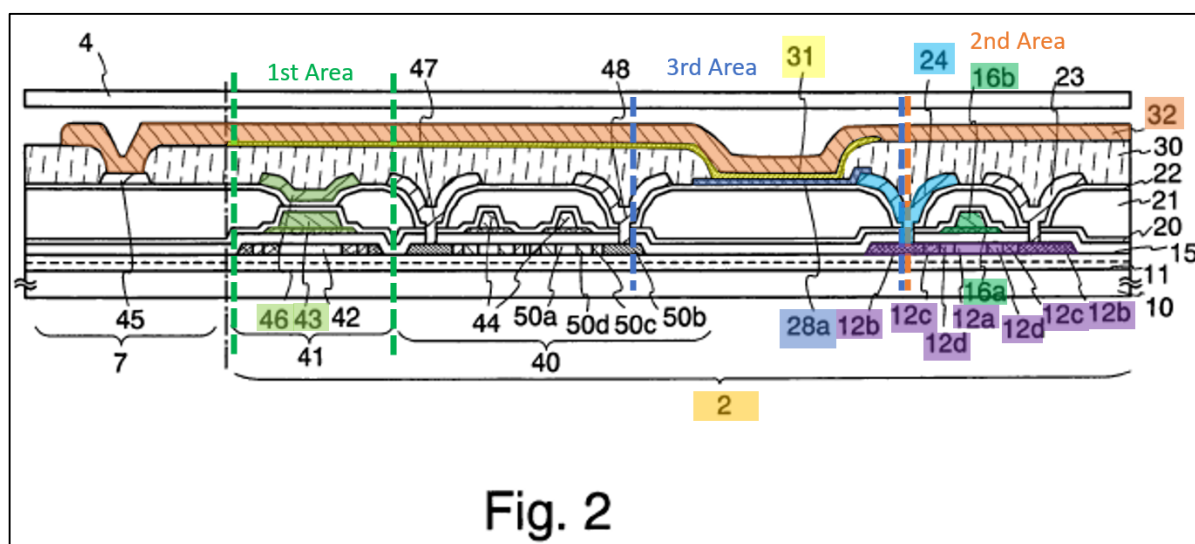
4. [1c]

The combination of Yamazaki and Anzai renders obvious “at least a first capacitor (Yamazaki’s **capacity 41**) and a second capacitor (Yamazaki’s **capacity 41**) in the first area, the first capacitor including a first conductive layer (Yamazaki’s **electrode 43**) formed over a first gate oxide layer (Yamazaki’s gate insulating film 15), a first dielectric layer (Yamazaki’s interlayer insulation films 22 and 20) over the first conductive layer (Yamazaki’s **electrode 43**), and a second conductive layer (Yamazaki’s **electrode 46**) over the first dielectric layer (Yamazaki’s interlayer insulation films 22 and 20), and the second capacitor including the second conductive layer (Yamazaki’s **electrode 46**), a second dielectric layer (Yamazaki’s insulating material 30 as modified by Anzai) over the second conductive layer, and a third conductive layer (Yamazaki’s **2nd electrode (cathode) 32**, referred to herein as “**cathode 32**”) over the second dielectric layer.”

EX1002, ¶86-97.

As seen in Figure 2 below, Yamazaki discloses a first embodiment having a capacity 41 within the first area, the **Capacitor Area** (e.g., the area between the two green dotted lines) that includes a capacitor composed of the **electrode 43** and **electrode 46** where interlayer insulation films 22 and 20 act as the dielectric material that is sandwiched in between. EX1004, 9:65-10:55, Fig. 2. **Electrode 43** is formed over the gate insulating film 15, which is made from a silicon oxide film that is formed on top of the substrate 10. *Id.*

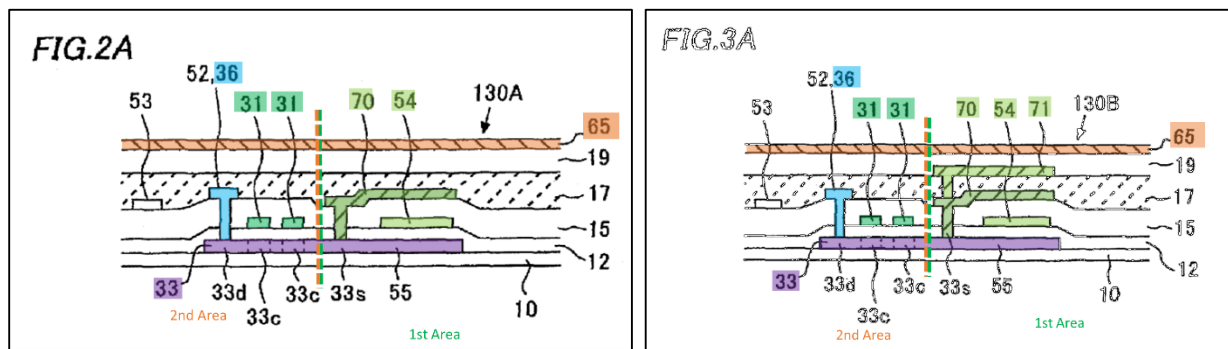
The fact that Yamazaki discloses a holding capacity (i.e., capacitor) formed between **electrode 43** and the semiconductor layer 42 is not relevant to claim 1. EX1002, ¶88. Claim 1 is an open ended “comprising” claim to “at least” a first and second capacitor, and the capacitors themselves are recited as “including” the recited layers. EX1001, claim 1. Thus, a device with the claimed capacitors including the claimed layers practices the claims even if the device includes additional capacitors and the capacitor includes additional layers. EX1002, ¶88.



The second capacitor is formed between **electrode 46** and **cathode 32** with insulating material 30 acting as the dielectric materials sandwiched in between the electrodes when the thickness of insulating material 30 is selected according to the teachings of Anzai. EX1004, 9:65-10:55, 11:22-12:13, Fig. 2. Although Yamazaki does not disclose a holding capacity (i.e., capacitor) formed between **electrode 46** and **cathode 32**, it would have been obvious to combine Yamazaki with the teachings of Anzai for the formation of a storage capacitor using the **cathode 32** of the EL device, which extends from the third area into the first area, as an electrode for a storage capacitor with **electrode 46**. EX1002, ¶89.

Anzai discloses “at least a first capacitor (layers 54, 15, 70, 71) and a second capacitor (layers 70, 71, 17, 19, 65) in the first area, the first capacitor including a first conductive layer (electrode layer 54) formed over a first gate oxide layer (gate insulating film 12), a first dielectric layer (interlayer insulating film 15) over the

first conductive layer (**electrode layer 54**), and a second conductive layer (**electrode layer 70 or 70/71**) over the first dielectric layer (interlayer insulating film 15), and the second capacitor including the second conductive layer (**electrode layer 70 or 70/71**), a second dielectric layer (first 17 and second 19 planarization films) over the second conductive layer, and a third conductive layer (**cathode layer 65**) over the second dielectric layer.” See §V.A.4.



Specifically, Anzai discloses a first capacitor between layers 55 and 54, a second capacitor between **electrode layers 54 and 70 or 70/71**, and a third capacitor between **electrode layers 70 or 70/71**, and **cathode 65** (which extends from the third area into the first area.) EX1002, ¶94; EX1003, 4:48-51 (“It is also possible to acquire the larger capacitance by extending the cathode layer 65 over the third capacitance electrode layer 70 through the first planarization film 17 and a second planarization film 19.”

It would have been obvious to a POSITA to combine the teachings of Anzai and Yamazaki to modify the thickness of insulating material 30 of Yamazaki to form the second capacitor of desired capacitance between **electrode 46** and **cathode**

32 (which extends from the third area into the first area) with insulating material 30 sandwiched in between as the capacitor dielectric material. EX1002, ¶95.

Anzai and Yamazaki are analogous prior art to the 121 patent, as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third area containing a light emitting device having an organic layer between two electrode layers. *Id.*, ¶96.

A POSITA would have understood the issue involved, namely that a capacitor can be formed between Yamazaki's electrode 46 and cathode 32 such that the insulating material 30 and EL layer 31 act as the dielectric material in between the two capacitor electrodes. EX1002, ¶97. A POSITA would have been motivated to apply the teaching of Anzai where a storage capacitor can be established between the electrode layer 70 and the cathode layer 65 where the first and second planarization layers 17 and 19 are the dielectric materials in between (*see* §V.A.4). A POSITA would have had a reasonable expectation of success in combining Yamazaki with the teachings of Anzai, as both references disclose forming two storage capacitors for use within a light emitting or electroluminescent device. EX1002, ¶97. Moreover, the combination of Yamazaki with Anzai would involve known methods to yield predictable results. *Id.*

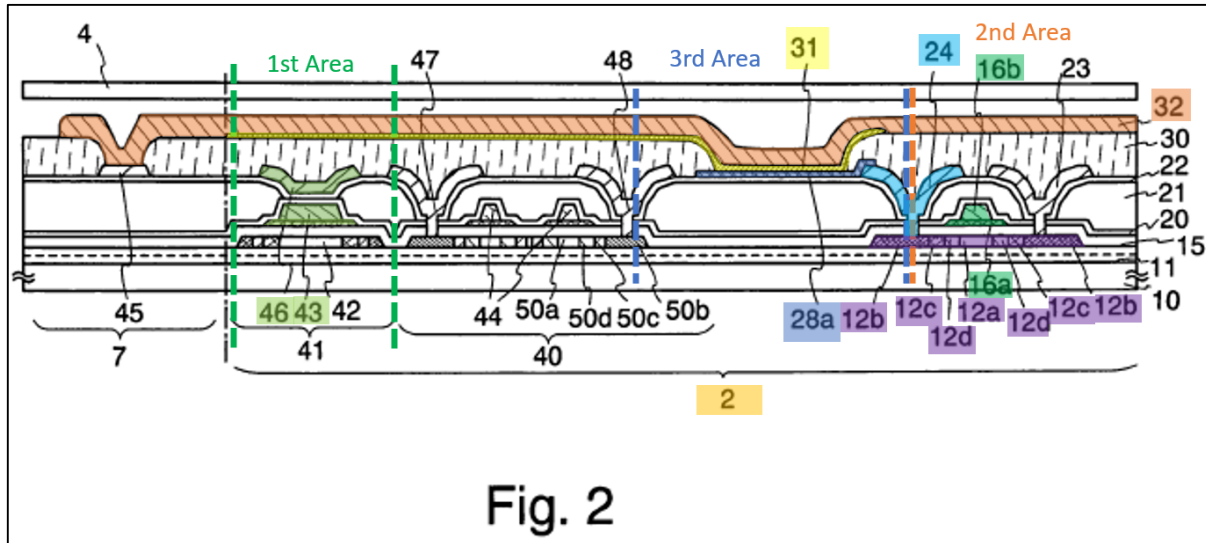
5. [1d]

The combination of Yamazaki and Anzai renders obvious “a transistor (Yamazaki’s current-controlling TFT) in the second area (Yamazaki’s TFT Area), the transistor including a first semiconductor layer (Yamazaki’s regions 12a-12d) formed on the substrate (Yamazaki’s substrate 10), the first gate oxide layer (Yamazaki’s gate insulating film 15) over the first semiconductor layer (Yamazaki’s regions 12a-12d) and a fourth conductive layer (Yamazaki’s gate electrode 16a/16b) over the first gate oxide layer (Yamazaki’s gate insulating film 15), wherein the fourth conductive layer (Yamazaki’s gate electrode 16a/16b) is formed of the same conductive film as the first conductive layer (Yamazaki’s electrode 43), and wherein both the first conductive layer (Yamazaki’s electrode 43) and the fourth conductive layer (Yamazaki’s gate electrode 16a/16b) are directly formed on the gate oxide layer (Yamazaki’s gate insulating film 15).” EX1002, ¶98-102.

As seen in Figure 2 below, Yamazaki discloses in the second area, the TFT Area (e.g., the area to the right of the orange dotted lines), a current-controlling TFT (not numbered) arranged on pixel part 2 which is formed on substrate 10 below gate insulating film 15. EX1004, 9:47-64, Fig. 2. The current-controlling TFT comprises an n-channel TFT having a channel forming region 12a, source and drain (high impurity) regions 12b, and low-level impurity regions 12c and 12d over

which the gate electrodes 16a/16b are deposited. *Id.* Regions 12a-12d are formed on substrate 10. *Id.*, Fig. 2. A POSITA would have understood that regions 12a-12d of the current controlling TFT are a semiconductor layer. EX1002, ¶99. Gate insulating film 15 is formed over the regions 12a-12d, and is constructed of a silicon oxide film. EX1004, Fig. 2, 10:31-33. Gate electrode 16a/16b and electrode 43 are directly formed on gate insulating film 15. *Id.*, Fig. 2.

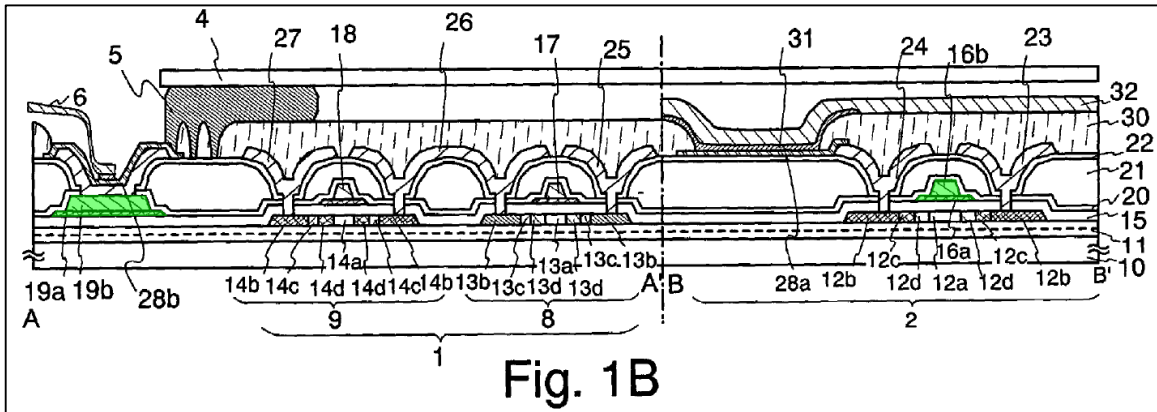
Yamazaki does not disclose the materials used to form gate electrode 16a/16b and electrode 43. However, gate electrode 16a/16b is referred to collectively as electrode 16 that includes “the first conductive layer 16a as a lower layer and the second conductive layer 16b as an upper layer.” EX1004, 18:8-14. Lower layer 16a is shown as a thin layer formed directly on insulation layer 15, and upper layer 16a is shown as a narrower but thicker trapezoidal layer formed directly on lower layer 16. *Id.*, Fig. 2. Electrode 43 is shown to have the same configuration as electrode 16, namely, a thin lower layer that is formed directly on insulation layer 15, and a narrower but thicker trapezoidal upper layer formed directly on the lower layer. *Id.* The composition and general shapes of electrode 16 and electrode 43 are shown to be the same.



It would have been obvious to a POSITA to form **electrode 16** and **electrode 43** of the same conductive film. EX1002, ¶101.

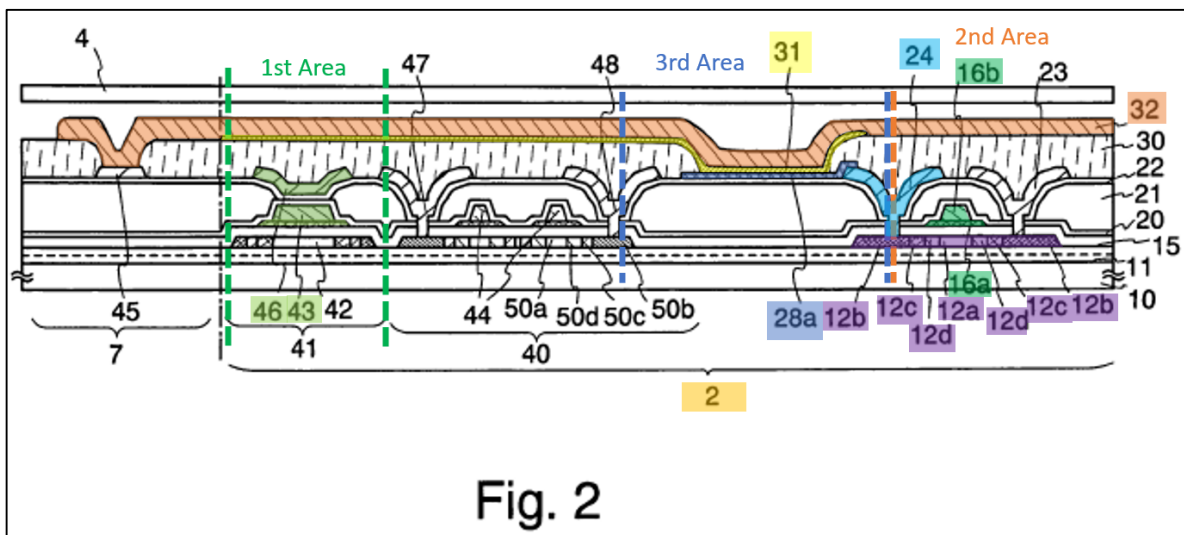
A POSITA would have understood the issue involved, namely how to form the device of Yamazaki with an efficient manufacturing process flow. EX1002, ¶102. To address this issue, a POSITA would have investigated what components could be formed using the same process step (i.e., layer deposition and patterning), which results in the components being formed of the same film, is common practice when forming semiconductor products. *Id.* Motivation to do so comes from Yamazaki, which discloses forming multiple components “in the same step.” EX1004, 12:21-28 (“In addition, on the terminal portion shown in FIG. 1B, a terminal electrode formed as a laminate of electrodes 19a, 19b formed by the same step as that of the gate electrode.” Fig. 1b shows that **terminal electrode 19a/19b** has the same configuration as **gate electrode 16a/16b** (thin lower layer that is

formed directly on insulation layer 15, and a narrower but thicker trapezoidal upper layer formed directly on the lower layer).



A POSITA would understand that Yamazaki is disclosing that terminal electrode 19a/19b and gate electrode 16a/16b are formed of the same conductive film.

EX1002, ¶102. Moreover, terminal electrode 19a/19b in Fig. 1B has the same configuration as electrode 43 in Fig. 2 (i.e., thin lower layer that is formed directly on insulation layer 15, and a narrower but thicker trapezoidal upper layer formed directly on the lower layer).



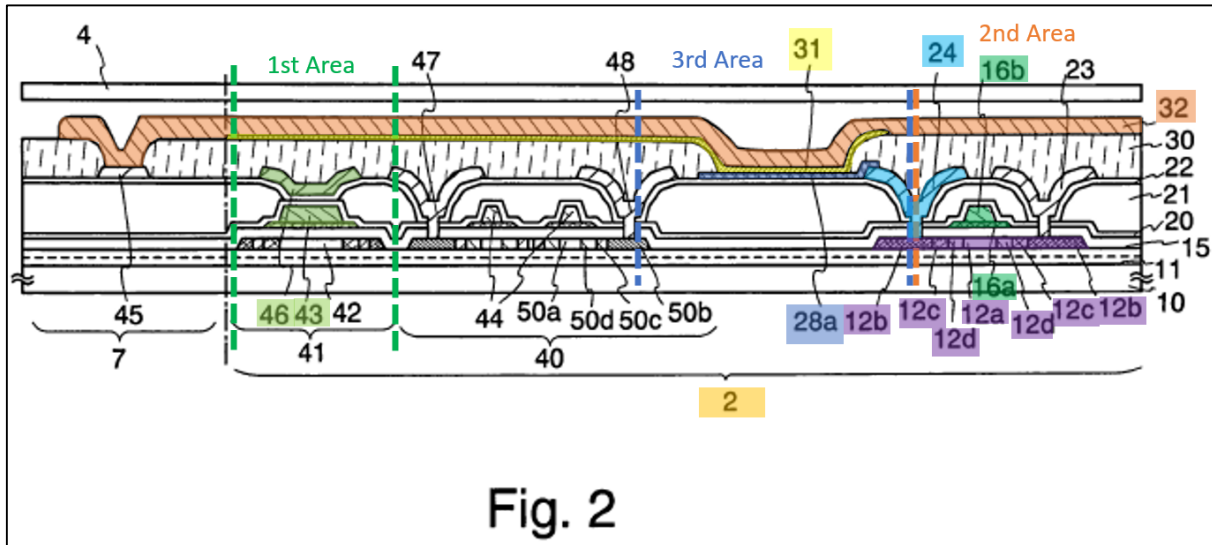
A POSITA would have therefore found it obvious to form **electrode 16** and **electrode 43** using the same step, of the same conductive film, to provide for a more efficient manufacturing process flow. EX1002, ¶102.

6. [1e]

The combination of Yamazaki and Anzai renders obvious “a light emitting device (Yamazaki’s EL element) in the third area (Yamazaki’s **EL Area**), the light emitting device including a fifth conductive layer (Yamazaki’s **1st electrode (anode) 28a**, referred to herein as “**anode 28**”), a first organic layer (Yamazaki’s **EL layer 31**) over the fifth conductive layer (Yamazaki’s **anode 28**), and a sixth conductive layer (Yamazaki’s **cathode 32**) over the first organic layer (Yamazaki’s **EL layer 31**), wherein the sixth conductive layer (Yamazaki’s **cathode 32** in the third area) is formed of the same conductive film as the third conductive layer (Yamazaki’s **cathode 32** in the first area).” EX1002, ¶103-106.

As seen in Figure 2 below, Yamazaki discloses, in the **EL Area** (*see* [1a]) (e.g., between the blue dashed lines), a **1st electrode 28a** which functions as an anode of the EL element, **EL layer 31** formed on anode 28, and **2nd electrode 32** which functions as the cathode formed on **EL layer 31**. EX1004, 11:22-12:20, 20:3-21:7, Fig. 2. Yamazaki goes on to disclose that since the EL element emits light through the **anode 28a**, it may be a transparent conductive film such as ITO. *Id.* The light emitting layer **EL layer 31** contains an organic compound. *Id.*

Lastly, the **cathode 32** is deposited on top of the light emitting layer within **EL layer 31**, which functions as wiring common to all pixels. *Id.*, EX1002, ¶104.



Yamazaki also teaches that EL layer 31 “is formed by freely combining a light emitting layer, electric charge transporting layers, and an electric charge injection layer where known polymeric organic materials can be employed. EX1004, 11:45-50, 20:3-21:7, Fig. 2. The purpose of EL layer 31 comprising a plurality of layers is for light emission and for moving carriers to cause light emission where it can be made from a monomeric organic EL material, a polymeric organic material, or other known materials. *Id.*

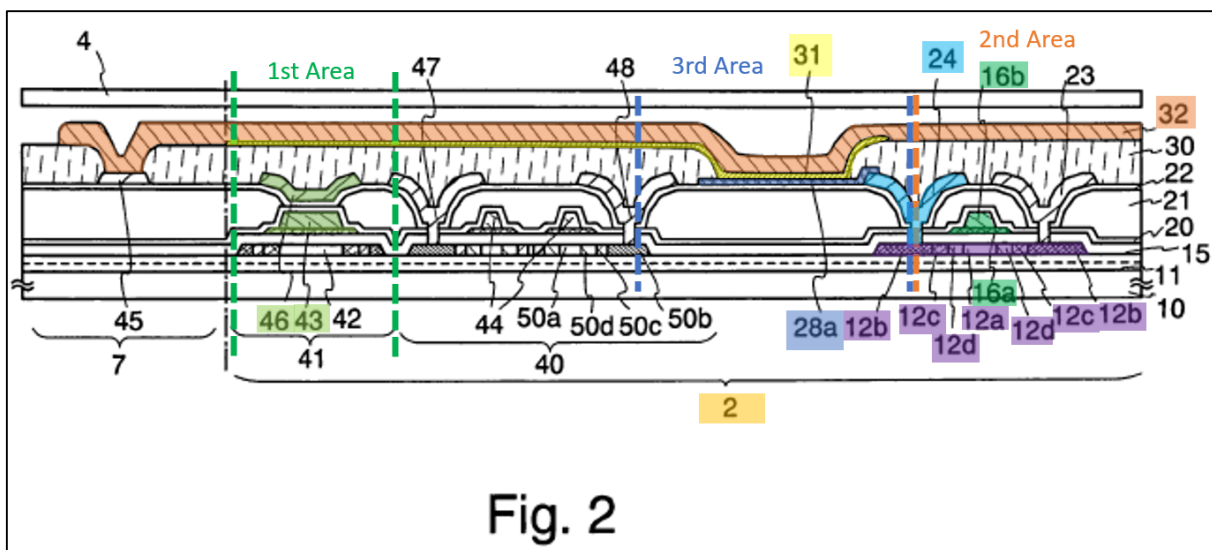
A POSITA would have understood that the sixth conductive layer (i.e., **cathode 32** in the third area) of the light emitting device of Yamazaki is formed from the same conductive film as the third conductive layer of the second capacitor of Yamazaki (i.e., **cathode 32** in the first area) because as shown above in [1c], the

same film (i.e., **cathode 32**) that serves as the third conductive layer in the first area also serves as the sixth conductive layer in the third area (*see above*). Thus, the third and sixth conductive layers are literally the same layer in Yamazaki. EX1002, ¶106.

B. Claim 2

The combination of Yamazaki and Anzai renders obvious “the device of claim 1 (*see claim 1*), each pixel further comprising a seventh conductive layer (Yamazaki’s **connecting electrode 24**) in the second area (Yamazaki’s **TFT Area**) for providing contact to the first semiconductor layer (Yamazaki’s **regions 12a-12d**).” EX1002, ¶107-109.

Yamazaki discloses, in the **TFT Area** (e.g., second area) **connecting electrode 24** for making a connection between the 1st **electrode 28a** (e.g., **anode 28a**) to the **source region 12b**. EX1004, 9:47-64, Fig. 2.

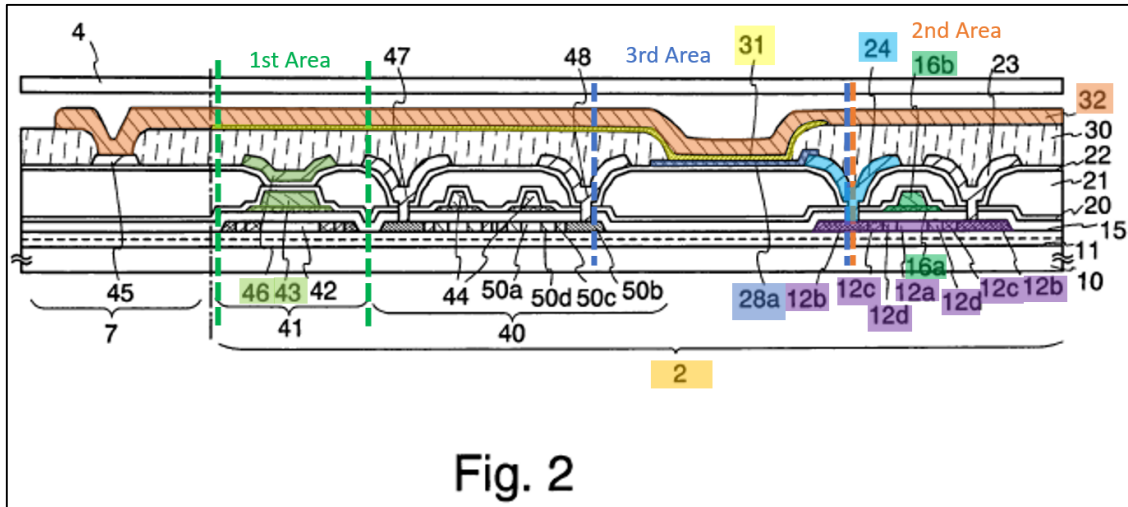


A POSITA would have understood that connecting electrode 24 to be a layer that provides contact to the regions 12a-12d, including source region 12b, which is a semiconductor layer. EX1002, ¶109.

C. Claim 3

The combination of Yamazaki and Anzai “the device of claim 1 (*see* claim 1), wherein the second dielectric layer (insulating material 30) comprises a passivation layer (Yamazaki insulating material 30) and a capping layer (Anzai’s planarization layer 19).” EX1002, ¶110-121.

The 121 patent provides no meanings for “passivation layer” and “capping layer.” In fact, the 121 patent discloses silicon nitride (SiN) as the sole example for both layers. For the passivation layer of the second dielectric layer, the 121 patent states: “A layer of passivation silicon nitride (SiN) 212 is formed over ILD208 and second metal patterns 210A and 210B.” EX1001, 5:34-36. For the capping layer of the second dielectric layer, the 121 patent states: “A layer of capping SiN 216 is disposed to cover passivation SiN 212 and ITO pattern 214C.” *Id.*, 5:40-42. A POSITA would understand from the 121 patent that there is no special meaning ascribed to passivation layer and capping layer other than they are two separate layers of insulation material. EX1002, ¶111. Moreover, given that the sole example given in the 121 patent is SiN for both layers, a POSITA would understand these two layers need not be made of different insulation materials. *Id.*

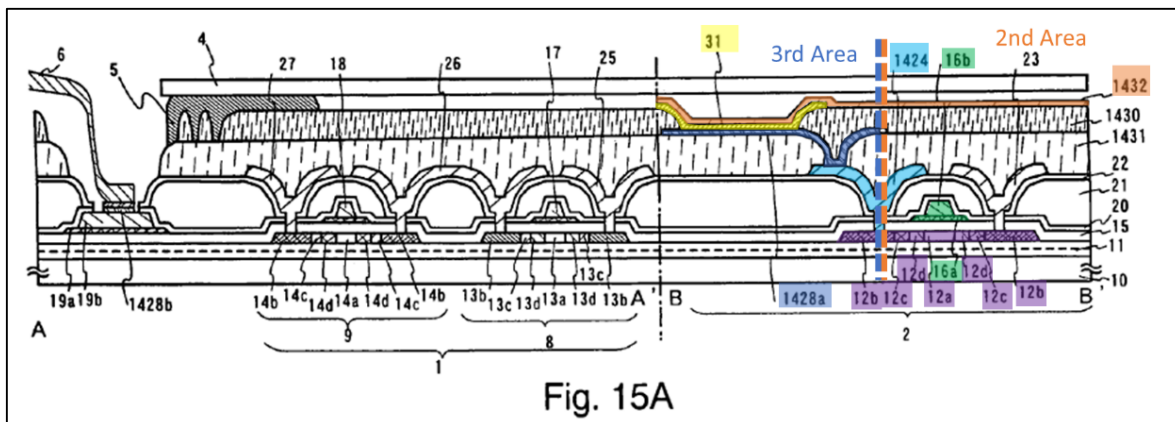


Yamazaki discloses “insulating material 30 which may be a photosensitive or non-photosensitive organic material (such as polyimide, acrylate, polyamide, polyimide amide, resist, or benzocyclobutene) or an inorganic material (such as silicon dioxide, silicon nitride, or silicon oxynitride). EX1004, 11:22-65, Fig. 2. Insulating materials 30, also called a bank, is formed on both ends of the 1st electrode 28a (e.g., anode), which may be formed by an organic resin film or an insulating film including silicon. *Id.*

Insulation layer 30 is disposed between cathode 32 and the electrodes 46, 47, 48, 24, 23 (similar to Anzai’s layers 17 and 19 disposed between cathode 65 and electrodes 53, 52, 70). EX1004, Fig. 2. The top surface of insulation layer 30 is flattened relative to the topology underneath that includes electrodes 46, 47, 48, 24, 23 and insulation film 21 (similar to Anzai’s layers 17, 19). *Id.*

Yamazaki, in Figure 15A below, also discloses, in another embodiment, the formation of an interlayer insulation film 1431 that is formed below insulation film

1430 (e.g., which corresponds to insulation layer 30). EX1004, 35:49-36:54; Fig. 15A. Figure 15A shows the same structural components as seen in Figures 1A and 1B, which also shows the same configuration of a light emitting device as shown in Figure 2. *Id.*, 35:49-58, 8:3-9, 8:56-62; Figs. 1A-1B, 2. Here, an interlayer insulating film 1431, also comprising of an organic material (e.g., a photosensitive or non-photosensitive) or an inorganic material (e.g., silicon dioxide, silicon nitride, or silicon oxynitride) is deposited below the insulating material 1430 (i.e., the bank) as previously described. *Id.*, 35:65-36:54; Fig. 15A. Yamazaki explicitly indicates that a silicon nitride film may be used to form the interlayer insulation film 1431. *Id.*, 36:6-15.



A POSITA would understand that this Yamazaki embodiment teaches the use of an additional insulation layer (i.e., interlayer insulation layer 1431) to be formed under insulating material 1430 (e.g., corresponding to insulating material 30). EX1002, ¶115.

Anzai also discloses “wherein the second dielectric layer (first and second planarization layers 17 and 19) comprises a passivation layer (first planarization layer 17) and a capping layer (second planarization layer 19).” EX1002, ¶116. *See* §V.C.

Anzai does not explicitly state what material(s) are used to form planarization layers 17 and 19 (other than an organic resin for layer 17). EX1003, 4:20-24. However, Anzai discloses that those layers function as the capacitance insulating film. *Id.*, 5:62-6:9. Anzai further expressly discloses that silicon nitride (SiN) can be used in the interlayer insulating film 15 that is between second capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitance element 130, and in the gate insulating film 12 between first and second capacitance electrode layers 55 and 54. *Id.*, 4:8-10, 17-24 and 40-47.

It would have been obvious to a POSITA to combine the teachings of Yamazaki and Anzai to add planarization layer 19 from Anzai to be formed on top of insulating material 30, since Yamazaki already teaches using an additional insulation layer (e.g., interlayer insulation film 1431) in a separate embodiment. EX1002, ¶118.

Anzai and Yamazaki are analogous prior art to the 121 patent, as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third

area containing a light emitting device having an organic layer between two electrode layers. *Id.*, ¶119

A POSITA would have understood the issue involved, adding another insulating layer to improve the planarization of the pixel area of Yamazaki. EX1002, ¶120. To address this issue, a POSITA would have been motivated to add planarization layer 19 from Anzai above insulating material 30 of Yamazaki because both insulating layer 30 and planarization layer 19 serve the same purpose of flattening the surface of the pixel area. EX1003, Fig. 2A, 4:8-10 and 4:17-24; EX1004, 11:22-12:52, 20:17-39, Fig. 2; EX1002, ¶120.

The modification to Yamazaki would simply involve deposition another planarization layer on top of an already existing planarization layer (e.g., insulating material 30), which would further improve the flattening purpose of the insulating material 30. EX1002, ¶121. A POSITA would have had reasonable expectation of success for combining Yamazaki and Anzai, as both references disclose forming capacitors for use with organic electroluminescent devices, and both references teach insulator films for such capacitors that comprise silicon nitride. *Id.* Moreover, combining the teachings of Yamazaki and Anzai would involve known methods that would have yielded predictable results. *Id.*

D. Claim 4

The combination of Yamazaki and Anzai renders obvious “the device of claim 3 (*see* claim 3 above) wherein at least one of the passivation layer (insulating material 30 of Yamazaki) and the capping layer (planarization layer 19 of Anzai) comprises silicon nitride.” EX1002, ¶122-124.

It would have been obvious to a POSITA to combine the teachings of Yamazaki and Anzai to add planarization layer 19 from Anzai to be formed on top of insulating material 30, as capping layer and passivation layer respectively. EX1002, ¶123. *See* §VII.C.

Yamazaki teaches that silicon nitride is a suitable material for insulation layer 30. EX1004, 11:45-50 (“The insulating material 30 may be a photosensitive or non-photosensitive organic material (such as polyimide, acrylate, polyamide, polyimide amide, resist, or benzocyclobutene), an inorganic material (such as silicon oxide, silicon nitride, or silicon oxynitride) with a CVD method, a sputtering method, or coating method, or a laminate thereof.” Therefore, Yamazaki discloses that at least the passivation layer (insulating material 30 of Yamazaki) comprises silicon nitride. EX1002, ¶124.

E. Claim 5

The combination of Yamazaki and Anzai renders obvious “the device of claim 1 (*see* claim 1), wherein the second conductive layer (electrode 46 of

Yamazaki) and the fifth conductive layer (anode 28a of Yamazaki) both comprise indium tin oxide (ITO).” EX1002, ¶125-132.

Yamazaki discloses anode 28a (which corresponds to the fifth conductive layer) can be formed of ITO (indium tin oxide alloy). EX1004, 20:6-12, Fig. 2.

Yamazaki does not expressly disclose that electrode 46 (which corresponds to the second conductive layer) is formed of ITO. Yamazaki discloses that electrode 46 can be formed using Al, Ti, Mo, W and the like, such as a lamination film of AL and TI. EX1004, 19:53-60. However, in addition to anode 28a, Yamazaki discloses that other electrodes can be formed of ITO, including the cathode electrode 1239 of the embodiment of Figs. 13A-13C (*Id.*, 31:43-52), the anode electrode 1336(a) of the embodiment of Fig. 14 (*Id.*, 35:36-38), and anode electrode 1428(a) of the embodiment of Figs. 15A-15B (*Id.*, 36:16-23). Yamazaki also shows that both anode 28a and electrode 46 are formed directly on the same insulation film 22. *Id.*, Fig. 2.

Anzai discloses an electroluminescent (“EL”) display device, with the first and second capacitors of claim 1, including electrode layer 71 that corresponds to the second conductive layer. *See* §V.A.4. Anzai also discloses the light emitting device of claim 1, including anode layer 61 that corresponds to the fifth conductive layer. *See* §V.A.6. Anzai teaches that both electrode layer 71 and anode layer 61 both comprise ITO. §V.D.

It would have been obvious to a POSITA to combine the teachings of Yamazaki and Anzai to use ITO as the material for the **electrode 46** since ITO was a well-known conductive material used for light emitting device electrodes, and **electrode 46** could be deposited at the same time as **anode 28a** for an efficient manufacturing process flow. EX1002, ¶129.

Anzai and Yamazaki are analogous prior art to the 121 patent, as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third area containing a light emitting device having an organic layer between two electrode layers. *Id.*, ¶130.

A POSITA would have understood the issue involved, namely what material(s) can be used to form **electrode 46** and **anode 28a** of Yamazaki. EX1002, ¶131. To address this issue, a POSITA would have investigated what conductive material(s) would be appropriate. *Id.* A POSITA would have been motivated to use ITO to form at least **electrode 46** and **anode 28a** of Yamazaki because (1) Yamazaki already teaches using ITO for **anode 28a** (EX1004, 20:6-12, Fig. 2), (2) Yamazaki teaches that **electrode 46** could be formed at the same time as **anode 28a** (given both **electrode 46** and **anode 28a** are directly formed on the same layer, namely, on insulation film 12) (*Id.*, Fig. 2), and (3) Anzai teaches using the same ITO material for the same two corresponding electrode layers (**anode layer 61** and

combined **electrode layer 70/71**) (EX1003, 5:14-25; Figs. 3A-3B, 5:55-57);
EX1002, ¶131.

The modification to Yamazaki would simply involve selecting the same conductive material for **electrode 46** as **anode 28a**, which could be formed by the same process. EX1002, ¶132. A POSITA would have had a reasonable expectation of success in combining Anzai and Yamazaki, as both references disclose forming capacitors for use with organic electroluminescent devices, and both references teach using ITO for the anode layer. *Id.* Moreover, because combining the teachings of Yamazaki and Anzai would involve known methods where it would have yielded predictable results. *Id.*

F. Claim 6

The combination of Yamazaki and Anzai renders obvious “the device of claim 1 (*see* claim 1), wherein the second dielectric layer comprises a layer of passivation silicon nitride (Yamazaki’s insulating material 30) and a second organic layer (Yamazaki’s **EL layer 31**) formed on the layer of passivation silicon nitride (Yamazaki’s insulating material 30), the second organic layer (Yamazaki’s **EL layer 31**) comprising the same material as the first organic layer (Yamazaki’s **EL layer 31**).” EX1002, ¶133-135.

The 121 patent provides no meaning for “passivation layer.” In fact, the 121 patent discloses silicon nitride (SiN) as the sole example for this layer. For the

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Therefore, the EL layer 31 in the first area comprises the same organic material as the EL layer 31 in the third area, because they are same layer. EX1002, ¶135.

G. Claim 7

The combination of Yamazaki and Anzai renders obvious “the device of claim 1 (*see* claim 1), wherein the second dielectric layer (Yamazaki’s modified insulating material 30) comprises a passivation layer (Yamazaki’s insulating material 30), a capping layer (Anzai’s planarization layer 19) on the passivation layer and a second organic layer (Yamazaki’s EL layer 31) formed on the capping layer, at least one of the passivation layer (insulating material 30) and the capping layer (Yamazaki’s insulating material 30) comprising silicon nitride, and the second organic layer (Yamazaki’s EL layer 31) comprising the same material as the first organic layer (Yamazaki’s EL layer 31).” EX1002, ¶136.

See §§VII.C, VII.D, and VII.F. EX1002, ¶136.

VIII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. 35 U.S.C. § 314(a) Analysis

The *Fintiv* factors (enumerated below) weigh against discretionary denial. IPR2020-00019, Paper 11, 5-6 (PTAB Mar. 20, 2020) (precedential).

1. Stay

This factor is neutral because no party has requested a stay. *Sand Revolution II, LLC. v. Continental Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020).

2. Trial Date

No trial date has been set yet in the Litigation. Thus, this factor weighs against a discretionary denial.

3. Parallel Proceeding

Petitioner has not yet answered the Complaint. Accordingly, this factor weighs against a discretionary denial.

4. Issue Overlap

Petitioner challenges 7 claims. The Complaint in the Litigation explicitly asserts only 1. Accordingly, this IPR addresses significantly more invalidity issues than the Litigation and, therefore, this factor weighs against a discretionary denial.

5. Same Party

Because Petitioner and the PO are the parties in the Litigation, and because this Board is likely to reach the merits around the same time as the district court, this factor weighs slightly against discretionary denial. *See NVIDIA Corp. v. Invensas Corp.*, IPR2020-00603, Paper 11, at 23.

6. Other Considerations

Other considerations weigh strongly against a discretionary denial. The Challenged Claims are clearly invalid, Petitioners have not previously challenged any related patents based on the references relied upon in this petition, and the patent has never been challenged in a post-issuance proceeding. Thus, this factor weighs against a discretionary denial.

Even if the Board were to determine that *Fintiv* factors on balance weigh in favor of denial, institution should nonetheless be granted because this Petition satisfies the compelling merits standards. Interim Guidance at 4; *Vizio, Inc. v. Maxell, Ltd.*, IPR2022-01458, Paper 8, at 62.

B. 35 U.S.C. § 325(b) Analysis

Applying the two-part framework discussed in *Advanced Bionics, LLC v. Med-El Elektromedizinische Gerate GMBH*, IPR2019-01469, Pap. 6, *8-9, the Board should not exercise its §325(d) discretion to deny institution.

None of the challenges are substantially the same as those considered during prosecution. In the event that the challenges herein are found to be based on prior art that is the same as or cumulative to prior art considered by the examiner during prosecution, the examiner has made a clear error in allowing the claims over such prior art. This is at least because the challenges in this Petition satisfy the compelling merits standard, and allowing the claims over such prior art is therefore clear error.

IX. COMPLIANCE WITH FORMAL REQUIREMENTS

A. Mandatory Notices Under 37 C.F.R. §§ 42.8(b)(1)-(4)

1. Real Party-In-Interest

BOE Technology Group Co., LTD is the real party-in-interest.

2. Related Matters

The 121 patent is subject to the following actions: *Optronic Sciences LLC v. BOE Technology Group Co., LTD*, 2:23-cv-00549 (EDTX).

3. Lead and Backup Counsel

Lead Counsel	Backup Counsel
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4. Service Information

Please address correspondence to counsel at the addresses above. Petitioner consents to electronic service to: dla-boe-optronicsciences-IPR@us.dlapiper.com and the email addresses listed above.

B. Proof of Service on the Patent Owner

In accordance with 37 C.F.R. §§42.6(e) and 42.105, as identified in the attached Certificate of Service, a copy of this Petition in its entirety is being served

electronically (by agreement) on counsel for Patent Owner in the District Court
Litigation.

C. Power of Attorney

Powers of attorney are being filed with designation of counsel in accordance
with 37 C.F.R. § 41.10(b).

D. Standing

In accordance with 37 C.F.R. §42.104(a), Petitioner certifies that the 121
patent is available for *inter partes* review and that Petitioner is not barred or
estopped from requesting an *inter partes* review challenging the patent claims on
the grounds identified in this Petition.

E. Fees

The undersigned authorizes the Director to charge the fee specified by 37
C.F.R. § 42.15(a) and any additional fees that might be due in connection with this
Petition to Deposit Account No. 07-1896.

X. CONCLUSION

All Challenged Claims of the 121 patent should be found unpatentable for the reasons discussed in this Petition.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 10,150 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, claim listing, and exhibits.

Date: July 12, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies pursuant to 37 C.F.R. §§ 42.6(e) and 42.105 that on July 12, 2024, a true and correct copy of the Petition for Inter Partes Review of U.S. Patent No. 7,586,121 was served by emailing a copy of same (by agreement) to the following attorneys for the Patent Owner:

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