

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., LTD.

Petitioner

v.

Optronic Sciences LLC

Patent Owner

Inter Partes Review No.: IPR2024-01132

**DECLARATION OF DR. DEAN NEIKIRK IN SUPPORT OF PETITION
FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,586,121**

I hereby declare under penalty of perjury under the laws of the United States of America that the following is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code.

July 11, 2024

Date



Dr. Dean Neikirk

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INDEX OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 7,586,121 (121 Patent)
1002	Declaration of Dean Neikirk in Support of Petition for Inter Partes Review of U.S. Patent 7,586,121 (121 Patent)
1003	U.S. Patent No. 7,330,168 (“Anzai”)
1004	U.S. Patent No. 6,992,332 (“Yamazaki”)
1005	File History of U.S. Patent No. 7,586,121
1006	Polysilicon TFT Technology for Active Matrix OLED Display by Mark Stewart, et. al., (“Stewart”)
1007	U.S. Patent Publication No. 2003/0067266 (“Kim”)
1008	U.S. Patent Publication No. 2006/0208979 (“Fish”)
1009	PCT Publication No. WO 2003/71511 (“Choi”)
1010	U.S. Patent No. 6,476,419 (“Yasuda”)

CHART OF CLAIMS
[1pre] An electroluminescence (EL) device, comprising:
[1a] a substrate; and
[1b] a plurality of pixels formed on the substrate, each pixel being in a respective pixel area, each pixel area including at least a first area, a second area, and a third area, wherein each pixel includes:
[1c] at least a first capacitor and a second capacitor in the first area, the first capacitor including a first conductive layer formed over a first gate oxide layer, a first dielectric layer over the first conductive layer, and a second conductive layer over the first dielectric layer, and the second capacitor including the second conductive layer, a second dielectric layer over the second conductive layer, and a third conductive layer over the second dielectric layer;
[1d] a transistor in the second area, the transistor including a first semiconductor layer formed on the substrate, the first gate oxide layer over the first semiconductor layer, and a fourth conductive layer over the first gate oxide layer, wherein the fourth conductive layer is formed of the same conductive film as the first conductive layer, and wherein both the first conductive layer and the fourth conductive layer are directly formed on the gate oxide layer; and
[1e] a light emitting device in the third area, the light emitting device including a fifth conductive layer, a first organic layer over the fifth conductive layer, and a sixth conductive layer over the first organic layer, wherein the sixth conductive layer is formed of the same conductive film as the third conductive layer.
[2] The device of claim 1, each pixel further comprising a seventh conductive layer in the second area for providing contact to the first semiconductor layer.
[3] The device of claim 1, wherein the second dielectric layer comprises a passivation layer and a capping layer.
[4] The device of claim 3, wherein at least one of the passivation layer and the capping layer comprises silicon nitride.
[5] The device of claim 1, wherein the second conductive layer and the fifth conductive layer both comprise indium tin oxide (ITO).
[6] The device of claim 1, wherein the second dielectric layer comprises a layer of passivation silicon nitride and a second organic layer formed on the layer of passivation silicon nitride, the second organic layer comprising the same material as the first organic layer.
[7] The device of claim 1, wherein the second dielectric layer comprises a passivation layer, a capping layer on the passivation layer and a second organic layer formed on the capping layer, at least one of the passivation layer and the capping layer comprising silicon nitride, and the second organic layer comprising the same material as the first organic layer.

I. INTRODUCTION

I, Dean Neikirk, declare as follows:

1. My name is Dean Neikirk. I have been asked by Petitioner BOE Technology Group Co. Ltd. (“Petitioner”) to provide my expert opinions in support of the above-identified petition for *inter partes* review of claims 1-7 (“Challenged Claims”) of U.S. Patent No. 7,586,121 (“121 patent,” EX1001), owned by Optronic Sciences LLP (“PO”), pursuant to 35 U.S.C. §§311–19 and 37 C.F.R. §42.100.

2. I currently hold the opinions set forth in this declaration.

3. In summary, it is my opinion that the references cited below anticipate or render obvious the Challenged Claims. My detailed opinions on the claims are set forth below.

4. I am being compensated for my time at the rate of \$800 per hour. This compensation is not contingent upon my performance, the outcome of this matter, or any issues involved in or related to this matter.

II. BACKGROUND AND QUALIFICATION

5. My qualifications generally are set forth in my Curriculum Vitae, which is attached as Exhibit A and also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

6. I am currently an emeritus Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin, holding the Emeritus Cullen Trust for Higher Education Professorship in Engineering. I received a B.S. in Physics and Mathematics from Oklahoma State University in 1979, an M.S. in Applied Physics from the California Institute of Technology in 1981, and a Ph.D. in Applied Physics from the California Institute of Technology in 1984. Until January 2021, I was a tenured professor and endowed chair in the Cockrell School of Engineering at the University of Texas at Austin, where I have been a member of the engineering faculty since 1984. From 1992 to 2020 I held the Cullen Trust for Higher Education Professorship in Engineering at the University of Texas. From 2014 to 2020 I was the Associate Dean of Graduate Studies where I oversaw graduate student services for over 78 doctoral programs and 116 master's degree programs. I have also served as the Graduate Advisor of the Department of Electrical and Computer Engineering (ECE) at UT-Austin, an Associate Chairman of the ECE Department, the Chair of the UT-Austin Graduate Assembly, the Chair of the UT-Austin Faculty Council, and the Secretary of the General Faculty at UT-Austin.

7. In 1985, I established the Microelectronics Fabrication Teaching Laboratory at The University of Texas at Austin, which continues to this day to provide undergraduate and graduate students with hands-on experience in IC

fabrication. I have taught many courses in integrated-circuit fabrication, microwave devices, IC packaging, electromagnetics, computer aided design methods for circuit simulation, sensors of all sorts, and micro-electromechanical systems. In recognition of my research and classroom teaching accomplishments, I received the 1984-85 Engineering Foundation Faculty Award from the University of Texas at Austin Engineering Foundation Advisory Council, the 1985-90 General Motors Foundation Centennial Teaching Fellowship, the 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, the 1990-1992 Temple Foundation Endowed Faculty Fellowship, the 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, the 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, and the 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching. In recognition of my service to the University of Texas at Austin I also received the 2015 University of Texas at Austin Civitatis Award.

8. My research over the last thirty-five years has concentrated heavily in the areas of optical systems, microelectronics, semiconductor devices, IC fabrication, and new sensors. This research work has been funded by many agencies, focusing on the fabrication and modeling of semiconductor devices, electromagnetic devices and detectors, chemical sensors, temperature sensors,

proximity sensors, and pressure sensors, as well as research on the high frequency properties of transmission lines, RF devices, and infrared to terahertz detectors for use in focal plane imaging arrays. My research related to the development of new chemical sensors (an “electronic taste” sensor) was selected for a commercialization venture between The University of Texas and two outside start-up companies.

9. My earliest research was in the interaction of light with optically active materials, including color centers in crystals for use as light emitters. Each of my academic degrees involved significant studies in solid state physics, semiconductor devices, electrical engineering, electronic systems, electromagnetics, optics, radio frequency systems, and antennas. For example, courses relating to these fields that I took include two years of study in electromagnetics and optics, one year of study in solid state and semiconductor physics, as well as four years of graduate research in electronic devices, antenna design, antenna fabrication, and optical systems. My Ph.D. thesis was on the design and fabrication of high frequency electromagnetic detectors and quasi-optical imaging antenna arrays, including research on integrated-circuit fabrication, semiconductor devices, integrated circuits, antennas, sensors, and IC packaging. I designed and fabricated the first monolithic integrated-circuit imaging antenna array for use at wavelengths in the far infrared (sometimes referred to as the

terahertz) region of the electromagnetic spectrum. For this work on the first high resolution focal plane antenna array for use at wavelengths between 0.1 mm and 1 mm I was awarded the 1984 Marconi International Fellowship Young Scientist Award “for contributions to the development of millimeter wave integrated circuits especially in the area of detectors and imaging arrays.” In recognition of my early research efforts I received the 1985–1986 IBM Corporation Faculty Development Award, and the 1986 National Science Foundation Presidential Young Investigator Award.

10. As represented by the publications listed in my CV, I have extensive experience with microelectronics, semiconductors, and IC fabrication. My academic research has included a substantial body of work on new designs for imaging arrays, including the design and fabrication of arrays of pixels for use in the infrared spectrum. This work included new research on focal plane arrays made up of wavelength-selective pixels to allow for “color vision” in the infrared portion of the electromagnetic spectrum. In addition to optical sensing, my work also involved the growth of compound semiconductor materials used to generate light in light emitting diodes. Later advances in these materials have led to their use in light emitting displays. My work has involved study of optical properties of material, including the interaction with and generation of light in semiconductors and other materials. I have over 30 years of experience in design, modeling and

fabrication of stacked and interdigitated capacitors for integration with semiconductor devices. I have taught MOSFET fabrication for over 30 years, including teaching labs that have made MOSFETs.

11. I am a senior member of the Institute of Electrical and Electronics Engineers (IEEE) and served as Associate Editor for Solid State and VLSI Electronics, IEEE Transactions on Education from March 1991 through October 1994.

12. Through my work on electronic systems and innovations in other related fields, I have been named an inventor on 17 U.S. patents. These are summarized in my curriculum vitae.

13. I have also co-authored over 250 technical papers in international journals and conferences and presented over 30 invited lectures and professional society presentations. My publications have addressed technologies such as integrated circuits for antenna arrays, multilayer interconnection lines for high speed digital integrated circuits, determining conductor loss in transmission lines, optical and electromagnetic devices for infrared detection, RF oscillator circuits, memory-switching double-barrier quantum-well diodes circuits, RF and infrared detection circuits, and other topics related to semiconductor and IC fabrication.

III. DOCUMENTS AND OTHER MATERIALS RELIED UPON

1. In forming the opinions set forth in this declaration, I have reviewed the documents in the following table:

Exhibit No.	Description
1001	U.S. Patent No. 7,586,121 (121 Patent)
1003	U.S. Patent No. 7,330,168 (“Anzai”)
1004	U.S. Patent No. 6,992,332 (“Yamazaki”)
1005	File History of U.S. Patent No. 7,586,121
1006	Polysilicon TFT Technology for Active Matrix OLED Display by Mark Stewart, et. al., (“Stewart”)
1007	U.S. Patent Publication No. 2003/0067266 (“Kim”)
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1009	PCT Publication No. WO 2003/71511 (“Choi”)
1010	U.S. Patent No. 6,476,419 (“Yasuda”)

2. Additionally, I have utilized my own experience and expertise, including regarding the knowledge and capabilities of a person of ordinary skill in the relevant art in the timeframe of the claimed priority date of the 121 patent.

IV. STATUTORY GROUNDS FOR CHALLENGE

3. In this declaration, I offer opinions on the following grounds that are the basis for this IPR proceeding:

Ground	Claims	Stat. Basis	Prior Art
1	1-3 and 5	35 U.S.C. §102	Anzai
2	4	35 U.S.C. §103	Anzai in view of Yamazaki
3	1-7	35 U.S.C. §103	Yamazaki in view of Anzai

V. RELEVANT PATENT LAW AND LEGAL STANDARDS

A. Date of Invention

4. I have been asked to use the date of the filing of the earliest application to which priority is claimed (i.e., December 7, 2004) as the date of invention for purposes of my analysis.

B. Anticipation

5. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 102 if a prior art disclosure teaches every element required by the claim, either expressly or inherently. The identical invention must be shown in as complete detail as is contained in the claim. When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art.

C. Obviousness

6. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art to which the subject matter pertains. Obviousness, as has been explained to me, is based on (i) the scope and content of the prior art, (ii) the differences between the prior art and the claim, (iii) the level of ordinary skill in the art, and (iv) any secondary indicia of non-obviousness (*e.g.*,

“secondary considerations” such as commercial success in the marketplace of the claimed invention), to the extent that they exist.

7. I further understand that obviousness may be demonstrated by showing that it would have been obvious to combine the teachings of more than one item of prior art. In determining whether a piece of prior art could have been combined with other prior art or with other information within the knowledge of a person having ordinary skill in the art, the following are examples of approaches and rationales that may be considered:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of a known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- Applying a technique or approach that would have been obvious to try (choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success);

- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a person having ordinary skill in the art; and
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

8. I further understand that an invention may be obvious if one of ordinary skill in the art, facing a wide range of needs created by developments in the field, would have seen an obvious benefit to the solutions tried by the applicant. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, it may be obvious to a person of ordinary skill to try the known options. If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious.

9. I further understand that a person of ordinary skill in the art is a hypothetical person who is presumed to be aware of all of the relevant art at the time of the invention. The person of ordinary skill may be able to fit together the

teachings of multiple patents and/or printed publications employing ordinary creativity and the common sense that familiar items may have uses in another context or beyond their primary purposes.

10. I also understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when combining or modifying the prior art. I understand this test should not be applied rigidly, but that the test can be important to avoid such hindsight.

11. I also understand that one of ordinary skill in the art must have a reasonable expectation of success in combining or modifying prior art references.

12. I also understand that all elements of a claim must be considered in an obviousness analysis.

D. Claim Construction

13. I understand that claims are construed from the perspective of a person of ordinary skill as of the effective filing date of the patent application. A “person of ordinary skill in the art” is a hypothetical person who is presumed to have known the relevant art at the time of the invention.

14. I understand that persons of ordinary skill in the art are deemed to read the claims in the context of the entire patent, including the specification and prosecution history. In other words, the terms are not considered in a vacuum.

15. I understand that the claims define the invention and the terms used in the claims are generally given the plain and ordinary meanings they would have to a person of ordinary skill in the art at the time of the effective filing date of the application. The context of a claim can be particularly helpful, and other claims may inform the meaning of a term in a particular claim.

16. I understand that claim terms are normally used consistently throughout a patent. Thus, the meaning of a term may help inform the meaning of the same term in other claims. Differences between claims may also help define the terms, although this may not be the case where the specification or prosecution history indicate that such differences do not impact the scope of the claims.

17. I understand that a patentee can act as its own lexicographer by defining a term, in the patent specification, to have specific meaning. It is my understanding that statements made to the patent office by the patentee or its legal representative during prosecution can serve to illuminate, or possibly narrow the proper scope of claim terms, and that such statements must be considered when construing the claim terms. This is sometimes referred to as disclaimer. I have taken into account these principles in my analysis.

18. I understand that reference materials that were publicly available at the time that the patent application was filed, such as dictionaries, treatises or other

technical references, may provide context and background for deciphering how one of ordinary skill in the art would have considered the terms used in the claims.

19. However, I understand that such references, as well as testimony (including this report) are generally known as “extrinsic evidence,” and are accorded less weight than evidence found within the patent and prosecution history. In addition, I understand that extrinsic evidence that is inconsistent with the claims, specification, or prosecution history should not be considered in the claim construction process.

E. Standard of Proof

20. I understand that the standard to prove unpatentability in an *inter partes* review proceeding is by a preponderance of the evidence, which means more likely than not.

VI. LEVEL OF ORDINARY SKILL IN THE ART

21. I have considered the level of ordinary skill in the art relevant to the 121 patent. I understand that factors such as the education level of those working in the field, the sophistication of the technology, the types of problems encountered in the art, the prior art solutions to those problems, and the speed at which innovations are made may help establish the level of skill in the art.

22. After reviewing the 121 patent, the relevant portions of the prosecution history of the 121 patent and its reexamination, and cited references, it

is my opinion that the relevant art of the 121 patent is in the field of electronic and optoelectronic device design.

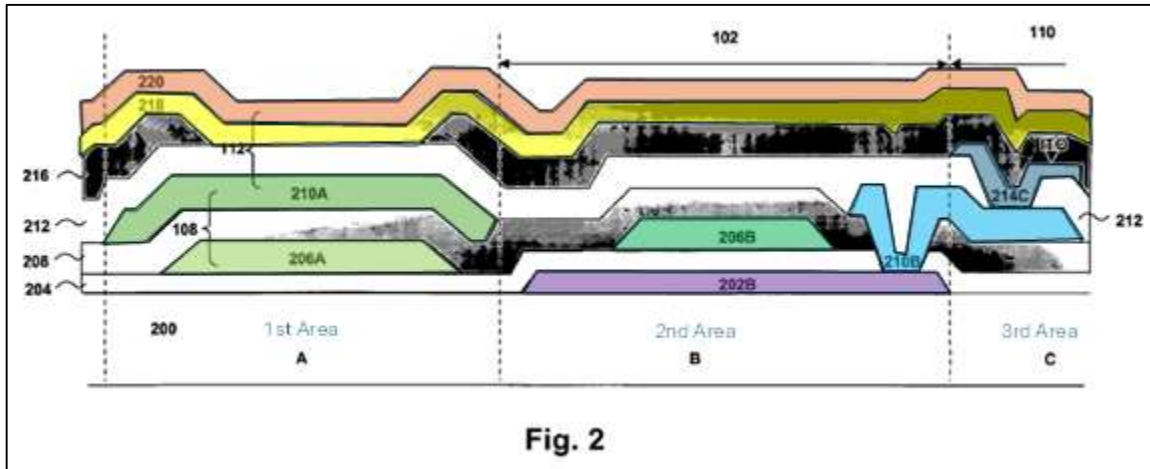
23. Based upon my knowledge of this field, I conclude that a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the 121 patent (December 7, 2004), and for that matter, at all subsequent times through the present, would have had a Bachelors’ degree in electrical engineering or a comparable field of study, plus approximately two to three years of professional experience with electronic and optoelectronic device design. Additional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education.

24. I am and was at the time of the earliest filing date at least a person of skill in the relevant art and I am able to provide insight and opinions into the understandings of such persons at all relevant times by virtue of my education, training and experience.

VII. THE 121 PATENT AND ITS PROSECUTION HISTORY

A. Overview of the 121 Patent

25. The 121 Patent was filed on December 7, 2004, published on June 8, 2006, and issued on September 8, 2009. EX1001, Face of Patent.



26. The 121 Patent, as seen in Figure 2 above (coloring has been added), is directed to an OLED device with a plurality of pixels where each pixel (100) comprises three areas formed on a substrate 200. EX1001, Abstract. In the first area, area A, a first capacitor 108 and a second capacitor 112 are formed vertically stacked above each other, where the two storage capacitors share the second conductive layer 210A to increase the storage capacitance without increasing chip area or additional masks. *Id.*, Abstract, 5:5-6:49.

27. Here, in the first area, area A, the first storage capacitor 108 comprises a first metal pattern 206A (light green), the interlayer dielectric 208, and the second metal pattern 210A (light green). The second storage capacitor 112 comprises the second metal pattern 210A, the passivation SiN layer 212 and the capping silicon nitride 216, organic layer 218 (yellow), and the third metal layer 220 (orange). *Id.*, 5:47-6:35. The two storage capacitors 108 and 112 share a common electrode (second metal pattern 210A); this configuration is commonly

referred to in the art as a tri-plate capacitor. The 121 Patent discloses that the first metal pattern 206A may be formed using an existing mask for the first metal pattern 206B and the same for second metal patterns 210A and 210B, thus reducing the number of masks needed to form the capacitors. *Id.* In addition, capacitors 108 and 112 are coupled in parallel to each other and may be collectively viewed as the storage capacitor of pixel 100 "whose capacitance is equal to the sum of the capacitance of both capacitors 108 and 112" such that capacitor 112, is coupled between the gate of transistor 102 and the cathode 220 of the EL element 110. *Id.*, 4:66-5:11.

28. In the second area, area B, the 121 Patent discloses a first metal pattern 206B, which serves as the gate of the transistor 102, and is formed over a polysilicon pattern 202B (i.e., semiconductor layer) (purple), which serves as the source and drain of transistor 102, with a gate oxide layer 204 in between. EX1001, 5:22-58; Fig. 2. The source of transistor 102 is coupled to power supply voltage V_{DD} and the drain is connected to drive the OLED element 110. *Id.*, 4:36-63. Second metal pattern 210B (blue) provides contact between polysilicon pattern 202B to the indium tin oxide ("ITO") pattern 214C of the OLED element 110 (see below). *Id.*, Fig. 2. Second metal pattern 210B is formed by depositing a layer of metal over ILD 208 and patterned, where the second metal pattern 210B contacts

polysilicon pattern 202B through a via hole in ILD 208 and gate oxide 204. *Id.*, 5:29-34; Fig. 2.

29. In the third area, area C, the 121 Patent discloses an OLED element 110 that includes an indium tin oxide ("ITO") pattern 214C (i.e., the anode) formed under a capping layer SiN 216 (black), which is formed under an organic layer 218 (yellow), which is formed under a third metal layer 220 (i.e., the cathode) (orange). EX1001, 4:58-65; 5:22-58.

30. The 121 Patent includes various embodiments where the first storage capacitor 108 and the second storage capacitor 112 comprise different combinations of insulation layer(s) between the conductive layers. *Id.*, Figs. 3-9, 11.

B. Overview of the 121 patent's File History

31. I have found at least the following from the file history that may be relevant.

32. The '121 Patent was issued on September 8, 2009, from U.S. Patent Application No. 11/005,648, which was filed on December 7, 2004. Ex. 1001, Patent Face. During prosecution, the initially filed claims went through two rounds of restrictions and elections, after which the pending claims were initially rejected under section 112 for lack of written support and indefiniteness based on the submitted specification. EX1005, Office Action dated May 04, 2007, at pp. 2-3.

The claims were further rejected under § 102 as anticipated by Yamazaki (U.S. 2002/0104995) and under § 103 as rendered obvious by Yamazaki in view of Murade (6,610,997). *Id.*, pp. 3-12. After the Final Rejection on March 25, 2008, the Applicant filed a Request for Continued Examination (RCE) and amended claims on June 12, 2008, where the language of claim 1 was entirely replaced and other claims were amended. *Id.*, Amendment and Response to Final Office Action with RCE, pp. 2-3.

33. After the Non-Final Office Action on August 15, 2008, where the Examiner made similar 112, 102, and 103 rejections as before, the Applicant conducted an interview with the Examiner and filed a response on November 17, 2008, adopting the Examiner's suggestion of amending claim 1 to include that the "first conductive layer is formed over the first gate oxide layer" in the first area, and in the second area "both the first conductive layer and the fourth conductive layer are directly formed on the gate oxide layer." *Id.*, Amendment and Response to Non-Final Office Action, pp. 2-3. The application was then allowed.

VIII. CLAIM CONSTRUCTION

34. I have applied the plain and ordinary meaning to a POSITA at the time of the 121 patent for all the terms in the Challenged Claims.

IX. OVERVIEW OF THE PRIOR ART REFERENCES

A. EX1003 – Anzai

35. U.S. Patent 7,330,168 (“Anzai”) was filed on April 30, 2003, issued February 12, 2008, and claims priority to Japanese Patent Application 2002-128008, filed on April 30, 2002. EX1003, Face of the Patent. Anzai qualifies as prior art to the 121 Patent under at least pre-AIA 35 U.S.C. § 102 (e).

B. EX1004 – Yamazaki

36. U.S. Patent 6,992,332 (“Yamazaki”) was filed on May 5, 2003, issued on January 31, 2006, and claims priority to Japanese patent application 2002-13994. EX1004, Face of the Patent. Yamazaki qualifies as prior art to the 121 Patent under at least pre-AIA 35 U.S.C. § 102 (e).

X. GROUND 1: CLAIMS 1-3 AND 5 ARE ANTICIPATED BY ANZAI

37. In my analysis of each claim term, I begin with a quotation of the claim term in which I insert parentheticals explaining how the prior art reference(s) disclose the claim term. That is followed by a more detailed discussion on why I believe the claim term is disclosed by the prior art reference(s).

A. Claim 1

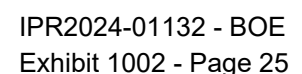
1. [1pre]

38. To the extent that the preamble is limiting, Anzai teaches “[a]n electroluminescence (EL) device (Anzai’s electroluminescent display device).”

EX1003, 1:6-17. More particularly, Anzai is directed to reducing the forming area of a storage capacitor for holding the video signal supplied to a transistor to improve the display quality of an electroluminescent display device with a storage capacitance element for holding a video signal supplied to the gate of a driving transistor (TFT) for an organic EL element. *Id.*, Abstract.

40. Anzai teaches the use of “a substrate (Anzai substrate 10).”

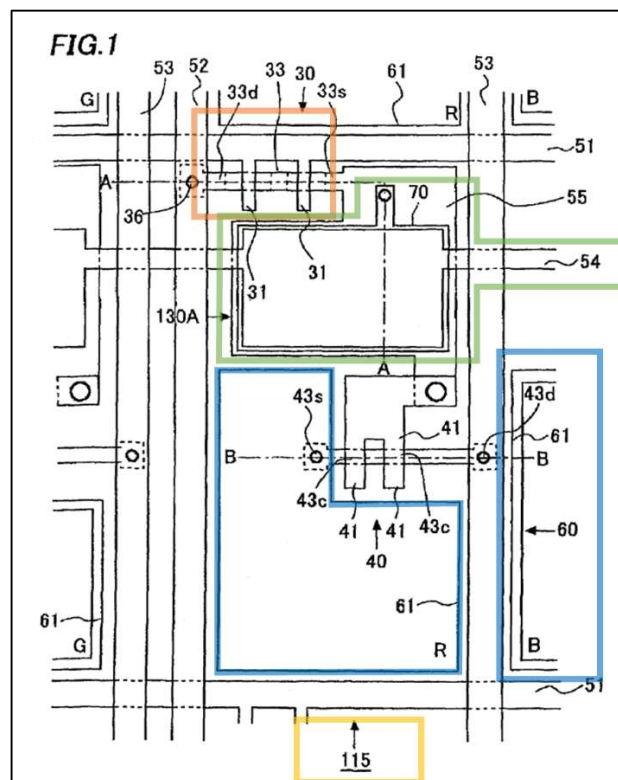
EX1003, 3:57-61; Figs. 2A-2B and 3A-3B.



3. [1b]

42. Anzai discloses “a plurality of OLED pixels (RGB OLED pixels), formed on the substrate (10), each pixel being in a respective pixel area (115), each pixel area including at least a first area (Capacitor Area), a second area (Transistor Area), and a third area (OLED Area), wherein each pixel includes (see [1c]-[1e]).”

43. Anzai discloses a plurality of pixel portions 115, disposed in a matrix configuration forming a display region. EX1003, 3:28-31; Fig. 1.

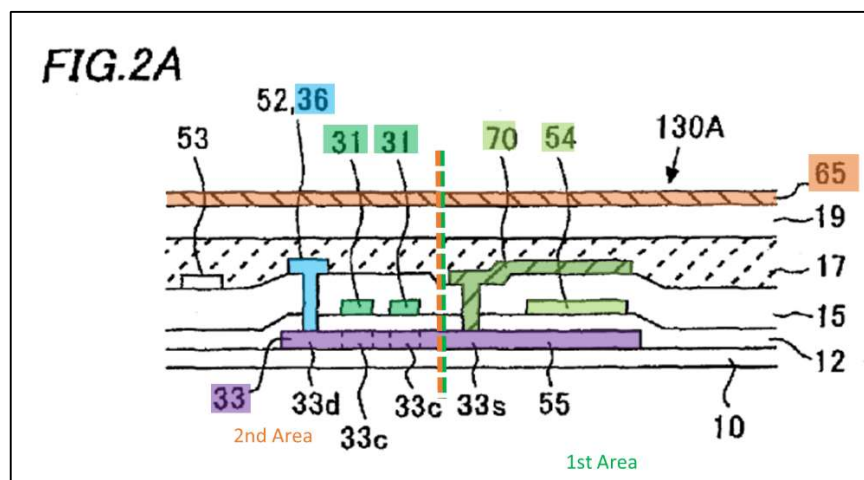


Each pixel portion 115 then comprises capacitors 130A (shown), 130B (not shown) in the first area (Capacitor Area) (see [1c]) a driving transistor 40 in the second area (Transistor Area) (see [1d]) and organic EL element 60 in the third area (OLED Area) (see [1e]). *Id.*, 3:32-40.

4. [1c]

44. Anzai discloses “at least a first capacitor (layers 54, 15, 70, 71) and a second capacitor (layers 70, 71, 17, 19, 65) in the first area, the first capacitor including a first conductive layer (electrode layer 54) formed over a first gate oxide layer (gate insulating film 12), a first dielectric layer (interlayer insulating film 15) over the first conductive layer (electrode layer 54), and a second conductive layer (electrode layer 70 or 70/71) over the first dielectric layer (interlayer insulating film 15), and the second capacitor including the second conductive layer (electrode layer 70 or 70/71), a second dielectric layer (first 17 and second 19 planarization films) over the second conductive layer, and a third conductive layer (cathode layer 65) over the second dielectric layer.”

45. As seen in Fig. 2A below, Anzai discloses a first embodiment having the first capacitor within the first area that includes electrode layer 54 and electrode layer 70 with insulating film 15 sandwiched in between. EX1003, Fig. 2A, 4:25-47. Electrode layer 54 is formed over gate insulating film 12, which Anzai discloses can be made from “a SiO₂ film” (i.e., an oxide layer). *Id.*, 3:61-67; Fig. 2A.



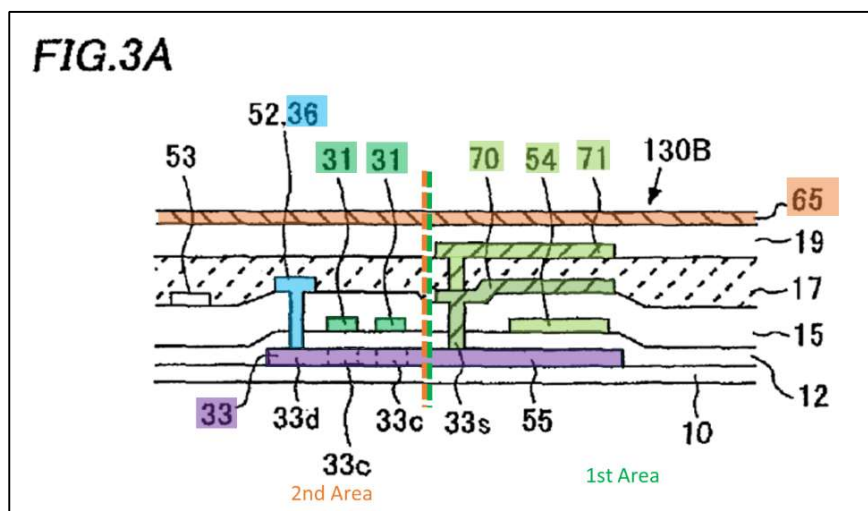
The fact that Anzai additionally discloses electrode layer 55 providing additional capacitance storage relative to electrode layer 54 is not relevant to claim 1. A POSITA would understand that electrode layer 54 and electrode layer 70 with insulating film 15 sandwiched in between form a capacitor on which claim 1 reads, and electrode layer 55 and electrode layer 54 with insulating film 12 sandwiched in between form another capacitor (which is not needed to meet the limitations of claim 1). Claim 1 is an open ended “comprising” claim to “at least” a first and second capacitor, and the capacitors themselves are recited as “including” the recited layers. EX1001, claim 1. Thus, a device with the claimed capacitors including the claimed layers practices the claims even if the device includes additional capacitors and the capacitor includes additional layers.

46. The second capacitor is formed between electrode layer 70 and cathode layer 65 with an insulating layer comprising first and second planarization films 17 and 19. *Id.*, Fig. 2A, 4:48-51, 5:62-67 (“In the first embodiment, a

capacitance is formed between the third capacitance electrode layer 70 and the cathode layer 65 when the cathode electrode is used as a fourth capacitance electrode layer. Both the first planarization film 17 and the second planarization film 19 function as the capacitance insulating film in this configuration.”).

47. Anzai discloses that each of the above identified first and second capacitors functions as a capacitor. EX1003, 4:30-47 (first capacitor), 4:48-51 and 5:58-65 (second capacitor). Anzai further discloses that interlayer insulating film 15 is formed of a SiO₂ film, a SiN film and a SiO₂ film, sequentially deposited. *Id.*, 4:60-63. Both the first planarization film 17 and second planarization film 19 “function as the capacitance insulating film.” *Id.*, 5:65-67. A POSITA would have understood the first and second capacitors share a “second conductive layer” as recited in claim 1 since the **electrode layer 70** is common to both capacitors.

48. In addition, Anzai discloses a second embodiment (Fig. 3A) that also satisfies this limitation. The embodiment of Fig. 3A is that same as that of Fig. 2A except for the capacitance electrode structure that adds electrode layer 71. EX1003, 5:39-41. As seen in Figure 3A below, the formation of the first capacitor within the first area is between **electrode layer 54** stacked below the **combined electrode layer 70/71** with a gate insulating film 15 sandwiched in between. EX1003, Fig. 3A, 5:34-57.



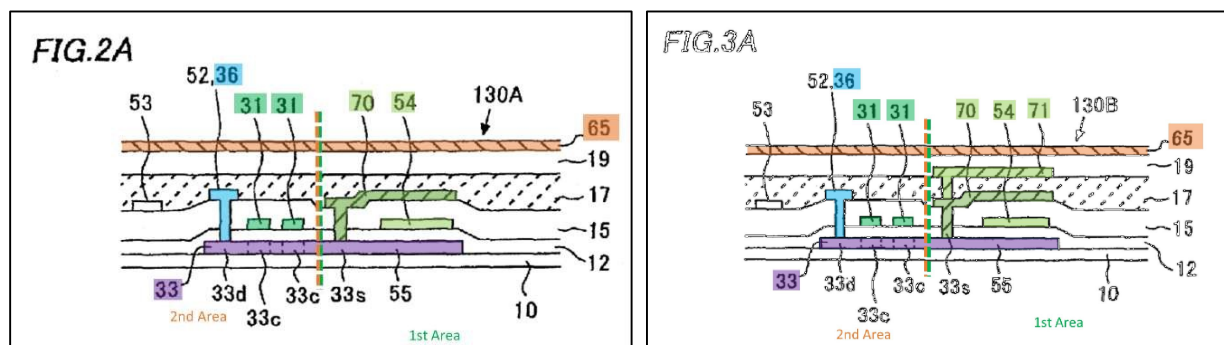
The second capacitor is formed between the combined electrode layer 70/71 and the cathode layer 65, with second planarization layer 19 sandwiched in between. *Id.*, 5:52-61 and 5:67-6:3. Here, a POSITA would have understood the first and second capacitors share a “second conductive layer” as recited in claim 1 since the electrode layer 71 extends over and is electrically connected to electrode layer 70 (i.e., electrode layers 70 and 71 form a U-shaped conductive layer that is shared between the first and second capacitors). As with the first embodiment, the fact that Anzai additionally discloses an additional electrode layer 55 is not relevant.

49. Anzai discloses the second embodiment (Figs. 3A-3B) is identical to the first embodiment (Figs. 2A-2B) other than the addition of electrode layer 71 for the capacitor. EX1003, 5:34-43. Thus, all references herein to Anzai to either embodiment apply equally to both embodiments, except where explicitly stated otherwise.

5. [1d]

50. Anzai discloses “a transistor (pixel selecting TFT 30) in the second area (**Transistor Area**), the transistor including a first semiconductor layer (**active layer 33**) formed on the substrate (substrate 10), the first gate oxide layer (gate insulating film 12) over the first semiconductor layer (**active layer 33**), and a fourth conductive layer (**gate electrode 31**) over the first gate oxide layer (gate insulating film 12), wherein the fourth conductive layer (**gate electrode 31**) is formed of the same conductive film as the first conductive layer (**first electrode layer 54**), and wherein both the first conductive layer (**first electrode layer 54**) and the fourth conductive layer (**gate electrode 31**) are directly formed on the gate oxide layer (gate insulating film 12).”

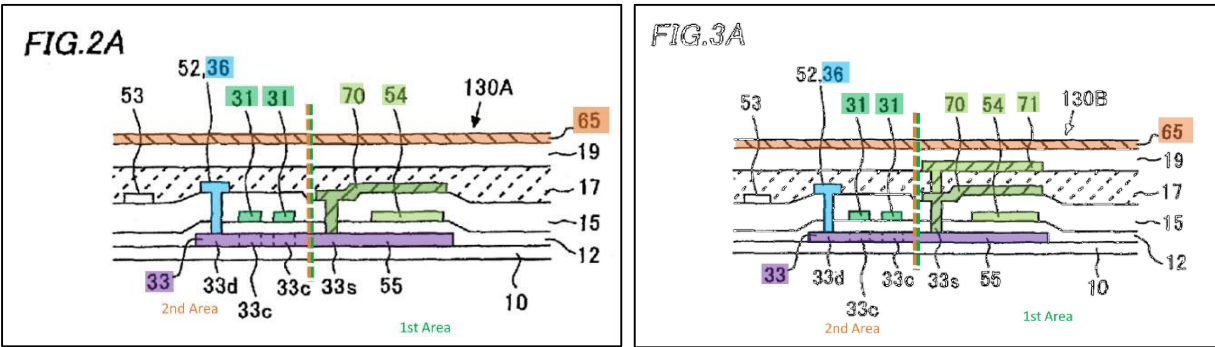
51. Anzai teaches that in the second, **Transistor Area**, as seen in Fig. 1 (*see* [1a]) and in Figs. 2A and 3A annotated below (e.g., on the left side of the orange dashed line), pixel selecting TFT 30 is formed by **gate electrode 31** above an **active layer 33** with a gate insulating film 12 in between. EX1003, Figs. 2A and 3A; 4:1-25 and 37-40.



Drain electrode 36 is connected to the drain 33d, and the third capacitance electrode layer 70 is connected to the source 33s, of the TFT 30. *Id.*

52. Anzai discloses the device is fabricated using sequentially deposited layers. *Id.* Anzai discloses depositing on substrate 10 an amorphous silicon film, which is re-crystallized to form a polycrystalline silicon film that functions as the active layer 33. *Id.*, 4:1-7. A single or multiple layers of SiO₂ and SiN are formed on layer 33 to serve as the gate insulating film 12. *Id.*, 4:8-10. A gate signal line 51 also working as the gate electrode 31 is disposed on gate insulating film 12. *Id.*, 4:11-14; Figs. 2A and 3A. A POSITA would have understood the active layer 33 to be the first semiconductor layer, the insulating film 12 to be the gate oxide layer that is deposited over the first semiconductor layer, and the gate electrode 31 to be the fourth conductive layer.

53. Anzai discloses that gate electrode 31 (the fourth conductive layer) is formed of the same conductive film as the first electrode layer 54 (the first conductive layer) because each is disclosed as being formed directly on the same underlying structure (i.e., gate insulating layer 12), they are formed by the same process, and they are formed of the same material. EX1003, Figs. 2A, 3A, 4:25-40 ("The second capacitance electrode layer 54 is made of Cr or Mo, and formed in the same layer as the gate electrode 31 and by the same process as the gate electrode 31.")

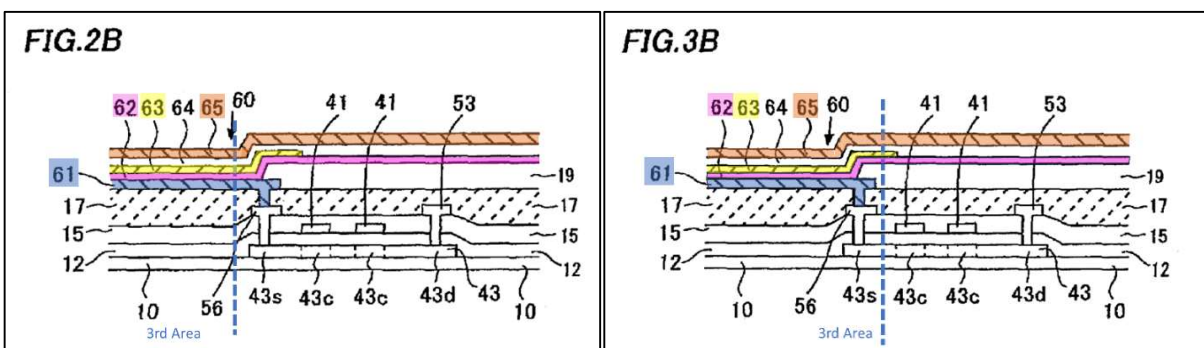


A POSITA would understand that forming electrode layers in the same layer, by the same process, with the same material, would mean these two electrode layers are formed of the same conductive film.

6. [1e]

54. Anzai teaches “a light emitting device (organic EL element 60) in the third area (OLED Area), the light emitting device including a fifth conductive layer (anode layer 61), a first organic layer (emissive layer 63) over the fifth conductive layer (anode layer 61), and a sixth conductive layer (cathode layer 65) over the first organic layer (emissive layer 63), wherein the sixth conductive layer (cathode layer 65) is formed of the same conductive film as the third conductive layer (cathode layer 65).”

55. Anzai discloses, in the third OLED Area (see [1a]) and as seen in Figs. 2B and 3B below (e.g., the left side of the blue dashed line), an EL element is formed with an anode layer 61 (that is connected to the active layer source 43s through source electrode 56), an emissive layer 63 over anode layer 61, and a cathode layer 65 over the emissive layer 63. EX1003, 5:3-33; Figs. 2B, 3B.



56. Anzai provides the following details of the organic EL element 60:

“The organic EL element 60 includes the **anode layer 61** made of the transparent electrode such as ITO (Indium Tin Oxide), a **hole transportation layer 62** having a first hole transportation layer made of MTDATA (4,4-bis(3-methylphenylphenylamino)biphenyl) and a second hole transportation layer made of TPD (4,4,4-tris (3-methylphenylphenylamino)triphenylamine), an **emissive layer 63** made of Bebq2 (bis(10-hydroxybenzohquinolinato)beryllium) including quinacridone derivative, an electron transportation layer 64 made of Bebq2, and the **cathode layer 65** made of either magnesium-indium alloy, aluminum or aluminum alloy.” *Id.*, 5:14-25.

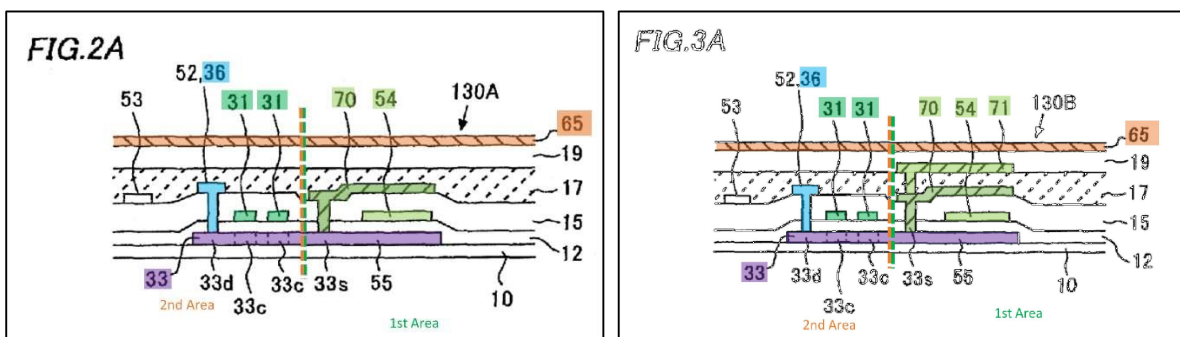
A POSITA would understand that **emissive layer 63** is an organic layer because Anzai explains that during operation, organic molecules in the emissive layer are activated. *Id.*, 5:26-29. A POSITA would also have understood that intervening layers 62 and 64 in the organic EL element 60 do not change the relative positioning of the layers as called for in claim 1, namely, that the **emissive layer 63** is over the **anode layer 61**, and the **cathode layer 65** is over the **emissive layer 63**.

57. Finally, a POSITA would have further understood that the sixth conductive layer (i.e., **cathode layer 65**) of the light emitting device of Anzai is formed from the same conductive film as the third conductive layer of the second capacitor of Anzai because as shown above in section [1c], the same film (i.e., **cathode layer 65**) that serves as third conductive layer also serves as the sixth conductive layer (see above). Thus, the third and sixth conductive layers are literally the same layer in Anzai (i.e., **cathode layer 65**).

B. Claim 2

58. Anzai discloses “the device of claim 1 (*see claim 1*), each pixel further comprising a seventh conductive layer (**drain electrode 36**) in the second area (**Transistor Area**) for providing contact to the first semiconductor layer (**active layer 33**).”

59. Anzai discloses that **drain electrode 36** is formed by filling a contact hole formed at the location corresponding to the drain 33d. EX1003, 4:20-24. Figs. 2A and 3A show drain electrode to be in the **Transistor Area** and in contact with the drain portion 33d of **active layer 33**.



A POSITA would have also understood [drain electrode 36](#) to be a layer that provides contact to the [active layer 33](#). The sole example of the seventh conductive layer in the 121 patent is metal pattern 210B (which provides contact to the first semiconductor layer (i.e., polysilicon pattern 202B)). EX1001, 5:29-34; Fig. 2. The 121 patent teaches that metal pattern 210B is formed by depositing a layer of metal over ILD 208 and patterned to form metal pattern 210B over both areas B and C, “wherein second metal pattern 210B contacts polysilicon pattern 202B through a via hole (not numbered) in ILD 208 and gate oxide 204.” *Id.* Therefore, Anzai teaches forming its seventh conductive layer ([drain electrode 36](#)) in the same manner as the 121 patent forms its seventh conductive layer (metal pattern 210B), namely, by filling a hole with conductive material.

C. Claim 3

60. Anzai also discloses “the device of claim 1 (*see* claim 1), wherein the second dielectric layer (first and second planarization layers 17 and 19) comprises a passivation layer (first planarization layer 17) and a capping layer (second planarization layer 19).”

61. The 121 patent provides no meanings for “passivation layer” and “capping layer.” In fact, the 121 patent discloses silicon nitride (SiN) as the sole example for both layers. For the passivation layer of the second dielectric layer, the 121 patent states: “A layer of passivation silicon nitride (SiN) 212 is formed

over ILD208 and second metal patterns 210A and 210B.” EX1001, 5:34-36. For the capping layer of the second dielectric layer, the 121 patent states: “A layer of capping SiN 216 is disposed to cover passivation SiN 212 and ITO pattern 214C.” *Id.*, 5:40-42. A POSITA would understand from the 121 patent that there is no special meaning ascribed to passivation layer and capping layer other than they are two separate layers of insulation material. Moreover, given that the sole example given in the 121 patent is SiN for both layers, a POSITA would understand these two layers need not be made of different insulation materials. *Id.*

62. Anzai discloses that planarization layer 17 may be made of an organic resin for flattening the surface. EX1003, 4:20-24. While Anzai does not disclose the material for planarization layer 19, it must be made of an insulation material because in the embodiment of Fig. 3A, it is the sole layer between **electrode layer 71** and **cathode layer 65** forming the second capacitor. *Id.*, 6:3-8; Fig. 3A. Moreover, Anzai discloses that the first planarization film 17 and the second planarization film 19 for the first embodiment “function as the capacitance insulating film for this configuration.” *Id.*, 5:62-67.

63. A POSITA would have understood that when the first and planarization layers 17 and 19 are used as the insulating film, one of the layers can be understood as a passivation layer while the other layer is a capping layer. EX1003, 5:44-6:9. The first planarization film 17 is formed over the entire surface

for flattening, which will protect the semiconductor surface from the surrounding environment (for passivation). *Id.*, 4:17-24, 5:3-13. The POSITA would further understand that the second planarization film 19 is then further disposed on the first planarization film 17 (capping the passivation layer). *Id.*, 5:3-13; Figs. 2A-B, 3A-B.

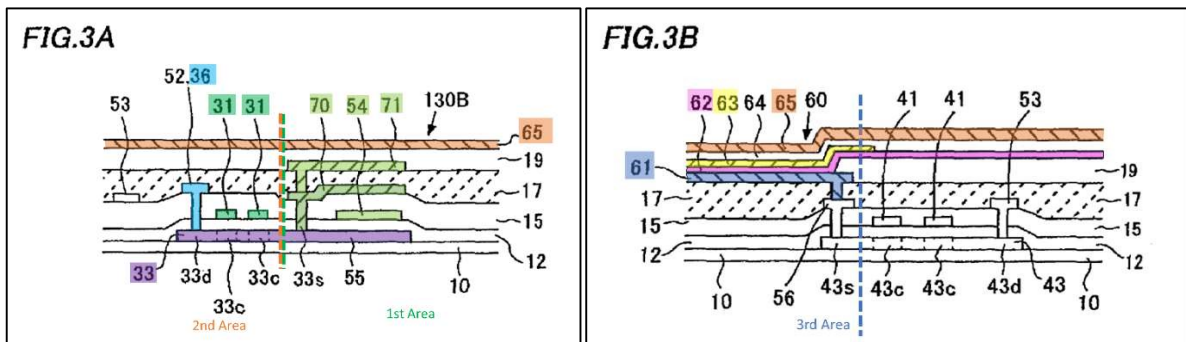
64. As such, a POSITA would understand that Anzai's planarization film 17 is a passivation layer and Anzai's planarization film 19 is a capping layer.

65. It should be noted that using a passivation layer and a capping layer between a cathode layer and a source/drain layer was well known prior to the filing date of the 121 patent. For example, Stewart discloses using a passivation and capping layer to create a smooth surface before depositing an EL electrode element. EX1006 at 849-850. Stewart is directed to method of forming a pixel with varying number of transistors for an organic light emitting diode. EX1006 at 845. In particular, Stewart discloses depositing a 300 nm of PECVD passivation oxide over the transistor gate islands to prevent shorts between the gate and data lines and using a Ni capping layer to prevent the formation of hillocks to produce a smooth ITO surface prior to the OLED material deposition. EX1006 at 848-849. Here, the POSITA would understand that the intention of the passivation oxide and Ni capping layer is for passivation and planarization. *Id.*

D. Claim 5

66. Anzai discloses “the device of claim 1 (*see* claim 1 – second embodiment (Figs. 3A, 3B)), wherein the second conductive layer (**combined electrode layer 70/71**) and the fifth conductive layer (**anode layer 61**) both comprise indium tin oxide (ITO).”

67. For the second embodiment in Figures 3A and B, Anzai explicitly discloses **anode layer 61** (i.e., the fifth conductive layer) is made of a transparent electrode such as ITO (Indium Tin Oxide). EX1003, 5:14-25; Figs. 3A-3B.



Anzai further discloses that “electrode layer 71 is in the same layer as and formed by the same process as anode layer 61.” *Id.*, 5:55-57.

68. Accordingly, a POSITA would have understood that Anzai discloses the **anode layer 61** comprises ITO, as does the **combined electrode layer 70/71**.

XI. GROUND 2: CLAIM 4 RENDERED OBVIOUS BY ANZAI IN VIEW OF YAMAZAKI

A. Claim 4

69. The combination of Anzai and Yamazaki renders obvious “the device of claim 3 (*see* claim 3 above) wherein at least one of the passivation layer

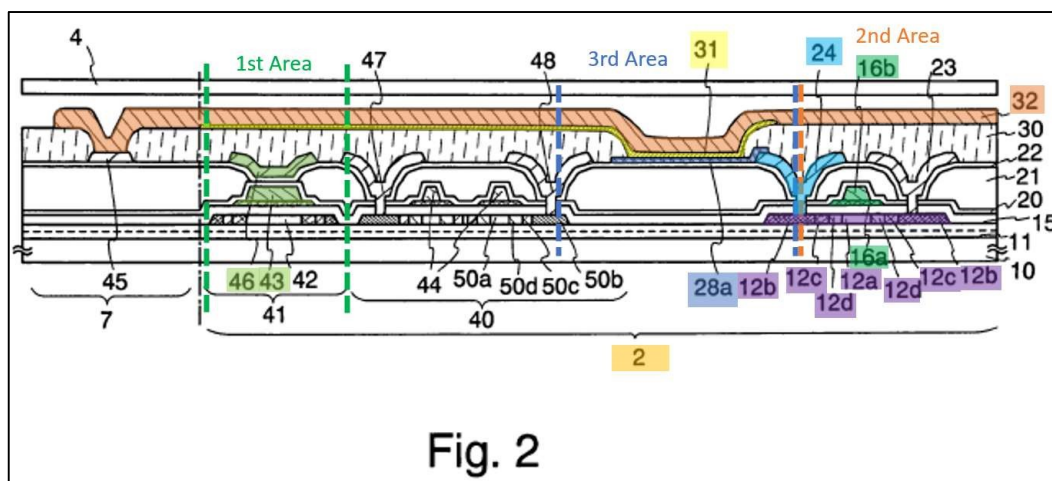
(Anzai's planarization film 17) and the capping layer (Anzai's planarization film 19) comprises silicon nitride."

70. The 121 patent provides no meanings for "passivation layer" and "capping layer." In fact, the 121 patent discloses silicon nitride (SiN) as the sole example for both layers. For the passivation layer of the second dielectric layer, the 121 patent states: "A layer of passivation silicon nitride (SiN) 212 is formed over ILD208 and second metal patterns 210A and 210B." EX1001, 5:34-36. For the capping layer of the second dielectric layer, the 121 patent states: "A layer of capping SiN 216 is disposed to cover passivation SiN 212 and ITO pattern 214C." *Id.*, 5:40-42. A POSITA would understand from the 121 patent that there is no special meaning ascribed to passivation layer and capping layer other than they are two separate layers of insulation material. Moreover, given that the sole example given in the 121 patent is SiN for both layers, a POSITA would understand these two layers need not be made of different insulation materials.

71. Anzai discloses that the second dielectric layer (first and second planarization layers 17 and 19) comprises a passivation layer (first planarization layer 17) and a capping layer (second planarization layer 19). *See* claim 3, §X.C. Anzai does not explicitly state what material(s) are used to form planarization layers 17 and 19 (other than an organic resin for layer 17). EX1003, 4:20-24. However, Anzai discloses that those layers function as the capacitance insulating

film. *Id.*, 5:62-6:9. Anzai further expressly discloses that silicon nitride (SiN) can be used in the interlayer insulating film 15 that is between second capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitance element 130, and in the gate insulating film 12 between first and second capacitance electrode layers 55 and 54. *Id.*, 4:8-10, 4:17-24 and 4:40-47.

72. Yamazaki discloses an active-matrix type light emitting device with organic compound light emitting element, that includes pixel parts 2. EX1004, Abstract, 8:56-67, Fig. 2.



Each pixel part 2 includes a first area that contains capacitors, a second area that contains a transistor and a third area that contains a light emitting element. *Id.*, 9:47-12:20, Fig. 2. It should be noted that Yamazaki refers to “a capacity 41”, and “a holding capacity is formed using an electrode 46 and an electrode 43,” and “a holding capacity is also formed using the electrode 43 and a semiconductor film 42.” EX1004, 9:65-10:15. A POSITA would have understood that “capacity”

refers to a “capacitor” given the structure at issue (two electrodes separated by insulation which is well known to form a capacitor).

73. The first area (Capacitor Area) includes a first capacitor formed between **electrode 43** and **electrode 46** with interlay insulating films 22 and 20 disposed in between, and a second capacitor formed **electrode 46** and **2nd electrode 32** (e.g., cathode of the EL device) with an insulating material 30 and **EL layer 31** disposed in between. EX1004, 9:65-12:20, Fig. 2. The second area (**TFT Area**) includes a transistor (e.g., current-controlling TFT) formed by **gate electrodes 16a/16b** disposed on top of **regions 12a-12d** on top of substrate 10. *Id.*, 9:47-64, Fig. 2. The third area includes a light emitting element formed by a **2nd electrode 32** disposed above an **EL layer 31** which is disposed above **1st electrode 28a** (e.g., anode of the EL device). *Id.*, 11:22-12:20, Fig. 2.

74. Insulation layer 30 is disposed between **cathode electrode layer 32** and the electrodes 46, 47, 48, 24, 23 underneath (similar to Anzai’s layers 17, 19 disposed between cathode 65 and electrodes 53, 52, 70). EX1004, Fig. 2. The top surface of insulation layer 30 is flattened relative to the topology underneath that includes electrodes 46, 47, 48, 24, 23 and insulation film 21 (similar to Anzai’s layers 17, 19). *Id.* Yamazaki teaches that silicon nitride is a suitable material for insulation layer 30. *Id.*, 11:45-50. Yamazaki teaches that the flat top surface of

insulation layer 30 can be achieved by CMP (chemical mechanical polish), which can be performed after the formation of insulating material 30. *Id.*, 20:17-24.

75. It should be noted that using a silicon nitride for an insulation and/or planarization layer was well known in the art prior to the filing date of the 121 patent. For example, Kim (EX1007), Fish (EX1008), and Choi (EX1009) all teach the use of a silicon nitride as a suitable material for an insulation and/or planarization layer. First, Kim¹ discloses the use of four passivation layers 114, 118, 124, and 129 that are preferably made of an inorganic insulating material such as silicon dioxide SiO₂ or silicon nitride SiN. EX1007, [0053]. Second, Fish² discloses the use of silicon nitride as an insulating and/or planarization layer 116 that is sandwiched between the cathode 114 and the pixel electrode 110. EX1008, [0095]. Lastly, Choi (EX1009) discloses the use of a silicon nitride layer that is deposited to form passivation layer 130 which insulates the data line it is deposited below. EX1009, [0060]. Thus, a POSITA would understand that silicon nitride is a suitable material for use as an insulating layer in devices such as that disclosed in Anzai.

¹ Kim is directed to an organic electroluminescent device that uses various passivation layers as insulation materials between various elements within each pixel design. EX1007 at Abstract, ¶¶ [0051-54].

² Fish is directed to the pixel design for active-matrix display devices that includes an insulating layer between the pixel electrode and the cathode of the EL element. EX1008 at Abstract, ¶ [0095].

76. It would have been obvious to a POSITA to combine the teachings of Anzai and Yamazaki to use silicon nitride as the material for at least one of the planarization films 17 or 19 of Anzai.

77. Anzai and Yamazaki are analogous prior art to the 121 patent, as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third area containing a light emitting device having an organic layer between two electrode layers.

78. A POSITA would have understood the issue involved, namely what material(s) can be used to form the first and second planarization layers 17 and 19 for the second capacitor of Anzai. To address this issue, a POSITA would have investigated what insulator material(s) would be appropriate. A POSITA would have been motivated to use silicon nitride to form at least one of the first and second planarization layers 17 and 19 of Anzai because (1) Yamazaki teaches using silicon nitride as the insulating layer 30 under its cathode layer (EX1004, 11:45-50), (2) Yamazaki teaches using silicon nitride for use as a planarization film for flattening the surface (compare upper and lower surfaces of insulation layer 30 (*Id.*, 11:22-12:20), and (3) Anzai teaches using silicon nitride in the interlayer insulating film 15 between second and third capacitance electrode layers 54 and 70, and in the gate insulating film 12 between first and second capacitance

electrode layers 55 and 54 (EX1003, Fig. 2A, 4:8-10 and 17-24 and EX1004, 11:22-12:52, 20:17-39, Fig. 2). Additionally, Anzai discloses that both films 17 and 19 are used as the capacitance insulating film. EX1003, 5:65-67. A POSITA would have known that organic materials usually have lower dielectric constants than inorganic materials such as SiN, and a higher dielectric constant is desirable for the insulator in a capacitor since that leads to a higher capacitance per unit area. That then allows a reduced area storage capacitance element, one of the objectives of Anzai. EX1003, Abstract (“The forming area of the storage capacitance element for holding the video signal supplied to the gate of the driving transistor can be thus reduced, improving display quality as well as extending life span of the organic El element.”). Therefore, a POSITA would have been motivated to consider using an inorganic material such as SiN for the films 17 and 19.

79. The modification to Anzai would simply involve selecting an appropriate insulation material for the first and second planarization layers 17 and 19. A POSITA would have had a reasonable expectation of success in combining Anzai and Yamazaki, as both references disclose forming capacitors for use with organic electroluminescent devices, and both references teach insulator films for such capacitors that comprise silicon nitride. Moreover, because combining the teachings of Anzai and Yamazaki would involve known methods, it would have yielded predictable results.

**XII. GROUND 3: CLAIMS 1-7 RENDERED OBVIOUS BY YAMAZAKI
IN VIEW OF ANZAI**

A. Claim 1

1. [1pre]

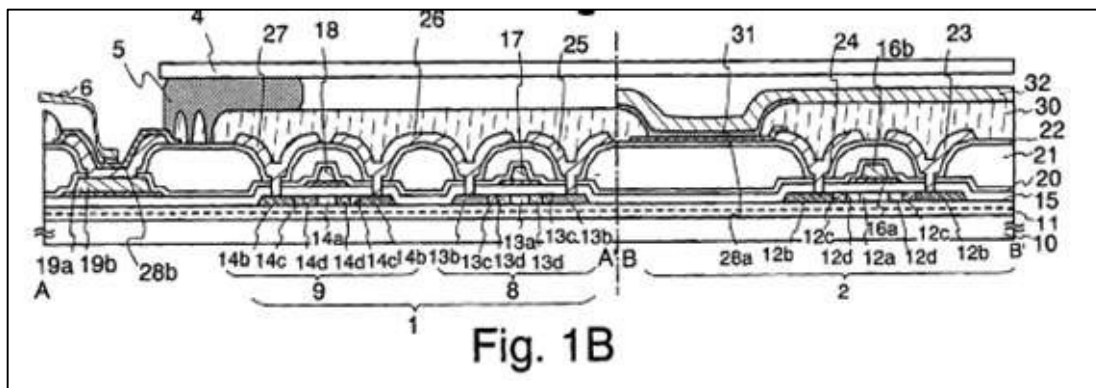
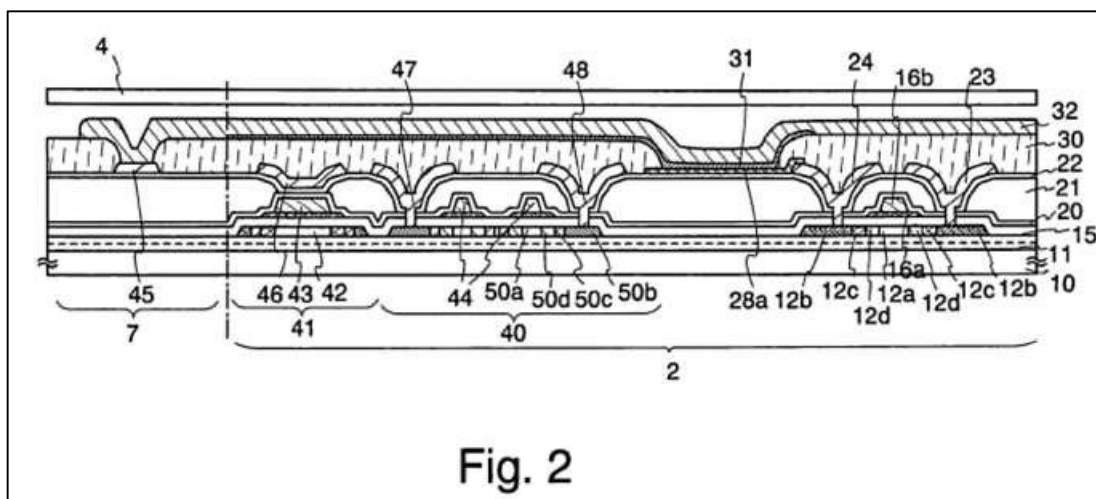
80. To the extent that the preamble is limiting, the combination of Yamazaki and Anzai renders obvious “[a]n electroluminescence (EL) device (Yamazaki’s light emitting device).”

81. Yamazaki is directed to a light emitting device. EX1004, Abstract. In particular, Yamazaki is directed to a light emitting display device (“EL element”) in which a light emitting element arranged in a matrix configuration has a layer that contains an organic compound between a pair of electrodes. *Id.*, 1:7-24, 2:37-64, 20:3-21:7.

2. [1a]

82. The combination of Yamazaki and Anzai renders obvious “a substrate (Yamazaki’s substrate 10).”

83. Yamazaki disclose a substrate 10 on which driving circuits and the pixel part are formed. EX1004, 9:14-18; Figs. 1B, 2. Figure 1B and Figure 2 contain the same structure components which are represented by the same reference numbers. *Id.*, 10:15-17.

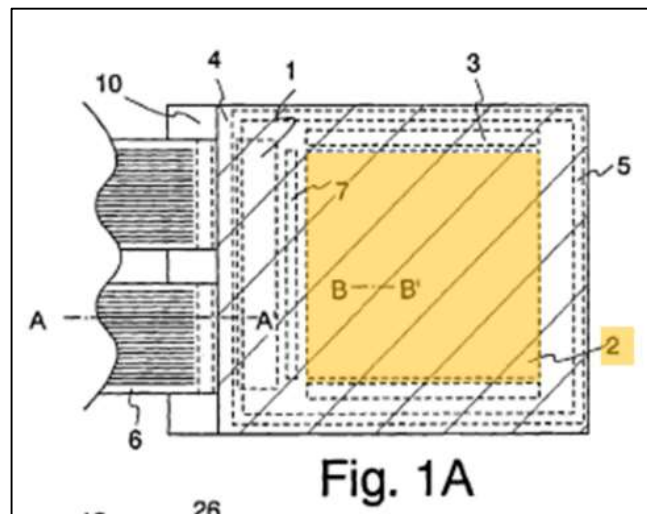
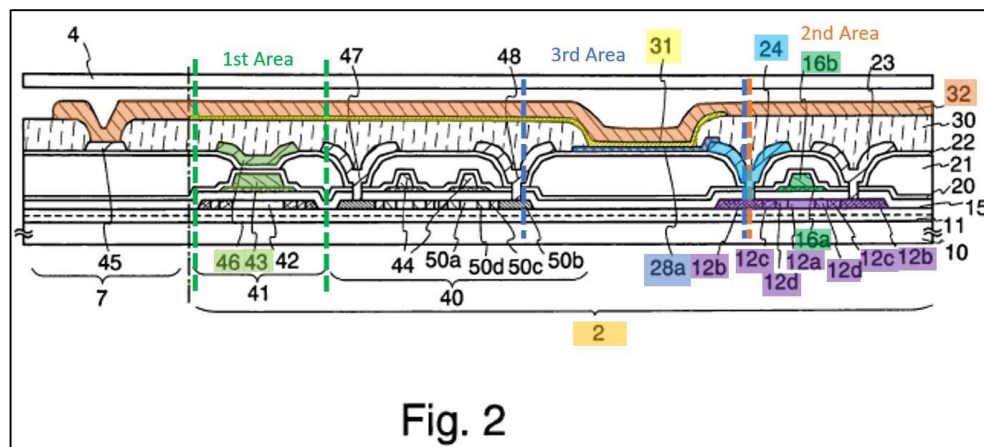


3. [1b]

84. The combination of Yamazaki and Anzai renders obvious “a plurality of OLED pixels (Yamazaki’s plurality of pixels), formed on the substrate (Yamazaki’s substrate 10), each pixel being in a respective pixel area (Yamazaki’s pixel part 2), each pixel area including at least a first area (Yamazaki’s Capacitor Area), a second area (Yamazaki’s TFT Area), and a third area (Yamazaki’s EL element), wherein each pixel includes (see [1c]-[1e]).”

85. Yamazaki discloses that pixel part 2 comprises a plurality of pixels within an active-matrix type light emitting device. EX1004, 2:37-64, 8:63-9:4,

9:47-64, Figs. 1A, 2. Each pixel part 2 comprises a capacity 41 (i.e., capacitors) in the first area (Capacitor Area) (see 1[c]), a current-controlling TFT in the second area (TFT Area) (see 1[d]) and an EL element in the third area (EL Area) (see 1[e]). *Id.*, 9:47-10:55, 11:22-12:13, 20:3-21:7; Fig. 2.



4. [1c]

86. The combination of Yamazaki and Anzai renders obvious “at least a first capacitor (Yamazaki’s capacity 41) and a second capacitor (Yamazaki’s capacity 41) in the first area, the first capacitor including a first conductive layer

(Yamazaki's **electrode 43**) formed over a first gate oxide layer (Yamazaki's gate insulating film 15), a first dielectric layer (Yamazaki's interlayer insulation films 22 and 20) over the first conductive layer (Yamazaki's **electrode 43**), and a second conductive layer (Yamazaki's **electrode 46**) over the first dielectric layer (Yamazaki's interlayer insulation films 22 and 20), and the second capacitor including the second conductive layer (Yamazaki's **electrode 46**), a second dielectric layer (Yamazaki's insulating material 30 as modified by Anzai) over the second conductive layer, and a third conductive layer (Yamazaki's **2nd electrode (cathode) 32, referred to herein as "cathode 32"**) over the second dielectric layer."

87. As seen in Figure 2 below, Yamazaki discloses a first embodiment having a capacity 41 within the first area, the **Capacitor Area** (e.g., the area between the two green dotted lines) that includes a capacitor composed of the **electrode 43** and **electrode 46** where interlayer insulation films 22 and 20 act as the dielectric material that is sandwiched in between. EX1004, 9:65-10:55, Fig. 2. **Electrode 43** is formed over the gate insulating film 15, which is made from a silicon oxide film that is formed on top of the substrate 10. *Id.*

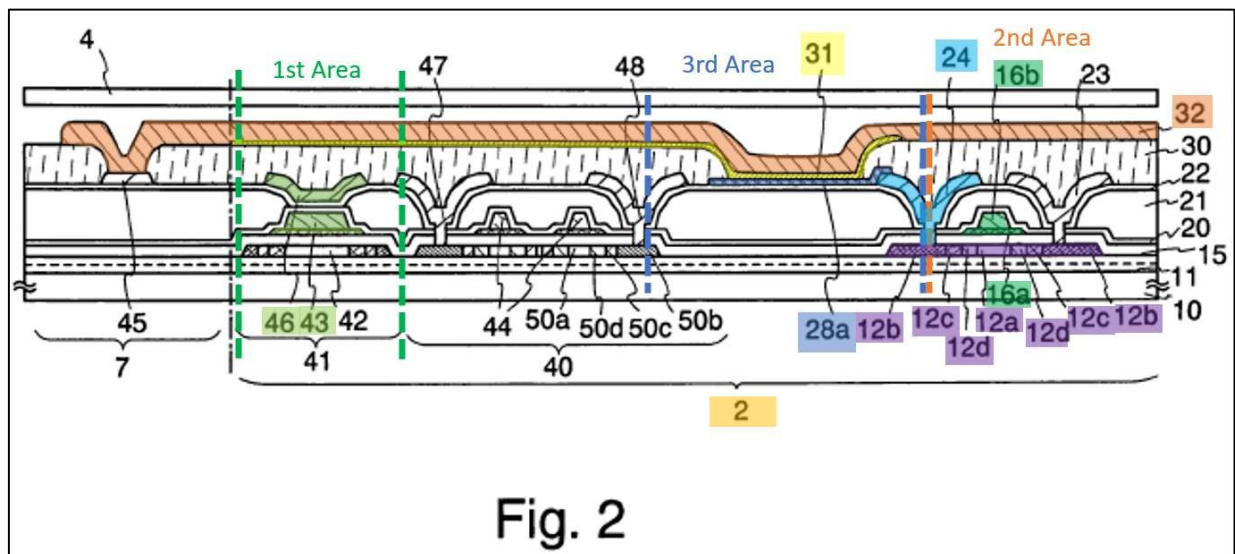


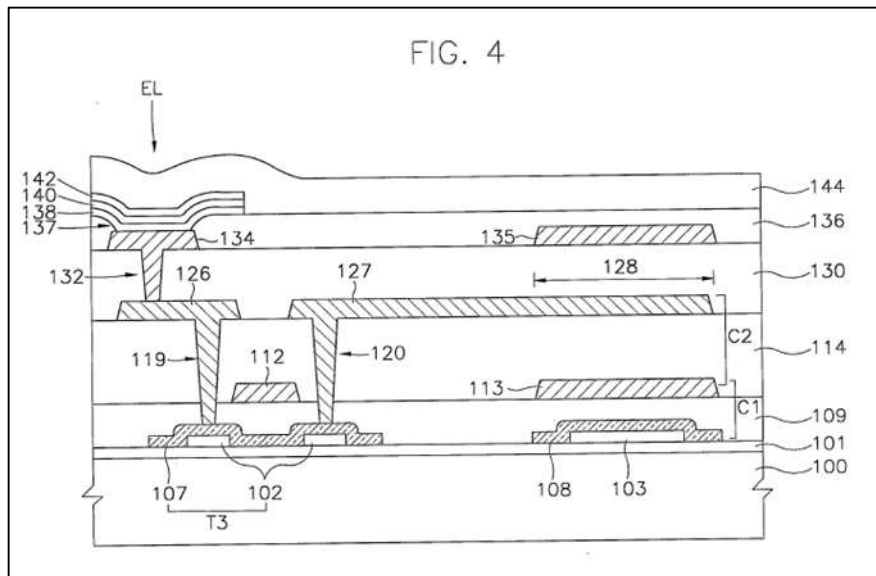
Fig. 2

88. The fact that Yamazaki discloses a holding capacity (i.e., capacitor) formed between **electrode 43** and the semiconductor layer 42 is not relevant to claim 1. A POSITA would understand that **electrode 43** and **electrode 46** with insulating film 22 and 20 sandwiched in between form a capacitor on which claim 1 reads, and **electrode 43** and semiconductor layer 42 with insulating film 15 sandwiched in between form another capacitor (which is not needed to meet the limitations of claim 1). Claim 1 is an open ended “comprising” claim to “at least” a first and second capacitor, and the capacitors themselves are recited as “including” the recited layers. EX1001, claim 1. Thus, a device with the claimed capacitors including the claimed layers practices the claims even if the device includes additional capacitors and the capacitor includes additional layers.

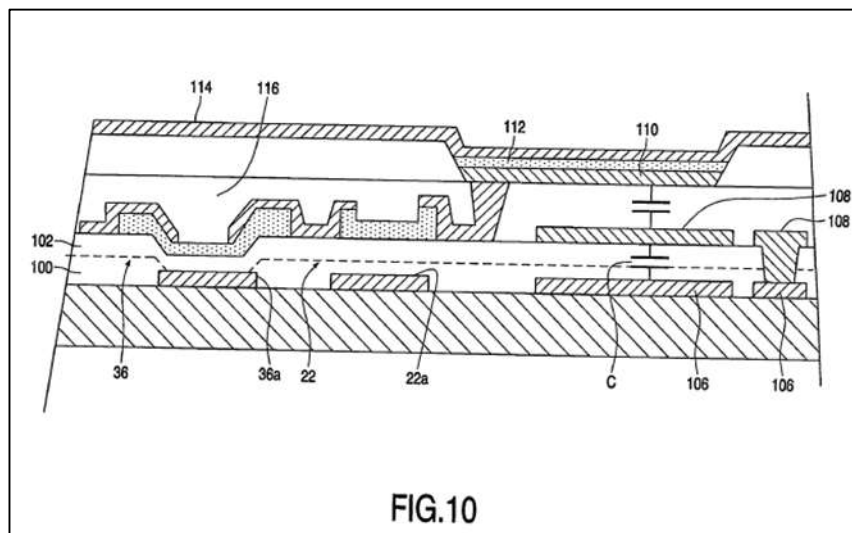
89. The second capacitor is formed between **electrode 46** and **cathode 32** with insulating material 30 acting as the dielectric materials sandwiched in

between the electrodes when the thickness of insulating material 30 is selected according to the teachings of Anzai. EX1004, 9:65-10:55, 11:22-12:13, Fig. 2. Although Yamazaki does not disclose a holding capacity (i.e., capacitor) formed between **electrode 46** and **cathode 32**, it would have been obvious to combine Yamazaki with the teachings of Anzai for the formation of a storage capacitor using the **cathode 32** of the EL device, which extends from the third area into the first area, as an electrode for a storage capacitor with **electrode 46**.

90. It should be noted that it was well known prior to the filing date of the 121 patent that a two capacitor design could be used within a pixel area for an OLED device. For example, Choi (EX1009) discloses the use of two vertically stacked capacitors (e.g., C1 and C2) that share an electrode layer within a pixel area for an active matrix type organic electroluminescent display device. EX1009 at Abstract, pp. 9-10; Fig. 4. As seen in Figure 4 below, the first capacitor C1 is composed a first electrode 108, a gate insulating layer 109, and a second electrode 113 while the second capacitor C2 is composed of the second electrode 113, which is shared with the first capacitor C1, insulating interlayer 114 and the third electrode 127. EX1009 at p. 10.

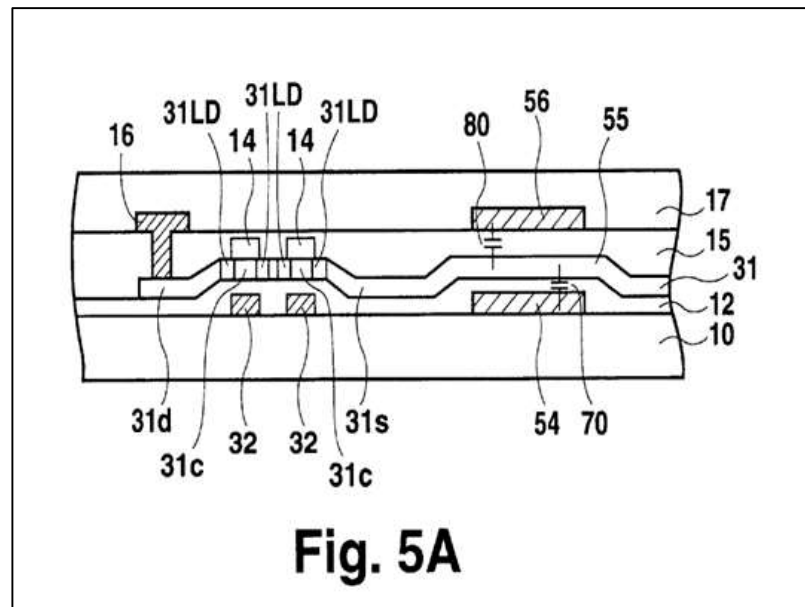


91. Fish (EX1008) also discloses the use of two storage capacitors within a pixel area where the two capacitors are stacked vertically and share a common electrode. For instance, as seen in Figure 10 below, where the first capacitor is composed of the bottom metal layer 106 disposed below the first gate dielectric layer 100 which is disposed below the second gate dielectric layer 102 which is disposed below the top metal layer 108 (i.e., two dielectric layers are disposed between the electrodes of the first capacitor). EX1008, [0094]-[0096]; Fig. 10. The second capacitor (not labeled but marked) is composed of the top metal layer 108, which is shared with the first capacitor, disposed below insulating/planarization layer 116, which is disposed below the pixel electrode 110. *Id.* Fish expressly discloses that “[o]ne or more of the capacitors in the pixel circuit may also use the thin gate insulator layer as a dielectric” which can be used to reduce the area needed to achieve the same capacitance. *Id.*

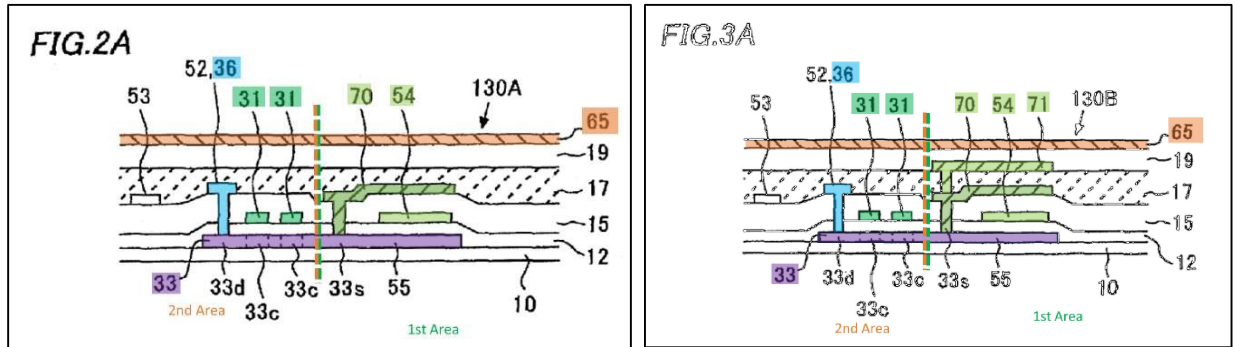


92. Lastly, Yasuda (EX1010) also discloses, in Figure 5A below, the use of a capacitor stack with a first storage capacitor 70 that is formed from a second capacitor electrode 55 stacked above a first capacitor electrode 54 with a gate insulating film 12, a p-Si film, sandwiched in between, and a second storage capacitor 80 formed between the second capacitor electrode 55 and the third capacitor electrode 56 with another gate insulating film 15 sandwiched between. EX1010 at Abstract; 5:26-7:3; Fig. 5A. Yasuda also discloses the use of first and second storage capacitors 70 and 80 to increase the voltage applied to the gate electrode 42 of the EL driving TFT 40 by sharing an electrode (i.e., electrode 55) between the two storage capacitors to increase the storing capacity without enlarging the area of the storage capacitor in the planar direction. *Id.*, 5:26-6:7; 7:64-8:33. Thus, a POSITA would understand that it was well known before

the filing of the 121 patent that two capacitors can be used within a pixel design where the two capacitors share a common electrode.



93. Anzai discloses “at least a first capacitor (layers 54, 15, 70, 71) and a second capacitor (layers 70, 71, 17, 19, 65) in the first area, the first capacitor including a first conductive layer (**electrode layer 54**) formed over a first gate oxide layer (gate insulating film 12), a first dielectric layer (interlayer insulating film 15) over the first conductive layer (**electrode layer 54**), and a second conductive layer (**electrode layer 70 or 70/71**) over the first dielectric layer (interlayer insulating film 15), and the second capacitor including the second conductive layer (**electrode layer 70 or 70/71**), a second dielectric layer (first 17 and second 19 planarization films) over the second conductive layer, and a third conductive layer (**cathode layer 65**) over the second dielectric layer.” See §X.A.4.



94. Specifically, Anzai discloses a first capacitor between layers 55 and 54, a second capacitor between electrode layers 54 and 70 or 70/71, and a third capacitor between electrode layers 70 or 70/71, and cathode 65 (which extends from the third area into the first area.) EX1003, 4:48-51 (“It is also possible to acquire the larger capacitance by extending the cathode layer 65 over the third capacitance electrode layer 70 through the first planarization film 17 and a second planarization film 19.”)

95. It would have been obvious to a POSITA to combine the teachings of Anzai and Yamazaki to modify the thickness of insulating material 30 of Yamazaki to form the second capacitor of desired capacitance between electrode 46 and cathode 32 (which extends from the third area into the first area) with insulating material 30 sandwiched in between as the capacitor dielectric material.

96. Anzai and Yamazaki are analogous prior art to the 121 patent, as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third

area containing a light emitting device having an organic layer between two electrode layers.

97. A POSITA would have understood the issue involved, namely that a capacitor can be formed between Yamazaki's **electrode 46** and **cathode 32** such that the insulating material 30 and EL layer 31 act as the dielectric material in between the two capacitor electrodes. A POSITA would have been motivated to apply the teaching of Anzai where a storage capacitor can be established between the **electrode layer 70** and the **cathode layer 65** where the first and second planarization layers 17 and 19 are the dielectric materials in between (*see* §X.A.4). A POSITA would have had a reasonable expectation of success in combining Yamazaki with the teachings of Anzai, as both references disclose forming two storage capacitors for use within a light emitting or electroluminescent device. Moreover, the combination of Yamazaki with Anzai would involve known methods to yield predictable results.

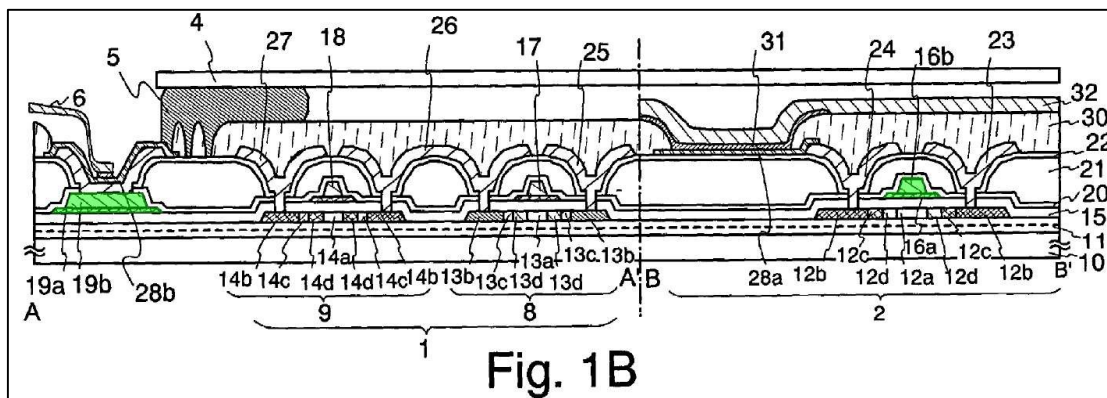
5. [1d]

98. The combination of Yamazaki and Anzai renders obvious “a transistor (Yamazaki's current-controlling TFT) in the second area (Yamazaki's **TFT Area**), the transistor including a first semiconductor layer (Yamazaki's **regions 12a-12d**) formed on the substrate (Yamazaki's substrate 10), the first gate oxide layer (Yamazaki's gate insulating film 15) over the first semiconductor layer

(Yamazaki's regions 12a-12d) and a fourth conductive layer (Yamazaki's gate electrode 16a/16b) over the first gate oxide layer (Yamazaki's gate insulating film 15), wherein the fourth conductive layer (Yamazaki's gate electrode 16a/16b) is formed of the same conductive film as the first conductive layer (Yamazaki's electrode 43), and wherein both the first conductive layer (Yamazaki's electrode 43) and the fourth conductive layer (Yamazaki's gate electrode 16a/16b) are directly formed on the gate oxide layer (Yamazaki's gate insulating film 15)."

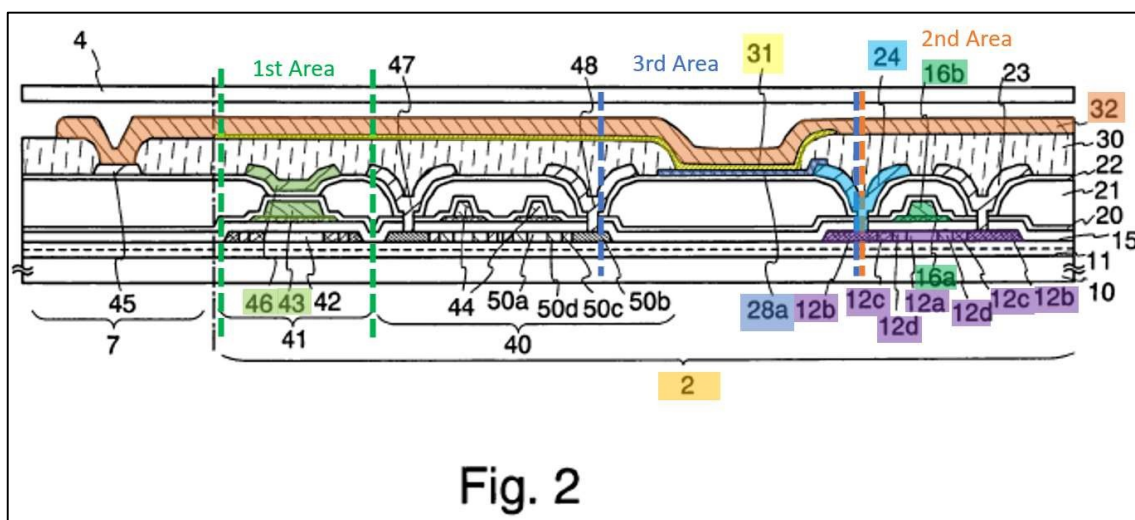
99. As seen in Figure 2 below, Yamazaki discloses in the second area, the TFT Area (e.g., the area to the right of the orange dotted lines), a current-controlling TFT (not numbered) arranged on pixel part 2 which is formed on substrate 10 below gate insulating film 15. EX1004, 9:47-64, Fig. 2. The current-controlling TFT comprises an n-channel TFT having a channel forming region 12a, source and drain (high impurity) regions 12b, and low-level impurity regions 12c and 12d over which the gate electrodes 16a/16b are deposited. *Id.* Regions 12a-12d are formed on substrate 10. *Id.*, Fig. 2. A POSITA would have understood that regions 12a-12d of the current controlling TFT are a semiconductor layer. Gate insulating film 15 is formed over the regions 12a-12d, and is constructed of a silicon oxide film. EX1004, Fig. 2, 10:31-33. Gate electrode 16a/16b and electrode 43 are directly formed on gate insulating film 15. *Id.*, Fig. 2.

102. A POSITA would have understood the issue involved, namely how to form the device of Yamazaki with an efficient manufacturing process flow. To address this issue, a POSITA would have investigated what components could be formed using the same process step (i.e., layer deposition and patterning), which results in the components being formed of the same film, is common practice when forming semiconductor products. Motivation to do so comes from Yamazaki, which discloses forming multiple components “in the same step.” EX1004, 12:21-28 (“In addition, on the terminal portion shown in FIG. 1B, a terminal electrode formed as a laminate of electrodes 19a, 19b formed by the same step as that of the gate electrode.” Fig. 1b shows that terminal electrode 19a/19b has the same configuration as gate electrode 16a/16b (thin lower layer that is formed directly on insulation layer 15, and a narrower but thicker trapezoidal upper layer formed directly on the lower layer).



A POSITA would understand that Yamazaki is disclosing that terminal electrode 19a/19b and gate electrode 16a/16b are formed of the same conductive film.

Moreover, **terminal electrode 19a/19b** in Fig. 1B has the same configuration as **electrode 43** in Fig. 2 (i.e., thin lower layer that is formed directly on insulation layer 15, and a narrower but thicker trapezoidal upper layer formed directly on the lower layer).



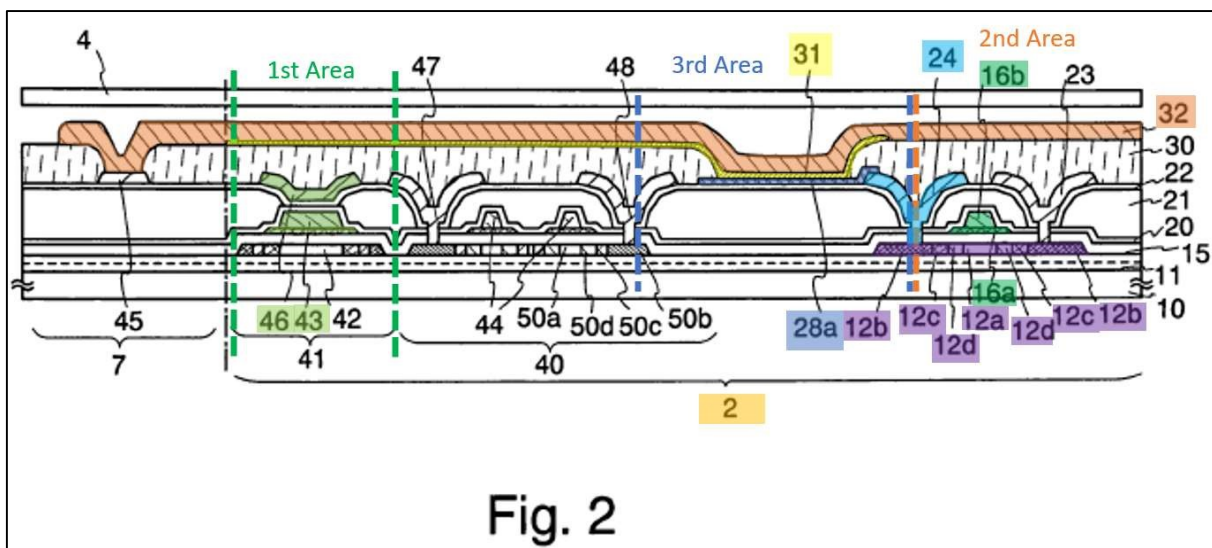
A POSITA would have therefore found it obvious to form **electrode 16** and **electrode 43** using the same step, of the same conductive film, to provide for a more efficient manufacturing process flow.

6. [1e]

103. The combination of Yamazaki and Anzai renders obvious “a light emitting device (Yamazaki’s EL element) in the third area (Yamazaki’s **EL Area**), the light emitting device including a fifth conductive layer (Yamazaki’s **1st electrode (anode) 28a, referred to herein as “anode 28”**), a first organic layer (Yamazaki’s **EL layer 31**) over the fifth conductive layer (Yamazaki’s **anode 28**), and a sixth conductive layer (Yamazaki’s **cathode 32**) over the first organic layer

(Yamazaki's EL layer 31), wherein the sixth conductive layer (Yamazaki's cathode 32 in the third area) is formed of the same conductive film as the third conductive layer (Yamazaki's cathode 32 in the first area).”

104. As seen in Figure 2 below, Yamazaki discloses, in the EL Area (see [1a]) (e.g., between the blue dashed lines), a 1st electrode 28a which functions as an anode of the EL element, EL layer 31 formed on anode 28, and 2nd electrode 32 which functions as the cathode formed on EL layer 31. EX1004, 11:22-12:20, 20:3-21:7, Fig. 2. Yamazaki goes on to disclose that since the EL element emits light through the anode 28a, it may be a transparent conductive film such as ITO. *Id.* The light emitting layer EL layer 31 contains an organic compound. *Id.* Lastly, the cathode 32 is deposited on top of the light emitting layer within EL layer 31, which functions as wiring common to all pixels. *Id.*



105. Yamazaki also teaches that **EL layer 31** “is formed by freely combining a light emitting layer, electric charge transporting layers, and an electric charge injection layer where known polymeric organic materials can be employed. EX1004, 11:45-50, 20:3-21:7, Fig. 2. The purpose of **EL layer 31** comprising a plurality of layers is for light emission and for moving carriers to cause light emission where it can be made from a monomeric organic EL material, a polymeric organic material, or other known materials. *Id.*

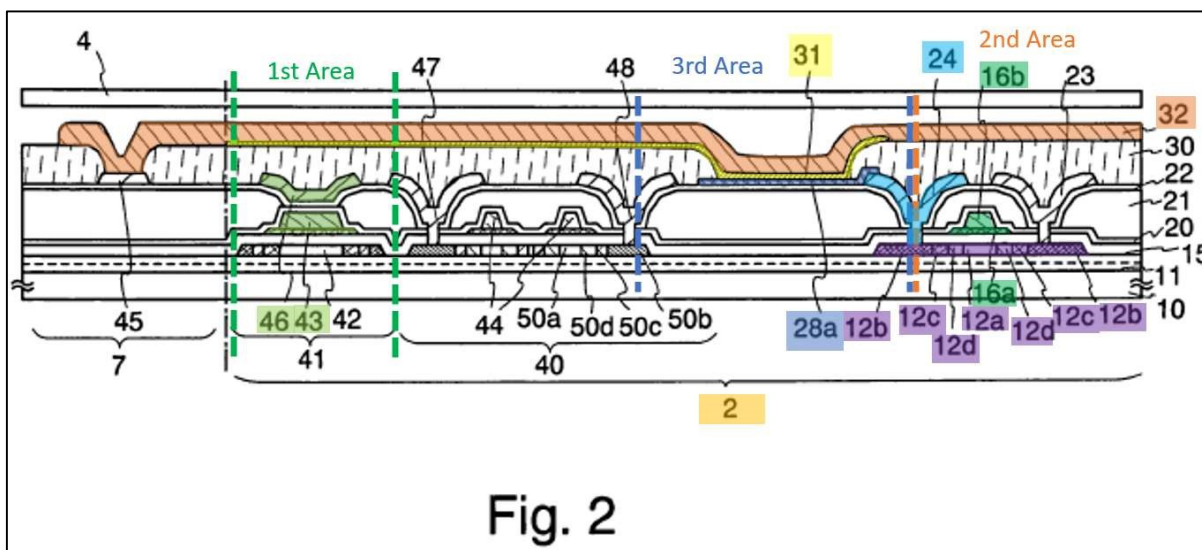
106. A POSITA would have understood that the sixth conductive layer (i.e., **cathode 32** in the third area) of the light emitting device of Yamazaki is formed from the same conductive film as the third conductive layer of the second capacitor of Yamazaki (i.e., **cathode 32** in the first area) because as shown above in [1c], the same film (i.e., **cathode 32**) that serves as the third conductive layer in the first area also serves as the sixth conductive layer in the third area (*see above*). Thus, the third and sixth conductive layers are literally the same layer in Yamazaki.

B. Claim 2

107. The combination of Yamazaki and Anzai renders obvious “the device of claim 1 (*see claim 1*), each pixel further comprising a seventh conductive layer (Yamazaki’s **connecting electrode 24**) in the second area (Yamazaki’s **TFT Area**)

for providing contact to the first semiconductor layer (Yamazaki's regions 12a-12d)."

108. Yamazaki discloses, in the TFT Area (e.g., second area) connecting electrode 24 for making a connection between the 1st electrode 28a (e.g., anode 28a) to the source region 12b. EX1004, 9:47-64, Fig. 2.

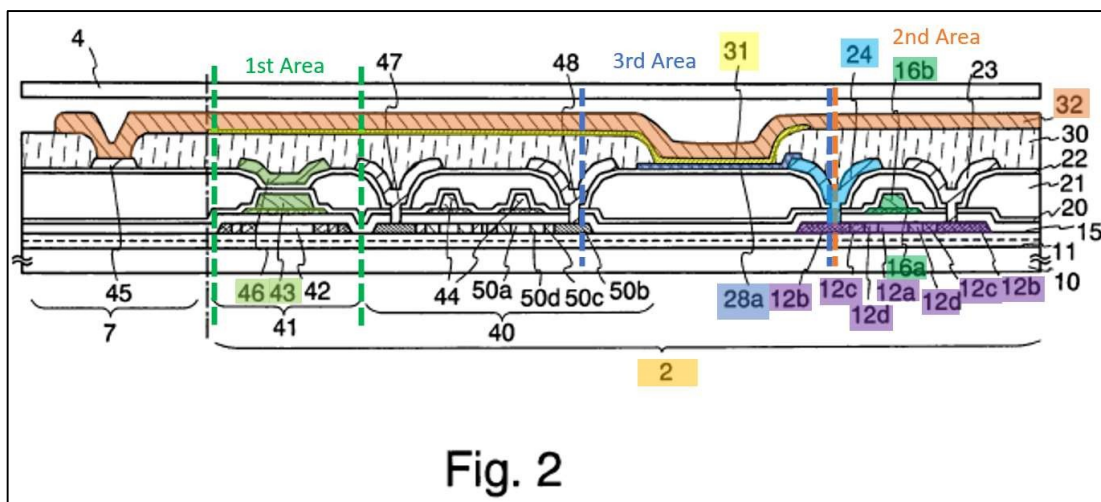


109. A POSITA would have understood that connecting electrode 24 to be a layer that provides contact to the regions 12a-12d, including source region 12b, which is a semiconductor layer.

C. Claim 3

110. The combination of Yamazaki and Anzai "the device of claim 1 (*see* claim 1), wherein the second dielectric layer (insulating material 30) comprises a passivation layer (Yamazaki insulating material 30) and a capping layer (Anzai's planarization layer 19)."

111. The 121 patent provides no meanings for “passivation layer” and “capping layer.” In fact, the 121 patent discloses silicon nitride (SiN) as the sole example for both layers. For the passivation layer of the second dielectric layer, the 121 patent states: “A layer of passivation silicon nitride (SiN) 212 is formed over ILD208 and second metal patterns 210A and 210B.” EX1001, 5:34-36. For the capping layer of the second dielectric layer, the 121 patent states: “A layer of capping SiN 216 is disposed to cover passivation SiN 212 and ITO pattern 214C.” *Id.*, 5:40-42. A POSITA would understand from the 121 patent that there is no special meaning ascribed to passivation layer and capping layer other than they are two separate layers of insulation material. Moreover, given that the sole example given in the 121 patent is SiN for both layers, a POSITA would understand these two layers need not be made of different insulation materials.



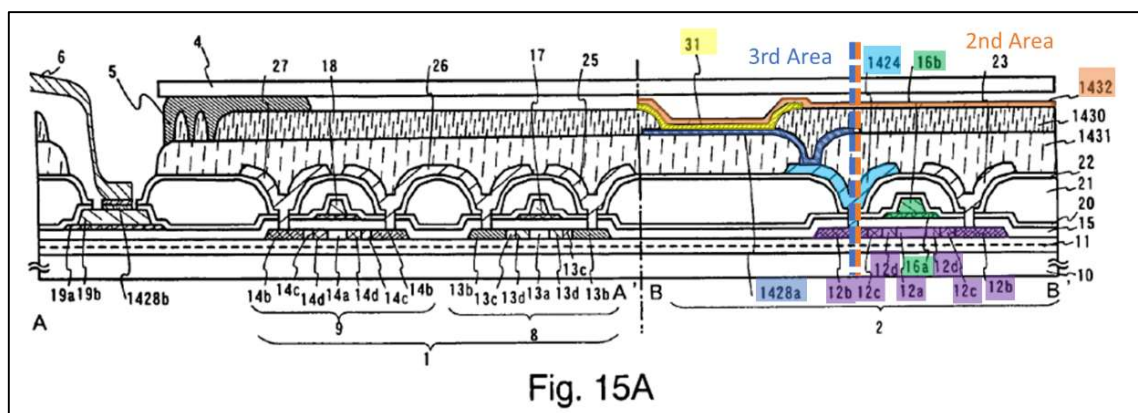
112. Yamazaki discloses “insulating material 30 which may be a photosensitive or non-photosensitive organic material (such as polyimide, acrylate,

polyamide, polyimide amide, resist, or benzocyclobutene) or an inorganic material (such as silicon dioxide, silicon nitride, or silicon oxynitride). EX1004, 11:22-65, Fig. 2. Insulating materials 30, also called a bank, is formed on both ends of the 1st electrode 28a (e.g., anode), which may be formed by an organic resin film or an insulating film including silicon. *Id.*

113. Insulation layer 30 is disposed between cathode 32 and the electrodes 46, 47, 48, 24, 23 (similar to Anzai's layers 17 and 19 disposed between cathode 65 and electrodes 53, 52, 70). EX1004, Fig. 2. The top surface of insulation layer 30 is flattened relative to the topology underneath that includes electrodes 46, 47, 48, 24, 23 and insulation film 21 (similar to Anzai's layers 17, 19). *Id.*

114. Yamazaki, in Figure 15A below, also discloses, in another embodiment, the formation of an interlayer insulation film 1431 that is formed below insulation film 1430 (e.g., which corresponds to insulation layer 30). EX1004, 35:49-36:54; Fig. 15A. Figure 15A shows the same structural components as seen in Figures 1A and 1B, which also shows the same configuration of a light emitting device as shown in Figure 2. *Id.*, 35:49-58, 8:3-9, 8:56-62; Figs. 1A-1B, 2. Here, an interlayer insulating film 1431, also comprising of an organic material (e.g., a photosensitive or non-photosensitive) or an inorganic material (e.g., silicon dioxide, silicon nitride, or silicon oxynitride) is deposited below the insulating material 1430 (i.e., the bank) as previously described. *Id.*,

35:65-36:54; Fig. 15A. Yamazaki explicitly indicates that a silicon nitride film may be used to form the interlayer insulation film 1431. *Id.*, 36:6-15.



115. A POSITA would understand that this Yamazaki embodiment teaches the use of an additional insulation layer (i.e., interlayer insulation layer 1431) to be formed under insulating material 1430 (e.g., corresponding to insulating material 30).

116. Anzai also discloses “wherein the second dielectric layer (first and second planarization layers 17 and 19) comprises a passivation layer (first planarization layer 17) and a capping layer (second planarization layer 19).” See §X.C.

117. Anzai does not explicitly state what material(s) are used to form planarization layers 17 and 19 (other than an organic resin for layer 17). EX1003, 4:20-24. However, Anzai discloses that those layers function as the capacitance insulating film. *Id.*, 5:62-6:9. Anzai further expressly discloses that silicon nitride (SiN) can be used in the interlayer insulating film 15 that is between second

capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitance element 130, and in the gate insulating film 12 between first and second capacitance electrode layers 55 and 54. *Id.*, 4:8-10, 17-24 and 40-47.

118. It would have been obvious to a POSITA to combine the teachings of Yamazaki and Anzai to add planarization layer 19 from Anzai to be formed on top of insulating material 30, since Yamazaki already teaches using an additional insulation layer (e.g., interlayer insulation film 1431) in a separate embodiment.

119. Anzai and Yamazaki are analogous prior art to the 121 patent, as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third area containing a light emitting device having an organic layer between two electrode layers.

120. A POSITA would have understood the issue involved, adding another insulating layer to improve the planarization of the pixel area of Yamazaki. To address this issue, a POSITA would have been motivated to add planarization layer 19 from Anzai above insulating material 30 of Yamazaki because both insulating layer 30 and planarization layer 19 serve the same purpose of flattening the surface of the pixel area. EX1003, Fig. 2A, 4:8-10 and 4:17-24; EX1004, 11:22-12:52, 20:17-39, Fig. 2.

121. The modification to Yamazaki would simply involve deposition another planarization layer on top of an already existing planarization layer (e.g., insulating material 30), which would further improve the flattening purpose of the insulating material 30. A POSITA would have had reasonable expectation of success for combining Yamazaki and Anzai, as both references disclose forming capacitors for use with organic electroluminescent devices, and both references teach insulator films for such capacitors that comprise silicon nitride. Moreover, combining the teachings of Yamazaki and Anzai would involve known methods that would have yielded predictable results.

D. Claim 4

122. The combination of Yamazaki and Anzai renders obvious “the device of claim 3 (*see* claim 3 above) wherein at least one of the passivation layer (insulating material 30 of Yamazaki) and the capping layer (planarization layer 19 of Anzai) comprises silicon nitride.”

123. It would have been obvious to a POSITA to combine the teachings of Yamazaki and Anzai to add planarization layer 19 from Anzai to be formed on top of insulating material 30, as capping layer and passivation layer respectively. *See* §XII.C.

124. Yamazaki teaches that silicon nitride is a suitable material for insulation layer 30. EX1004, 11:45-50 (“The insulating material 30 may be a

photosensitive or non-photosensitive organic material (such as polyimide, acrylate, polyamide, polyimide amide, resist, or benzocyclobutene), an inorganic material (such as silicon oxide, silicon nitride, or silicon oxynitride) with a CVD method, a sputtering method, or coating method, or a laminate thereof.” Therefore, Yamazaki discloses that at least the passivation layer (insulating material 30 of Yamazaki) comprises silicon nitride.

E. Claim 5

125. The combination of Yamazaki and Anzai renders obvious “the device of claim 1 (*see* claim 1), wherein the second conductive layer (electrode 46 of Yamazaki) and the fifth conductive layer (anode 28a of Yamazaki) both comprise indium tin oxide (ITO).”

126. Yamazaki discloses anode 28a (which corresponds to the fifth conductive layer) can be formed of ITO (indium tin oxide alloy). EX1004, 20:6-12, Fig. 2.

127. Yamazaki does not expressly disclose that electrode 46 (which corresponds to the second conductive layer) is formed of ITO. Yamazaki discloses that electrode 46 can be formed using Al, Ti, Mo, W and the like, such as a lamination film of AL and TI. EX1004, 19:53-60. However, in addition to anode 28a, Yamazaki discloses that other electrodes can be formed of ITO, including the cathode electrode 1239 of the embodiment of Figs. 13A-13C (*Id.*, 31:43-52), the

anode electrode 1336(a) of the embodiment of Fig. 14 (*Id.*, 35:36-38), and anode electrode 1428(a) of the embodiment of Figs. 15A-15B (*Id.*, 36:16-23). Yamazaki also shows that both **anode 28a** and **electrode 46** are formed directly on the same insulation film 22. *Id.*, Fig. 2.

128. Anzai discloses an electroluminescent (“EL”) display device, with the first and second capacitors of claim 1, including **electrode layer 71** that corresponds to the second conductive layer. *See* §X.A.4. Anzai also discloses the light emitting device of claim 1, including **anode layer 61** that corresponds to the fifth conductive layer. *See* §X.A.6. Anzai teaches that both **electrode layer 71** and **anode layer 61** both comprise ITO. §X.D.

129. It would have been obvious to a POSITA to combine the teachings of Yamazaki and Anzai to use ITO as the material for the **electrode 46** since ITO was a well-known conductive material used for light emitting device electrodes, and **electrode 46** could be deposited at the same time as **anode 28a** for an efficient manufacturing process flow.

130. Anzai and Yamazaki are analogous prior art to the 121 patent, as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third area containing a light emitting device having an organic layer between two electrode layers.

131. A POSITA would have understood the issue involved, namely what material(s) can be used to form **electrode 46** and **anode 28a** of Yamazaki. To address this issue, a POSITA would have investigated what conductive material(s) would be appropriate. A POSITA would have been motivated to use ITO to form at least **electrode 46** and **anode 28a** of Yamazaki because (1) Yamazaki already teaches using ITO for **anode 28a** (EX1004, 20:6-12, Fig. 2), (2) Yamazaki teaches that **electrode 46** could be formed at the same time as **anode 28a** (given both **electrode 46** and **anode 28a** are directly formed on the same layer, namely, on insulation film 12) (*Id.*, Fig. 2), and (3) Anzai teaches using the same ITO material for the same two corresponding electrode layers (**anode layer 61** and combined **electrode layer 70/71**) (EX1003, 5:14-25; Figs. 3A-3B, 5:55-57).

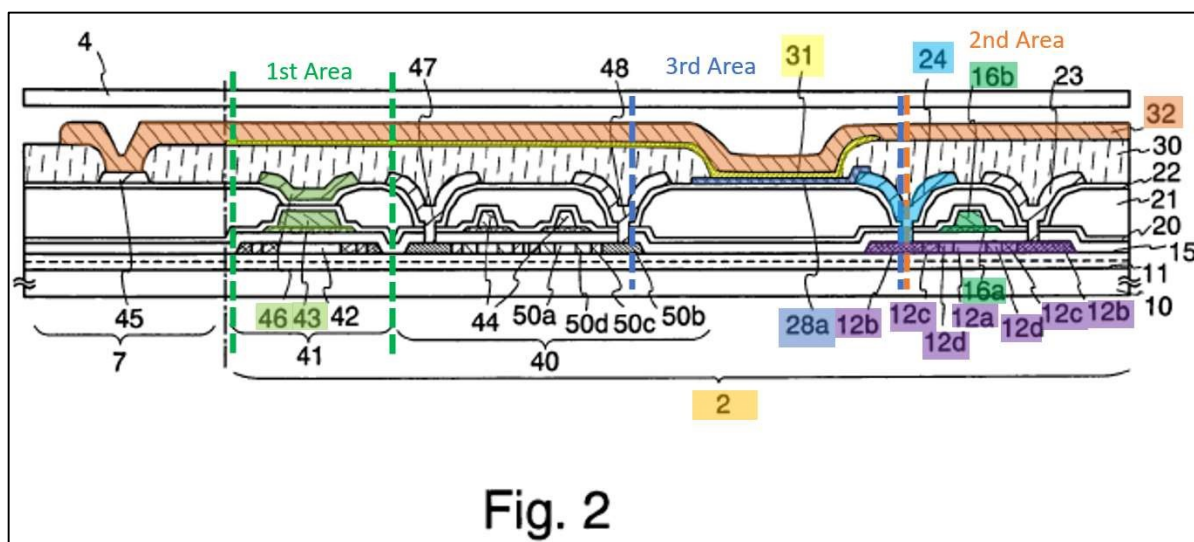
132. The modification to Yamazaki would simply involve selecting the same conductive material for **electrode 46** as **anode 28a**, which could be formed by the same process. A POSITA would have had a reasonable expectation of success in combining Anzai and Yamazaki, as both references disclose forming capacitors for use with organic electroluminescent devices, and both references teach using ITO for the anode layer. Moreover, because combining the teachings of Yamazaki and Anzai would involve known methods where it would have yielded predictable results.

F. Claim 6

133. The combination of Yamazaki and Anzai renders obvious “the device of claim 1 (*see* claim 1), wherein the second dielectric layer comprises a layer of passivation silicon nitride (Yamazaki’s insulating material 30) and a second organic layer (Yamazaki’s **EL layer 31**) formed on the layer of passivation silicon nitride (Yamazaki’s insulating material 30), the second organic layer (Yamazaki’s **EL layer 31**) comprising the same material as the first organic layer (Yamazaki’s **EL layer 31**).”

134. The 121 patent provides no meaning for “passivation layer.” In fact, the 121 patent discloses silicon nitride (SiN) as the sole example for this layer. For the passivation layer of the second dielectric layer, the 121 patent states: “A layer of passivation silicon nitride (SiN) 212 is formed over ILD208 and second metal patterns 210A and 210B.” EX1001, 5:34-36. A POSITA would understand from the 121 patent that there is no special meaning ascribed to passivation layer other than it is a layer of insulation material.

135. Yamazaki discloses that in the 1st area (**Capacitor Area**), the material between **cathode 32** and **electrode 46** includes insulation layer 30 (formed on **electrode 46**) and **EL layer 31** (formed on insulation layer 30), with **cathode 32** formed on **EL layer 31**). EX1004, Fig. 2.



Yamazaki further discloses that the same EL layer 31 (corresponding to the first organic layer) and cathode 32 (corresponding to the third conductive layer) in the third area, extend into the first area (where cathode 32 corresponds to the sixth conductive layer and EL layer 31 corresponds to the second organic layer). Therefore, the EL layer 31 in the first area comprises the same organic material as the EL layer 31 in the third area, because they are same layer.

G. Claim 7

136. The combination of Yamazaki and Anzai renders obvious “the device of claim 1 (*see* claim 1), wherein the second dielectric layer (Yamazaki’s modified insulating material 30) comprises a passivation layer (Yamazaki’s insulating material 30), a capping layer (Anzai’s planarization layer 19) on the passivation layer and a second organic layer (Yamazaki’s EL layer 31) formed on the capping layer, at least one of the passivation layer (insulating material 30) and the capping

layer (Yamazaki's insulating material 30) comprising silicon nitride, and the second organic layer (Yamazaki's [EL layer 31](#)) comprising the same material as the first organic layer (Yamazaki's [EL layer 31](#)).”

See §§XII.C, XII.D, and XII.F.

EXHIBIT A

Dean P. Neikirk

Emeritus Professor, Emeritus Cullen Trust for Higher Education Professorship in Engineering
Department of Electrical and Computer Engineering
Cockrell School of Engineering
The University of Texas at Austin
Austin, TX 78712

Education:

Oklahoma State University (Physics and Mathematics; with Honors)	B.S.	1979
California Institute of Technology (Applied Physics)	M.S.	1981
California Institute of Technology (Applied Physics)	Ph.D.	1984

Professional Experience:

Assistant Professor, University of Texas at Austin, Jan. 1984 - Aug. 1988
Associate Professor, University of Texas at Austin, Sept. 1988- Aug. 1992
Full Professor, University of Texas at Austin, Sept. 1992-Jan. 2021
Associate Dean of Graduate Studies, Aug. 2014 – Jan. 2021
Emeritus Professor, Feb. 2021 - present

Honors and Awards:

- 1984 Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter wave integrated circuits especially in the areas of detectors and imaging arrays."
- Listed in the Second Edition of Who's Who in Frontiers of Science and Technology, 5th Edition of Who's Who in Technology Today, 1994 American Men & Women of Science; 1985 Outstanding Young Man of America, 1989 Outstanding Young Man of America; 7th Edition of Who's Who in Technology.
- 1984-85 Engineering Foundation Faculty Award, University of Texas at Austin Engineering Foundation Advisory Council.
- 1985-90 General Motors Foundation Centennial Teaching Fellowship, University of Texas at Austin.
- 1985-86 IBM Corporation Faculty Development Award
- 1986 National Science Foundation Presidential Young Investigator.

- 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, College of Engineering, University of Texas at Austin.
- 1990-1992 Temple Foundation Endowed Faculty Fellowship (No. 1), University of Texas at Austin.
- 1992-present Cullen Trust for Higher Education Professorship in Engineering (No. 7), University of Texas.
- 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, University of Texas at Austin.
- 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, University of Texas at Austin.
- 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching
 - each year since 1956, Lockheed Martin and its predecessor, has sponsored an award for excellence in engineering teaching to reward one College of Engineering faculty member for exceptional teaching. This prestigious award is given to a faculty member dedicating time and energy in abundance to teaching undergraduate and graduate students. As a result, his or her work leaves a mark of excellence on the entire College of Engineering. Nominations for this award are made by The University of Texas at Austin engineering students and faculty. Final selection is made by a committee composed the five most recent faculty recipients of the award and the student presidents of the Student Engineering Council (SEC) and the Graduate Engineering Council (GEC).
- 2015 Civitatis Award: The University of Texas at Austin Civitatis Award was established in 1997 to recognize outstanding faculty citizenship. The Civitatis Award is conferred upon a member of the faculty in recognition of dedicated and meritorious service to the University above and beyond the regular expectations of teaching, research, and writing. The award is made by the President upon the recommendation of the Faculty Council Executive Committee. Prof. Neikirk was nominated for the award for his “extensive, effective and distinguished service record to his department, college and [the] University of Texas.”

Vita for Dean P. Neikirk:

Dean P. Neikirk was born in Oklahoma City, Oklahoma, on October 31, 1957. He received the B.S. degree (1979) in physics from Oklahoma State University, and the M.S. (1981) and Ph.D. (1984) degrees in applied physics from the California Institute of Technology. He joined the faculty of The University of Texas at Austin in 1984, and is currently a Professor in the Department of Electrical and Computer Engineering, holding the Cullen Trust for Higher Education Professorship in Engineering (No. 7). Dr. Neikirk developed the first monolithic, high resolution focal plane detector array for use at wavelengths between 0.1 mm and 1 mm, and in 1984 received the Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter

wave integrated circuits especially in the area of detectors and imaging arrays." He has also been named a 1986 National Science Foundation Presidential Young Investigator.

Dr. Neikirk's research interests concentrate on the fabrication and modeling of electromagnetic and micromachined sensors and actuators. His work also included projects involving integrated circuit processing and the high frequency properties of transmission lines. His work concentrated on the use of advanced fabrication techniques, including silicon micromachining, for new device and sensor development. Dr. Neikirk developed the teaching laboratory for semiconductor device fabrication at The University of Texas at Austin, and was an active member of The University of Texas at Austin Microelectronics Research Center. Recently Dr. Neikirk's research project related to the development of new chemical sensors (an "electronic taste" sensor) was selected for a commercialization venture between the University of Texas and LabNow, Inc. Dr. Neikirk has also served as the Graduate Advisor of the Department of Electrical and Computer Engineering at UT-Austin, an Associate Chairman of the ECE Department, the Chair of the UT-Austin Graduate Assembly, the Chair of the UT-Austin Faculty Council, the Secretary of the General Faculty at UT-Austin, and as an Associate Dean of the University of Texas at Austin Graduate School.

Professional Societies:

Senior Member, Institute of Electrical and Electronics Engineers

- Associate Editor for Solid State and VLSI Electronics, **IEEE Transactions on Education** (March 1991- Oct. 1994)

Commercialization of Technology:

Two companies have been founded based on technology developed by Dr. Neikirk's research group. In both cases the technology was developed at The University of Texas at Austin and licensed to start-ups.

From a University of Texas news release:

Firm commercializing University of Texas technology rounds up \$14 million venture capital investment (October 1, 2004)

AUSTIN, Texas—LabNow Inc. has received \$14 million in first-round venture investment for its point-of-care diagnostic system from the Soros Group, Austin Ventures and other investors.

The money will be used to develop the company's technology and to launch its initial product, CD4Now™, a point-of-care diagnostic tool for HIV/AIDS patients.

The device, which is based on technology developed at The University of Texas at Austin, quickly and accurately analyzes complex fluids such as blood.

Patents

1. US Patent 5,080,870: "Sublimating and Cracking Apparatus," Jan. 14, 1992; Inventors: B. G. Streetman, T. J. Mattord, D. P. Neikirk
2. US Patent 5,408,107: "Semiconductor Device Having Multiple Current-Voltage Curves and Zero-Bias Memory," April 18, 1995;
Inventors: Dean P. Neikirk and Kiran Kumar Gullapalli
3. US Patent 6,589,779: "General signaling protocol for chemical receptors in immobilized matrices," July 8, 2003;
Inventors: McDevitt; John T.; Anslyn; Eric V.; Shear; Jason B.; Neikirk; Dean P.
Assignee: Board of Regents, The University of Texas System (Austin, TX)
4. US Patent 6,602,702: "Detection system based on an analyte reactive particle," August 5, 2003
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)

Assignee: The University of Texas System (Austin, TX)

5. US Patent 6,649,403: "Method of preparing a sensor array," November 18, 2003
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
6. US Patent 6,680,206, "Sensor arrays for the measurement and identification of multiple analytes in solutions," January 20, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
7. US Patent 6,713,298, "Method and apparatus for the delivery of samples to a chemical sensor array," March 30, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Travis, TX); Shear; Jason B. (Travis, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
8. US Patent 6,908,770, "Fluid based analysis of multiple analytes by a sensor array," June 21, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
9. US Patent 7,022,517, "Method and apparatus for the delivery of samples to a chemical sensor array," April 4, 2006, filed: July 14, 2000
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX); Borich; Damon V. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
10. US Patent 7,316,899, "Portable sensor array system," January 8, 2008, filed: January 31, 2001
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
11. US Patent 7,491,552, "Fluid based analysis of multiple analytes by a sensor array," February 17, 2009, filed: January 20, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
12. United States Patent 7,651,868, "Method and system for the analysis of saliva using a sensor array," January 26, 2010, Filed: December 13, 2004

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: The Board of Regents of The University of Texas System (Austin, TX)

13. United States Patent 8,101,431, "Integration of fluids and reagents into self-contained cartridges containing sensor elements and reagent delivery systems," January 24, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

14. United States Patent 8,105,849, "Integration of fluids and reagents into self-contained cartridges containing sensor elements," January 31, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

15. United States Patent 8,257,967, "Method and system for the detection of cardiac risk factors," September 4, 2012, Filed: April 28, 2003

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

16. United States Patent 9,291,586, "Passive wireless self-resonant sensor," March 22, 2016, Filing Date: May 5, 2013

Inventors: Neikirk, Dean P. (Austin, TX, US), Pasupathy, Praveenkumar (Austin, TX, US), Zhang, Sheng (Austin, TX, US), Leonhardt, Brad (Austin, TX, US), Ekerdt, John G. (Austin, TX, US), Korgel, Brian A. (Austin, TX, US), Holmberg, Vincent C. (Seattle, WA, US), Shipman, Catherine D. (Reston, TX, US), Bogart, Timothy D. (Oxford, GB), Chockla, Aaron (Chicago, IL, US)

Assignee: Board of Regents, The University of Texas System (Austin, TX, US)

17. United States Patent 9,581,559, "Corrosion detection sensor embedded within a concrete structure with a diffusion layer placed over the sacrificial transducer," February 28, 2017, Filing Date: August 14, 2014

Inventors: Neikirk; Dean P. (Austin, TX), Wood; Sharon L. (Austin, TX), Pasupathy; Praveenkumar (Austin, TX), Yosef; Ali Abu (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

Publications:

A: Refereed archival journal publications

1. D. P. Neikirk and R. C. Powell, "Laser Time-Resolved Spectroscopy of Host-Sensitized Energy Transfer in $\text{Bi}_4\text{Ge}_3\text{O}_{12}:\text{Er}^{3+}$ Crystals," **J. Lumin.**, vol. 20, 1979, pp. 261-270.
2. R. C. Powell, D. P. Neikirk, J. M. Flaherty, and J. G. Gualtieri, "Lifetime Measurements, Infrared and Photoacoustic Spectroscopy of $\text{NdP}_5\text{O}_{14}$," **J. Phys. Chem. Solids**, vol. 41, 1980, pp. 345-350.
3. R. C. Powell, D. P. Neikirk, and D. Sadar, "Radiationless Decay Processes of Nd^{3+} Ions in Solids," **J. Opt. Soc. Am.**, vol. 70 (5), May 1980, pp. 486-490.
4. D. P. Neikirk, D. B. Rutledge, M. S. Muha, H. Park, and C. X. Yu, "Far-Infrared Imaging Antenna Arrays," **Appl. Phys. Lett.**, vol. 40 (3), 1 February 1982, pp. 203-205.
5. D. P. Neikirk, D. B. Rutledge, M.S. Muha, H. Park, and C. X. Yu, "Progress in Millimeter-Wave Integrated-Circuit Imaging Antenna Arrays," **Proc. Soc. Photo-Opt. Instr. Eng.**, vol. 317, 1981, pp. 206-211.
6. D. P. Neikirk, D. B. Rutledge, P.P. Tong, H. Park, and P. E. Young, "Imaging Antenna Array at $119\mu\text{m}$," **Appl. Phys. Lett.**, vol. (41), 15 August 1982, pp. 329-331.
7. D. P. Neikirk and D. B. Rutledge, "Self-Heated Thermocouples for Far-Infrared Detection," **Appl. Phys. Lett.**, vol. 41, (5), 1 September 1982, pp. 400-402
8. P.P. Tong, D. P. Neikirk, D. Psaltis, D. B. Rutledge, K. Wagner, and P. E. Young, "Tracking Antenna Arrays for Near- Millimeter Waves," **IEEE Trans. Antennas Propagat.**, vol. AP- 31, May, 1983, pp. 512-515.
9. D. P. Neikirk and D. B. Rutledge, "Air-Bridge Microbolometer for Far-Infrared Detection," **Appl. Phys. Lett.** **44**, 15 Jan. 1984, pp. 153-155.
10. P.P. Tong, D. P. Neikirk, D. B. Rutledge, P. E. Young, W. A. Peebles, N. C. Luhmann, Jr., "Imaging Polarimeter Arrays for Near-Millimeter Waves," **IEEE Trans. Microwave Theory Tech. MTT-32**, March 1984, pp. 507-512.
11. D. P. Neikirk, D. B. Rutledge, and W. Lam, "Far-Infrared Microbolometer Detectors," **Int. J. Infrared and Millimeter Waves** **5**, March 1984, pp. 245-277.
12. D. P. Neikirk and D. B. Rutledge, "Far-Infrared Imbedding Impedance Measurements,"

Int. J. Infrared and Millimeter Waves **5**, July 1984, pp. 1017-1026.

13. P. E. Young, D. P. Neikirk, P.P. Tong, D. B. Rutledge, and N. C. Luhmann, Jr., "Multichannel far-infrared phase imaging for fusion plasmas," **Rev. Sci. Instrum.** **56**, Jan. 1985, pp. 81-89.

14. P. E. Young, N. C. Luhmann, Jr., R. J. Taylor, D. P. Neikirk, and D. B. Rutledge, "Far-infrared imaging of tokamak plasma," **Rev. Sci. Instrum.** **56**, May 1985, pp. 903-904.

15. Y. Fukuoka, Q. Zhang, D. Neikirk, and T. Itoh, "Analysis of multilayer interconnection lines for a high speed digital integrated circuit," **IEEE Trans. Microwave Theory Tech. MTT-33**, June 1985, pp. 527-532.

16. N. Song, D. P. Neikirk, and T. Itoh, "Modeling of Ion-implanted GaAs MESFETs by the Finite Element Method," **IEEE Electron Device Lett. EDL-7**, April 1986, pp. 208-210.

17. V. P. Kesan, D. P. Neikirk, B. G. Streetman, and P. A. Blakey, "A New Transit Time Device Using Quantum Well Injection," **IEEE Electron Device Lett. EDL-8**, April 1987, pp. 129-131.

18. A. C. Cambell, V. P. Kesan, G. E. Crook, C. M. Maziar, D. P. Neikirk, and B. G. Streetman, "Impedance Switching Effects in GaAs/AlAs Barrier Structures," **Electronics Letters** **23**, Aug 27, 1987, pp. 926-927.

19. Y. D. Lin, D. P. Neikirk, and T. Itoh, "Coplanar Waveguide Phase Shifter Controlled by a Spatially Periodic Optical Illumination," **Int. J. Infrared and Millimeter Waves** **8**, Sept. 1987, pp. 1027-1036.

20. C. W. Farley, G. E. Crook, V. P. Kesan, T. R. Block, H. A. Stevens, T. J. Mattord, D. P. Neikirk, and B. G. Streetman, "Substrate Rotation and Carbon Generation in a Molecular Beam Epitaxy System," **J. Vac. Science Tech. B**, Sept./Oct. 1987, pp. 1374-1376.

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23. V. P. Kesan, A. Mortazawi, D. P. Neikirk, and T. Itoh, "Monolithic Millimeter-Wave Oscillator using a Transmission Line Periodically Loaded by QWITT Diodes," **Electronics Letters**, May 26, 1988, pp. 666-667.

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25. V. P. Kesan, A. Dodabalapur, D. P. Neikirk, and B. G. Streetman, "Growth and Rapid Thermal Annealing of AlGaAs/InGaAs Pseudomorphic Modulation-doped Structures," **Appl. Phys. Lett.** **53**, 22 Aug. 1988, pp. 681-683.
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29. C. S. Kyono, V. P. Kesan, D. P. Neikirk, C. M. Maziar, and B. G. Streetman, "Dependence of Apparent Barrier Height on Barrier Thickness for Perpendicular Transport in AlAs/GaAs Single Barrier Structures Grown by MBE," **Appl. Phys. Lett.** **54**, 6 Feb. 1989, pp. 549-551.
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31. R. L. Rogers and D. P. Neikirk, "Radiation Properties of Slot and Dipole Elements on Layered Substrates," **Int. J. Infrared and Millimeter Waves** **10**, June 1989, pp. 697-728.
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34. S. M. Wentworth, D. P. Neikirk, and C. R. Brahce, "The High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," **IEEE. Trans. Components, Hybrids, and Manufacturing Tech.** **12**, Sept. 1989, pp. 340-347.

35. V. P. Kesan, A. Mortazawi, D. R. Miller, V. K. Reddy, D. P. Neikirk, and T. Itoh, "Microwave and Millimeter Wave QWITT Diode Oscillators," **IEEE Trans. Microwave Theory Tech. MTT-37**, Dec. 1989, pp. 1933-1941.
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159. Jong Yeon Park, James E. Gardner, Praveen Pasupathy, Ji Won Suk, Rodney S. Ruoff, and Dean P. Neikirk, “Fabrication and Characterization of Wavelength Selective Microbolometers using a Planar Self-aligned Process for Low Deformation Membranes,” in MOEMS and Miniaturized Systems XI, part of SPIE MOEMS-MEMS, San Francisco, California, 25 Jan 2012, SPIE Paper Number 8252-33, Proc. SPIE 8252, 82520Y (2012); <http://dx.doi.org/10.1117/12.906290> , 7 pages.

160. Ye Chen, Praveen Pasupathy, Tanuj Trivedi, Dean P. Neikirk and Sharon L. Wood, “Improved magneto-inductive waveguide as wireless sensor net for structural health monitoring,” Nondestructive Characterization for Composite Materials, Aerospace Engineering, Civil Infrastructure, and Homeland Security 2012, San Diego, California, USA, Proc. SPIE 8347, 83472H (2012); <http://dx.doi.org/10.1117/12.915227>, Monday 12 March 2012, 8 pages.

161. Ali E. Abu-Yosef, Praveen Pasupathy, Sharon L. Wood and Dean P. Neikirk, “Detection of multiple corrosion thresholds in reinforced concrete structures using passive sensors,” Nondestructive Characterization for Composite Materials, Aerospace Engineering, Civil Infrastructure, and Homeland Security 2012, San Diego, California, USA, Proc. SPIE 8347, 83470J (2012); <http://dx.doi.org/10.1117/12.915164> , Monday 12 March 2012, 7 pages.

162. JinYoung Kim, Praveenkumar Pasupathy, Sharon L. Wood and Dean P. Neikirk, “Enhanced resolution of passive wireless conductivity sensors,” Sensors and Smart Structures Technologies for Civil, Mechanical, and Aerospace Systems 2012, San Diego, California, USA, Proc. SPIE 8345, 83451B (2012); <http://dx.doi.org/10.1117/12.916754> , Monday 12 March 2012, 7 pages.

163. Tanuj Trivedi, Frank Raffaeli, Praveen Pasupathy, Ali E. Abu-Yousef, Ye Chen, Dean Neikirk and Sharon Wood, “A reflectometer-based reader for passive wireless structural surveillance sensors,” Nondestructive Characterization for Composite Materials, Aerospace Engineering, Civil Infrastructure, and Homeland Security 2012, San Diego, California, USA, Proc. SPIE 8347, 83470I (2012); <http://dx.doi.org/10.1117/12.915223> Monday 12 March 2012, 7 pages.

164. Hoo Kim and Dean P. Neikirk, “Three Dimensional Dual-band Stacked Microbolometer Design using resistive dipoles and slots,” SPIE Infrared Technology and Applications XXXIX, edited by Bjørn F. Andresen, Gabor F. Fulop, Charles M. Hanson, Paul R. Norton, Proc. of SPIE Vol. 8704, 870419, 11 June 2013.

165. Dean P. Neikirk, Hoo Kim, Jong Yeon Park, Joo-Yun Jung, “Patterned resistive sheets for use in infrared microbolometers,” SPIE Security + Defence, 25 Sep 2013 4:00 PM - 4:20 PM.

C. Published Abstracts

1. P.E. Young, Q.-X. Yu, W. A. Peebles, N.C. Luhmann, Jr., D. P. Neikirk, and D. B. Rutledge, "Application of Far-Infrared Imaging Arrays to Plasma Density and Magnetic Field Measurements," 4th APS Topical Conference on High Temperature, 1982.
2. P.E. Young, Q.-X. Yu, W.A. Peebles, N.C. Luhmann, Jr., D. P. Neikirk, and D. B. Rutledge, "Demonstration of Far-Infrared Phase Imaging," 24th Annual Meeting, Division of Plasma Physics, New Orleans, La., November, 1982.
3. P. E. Young, W.A. Peebles, N.C. Luhmann, Jr., R.J. Taylor, D. B. Rutledge, D. P. Neikirk, and P.P. Tong, "Current Profile Measurements in a Tokamak Plasma," 25th Ann. APS Meeting, Div. of Plasma Physics, Nov., 1983.
4. D. B. Rutledge, D. P. Neikirk, P.P. Tong, P.E. Young, W.A. Peebles, N.C. Luhmann, Jr., and R.J. Taylor, "Demonstration of a FIR Imaging System as a Multi-Channel Interferometer," 25th Ann. APS Meeting, Div. of Plasma Physics, Nov., 1983.
5. P.E. Young, N.C. Luhmann, Jr., R.J. Taylor, D. P. Neikirk, and D. B. Rutledge, 26th Annual Meeting of the Division of Plasma Physics, Boston, MA, Oct 29- Nov 2, 1984.
6. D.L. Brower, W.A. Peebles, S. Kim, R.L. Savage, Jr., T. Lehecka, N.C. Luhmann, Jr., J. Wagner, D. B. Rutledge, D. P. Neikirk, P.E. Young, and H.K. Park, "Recent advances in multichannel far-infrared collective scattering and interferometry systems," Eleventh Symposium on Fusion Engineering, Austin, TX, Nov. 18-22, 1985.
7. A.C. Campbell, V.P. Kesan, G.E. Crook, C.M. Maziar, D. P. Neikirk, and B. G. Streetman, "Capacitive Hysteresis Effects in 5.0nm single and double barrier AlAs Tunneling Structures," 8th Molecular Beam Epitaxy Workshop, Los Angeles CA, September 9-11, 1987.
8. A.C. Campbell, V.P. Kesan, G.E. Crook, D. P. Neikirk, and B. G. Streetman, "Capacitance Transient Analysis of GaAs/AlAs Tunneling Structures," 1988 Electronics Materials Conference, University of Colorado, Boulder, Colorado, June 22-24, 1988.
9. V.P. Kesan, A. Dodabalapur, D. P. Neikirk, and B. G. Streetman, "Influence of MBE Growth and Rapid Thermal Annealing Conditions on the Electrical Properties of Normal and Inverted AlGaAs/InGaAs Pseudomorphic HEMT Structures," IEEE 46th Annual Device Research Conference, June 20-22, 1988, Boulder, CO.

10. A. Dodabalapur, V.P. Kesan, T.R. Block, D. P. Neikirk, and B. G. Streetman, "Optical and Electrical Characteristics of Normal and Inverted AlGaAs/InGaAs Pseudomorphic HEMT Structures Processed by RTA," 9th Molecular Beam Epitaxy Workshop, West Lafayette, Indiana, September 21-23, 1988.
11. A. Sharif, D. P. Neikirk, and D.R. Diller, "Design and Fabrication of a Multi-Sensor Cryomicroscope Stage using VLSI Technology," Cryo 89, Charleston, SC, June 1989, published in **Physics in Medicine and Biology** 33.
12. A. Dodabalapur, V.P. Kesan, D. P. Neikirk, B. G. Streetman, M.H. Herman, and I.D. Ward, "Photoluminescence and Electreflectance Characterization of Modulation-Doped Quantum Wells," Journal of Electronic Materials 18, July 1989, p. 51.
13. V.K. Reddy and D. P. Neikirk, "Influence of Growth Interruption on I - V Characteristics of AlAs/GaAs Double Barrier Resonant Tunneling Diodes," 11th Annual Molecular Beam Epitaxy Workshop, Austin TX, Sept. 16-18, 1991.
14. A.J. Tsao, V.K. Reddy, D.R. Miller, K.K. Gullapalli, and D. P. Neikirk, "The effect of barrier thickness asymmetries on the electrical characteristics of AlAs/GaAs double barrier resonant tunneling diodes," 11th Annual Molecular Beam Epitaxy Workshop, Austin TX, Sept. 16-18 1991.
15. T.R. Block, D. P. Neikirk, and B. G. Streetman, "MBE growth condition dependence of RHEED dampening and QW photoluminescence," Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.
16. T.J. Mattord, D. P. Neikirk, A. Srinivasan, A. Tang, K. Sadra, Y.C. Shih, and B. G. Streetman, "Real time flux monitoring and feedback control of a valved arsenic source" Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.
17. Y.C. Shih, D. P. Neikirk, and B. G. Streetman, "Effects of As flux on Si δ -doped GaAs," Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.
18. Y. Kim and D. P. Neikirk, "Monolithically integrated optically interrogated pressure microsensors," **J. Acoust. Soc. Am.**, Vol. 92, No. 4 (pt. 2), October 1992, p. 2353.
19. O. Hartin, D. P. Neikirk, A. Anselm, and B. Streetman, "Memory Switching Simulation in Resonant Tunneling Devices," 1997 American Physical Society March Meeting, Kansas City, MO, March 17-21, Bulletin of the American Physical Society, Vol. 42, No. 1, 1997, p. 548.
20. O. Hartin and D. P. Neikirk, "Tight Binding Simulation of Memory Switching in Resonant Tunneling Devices," 1997 American Physical Society International Conference on Computational Physics, University of California, Santa Cruz, Aug. 25, 1997.

21. D. Neikirk, "Embedded Passive Sensors for State Monitoring," presented at NSF Workshop on Exploring the Uses of Autoadaptive Media in Geotechnical Earthquake Engineering, Austin, TX, January 10-12 2001.

22. Lavigne, John J.; Savoy, Steve; Best, Michael; Anslyn, Eric V.; Shear, Jason B.; McDevitt, John T.; Neikirk, Dean, "Toward the development of an 'electronic tongue'," Book of Abstracts, 219th ACS National Meeting, San Francisco, CA, March 26-30, 2000 (2000), AGFD-193.

23. Wood, Sharon; Neikirk, Dean, "Development of a passive sensor to detect cracks in welded steel construction," US-Japan Joint Workshop and Third Grantees Meeting, US-Japan Cooperative Research in Urban Earthquake Disaster Mitigation, Monbu-Kgagku-sho and The National Science Foundation, Seattle, August 15-16, 2001.

24. McCleskey, Shawn C.; Goodey, Adrian P.; Rodriguez, Marc D.; McDevitt, John T.; Anslyn, Eric V.; Neikirk, Dean P., "Development of a multi-component sensor array for the simultaneous detection of various analytes in solution," Abstracts of Papers, 222nd ACS National Meeting, Chicago, IL, United States, August 26-30, 2001.

D. Other Major Publications

V. Kesan and D. P. Neikirk, "Quantum Well Devices," **Microwaves and RF**, vol. 25, July 1986, pp. 93-97.

D. P. Neikirk, P. Cheung, M.S. Islam, and T. Itoh, "Optically Controlled Coplanar Waveguide Phase Shifters," **Microwave Journal**, Dec. 1989, pp. 77-88.

D. P. Neikirk, "Quantum Wells and Other Deep Subjects," **Discovery**, Vol. 11, No. 3, 1989, pp. 5-8.

S. M. Wentworth, J. M. Lewis, and D. P. Neikirk, "Antenna-Coupled Thermal Detectors of mm-Wave Radiation," **Microwave Journal**, Jan. 1993, pp. 94-103.

E. Book Chapter

D. B. Rutledge, D. P. Neikirk, and D. Kasilingam "Integrated- Circuit Antennas," in **Infrared and Millimeter Waves**, vol. 11, editor K.J. Button, 1984.

Nicolaos Christodoulides, Priya Dharshan, Jorge Wong, Pierre N. Floriano, Dean Neikirk and John T. McDevitt, "A Microchip-Based Assay for Interleukin-6," In: *Methods in Molecular Biology*, Volume 385: Microchip-Based Assay Systems, Humana Press, ISBN 978-1-58829-588-0 (Print) 978-1-59745-426-1 (Online), Copyright 2008, pages 131-144.

F. Technical Reports

C-K Tzuang, D. P. Neikirk, and T. Itoh, "Finite Element Analysis of Slow-Wave Schottky Contact Printed Lines," Microwave Laboratory Report No. 87-P-2, AFOSR Grant 86-0036, Feb., 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 87-P-3, AFOSR Grant 86-0036, Jan., 1987.

V. P. Kesan and D. P. Neikirk, "Quantum Well Devices," Electrical Engineering Research Laboratory Report No. 87-P-8, Joint Services Electronics Program Research Contract AFOSR F49620-86-C-0045, August 7, 1987.

Stuart M. Wentworth and D. P. Neikirk, "High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," Microwave Laboratory Report No. 87-P-7, August 26, 1987.

Stuart M. Wentworth and D. P. Neikirk, "Characterization of Tape Automated Bonding (TAB) Interconnects at High Frequency," Microwave Laboratory Report No. 87-P-9, October 23, 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 90-P-1, Final Technical Report for AFOSR Grant 86-0036, Feb., 1990.

A. Mortazawi, D. Neikirk, and T. Itoh, "Microwave and millimeter wave oscillators and planar power combining structures for QWITT and Gunn diodes," Microwave Laboratory Report No. 90-P-4, Technical Report for ARO Grant DAAL03-88-K-0005 and JSEP Grant F49620-89-0044, Aug., 1990.

Oral Presentations

A. Professional Society Presentation

D. B. Rutledge and D. P. Neikirk, "Imaging Antenna Arrays," Invited Keynote Speakers, Sixth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 7-12, 1981.

D. P. Neikirk and D. B. Rutledge, "Advances in Microbolometers," Invited Keynote Speakers, Eighth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 12-17, 1983.

D. P. Neikirk, "Optically Controlled Coplanar Waveguide Millimeter Wave Phase Shifter," Tenth International Conference on Infrared and Millimeter Waves, Lake Buena Vista, Fl., Dec. 9-13, 1985.

D. P. Neikirk, "Picosecond Response of an Optically Controlled Millimeterwave Phase Shifter," Second Topical Meeting on Picosecond Electronics and Optoelectronics, Jan., 1987.

D. P. Neikirk, "Influence of Transit Time Effects on the Optimum Design and Maximum Oscillation Frequency of Quantum Well Oscillators," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "Measurements of an Optically Controlled Coplanar Waveguide Phase-Shifter," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "High Frequency Characterization of Tape-Automated Bonding Interconnects," 5th Annual Texas Regional Symposium, International Society of Hybrid Manufacturing, April 11, 1988.

D. P. Neikirk, "Time Dependent Simulation of the Quantum Well Injection Transit Time Diode," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

D. P. Neikirk, "Experimental Performance of a Periodically Illuminated Optically Controlled Coplanar Waveguide Phase Shifter," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

B. Invited Lectures

1. D. P. Neikirk, "Exotic Heterojunction Devices for Microwave Circuits," NSF Workshop on Future Research Opportunities in Electromagnetics, Arlington, TX., January 29-31, 1986.

2. D. P. Neikirk, "Optical Control of a Monolithic Millimeter Phase Shifter," ARO Workshop on Fundamental Issues in Millimeter and Submillimeter Waves, Los Angeles, Ca., Sept. 15-16, 1986.

3. Dean P. Neikirk, "Quantum Well Oscillators for Millimeter Wave Applications," 1987 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Hilton Head Island, S.C., March 2-4, 1987.

4. S.M. Wentworth and D. P. Neikirk, "High Frequency Tape-Automated Bonding (TAB) Interconnect Characterization," IEEE 6th Annual VLSI and GaAs Packaging Workshop, Sept. 14-16, 1987.

5. D. P. Neikirk, "The quantum well injection transit time diode," Engineering Foundation Conference on Advanced Heterostructure Transistors, Keauhou-Kona, Hawaii, Dec. 5-10, 1988.
6. D. P. Neikirk, ""The High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," presented to the Microelectronics and Computer Technology Corporation, April 19, 1989.
7. Dean P. Neikirk, "Impedance measurements of quantum well diodes for millimeter wave applications," 1990 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), San Francisco, CA., Feb. 12-14, 1990.
8. Dean P. Neikirk, "Twin-slot multi-layer substrate-supported antennas and detectors for terahertz imaging," First International Symposium on Space Terahertz Technology, University of Michigan, Ann Arbor, Mich., March 5-6, 1990.
9. Dean P. Neikirk, "Microwave and Millimeterwave Oscillators using Quantum Well Diodes," Joint IEEE MTT/ED Dallas Chapter meeting, Sept. 27, 1990.
10. Dean P. Neikirk, "Quantum Transport Simulations of Resonant Tunneling Diodes," 1991 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Ft. Lauderdale, FL., Feb. 18-20, 1991.
11. Dean P. Neikirk, "The Application of Physics in Electrical Engineering (or is it Engineering in Physics?): Electromagnetics in Very High Frequency Semiconductor Devices," Physics Colloquium, Oklahoma State University, March 5, 1992.
12. D. P. Neikirk and B. G. Streetman, "MBE growth of multilayer heterostructures for photonic and high-speed electronic devices," Engineering Foundation Conference on High Speed Optoelectronic Devices and Circuits II, Banff, Alberta, Canada, Aug. 9-13, 1992.
13. L. T. Pillage, D. P. Neikirk, and R. Mercer, "Design automation techniques and algorithms for application specific electronic modules (ASEMs)," ARPA Electronic Packaging & Interconnect Principle Investigator Meeting, Marina del Ray, CA, Feb. 14-18, 1994.
14. D. P. Neikirk, "Micro-sensors - What happens when you make classical devices small?: Integrated Bolometric Radiation Detectors," Texas Instruments, Dallas, Texas, Oct. 20, 1994.
15. Dean P. Neikirk, "Micromachined sensors," Motorola Sensors Steering Committee, Albuquerque, New Mexico, March 28, 1995.
16. D. P. Neikirk, E. Tuncer, and B.-T. Lee, "The Use of Effective Internal Impedance Approximations in Lossy Transmission Line Modeling," *Progress in Electromagnetics*

Research Symposium PIERS 95, The University of Washington, Seattle, Washington, July 28, 1995.

17. D. P. Neikirk, M. S. Islam, and E. Tuncer, "Accurate Quasi-Static Modeling of Transmission Lines on Semiconducting Substrates," *Progress in Electromagnetics Research Symposium PIERS 95*, The University of Washington, Seattle, Washington, July 28, 1995.

18. D. P. Neikirk, "Impact of Finite Metal Conductivity on Inductance Extraction of Interconnects and Packages," Sematech meeting on Electrical Modeling Challenges Faced by Packaging Designers, Austin, Texas, Nov. 19, 1995.

19. D. P. Neikirk, "Micromachined Fabry-Perot Pressure Transducers," Hughes Research Laboratory, Malibu, California, Nov. 21, 1995.

20. D. P. Neikirk, "Classical Devices Made Small; or 'What's the big deal about little machines?'" , Manufacturing 2000, University of Texas at Austin, Feb. 23, 1996.

21. D. P. Neikirk, "Interconnect Inductance Modeling from DC to the Skin Effect Limit," Quad Designs, Camarillo, CA, July 10, 1996.

22. D. P. Neikirk, "Efficient Conductor Boundary Conditions in the dc to Skin Effect Limit," DARPA MAFET Program Review, Fairfax, VA, Oct. 27-31, 1997.

23. Micromachined Array-based Multi-analyte Chemical Sensors: Towards the Fabrication of an "Electronic Tongue" South, Texas Local Section of The Electrochemical Society Meeting, April 17, 1999.

24. D. P. Neikirk, "Resonant Chemical Surveillance Tags," IEEE Electron Device Chapter, Central Texas Section, September 25, 2008.

25. D.P. Neikirk, "Near Borehole Condition Sensing," Nanotechnology Conference and Trade Show - Nanotech 2009, Houston, TX May 3-7, 2009, Nanotech & Cleantech for Oil & Gas Session, (Session chair: Sean Murphy, Advanced Energy Consortium), May 5, 2009.

26. D.P. Neikirk, "Integrated Threshold Nanosensor Systems," Advanced Oil Consortium Microfabricated Sensors Workshop, Houston Research Center, Bureau of Economic Geology, University of Texas at Austin, September 8th-9th, 2010.

27. D. P. Neikirk, "Sensing systems for "harsh" environments," Engineering Challenges for Deepwater Drilling at the "U.S. Offshore Oil Exploration: Managing Risks to Move Forward," James A. Baker III Institute for Public Policy and PFC Energy, Rice University, Houston, TX, February 11, 2011.

C. Other Conference Presentations

Praveen Pasupathy, Mingxiang Zhuzhou, Shasi K. Munukutla, Dean P. Neikirk, and Sharon L. Wood, “Resonant Wireless Sensor Nets for Civil Infrastructure Health Monitoring,” 2009 National Science Foundation Division of Civil, Mechanical and Manufacturing Innovation (CMMI) Engineering Research and Innovation Conference, Honolulu, Hawaii, June 22-25, 2009.

Technical Consulting

Teltech Resource Network (1985-1993)
Ardex, Inc. (1986-88)
University and Polytechnic Grants Committee, Consultancy to examine Equipment Requirements for the Hong Kong University of Science and Technology, July, 1989
E. P. Hamilton Associates, (1987-90)
Burnett Company, Microwave Heating for Secondary Oil Recovery, July, 1990
Microelectronics and Computer Technology Corporation, June, 1990
Microelectronics and Computer Technology Corporation, Oct., 1994 - Sept., 1996
Baker-Hughes

University Committee Assignments

Departmental:

Graduate Student Financial Aid, Sept. 1984- Sept. 1987
Faculty Recruiting, Sept. 1984- Aug. 1985
Microelectronics Jr. Faculty Recruiting, Sept. 1985- Sept. 1987 (chairman)
ECE Safety Committee, Sept. 1985- Aug. 1993 (chairman, 1985-89)
ECE Electronics Shop Coordinating Committee, March 1986- Aug. 1993
Solid State Electronics Area Graduate Advisor, Aug. 1986- Aug. 89
ECE Space Allocation Committee, Sept. 1989-Aug. 1993 (chairman)
ECE Facilities Committee, Sept. 1993- Aug. 1996 (chairman)
ECE Areas Committee, Electromagnetics/Acoustics, Sept. 1993-present
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1995- Aug. 1995
ECE World Wide Web Home Page Committee, Sept. 1995-Aug. 1996
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1997- Aug. 1997
ECE Areas Committee, Materials and Quantum Electronics, Sept. 1993-present; chairman, Sept. 1996-present
Chair of ECE Graduate Studies Committee, May 1998-August 2006
ECE Chair's council, November 1999-2010
ECE Graduate Advisor, Sept. 1999- 2010
ECE Associate Chair, Sept. 2001-Dec. 2010
ECE peer Faculty Annual Review Committee, Sept. 2012-Aug. 2013

College:

Engineering Scholastic Appeals, Sept. 1984- Aug. 1985
Engineering Safety Committee, Sept. 1985- Aug. 1994 (chairman, Sept. 1989-Aug. 1994)

Aerospace Engineering Machine Shop, Sept. 1989-Aug. 1993
College Annual Report Quality Team, Jan. 1994- Aug. 1994
College Multimedia Committee, Sept. 1995-Aug. 2000
Equal Opportunity in Engineering (EOE) Program, 1995-Dec. 1996
Graduate Fellowship Review Committee, Sept. 2011-Aug. 2013

University:

Presidential Ad Hoc Committee on Research Infrastructure Enhancement, Jan. 1988 - Aug. 1994
Research Safety Advisory Committee, Oct. 1991-present (chairman, Sept. 1996-1999)
Ad Hoc Consultative Committee for the Selection of a Dean of the College of Engineering, Nov. 1995-May 1996
Faculty Building Advisory Committee, Sept. 1995-Aug. 2000; Aug. 2003-Aug. 2004
Ad Hoc Project Committee for Parking Garage # 4A, Sept. 1996-Aug. 2000
Faculty Council, Sept. 1996-Aug. 2000; Sept. 2002 - Aug. 2004
Faculty Advisory Committee on the Budget, Sept. 99 - Aug. 2000; Sept. 2008 – Aug. 2011 (vice chair Sept. 2009- Aug. 2010)
Graduate Assembly, April 1997- Aug. 2000; Sept. 2001 - Aug. 2008
Administrative sub-committee of GA, Sept. 1997-Aug. 1998; Sept. 2006-Aug. 2007
Academic sub-committee of GA, Sept. 1998-Aug. 2000; Sept. 2001-Aug. 2006; Sept. 2007-Aug. 2008
Chair, Graduate Assembly, 2004-2005
Academy of Distinguished Teachers selection committee, academic year 1999-2000
Outstanding Graduate Adviser selection committee, academic year 1999-2000
Outstanding Graduate Coordinator selection committee, academic year 1999-2000
Faculty Council, Sept. 2008 – Aug. 2012; Chair-elect Sept. 2009- Aug. 2010; Chair Sept. 2010- Aug. 2011; past chair: Sept. 2011-Aug. 2012
Faculty Council Executive Committee, Sept. 2009 – Aug. 2012
General Faculty Rules and Governance Committee, Sept. 2010 – Aug. 2015 (Chair, Sept. 2011 – Aug. 2013)
Ad Hoc Consultative Committee for the Selection of a Dean of the Graduate School, Nov. 2012 – Sept. 2012
Secretary of the General Faculty and Faculty Council, Sept. 2013 – Aug. 2015
Committee on Undergraduate Degree Program review, Sept. 2013 – Aug. 2015
Faculty Council Executive Committee, Sept. 2013 – Aug. 2015
Faculty Committee on Committees, *ex officio* member, Sept. 2013 – Aug. 2015

UT System:

Task Force on Doctoral Programs and Post-Doctoral Experience, Spring-Fall 2006

University of Texas System Faculty Advisory Council, Sept. 2009- Aug. 2011

State of Texas:

Texas Higher Education Coordinating Board Graduate Education Advisory Committee (GEAC), September 1, 2015 - August 31, 2018.

Evidence of Teaching Effectiveness

Senior Design Projects:

Umer Yousafzai and Venuka Jayatilaka, Spring 1994

Chris Eiting and Sonny Gonzalez, Spring 1994

David Lee and David Onsongo, Fall 1996

Dave Pyle and Aruna Murthy, Spring 1999

Hitesh Mehta and Edward Zhu, Spring 1999, "Giving the electronic tongue a sense of good taste: image analysis tools and GUI"

Gus Espinosa and Donnie Garcia, Spring 1999, "Design and Implementation of a Computer Interfacing Circuit to Control LED's for use with a Chemical Sensor"

Nathanant Pon Skulkaew and Prem Nainani, Spring 2001, "PC-based data acquisition and wireless transmission system"

Matthew Andringa and Allen Hall, Spring 2001, "Non-Invasive RFID Weld Inspection"

Michael Amalfitano and Sapun Parekh, Spring 2002, "Output circuitry for a transmitter used in an Electronic Structural Surveillance system"

Kunal Patel and Jacy Little, Spring 2002, "Swept, high frequency oscillator to work in an Electronic Structural Surveillance (ESS) system"

Dong Pak, Spring 2002, "Automated image-processing software of an electronic chemical sensor"

Rajesh Nerlikar, Jonathan Solomon, Spring 2003, "Wireless Data Acquisition System for Bluetooth-enabled RFID Readers"

Nola Li, Judith Chen, Maria Huang, Fall 2003, "Design and build a tuning network for a swept frequency reader used in structural health analysis"

Tuenlap (Daniel) Chan, Imranul Islam, Derek Choi, Spring 2004, "Design and build an RFID Interrogator Receiver"

John McKee and Terence Man, Spring 2007, "Improved Corrosion Sensors"

Abdulaziz Beayeyz, Sravan Bhagavatula, Rahul Mitra, Shasi Munukutla, Spyder Spann, Fall 2009, "Portable Corrosion Detector"

Jonathan Pham, Po-Han Wu, Josh Schulte, Pritesh Solanki, Mesele Bedasa, Spring 2011- Fall 2011, "Multi-Sensor Robotics Platform"

Raymund Lee, Simon Chow, Connor Landy, Kevin Woo, and Anirudh Kashyap, Fall 2012-Spring 2013, "Variable Frequency RFID Tag and Reader"

Javier Chacon, Joshua Poncik, Joshua Orozco, Sebastian Salomon, Yongcong Zou, Fall 2013-Spring 2014, "Environmental Sensor Monitoring Network"

Organized Classes Taught:

EE 363M Introduction to Microwaves, Spring 1984, # 16455
EE 396K VLSI Fabrication Techniques, Fall 1984, # 16255
EE 379K Integrated Circuit Fabrication, Spring 1985, # 16055
EE 396K VLSI Fabrication Techniques, Fall 1985, # 16275
EE 379K Integrated Circuit Fabrication, Fall 1985, # 16070
EE 396K VLSI Fabrication Techniques, Spring 1986, # 17680
EE 379K Integrated Circuit Fabrication, Spring 1986, # 17450
EE 396K VLSI Fabrication Techniques, Fall 1986, # 15245
EE 379K Integrated Circuit Fabrication, Fall 1986, # 15020
EE 396K VLSI Fabrication Techniques, Spring 1987, # 15205
EE 379K Integrated Circuit Fabrication, Spring 1987, # 14970
EE 396K VLSI Fabrication Techniques, Fall 1987, # 15010
EE 440 Integrated Circuit Fabrication, Fall 1987, # 14545
EE 363M Introduction to Microwaves, Spring 1988, # 14535
EE 396K VLSI Fabrication Techniques, Spring 1988, # 14865
EE 440 Integrated Circuit Fabrication, Spring 1988, # 14390
EE 396K VLSI Fabrication Techniques, Fall 1988, # 15165
EE 440 Integrated Circuit Fabrication, Fall 1988, # 14705
EE 363M Introduction to Microwaves, Spring 1989, # 14525
EE 396K VLSI Fabrication Techniques, Spring 1989, # 14855
EE 396K VLSI Fabrication Techniques, Fall 1989, # 15165
EE 440 Integrated Circuit Fabrication, Fall 1989, # 14705
EE 363M Introduction to Microwaves, Spring 1990, # 14050
EE 396K VLSI Fabrication Techniques, Spring 1990, # 14355, 14360
EE 440 Integrated Circuit Fabrication, Spring 1990, # 13915, 13920
EE 396K VLSI Fabrication Techniques, Fall 1990, # 14630, 14635
EE 440 Integrated Circuit Fabrication, Fall 1990, # 14200, 14205
EE 363M Introduction to Microwaves, Spring 1991, # 14365
EE 396K VLSI Fabrication Techniques, Spring 1991, # 14660, 14665, 14670
EE 440 Integrated Circuit Fabrication, Spring 1991, # 14220, 14225, 14230
EE 396K VLSI Fabrication Techniques, Fall 1991, # 14865, 14860
EE 440 Integrated Circuit Fabrication, Fall 1991, # 14425, 14430
EE 363M Introduction to Microwaves, Spring 1992, # 14270
EE 396K VLSI Fabrication Techniques, Spring 1992, # 14545, 14550, 14555
EE 440 Integrated Circuit Fabrication, Spring 1992, # 14130, 14135
EE 396K VLSI Fabrication Techniques, Fall 1992, # 15095, 15100, 15105
EE 440 Integrated Circuit Fabrication, Fall 1992, # 14670, 14675
EE 397K Microwave Devices, Spring 1993, # 14805
EE 396K VLSI Fabrication Techniques, Fall 1993, # 14800, 14805, 14810
EE 440 Integrated Circuit Fabrication, Fall 1993, # 14385, 14390
EE 363M Introduction to Microwaves, Spring 1994, # 14370
EE 396K VLSI Fabrication Techniques, Fall 1994, # 14365

EE 440 Integrated Circuit Fabrication, Fall 1994, # 13870
 EE 397K Electromagnetics in Packaging, Spring 1995, # 14555
 EE 396K VLSI Fabrication Techniques, Fall 1995, # 14765
 EE 440 Integrated Circuit Fabrication, Fall 1995, # 14260
 EE 397K Electromagnetics in Packaging, Spring 1996, # 14695
 EE 382M Simulation Methods in CAD/VLSI, Spring 1996, # 14500
 EE 396K VLSI Fabrication Techniques, Fall 1996, # 14535
 EE 440 Integrated Circuit Fabrication, Fall 1996, # 14090
 EE 382M Simulation Methods in CAD/VLSI, Spring 1997, # 14325
 EE 363M Introduction to Microwaves, Spring 1997, # 14120
 EE 396K VLSI Fabrication Techniques, Fall 1997, # 15315
 EE 440 Integrated Circuit Fabrication, Fall 1997, # 14820
 EE 363M Introduction to Microwaves, Spring 1998, # 14530
 EE 397K Microwave Devices, Spring 1998, # 14950
 EE 396K VLSI Fabrication Techniques, Fall 1998, # 15475
 EE 440 Integrated Circuit Fabrication, Fall 1998, # 14965
 EE 363M Introduction to Microwaves, Spring 1999, # 14825
 EE 397K Microwave Devices, Spring 1999, # 15260
 EE 396K VLSI Fabrication Techniques, Fall 1999, # 15340
 EE 440 Integrated Circuit Fabrication, Fall 1999, # 14820
 EE 363M Introduction to Microwaves, Spring 2000, # 14755
 EE 396K VLSI Fabrication Techniques, Fall 2000, # 15600
 EE 440 Integrated Circuit Fabrication, Fall 2000, # 15100
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2001, #15170
 EE 396K VLSI Fabrication Techniques, Fall 2001, # 15725
 EE 440 Integrated Circuit Fabrication, Fall 2001, # 15230
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2002, #15330
 EE 396K VLSI Fabrication Techniques, Fall 2002, # 16050
 EE 440 Integrated Circuit Fabrication, Fall 2002, # 15485
 EE 397K Microwave Devices, Spring 2003, # 15110
 EE 396K VLSI Fabrication Techniques, Fall 2003, # 15580
 EE 440 Integrated Circuit Fabrication, Fall 2003, # 15095
 EE 325 Electromagnetic Engineering, Spring 2004, # 14345
 EE 396K VLSI Fabrication Techniques, Fall 2004, # 16250
 EE 440 Integrated Circuit Fabrication, Fall 2004, # 15715
 EE 396K 26-Microelectromechanical Systems, Spring 2005, # 15690
 EE 396K VLSI Fabrication Techniques, Fall 2005, # 16455
 EE 440 Integrated Circuit Fabrication, Fall 2005, # 15930
 EE 396K VLSI Fabrication Techniques, Fall 2006, # 17040
 EE 440 Integrated Circuit Fabrication, Fall 2006, # 16430
 EE 325 Electromagnetic Engineering, Spring 2007, # 15765
 EE 396K VLSI Fabrication Techniques, Fall 2007, # 17425
 EE 440 Integrated Circuit Fabrication, Fall 2007, # 16770
 EE 396K-26 Microelectromechanical Systems, Spring 2008, # 16815
 EE 396K VLSI Fabrication Techniques, Fall 2008, # 17380
 EE 325 Electromagnetic Engineering, Spring 2009, # 16000

EE 396K-24 Microwave Devices, Spring 2010, # 16975
 EE 396K VLSI Fabrication Techniques, Fall 2010, # 17075, 17080, 17085, 17090
 EE 440 Integrated Circuit Fabrication, Fall 2010, # 16540, 16545, 16550, 16555
 EE 396K VLSI Fabrication Techniques, Fall 2011, # 17295, 17300, 17305, 17310
 EE 440 Integrated Circuit Fabrication, Fall 2011# 16760, 16765, 16770, 16775
 EE 396K 26-Microelectromechanical Systems, Spring 2012, #17070
 EE 396K VLSI Fabrication Techniques, Fall 2012, # 17185, 17190, 17195, 17200
 EE 440 Integrated Circuit Fabrication, Fall 2012, # 16640, 16645, 16650, 16665
 EE 363M Introduction to Microwaves, Spring 2013, # 16605
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2013, # 17425, 17430, 17435, 17440
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2013, # 16790, 16795, 16800, 16805
 EE 396K-24 Microwave Devices. Spring 2014, #17440
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2014, #17525, 17530, 17535, 17540
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2014, #16960, 16965, 16970, 16975
 EE 363M Microwave and Radio Frequency Engineering, Spring 2015, #16355
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2015, #16965, 16970, 16975
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2015, #16480, 16485, 16490
 EE 363M Microwave and Radio Frequency Engineering, Spring 2016, #16550
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2016
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2016
 EE 396K 26-Microelectromechanical Systems, Spring 2017
 EE 363M Microwave and Radio Frequency Engineering, Spring 2018, #15890
 EE 363M Microwave and Radio Frequency Engineering, Spring 2019, #16625
 EE 363M Microwave and Radio Frequency Engineering, Spring 2020, #16695

Continuing Education Courses Taught

"Microelectronics Fabrication - Chemical Aspects," with Isaac Trachtenberg,
 Continuing Engineering Studies, College of Engineering, The University of
 Texas at Austin, June 1-4, 1987.
 "Integrated Circuit Process & Design," with M. R. Mercer, Motorola short course,
 Continuing Engineering Studies, College of Engineering, The University of

Texas at Austin:

- Aug.-Sept., 1987
- Nov.-Dec., 1987
- Nov.-Dec., 1988
- March-April, 1989
- Aug.-Sept., 1989
- Nov.-Dec., 1989
- Feb.-March, 1990
- April, 1990
- Aug., 1990

"Integrated Circuit Processing and Design," with L. T. Pillage, Advanced Micro Devices short course, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin:

- Oct.-Nov., 1990
- June-July, 1991

"Microelectronics Fabrication," for the Fellows of the Senior Service College Fellowship Program, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin, yearly 1993-2003.

Cases in last five years with declaration, report, or testimony at trial or deposition: Dean P. Neikirk
As of July 2024

- April 2017 – January 2019: Baker & Hostetler LLP, on behalf of Renesas Electronics Corp., in Lone Star Silicon Innovations LLC v. Renesas Electronics Corp., et al. (E.D. TX), and associated IPRs.
- June 2018 – Nov. 2018: O’Melveny & Myers LLP on behalf of Samsung in Certain Wafer-Level Packaging Semiconductor Devices and Products Containing Same (Including Cellular Phones, Tablets, Laptops, and Notebooks) and Components Thereof, ITC No. 337-3262; Tessera Advanced Techs., Inc. v. Samsung Elecs. Co., Ltd., et al., No. 2:17-cv-00671 (E.D. Tex.); Tessera Advanced Techs., Inc. v. Samsung Elecs. Am., Inc., et al., No. 2:17-cv-07621 (D.N.J.); Invensas Corp. v. Samsung Elecs. Co., Ltd., et al., No. 2:17-cv-00670 (E.D. Tex.); Invensas Corp. v. Samsung Elecs. Co., Ltd., et al., No. 1:17-cv-01363 (D. Del.); Invensas Bonding Techs., Inc. v. Samsung Elecs. Am., Inc., et al., No. 1:17-cv-07609 (D.N.J.); FotoNation Ltd. et al. v. Samsung Elecs. Co., Ltd., et al., No. 2:17-cv-00669 (E.D. Tex.).
- October 2018 – July 2020: Lowenstein & Weatherwax LLP on behalf of VLSI Technology LLC in connection with inter partes review proceedings.
- October 2018 – September 2023: Irell & Manella LLP on behalf of VLSI Technology LLC, in VLSI Technology LLC v. Intel Corp., Case No. 1:18-cv-00966-CFC-CJB, as well as in Northern District of California captioned VLSI Technology LLC v. Intel Corp., Case No. 5:17-cv-05671-BLF and related IPRs.
- March 2019 – October 2019: Alston & Bird LLP, on behalf of Cellco Partnership d/b/a Verizon Wireless in FRACTUS, S.A., Plaintiff, v. AT&T MOBILITY LLC, Defendant. SPRINT COMMUNICATIONS COMPANY, L.P., ET AL., Defendants. T-MOBILE US, INC. ET AL., Defendants. VERIZON COMMUNICATIONS INC. ET AL., Defendants.
- Dec. 2018 - Feb. 2020: Fish & Richardson P.C., on behalf of Wasica Finance GMBH and Bluearc Finance AG in WASICA FINANCE GMBH and BLUEARC FINANCE AG, Plaintiffs, v. SCHRADER INTERNATIONAL, INC. and SCHRADER-BRIDGEPORT INTERNATIONAL, INC., Defendants, C.A. No. 13-1353-LPS.
- July 2019 – November 2019: Weil, Gotshal & Manges LLP (“Weil”), on behalf of Bio-Rad Laboratories, Inc., in Agilent Technologies, Inc. v. Bio-Rad Laboratories, Inc., and related IPRs.
- August 2019 – July 2020: Kirkland & Ellis LLP, on behalf of Samsung, in Greenthread, LLC v. Samsung Electronics Co., Ltd., et al., UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS MARSHALL DIVISION Case No. 2:19-CV-0147-JRG.

- February 2020 – December 2021: Weil, Gotshal & Manges LLP (“Weil”), on behalf of Pacific Biosciences, Inc., in Personal Genomics Taiwan, Inc. v. Pacific Biosciences of California, Inc. before the United States District Court for the District of Delaware, C.A. No. 19-cv-1810-LPS, and related IPRs.
- March 2020 – September 2020: Fish & Richardson, on behalf of Samsung, in Bell Northern Research, LLC v. Samsung Electronics Co., Ltd., et al., USDC-EDTEX, Case No. 2:19-cv-00286-JRG.
- November 2020- May 2021: Kirkland & Ellis LLP on behalf of Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively “Samsung”) in Pictos Technologies v. Samsung USITC Inv. No. 337-TA-1231.
- February 2021 – November 2021: O’Melveny & Myers, on behalf of Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Display Co., Ltd., in Samsung Display Co., Ltd. (collectively “Samsung”), in Certain Active Matrix OLED Display Devices And Components Thereof, 337-TA-1243 and Solas OLED Ltd. v. Samsung Electronics Co., Ltd. et al, 2:20-cv-00307-JRG (E.D. Tex.),
- November 2019 – present: Ropes & Gray LLP, on behalf of Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc., in Collect LLC v. Samsung Electronics Co., Ltd., et al., USDC-COL Civil Action No. 1:19-cv-00438-CMA-MEH
- February 2020 – October 2021: Weil, Gotshal & Manges LLP (“Weil”), on behalf of Pacific Biosciences, Inc., in Personal Genomics Taiwan, Inc. v. Pacific Biosciences of California, Inc. before the United States District Court for the District of Delaware, C.A. No. 19-cv-1810-LPS, and related IPRs.
- May 2020 – June 2021: Sidley Austin LLP, on behalf of Renesas Electronics America Inc., in Bell Semiconductor, LLC v. Renesas Electronics Corporation, Renesas Electronics America Inc., 6-19-cv-02196 (MDFL).
- March 2020 – July 2021: Haltom & Doan, on behalf of Hewlett Packard Enterprise, in Network-I Technologies, Inc. v. Hewlett-Packard Company and Hewlett Packard Enterprise Company, United States District Court of the Eastern District of Texas, Tyler Division, Civil Action No. 6: 13-cv-072-RWS.
- July 2021 – present: DLA Piper LLP on behalf of Home Depot, in Lynk Labs, Inc., Plaintiff, v. Home Depot USA, Inc., The Home Depot Inc., and Home Depot Product Authority, LLC, Defendants, Case No. 6:21-cv-00097-ADA, and related IPRs.
- September 2021 – May 2022: Ropes & Gray LLP, on behalf of LG Electronics, Inc. (“LGE”) in ParkerVision Inc. v. LG Electronics United States District Court of the Western District of Texas 6:21-cv-00520.

- October 2021 – April 2022: Sidley Austin LLP, on behalf of Canadian Solar in the ITC action entitled Certain Silicon Photovoltaic Cells and Modules with Nanostructures, and Products Containing The Same, Inv. No. 337-TA-1271.
- October 2021 – February 2022: Willkie Farr & Gallagher on behalf of Lenovo *inter partes* review (“IPR”) of patents asserted in the dispute with Bell Northern Research, LLC (“BNR”), currently pending as *Bell Northern Research, LLC v. Lenovo Group, Ltd., Lenovo (United States), Inc. and Motorola Mobility, LLC*, No. 6:21-cv-00847 (W.D. Tex.).
- February 2022 – October 2022: DLA Piper LLP, on behalf of Lenovo (United States) Inc., Lenovo Holding Company, Inc., and Motorola Mobility LLC, in Fundamental Innovations Systems International LLC v. Lenovo and Motorola Mobility, Civil Action No. 20-cv-551-CFC-CJB (US District Court for the District of Delaware)
- January 2022 – October 2022: Ratner Prestia, on behalf of Bayerische Motoren Werke AG and BMW of North America, LLC (“BMW”), Daimler AG and Mercedes-Benz USA, LLC (“Mercedes”), General Motors LLC (“General Motors”), Nissan Motor Co., Ltd. and Nissan North America, Inc. (“Nissan”); Tesla, Inc. and Tesla Motors TX, Inc. (“Tesla”), Toyota Motor Corp. and Toyota Motor North America, Inc. (“Toyota”); Volkswagen AG and Volkswagen Group of America, Inc. (“VW”), and ADC Automotive Distance Control Systems GmbH, Continental AG, and Conti Temic microelectronic GmbH (“Conti”), collectively, the “Defendants” in *Arigna Technology Limited v. Volkswagen AG et al* Case No. 2:21-cv-00054-JRG (E.D. Tex.).
- March 2022 – December 2022: Alston & Bird LLP on behalf of Ericsson AB, Telefonaktiebolaget LM Ericsson, and Ericsson Inc., in ITC action entitled Certain Cellular Base Station Communication Equipment, Components Thereof, and Products Containing Same, Inv. No. 337-TA-1302.
- December 2022 – June 2023: Goodwin Proctor LLP on behalf of Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung SDS Co., Ltd., Samsung SDS America, Inc., Coates US Inc., and Coates Signco Pty Ltd., in ITC action entitled - Certain Outdoor and Semi-Outdoor Electronic Displays, Investigation ITC Inv. No. 337-TA-1331,
- April 2020 – August 2023: Irell & Manella LLP on behalf of VLSI Technology LLC, in litigation in the Northern District of California captioned VLSI Technology LLC v. Intel Corp., Case No. 5:17-cv-05671-BLF.
- November 2022 – November 2023: Sidley Austin LLP on behalf of STMicroelectronics, in litigation entitled The Trustees of Purdue University v. STMicroelectronics, Inc. et al., Case No. 6:21-cv-727-ADA (W.D. Tex.).
- February 2023 – present: Dickinson Wright on behalf of Force MOS Technology , in Force MOS Technology v. Asustek Computer, Case No. 2:22-CV-0460-JRG, (E.D. Tex).

- May 2023 – February 2024: Fish & Richardson P.C. on behalf of BOE Technology Group Co., Ltd. and Beijing BOE Display Technology Co., Ltd. and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd., in connection with Element Capital Commercial Company PTE. Ltd. v. BOE Technology Group Co., Ltd.; Beijing BOE Display Technology Co., Ltd; and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd., 2:22-cv-00118-JRG (E.D. Tex.).