Polysilicon TFT Technology for Active Matrix OLED Displays

Mark Stewart, Robert S. Howell, Leo Pires, and Miltiadis K. Hatalis

***Abstract*—The integration of active matrix polysilicon TFT technology with organic light emitting diode (OLED) displays has been investigated with the goal of producing displays of uniform brightness. This work identifies and addresses several process integration issues unique to this type of display which are important in achieving bright and uniform displays. Rapid thermal processing (RTP) has been incorporated to achieve uniform polysilicon microstructure, along with silicides to reduce parasitic source and drain series resistance. Using these processes, TFT drain current nonuniformity has been reduced below 5% for 90% of the devices. This work also introduces transition metals to produce low resistance contacts to indium-tin-oxide (ITO) and to eliminate hillock formation in the aluminum metallization. These processes, along with spin on glasses for planarization, have been used to produce functional active matrix arrays for OLED displays. The final array pixel performance is also presented.**

***Index Terms*—Hillocks, nickel silicide, organic light emitting diode displays, polysilicon, rapid thermal processing.**

I. Introduction

A variety of technologies are currently in competition for a share of the flat panel display market. Currently, the dominant technology is the liquid crystal display (LCD), which operates by modulating light generated by a back-light. A new emissive technology, known as organic light emitting diode displays (OLED displays), recently has shown promise for high luminous efficiency (12 Lum/W), low voltage $(< 10\ \mathrm{V})$ and large viewing angle displays [1]. In these displays, current is passed through a thin multilayer organic material where it is converted into light. One of the layers is an electron transporting material while the other is a hole transporting material. At the junction between the two is a layer optimized for luminous recombination where the carriers recombine and the excess energy is released as light. The wavelength of the light can vary depending on the dopant species used in this light-emitting layer [1], [2]. The organic layers are sandwiched between a hole-injecting electrode consisting of a large work function material and an electron-injecting electrode consisting of a small work function material.

Since the most common electron injecting materials (Al-Li, MgAg) are opaque to visible light, the light must exit the structure through the hole injecting material. Therefore the hole injecting material must not only have a large work function, but must also be transparent to visible light. The most commonly used material is indium-tin-oxide (ITO) and this was chosen for this work.

Due to the nature of the light emission process, the brightness of the OLED material is proportional to the amount of current passing through it. Because of this, an active matrix pixel array needs to deliver uniform currents to the OLED material in order to create uniform light. This is different from active matrix liquid crystal display (AMLCD) array technologies which only need to deliver voltages, not currents, to switch the liquid crystal material. Therefore, different processing issues will arise for the development of active matrix OLED (AM-OLED) displays compared with AMLCD display technologies. This paper discusses these issues and presents a fabrication process for AM-OLED display arrays. First, the design strategy will be discussed and a justification for the need of polysilicon TFTs will be presented.

II. OLED Display Array Design Approach

OLED displays have been designed in both passive matrix and active matrix modes. In the passive matrix mode, each pixel consists of an overlap between two conductors, the address line and the data line, with the OLED material in between. No transistors are required. To turn on a pixel, a certain voltage needs to be dropped across the OLED material. The address line delivers a fraction of this voltage, and the data line provides the remainder. A pixel receiving only part of the full voltage will be off. However, this approach limits the contrast and restricts the format of the display to smaller pixel counts. In addition, this approach requires patterning of both the hole injecting and electron injecting electrodes, which is difficult if MgAg is used as the electron-injecting electrode.

Using an active matrix design approach can solve the image contrast and MgAg electrode pattering problems. In the active matrix approach, a transistor is placed at each pixel to separate the effect of the data line voltage and the address line voltage on the voltage across the OLED material. A common MgAg electrode is used to eliminate the need to pattern the electron injecting electrode. Within AM-OLED designs, a variety of pixel architectures have been proposed [3]. Different pixel architectures may contain different numbers of transistors per pixel. The simplest design uses one transistor per pixel. A single transistor design approach has the advantage of increased contrast compared to a passive matrix design, and will have a higher yield than designs containing more than 1 TFT per pixel. However,

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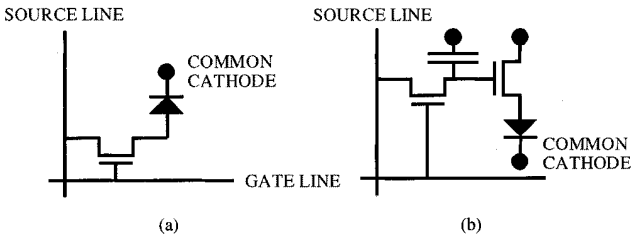

Fig. 1. Pixel design schematics showing (a) the single TFT per pixel design, and (b) the two TFT per pixel design.

in this approach each pixel is only pulsed ON for a fraction [1/(number of gate lines)] of the frame time. This requires the peak OLED current to be much higher than the average current, which leads to faster degradation of the OLED material.

To avoid the high current pulses native to the single TFT design, designs involving two transistors per pixel have been proposed which have pixel memory [3]. This memory allows the pixel to deliver a small current throughout the entire frame period. Though the average current through the OLED material is the same, the peak current is greatly reduced which leads to increased brightness and OLED material lifetime. Other architectures have also been proposed to improve brightness uniformity by correcting for variations in the transistor threshold voltage ($\geq$ 4 transistors per pixel) [4]. Our work attempts to reduce brightness variations across the substrate through processing improvements rather than circuit design corrections. Both the one and two transistor-per-pixel designs are considered in this work. Fig. 1 shows a schematic of these architectures.

The next design issue is to determine which technology should be used to fabricate the transistor array. The most commonly used technologies for AMLCDs are amorphous silicon and polycrystalline-silicon (polysilicon). Both of these materials are compatible with large area glass substrate processes, which is necessary to fabricate displays at reasonable cost. Polysilicon TFT technology was chosen for its higher mobility and greater stability compared with amorphous TFTs as well as for its ability to provide p-channel devices. The higher mobility is needed for the single TFT per pixel design because the pixels only emit light for a small fraction of the frame time and therefore large currents are required. A calculation of the required mobility is as follows.

The average current necessary to produce a bright display ($100\,\mathrm{cd/m^2}$) is approximately $10\,\mathrm{mA/cm^2}$ [5]. If we assume a pixel size of $50\,\mu\mathrm{m} \times 50\,\mu\mathrm{m}$, a steady current of $0.25\,\mu\mathrm{A}$ is necessary. Since each pixel emits light only when it is activated by its address line, each address line is ON for only a small fraction [1/(# address lines)] of the frame time. Thus, in order to maintain an average dc current of $0.25\,\mu\mathrm{A}$, assuming 480 address lines, the maximum transistor current requirement ($I_{\max}$) is $0.25\,\mu\mathrm{A} \times 480 = 240\,\mu\mathrm{A}$. Assuming a TFT operating in saturation, the required mobility can be calculated according to

$$\mu = \frac{I_{\max}}{\frac{W}{2L} C_{ox} (V_{gs} - V_{th})^2_{\max}}. \tag{1}$$

To achieve the proper current levels using small device geometry ($W/L = 2$), and a gate oxide thickness of 50 nm, a mobility greater than $34\,\mathrm{cm^2/V\text{-}s}$ is required. Since a mobility of $34\,\mathrm{cm^2/V\text{-}s}$ is required, amorphous silicon cannot be used because it has mobilities less than $1\,\mathrm{cm^2/V\text{-}s}$ and therefore cannot deliver high enough currents with compact device geometry. Polysilicon based transistors have mobilities more than an order of magnitude greater than amorphous silicon and therefore were selected for this work. It is important to note that the pixel designs using two transistors per pixel require significantly lower drive currents. As a result, the mobility requirement is much less and, strictly from a drive current perspective, amorphous silicon TFTs may be adequate.

However, p-channel devices are desired to prevent variations in the OLED material turn on voltage from leading to current variations in the OLED material. To accomplish this, a p-type transistor operating in the saturation mode is used to drive current into the OLED material because both the gate and source voltages of a p-channel transistor can be delivered directly via the gate and data lines. However, if an n-channel TFT were used only the gate voltage could be written directly to the pixel, the source voltage would depend upon the voltage across the OLED material. Since amorphous silicon technology can not produce adequate p-channel TFTs, it may not be a good candidate for AM-OLEDs, even for the two transistor per pixel designs where much smaller drive currents are required.

Next, this paper discusses the processing issues in matching polysilicon TFT technology with active matrix OLED displays.

III. Display Processing

This section describes a fabrication process used to realize both pixel designs. In both architectures (one transistor per pixel and two transistors per pixel), the current passes out of a transistor and into the organic light emitting diode structure. Since the transistor controls the current through the OLED material, the uniformity of the transistor threshold voltage, carrier mobility, and series resistance is crucial to the final performance of the display array. This is because, to first order, the saturation TFT current can be written as shown in (2) where R_{s} represents a sum of both the series and contact resistance, μ_{p} represents the hole mobility, and Vt represents the threshold voltage.

$$Ids = \frac{\frac{W}{2L} \mu_p C_{ox} (Vgs - Vt)^2}{1 + \frac{W}{L} \mu_p C_{ox} R_s (Vgs - Vt)}. \tag{2}$$

It is evident from (2) that variations in the threshold voltage, carrier mobility, or series resistance will directly impact the uniformity of the TFT current and consequently, the brightness of the display. In this work, a variety of steps were implemented to reduce the series resistance and improve the uniformity of the pixel electrical characteristics. The carrier mobility and threshold voltage variations were reduced through the use of rapid thermal processing (RTP) for polysilicon crystallization to achieve uniform polysilicon microstructure. A silicidation process was developed to eliminate TFT series resistance and a low resistance contact scheme was developed to connect the ITO to the drain of the TFT. Finally, a planarization scheme based on spin on glasses (SOGs) was used in order to provide a smooth and uniform surface prior to OLED material deposition. These steps are described below along with a process used to fabricate the display arrays.

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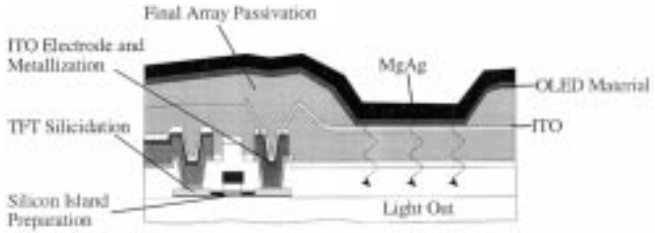

Fig. 2. AM-OLED array process overview.

The fabrication process is divided into four parts: a) silicon island preparation, b) TFT silicidation, c) ITO electrode and metallization, and d) final array passivation. A cross section of the process indicating these four areas is shown in Fig. 2.

A. Silicon Island Preparation

The silicon films were deposited by pyrolysis of disilane in a low pressure chemical vapor deposition reactor at a temperature of 470 °C or 500 °C. The films were then crystallized into the solid phase using rapid thermal processing (RTP). The RTP process was chosen over alternative crystallization methods, such as excimer laser annealing (ELA), because of its high uniformity and high throughput [6]. The uniformity of heating during crystallization is important to create uniform polysilicon microstructure across the wafer. In the ELA process, due to the narrow localization of the light beam and the melting of the silicon film, significant microstructural variations can result. In contrast, the wide profile of the RTP lamp and the solid phase crystallization nature of the process results in uniform polysilicon microstructure. The RTP throughput is determined by the speed with which the wafers are passed underneath the heating lamps. For this work, scan speeds of 5 mm/s or greater were used. The RTP crystallization temperatures were in the range of 677 °C to 720 °C. The thickness of the polysilicon islands was 50 nm.

After the amorphous silicon films were crystallized and patterned, a 100 nm gate oxide and a 100 nm amorphous silicon gate were then deposited by plasma enhanced chemical vapor deposition (PECVD). The wafers were then annealed in a furnace in a nitrogen ambient at 800 °C for 30 min to crystallize the amorphous silicon gate, and then further annealed at 1000 °C to improve the properties of the polysilicon islands. The gate electrode was then patterned and the gate, source and drain were doped either with Phosphorus or Boron to a dose of 2×10^{15} cm^{-2}. The dopants were activated at 800 °C in a furnace, though again RTP could be used for dopant activation.

B. TFT Silicidation

Nickel silicides were formed on the source, drain and gate regions to reduce the series resistance of the TFT. The gate region directly on top of the channel was not silicided because of the use of an oxide mask. This mask was necessary to preserve a p+ region in contact with the channel to maintain a blocking junction and thus proper device operation. The silicidation step becomes increasingly important as polysilicon islands are reduced in thickness, because thinner islands increase the series resistance of the TFT. It is desirable to reduce the polysilicon island thickness to improve the TFT performance and to increase manufacturing throughput. Our previous work has shown that the use of silicides can enable ultrathin $(< 30\ \mathrm{nm})$ island TFTs to be made without significant reduction in the ON current due to the island series resistance [7]. Furthermore, since the silicidation process reduces significantly the source and drain parasitic series resistance and its associated variability, the uniformity of the TFT is expected to improve.

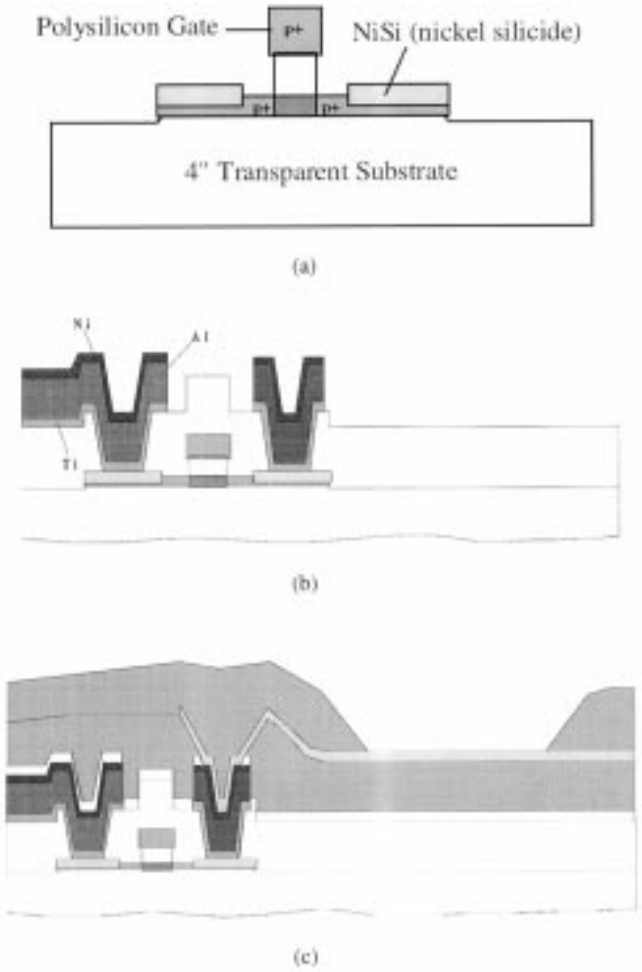

Fig. 3. Cross sections of the array pixel at three different stages in processing: (a) after TFT formation, (b) after metallization, and (c) the final pixel cross section.

The silicides were formed by sputter depositing Ni onto the wafers followed by an in-situ vacuum anneal at 400 °C for 10 min. The silicided source and drain regions had a sheet resistance of 20 $\Omega/\square$, whereas the nonsilicided regions had a sheet resistance of 800 $\Omega/\square$. Since the polysilicon gate lines were also silicided, the gate line resistance was improved by a factor of 40 compared with a nonsilicided polysilicon gate. Fig. 3(a) shows a pixel cross section after the silicide stage in the array fabrication process.

It is important to note that NiSi is resistant to both reactive ion etching and wet etching of silicon dioxide [8], and thus it can be used as an effective etching stop for the opening of the source and drain contact windows. Doped silicon is not as resistant to dry etching as nickel silicide. This is another advantage of using the nickel silicided source and drain process.

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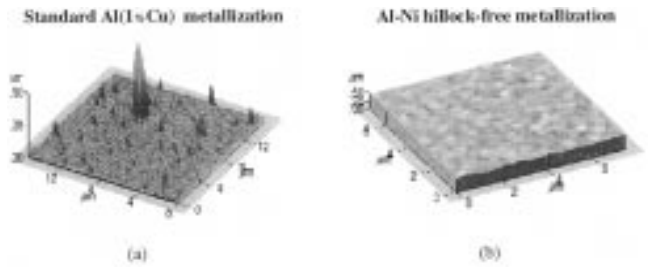

Fig. 4. Comparison of AFM pictures of (a) an Al film and (b) an Al — Ni film after both films were heated at 500 °C. It is clear that the Al-Ni film resists the formation of hillocks.

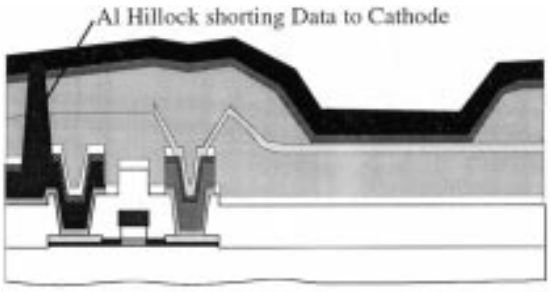

Fig. 5. Illustration of how Al hillock can short a data line to the common cathode of the AM-OLED structure.

C. ITO Electrode Formation and Metallization

After the transistor formation, 300 nm of PECVD passivation oxide was deposited to cover the islands and gates and to prevent shorts between gate and data lines. Contact holes were then opened to the gate and island regions using wet etching followed by deposition of the data metals.

The data metallization consisted of a three-layer stack to prevent the formation of hillocks. The layers were 50 nm of Ti, 200 nm Al, and 50 nm of Ni. A cross section of the pixel at this stage is shown in Fig. 3(b). It was found that the Ti alone could not prevent the formation of hillocks during hydrogenation, but that the addition of an extra layer of nickel on top of the aluminum prevented the formation of hillocks [9]. Fig. 4 compares atomic force microscope (AFM) images of an Al film with a Ni capping layer with an Al film with no capping layer after both films have been annealed at 500 °C. It is clear that the nickel layer prevents the formation of hillocks even at temperatures far greater than those required for AM-OLED processing. This is an important consideration in OLED displays because a hillock can cause a short between the data line and the common cathode of the OLED material. Fig. 5 shows an example of OLED display damage that may occur from a hillock. After metallization, the wafers were plasma hydrogenated for 1 h at 300 °C.

The data metals were then covered with a double layer of PECVD oxide and spin on glass (SOG). The SOG was cured on a hotplate at 300 °C. A higher cure temperature was not used because it may have instigated out-diffusion of hydrogen and reduced the performance of the TFTs. The combination of these two dielectrics provided excellent protection of the metals from future corrosive etches as well as a smooth, well-planarized surface for the deposition of the ITO electrode. It is important that the ITO electrode resides on a well planarized surface so that the surface of the ITO is free of any asperites that may cause nonuniform current flow across the OLED material. A contact hole was then opened in the SOG and oxide so that the ITO could connect to the drain of the TFT. The ITO was sputter deposited at 200 °C.

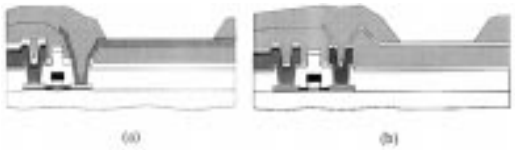

Fig. 6. Two different processes are shown to contact the ITO to the silicided polysilicon island; (a) the ITO contacts the silicide directly, and (b) the ITO contacts a data metal plug which then contacts the silicide.

Two different approaches were investigated to contact the ITO electrode to the silicided polysilicon island. In one approach, the ITO contacted the silicided island directly. In another approach, the ITO contacted a data metal plug, which in turn contacted the silicided island. Fig. 6 shows a comparison of these two contact approaches. Both processes were used in order to investigate which process could provide more uniform pixel characteristics.

In the metal plug approach, the Ni capping layer in the Ti-Al-Ni stack is necessary not just to prevent hillock formation, but also to ensure a good contact of the ITO to the metals. Previous work has demonstrated that the Al-ITO forms an interfacial oxide and the contact is not ohmic. However, adding a Ni capping layer prevents the formation of this oxide and the Al-Ni-ITO forms a low resistance, ohmic contact [10].

D. Final Array Passivation

After the ITO patterning, a second SOG dielectric was spun onto the wafer and cured on a hot plate at 275 °C. This cure temperature was chosen to be less than the cure temperature of the previous SOG layer in order to prevent stressing and possibly cracking the previous SOG film. A contact hole was then patterned and etched using wet chemistry to open an area where the OLED material would contact the ITO. This window defines the area from which light will be emitted. The use of wet chemistry is important at this stage in order to provide a gradual slope in the etched passivation oxide around the OLED window formed on top of the ITO. A gradual slope is important in order to achieve good step coverage of the OLED material.

Also, in order to guarantee a smooth surface for the OLED material, this final cut to the ITO was placed only over the area of the ITO that has minimal topological variations underneath it. The SOG underneath the ITO will ensure that the ITO is smooth except where this SOG has been etched for the ITO-data metal contact, while the SOG on top of the ITO will planarize the region where the ITO contacts the metal plug. Thus, a smooth topology is provided for the OLED material. A smooth surface prior to OLED material deposition will minimize unwanted OLED material thickness variations and therefore improve the brightness uniformity of the display. Fig. 3(c) shows a final cross section of the pixel prior to OLED material deposition.

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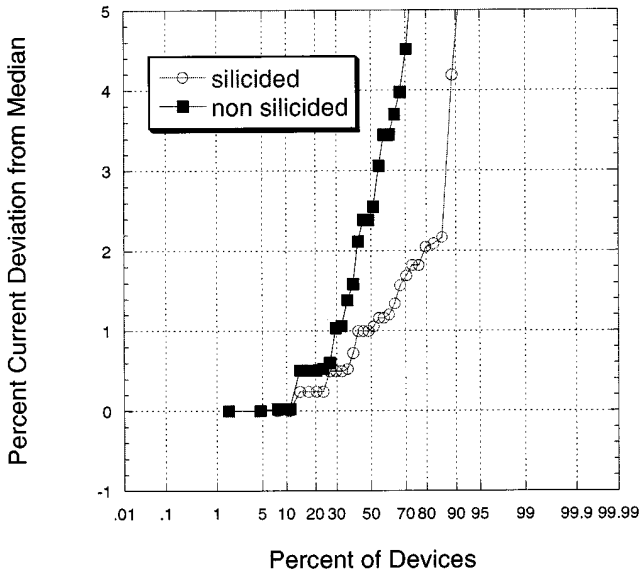

Fig. 7. Cumulative probability plot of TFT drain currents falling within a percentage of the median current. It can be seen that the silicided devices are more uniform.

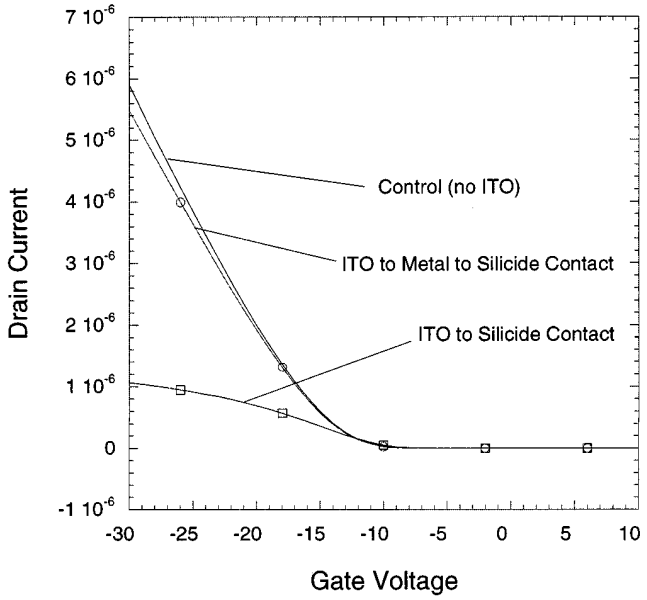

Fig. 8. TFT transfer characteristics comparing a TFT using an ITO-metal-silicide contact scheme with a TFT using an ITO-silicide contact scheme.

IV. Array Performance

The four major process improvements discussed above were all important to the final array performance. The RTP process achieved uniform polysilicon characteristics. The silicidation and ITO contact step reduced parasitic series resistance and therefore further improved uniformity. The metallization was hillock free and prevented shorts to the OLED common cathode. Finally, the passivation and planarization produced a viable, smooth ITO surface prior to OLED material deposition.

To determine the uniformity of polysilicon TFTs crystallized using the RTP process, data was collected from wafers processed by RTP. These devices were silicided and completed through patterning of the metallization layer. The maximum process temperature of these devices was kept below 700 °C. The local uniformity was determined by measuring the standard deviation of threshold voltage over the area of one die ($0.25\ \text{cm}^2$). The global wafer uniformity was determined by evaluating the data over an area of ($10\ \text{cm}^2$. The local deviation was 65 mV for n-channel TFTs and 140 mV for p-channel TFTs. The global deviation was 100 mV for n-channel TFTs and 150 mV for p-channel TFTs. This data confirms that the RTP crystallization process leads to highly uniform polysilicon TFTs.

The silicidation process also was found to improve the uniformity of the TFTs. Fig. 7 shows a cumulative probability plot comparing TFTs fabricated with silicides to TFTs fabricated without silicides. For a large group of silicided or nonsilicided devices, the value of V_{GS} was determined that achieved a median current level of $20\ \mu\text{A}$, at $V_{\text{DS}} = 1\ \text{V}$. Then, the individual devices were measured to determine the exact drain current of each TFT at this fixed V_{GS} value. The percent deviation from the median current (the target current) was then measured for each TFT. This graph plots the deviation in the targeted current as a function of the percentage of devices. This method takes into account both mobility and threshold voltage nonuniformity and therefore best imitates the nonuniformity in TFT pixel current.

For the graph, it is clear that the silicided devices are more uniform. For example, 80% of the silicided devices have currents that vary within 2% of each other, whereas the nonsilicided devices have currents with variation greater than 5%. This increase in uniformity is attributed to a reduction in the variable series resistance.

In addition to TFT silicidation, it was also found that the method of contacting the ITO to the silicon island was critical in determining the parasitic resistance of the pixel. The series resistance resulting from connecting the ITO directly to the silicided island was intolerably high and significantly deteriorated the pixel drive current. This is because when the ITO was in direct contact with the nickel silicide an interfacial oxide was formed. This contact then was no longer ohmic in nature. However, when adding the metal plug between the ITO and the NiSi, the contact was ohmic and parasitic resistance had only a minor effect on the pixel performance. The contact resistance using the ITO-metal-silicide contact scheme was $480\ \mu\Omega\text{-cm}^2$ at a bias of 1 V. In contrast, the contact resistance of the ITO-silicide scheme was $33\ \text{m}\Omega\text{- cm}^2$, even at a bias of 10 V.

To illustrate the advantages of this new contact method, Fig. 8 shows the linear transfer characteristics of the completed pixels using the ITO-metal-silicide contact method as well as the ITO-silicide contact method. A control TFT is also shown which has no ITO connection, but rather the silicide was probed directly. It can be seen that pixel using the ITO-silicide contact suffered greatly due the contact resistance, but that the pixel using the ITO-metal-silicide contact does not have this problem and achieves characteristics similar to the control TFT.

VGA size arrays with a 4-cm diagonal were fabricated using the process described above. Fig. 9 shows a microscope photograph of a completed pixel having the single TFT per pixel design. The pixel size is $50\ \mu\text{m}$ by $50\ \mu\text{m}$. Fig. 10 shows a transmission mode photograph of a pixel having the two TFT per pixel design; its pixel size is $100\ \mu\text{m}$ by $100\ \mu\text{m}$.

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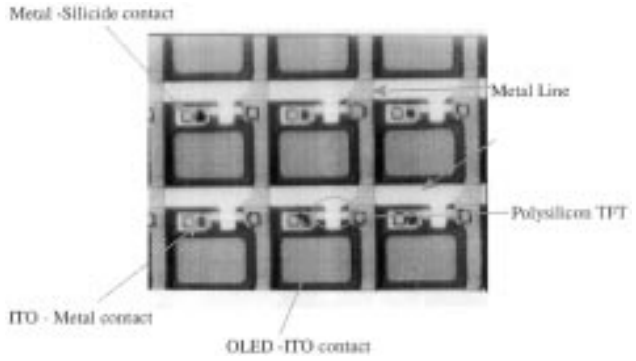

Fig. 9. Photograph of a completed $50\ \mu$m square single TFT pixel (top view).

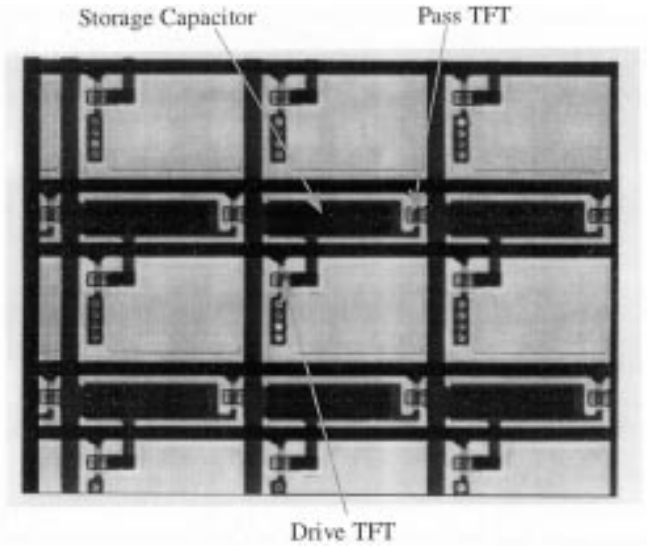

Fig. 10. Photograph of completed $100\ \mu$m square pixel having the 2-TFT design. The pass TFT, storage capacitor, and drive TFT are indicated.

The pixel functionality was tested by probing the ITO pad and applying test voltages to the periphery of the array. Pixel TFT characteristics were measured for n channel and p channel wafers and for wafers with both types of ITO to island contacts. Fig. 11 shows the transfer characteristics at $V_{\rm DS} = -1$ V of a p channel TFT in the single TFT pixel structure. The p channel pixel TFT has a mobility of $21\ \mathrm{cm}^2/\mathrm{V\text{-}s}$ and the n channel pixel TFT has a mobility of $46\ \mathrm{cm}^2/\mathrm{V\text{-}s}$. These characteristics were measured for the case where the ITO contacts the NiSi via a metal plug. After the completion of the arrays, the OLED material was deposited and the displays were tested. An average brightness of $101\ \mathrm{cd}/\mathrm{m}^2$ was obtained at a frame rate of 60 Hz [11]. The operating AM-OLED display testifies to the success of the active matrix array panel and the fabrication approach discussed in this paper.

V. Conclusions

A process to fabricate polysilicon TFT active matrix OLED display arrays has been described. In order to create a display with uniform brightness, a variety of steps have been introduced to reduce nonuniformity that may arise through processing. To achieve uniform transistor threshold voltage and carrier mobility, a solid phase polysilicon crystallization by rapid thermal processing (RTP) was used. TFT threshold voltage variation less than 200 mV was achieved using the RTP crystallization process. To reduce the TFT series resistance, silicides were incorporated onto the source and drain regions of the TFT and the silicides were found to significantly improve TFT current uniformity. To reduce the series resistance of the pixel, a Ti-Al-Ni metallization scheme was developed to interface the ITO and the TFT island, resulting in a good ohmic contact to the ITO. The Ti-Al-Ni metallization scheme also eliminated hillocks, which could otherwise cause catastrophic shorts in the display. Finally, spin on glasses were integrated to provide a well-planarized surface for the OLED material. The final array pixel TFT's had effective mobilities of $46\ \mathrm{cm}^2/\mathrm{V\text{-}s}$ for n channel TFT's, and $21\ \mathrm{cm}^2/\mathrm{V\text{-}s}$ for the p channel TFTs. These arrays resulted in functional VGA AM-OLED displays with brightness of $101\ \mathrm{cd}/\mathrm{m}^2$.

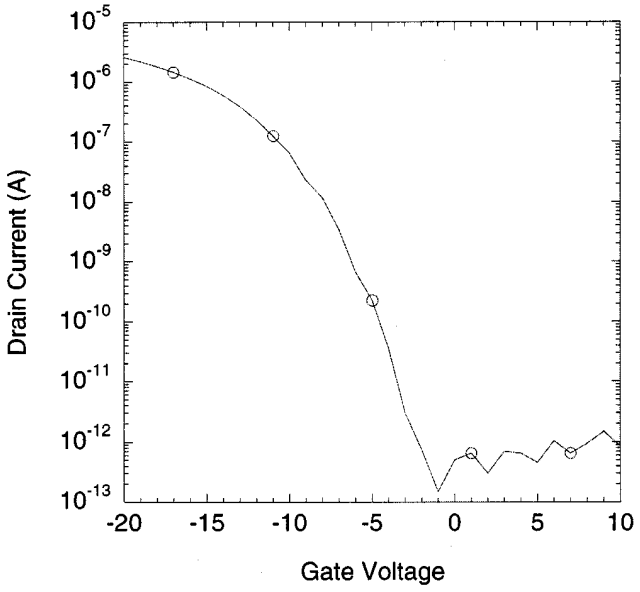

Fig. 11. P-channel pixel TFT transfer characteristics. $W/L = 4\ \mu\mathrm{m}/8\ \mu\mathrm{m}$, $V_{\rm DS} = -1$ V.

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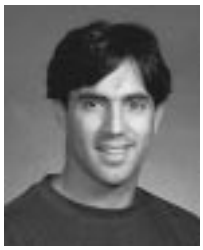

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