

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

OPTRONIC SCIENCES LLC,
Patent Owner.

IPR2024-01132
Patent 7,586,121 B2

Before THU A. DANG, BENJAMIN D. M. WOOD, and
BRIAN J. McNAMARA, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

BOE Technology Group Co. LTD. (“Petitioner”) filed a petition, Paper 1 (“Petition” or “Pet.”), to institute an *inter partes* review (“IPR”) of claims 1–7 (the “challenged claims”) of U.S. Patent No. 7,586,121 B2 (“the ’121 patent”). 35 U.S.C. § 311. Optronic Sciences LLC (“Patent Owner”) filed a Preliminary Response, Paper 7 (“Prelim. Resp.”), contending that it “does not believe the Petition merits institution.” Prelim. Resp. 1. The Patent Owner Preliminary Response does not include any substantive analysis of Petitioner’s challenges. *Id.* We have jurisdiction under 35 U.S.C. § 6. 35 U.S.C. § 314 provides that an *inter partes* review may not be instituted unless the information presented in the Petition “shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

A decision to institute under § 314 may not institute on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018). In addition, per Board practice, if the Board institutes trial, it will institute “on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” *See* 37 C.F.R. § 42.108(a).

Having considered the arguments and the associated evidence presented in the Petition and the Preliminary Response, for the reasons described below, we institute *inter partes* review.

II. REAL PARTIES IN INTEREST

The Petition identifies Petitioner (BOE Technology Group Co., LTD) as its real party-in-interest. Pet. 55. Patent Owner identifies itself (Optronic Sciences LLC) as its real party-in-interest. Paper 4, 1; Paper 6, 1.

III. RELATED MATTERS

Petitioner and Patent Owner state that the '121 patent is asserted in the following litigation: *Optronic Sciences LLC v. BOE Technology Group Co., LTD.*, 2:23-cv-00549 (EDTX). Pet. 55; Paper 4, 1; Paper 6, 1.

Patent Owner identifies the following *inter partes* review proceedings between the parties as concerning other patents that may affect or be affected by a decision in this proceeding: IPR2024-01130 (U.S. Patent No. 7,168,842), IPR2024-01131 (U.S. Patent No. 7,226,801), IPR2024-01133 (U.S. Patent No. 9,263,509), IPR2024-01134 (U.S. Patent No. 9,406,733), IPR2024-01135 (U.S. Patent No. 8,158,477).

IV. THE '121 PATENT

The '121 patent concerns storage capacitors in electroluminescent (EL) devices. Ex. 1001, 1:6–9. The '121 patent states that known EL devices typically include thin film transistors (TFTs) and light emitting diodes (LEDs) that may contain organic material and emit light when current is passed through them. *Id.* at 1:13–21. In a current or voltage driven active matrix organic light emitting diode (OLED) device or polymer light emitting diode (PLED) device, each pixel comprises a set of sub-pixels that include a switching transistor, driving transistor and a storage capacitor. *Id.* at 1:22–27. Noting that a large capacitance avoids grey scale fading, the '121 patent seeks to provide an improved storage capacitance in a limited area. *Id.* at 1:27–37.

The '121 patent discloses an EL device may include an array of pixels formed on a substrate, e.g., glass, with each pixel formed in a respective pixel area. Ex. 1001, 1:41–45, 4:36–37. Figure 1 of the '121 patent,

reproduced below, is a circuit diagram of a pixel of such an EL device. *Id.* at 3:62–64.

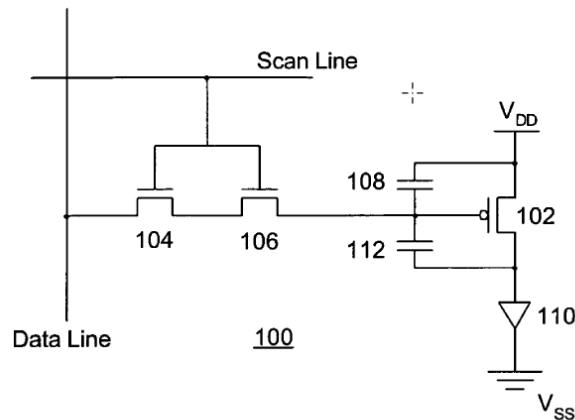


Fig. 1

Ex. 1001, Fig. 1. Transistor 102 is a p-type MOS transistor and transistors 104, 106 are n-type MOS transistors. *See id.* at 4:36–49. The anode of OLED 110 is coupled to the drain of transistor 102 and the cathode is coupled to V_{ss} , which may be ground. As capacitors 108 and 112 hold a charge when transistors 104 and 106 are turned off, in this condition they effectively act in parallel to form a storage capacitor, whose capacitance equals the sum of the individual capacitances, that maintains the gate voltage of transistor 102 for driving OLED 102. *Id.* at 4:60–5:4. By forming capacitor 112 over the same area where capacitance 108 is formed, the storage capacitance is increased without consuming additional chip area and without requiring additional masks. *Id.* at 5:5–11.

Figure 2 of the '121 patent, reproduced below, is a cross sectional view of a part of pixel 100. *Id.* at 3:65–67, 5:12–16.

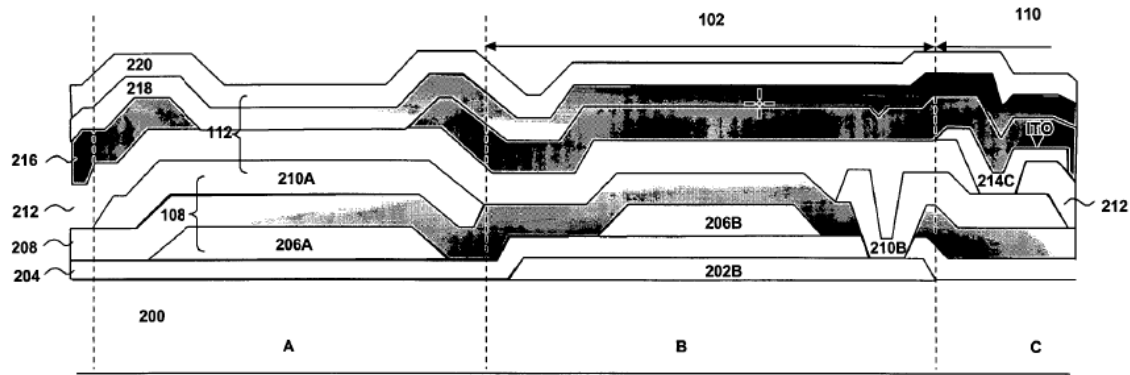


Fig. 2

Ex. 1001, Fig. 2. In Figure 2, part of pixel 100 is shown with capacitors 108, 112 formed over area A, a portion of transistor 102 formed over area B, and gate oxide layer 204 formed over all of area A, B, and C; transistors 104 and 106 are not shown. *Id.* at 5:13–21. Over area A first metal pattern 206A, interlayer dielectric (ILD) layer 208 and second metal pattern 210A collectively form capacitor 108. *Id.* at 5:47–48. Second metal pattern 210A, SiN passivation 212, organic 218, and third metal 220 collectively form capacitor 112. *Id.* at 5:48–50.¹ Over area B, polysilicon pattern 202B provides the source and drain of transistor 102 and first metal pattern 206B serves as the gate of transistor 102. *Id.* at 5:50–53. Over area C, indium tin oxide (ITO) pattern 214C, capping SiN 216, organic 218 and third metal 220 collectively form part of OLED 110. *Id.* at 5:53–55.

V. ILLUSTRATIVE CLAIM

Claim 1, reproduced below with paragraph designations used in the Petition, is illustrative of the subject matter of the '121 patent.

1. An electroluminescence (EL) device, comprising:
a substrate; and

¹ Ex. 1001, 5:50 appears to have a typographical error: “capacitor 110” should read --capacitor 112--; reference designator 110 refers to the OLED.

- a plurality of pixels formed on the substrate, each pixel being in a respective pixel area, each pixel area including at least a first area, a second area, and a third area, wherein each pixel includes:
- at least a first capacitor and a second capacitor in the first area, the first capacitor including a first conductive layer formed over a first gate oxide layer, a first dielectric layer over the first conductive layer, and a second conductive layer over the first dielectric layer, and the second capacitor including the second conductive layer, a second dielectric layer over the second conductive layer, and a third conductive layer over the second dielectric layer;
- a transistor in the second area, the transistor including a first semiconductor layer formed on the substrate, the first gate oxide layer over the first semiconductor layer, and a fourth conductive layer over the first gate oxide layer, wherein the fourth conductive layer is formed of the same conductive film as the first conductive layer, and wherein both the first conductive layer and the fourth conductive layer are directly formed on the gate oxide layer, and
- a light emitting device in the third area, the light emitting device including a fifth conductive layer, a first organic layer over the fifth conductive layer, and a sixth conductive layer over the first organic layer, wherein the sixth conductive layer is formed of the same conductive film as the third conductive layer.

VI. ASSERTED GROUNDS

Petitioner asserts that claims 1–7 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)
1–3, 5	102(e)	Anzai ²
4	103(a)	Anzai, Yamazaki ³
1–7	103(a)	Yamazaki, Anzai

² U.S. Patent No. 7,330,168 B2 (Ex. 1003).

³ U.S. Patent No. 6,992,332 B2 (Ex. 1004).

Petitioner also cites the Declaration of Dr. Dean Neikirk in Support of the Petition (Ex. 1002, Neikirk Decl.) as testimonial evidence in support of its challenges.

VII. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner describes a person of ordinary skill in the art (“POSITA” or “ordinarily skilled artisan”) at the time of the invention as having “a Bachelors’ degree in electrical engineering or a comparable field of study, plus approximately two to three years of professional experience with electronic and optoelectronic device design” and notes that “[a]dditional graduate education could substitute for professional experience, and significant experience in the field could substitute for formal education.” Pet. 5–6 (citing Ex. 1002, Neikirk Decl. ¶ 23). Patent Owner does not comment on the level of ordinary skill in the art. *See* Prelim. Resp.

The level of ordinary skill in the art usually is evidenced by the references themselves. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978). As Petitioner’s unchallenged description of an ordinarily skilled artisan appears consistent with the subject matter discussed in the references and that of the challenged claims, for purposes of this Decision we apply Petitioner’s description of a person of ordinary skill in the art.

VIII. CLAIM CONSTRUCTION

We interpret claim terms using “the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b).” 37 C.F.R. § 42.100(b) (2024). In this context, claim terms “are generally given their ordinary and customary meaning” as understood by a

person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (citations omitted) (en banc). “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Extrinsic evidence is “less significant than the intrinsic record in determining ‘the legally operative meaning of claim language.’” *Phillips*, 415 F.3d at 1317 (citations omitted).

Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). “The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Neither party has proposed a special definition or explicit construction of any claim term. Pet. 5–6, Prelim. Resp. 1. As we do not perceive a need to construe any term, we apply the plain and ordinary meaning to the claim language.

IX. ANALYSIS

A. Introduction

1. *Inter Partes* Review

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is

unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

The Patent Owner Preliminary Response states “if the Board decides that institution is warranted, Petitioner [sic] respectfully requests that the Board’s Institution Decision articulate which ground the Board believes has the highest likelihood of success so that Patent Owner can focus on addressing that ground in its Patent Owner Reply.” Prelim. Resp. 1. We limit our analysis of the asserted grounds of unpatentability and any response filed by Patent Owner to determining whether Petitioner has met its burden to establish a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. *See* 35 U.S.C. § 314(a).

2. *Anticipation*

Anticipation is a question of fact, as is the question of what a prior art reference teaches. *In re NTP, Inc.*, 654 F.3d 1279, 1297 (Fed. Cir. 2011). “A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, “a single prior art reference must expressly or inherently disclose each claim limitation”). Moreover, “[b]ecause the hallmark of anticipation is prior

invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

Whether a reference anticipates is assessed from the perspective of an ordinarily skilled artisan. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) (“[T]he dispositive question regarding anticipation [i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference’s] teaching that every claim element was disclosed in that single reference.” (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))).

Additionally, under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates. *MEHL/Biophile Int’l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (citation omitted); *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349–50 (Fed. Cir. 2002).

3. *Obviousness*

The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of “whether there was an apparent reason to combine the known elements in

the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring “articulated reasoning with some rational underpinning to support the legal conclusion of obviousness”)); see *In re Warsaw Orthopedic, Inc.*, 832 F.3d 1327, 1333 (Fed. Cir. 2016) (citing *DyStar Textilfarben GmbH & Co. Deutschland KG v. C. H. Patrick Co.*, 464 F.3d 1356, 1360 (Fed. Cir. 2006)).

An obviousness analysis “need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 550 U.S. at 418; accord *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Instead, Petitioner must articulate a reason why a person of ordinary skill in the art would have combined the prior art references. *In re NuVasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016).

A reason to combine or modify the prior art may be found explicitly or implicitly in market forces; design incentives; the “interrelated teachings of multiple patents”; “any need or problem known in the field of endeavor at the time of invention and addressed by the patent”; and the background knowledge, creativity, and common sense of the person of ordinary skill. *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1328–29 (Fed. Cir. 2009) (quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–21 (2007)).

In determining whether a claim would have been obvious in light of the prior art, when in evidence, we consider any relevant objective evidence

of non-obviousness. *See Graham*, 383 U.S. at 17. Notwithstanding what the teachings of the prior art would have suggested to one of ordinary skill in the art at the time of the invention, the totality of the evidence submitted, including objective evidence of non-obviousness, may lead to a conclusion that the challenged claims would not have been obvious to one of ordinary skill. *In re Piasecki*, 745 F.2d 1468, 1471–72 (Fed. Cir. 1984). At this stage of the proceeding Patent Owner does not present evidence of such objective considerations.

B. Petitioner’s Contentions That Claims 1–3 and 5 Are Anticipated by Anzai

1. *Anzai*

Anzai relates to an EL display device “with a storage capacitance element for holding a video signal supplied to a gate of a driving transistor.” Ex. 1003, 1:7–9. Each pixel portion includes a transistor that drives an EL element and a pixel selecting transistor that supplies a signal from the drain signal line to the gate of the driving transistor. *Id.* at 2:37–42. A storage capacitance element holds the signal supplied to the gate of the driving transistor. *Id.* at 2:37–45. The storage capacitance element includes an extension of the source of the pixel selecting transistor as a first capacitance electrode layer; a second capacitance electrode layer is disposed above the extension of the source, and a third capacitance electrode layer is connected to the source and disposed above the second capacitance electrode layer. *Id.* at 2:45–50.

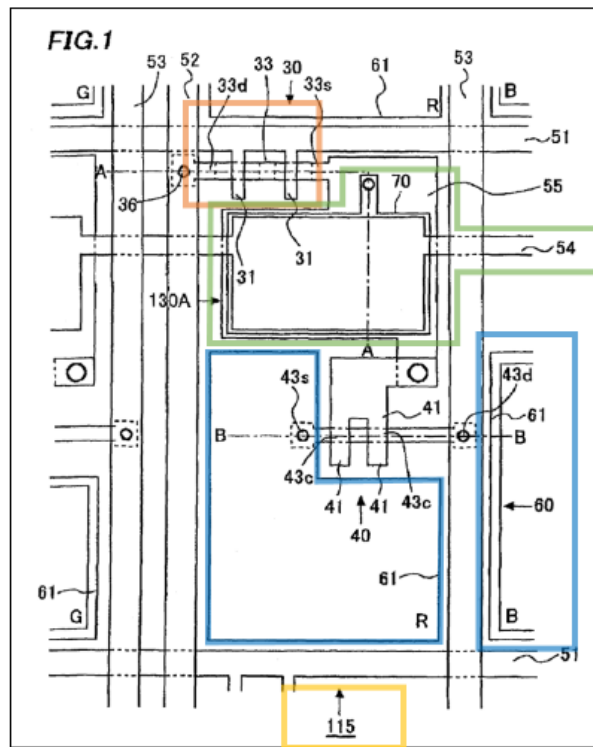
2. *Claim 1*

a) *Limitation [1.pre], [1.a], and [1.b]*

As designated by Petitioner, the preamble of claim 1 [1.pre] recites “[a]n electroluminescence (EL device),” and limitation [1.a] recites “a

substrate.” Pet. vi. Petitioner notes that Anzai is directed to an EL display device having a reduced area for forming a storage capacitor that holds the video signal supplied to a transistor to improve the quality of the EL device display by holding the video supplied to the gate of a transistor that drives an OLED. *Id.* at 7 (citing Ex. 1003, (code 57), 1:6–17). Petitioner cites Anzai as disclosing a substrate (limitation [1.a]) made of glass, synthetic resin, a conductive material, or a semiconductor. *Id.* at 7–8 (citing Ex. 1003, 3:57–61; Figs. 2A, 2B, 3A, 3B).

As designated by Petitioner, limitation [1.b] recites “a plurality of pixels formed on the substrate, each pixel being in a respective pixel area, each pixel area including at least a first area, a second area, and a third area.” Pet. vi. Petitioner’s annotated version of Figure 1 of Anzai is reproduced below (Pet. 9).



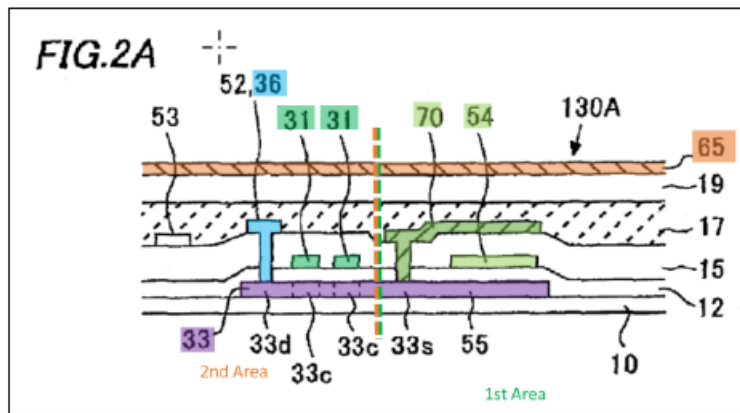
Petitioner’s Annotated Version of Figure 1 of Anzai

Petitioner cites Anzai as disclosing a plurality of pixel areas formed on the substrate with each pixel area 115 including at least a first area (a capacitor area, including capacitor 130A and 130B (not shown)), a second area (a transistor area, including driving transistor 40), and a third area (an OLED area, including OLED element 60). *Id.* at 8–9 (citing Ex. 1002, Neikirk Decl. ¶¶ 42–43; Ex. 1003, 3:37–31, Fig. 1).

b) Limitation 1.c

As designated by Petitioner, claim limitation [1.c] recites “at least a first capacitor and a second capacitor in the first area, the first capacitor including a first conductive layer formed over a first gate oxide layer, a first dielectric layer over the first conductive layer, and a second conductive layer over the first dielectric layer, and the second capacitor including the second conductive layer, a second dielectric layer over the second conductive layer, and a third conductive layer over the second dielectric layer.” Pet. vi.

Petitioner’s annotated version of an embodiment of a pixel portion of an organic EL display device in Figure 2A of Anzai is reproduced below.



Pet. 10; *see also* Ex. 1003, 21–24. In this embodiment, Petitioner identifies a first capacitor in the first area as formed by electrode layers 54 and 70 with insulating film 15 sandwiched between them. *Id.* Petitioner notes that in

Anzai electrode layer 54 is formed over gate insulating film 12 formed of SiO₂ (an oxide layer). *Id.* (citing Ex. 1003, 3:61–67, 4:25–47, Fig. 2A; Ex. 1002, Neikirk Decl. ¶ 45). Petitioner identifies a second capacitor as formed between third electrode capacitance layer 70 and cathode layer 65, with an insulating layer comprising first and second planarization films 17 and 19 that function as a capacitance insulating film. *Id.* at 11 (citing Ex. 1003, 4:30–51, 5:58–67). Petitioner cites Dr. Neikirks’s testimony that a person of ordinary skill in the art would have recognized the first and second capacitors share a second conductive layer, as recited in claim 1, because electrode layer 70 is common to both capacitors. *Id.* at 11–12 (citing Ex. 1002, Neikirk Decl. ¶ 47).

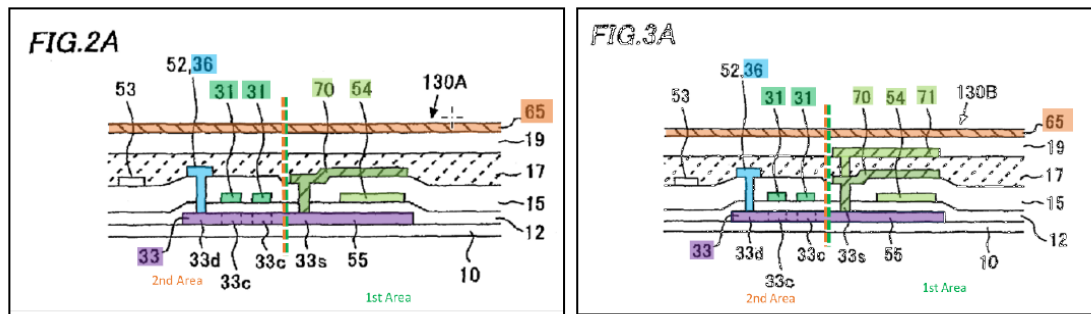
Petitioner also cites the embodiment in Anzai’s Figures 3A and 3B as disclosing the same structure as that shown in Figure 2A, except for the addition of electrode layer 71 to the capacitance structure such that electrode layers 70 and 71 form a U-shaped structure conductive layer that is shared between the first and second capacitor. *Id.* at 12–13 (citing Ex. 1002, Neikirk Decl. ¶ 48; Ex. 1003, 5:52–61, 5:67–6:3). Thus, according to Petitioner, the claimed second capacitor is formed by the combined electrode layer 70/71 and cathode layer 65. *Id.*

c) Limitation 1.d

As designated by Petitioner, claim limitation [1.d] recites “a transistor in the second area, the transistor including a first semiconductor layer formed on the substrate, the first gate oxide layer over the first semiconductor layer, and a fourth conductive layer over the first gate oxide layer, wherein the fourth conductive layer is formed of the same conductive film as the first conductive layer, and wherein both the first conductive layer

and the fourth conductive layer are directly formed on the gate oxide layer.”
Pet. vi.

Petitioner identifies Anzai’s pixel selecting transistor 30 as corresponding to the transistor recited in claim 1. Pet. 13–14. Petitioner’s annotated version of embodiments of pixel portions of an EL display device shown Figures 2A and 3A of Anzai is reproduced below.

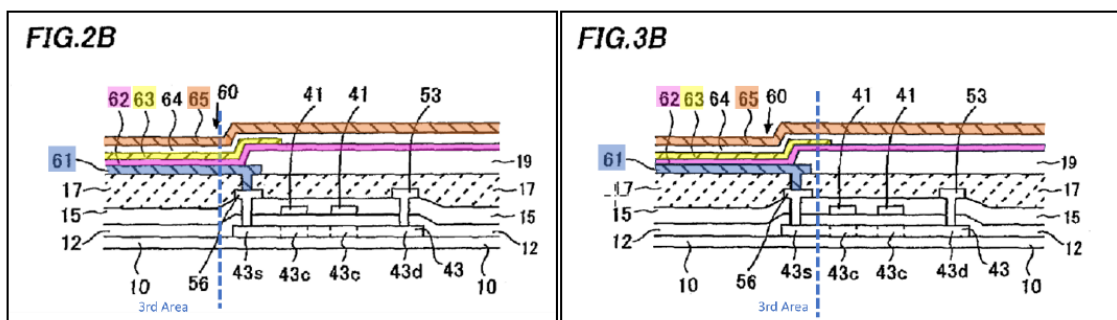


Id. at 15; *see also* Ex. 1003, 3:6–12. Petitioner states that transistor 30 is formed in the transistor area discussed above by gate electrode 31 above active layer 33 with gate insulating film 12 between them; drain electrode 36 is connected to drain 33d and third capacitance electrode layer 70 is connected to source 33s. *Id.* (citing Ex. 1003, 4:1–25, 4:37–40, Figs. 2A, 3A; Ex. 1002, Neikirk Decl. ¶¶ 50–53). Petitioner notes that the device is fabricated using sequentially deposited layers by (i) depositing an amorphous silicon film on substrate 10 and recrystallizing it to form a polycrystalline film that functions as active layer 33 (the claimed first layer), (ii) forming a single or multiple layers of SiO₂ and SiN on layer 33 to serve as gate insulating film 12 (the claimed fourth layer) and (iii) disposing on gate insulating film 12 gate signal line 51 that works as gate electrode 31. *Id.* at 14 (citing Ex. 1003, 4:11–14, Figs. 2A, 3A; Ex. 1002, Neikirk Decl ¶ 52). According to Petitioner, Anzai’s gate electrode 31 (the claimed fourth conductive layer) is formed of the same conductive film as first electrode

layer 54 (the claimed first conductive layer) because Anzai discloses each as being formed directly on the gate insulating layer 12 (the same underlying structure) by the same process and of the same material. *Id.* at 15 (citing Ex. 1003, 4:25–40 (stating that second capacitance electrode layer 54 is made of Cr or Mo and formed in the same layer as gate electrode 31 by the same process), Figs. 2A, 3A). Petitioner asserts that an ordinarily skilled artisan would have understood that forming electrode layers in the same layer by the same process with the same material would mean that the two electrode layers are formed of the same conductive film. *Id.* at 15 (citing Ex. 1002, Neikirk Decl. ¶ 53).

d) Limitation 1.e

As designated by Petitioner, claim limitation [1.e] recites “a light emitting device in the third area, the light emitting device including a fifth conductive layer, a first organic layer over the fifth conductive layer, and a sixth conductive layer over the first organic layer, wherein the sixth conductive layer is formed of the same conductive film as the third conductive layer.” Pet. vi. Petitioner’s annotated version of the pixel embodiments shown in Figure 2B and 3B of Anzai is reproduced below.



Id. at 16. Petitioner cites Anzai as disclosing a third OLED area with anode layer 61 (the claimed fifth conductive layer) connected to active source 43a through electrode 56, emissive layer 63 (the claimed first organic layer) over

anode layer 61 (the claimed fifth conductive layer), and cathode layer 65 (the claimed sixth conductive layer) over emissive layer 63 (the claimed first organic layer) formed of the same conductive film as cathode layer 65 (the claimed third conductive layer). *Id.* at 15–16 (citing Ex. 1002, Neikirk Decl. ¶¶ 54–57; Ex. 1003, 5:3–33, Figs. 2B, 3B). Petitioner notes that EL element 60 includes anode layer 61 made of the transportation electrode, e.g., Indium Tin Oxide, hole transportation layer 62, emissive layer 63, electron transportation layer 64, and cathode layer 65. *Id.* at 16–17. According to Petitioner, an ordinarily skilled artisan would have understood (i) that emissive layer 63 is organic because organic molecules are activated during operation, (ii) that intervening layers 62, 64 in organic element 60 do not change the relative positions of the layers recited in claim 1, because emissive layer 63 is over anode 61 and cathode layer 65 is over emissive layer 63, and (iii) that cathode layer 65 (the claimed sixth conductive layer) is formed from the same conductive film as the third conductive layer of the second capacitor because the same film that serves as the third conductive layer serves as the sixth conductive layer. *Id.* at 17 (citing Ex. 1002, Neikirk Decl. ¶¶ 56–57).

3. *Claim 2*

Claim 2 depends from claim 1 and recites “each pixel further comprising a seventh conductive layer in the second area for providing contact to the first semiconductor layer.” Petitioner cites Anzai as disclosing drain electrode 36 formed by filling a contact hole at a location in the Transistor Area corresponding to drain portion 33d of active layer 33. Pet. 18. According to Petitioner, an ordinarily skilled artisan would have understood Anzai’s drain electrode 36 to be a layer (the claimed seventh

conductive layer) that provides contact to active layer 33 by filling the contact hole. *Id.* (citing Ex. 1002, Neikirk Decl. ¶ 59). Petitioner contends that Anzai is similar to the '121 patent, which teaches metal pattern 210B is formed by depositing metal over ILD 208 to form a pattern over areas B and C, and that metal pattern 210 contacts polysilicon pattern 202B through a via hole in ILD 208 and gate oxide 204. *Id.* at 18–19.

4. *Claim 3*

Claim 3 depends from claim 1 and recites “the second dielectric layer comprises a passivation layer and a capping layer.” Petitioner notes that the '121 patent describes a passivation layer 212 of SiN formed over ILD208 and second metal patterns 210A and 210B and a SiN capping layer 216 disposed to cover passivation layer 212 and ITO pattern 214C. Pet. 19 (citing Ex. 1001, 5:34–36, 5:40–42). Petitioner also notes that, other than describing them as separate layers, the '121 patent does not ascribe any special meaning to the terms passivation layer and capping layer. *Id.* (citing Ex. 1002, Neikirk Dec. ¶ 61). According to Petitioner, consistent with the '121 patent description, an ordinarily skilled artisan would have understood that the passivation and capping layer need not be made of different materials. *Id.* (citing Ex. 1002, Neikirk Decl. ¶ 61). Petitioner notes that Anzai discloses first planarization film 17 and second planarization film 19 function as the capacitance insulating film in the first embodiment, and that, although Anzai does not specify the material for planarization layer 19, it is the sole layer between electrode layer 71 and cathode layer 65 forming the second capacitor. *Id.* at 19–20. Petitioner contends that an ordinarily skilled artisan would have understood that when first and second planarization layers 17 and 19 are used as the insulating films, one of the layers can be

understood as a passivation layer and the other layer as a capping layer, as claimed. *Id.* at 19–20.

5. *Claim 5*

Claim 5 depends from claim 1 and recites “the second conductive layer and the fifth conductive layer both comprise indium tin oxide (ITO).” Noting that in Figures 3A and 3B anode layer 61 (the claimed fifth conductive layer) is made of ITO, Petitioner cites Anzai’s second embodiment as disclosing this feature. *Id.* at 21 (citing Ex. 1003, 5:55–57. Figs 3A, 3B; Ex. 1002, Neikirk Decl. ¶¶ 66–68).

6. *Conclusion*

As noted above, Patent Owner does not rebut any of Petitioner’s contentions. Prelim. Resp. 1. Based on the evidence and arguments currently of record, we determine for purposes of institution that Petitioner has demonstrated that Anzai discloses to a person of ordinary skill all the limitations of claims 1–3 and 5.

C. *Petitioner’s Contention That Claim 4 Would Have Been Obvious Over Anzai and Yamazaki*

1. *Yamazaki*

Yamazaki concerns a light emitting device using a light emitting element having a layer that contains an organic compound between a pair of electrodes on which an electric field is applied to obtain fluorescence or phosphorescence. Ex. 1004, 1:7–12. Yamazaki’s light emitting device has a pixel part that includes a plurality of light emitting elements between first and second substrates which have their respective insulating surfaces and a driving circuit including a plurality of thin film transistors; the light emitting element has a first electrode, a layer containing an organic compound in contact with the first electrode, and a second electrode in contact with a

layer containing the organic compound. *Id.* at 2:42–51. Yamazaki discloses a number of manufacturing steps that seek to improve manufacturing yield and improve reliability. *See generally, id.* at 2:42–7:67.

2. *Petitioner’s Contentions Concerning Reasons to Combine the Teachings of Anzai and Yamazaki*

Petitioner contends that Anzai and Yamazaki are analogous art as each relates to organic light emitting devices on a substrate that includes a first area containing at least one capacitor, a second area containing a transistor, and a third area containing a light emitting device having an organic layer between two electrode layers. Pet. 25 (citing Ex. 1002, Neikirk Decl. ¶ 77). Petitioner acknowledges that Anzai does not state explicitly what materials are used to form planarization layers 17 and 19 (other than an organic resin for layer 17), but notes Anzai’s explicit disclosure that silicon nitride (SiN) can be used in interlayer insulating film 15 between second capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitance element 130 and in gate insulating film 12 between first and second capacitance electrode layers 55 and 54. *Id.* at 23 (citing Ex. 1004, 4:8–10, 4:17–24, 4:40–47). Petitioner contends that to address the issue of what materials can be used to form the first and second planarization layers of Anzai, an ordinarily skilled artisan would have had reason to look to Yamazaki, because Yamazaki teaches using SiN as an insulating layer under its cathode layer and as a planarization film for flattening the surface. *Id.* at 25–26 (citing Ex. 1004, 11:45–50, 11:22–12:20).

3. *Claim 4*

Claim 4 depends from claim 3 and recites “at least one of the passivation layer and the capping layer comprises silicon nitride.” Petitioner

cites Anzai as disclosing a second dielectric layer comprises a first passivation layer (first planarization layer 17) and a capping layer (second planarization layer 19). Pet. 23, 45; *see* Section IX.C.4 herein. Petitioner acknowledges that Anzai does not explicitly state what materials are used to form planarization layers 17 and 19 (other than organic resin for layer 17), but argues that Anzai discloses those layers function as the capacitance insulating film. Pet. 45 (citing Ex. 1003, 4:20–24, 5:62–6:9). Petitioner also argues Anzai teaches that SiN can be used as interlayer insulating film 15 between second capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitor element 130 and in gate insulating film 12 between first and second capacitance layers 55, 54. Pet. 23; *see also id.* at 45 (citing Ex. 1003, 4:8–10, 4:17–24, 4:40–47, 5:62–6:9). *See* Section IX.C.4 herein.

Petitioner asserts that Yamazaki discloses the claimed passivation layer, i.e., insulating material 30 disposed between cathode 32 and electrodes 46, 47, 48, 24, and 23, in a manner similar to Anzai’s layer 17 and 19, disposed between cathode 65 and electrodes 53, 52, 71, where the top surface is flattened relative to the topology underneath, using, e.g., a chemical mechanical polish process. Pet. 24–25 (citing Ex. 1004, 20:17–24); *see also* Pet. 42–43 (citing Ex. 1004, Fig. 2; Ex. 1002, Neikirk Decl. ¶¶ 110–121). Petitioner also cites Yamazaki as disclosing SiN is a suitable material for layer 30 and argues it would have been obvious to an ordinarily skilled artisan to use SiN for at least one of Anzai’s planarization films 17 or 19. *Id.* at 23–27 (citing Ex. 1004, 11:45–50; Ex. 1002, Neikirk Decl. ¶ 76). Thus, according to Petitioner, an ordinarily skilled artisan would have had

reason to modify Anzai to use inorganic materials, such as SiN for Anzai's films 17 and 19. *Id.*

4. *Conclusion*

As noted above, Patent Owner does not rebut any of Petitioner's contentions. Based on the evidence and arguments currently of record, we determine for purposes of institution that Petitioner has demonstrated that a person of ordinary skill would have had reason to combine the teachings of Yamazaki and Anzai and that in combination, these references would have disclosed or suggested the limitations of claim 4 to such an ordinarily skilled artisan.

D. Petitioner's Contentions That Claims 1–7 Would Have Been Obvious Over Yamazaki and Anzai

1. *Claim 1*

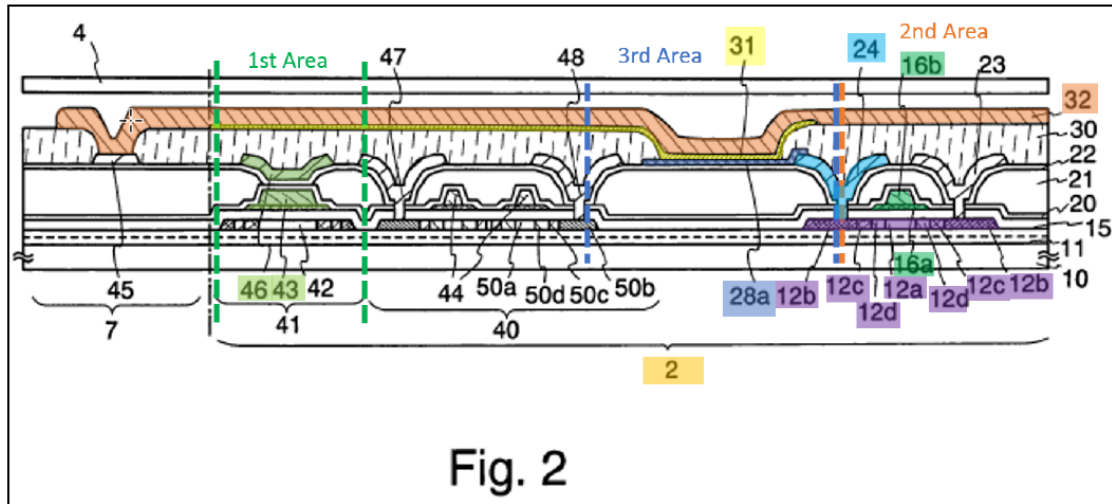
a) *Limitations 1.pre, 1.a, 1.b*

Petitioner cites Yamazaki as disclosing an EL device having a substrate 10 on which driving circuits and pixel parts are formed. Pet. 27–28. Petitioner also cites Yamazaki as disclosing pixel part 2 comprising a plurality of pixels within an active-matrix light emitting device. *Id.* at 29. Petitioner notes that each of Yamazaki's pixel parts includes “capacity” 41⁴ in a Capacitor Area (the claimed first area) and a current controlling TFT in a TFT Area (the claimed second area) and an EL element in an EL Area (the claimed third area). *Id.* (citing Ex. 1004, 2:37–64, 8:63–9:4, 9:47–64, 9:47–10:55, 11:22–12:13, 20:3–21:7, Figs 1A, 2; Ex. 1002, Neikirk Decl. ¶ 85).

⁴ Petitioner contends, and Patent Owner does not dispute, that one of ordinary skill in the art would have understood the term “capacity” used in this context to mean “capacitor.” Pet. 24 n.1.

b) *Limitation 1.c*

Petitioner cites Yamazaki as disclosing first and second capacitors in the first area (capacity 41). Pet. 30. Petitioner's annotated version of Figure 2 of Yamazaki is reproduced below.



Pet. 32. According to Petitioner, Yamazaki's discloses a first capacitor in the first area formed by electrode 43 (the claimed first conductive layer) over gate insulating film 15 (the claimed first gate oxide layer), interlayer insulation films 20, 22 (the claimed first dielectric layer) over electrode 43 (the claimed first conductive layer), and electrode 46 (the claimed second conductive layer) over interlayer insulation films 20, 22 (the claimed first dielectric layer). *Id.* at 30–31. Petitioner asserts that, in the proposed combination, Yamazaki's second capacitor includes electrode 46 (the claimed second conductive layer), cathode 32, and sandwiched between them, insulating material 30 having a thickness selected according to the teachings of Anzai that acts as a dielectric material. *Id.* at 32 (citing Ex. 1004, 9:65–10:55, 11:22–12:13).

Petitioner acknowledges that Yamazaki does not disclose a capacitor formed between electrode 46 and cathode 32, but argues that, to an

ordinarily skilled artisan, it would have been obvious to combine Yamazaki's teaching with those of Anzai for the formation of a storage capacitor using cathode 32, which extends from the third area into the first area, as an electrode for a storage capacitor with electrode 46. Pet. 32–34 (citing Ex. 1002, Neikirk Decl. ¶ 89). In particular, Petitioner cites Anzai as disclosing a first capacitor between layers 54 and 55, a second capacitor between electrode layers 54 and 70 or 70/71, and a third capacitor between electrode layers 70 or 70/71 and cathode 65, which extends from the third area into the first area. *Id.* at 33 (citing Ex. 1003, 4:48–51; Ex. 1002, Neikirk Decl. ¶ 94). According to Petitioner, applying Anzai's teaching of establishing a storage capacitor between electrode layer 70 and cathode layer 65 where first and second planarization layer 17 and 19 are the dielectric materials, a person of ordinary skill in the art would have understood that a capacitor can be formed between Yamazaki's electrode 46 and cathode 32, such that insulating material 30 and EL layer 31 act as the dielectric between the capacitor electrodes. *Id.* at 34 (citing Ex. 1002, Neikirk Decl. ¶ 97).

c) Limitation 1.d

Referencing its annotated Figure 2, Petitioner cites Yamazaki as disclosing the claimed transistor in the second area in the form of an unnumbered current-controlling TFT arranged on pixel part 2 formed on substrate 10 below gate insulating film 15. Pet. 35–36 (citing Ex. 1004, 9:47–64, Fig. 2). Petitioner states that regions 12a–12d of the current controlling TFT (i.e., channel region 12a, high level impurity source and drain regions 12b, low impurity regions 12c, 12d over which gate electrode 16a, 16b are deposited) are a semiconductor layer, that gate insulating film 15 (constructed of a silicon oxide film) is formed over regions 12a–12d, and

that gate electrode 16a/16b and electrode 43 are formed on gate insulating film 15. *Id.* at 35–36 (citing Ex. 1004, 10:31–33, Fig. 2; Ex. 1002, Neikirk Decl. ¶ 99). Noting that Yamazaki does not explicitly disclose the materials used to form gate electrode 16a/16b and electrode 43, Petitioner observes that Yamazaki refers to gate electrode 16a/16b collectively as electrode 16 including first conductive layer 16a (a thin lower layer formed directly on insulation layer 15) and second conductive layer 16b (a narrower but thicker trapezoidal upper layer formed directly on lower layer 16a). *Id.* at 36 (citing Ex. 1004, 18:8–14, Fig. 2). Noting that electrode 43 has the same configuration (composition and general shape) as that of electrode 16, Petitioner contends it would have been obvious to an ordinarily skilled artisan to form electrode 16 and electrode 43 of the same conductive film. *Id.* at 36–37 (citing Ex. 1004, Fig. 2; Ex. 1002, Neikirk Decl. ¶ 101).

Petitioner further states that, consistent Yamazaki’s disclosure and the common semiconductor manufacturing practice of forming multiple components in the same processing steps (e.g., layer deposition and patterning), an ordinarily skilled artisan would have understood that Yamazaki discloses that terminal electrode 19a/19b in Figure 1B has the same configuration as electrode 43 in Figure 2 and formed them in the same step as an efficient manufacturing process. *Id.* at 37–39.

d) Limitation 1.e

Petitioner cites Yamazaki as disclosing in the EL area a first electrode 28a that functions as an anode of the EL element formed on anode 28 (the claimed fifth conductive layer) and second electrode 32 (the claimed sixth conductive layer) that functions as the cathode also formed over EL layer 31 (the claimed first organic layer), such that cathode 32 (in the third area) is

formed of the same conductive film as the third conductive layer. Pet. 39–41 (citing Ex. 1002, Neikirk Decl. ¶ 106). Petitioner also notes that anode layer 28a may be transparent conductive film, e.g., ITO, and cathode 32 is deposited on top of EL layer 31, which functions as wiring common to all pixels. *Id.* at 39–40 (citing Ex. 1002, Neikirk Decl. ¶ 104).

2. *Claim 2*

Petitioner cites Yamazaki’s disclosure of connecting electrode 24 for making a connection between the first electrode (anode electrode 28a) to source region 12b as teaching the claimed seventh conductive layer. Pet. 41 (citing Ex. 1004, 9:47–64, Fig. 2; Ex. 1002, Neikirk Decl. ¶¶ 107–109).

3. *Claim 3*

Petitioner notes that the ’121 patent does not define the claimed passivation layer and capping layer that comprise the second dielectric layer. Pet. 42. Petitioner cites Anzai’s disclosure of planarization layer 19 as the claimed capping layer. *Id.* (citing Ex. 1002, Neikirk Decl. ¶¶ 110–121). Petitioner asserts that Yamazaki discloses the claimed passivation layer, i.e., insulating material 30 disposed between cathode 32 and electrodes 46, 47, 48, 24, and 23, in a manner similar to Anzai’s layers 17 and 19, disposed between cathode 65 and electrodes 53, 52, 71, where the top surface is flattened relative to the topology underneath. *Id.* at 42–43 (citing Ex. 1004, Fig. 2; Ex. 1002, Neikirk Decl. ¶¶ 110–121). According to Petitioner, insulating material 30, which can be photosensitive or non-photosensitive organic material or inorganic material, also called a bank, is formed on both ends of electrode 28a (e.g., anode), which may be formed by an organic resin film or an insulating film including silicon. *Id.* at 43 (citing Ex. 1004, 11:22–65, Fig. 2).

Referencing the embodiment disclosed in Figure 15A of Yamazaki, Petitioner also argues that interlayer insulation film 1431 made of organic or inorganic material, e.g., a silicon nitride film, deposited below insulation film 1403, corresponds to insulation layer 30, and that an ordinarily skilled artisan would have understood this embodiment to teach an additional insulation layer 1431 formed under insulating material 1430. Pet. 43–44 (citing Ex. 1004, 35:65–36:54, Fig. 15A; Ex. 1002, Neikirk Decl. ¶ 115).

Petitioner acknowledges that Anzai does not explicitly state what materials are used to form planarization layers 17 and 19 (other than organic resin for layer 17), but argues that Anzai discloses those layers function as the capacitance insulating film. Pet. 45 (citing Ex. 1003, 4:20–24, 5:62–6:9). Petitioner also argues Anzai teaches that SiN can be used as interlayer insulating film 15 between second capacitance electrode layer 54 and third capacitance electrode layer 70 of storage capacitor element 130 and in gate insulating film 12 between first and second capacitance layers 55, 54. Pet. 45 (citing Ex. 1003, 4:8–19, 4:17–24, 4:40–47, 5:62–6:9).

According to Petitioner, an ordinarily skilled artisan would have understood that adding another insulating layer would improve the planarization of Yamazaki's pixel area and would have had reason to add Anzai's planarization layer 19 above Yamazaki's insulating material 30 because both flatten the surface of the pixel area. *Id.* at 46 (citing Ex. 1003, 4:8–10, 4:17–24, Fig. 2A; Ex. 1004, 11:22–12:52, 20:17–39, Fig. 2; Ex. 1002, Neikirk Decl. ¶ 120). Petitioner adds that this modification to improve flattening would involve require only depositing another planarization layer on top of an already existing planarization layer using materials disclosed in both references and known methods. *Id.*

4. *Claim 4*

Petitioner cites Yamazaki's disclosure of SiN as a suitable material for insulation layer 30 as teaching the claimed feature that at least one of the passivation layer (insulating material 30) and capping layer (planarization layer of Anzai) comprises SiN. Pet. 47 (citing Ex. 1004, 11:45–50; Ex. 1002, Neikirk Decl. ¶¶ 122–124).

5. *Claim 5*

Petitioner cites Yamazaki as disclosing an EL device in which anode 28a (corresponding to the fifth conductive layer) can be formed of ITO as claimed, but acknowledges that Yamazaki does not expressly disclose electrode 46 (corresponding to the second conductive layer) is formed of ITO, as claimed. Pet. 47–48. Petitioner cites Anzai's disclosure of an EL device in which anode layer 61 (corresponding to the fifth conductive layer) and electrode layer 71 both comprise ITO. *Id.* at 48. Petitioner asserts a person of ordinary skill would have understood from Yamazaki that electrode 46 and anode 28a could be deposited at the same time and, given Anzai's disclosure of forming two corresponding layers (anode layer 46 and combined electrode layer 70/71 using the same ITO material), an ordinarily skilled artisan would have had reason to use ITO, a well-known conductive material used in light emitting device electrodes, for both electrodes, in the manner claimed. *Id.* at 49–50 (citing Ex. 1002, Neikirk Dec. ¶¶ 131–132).

6. *Claim 6*

Claim 6 depends from claim 1 and recites “the second dielectric layer comprises a layer of passivation silicon nitride and a second organic layer formed on the layer of passivation silicon nitride, the second organic layer comprising the same material as the first organic layer.” Again noting that

the '121 patent “provides no meaning for ‘passivation layer,’” Petitioner cites Yamazaki as disclosing that in the claimed first area (the capacitor area) the material between cathode 32 and electrode 46 includes insulation layer 30 (formed on electrode 46) and EL layer 31 (formed on insulation layer 30), with cathode 32 formed on EL layer 31. Pet. 50–51 (citing Ex. 1004, Fig. 2). Petitioner further asserts that EL layer 31 in the first area comprises the same organic material as EL 31 in the third area, because they are the same layer. *Id.* at 51–52 (citing Ex. 1002, Neikirk Dec ¶ 135).

7. *Claim 7*

Claim 7 depends from claim 1. Petitioner reads the limitations of claim 7 on Yamazaki and Anzai as follows:

the second dielectric layer (Yamazaki’s modified insulating material 30) comprises a passivation layer (Yamazaki’s insulating material 30), a capping layer (Anzai’s planarization layer 19) on the passivation layer and a second organic layer (Yamazaki’s EL layer 31) formed on the capping layer, at least one of the passivation layer (insulating layer 30) and the capping layer (Yamazaki’s insulating material 30) comprising silicon nitride, and the second organic layer (Yamazaki’s EL layer 31) comprising the same material as the first organic layer (Yamazaki’s EL layer 31).

Pet. 52 (citing Ex. 1002, Neikirk Decl. ¶ 136).

8. *Conclusion*

As noted above, Patent Owner does not rebut any of Petitioner’s contentions. Based on the evidence and arguments currently of record, we determine that Petitioner has demonstrated for purposes of institution that a person of ordinary skill would have had reason to combine the teachings of Yamazaki and Anzai and that in combination, these references would have disclosed or suggested the limitations of claims 1–7 to such an ordinarily skilled artisan.

X. CONCLUSION

For the reasons discussed above, we are persuaded that Petitioner has demonstrated a reasonable likelihood that it will succeed on each of its challenges to patentability.

XI. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a) an *inter partes* review of the '121 patent is hereby instituted, commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

FURTHER ORDERED that the trial is authorized on all grounds set forth in the Petition;

FURTHER ORDERED that the trial will be conducted in accordance with a corresponding separately issued Scheduling Order.

IPR2024-01132
Patent 7,586,121 B2

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