UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,	:	IPR2024-01132 and IPR2024-01315
Petitioner,	:	
v.	:	
OPTRONIC SCIENCES, LLC,	:	
Patent Owner.	:	

VIDEOTAPED DEPOSITION OF

DEAN NEIKIRK, PH.D.

CONDUCTED REMOTELY

Thursday, April 17, 2025

10:02 a.m. Central Time

Job No.: 110991

Stenographically Reported By:
Theresa Williamson, RPR, RMR, CRR, CA CSR No. 14545

(All appearing via video conference.)

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TRANSCRIPT MARKED AT THE REQUEST OF COUNSEL

(None.)

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QUESTIONS WITNESS INSTRUCTED NOT TO ANSWER

(None.)

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P R O C E E D I N G S

THE VIDEOGRAPHER: Okay. Good morning. We are now on the record. This is the beginning of Media Number 1 in the deposition of Dr. Dean Neikirk in the matter of BOE Technology Group Co., Ltd., versus Optronics Sciences, LLC. The case number is IPR2024-01132 and 01315.

This deposition is being held remotely as a Zoom conference and being taken on behalf of defendants on April 17, 2025, at 10:02 a.m. Central time.

The court reporter is Terry Williamson. I am Mariel Mercado, the videographer, on behalf of First Legal Depositions located in Los Angeles, California.

This deposition is being videotaped at all times unless specified to go off the video record.

Would all present please identify themselves, beginning with the noticing attorney.

MR. CUMMINGS: This is Jefferson Cummings with Russ August & Kabat representing patent owner. With me is my colleague Peter Tong.

THE VIDEOGRAPHER: Mr. Loney, I'm not sure if you're speaking, but I can't hear you.

MR. LONEY: Can you hear me now?

THE VIDEOGRAPHER: Yes.

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MR. LONEY: I'll just switch mikes.

Zachary Loney, with DLA Piper, on behalf of petitioner, BOE Technology Group, and the witness. With me are my colleagues Peiyao Zhang and Brian Erickson.

THE VIDEOGRAPHER: Okay. Thank you. Now the court reporter has a read-on and then she will swear in the witness.

THE STENOGRAPHER: Good morning. My name is Theresa Williamson, and my California CSR number is 14545.

(Whereupon, the deponent was duly sworn.)

EXAMINATION

BY MR. CUMMINGS:

Q Mr. Neikirk, you understand that this is a deposition in which I will ask you questions and you must answer them truthfully?

A I do.

Q And your attorney may object from time to time, but you must still answer the question unless your attorney tells you clearly and directly not to answer. Do you understand?

A I do.

Q Although no judge is present, this is a formal legal proceeding, just like testifying in

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court, and you are under the same legal obligation to tell the truth, the whole truth and nothing but the truth. Do you understand?

A I do.

Q If you do not understand any of my questions, let me know, and I will rephrase it. Do you understand?

A I do.

Q We will take a break from time to time. Usually every hour or so. You may ask for a break but not during the middle of a question. We'll need to finish the question before we take a break. Do you understand?

A Yes, I do.

Q And please answer my questions audibly and after I have finished speaking, for the court reporter. Do you understand?

A Yes, I do.

Q Are you on any drugs or medication that may affect your memory today?

A No, I am not.

Q Is there any other reason why you can't provide truthful testimony?

A No, there is not.

Q Before we begin, since we're all doing this

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remotely today and I can't see anything that's in front of you, can you let me know if you have any documents open in front of you?

A I have a clean paper copy of the two declarations that are -- that I've submitted in these two IPRs, along with clean paper copies of the two patents at issue.

I have no other paper documents in front of me. All the windows on my computer are closed, other than this Zoom window.

Q Thank you. You've been deposed before; correct?

A Yes, it is -- that is correct.

Q How many times?

A I don't keep count, but I'm sure it is well over 50 times.

Q Is there anybody in the room with you?

A No, there is not.

Q How many IPR proceedings have you been a part of?

A I have not counted those, but I'm -- I would guess it's in -- around 20 or perhaps a few more than that.

Q BOE retained you in this matter; is that correct?

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A Yes.

Q When were you retained?

A I didn't go back and check my records, so I don't recall precisely. I think it was on the order of six to nine months ago, I -- I think.

Q Now, I know you have a paper copy in front of you, but I'm going to introduce as Exhibit 1001 -- actually, that may get confusing. Sorry. Strike that.

Exhibit 1. This is your declaration for the '121 patent which is IPR2024-01132.

A And will a link appear in the chat window for that?

I'm sorry. I see it now. Excuse me. And I'll open that document to make sure it opens. Give me a moment. It's prompting. Save. So let me save that, and then I'll open it.

If you'll give me a moment, it is giving me a "Document Not Found" error, so let me try to figure out what's going on.

Sorry. It still is not opening. Give me one moment to try to -- ah.

Okay. Sorry. Now it -- now it has opened, and I see the document labeled as Exhibit 1002. It -- let me scan through it.

And it certainly does appear to be a copy of my declaration for the '121 patent.

Q How long did you spend working on this report?

A Well, I think I have a rough idea of total hours I've spent so far on these three patents, and it's in excess of 50 hours I believe. I didn't really break it out by patent. So I -- I would guess 15, 20 hours, something like that for this one.

Q Did you draft your own report?

A I did not type every word of this. Certainly I was, from the outset, involved in extensive discussions about the patent, about prior art. I made clear what my opinions were.

I did have help drafting and writing the actual type -- getting the actual text in, annotating figures; but in all cases, I have -- I have reviewed the documents, revised them to make sure they accurately reflected my own opinions.

Q Which documents did you review first?

A Well, I would have started with the patent itself, so the '121 patent and various pieces of prior art or what I think I've called -- referred to as background art.

Q Did you find the background art yourself or

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was it provided to you?

A I -- I suspect it was a mix. Some of the background art, I suspect I found.

We would have -- I would have discussions as to where I believed information would have been known to one of ordinary skill; and then in conjunction with that, there might have been a -- I would have expressed an opinion that it would be useful to have other art that simply reflected what one of ordinary skill would -- would, in my opinion, know.

Q Did you find any of the references that were applied in your grounds or were those provided to you?

A My recollection is that the references had already been identified.

Q Have you read the IPR petition?

A The petition itself, I'm not sure that I have.

Q Have you read the institution decision?

A I don't believe I have reviewed the institution decision either.

Q Did you do anything to prepare for the deposition today?

A I did.

Q What did you do?

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A I reviewed the patents. I reviewed the art that I have cited in my declaration. I reviewed my declaration. I did meet with counsel to discuss those documents.

Q About how long did you spend preparing for your deposition today?

A Again, I have not separated this out by patent; but I've worked on this, for the three, about two days. About 16, 18 hours total.

Q All right. I'd like to take a look at your declaration now. Let's start at paragraph 5, with your background and qualifications.

Looking through now at paragraph 8, I see you describe experience working with optical systems; is that correct?

A Yes, it is correct.

Q What sort of optical systems did you work with?

A I have worked with -- with many optical systems over the last, I guess, 40-plus years now. I did a lot of what's called optical spectroscopy early in my education, which involved many different types of optical measurement equipment, equipment for producing light, samples for -- examining samples using light.

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I continued to work on optoelectronics systems that operated over a very wide range of wavelengths. Most of my work was done in what's called the far infrared to infrared. Some of my work did involve optical, visible wavelengths, as well.

I worked with optically-controlled microwave devices, a number of optical sensors.

Also, I did some work with light emitters or materials designed to emit light.

Q Did any of that experience relate to manufacturing LEDs or OLEDs?

A Much of that related to the design and manufacture of LEDs. I did a great deal of work on so-called compound semiconductors which are used for LEDs.

I have been on Ph.D. committees for a colleague whose specialty was organic layers for -- for organic light-emitting diodes.

I personally did not work on the organic materials. Again, I'm quite familiar with them and have been on Ph.D. committees of students who were working in that area.

Q Is the -- is the design of LEDs different from the implementation of LEDs in a circuit? The physical design.

A I -- I'm not exactly sure I -- I understand what you mean; but generally, when I use the phrase "design," I'm talking about the structure used to build the LED, and I have built many LEDs personally.

Those structures, which are inherently tied to how they are made, when you talk about an electrical -- overall electrical circuit, you frequently abstract that as an electrical schematic and do some of your electrical design in a schematic fashion, at which point you have represented the electrical characteristics of the LED in some fashion appropriate for that schematic design.

Q So would all electrical engineers have a knowledge of semiconductor fabrication?

A Well, certainly in -- the electrical engineers in my department, my electrical and computer engineering at the University of Texas, that is a require -- was a required course, the fabrication of the devices.

One of the -- the device physics course -- semiconductor-device physics course that all our students are required to take, I also presented or taught some of the basics of how those devices are fabricated.

Q And you said "was." So that no longer is a

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requirement?

A Well, I retired in 20 -- the beginning of 2021, and I haven't checked recently for the overall requirements.

When I retired, I believe that our device physics course was still required for all of our electrical engineering students.

Our fabrication course, which is a separate course that I used to teach myself, was required for all of our students whose specialty, as an undergraduate, was in the semiconductor area.

Q Is that generally a required course in electrical engineering curriculums, or is that unique to the university you were at?

A It's certainly not unique to the University of Texas at Austin. I believe that sort of requirement was quite common amongst schools like University of Illinois, UC Berkeley, UCLA.

I'm trying to think of the ones where I knew people and had some specific familiarity with their curriculum. Michigan, Wisconsin.

Broadly speaking, I think most of the top 15 EE programs had requirements similar to that.

Q I see also in paragraph 8 of your declaration, you talk about IC fabrication. Is that

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integrated circuits?

A Yes. IC stands for integrated circuits.

Q What sort of integrated circuits did you fabricate?

A Well, most of my -- my research group's work was done in compound semiconductor devices and integrated circuits.

My teaching was specifically focused more on silicon-integrated circuits, so all sorts: Digital, analog, the scales of different levels of integration starting in the old days with VLSI and then transitioning into ULSI dimensions, ranging from multiple microns, down to about 100 nanometers over the years.

Q Did any of that include the patented technology at issue here?

A Well, by "patented technology," if you're referring to the multi -- if you are referring to the '121 patent, which concentrates on layers and their arrangements relative to one another to form components like capacitors, well, yes, certainly, those topics were covered.

Q When was your relevant experience? What time period?

A Well, I -- I mean, I -- I started doing this

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work in 1981, and so -- and continued that until my retirement in 2021. So over the course of about -- I guess that's 30 years.

Q And is your IC experience the closest to the subject matter of the '121 and '477 patents?

A Well, I -- I'd certainly say that experience is very relevant. I don't know whether -- I'm just looking at the claims of the '121 very quickly.

Given the elements of the claims, I'd say that work on the design and fabrication of interconnects, electrodes, their use in electrical circuits, all that's very relevant. So certainly, broadly, the IC design and IC fabrication would be extremely relevant.

Q Can you explain to me what an electrode is?

A An electrode is a word that is used broadly to refer to a portion, an object, in many cases a specific object, that's used as part of an electrical device.

It's rarely, standing by itself, forming a complete component; but it's part of an electrical component.

Q What do you mean "part of an electrical component"?

A Well, for instance, a MOSFET has four

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electrical connections to the outside world, if you will: A substrate, a source, a gate and a drain. And the connections to the outside world, in many cases, are referred to as electrodes.

Now, as is usually the case, the meaning of the word is context-sensitive; but broadly speaking, the connection and, in some cases, people would call the source itself, the physical source, an electrode of the MOSFET. Similarly, gate, drain and substrate.

Q Is an interconnect an electrode?

A It could be. An interconnect is usually something that people talk about as, if you will, wiring that's used to connect different components or portions of components together in an integrated circuit.

So usually when I use, and I think people generally use, the phrase "interconnect," they are singling out something that's used to wire together, if you will, other things; but in some instances, people call those electrodes, as well. They certainly are usually connected to electrodes.

Q So there is some distinguishment between an electrode and an interconnect? For example, an interconnect could connect to an anode? And the anode would be an electrode?

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MR. LONEY: Objection. Form.
THE DEPONENT: Well, so "interconnect" is, I'd say, in many cases -- again, it's context-sensitive; but in many cases, it's probably somewhat narrower than "electrode," but it might very well refer to the wiring connected to an electrode, a part of a component. In something that has a cathode and an anode, you might well have a wire connected to one or both of those, and those might be referred to as interconnects.
BY MR. CUMMINGS:
Q So to clarify my understanding, an electrode -- an anode would be an electrode?
MR. LONEY: Objection. Form.
THE DEPONENT: In some contexts, what is identified as an anode might also be referred to as an electrode. I would agree with that.
BY MR. CUMMINGS:
Q What about a bus line? Is that an electrode?
A Again, it depends on the context. I've seen "electrode" used very broadly. I've seen it used in a very narrow fashion. Depending on the context, it might be.
A bus line is something that I would put generally in the class of an interconnect.

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Q And generally, in the art, as an expert, would it be an electrode?

MR. LONEY: Objection to form.

THE DEPONENT: I could -- I couldn't answer that in general. It depends on the specific context. Again, I think I just explained: I have seen the word "electrode" used to describe very specific and narrow structures. I have also seen it used to describe a very wide range of structures and used very broadly. So it's -- it's certainly context-sensitive.

BY MR. CUMMINGS:

Q What context would cause this to go one way or another?

MR. LONEY: Objection. Form.

THE DEPONENT: You know, I -- I have read patents where an electrode was clearly used in both the specification and the -- the claims, to refer to a very specific shape and location of a metal structure, for instance.

I've seen other cases where it referred to everything connected to a battery. So, you know, an entire conductive path connected to a battery. It's very context-sensitive.

BY MR. CUMMINGS:

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Q Are there any contexts, outside of the teachings of the patent, that would impact your understanding?

A I think you find the same thing in textbooks, for instance. You know, you -- the context in which the word is used would explain to a reader in a book, a textbook, what the reference was to.

In a -- an electroplating solution, the two -- the two things that are dipped into a liquid electroplating solution are frequently referred to as electrodes. That description would -- someone who was trying to learn about electroplating would understand what was meant by the context, in that context.

Q All right. I'd like to move on now. I guess referring back to paragraph 8, it seems like you have a lot of experience in the semiconductor fabrication realm. Is that fair to say?

A Yes, it is.

Q In your opinion, would someone, who has experience taking pre-packaged LEDs and using them in a circuit, be less qualified than someone like yourself who has experience with the actual fabrication of the LEDs?

A I don't know that I would necessarily

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characterize it as less experience. It might be different experience.

Q In the context of LED manufacture or fabrication?

A Well, if the person has never done anything but place a packet -- pre -- already completed and packaged LED into an electrical circuit and use it in that fashion, they might well not know anything about how it was built inside that, nor would they need to.

Q Would they be qualified as a person of ordinary skill in the context of this patent?

A Well, I believe in -- I believe in my report I have explained what I believe -- what, in my opinion, is the level of ordinary skill.

That's on -- in this document, it is paragraph 23 on page 14, where I have stated that it would be someone with a Bachelor's degree in electrical engineering or a comparable field of study, two to three years of professional experience with electronic and optoelectronic device design, and then pointing out that additional education can substitute for professional experience and, if you will, vice versa.

In order to do device design, you need to understand how devices are built.

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This -- I did point to experience with electronic and optoelectronic device design. That's more than just saying they have knowledge of circuit design.

Q That's what I'm asking. Would the mere use of pre-packaged LEDs qualify as the needed experience?

A I don't think that would meet my -- what is, my opinion, would be one of ordinary skill. You wouldn't know what was inside the package.

Q So is your definition of optoelectronic device design specific to the fabrication of the package?

A Not necessarily the package, although the package would be one part of it. It would also include understanding the layers used inside the materials, the stack-ups, how those are used to design a device. It's a physical design, not just -- just an electrical look-up table.

Q Is there anything else encompassed by the term "optoelectronics"?

A Well, that term, standing on its own, broadly refers to electronic systems that have some aspect involving light. I think that's what optoelectronics means.

Q So designing a flashlight would qualify under the term "optoelectronics"?

A In its broadest sense, yes. Many flashlights today use LEDs and have driver circuits and voltage regulators. Ultimately, it's about emitting light, controlling its brightness. If that's the kind of flashlight you want, that's an optoelectronics system -- system design.

Q You emphasized "system" there. Can you describe the difference between "system" and "device design"?

A Well, in a flash -- you used the example of a flashlight. The design of the LED is a device design. The design of -- let's say it had a regulator in it used to power MOSFET. The design of the MOSFET is a device design.

The flashlight viewed as a combination of pre-packaged components: Batteries, LEDs, say, an integrated circuit, can be done as a system-level design, where each of those components is simply represented as a black box with certain terminal electrical characteristics; but that's not what I was referring to here. I said "device design."

Q For the technology here, wouldn't some experience with displays or LEDs be needed?

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A Well, for this particular patent, inasmuch as it discusses the layers used for an electroluminescent device, the -- having experience with optoelectronic device design, as I've stated in my opinion as to what would constitute one of ordinary skill, yes, that would be required.

Q And just to be clear, LED device design refers to the fabrication of the LED itself?

A That's part of it. I mean, a device design is, with some desired output -- for an LED, it would be light of, for instance, a particular color, at a particular brightness or luminance, power consumption, all of those things, coupled to the selection of materials and any appropriate -- I'll refer to it as stack-up, arrangement of various layers, sizes, geometries, their orientations relative to one another, all of that would be involved in that design.

Q So in order to properly design it, would a person of ordinary skill need an understanding of displays?

MR. LONEY: Objection. Form.

THE DEPONENT: Well, if -- if the application was for displays, that would be useful. Again, I said a device with a certain luminance, power

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consumption, thermal characteristics. Well, that can be different in the display than a single device.

But generally, you have to understand how the layer selections, their arrangements, their sizing, how that influences the performance of each device. In a -- in a display, a display would normally have many devices.

BY MR. CUMMINGS:

Q What role do the thermal characteristics play in a display device?

A Well, the same role they do in every device. Many devices are limited, ultimately, by thermal dissipation because most semiconductors, if they get too hot, their electrical characteristics change and, in many cases, they might completely stop working, but they will definitely work differently.

In a single device, that's true. In a display, that's true. The style -- your ability to remove heat from the two may be different.

In a display, you typically have a very large number of devices in some proximity to one another.

In a single LED, you may just have one, with lots of, if you will, space around it, to get heat out. So they can be different, certainly.

Q So is thermal management an important factor

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in designing an LED?

A Well, you know, with respect to -- to the '121, I don't think thermal management has been discussed at all, and I don't think the layers, and their arrangements discussed, clearly have a direct connection to thermal management.

In a broader sense, yes, thermal management is a topic, that if you're actually going to build something, you need to be -- have some awareness of.

Q What's covered by electronic device design?

A Well, I think it's -- it's a somewhat broader -- optoelectronics, I would say, is a subset of electronic; but electronic systems, some don't involve light in any fashion. A power MOSFET doesn't typically have much to do with light. It's an electronic device design.

Q Are there any optoelectronic devices that don't emit light?

A Oh, well, okay, yes, of course. Optical detectors. A camera chip is an optoelectronic system; and the individual photodetectors inside it, as well as their arrangement relative to lenses, other optical components, as well as their electrical characteristics, are all an optoelectronic device design.

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That's designed to convert light into electrical signals. So they don't emit light. They certainly interact with light. They absorb it.

Q Are there different considerations in the design of detectors as opposed to emitters?

A Certainly there are. Most detectors won't emit or will emit poorly. Many emitters will either not detect or detect poorly because they have been optimized for different things.

Q Would the thermal management be an issue in detectors?

A Certainly. The absorption of light converts -- if it's a light-to-charge conversion, in an ideal world, you want all the light that gets absorbed to be turned into charge. Unfortunately, that's rarely the case. Some of that light gets absorbed and converted into heat.

So, yeah, thermal issues. One type of infrared device that I and my research group did a great deal of work on actually converts light to heat, and then the heat is converted to an electrical signal. So that was all about thermal management.

Q Do you have any experience working with cathode-ray tubes?

A A limited amount. I have not built a

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cathode-ray tube.

I have worked on what's called vacuum electronics and some rather exotic types of detectors where field emission, which is one of the techniques used to generate the so-called cathode rays, in a cathode-ray tube, was the transduction mechanism; but in that case, I don't think it -- that particular device, there wasn't a phosphor to convert that into light, as there would be in a CRT. I actually have done some work on phosphors but not really specifically for use in CRTs.

Q Is the design of a CRT similar to that of an LED display?

A No. I would say a CRT design is substantially different. I don't know whether -- well, there are some planar field-emission devices; but the classic CRT is a vacuum device using high voltages to generate an electron beam, electric fields to steer that beam, in some cases magnetic fields to focus it, and the phosphor for color CRT, a moderately complicated set of phosphors. Those are very different structures than you'd find in an LED.

Q Do you have any experience working with capacitive touch?

A Some, yes.

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Q Can you describe that experience?

A Well, I did, and my -- my students and I did a great deal of work on a variety of sensors. Force transducers was one of the things that we did do quite a bit on. Very small force transistors, so-called microelectromechanical systems.

In force transduction, you can either stress -- you can either detect -- well, there are multiple quantities you can detect. One is a change in capacitance.

Our own research, we were more interested in other transduction mechanisms; but in order to understand if our other transduction mechanisms might have an advantage, we had to compare them to the -- sort of, a classic capacitance transducer.

Q And is that within the definition of "optoelectronics"?

A Well, the capacitance transducer, I -- inasmuch as those use capacitance change, that's not normally sensed using an optical signal.

Now, I actually did do a lot of work on what are called membrane transducers, where we used the change in optical reflectants as the transduction mechanism, but those weren't capacitive sensors.

A capacitive sensor -- capacitance is an

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electrical-effect change, not an optical change, normally.

Q What about capacitive-touch screens? Do you have any experience there?

A Again, only -- only as it would relate to the individual transducers.

The only other work I did a little bit on, relative to touch displays, were using infrared systems as opposed to capacitance.

Q All right. Before I start my next line of questioning, do you want to take a break and go off the record?

A Yes, that would be -- that would be fine. Five minutes would be plenty for me.

MR. CUMMINGS: All right. Let's do a five-minute break.

MR. LONEY: If we can stay down on the record for a second.

Dean, if you could drop off, that would be great. Just make sure you can't hear. I just want to speak with counsel for a minute.

THE DEPONENT: I will turn off my audio.

MR. ERICKSON: Okay. You're muted. I just want to make sure you can't hear me. Okay. Great.

THE VIDEOGRAPHER: Okay. Off the video

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record --
THE DEPONENT: Wait, wait, wait.
MR. ERICKSON: We should stay on the record for just a second.
THE DEPONENT: Hold on. I'm still hearing. I turned off my microphone. Let me do the -- I'm going to turn off my audio.
MR. ERICKSON: Turn it off completely, please.
THE DEPONENT: Turn off the audio. Okay. So hopefully I can no longer hear anything. I'm going to turn off my microphone now.
MR. ERICKSON: Great.
THE DEPONENT: And step away.
MR. ERICKSON: Thanks, Dean.
THE VIDEOGRAPHER: Okay.
MR. ERICKSON: Okay.
THE VIDEOGRAPHER: Off --
MR. ERICKSON: No, we are still on -- we can stay on the record. I just want to note that, you know, I would hope that the questioning is more tailored to these IPRs. There was a lot of questions about, for example, electrode. That is a term that doesn't even appear in any of these patents that I'm aware of.

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It is obviously a claim-construction dispute in other patents, in the other litigation between the parties, and I'm not sure what capacitive sensors have to do with these IPRs.

So I just wanted to note for the record that we request that counsel try to focus his questioning better on the issues on which Dr. Neikirk has applied in these two IPRs. That's all I had. We can go off the record now.

THE VIDEOGRAPHER: All righty. Off the video record at 10:52 a.m.

(Off the record.)

THE VIDEOGRAPHER: On the video record at 10:58 a.m.

BY MR. CUMMINGS:

Q Dr. Neikirk, did you talk with anyone during the break?

A I spoke to my wife.

Q You didn't speak with counsel?

A No, I did not.

Q All right. I'd like to turn to paragraph 25 of your declaration.

A I have it in front of me.

Q Do you see the drawing?

A The drawing on the page -- above paragraph 26

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on page 15? I do.

Q Yes. Did you prepare the annotations in this figure?

A So I -- I had assistance in -- in getting the graphic done; but the identification of the layers -- I don't know that I picked orange and yellow and green as the specific colors; but the identification of the layers that I wanted to highlight, yes, I participated in that. That -- those are the ones I wanted to be able to call out.

Q And is passivation layer 212 shown in white?

A I've got to refresh my memory as to which numbers correspond to what.

Q Okay. I believe it's --

A So --

Q -- in paragraph 27.

A Let's see. The layer 212 -- I'm just looking for it. Oh, there it is. Yes, I'm sorry. It's actually in paragraph 27. I was actually also going to check the patent. I think the cite there in paragraph 27 would be where I also would have gone.

But yes, 212, in that figure, I don't think it actually is colored white. I think the -- from the original patent document, that layer was white, and it simply was not changed at all.

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Q And second metal pattern 210B is annotated in blue; is that correct?

A Blue. There it is. Yes. I'm just double-checking the numbers. Some of these get kind of hard to see.

Yes, 210B is in blue.

Q Is second metal pattern 210B an organic or inorganic material?

A So 210B itself, if we look to -- so in my paragraph 27, but on the next page, page 16, I've identified second metal patterns 210A and 210B. So I indicate it's metal, which I believe also corresponds to the disclosure in the patent, and normally I wouldn't refer to a metal as an organic, although there are organic conductors, but I usually wouldn't call that organic conductor a metal.

Q And then 214C is an indium tin oxide; is that correct?

A So in my Figure 2 on page 15, 210C -- I'm sorry. 214C, you asked about, is -- I guess I describe what I'm looking at as a slightly darker blue. I'm sorry. Let me look at the PDF, as well. I have my printed copy, and then the colors are influenced by the inkjets.

And in the PDF, I think it shows up as a

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slightly darker blue, so that's 214C.

I don't believe I discussed 214C in paragraph 27 in my declaration, but -- that's white.

Q You could refer to paragraph 29.

A Yes. And in paragraph 29, where I do identify 214C, an anode, as being indium tin oxide, or ITO for short, yes.

Q Is ITO an organic material?

A No.

Q And referring to Figure 2, which is annotated on page 15, ITO pattern 214C connects to second metal pattern 210B through the passivation silicon nitride layer 212; is that correct?

A I'm sorry. You asked if 214C connects to what layer?

Q The 210B --

A Ah.

Q -- shown in blue.

A Yes, I just had to find the 210B. Yes, it does connect to 210B; and in that cross-section, there is indicated a -- if you will, a via or a pass-through or a hole that has to be made in layer 212. 212 is a silicon nitride layer, yes.

Q So how would that hole be made in layer 212?

A Well, the most common -- well, there are a

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variety of ways it can be made. A very common way would be to use an etching process to make a hole in a continuously -- in a layer, or a sheet, if you will, of silicon nitride that had been formed across an entire sample. So you would use potentially probably photolithography and etch to make that hole.

There are other methods besides etch. You can use laser ablation. You can use a laser-driven plasma etch. There are some others, but the most common would be to form a photolithography pattern, use that as a mask for an etch.

Q Are there any difficulties in etching a silicon nitride layer?

A Etching silicon nitride is very common. I wouldn't say it's more difficult than etching many other layers. Each layer requires a proper etchant chemistry and environment. Doing silicon nitride is no harder or easier than many other things. You do them -- do many different layers in an integrated circuit or a multi-layer -- multi -- multiple-layer system or device.

Q Can you step me through, layer by layer, how Figure 2 would be manufactured?

A Well, I can certainly identify a set of processes that could be used. Not necessarily the

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only.

Typically, you start at the bottom and work your way up. The first layer most likely would be 202B. That would be deposited, and then a photolithography-and-etch process used to form the desired pattern in 202B.

It would be overcoated with layer 204. Again, poten -- quite likely photolithography and etch would be used to make the desired pattern in that layer.

Looking at the stack -- have to check for 206A and B. Look at those two. 206A.

No, on paragraph 27 I identify what 206A is. I use light green. It is a metal pattern.

The layer 206B is darker green. Let's see.

So in paragraph 27, on page 16 of my declaration, again this is all from the patent, from the 1 -- from the '121 patent. It states that it's possible that the metal pattern 2 -- 206A could be formed -- 206B.

So that -- the first sentence there, which I think is coming from column 4, 66, through column 5, line 11, in the patent itself, indicates that those two could be the same metal. If they were the same metal, you could do a blanket deposition of that

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metal, all the way across -- let's see. I'd gotten you up through layer 204.

So the material for 206A and B could be blanket deposited. Photolithography could be used -- photolithography and etch to produce the desired pattern.

The next layer in this proposed process sequence would be 208. A blanket deposition followed by photolithography and etch to provide -- to produce the desired pattern.

The next layer, 210A and B. 210A is referred to as the second metal pattern, and 210B is also second metal pattern. So a simple way to do that would have been a blanket deposition across everything, followed by photolithography and etch to produce the desired pattern.

The next layer would appear to be 212 or -- not layer. That's claim language, about "sheet."

212 is -- that sheet would be 212. I did not color-code, and I'm not sure I called that one out directly in this section of my report; but going to the patent, 212 is described in column 5 at line 40 as being a passivation silicon nitride film. So a blanket deposition of film 212, followed by photolithography and etch to form its desired

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pattern.

The next layer would appear to be 214C probably. So 214C. I think we already talked about that, but that is -- that's the darker blue.

There it is. It's paragraph 29, of my declaration, page 17. 214C is identified by the patent, but I have explained it in my declaration as an ITO pattern. So a blanket deposition of a sheet of ITO followed by lithography and etch to pattern -- to produce the desired pattern in that layer.

The next layer would appear to be, I believe, 216. Or sheet. I want to be careful about not using claim language.

216 is a sheet, that could be deposited as a sheet. It is -- 216.

Again, I didn't separately color-code that one, but it's identified in the patent, and I discussed it in my paragraph 27 as "capping silicon nitride." So a blanket deposition of that sheet of silicon nitride, followed by lithography and etch, to produce its desired pattern.

The next indicated number is 218. I believe we just did 216. Yes, 218, which I highlighted in yellow in that figure above paragraph 26.

218 is identified by the patent, and I

pointed this out in my paragraph 27 as an organic layer. So that would be another blanket deposition; and if there was need to form a pattern in that, lithography and etch would be done.

In the particular cross-section we use -- we see in Figure 2, there is no pattern obvious, but there might be some regions where it is removed.

Then the next sheet, or next number, is listed as 220, which I did highlight as orange, called it out in my paragraph 27. The patent identifies as being a third metal layer, so that metal would be blanket deposited, and whatever desired pattern would be formed using lithography and etch.

So that -- that would be a sequence of process steps that could produce something as shown or illustrated in Figure 2.

Q And you made some distinguishment between the term "layer" and the term "sheet." Can you explain what the difference would be, if any?

A Well --

MR. LONEY: Object to form.

THE DEPONENT: "Layer" is a claim term, and the patent itself gives examples where something that is called -- that it calls a layer is actually made

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of two other lay -- in fact, I believe it says two -- two layers of material.

It -- it -- there are other places in claims, for instance, where it says "a given layer comprises," and then it gives an example. Of course "comprises" means it could be more than one thing.

So I was trying to distinguish. You asked for a process flow; and if one of these layers in Figure 2 is actually made of more than one layer, there would have to be more than one sheet deposition -- blanket sheet deposition.

So I was trying to use a -- a word about the processing step. So I called -- I think I tried to -- tried to consistently -- I probably wasn't completely consistent -- but I tried to refer to it as a blanket deposition of a sheet.

So you think of something that covers everything at that point, whereas I want to be careful about the word "layer" because it's a claim word. It's a word in the written description of the patent that has other explanations about it that might -- you know, process flow -- require the deposition of two blankets. So that would actually be two steps. Not one.

Q Is the term "layer" normally used in the art?

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A It's a word, again, that's very context-sensitive. "Layer" will have a meaning to one of ordinary skill. It has a plain and ordinary meaning in the context in which it's used. So I -- I can't give you a universal definition of that word. I need to know the context.

In this patent, it -- the context is made clear as to what "layers" -- what that word indicates to one of ordinary skill.

In a different patent, it might -- one of ordinary skill might very well understand it to be something different.

Q All right. Let's take a look at paragraph 44 of your declaration. Can you let me know when you're there?

A I'm at paragraph 44.

Q Towards the end, you state that first 17 and second 19 planarization films correspond to a second dielectric layer; is that correct?

A I'm sorry. I have to find -- could you read that quotation again? I -- I think I found mine in the paragraph.

Q "A second" -- quote, A second dielectric layer, parentheses, first 17 and second 19 planarization films, end quote.

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A And I'm sorry; I'm having a hard time spotting this in that language. In paragraph 44. I don't suppose you happen to know how many lines down in 44 you started that. It would speed it up.

Q It's the third from the bottom is where it starts.

A The third from the bottom. Okay. "A second dielectric." I've got it now, yes.

And yes, that was a direct quote from -- from what I have there, yes.

Now, to be clear, the parentheticals are mine. The words not in parentheses is a direct quotation from element 1C of the '121 patent, just to be clear.

Q So it's a -- your understanding that first 17 and second 19 planarization films, of the reference you're applying, corresponds to the claimed second dielectric layer?

A Yes, that is correct. So 17 and 19, we can see them illustrated in a cross-section on the next page, from the reference from Anzai. We're discussing Anzai here.

So 17 and 19, in my opinion, would constitute the second dielectric layer as required by element 1C of the '121 patent.

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Q Okay. I'm going to mark the Anzai reference as Exhibit 2 and put it in the chat. Can you let me know when you have that open?

A I will. I'm going to try and open it now.

And yes, I have it open. For clarity, the document I have says at the bottom "Exhibit 1003."

Q Yes. It is Exhibit 1003 in IPR2024-01132 marked Exhibit 1 in this deposition.

A Okay. I just wanted to make sure I had the right document. I do have it.

Q You annotate Figure 2A of Anzai in paragraph 45 at the top of page 23 of your declaration; is that correct?

A Yes, that is correct.

Q Did you make these annotations yourself?

A Again, I didn't actually put the colors on this figure, but these are the layers that I wanted to call out.

Q Did BOE's counsel annotate these figures for you?

A Well, I had counsel's assistance in doing the graphics. So yes, they did the graphics necessary to add those colors to those layers.

Q And in Figure 2A at the top of page 23, you did not color layer 17 or 19; is that correct?

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A That's correct. These are the figures as they stood. I mean, just for -- for the purposes of being able to read the figures 17 and 19, they are quite easy to find, even without colors.

Q What does Anzai call layer 17?

A 17 itself, in Anzai, I believe in paragraph 46. Yeah. So this is a cite, too.

So in paragraph 46, there is a cite to Anzai and followed by a quotation, which is a quotation from Anzai, the site locations.

And you'll notice that at the top of page 24, Anzai identifies first planarization film 17 and second planarization film 19. So that's what it identifies 17 and 19 are, at that particular point in the -- further specified them as being capacitance-insulating film.

THE STENOGRAPHER: As being the what?

THE DEPONENT: Sorry. As being the, to quote from Anzai, capacitance-insulating film in this configuration.

So they are identified -- 17 and 19 are both identified as planarization films and that they function as the capacitance insulating film.

BY MR. CUMMINGS;

Q Does Anzai disclose what material is being

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used for these layers?

A Yes, I believe Anzai does. Let me just -- oh. Let me -- you gave me Anzai electronically. I'm sorry. I don't have that on paper.

Let me -- so you asked about -- to be clear, are you asking about layers 17 and 19, just so I am sure I know what layers you're asking about.

Q (Moves head up and down.)

A So I believe what I quoted in my paragraph 46 was in -- no. That isn't -- there is a -- it's another place where it mentions planarization films. That's in column 4. Let me keep looking.

17. So for instance, in Anzai, column 5, starting at line 3, it states, to quote, "Furthermore, the first planarization film 17 made of an organic resin for flattening the surface is deposited on the entire surface." So there is a spot where it identifies a possible material choice for film 17, an organic resin.

Q What is a planarization layer?

A Broadly, a planarization layer is a sheet -- I'm going to sound -- of course, let's be careful about the use of the word "layer" again. Anzai is a slightly different context than the '121.

So a planarization -- it actually calls it a

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planarization film 17, not layer, but that film is one that is deposited and, if necessary, further processed so that its top surface will be relatively flat.

Q How is a layer or sheet planarized?

A There are a number of ways that you can take a film that -- whose surface is not flat and make it flat. You can use polishing processes. Broadly, people tend to refer to those usually as chemical/mechanical proc -- chemical-mechanical polish processes. Very common in the integrated-circuit world.

You can, for some materials, heat the sample enough to cause what's called reflow. That was a technique that was used from, I believe, the seventies, on. Certainly I was aware of it in the early eighties.

You can use the flow properties of the material, combined with surface-tension effects, to try to cause the surface to be flattened -- flatter or flattened.

So there is a number of ways you could do it.

Q Can you describe what a polishing process is?

A Polishing usually refers to a mechanical process, where you bring a surface into contact with

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a -- an abrasive polishing compound and, when done properly, it first removes high points through a mechanical abrasion and, in chemical-mechanical polish, a combination of abrasion and chemical etch; and if controlled carefully, you can do that long enough to where you end up with a surface that is much flatter than it originally was.

Q And can you describe reflow briefly?

A In reflow, it normally refers to a situation where a film is present. Its surface is not as flat as you might like it to be.

Through usually a heating process, you heat the material above its glass-transition temperature; and under those circumstances, it will flow, like a viscous fluid, and the -- that tends to eliminate sharp corners. It tends to flatten out the surface because surface tension wants to minimize surface area.

Q Can you think of any other techniques for planarization?

A So polish and flow are the two techniques I have used and the ones that I certainly used to teach in my course.

There are tricks to do that in a more localized fashion. You can sometimes use a

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straight-etch process, but usually that doesn't work all that well because you tend to etch everything.

And those are certainly the two that I'm most familiar with.

Q Is one method preferred over the other for an organic resin?

A Not necessarily, no. I mean, that -- organic resins may, in some cases, be easier to reflow than other inorganic films, in which case, for an organic resin, your choice to use reflow might be enhanced, easier.

But when people do -- chemical-mechanical polish is very popular now because it's such a good way to do what's called global planarization, for a very large wafer.

The reflow processes make a surface more planar, and you would still call that a planarization film, but they can be trickier to get them to be as flat. It depends, on the application, whether you care or not.

Q You mentioned that chemical-mechanical polish is very popular now. When did chemical-mechanical polish become a viable manufacturing technique?

A IBM was using it in their manufactured product lines in the eighties. It absolutely became

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much more widely used by many other companies in the nineties.

Q Is there any difference between a planarization layer and a passivation layer?

A Well, I believe in -- no, let's see. In the '121, I believe "capping" and "passivation" are used. I'm not sure "planarization" is used.

Not necessarily. A film could do -- have multiple functions. Given that the '121 actually doesn't call out any special characteristic that it's passivating for, I believe that Anzai's planarization films could act, would act as a -- as a passivation layer.

It typically means to protect the surface that's underneath it, and Anzai 17 and 19 would do so.

Q Are the terms "passivation" and "planarization" synonymous?

A No, I don't think they are necessarily synonymous; but in many cases, the same sheet of material can perform both functions.

Q Are there cases where the same sheet of material would not perform both functions?

A Well, if the -- if the context specified the -- I'm going to use the word "specific" twice. I'm

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apologizing. If the -- if the situation or the -- the art were to identify the type, its passivation more narrowly, and say, for instance, passivation of a silicon surface to prevent dark current, well, there are certainly films that you could deposit on a silicon surface that could be used to planarize that would not necessarily passivate that silicon surface with respect to dark current.

There are other film choices that might, or would. Again, I point out the '121 doesn't state that -- the kind of passivation it's referring to. It just says "passivation" broadly.

So yes, there are certainly some circumstances, depending on context, where passivation might be defined as being a very specific result, and then the choices for films to do that would be potentially narrow.

Q Are the terms "capping layer" and "planarization layer" synonymous?

A Again, I would say that they might be done by the same layer, but would not necessarily.

A capping layer in the '121 patent, again, there is no special explanation of what kind of capping; but in the sense of covering over structures below, then as an example, Anzai's 19 certainly caps

everything that's in that -- Figure 3A is illustrated as capping everything that's below. It covers over.

So a planarization layer might well be a capping layer.

Q Well, let's look then at Figure 2B or 3B. You've annotated them on page -- on the top of page 29.

A Yes, I'm on page 29. I see the two annotated figures.

Q These correspond to a different portion of Figures 2A or 3A; is that correct?

A So let's see. So if you look at -- let me look at Anzai real quick here. 2B.

Okay. So on page 29, I have 2B and 3B. So these are cross-sections, and they -- what you have to be a little careful about is the cross-sections in Anzai.

If you look at Figure 1, you'll see a cut line. So in Figure 1 of Anzai, it's kind of hard to pick out; but if you look horizontally, on the left, look for the letter, capital "A," and then you'll see sort of a long-dashed, short-dashed line, that extends across horizontally. Then it turns at a right angle and goes down.

So these cross-sections are actually laid

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along that line that's not straight. But you have to be --

Q Did --

A I'm just trying to be a little careful about what we're seeing in these. And that's true, I believe, for all of them. For 2B, 2A.

Let's see. 2B is in a different location. Let's see. Where is that.

Q But the figures are referring to the same layers?

A The -- the -- so 2A and -- just a second. 3B.

So in that Figure 1, there is another cut line that's labeled "B to B," and you notice that that goes through -- they are transistor regions -- that are labeled 43. Those show up in Figure 2B and 3B; okay? And that cross-section is just straight across.

It's the "A" cross-sections that you have to be a little bit more careful about. Those show up in Figures 2A and 3A.

I just needed to -- the 2B's -- 2B and 3B, the cut line in Figure 1 is supposed to be that "BB" cut line. It is just straight across. So it's a little simpler.

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Q Thank you for that clarification. Are the layers in Figure 2A and 2B referring to the same layers?

MR. LONEY: Objection. Form.

THE DEPONENT: So for instance, in 2A and 2B, you have some layer numbers that are the same as the layer numbers in 2A, and they do refer to the same -- well, Anzai refers to them as films. They do refer to the same films, the same numbers.

There are some shown in 2B that you do not see in 2A. The numbers -- the 60's, for instance, show up in 2B. They don't show up in 2A.

BY MR. CUMMINGS:

Q But planarization layers 17 and 19 are present in both figures; correct?

A They are. I'm sorry; I apologize for speaking over you.

Yes, 17 and 19 appear in both Figure 2A and 2B.

Q Does 19 cover all of the elements in Figure 2B?

A It doesn't.

Q Is there any difference between a passivation layer and an insulation layer?

A Yes, there can be. Sometimes the same film

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can do both, but there are other circumstances where passivation layers aren't made of an insulator.

Q Can you explain that distinction a little more?

A Well, earlier, I mentioned a specific type of passivation with respect to dark current in -- due to a silicon surface, and one passivation layer is another doped layer of semiconductor. That's not an insulator.

Q What is a doped layer?

A A doped layer -- well, I was referring to a doped semiconductor layer. Well, ex -- again, let's not use the word "layer" because that's not the layers that we're talking about on the '121 patent. A film made of semiconductor with additional electrical dopants in it. That's a doped semiconductor film.

Q What properties does a doped semiconductor film have that make it desirable?

MR. LONEY: Objection. Form.

THE DEPONENT: Well, desirable -- desirable in what? Desirable in a -- in a MOSFET? You have to have a doped source and drain or you can't make a MOSFET.

BY MR. CUMMINGS:

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Q Why is that?

A Well, a MOSFET has -- must have a source and a drain. It's a four-terminal device, two of which are -- one is a source and one is a drain, and that requires doping a semiconductor film to form that source and that drain. It -- you just can't build it without those.

Q All right. Looking at Figure 2B of Anzai on page 29, can you walk me through how this would be fabricated, or an example process?

A I want to look. I think Anzai may actually do this. Anzai has a little bit more in terms of step-by-step processing. Let me look and see.

So you're asking about 2B. So broadly, if you look at Anzai itself, starting at -- let's see. What's a good place to pick as a starting point?

Roughly, say, starting in column 3 in Anzai, at line 57 I believe, continuing all the way through column -- I think it would be appropriate to go probably to column -- all the way through column 5 at line 30 -- all the way to line 33. The entirety of that is a layer -- or a sheet-by-sheet or film-by-film. I believe Anzai uses, in many cases, the word "film."

And it goes through a film-by-film process

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where it identifies when a film would be -- where it would be placed. It identifies -- let's see, column 4, what those films or layers do.

I think it identifies formations of -- of patterns in those films and so on.

So in Figure 2B, for instance, what's labeled as "10" is discussed in column 3, lines 61 through about 64 in Anzai, and specifies that when a conductive substrate or a semiconductor substrate is used as the insulating substrate 10.

So 10 is referring to the -- if you will, the bottom, the thing on which everything else is built.

It specifies that the next layer -- or next film, it says, "Insulating film 12, such as SiO2 or SiN should first be deposited before forming the TFTs."

So you end up -- it says, "Start with the substrate tin, deposit a film 12." Let's see. Let me back up.

Film -- let me find -- you're asking about 2B. So let me find what -- there is a film there that has 43s called out for it, and it generally describes what those things -- that the 43S, 43D, source and drains of a TFT. That's in column 3 of Anzai. I'm trying to find whether it calls out the

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layer -- or the sheet -- the film deposition step for that one.

And I don't think it does, although what I just pointed you to at the bottom of column 3 states that before you form the TFTs, you would place this insulating film 12.

So deposit film -- well, that goes over. So that's -- that's before you put the gates down. So you deposit -- well, you have 10. You have -- the way 2B is illustrated, you would deposit a layer -- a film that would be then patterned to form those structures that are labeled as 43S, C and D. All that is labeled 43. So that would be a deposition step.

There. It calls it out in Anzai column 4. These are the 43s. Yes. Line 52 and following. This is a polycrystalline silicon film 43. That would normally be blanketed deposit -- blanket deposited and then patterned using lithography and etch.

It's then -- as Figure 2B is drawn, there would be a blanket deposition of film 12.

There would then be a blanket deposition of the film that is patterned to form the elements 41, in that cross-section. Those are gates. It would be

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covered with the blanket deposition of film, or could be. This is one process flow.

Blanket deposition of layer -- of film 15. That's described -- let's see. 15. I'm looking at the text of Anzai.

I'm not sure -- I'm not sure it actually calls out film 15 specifically; but given where it is in that figure and its stack-up, I would expect 15 to be an insulating material.

There would then be photolithography and etch to form holes through 15 and 12, down to 43. There would be a blanket deposition -- let's see. It's going to form after patterning 53 and 56. Yeah, and I'm not sure.

There is -- so it does describe 53 as a driving source line, and 56 as a source electrode formed by filling a contact hole. So that's -- that would be a deposition.

It does give an example. Could be aluminum. There would have to be a lithography step to pattern that. And based on the stack-up, there would be a blanket deposition of layers 17 -- of film 17.

There would have to be a lithography and etch to open a contact hole through it. Most likely, then, a blanket deposition of film that makes up 61,

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followed by lithography and etch, followed by blanket deposition of film 19, followed by lithography and etch, A blanket deposition of 62.

62 itself, in Figure 2B, you can't tell whether there is a pattern formed in it or not. 62 -- I'm sorry. We're up to 62. I'm sorry. I'm just checking. I'm looking at Figure 1 of Anzai, the top view, to see if I see 62.

I'm not immediately seeing 62. I would have to do a little bit of digging to see whether 62 requires lithography and etch.

The next layer -- the next film is 63. I would expect that would be blanket deposited and etched -- lithography and etched to form its desired pattern.

There is 64, which would be another film. 64 itself is an electron transportation layer. That's in column 5 of Anzai.

Again, it's not shown that it has been patterned in Figure 2B. I'd have to take a look to see whether it would -- whether I believe it would or would not need lithography and etch.

And then the last layer shown is 65, and 65 is a cathode layer which is called out in column 5.

Q And where in that process does the

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planarization step happen for film 17?

A Well, Anzai says that 17 is a planarization layer. He doesn't -- doesn't give -- as I've just pointed out, he actually didn't give every single step. He didn't call out how that planarization is performed.

Q So if you were going to reform 17, when would that need to take place?

MR. LONEY: Objection. Form.

THE DEPONENT: Well, if you -- if you were going to do a reflow-type planarization, you would do that after you deposited layer 17 -- or film 17. Anzai calls them films.

It would be after the first planarization film 17 is depos -- deposited over the films that have already been patterned. That's why you end up with topography. So you flatten it before you add the next film, which in the stack-up, I believe, would be 61.

BY MR. CUMMINGS:

Q So the planarization step takes place before you add the next film; is that correct?

A Normally. Sometimes people will form a -- a contact hole or via before they do planarization. That's a possible option. But a pretty common option

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would be to flatten it before you create any patterns in it.

Q And that holds true for reflow and polishing?

A Yes, although -- well, I would say that if you're polishing, it would be more common to polish before you open any -- make any openings in the film you want to flatten. For polish, I think that's probably more common you do it before, but it's not universal.

Q And just to be clear, we're referring to flattening layer 17 and how that's planarized?

A Well, yes. Anzai describes film 17 as being a first planarization film, and so the step -- the processing step to try to make the surface of 17 flatter, in other words to be planarized, and planar -- to be clear, planarization doesn't require perfect flatness, normally. It rarely is. But to make it flatter, you would do that step normally before you put anything on top of that.

Q And the same is true for planarization film 19?

A Yes, that's correct.

MR. CUMMINGS: All right. Why don't we go off the record and take a break if that's all right.

THE DEPONENT: Okay. Five minutes?

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MR. CUMMINGS: Yeah. We can discuss how long off the record.

THE DEPONENT: Okay. I -- I will come back in five to find out what happens. Okay.

THE VIDEOGRAPHER: Okay. Off the video record at 12:06 p.m.

(Off the record.)

THE VIDEOGRAPHER: On the video record at 12:14 p.m.

BY MR. CUMMINGS:

Q Dr. Neikirk, did you talk with your counsel during the break?

A I did not.

Q All right. I'd like to move to ground 2 in your declaration which starts at paragraph 69. Can you let me know when you're there?

A I am there.

Q Here, you rely on the Yamazaki reference, which I'm going to introduce as Exhibit 3 of the deposition. Can you let me know when you have that open?

A I have it open.

Q In paragraph 72 of your declaration, on page 36, you provide an annotated Figure 2 of Yamazaki; is that correct?

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A Yes, it is.

Q You've annotated a first area, a second area and a third area. Do you see that?

A Yes. Right there.

Q There are several areas that are not labeled. Do you see those?

A I do.

Q What are those areas?

A Well, starting to the left, which Yamazaki calls out with the letter -- or the number "7" -- I'm just looking at the written description for Yamazaki. Let's see.

Yamazaki in column 9, line 1 through 4, states that the referenced numeral 7 denotes a connecting region for making connection between an upper electrode, common to the light-emitting elements, and wiring on the substrate.

So it's a -- it's a region where electrical connections are being made. Let's see. The region between what I have annotated as first and third regions -- or areas, areas, in large part corresponds to what Yamazaki labels as 40.

And Yamazaki refers to 40, at the bottom of column 9 and continuing to the top of column 10, as being the switching TFT.

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And looking at that, what -- Yamazaki has a little set bracket with "40" underneath it. I can see within that, for instance labeled as 44s, those appear to be gates. 50d and 50c certainly look like they correspond probably to sources and drains. I'd have to go through.

But that that corresponds to a region where transistors are formed, switching TFTs in particular. That fits the diagram.

It just so happens that Yamazaki extends that set bracket far enough to, broadly speaking, include this via that he labels 47-48 which are to make electrical connections to -- let's see. 47 and 48 are -- let me make sure that's -- that's that.

Simply looking at the figure, they look like the connections down to the TFTs. I was looking in the specification of Yamazaki to see if it calls out what 47 and 48 specifically are.

So I see one reference that would include 47 and 48. Yamazaki column 19, starting at line 53, talks about electrodes 23 to 27 and 46 to 48, and then identifies metals that could be used to form those. So broadly speaking, he's referring to 47 and 48 as electrodes.

And then the next area I have annotated is

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third area. The next is secondary. So those are the only areas that I didn't include was Yamazaki 7 and basically Yamazaki 40.

Q Looking at paragraph 74 now, you point to insulation layer 30 as teaching that silicon nitride is a suitable material for insulation 30; is that correct?

A Yes, that -- so paragraph 74. And yes, those citations in Yamazaki are about -- there may be other layers that, specifically, they are about: layer 30 and a teaching of how to flat -- how to make the top surface flat.

Q And the teaching of how to make the top surface flat refers to chemical-mechanical polish; is that correct?

A Yes. In Yamazaki, I know he certainly does mention -- and I don't remember whether he calls it CMP. Let me look at the citation I have of column 20.

Yes. So in column 20, at lines 17 and following, it states, "In addition for flattening the surface." Now, that one says they are talking about 28a, but that one mentions, "Any flattening process, such as CMP, may be formed" -- "may be performed."

And it calls out, "After formation of first

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load 20" -- "electrode 28a or after the formation of an insulating material 30."

So it's explicitly stating that to flatten 30, you can -- could perform CMP, and that's an example. "Any flattening process such as CMP."

It goes on to make some comments about other films, such as 22, that might be desirable if you're going to do CMP with 30, but not required.

Q Would it be possible to use reflow with 30? Is that one of the "any other flattening processes" that Yamazaki describes?

A So I don't believe -- I think Yamazaki only points -- points to any flattening process and then gives, as an example, CMP.

I don't think Yamazaki happens to point to a reflow process, although he does state that 30 may be formed of an organic resin or an insulating film, including -- including silicon.

So it -- for instance, that word is going to mention -- that's for 30. So he mentions an insulating film including silicon. Well, silicon nitride would be such a film.

I think there is a -- there was another spot where it's -- it actually lists silicon nitride as an example material.

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I'm sorry. This is 30. 11. So that's actually earlier than where I am right now.

So back in column 11, Yamazaki points out that insulating material 30, and he gives a relatively long list of materials that could be used, including photosensitive or non-photosensitive organics or -- keep reading down.

I think we need to go on to -- what's that? Oh. Yes. I'm sorry. It's right there. Line 48, "The insulating material 30 may be an inorganic material such as silicon oxide, silicon nitride or silicon oxynitride" -- "nitride."

So all of those are things that Yamazaki indicates you could use for 30. And as an example, again we were talking about CMP, he states you can use any flattening process and then it's a "such as CMP."

So I don't believe Yama -- Yamazaki explicitly states -- gives examples of other flattening techniques. It clearly indicates you have choices. CMP is one, and that's the one he mentions in his words, "Such as CMP."

Q Would you use reflow with a silicon nitride material or just CMP?

A Broadly, I would normally not expect to use

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reflow with silicon nitride. The glass-transition temperature for pure silicon nitride is relatively high. It's actually pretty common to use a doped glass and reflow.

Those are usually oxynitrides, which is another example that Yamazaki gave earlier; but for a pure nitride, probably not.

Q Is there a difference between a gate oxide layer and an oxide layer?

A Not necessarily. A gate oxide layer refers to an oxide placed in a specific location relative -- in a MOSFET normally. Normally between gate and channel.

Q Is there any difference with how that is formed?

A Not necessarily.

Q All right. I'll move on to paragraph 110, and this is in ground 3 now.

A Okay. I'm at paragraph 110.

Q So here, instead of modifying Anzai with Yamazaki, you're proposing to modify Yamazaki with Anzai; is that correct?

A Just one moment.

3. So yes, that's correct. Yamazaki -- in ground 3, I've identified Yamazaki as, to use the

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euphemism, the primary reference, and it's done in view of Anzai.

So yes, paragraph 110 and this whole section, that's the analysis on it I'm doing.

Q So in paragraph 111, you provide an annotated Figure 2 of Yamazaki; is that correct?

A Yes, it is correct.

Q How would you modify this figure in view of Anzai?

MR. LONEY: Objection. Form.

THE DEPONENT: So the claim element we're talking about, and we're talking about claim 3, and claim 3 itself requires device of claim 1, wherein the second dielectric layer, which in analyzing Yamazaki, in my opinion, would correspond to material 30 in that Figure 2, comprises a passivation layer. Again, in my opinion, that would be insulating material 30 in Yamazaki. And a capping layer.

So in claim 3, there is an example where there is one thing described as a die -- a second dielectric layer, that comprises, so it has at least two other layers within it, a passivation layer and a capping layer.

And if we look to Anzai, he uses examples where there are two layers used, and so the -- that's

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-- let's see. This is -- if you skip forward to paragraph 116, I discussed those first and second planarization layers.

So in paragraph 118, the combination, really, is to add planarization layer 19 from Anzai to be on top of insulating material 30.

And I point out before that, in the preceding paragraphs, that in fact, Yamazaki itself has shown examples, Figure 15A on page 61, where Yamazaki already added a layer on top of what would cor -- or a film on top of what would correspond to film 30.

So this is a combination that is actually already, if you will, hinted at, one of ordinary skill looking at Yamazaki, seeing the structures, seeing the layers, seeing and teaching where there are two layers, would be motivated, in my opinion, to look to other references where two layers are used. And Anzai is such an example.

Q So adding another layer to Figure 2 on top of layer 30 is what you're proposing?

A So be -- in that process sequence -- remember, we got to a step of a blanket deposition of 30, before adding 32. You would simply do a blanket deposition of 30, followed by what Anzai referred to as its -- let me find that. Planarization layer -- I

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believe Anzai calls it planarization layer 19. Let me go back to Anzai again and make sure I've got the right number.

Q I believe you do.

A Yeah. Yeah, 19. Yes.

So, yes, you would do a deposition, put down 30, put down 19.

30 itself, you might well do -- depends on what materials you choose and what planarization techniques you use, but you might planarize 30 and deposit 19.

If 30 was already planarized, 19 still remains planar. It's still a planarization layer but might not require additional planarization.

Then you would define the pattern in Figure 2 of Yamazaki.

If you look at those dips, if you will, in the orange layer, where it goes down, you would do that lithography on the combination of 30 and 19 -- the lithography and etch -- to open those windows.

And then you would simply follow it with -- I believe the next layer in sequence is the yellow layer 31 -- or next film is yellow film 31.

And then I think the -- there is a lithography and etch step of that, and then 32 and

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lithography and etch.

MR. CUMMINGS: All right. I believe that's all I have for the '121 patent at this time.

Zach, do you want to do the redirect now or do you want to do it combined with the '477 patent?

MR. LONEY: We are -- we are going to wait and do our redirect on both patents at the end.

MR. CUMMINGS: Great. Do you want to go off the record and take a lunch break now?

THE DEPONENT: That's fine with me.

MR. LONEY: Yep. Let's do it.

MR. CUMMINGS: All right. We'll go off the record.

THE VIDEOGRAPHER: All righty. We're going off the video record at 12:38 p.m.

(Off the record.)

THE VIDEOGRAPHER: On the video record at 1:28 p.m.

BY MR. CUMMINGS:

Q Dr. Neikirk, did you talk with counsel during the break?

A I did not.

Q Now we're going to be talking about IPR2024-01315, and this covers patent number 8,158,477, which we'll refer to as the '477 patent.

Do you understand?

A I do.

Q All right. I'm going to mark your declaration for the '477 patent at Exhibit 4 and put it in the chat. Can you let me know when you have it open?

A Well -- and I do have it open.

Q All right. Looking at paragraph 5, your background and qualifications are the same as your previous declaration?

A Yes, they are.

Q And your definition of a person of ordinary skill in the art is the same?

A Yeah, I believe it is. I -- you know, I noticed -- I'm trying to look to see if there is maybe one word that is different. I don't think that there is any difference of any matter; but if we compared it, there might be one word that's different. Let me -- let me look.

Page 14.

I -- it's certainly for -- it's -- in terms of any words that matter, it's identical, and it may very well be absolutely identical. I couldn't recall whether there was one word that changed somehow or not.

Q Is it your understanding that the '477 patent and the '121 patent are in a related family?

A Yes, I do.

Q Or are in the same family. Sorry.

A Excuse me. Yes, I do understand that.

Q And you rely on several of the same references in the '477 patent as you do in the '121 patent; correct?

A Yes, that is correct.

Q Beginning with paragraph 57, this is your ground 1. Can you let me know when you're there?

A I'm there.

Q Is your understanding of Anzai the same in the '477 patent as it is in the '121, or are there any distinctions you would like to make with respect to its teachings?

MR. LONEY: Object to form.

THE DEPONENT: Let me -- let me look. In general terms, of course Anzai remains Anzai. There was -- let's see.

For previous document, there were certain regions that I focused on. I -- if I recall correctly, for the '171, there may have been a bit more focus on one transistor versus -- I'm trying to recall.

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It seems there was some discussion, I think, that tended to focus a bit more on the access transistor as opposed to the drive transistor in the '477. I believe there is a bit more focus on the drive transistor.

So there may be some slightly different focuses; but in terms of the teachings of Anzai, that hasn't changed, and I haven't seen any -- there is nothing different in that sense.

BY MR. CUMMINGS:

Q And when you refer to the drive transistor, what structure are you referring to?

A Let me look here real quick.

So in the '477, in the claims, there is a requirement for first area -- let me find it. First area. First area.

Actually, I'm -- I'm looking at the claims of the '477 right now; and in claim 1, for instance, there is a first area, a required second area, and a required -- it was required earlier. Give me just a moment.

No, first and second areas.

For instance, on page 25 of my declaration, I've identified second area and a first area in plan view in the figure just above paragraph 61. And the

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orange rectangle there is calling out a second area, which claim 1 identifies as a second area for a transistor on the substrate.

The transistor that I'm discussing there, transistor -- broadly, I'll call it transistor 41.

If you look back on the electrical schematic on page 22 of my declaration, for the '477, you'll see that transistor to the right. That is a drive transistor for the LED.

The other two transistors, which let's call 31, for simplicity, are access transistors. So the area that I'm going to look at and explain its presence in Anzai corresponds to the drive transistor, just to give it a name. But it's the region that contains the transistor 41.

Q Referring to paragraph 66, you talk about an alternative read on Anzai. Can you explain what the distinction is with this read?

A One moment to read through that paragraph.

So this is the section about element 1b and, in particular, is looking at the required -- requirements from the '477, claim 1, defining at least the first area or -- and a second area.

So in paragraph 61 through 65, I was discussing the different regions that could satisfy

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that.

In paragraph 66, I'm simply pointing out that it's an obvious design to place Anzai's stacked capacitor in -- let's see. There -- there are some layers -- some films, layers, that are common between the areas, and a POSITA would know that you have a choice between adding layers and then you could end up with some of these components overlapping in the same area, or you would actually just simply put them in separate areas.

Anzai's Figure 1, for instance, puts them in separate areas. And so I'm simply pointing out that it's obvious with Anzai that you would -- that you could and would put them in separate areas. It's -- it's both disclosed and obvious.

Q Looking at paragraph 67 now, you map Anzai's electrode layer 54 to be the, claimed, first conductive layer. Do you see that?

A Yes.

Q What is electrode layer 54?

A So 54, you can see it in the cross-section, and I'll -- it's -- it has a shape that you might call a plate.

If you look at the plan view, back on page 25, you can identify where 54 is. It's, roughly

speaking, rectangular. It has extensions from either side of it, as well; but roughly speaking, it is a rectangle. So that object that makes -- this is Anzai. So let me open my copy.

So Anzai was Exhibit 2, I believe. And we're discussing 54.

Anzai itself describe -- shows -- let's see where it discusses that.

In column 4, for instance, at line -- I think it's 28. It starts at 28. It says, "The second capacitance electrode layer 54." So that is a plate that is forming part of the capacitor.

Q Is there a term for a plate that is forming a part of a capacitor? Is that known as an anode?

MR. LONEY: Objection. Form.

THE DEPONENT: So not normally. Anzai itself uses the word "electrode layer." And I think we talked about electrode this morning. That's a term that is quite broad, and it depends on the context -- context. It's not unusual to refer to one of the conductive parts that provide area, in a capacitor, as an electrode.

It would only be called an anode if you were using a capacitor that is polarized; okay? Anode is the positive terminal. This capacity -- these

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capacitors are unlikely to be polarized. Many, many capacitors are not.

And so the -- the various conductive structures that provide the area of the capacitor, it's only in a polarized capacitor where one of them would actually be called an anode.

BY MR. CUMMINGS:

Q I think I see. So the -- the surface area of the capacitor is the electrode?

A Well, so --

MR. LONEY: Objection. Form.

THE DEPONENT: -- the electrode, as used -- as the term is used in Anzai, is this is a conductive structure which is providing space, area, upon which charge will reside when a capacitor is charged.

BY MR. CUMMINGS:

Q Earlier we talked about how one would form the structure of Anzai, an exemplary process. That's the same here, as it was earlier, isn't it?

MR. LONEY: Objection. Form.

THE DEPONENT: It would certainly be -- I don't remember which example I gave you. I think I walked through the -- the stack-up. I don't remember whether I used 2A, but I probably did.

And for -- then that stack-up would still be

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the same if the reference figure is 2A.

We did, I believe, discuss different embodiment this morning. Let me just use Anzai -- Anzai itself.

So for instance, I -- I think we may have talked our way through the layer-by-layer -- or the film-by-film of Figure 2A.

We may also have done 3A. I've forgotten whether we did both.

Obviously there is -- there are more films in Figure 3A than there are in 2A. So there is a difference between those two.

BY MR. CUMMINGS:

Q Well, I'll move on to ground 2, and I believe this starts in paragraph 139 --

A Yes, I have paragraph 139 in front of me.

Q This is the same combination you made for the '121 patent; is that correct?

A So I did consider a combination of Anzai in view of the Yamazaki for the one-to-one, yes.

Q Then in ground 3, you introduce Yamada; is that right?

A Ground 3, I believe -- I think it starts in paragraph 166. So again, for ground 3, it's Anzai in view of Yamada. So, yes, that's where I used --

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where I have considered the combination with Yamada.

Q Okay. I'll introduce Yamada as Exhibit 5. Can you let me know when you have it open?

A I will. I'm just -- my internet connection is slow. I'm going to make sure it actually has downloaded.

Yes, I have Yamada open, and I can see the file, yes.

Q In paragraph 174 of your declaration, you state that Yamada teaches the same layers as Anzai, including layers 17 and 19. Do you see that?

A I do.

Q And then a few sentences later, you say, "Yamada differs from Anzai by expressly teaching that layer 19, quote, may be composed of a single layer of SiO2 film or SiN film or a lamination of those films," end quote. Do you see that?

A I do.

Q Why did you choose Yamada as a secondary reference for Anzai, to support Anzai's disclosure, if they teach identical layers?

A Well, but they don't --

MR. LONEY: Object to form.

THE DEPONENT: I'm sorry.

MR. LONEY: Go ahead.

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THE DEPONENT: They use the same layer numberings, but it doesn't -- as I've stated right there, there is an express teaching in Yamada concerning the composition of 19. So in Yamada, let's see, pointed to column 6, for instance, in Yamada.

So if I go to column 6, at line -- yes, it is 48 through 50. It -- or 50 -- that cite -- I'm just looking at the cite. Now, I think it's line -- column 6, yes. No, it is 48 to 50. I'm sorry.

It's talking about 19 in -- sorry. In Anzai -- in Anzai -- you know, Anzai, it simply describes 19 as a planar -- I believe it refers to it as a planarization and gives an example material, which was a poly -- I don't know whether it was a polymer layer. It was -- it was -- let's see. 19. There it is. And Anzai 19 was -- excuse me. So that was Exhibit 2.

And we discussed this earlier. 19 is called the planarizing film. There is another spot where it, I think, identifies -- let me find it.

It identifies film 17 made of an organic resin. Then 19 -- other than calling it a second planarization film, I don't believe it even identifies -- says specifically what material you

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might select for 19. That's different in Yamada. Yamada is explicit as to choices for that material.

BY MR. CUMMINGS:

Q But the structure is the same?

A Well, they both have layer 19, I believe, in the same location. So in -- let's see. Where is the Yamada number.

So if you look at Yamada -- let me get my copy of Yamada. Anzai. Here is Yamada.

So Yamada has not exactly the same plan view but a very similar one. Yamada has, for instance, at Figure 4A, so the cross-sections are similar but are not -- for instance, I believe 4A is only -- maybe partway through, you see layer 19, which you also see in Anzai; and below that, you see layer 17, which you also see in Anzai, labeled with the same numbers.

So if you compare the cross-section in Anzai at Figure -- I'm trying to find what's a -- a fairly comparable one.

The cross-sections -- some of the cross-sections are done in different locations in Yamazaki than they are in Anzai, but one place to compare would be to look at Figure 4A or 4 -- and 4B of -- gosh. Sorry. Of Yamada.

And for instance, look at Figure 2A of Anzai.

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You'll see layer 19. You'll see layer 17. You see a very similar layer stack-up.

Q Looking at Figure 4B of Yamada, can you walk me through the fabrication process of how this structure would be made?

A I --

MR. LONEY: Objection. Form.

THE DEPONENT: I -- I could walk through the -- the films there, and let me -- so for Yamada, presumably, one way to do this would be to start with 10. 10 in Yamada is called the "A" substrate. Beyond that -- if you'll excuse me just a moment, I'll try to split my screen to make this a little bit easier.

So you asked me to walk through Figure 4B of Yamada; is that correct?

BY MR. CUMMINGS:

Q Yes.

A Okay. So I've just simply split my screen so I can see the figure I want to, and I can also see the text at the same time.

So I'm starting in column 1 of Yamada. Around line 29 or 30, it identifies the substrate 10. When I look at Figure 4B, I would, just from that, expect that probably the next film would be where

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that "43" points.

Now, that discussion is about Figure 2. So let me see if I can find something that is more specific to Figure 4.

A lot of the discussion in Yamada starts at column 5, but the beginning of it is really about 4A; and talking about the transistor, I'll call it 33. You're asking about 40B -- I mean Figure 4B. Excuse me.

Ah. There it is. Okay. So column 6, lines 7 and following, there is an active layer 43. It even tells you what it's formed by -- what it's formed of, alpha -- amorphous silicon in the recrystallization step.

So there would be -- on 10, I would expect there to be a deposition, a blanket deposition of this amorphus silicon recrystallization as stated in column 6. That would then be followed by a lithography-and-etch step to pattern -- to reach the desired pattern, in active layer 43.

Then the next film -- and in Yamada, I believe it does use the word "layer."

The next one is the gate-insulating film. Yamada refers to it as 32. You see that as a blanket film. It would cover everything. Probably no

lithography and etch in that layer yet.

The next deposition would be a material blanket film to form gate electrodes 41. That would require lithography and etch step to produce the desired pattern.

Next would be an interlayer insulating film 15. That's a quote from Yamada starting at line 15 in column 6.

15 would then require a lithography and etch step to open contact hole or via, down through 15 and 32, reaching 43.

It looks like then there would be a blanket deposition for a layer that's used to form 52. "See 52 in Figure 4B." Let me see if I can find the -- the text description for 52.

50 -- 50 -- 52, yes, 52. There it is. So you have to skip forward to column 7, line 50 -- looks like about 53. It describes 52 as a drive signal line. So that would require -- likely would be a blanket deposition of some conductive material, followed by lithography and etch to form the desired pattern.

Next would be a -- likely would be a blanket deposition of -- of 17.

Q Is 17 formed on 32?

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A 17 -- in Figure 4B, 17 is formed on 15 in Figure 4B.

Q Okay. I see.

A All right. At that point, looking at Figure 4B's cross-section, I would expect there would be a lithography and etch process to open a via that goes through 17, through 15, through 12, to touch 43.

Then there would be a, most likely, blanket film deposition for 61, which I think is back in column -- 61 is identified as being the anode, but that is clearly something that has to be deposited and lithography and etched to produce the desired pattern.

And it also -- I don't know whether it specifies that the filling of the via is done with the same material as 19. That is a way to do it. I don't recall whether Yamada bothers to say.

Next would be the blanket deposition, most likely, of 19 and a lithography and etch process to open a window in that.

Next would be blanket deposition 62 -- for layer 62, 63; and although in Figure 4B you can't tell whether it's patterned or not, requiring lithography and etch.

It wouldn't surprise me if it is. I don't

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know whether that's illustrated in the complete plan view or not.

Q Is 63 formed on 19?

MR. LONEY: Objection. Form.

THE DEPONENT: As shown in Figure B, 63 -- in Figure B, it's shown on 62. 62 is on 19. So 63 and 62, if we go -- let me find the Figure 4B. 62, 63. Let me find it.

19. I'm still trying to find the text that corresponds to 62, 63 and 64.

So it describes 66, which it indicates is a com -- looks like it's a combination of 65, 64, 63. It refers to that as the emissive layer.

It does that first, I guess, in maybe column 6 at line 59, 60. It -- it refers to it at -- several times. 66 as being the emissive element layer.

Still trying to find whether it goes through -- there it is.

Column 7. I'll start at line 30. It's saying that the emissive element layer comprises first-hole transport layer 62.

So we see 62 in Figure 4B and, as illustrated there, 62 is on 19.

Following 62 is a second-hole transport layer

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63, and following that is an emissive layer 64. We can clearly see that 64 is patterned, so there is a lithography and etch step to produce the desired pattern.

Next, there would be a blanket deposition of 65, which is described as an electron transport layer in column 7 at line 35, 36.

Here in this cross-section, I can't tell whether that has a pattern or not. Again, it wouldn't surprise me if it does. So there may be a lithography and etch step.

And then finally, there is layers -- or 67, which is called out at line 37 in column 7, as the cathode.

Again, in Figure 4B, I can't tell whether it's patterned, so I don't know from Figure 4B whether there is a lithography and etch step, but it wouldn't surprise me if there was.

BY MR. CUMMINGS:

Q And is 67 formed on 64?

MR. LONEY: Objection. Form.

THE DEPONENT: In this figure -- so 67 is formed on 64 because -- well, formed is -- so I want to be careful. Formed is, like, layer, or over.

In the claims of the '477, "forming" is used

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repetitively throughout the claim language, and of course there is always a question as to whether you mean directly formed on or simply formed on.

67 is directly formed on 65. But nonetheless, 67 is formed on 60 -- what is it? It's on 64. It's formed on 63. There is an intervening layer, but I don't believe that the patent specifies that if it simply says "formed," it means formed directly on.

So all of these layers are formed on the layers below. Some of them are formed directly on, and that's a more -- a narrower statement.

MR. CUMMINGS: All right. Well, thank you, Dr. Neikirk, that is all I have for the '477 patent, so I will turn it over to Mr. Loney.

MR. LONEY: Let's go off the record, take a quick break while I check my notes.

THE VIDEOGRAPHER: Okay.

MR. LONEY: I will have a few questions.

THE DEPONENT: How -- how long? I'm sorry. Are we off the record? Excuse me.

THE VIDEOGRAPHER: Off the video record at 2:11 p.m.

(Off the record.)

THE VIDEOGRAPHER: On the video record at

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2:26 p.m.

EXAMINATION

BY MR. LONEY:

Q Welcome back, Dr. Neikirk. I just have a few questions for you. Do you recall earlier today when you were discussing the '121 patent and discussing your combination of Yamazaki with Anzai?

A Yes, I do.

Q All right. And do you also recall that you referred to Figure 15A on page 61 of your declaration?

A Yes, I do recall that discussion.

Q And in light of 15A on page 61, can you explain your opinions regarding the combination of Yamazaki with Anzai?

A Well, I -- so -- and I think I mentioned that -- that Yamazaki had an embodiment with multiple dielectric layers in a specific place.

If -- if -- I think in paragraph 15 there on page 61, I specifically mention that there is an additional insulation layer that's formed under the insulation layer 1430. So 1431 in Figure 15A is under 1430.

So I think that was -- I -- I think I tried to indicate that, but I may not have called out the

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layers, but we see 1431 there in that figure, and it's under -- it's formed under 1430 there.

MR. LONEY: Thank you. No more questions.

THE VIDEOGRAPHER: Okay. Is everyone ready to conclude the deposition?

MR. LONEY: Yes.

MR. CUMMINGS: Yes.

THE VIDEOGRAPHER: All right. This concludes the deposition of Dr. Dean Neikirk on April 17, 2025. Off the video record at 2:28 p.m.

(Off the record.)

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ACKNOWLEDGMENT OF DEPONENT

I, DEAN NEIKIRK, PH.D., do hereby acknowledge that I have read and examined the foregoing testimony and the same is a true, correct, and complete transcription of the testimony given by me and any corrections appear on the attached errata sheet signed by me.

_____ _____

DEAN NEIKIRK, PH.D. (DATE)

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E R R A T A S H E E T

DEPONENT: DEAN NEIKIRK, PH.D.
CASE NO.: 37-2023-00026501-CU-OR-NC
United States Patent and Trademark Office
STENOGRAPHER: Theresa Williamson, CA CSR No. 14545
DATE TAKEN: April 17, 2025

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REPORTER'S CERTIFICATE

I, THERESA WILLIAMSON, RPR, RMR, CRR, CA CSR NO. 14545, DO HEREBY CERTIFY THAT THE FOREGOING DEPOSITION OF DEAN NEIKIRK, PH.D., WAS TAKEN ON APRIL 17, 2025 VIA ZOOM CONFERENCE BEFORE ME AT 10:02 A.M. FOR THE PURPOSE IN THE CAPTION STATED; THAT THE WITNESS WAS FIRST DULY SWORN TO TELL THE TRUTH, THE WHOLE TRUTH, AND NOTHING BUT THE TRUTH; THAT THE DEPOSITION WAS TAKEN BEFORE ME STENOGRAPHICALLY AND AFTERWARDS TRANSCRIBED UNDER MY DIRECTION; THAT THE FOREGOING IS A FULL, TRUE, AND CORRECT TRANSCRIPT OF THE SAID DEPOSITION SO GIVEN; THAT COUNSEL FOR ALL PARTIES WERE PRESENT AT THE TIME OF THE DEPOSITION; THAT THERE WAS A REQUEST THAT THE WITNESS READ AND SIGN THE TRANSCRIPT.

I FURTHER CERTIFY THAT I AM NEITHER OF COUNSEL NOR OF KIN TO ANY OF THE PARTIES TO THIS ACTION, AND AM IN NO WAY INTERESTED IN THE OUTCOME OF SAID ACTION.

WITNESS MY SIGNATURE ON APRIL 23, 2025.

Theresa Williamson

THERESA WILLIAMSON,
RPR, RMR, CRR, CA CSR NO. 14545

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