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Surface passivation approaches for silicon, germanium, and III–V semiconductors ^{EP}

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ABSTRACT

Semiconductors are key to our modern society, enabling a myriad of fields, including electronics, photovoltaics, and photonics. The performance of semiconductor devices can be significantly hampered by defects occurring at the surfaces and interfaces of the semiconductor. As semiconductor devices continue to be scaled and nanostructuring is becoming more commonplace, such defects are increasingly becoming the limiting factor in the device performance. Surface passivation can be used to reduce the number of defects and improve device performance. However, effective surface passivation approaches and requirements can vary greatly depending on the semiconductor material and the envisioned application. In this review, we aim to bring together the separated fields of research on passivation of various semiconductor materials by drawing parallels and highlighting important differences in these fields. To this end, we focus on passivation of silicon, germanium, gallium arsenide, indium phosphide, and gallium nitride. For silicon, a high-quality interface with few defects is relatively straightforward to obtain, and the remaining defects at the surface can be further passivated by hydrogen. For germanium and III-V semiconductors, it is more challenging to form a high-quality interface, and the role of hydrogen for defect passivation is less clear. Nevertheless, similar surface passivation approaches are used for these various semiconductors, and mainly focus on interface management, involving the use of passivation layers combined with surface treatments and/or interlayers. Understanding and extending the toolbox of semiconductor surface passivation will be of great value for effective passivation of current and future semiconductor devices.

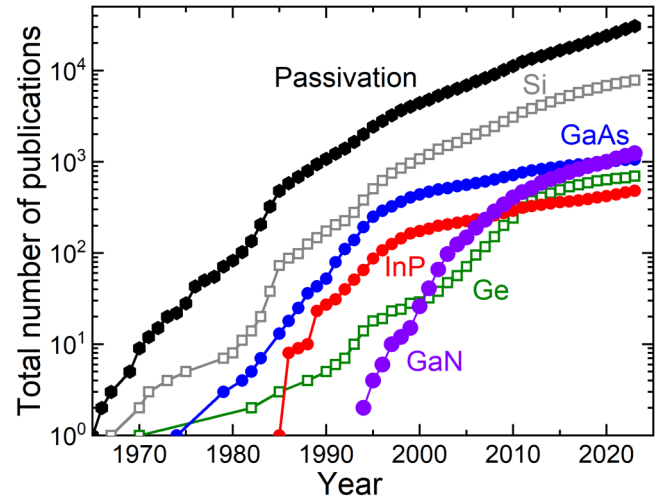
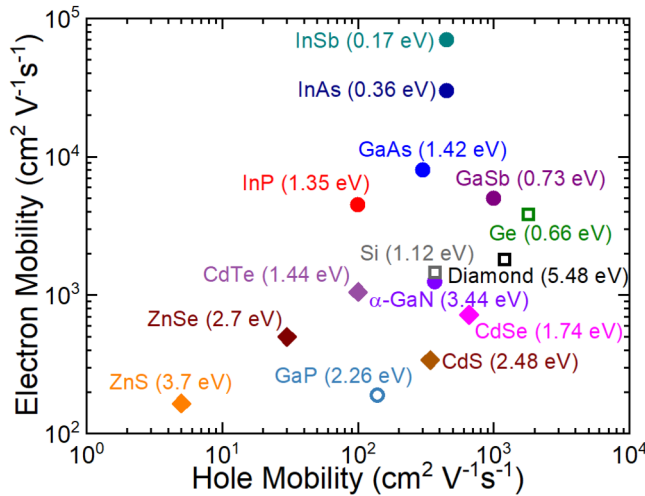
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I. INTRODUCTION

Semiconductors lie at the basis of (opto)electronic devices, including logic and memory devices, solar cells, displays, lasers, photodetectors, light emitting diodes (LEDs), power devices, and quantum devices.¹ These semiconductors include, but are not limited to, silicon, germanium, group III-V semiconductors, group II-VI semiconductors, perovskites, amorphous oxide semiconductors, and 2D semiconductors. The properties of these semiconductors determine their suitability for certain applications and include their bandgap (direct or indirect), bandgap energy, electron and hole mobilities, dopability, thermal conductivity, (chemical) stability, and toxicity. In Fig. 1, an overview of various group IV, III-V, and II-VI semiconductors is given in terms of their electron and hole mobility, along with their bandgap energy, which already demonstrates the wide variety in terms of the semiconductor properties.

For any semiconductor, the presence of defects and impurities in the semiconductor, or at the semiconductor surface, can greatly affect the performance of the devices they are used in.² Such defects are typically detrimental as they can function as recombination active sites, leading to the loss of charge carriers, or they can trap charge carriers, leading to scattering of charge carriers and a related decrease in mobility. In the bulk of the semiconductor, defects and impurities are generally minimized by advances in material synthesis. At the surface of the semiconductor, typically, a large number of structural defects are present. These defects may stem from unsatisfied bonds where the semiconductor lattice terminates. Furthermore, the interface of a semiconductor with another material, such as an insulator or a metal, can also lead to the formation of defects. The reduction of interface and surface defects is called surface passivation, and it is an active field of research. This can be seen in Fig. 2, which presents the total number of



publications on surface passivation, as well as the number of publications of surface passivation of some well-known semiconductors.

The defects at the surfaces and interfaces of semiconductors are becoming increasingly important in device performance. One reason is the continued improvement of the semiconductor bulk quality. To illustrate this, it is insightful to look at the evolution silicon solar cells. The relatively low bulk quality silicon used for solar cells (due to cost) is continuously improved by refining the silicon growth processes.³ This has allowed for steadily increasing bulk charge carrier lifetimes due to a decrease in bulk defects.⁴ Power efficiencies of silicon solar cells are now mainly limited by charge carrier recombination at the surfaces and contact areas of the solar cell.⁵ This is further amplified by the continued reduction in wafer thickness for solar cells. A similar route can also be anticipated for semiconductors other than silicon, i.e., continued improvements in material synthesis can reduce the amount of bulk defects and lead to surface defects becoming a dominant factor. Furthermore, many semiconductor devices are continuously “downscaled,” which leads to increased surface-to-volume ratios. This is exacerbated by a switch from planar to structured nanodevices. Since surface defects are becoming relatively more important, it is critical to understand how they can be passivated such that the performance of devices can be improved.

The most frequently used surface passivation approaches involve the deposition of passivation layers, which may be combined with surface treatments, interlayers, and/or postdeposition treatments. In some cases, providing good surface passivation is a requirement of a (passivation) layer, but not its main purpose. These layers are often not referred to as passivation layers. An example is the gate dielectric in a field-effect transistor (FET). This

layer should be a dielectric, and a high dielectric constant (high- κ) is preferred. However, because a low number of defects at the dielectric/semiconductor interface is required,⁹ it also needs to act as a passivation layer. In other cases, the main purpose of a layer is passivation, but it may also serve secondary purposes. For example, a passivation layer may also act as a protective layer for the underlying semiconductor. It may serve as an optical coating or antireflection layer. In some cases, it can be useful if the passivation layer can also conduct charge, i.e., serve as a “passivating contact.”⁵

In this review, the toolbox for semiconductor surface passivation will be discussed, with a focus on the use of passivation layers. Surface passivation of silicon (Si),^{4,10,11} germanium (Ge),^{12–14} and group III-V semiconductors^{15–19} will be discussed. For group III-V semiconductors, gallium arsenide (GaAs), indium phosphide (InP), and gallium nitride (GaN) will be used as general representatives. Figure 3 provides an overview of these semiconductor materials and a few examples of common semiconductor devices. Table I presents the properties of these semiconductors, along with their main application fields. Silicon has been the dominant semiconductor in electronics and photovoltaics. Germanium has high charge carrier mobilities—much higher than silicon—and is highly interesting for high-performance complementary metal-oxide-semiconductor (CMOS) and quantum applications.^{20,21} Gallium arsenide and indium phosphide have been of high interest for a variety of applications due to their direct bandgaps and high mobilities.^{22–25} Gallium nitride is used for power devices owing to its wide bandgap, high critical electric field, and

29 April 2025 18:47:46

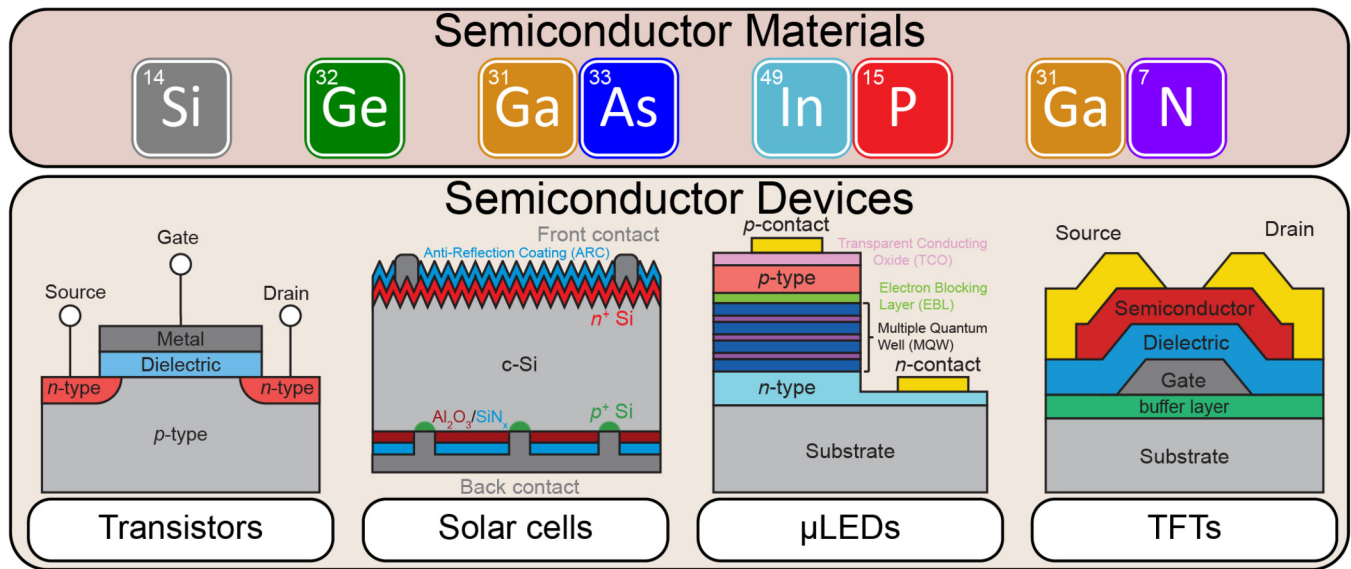


FIG. 3. Schematic overview of commonly used semiconductor materials and devices.

high electron saturation velocity²⁶ but is also used in (μ)LED applications.²⁷ While there are more semiconductor materials, we focus on these semiconductors, as they are some of the most commonly used, and will provide insights in the current toolbox for

semiconductor surface passivation. However, before going into the details of surface passivation approaches for these semiconductors, it is first discussed in more detail how (surface) defects lead to recom-

29 April 2025 18:47:46

TABLE I. Physical properties of silicon, germanium, gallium arsenide, and indium phosphide. Data at or near $T = 300$ K (Refs. 6–8 and 28). Some application fields for each semiconductor are also listed.

Property	Silicon	Germanium	GaAs	InP	GaN
Bandgap energy (E_g)	1.12 eV (ind)	0.66 eV (ind)	1.42 eV (dir)	1.34 eV (dir)	3.44 eV (dir)
Density (ρ)	2.33 g/cm ³	5.32 g/cm ³	5.32 g/cm ³	4.81 g/cm ³	6.07 g/cm ³
Lattice parameter (a)	5.43 Å	5.66 Å	5.65 Å	5.87 Å	3.19 Å
Refractive index (at 2.0 eV)	3.9	5.6	3.9	3.5	2.39
Melting point (T_m)	1687 K	1210 K	1511 K	1327 K	2791 K
Electron mobility (μ_e)	1450 cm ² V ⁻¹ s ⁻¹	3800 cm ² V ⁻¹ s ⁻¹	8000 cm ² V ⁻¹ s ⁻¹	4500 cm ² V ⁻¹ s ⁻¹	1245 cm ² V ⁻¹ s ⁻¹
Hole mobility (μ_h)	370 cm ² V ⁻¹ s ⁻¹	1800 cm ² V ⁻¹ s ⁻¹	300 cm ² V ⁻¹ s ⁻¹	100 cm ² V ⁻¹ s ⁻¹	370 cm ² V ⁻¹ s ⁻¹
Intr. carrier concentration (n_i)	1.02×10^{10} cm ⁻³	2.33×10^{13} cm ⁻³	2.1×10^6 cm ⁻³	3.3×10^7 cm ⁻³	... ^b
Thermal conductivity (κ)	1.3 W cm ⁻¹ K ⁻¹	0.6 W cm ⁻¹ K ⁻¹	0.5 W cm ⁻¹ K ⁻¹	0.7 W cm ⁻¹ K ⁻¹	1.3 W cm ⁻¹ K ⁻¹
Dielectric constant (ϵ_∞)	11.97 ^a	16.00	10.86	10.9	5.2
Applications	Electronics (Ref. 29) Photonics (Ref. 31) Photovoltaics (Ref. 11)	Electronics (Ref. 20) Photonics (Ref. 32) Quantum technology (Ref. 21)	Lasers (Ref. 22) Photonics (Ref. 23) Photovoltaics (Ref. 33)	Photonics (Ref. 24) Quantum dots (Ref. 25)	Power devices (Ref. 30) LEDs (Ref. 27)

^aMeasured at 750 MHz.
^bExtrinsic semiconductor.

II. THEORY

A. Recombination and passivation

Charge carrier generation and recombination in semiconductors can occur via various pathways. These processes are theoretically quite well-understood and described. In this section, only a short overview of these processes is given. For a rigorous treatment of charge carrier generation and recombination, the reader is referred to any semiconductor textbook, for example, Sze *et al.*¹ Figure 4 presents a schematic overview of the charge carrier generation and recombination mechanisms, as well as the interface between a semiconductor and a passivation layer. The individual processes are described in detail in this section.

Generation of an electron-hole pair can occur by absorption of a photon, where an electron from the valence band is excited to the conduction band, leaving behind a hole. This process is called band-to-band generation. The reverse process is band-to-band (radiative) recombination, where an electron from the conduction band recombines with a hole in the valence band under emission of a photon. The steady-state band-to-band generation/recombination process can be described by¹

$$U_{\text{rad}} = C_{\text{rad}}(pn - n_i^2), \quad (1)$$

where U_{rad} is the net radiative recombination rate ($\text{cm}^{-3} \text{s}^{-1}$), C_{rad} is the radiative recombination rate coefficient ($\text{cm}^3 \text{s}^{-1}$), p is the free

hole concentration (cm^{-3}), n is the free electron concentration (cm^{-3}), and n_i is the intrinsic carrier concentration [cm^{-3}]. Note that if U is negative, charge carriers are generated. In indirect semiconductors, band-to-band (radiative) transitions must be mediated by phonons to conserve the momentum. Therefore, typical values of C_{rad} for indirect semiconductors ($\sim 10^{-15} \text{cm}^3 \text{s}^{-1}$) are orders of magnitude smaller than those of direct bandgap semiconductors ($\sim 10^{-10} \text{cm}^3 \text{s}^{-1}$). The actual values depend on temperature and the band structure of the semiconductor.

Auger recombination is a three-particle process, where an electron and a hole recombine and transfer their excess energy to another free charge carrier (either an electron or a hole). The steady-state Auger recombination/generation process can be described by³⁴

$$U_{\text{Auger}} = C_n(n^2p - n_0^2p_0) + C_p(np^2 - n_0p_0^2), \quad (2)$$

where U_{Auger} is the net Auger recombination rate ($\text{cm}^{-3} \text{s}^{-1}$) and n_0 and p_0 are the equilibrium electron and hole densities (cm^{-3}), respectively (note that $n_0p_0 = n_i^2$). C_n and C_p are the Auger capture probabilities in case the third particle is an electron or hole ($\text{cm}^6 \text{s}^{-1}$), respectively.

Recombination processes can also occur via trap states in the bandgap. This type of recombination process is significantly more involved, as it considers the electron and hole capture and emission by the trap state. This recombination process is typically referred to as Shockley-Read-Hall (SRH) recombination.^{35,36} The steady-state

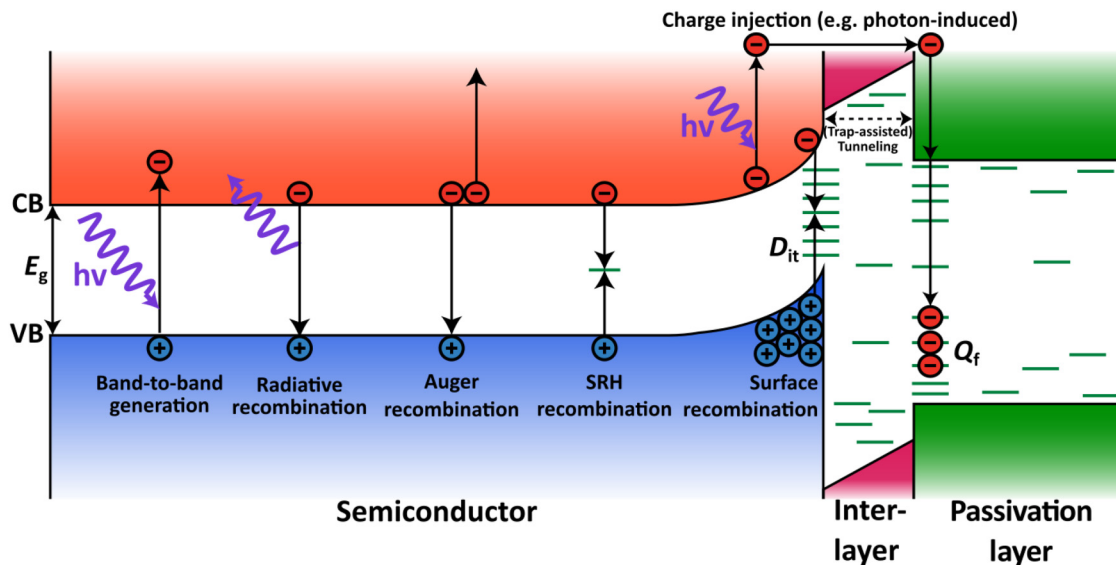


FIG. 4. Schematic representation of the interfaces of a semiconductor, an interlayer, and a passivation layer. In the semiconductor, the processes of charge carrier generation and radiative, Auger, SRH, and surface recombination are schematically shown. The number of defects at the interface of the semiconductor is represented by the interface defect density (D_{it}). In principle, a lower D_{it} implies less (surface) recombination and, hence, better surface passivation. Charges may become trapped in either interface states or bulk states. For traps away from the semiconductor interface, this can lead to a fixed charge density Q_f , which leads to band bending and alters the semiconductor surface charge carrier concentrations. The fixed charge can, for example, originate from (photon-induced) charge injection from the semiconductor into the passivation layer or from (trap-assisted) tunneling. In this particular example, a negative fixed charge is shown, while the fixed charge can also be positive. As the name suggests, the fixed charges typically remain trapped, but in some cases may be lost, for example, by (trap-assisted) tunneling or leakage through the interlayer. The values of D_{it} and Q_f can vary significantly per passivation scheme.

29 April 2025 18:47:46

SRH generation/recombination process for a single level trap is described by¹

$$U_{\text{SRH}} = \frac{\sigma_n \sigma_p v_{\text{th}} N_t (pn - n_i^2)}{\sigma_n \left[n + n_i e^{\frac{E_t - E_i}{kT}} \right] + \sigma_p \left[p + n_i e^{\frac{E_i - E_t}{kT}} \right]}, \quad (3)$$

where U_{SRH} is the net SRH recombination rate ($\text{cm}^{-3} \text{s}^{-1}$), σ_n is the electron capture cross section (cm^2), σ_p is the hole capture cross section (cm^2), v_{th} is the thermal velocity (cm s^{-1}), N_t is the trap concentration (cm^{-3}), E_t is the energy level of the trap (eV), E_i is the intrinsic Fermi level (eV), k is the Boltzmann constant (eV K^{-1}), and T is the temperature (K).

At the surface or interface of a semiconductor, the lattice terminates, which introduces a continuum of defect states in the bandgap through which SRH recombination can take place.³⁷ This surface recombination can be described by extending the SRH theory by considering a trap level density function ($D_{\text{it}}(E)$),^{37,38}

$$U_{\text{surf}} = \sigma_n \sigma_p v_{\text{th}} \times (pn - n_i^2) \times \int_{E_v}^{E_c} \frac{D_{\text{it}}(E)}{\sigma_n \left[n + n_i e^{\frac{E - E_i}{kT}} \right] + \sigma_p \left[p + n_i e^{\frac{E_i - E}{kT}} \right]} dE, \quad (4)$$

where U_{surf} is the net surface recombination rate ($\text{cm}^{-2} \text{s}^{-1}$), E_c and E_v are the conduction and valence band energies (eV), respectively, E is the energy position (eV), and D_{it} is the interface defect density ($\text{cm}^{-2} \text{eV}^{-1}$).

A typical quantity used to characterize recombination and passivation is the effective charge carrier lifetime τ_{eff} (s), which is determined by both surface and bulk recombination through³⁹

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{rad}}} + \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{SRH}}} + \frac{1}{\tau_{\text{surf}}}, \quad (5)$$

where τ_{rad} , τ_{Auger} , τ_{SRH} , and τ_{surf} are the charge carrier lifetimes (s) related to radiative, Auger, SRH, and surface recombination mechanisms, respectively. A higher value for τ_{eff} indicates better surface passivation, given that the other recombination processes are not limiting. Various methods exist to directly or indirectly determine τ_{eff} . The most used are photoconductance decay⁴⁰ for indirect bandgap semiconductors and time-resolved photoluminescence⁴¹ for direct bandgap semiconductors. Another measure for the passivation quality is the (effective) surface recombination velocity S_{eff} (cm s^{-1}). The relation between τ_{eff} and S_{eff} on planar wafers can be approximated (if S_{eff} is sufficiently low) by³⁹

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{2S_{\text{eff}}}{W} \quad (6)$$

and can be approximated for nanowires by⁴²

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{volume}}} + \frac{4S_{\text{eff}}}{d}, \quad (7)$$

where τ_{bulk} (s) is the wafer bulk lifetime, W (cm) is the wafer thickness, τ_{volume} (s) is the nanowire bulk lifetime, and d (cm) is the

nanowire diameter. A lower value of S_{eff} indicates better surface passivation, provided that bulk recombination is not limiting.

From a qualitative inspection of the equations above, several insights can be gained:

- Recombination processes (U) scale with the number of excess charge carriers. Auger recombination (U_{Auger}) is proportional to the cube of the number of excess charge carriers. This means that Auger recombination becomes an important recombination process in high injection (high concentrations of excess charge carriers) and for highly doped semiconductors.³⁹
- SRH recombination (U_{SRH}) for a single level trap is maximized if $E_t = E_i$,¹ indicating that the recombination is maximized if the energy level of the trap is near the middle of the bandgap of the semiconductor. This extends to SRH recombination at the surface (U_{surf}), where typically traps with energy levels near the midgap contribute most to the surface recombination.⁴³
- The effective charge carrier lifetime is limited by the lowest lifetime recombination processes, i.e., by the highest recombination rate.

To combat the detrimental effects of the surface defects, surface passivation can be used, which can be achieved in two main ways:

1. A reduction in the number of defects at the semiconductor surface, i.e., reducing D_{it} . Mainly a reduction in the number of defects with an energy level close to midgap is effective. This type of passivation is called chemical passivation¹¹ and can be achieved by surface treatments of the semiconductor and/or application of a passivation layer.
2. Reduction of the number of (minority) charge carriers reaching the surface, effectively reducing n and/or p in the equations for the recombination processes. This can be achieved in several ways. One is by (heavily) doping the near surface/interface region, which reduces the minority charge carrier concentration in this region, although it can lead to increased Auger recombination. A second way is by applying a passivation layer that provides a fixed charge density (Q_f), which can induce band bending near the surface of the semiconductor, and, thus, modifies the surface charge carrier concentrations. This second way is typically referred to as field-effect passivation.

B. Interface management

For any device, the combination of the semiconductor and passivation layer requires careful consideration of the important properties of the materials and their interface. Figure 5 presents a TEM image of the interface between a semiconductor and a passivation layer, and a schematic representation. At the interface, it is critical that defects are avoided or passivated, i.e., a low interface defect density (D_{it}) should be achieved. There are several “tools” that may be used to control the interface by avoiding or by passivating defects, such as the use of surface treatments, removal or controlled growth of an oxide interlayer, the use of a passivating interlayer, and the use of deposition processes that are not damaging to the substrate. These may also affect the fixed charge density (Q_f) to some extent.

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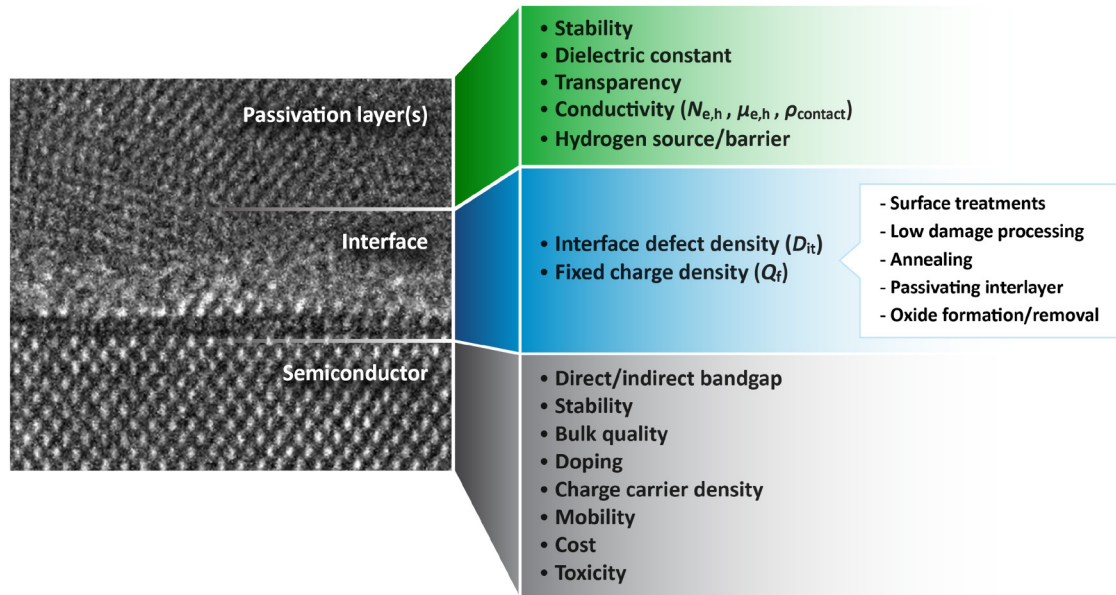


FIG. 5. Transmission electron microscopy (TEM) image of the interface between a semiconductor and a passivation layer, and a schematic representation. For the semiconductor and passivation layer, several aspects are mentioned that might require consideration depending on the device. For the interface, several tools are mentioned that can be used to affect the interface defect density (D_{it}) and the fixed charge density (Q_f). TEM image adapted from Black *et al.*, Sol. Energy Mater. Sol. Cells **188**, 182 (2018). Copyright 2018 Author(s), licensed under a Creative Commons License.

In many cases, several of these “tools” are used together and have to be tailored to the combination of the passivation layer and the semiconductor, which introduces significant complexity. Combinations of pretreatment(s), passivation layer(s), and postdeposition treatment(s) are sometimes referred to as a passivation scheme. Some passivation schemes may prove to be effective for passivation of a wide variety of semiconductors, while others may only be highly effective on select few semiconductors. When exploring approaches for surface passivation of a novel semiconductor, it can be beneficial to use passivation schemes of well-known semiconductors. However, in some cases, significant tailoring of the passivation schemes, or even completely new approaches, may be required to achieve adequate surface passivation. If a novel passivation layer or layer stack is investigated, it is important to consider also the pretreatments, interlayers, and postdeposition treatments. Some passivation layers may require the use of a pretreatment and/or an interlayer for effective passivation, while other passivation layers might not require them at all.

C. Atomic scale processing

In order to obtain passivation layers or layer stacks, whose thicknesses are typically on the order of a few to tens of nanometers, atomic scale processing (ASP) methods are used increasingly often. This is a general term, which refers to a collection of methods, which provide atomic scale control of material processing, including, but not limited to, atomic layer deposition (ALD),^{44–47} atomic layer etching (ALE),^{48,49} and chemical vapor

deposition (CVD).⁵⁰ While a rigorous treatment of these methods is beyond the scope of this work, an overview of ASP methods and various important aspects of these methods is shown in Fig. 6. The importance of the various aspects, such as throughput or uniformity, often depends on the intended application, and every method has its own strengths. For deposition of passivation layers, CVD and ALD are frequently used, and these processes have enabled the deposition of a wide variety of (passivating) thin-films. It is noted that the switch to 3D structured devices will lead to 3D compatible deposition methods, such as ALD, to become increasingly important. In Secs. III–V, the approaches for passivation of silicon, germanium, and III–V semiconductors are discussed.

III. SILICON

A. Surface and defects

The first transistor—invented at Bell Labs in 1947—did not feature silicon, but a germanium crystal as the semiconductor.⁵¹ At that time, research of semiconductors focused on both silicon and germanium. Germanium could already be made with high purity by a process called zone-refining, while this process was only later developed for silicon.^{51,52} Ultimately, the discovery of the high-quality interface between silicon and silicon oxide led to silicon becoming the dominant semiconductor. The silicon/silicon oxide (Si/SiO_2) interface is arguably the most well-characterized semiconductor/oxide interface, and it has played a critical role in the development of electronic and photovoltaic devices.

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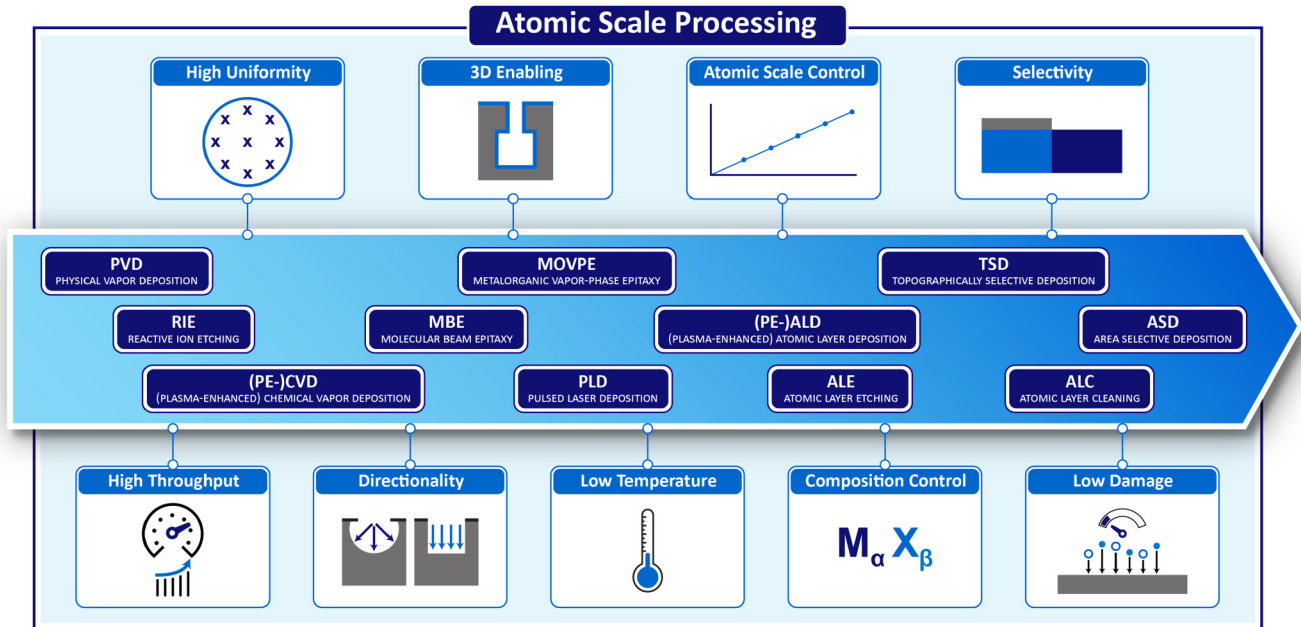


FIG. 6. Overview of atomic scale processing methods and various important aspects of these processes.

A layer of SiO_x on Si may form unintentionally due to contact of the Si surface with ambient oxygen or water,⁵³ but it also may be formed intentionally by surface oxidation or the deposition of an oxide (passivation) layer. Since SiO_x can form a stable and high-quality interface with silicon, it is often used for passivation in silicon-based devices, resulting in low values of the interface defect density (D_{it}).

Several defects occurring at the Si/SiO_x interface have been identified by electron spin resonance (ESR), including P_b , P_{b0} , and P_{b1} -type defects.⁵⁴ The P_b -type defects are identified as the most important defects at this interface,⁵⁵ and consist of three variants depending on the Si orientation, namely, the P_b -defect at the (111) Si/SiO₂, and the P_{b0} and P_{b1} -defects at the (100) Si/SiO₂ interface.⁵⁶ Various studies have reported the correspondence between the P_b -type defects and D_{it} ,^{57–62} suggesting that the P_b -type defects are mainly responsible for D_{it} at the Si/SiO_x interface. This correspondence can also be seen in the inset of Fig. 7. The P_b and P_{b0} -defects have the structure $\bullet\text{Si}\equiv\text{Si}_3$, i.e., an unsatisfied silicon atom bonded to three silicon atoms and are often referred to as a dangling bond. The P_{b1} -defect also has an unpaired Si bond but is assigned to a distorted interfacial dimer.⁶³ Since the P_b -type defects are mainly responsible for the interface defect density at the Si/SiO_x interface, it is important that they are passivated.

B. Passivation

It is reported that the P_b -type defects can be passivated by hydrogen.^{64,65} For example, annealing Si/SiO_x in a hydrogen-rich environment can significantly lower the D_{it} .^{57,58} This can be seen in Fig. 7, where the D_{it} drops an order of magnitude due to

hydrogen passivation of P_b -type defects by annealing in forming gas (red dash curve), which is a mixture of H_2 and N_2 gas. A subsequent longer anneal in only N_2 leads to a significant increase in D_{it} due to depassivation and a loss of hydrogen (blue dash dot curve).

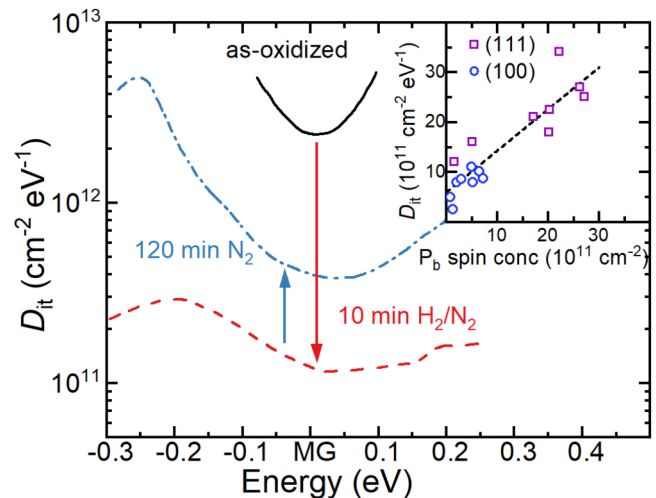


FIG. 7. Interface defect density for an oxidized silicon wafer (black solid), and after subsequent anneals in 10%/90% H_2/N_2 for 10 min at 500 °C (red dash), and in N_2 for 120 min at 500 °C (blue dash dot). The inset shows the correlation between D_{it} and P_b concentrations for oxidized (100) and (111) n -type silicon wafers. Data from Poindexter and Caplan (Ref. 57).

29 April 2025 18:47:46

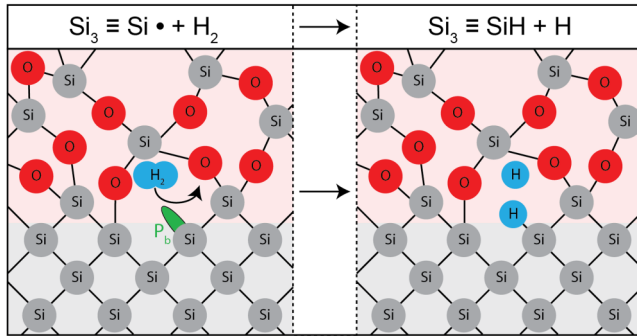
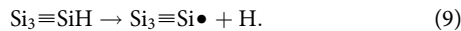


FIG. 8. Schematic representation of the passivation of a P_{b0} -defect at the (100) Si/SiO_x interface by molecular hydrogen.

The passivation of P_b -type defects by hydrogen may proceed via the reaction⁶⁶



Also, depassivation can occur by dissociation of $P_b\text{H}$ entities via the reaction⁶⁶



The passivation reaction [Eq. (8)] occurring at the (100)Si/SiO_x interface is schematically represented in Fig. 8. The incoming H₂ can react with the P_b -type defects, leading to passivation of the silicon dangling bond. It is noted that SiO₂ layers formed by silicon oxidation are typically considered to be amorphous but can in some cases be (partly) epitaxial.⁶⁷ The passivation reaction [Eq. (8)] typically has lower activation energies than the depassivation reaction [Eq. (9)].⁶⁶ In addition to molecular hydrogen (H₂), atomic hydrogen (H) can also lead to passivation of the P_b -type defects.⁶⁵ The hydrogen required to passivate the dangling bonds can come from various sources, for example, from a hydrogen-rich annealing ambient, but also from hydrogen-rich passivation layers, or from hydrogen plasma treatments. A (postdeposition) annealing treatment is typically required to deliver the hydrogen to the Si/SiO_x interface and to activate the (chemical) passivation by hydrogen [Eq. (8)].

C. Annealing

Annealing is a heat treatment, and typical temperatures range from 250 to 500 °C. Annealing may be conducted in various ambients, such as nitrogen, argon, or forming gas. Annealing at too high temperatures or for too long often leads to depassivation due to the breaking of Si–H bonds [Eq. (9)] and effusion of hydrogen, as also illustrated by the increase in D_{it} from the red dash curve to the blue dash dot curve in Fig. 7. For many passivation schemes on silicon, this leads to a U-shaped curve for S_{eff} as a function of annealing temperature, which is shown in Fig. 9. Annealing first activates the passivation, where the hydrogen originates from the passivation layer or another source, which leads to a decrease in S_{eff} . However, when the annealing temperature becomes too high,

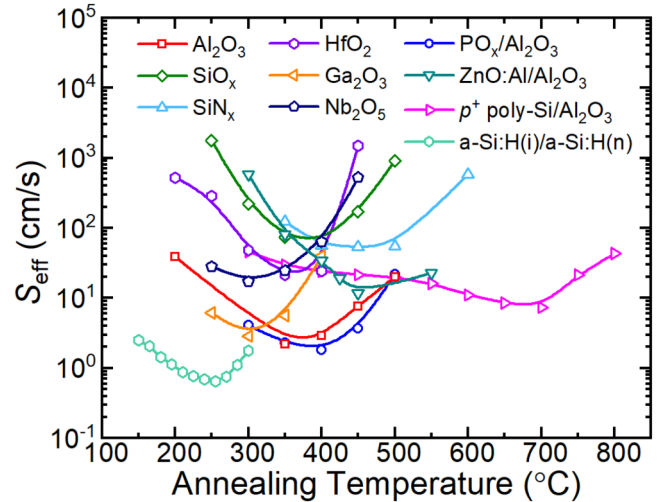


FIG. 9. Overview of the effective surface recombination velocity for Al₂O₃ (Ref. 72); SiO_x, SiN_x (Ref. 73); HfO₂ (Ref. 74); Ga₂O₃, Nb₂O₅ (Ref. 75); PO_x/Al₂O₃ (Ref. 76); ZnO:Al/Al₂O₃ (Ref. 75); p⁺ poly-Si/Al₂O₃ (Ref. 77); and a-Si:H(i)/a-Si:H(n) (Ref. 78) on silicon as a function of annealing temperature. S_{eff} determined from τ_{eff} under the assumption that bulk lifetimes were not limiting.

S_{eff} increases due to breaking of Si–H bonds and effusion of hydrogen. The optimum in passivation quality (lowest S_{eff}) is likely determined by the balance between the passivation [Eq. (8)] and depassivation [Eq. (9)] reactions,⁶⁸ and the amount of hydrogen available at the silicon surface. In some cases, annealing also activates the field-effect passivation of a passivation scheme by leading to an increase in the fixed charge density (Q_f). This has, for example, been observed to be the case for aluminum oxide (Al₂O₃) deposited on silicon by thermal ALD.⁶⁹

One very particular postdeposition annealing treatment for SiO_x is the so-called *alneal*, where an aluminum metal layer is deposited on the SiO_x, followed by an annealing step. This has led to extremely low S_{eff} values,⁷⁰ which is assumed to be related to passivation of silicon dangling bonds by atomic hydrogen, which may be formed due to reactions between the aluminum, and water or hydroxyl ions present in or on the SiO_x.⁷¹

D. Native oxide

Stoichiometric silicon oxide (SiO₂) is an insulator with a wide bandgap of around 9 eV and a dielectric constant of 3.9.⁷⁹ However, the stoichiometry of a layer often depends on the preparation method, and the native silicon oxides present on a silicon surface are not necessarily stoichiometric. The same holds for the quality of the interface between Si and a (native) SiO_x layer, which can vary significantly. Typical D_{it} values for the Si/SiO_x interface are 10¹² cm⁻² eV⁻¹⁸⁰ but can range from 10¹⁰ to 10¹³ cm⁻² eV⁻¹ depending on how the SiO_x is obtained. In addition to possibly leading to very low D_{it} values, SiO_x also provides a low positive fixed charge density (Q_f) on silicon, which is on the order of +10¹¹ cm⁻².¹⁰

29 April 2025 18:47:46

When SiO_x is used for passivation, the (low-quality) native oxide is often removed by wet-chemical etching and then a (high-quality) SiO_x layer is formed in a controlled way. In this way, a high-quality Si/SiO_x interface with low D_{it} , i.e., a well-passivated silicon surface, is straightforward to obtain. Removal of SiO_x is typically achieved by etching using hydrofluoric acid (HF),⁸¹ while SiO_x can be formed on silicon by thermal oxidation,⁸² plasma oxidation,⁸³ UV/ O_3 oxidation,⁸⁴ or wet-chemical oxidation.⁸⁵ Some well-known wet-chemical oxidation methods are Radio Corporation of America (RCA) clean, $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2$, and HNO_3 .^{84–86}

The SiO_x can act as a passivation layer by itself, but often, it serves as an interlayer for other passivation layers. Many of the passivation layers shown in Fig. 9 also have an SiO_x interlayer. The (SiO_x) interlayer provides a good interface, while the passivation layers can provide hydrogen for further passivation of the dangling bonds at the interface or can provide other benefits in a device. It is noted that an SiO_x interlayer does not have to be stoichiometric to provide a good interface. This has been observed for niobium oxide (Nb_2O_5) on silicon, which provides good passivation with a substoichiometric silicon oxide interlayer.⁸⁷ The use of oxide passivation layers (such as Al_2O_3 ⁸⁸) on silicon often inevitably leads to the formation of an SiO_x interlayer, either during the deposition of the oxide or during a subsequent annealing treatment.

Therefore, the (chemical) passivation mechanism of many oxide passivation layers on silicon is typically also attributed to the passivation of silicon dangling bonds at the Si/SiO_x interface by hydrogen. This is qualitatively shown in Fig. 10, which shows the electrically detected magnetic resonance (EDMR) spectra of as-deposited and annealed Al_2O_3 on silicon. Several defects, including a P_b -type defect ($g = 2.0087$ and $g = 2.0036$), could be identified in the as-deposited state.⁶⁹ After annealing, the EDMR spectra no longer reveals the presence of the defect states, which is in

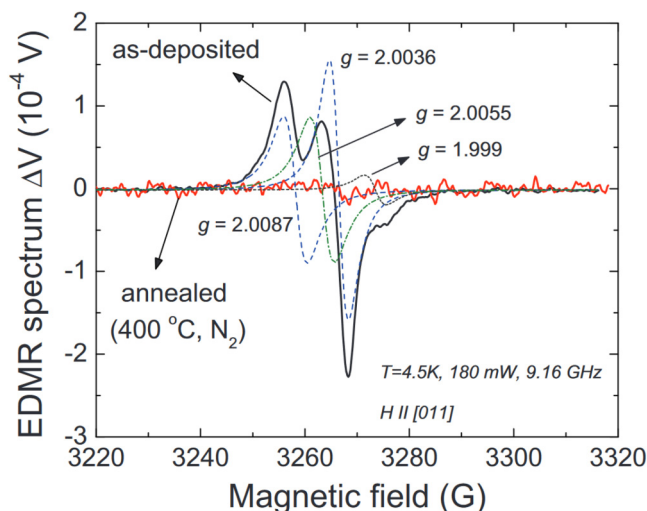


FIG. 10. EDMR spectra of as-deposited and annealed Al_2O_3 films on Si (100). Reprinted with permission from G. Dingemans and W. M. M. Kessels, *J. Vac. Sci. Technol. A* **30**, 040802 (2012). Copyright 2012 American Vacuum Society.

agreement with the low D_{it} ($\leq 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) obtained after annealing. Additionally, it is reported that $\text{Si}/\text{Al}_2\text{O}_3$ and Si/HfO_2 interfaces (without SiO_x interlayers) also exhibit P_b -type defects.^{89,90} The chemical passivation mechanism of many passivation layers on silicon is, thus, thought to be similar and related to hydrogen passivation of silicon dangling bonds.

E. Passivation schemes

Several passivation schemes that have been investigated on silicon were already shown in Fig. 9. Clearly, not all passivation schemes result in the same passivation quality. Optimization of surface pretreatments, deposition conditions, and postdeposition annealing conditions or other postdeposition treatments can lead to improvements in passivation quality. This optimization has been the subject of significant research over the past few decades and has already provided an extensive toolbox for passivation of silicon. This can be visualized by the overview of D_{it} and Q_f values for various passivation schemes on silicon, as shown in Figs. 11(a) and 11(b), respectively. Wide ranges of D_{it} and Q_f values have been reported, even for the same passivation scheme, which can be attributed to widely varying processing conditions. In principle, a low D_{it} is desired, but sometimes even higher D_{it} values may be acceptable if the passivation scheme provides other benefits, such as improved stability. The stability of the passivated interface is highly important since the passivation quality can degrade over time due to device operation or harsh external environments (e.g., high intensity radiation or high temperatures).

Figures 9 and 11 illustrate the wide variety of passivation schemes that have been investigated for silicon. Several additional passivation layers that have been investigated on silicon include TiO_x ,⁹¹ MoO_x ,⁷⁵ Ta_2O_5 ,⁹² ZrO_2 ,⁹³ and AlN ,⁹⁴ which each have their own benefits.⁷⁵ Furthermore, not only the use of different materials, but also the use of stacks of passivation layers can provide benefits. For example, using an Al_2O_3 capping layer on ZnO leads to improved stability, as well as an increase in the charge carrier density and mobility of the ZnO layer after annealing, as compared to a single layer of ZnO .⁹⁵ The increase in mobility is thought to be related to hydrogen passivating defects and traps at grain boundaries of the ZnO .⁹⁵ Capping of ZnO by Al_2O_3 furthermore led to improved passivation quality of the ZnO .⁹⁶ Another example is the use of SiN_x for capping Al_2O_3 , which improves the high temperature stability of the Al_2O_3 layers.⁹⁷ These examples illustrate that the use of stacks of materials can be a powerful tool to tailor passivation schemes to an application. In the remainder of this section, some of the most used and most interesting passivation schemes for silicon surface passivation will be discussed in more detail. The typical properties of these passivation schemes are presented in Table II.

F. Si-based passivation schemes

In addition to SiO_x , other Si-based layers, such as hydrogenated amorphous silicon (a-Si:H), polysilicon (poly-Si), silicon carbide (SiC), and silicon nitride (SiN_x), may be used for passivation of silicon, either as a passivation layer or an interlayer.

The a-Si:H layers typically provide excellent chemical passivation of silicon, because they terminate the Si dangling bonds by

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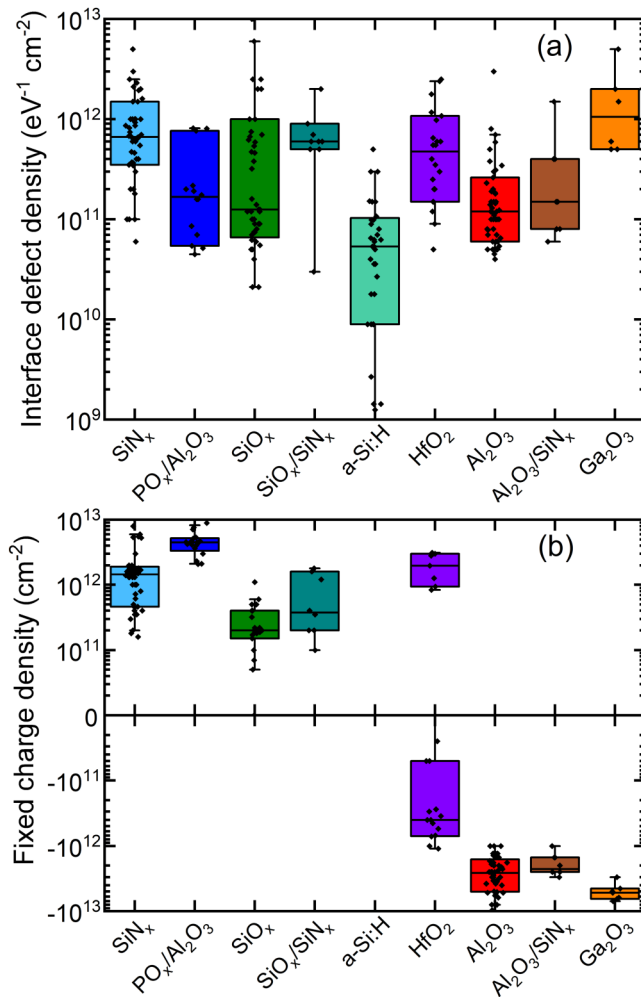


FIG. 11. Overview of interface properties of passivation schemes on c-Si, in terms of (a) interface defect density (D_{it}) and (b) fixed charge density (Q_f). Reprinted from Theeuwes *et al.*, *Sol. Energy Mater. Sol. Cells* **246**, 111911 (2022). Copyright 2022 Author(s), licensed under a Creative Commons License.

continuing the c-Si lattice into a disordered network of Si–H and Si–Si bonds.¹¹² Therefore, they are also great interlayers for passivation and are frequently used in conjunction with other layers. In addition to functioning as a passivation layer, a-Si:H has also been used as channel materials for thin-film transistors (TFTs); however, amorphous oxide semiconductors and 2D semiconductors are now also being used as channel materials.¹¹³ It is noted that TFTs devices can also benefit from passivation.

Semi-insulating poly-Si was used early on as a passivation layer for bipolar Si transistors, as it could protect the device against contamination and externally applied electric fields.¹¹⁴ Later, structures combining doped poly-Si with a thin SiO₂ interlayer (tunnel oxide) were realized as “passivating contacts” for applications in

solar cells.^{5,115} The solar cell concepts referred to as silicon heterojunction (SHJ) and tunnel oxide passivated contact (TOPCon) feature a-Si:H and poly-Si passivating contacts, respectively. Both concepts have enabled very high power efficiencies above 26%.¹¹⁶ The Si/SiO₂ interface of the poly-Si typically requires hydrogenation (i.e., passivation of silicon dangling bonds using hydrogen), which is often accomplished by using a H₂ plasma treatment, or by deposition of hydrogen-rich layers, such as Al₂O₃, SiN_x, or Al₂O₃/SiN_x stacks on top of the SiO₂/poly-Si stack followed by an annealing treatment.^{77,115,117–119}

SiC can be used for passivation of silicon, and it has been shown that SiO_x/SiC stacks can also act as passivating contacts on silicon, where the SiO_x again acts as a tunnel oxide.¹²⁰ An advantage of the SiO_x/SiC stacks is that they are highly transparent. In power electronics, SiC is used as a semiconductor, mainly in high power and high temperature devices. In those cases, the SiC requires passivation, where SiO_x is typically used. However, it is challenging to obtain a high-quality SiC/SiO_x interface, mainly due to the presence of carbon-related defects.^{121,122} Note the difference between the Si/SiO_x/SiC and the SiC/SiO_x interfaces. In the former case, Si is the semiconductor that is passivated. In the latter case, SiC is the semiconductor that is passivated.

SiN_x is frequently used as a passivation layer for silicon, but it can also serve as a capping layer for other passivation layers. It is furthermore often used as a combined passivation layer and antireflection coating for solar cells.^{100,123} SiN_x can achieve quite good chemical passivation of silicon with D_{it} values down to 10¹¹ cm⁻² eV⁻¹. Depending on the nitrogen content in SiN_x, its properties can be vastly different.¹⁰⁰ For example, the bandgap can vary from 2.9 to 5.3 eV depending on the N/Si ratio.¹⁰¹ The passivation of silicon is also affected by the composition of SiN_x, “Si-rich” SiN_x is reported to have better as-deposited passivation quality, while “N-rich” SiN_x is more thermally stable.¹²⁴ SiN_x is characterized by a high *positive* fixed charge on the order of +10¹¹–10¹³ cm⁻² on silicon. The magnitude of the fixed charge also appears to be impacted by the composition, with “Si-rich” SiN_x typically having lower Q_f .¹²⁵ The origin of the *positive* fixed charge in SiN_x is attributed to K-centers (•Si≡N₃) and N-centers (•N≡Si₂), both of which can also act as dangling bonds and contribute to D_{it} .¹²⁶ This means that an increase in Q_f in SiN_x is typically paired with an increase in D_{it} . Therefore, SiN_x typically has either low D_{it} or high Q_f , but not both at the same time. It is noted that these N- and K-centers are amphoteric, yet SiN_x on silicon is almost exclusively positively charged.

G. Aluminum oxide (Al₂O₃)

Al₂O₃ is a dielectric with a bandgap of 6–9 eV and a dielectric constant of 7–9.^{18,69} It is currently one of the most frequently used passivation layers, not just for silicon surface passivation, but also for germanium and III–V semiconductors, as will be shown later. On silicon, Al₂O₃ is used in a myriad of electronics and photovoltaics applications. Furthermore, Al₂O₃ is frequently used as a capping layer for other passivation layers, likely because it can provide chemical stability, and may act as a hydrogen source/effusion barrier.

For silicon solar cells, Al₂O₃ was already reported in 1989 by Hezel and Jaeger,¹²⁷ but it remained largely unnoticed until

29 April 2025 18:47:46

TABLE II. Typical properties of SiO₂, Al₂O₃, PO_x/Al₂O₃, SiN_x, and HfO₂ on silicon.

Passivation scheme	Bandgap (eV)	ϵ_r (–)	D_{it} (cm ^{–2} eV ^{–1})	Q_f (cm ^{–2})	S_{eff} (cm/s)	Reference
SiO ₂	9	3.9	10 ¹⁰ –10 ¹²	+10 ¹¹	10–100	10, 79, 80, 98, and 99
SiN _x	2.9–5.3	5–7	10 ¹¹ –10 ¹²	+10 ¹¹ –10 ¹²	10–100	98 and 100–102
Al ₂ O ₃	6–9	7–9	10 ¹⁰ –10 ¹²	–10 ¹² –10 ¹³	1–100	18, 69, and 103
HfO ₂	6	10–25	10 ¹¹ –10 ¹²	–10 ¹² –+10 ¹²	10–100	74, 79, and 104–106
PO _x /Al ₂ O ₃	>6	6.4–7.4	10 ¹⁰ –10 ¹²	+10 ¹² –10 ¹³	2–100	76 and 107–111

2008.¹²⁸ It has since enabled the transition from the aluminum back surface field (Al-BSF) solar cell design to the passivated emitter and rear cell (PERC) design,¹²⁹ which enables solar cell power efficiencies up to 24%. It is also featured on the front side of the TOPCon solar cell, the successor of the PERC solar cell.

Al₂O₃ has also been considered a gate dielectric for CMOS technology due to its moderately high dielectric constant (high- κ) and high stability.¹³⁰ SiO_x was first used as a gate dielectric, but a drive toward higher capacitance required the SiO_x layer thickness to decrease. Eventually, the SiO_x had to become too thin (<1.6 nm), leading to large leakage currents.⁹ Therefore, alternative materials were required, which could be made physically thicker than the SiO_x, while retaining the same capacitance per unit area. This is often represented by the equivalent oxide thickness [EOT (nm)], which can be calculated by⁹

$$EOT = d_{\text{high-}\kappa} \times \frac{K_{\text{SiO}_2}}{K_{\text{high-}\kappa}}, \quad (10)$$

where $d_{\text{high-}\kappa}$ is the thickness (nm) of the high- κ material, K_{SiO_2} is the dielectric constant of SiO₂ (3.9), and $K_{\text{high-}\kappa}$ is the dielectric constant of the high- κ material. A thicker high- κ layer can lead to the same capacitance as a thinner SiO₂ layer, and can thereby reduce the gate leakage current. There are several high- κ dielectrics that have been investigated for silicon, including HfO₂, Ta₂O₅, Y₂O₃, La₂O₃, and ZrO₂.¹³¹ For CMOS applications with high- κ dielectrics, band-alignment should be taken into account. For example, the conduction bands of silicon and Ta₂O₅ have a quite close alignment, which can lead to high leakage currents. The use of polycrystalline gate dielectrics can also lead to high leakage currents, therefore amorphous films are generally preferred.¹³¹

Al₂O₃ provides excellent chemical passivation of silicon, with an interface defect density as low as 10¹⁰ eV^{–2} cm^{–1}. It is furthermore characterized by a rather high *negative* fixed charge density (Q_f) of around –10¹² cm^{–2}. Due to this high Q_f , Al₂O₃ is not very well-suited for CMOS, as this leads to threshold voltage shifts. The origin of the fixed charge in Al₂O₃ is not yet fully understood.¹³² It has been attributed to negatively charged AlO₄ tetrahedra, which may occur preferentially at the Al₂O₃/SiO_x interface, as the silicon oxide is also tetrahedrally coordinated.¹³³ Furthermore, interstitial oxygen and aluminum vacancies were also shown to be preferentially negatively charged and could contribute to the negative Q_f .^{132,134}

H. Hafnium oxide (HfO₂)

HfO₂ is another high- κ dielectric that has been investigated extensively for CMOS technology.¹³⁵ The dielectric constant of HfO₂

can vary significantly depending on phase, but typically ranges between 10 and 25.¹⁰⁴ Quite low surface recombination velocities can be achieved by using HfO₂¹⁰⁶ due to relatively low D_{it} values of 10¹¹ cm^{–2} eV^{–1}. Since the magnitude of Q_f is relatively low, it is well-suited for CMOS applications. Interestingly, both negative and positive values for Q_f have been reported for HfO₂ on silicon.^{74,105,106} Annealing could result in a switch from positive to negative Q_f .¹⁰⁵ In addition to acting as a high- κ gate dielectric and a passivation layer, ferroelectric HfO₂-based materials have also attracted significant attention for nonvolatile memory applications.¹³⁶

I. Phosphorus oxide and aluminum oxide (PO_x/Al₂O₃)

PO_x/Al₂O₃ stacks have shown a unique combination of a very low defect density (~10¹⁰ cm^{–2} eV^{–1}) and a simultaneous very high *positive* fixed charge density (+10¹²–10¹³ cm^{–2}) on silicon. Therefore, these stacks have been investigated extensively over the past few years.^{76,107–111} The stack has a bandgap of >6 eV and a dielectric constant of 6.4–7.4.^{76,107} The Al₂O₃ layer serves as a capping layer, because the PO_x is highly hygroscopic. However, the Al₂O₃ layer also plays a role in the chemical passivation mechanism of the PO_x/Al₂O₃ stack. This mechanism is thought to be related to passivation of silicon dangling bonds by hydrogen, where the hydrogen is mobilized by the formation of AlPO₄ upon annealing.¹⁰⁷ The combination of a very low D_{it} and a high *positive* Q_f has shown to lead to state-of-the-art passivation of *n*-type doped silicon, with a passivation quality on par with SiO_x/SiN_x/SiO_x stacks and *annealed* SiO_x.¹⁰⁸ Although the origin of this high *positive* fixed charge remains unknown, it has been suggested that positively charged PO₄ tetrahedra in the PO_x, analogous to the negatively charged AlO₄ tetrahedra in Al₂O₃, may be the entities responsible for the *positive* fixed charge in the PO_x/Al₂O₃ stacks.¹⁰⁹

IV. GERMANIUM

A. Surface and defects

In contrast to the silicon/silicon oxide interface, the germanium/germanium oxide (Ge/GeO_x) interface does not easily result in a high-quality interface. The native oxide of germanium is typically viewed as a poor oxide, as it is thermally unstable and water soluble.^{12,14,137} This has hampered the development and scaling of germanium devices. Nevertheless, the high carrier mobilities of germanium, combined with its compatibility with silicon, have made it to be a highly interesting semiconductor for a wide variety of applications, including transistors, quantum technology, and

29 April 2025 18:47:46

(infrared) photonics. Furthermore, hexagonal germanium and silicon-germanium alloys exhibit a direct bandgap¹³⁸ and can be used in applications that require efficient light emission, such as LEDs and lasers.

The defects occurring at the Ge/GeO_x interface have been investigated by ESR, similarly as for the Si/SiO_x interface. However, ESR has been unable to detect Ge dangling bonds at the Ge/GeO_x interface.^{139,140} It is suggested that the energy level of the Ge dangling bond is located below the germanium valence band maximum.^{141,142} This would mean that the Ge dangling bond is only stable in a negative charge state, and therefore not observable by ESR.¹⁴⁰ It has furthermore been suggested that interstitial hydrogen in germanium acts only as an acceptor,^{139,142,143} which would mean that the Ge dangling bond and the hydrogen would repel each other, making hydrogen passivation unlikely.

Although ESR has been unsuccessful at measuring the Ge dangling bond defect, it has been reported on the basis of density functional theory (DFT) that a Ge dangling bond defect at the Ge/GeO₂ interface may have an energy level near the middle of the Ge bandgap.¹⁴⁴ This dangling bond has the structure of •Ge≡Ge₃, similar to the Si dangling bond. However, this Ge dangling bond density may be below the ESR detection limit, and therefore not observed.¹⁴⁴ This Ge dangling bond may be passivated by hydrogen, but it is unknown whether it is really present at the Ge/GeO_x interface.

On silicon-germanium alloys (SiGe), an interfacial Ge dangling bond was identified by ESR.¹⁴⁵ This defect, denoted GeP_{b1} present at the SiGe/SiO_x interface, can be passivated with hydrogen, following reactions similar to Eqs. (8) and (9). However, the same dangling bond is not observed for Si_{1-x}Ge_x alloys with compositions $x < 0.45$ and $x > 0.87$,¹⁴⁵ i.e., for “Si-rich” and “Ge-rich” compositions.

B. Passivation

From the discussion above, it appears that there is no consensus yet on the defects occurring at the germanium interface, and the role of hydrogen for passivation of germanium surfaces is not fully understood yet. Nevertheless, hydrogen does appear to play a role for the passivation of defects at the germanium surface. This is, for example, apparent in devices and passivation studies of germanium, where it is reported that postdeposition treatments involving hydrogen can result in positive effects, such as a reduction of D_{it} ^{146,147} and a decrease in S_{eff} .^{148–151} This is illustrated in Fig. 12, which reveals some similarities and differences for passivation of silicon and germanium by Al₂O₃ and PO_x/Al₂O₃. The U-shaped curves are also observed for germanium, which suggests the passivation of defects on germanium by hydrogen. However, it is not as straightforward to obtain low S_{eff} on germanium with Al₂O₃, as indicated by the high S_{eff} in comparison with silicon. It is noted that excellent passivation of germanium by Al₂O₃ is possible, but it requires the use of interlayers or surface treatments to control the interface, as will be shown later. For PO_x/Al₂O₃ on germanium, a much lower optimal annealing temperature is observed as compared to PO_x/Al₂O₃ on silicon.

These similarities and differences between passivation of silicon and germanium are also reflected in the passivation approaches of

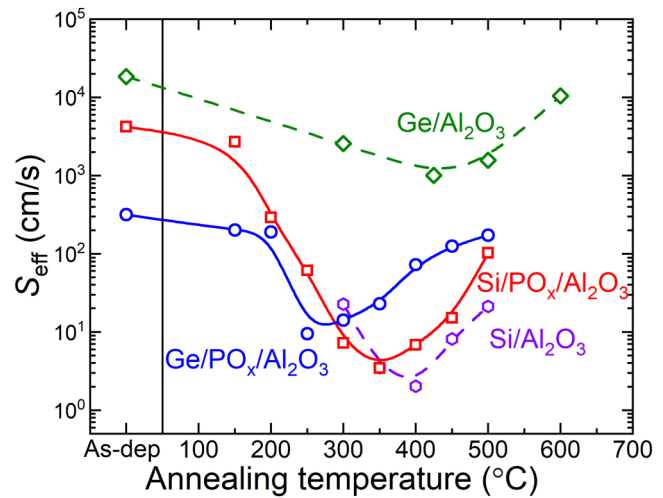


FIG. 12. Effective surface recombination velocity as a function of annealing temperature for Al₂O₃ and PO_x/Al₂O₃ on germanium and silicon. Reprinted from Theeuwes *et al.*, Appl. Phys. Lett. 123, 091604 (2023). Copyright 2023 Author (s), licensed under a Creative Commons License.

germanium. On germanium, the passivation approaches tend to focus on obtaining high-quality interfaces, rather than passivating the remaining defects on the interface with hydrogen. Even though the focus may be slightly different, many approaches and materials used are still similar to passivation of silicon.

C. Native oxide

The native oxide of germanium is typically removed prior to any further processing, similar as for silicon. Wet-chemical removal of the native GeO₂ may be done using HF, HCl, and HBr.¹⁵² HF removes the GeO₂, but the suboxides remain, while HBr removes all germanium oxides.¹⁵² It has been shown that intentionally grown GeO₂ can serve as a good passivating (inter)layer on germanium. Stoichiometric germanium oxide (GeO₂) has a bandgap of 4.7 eV¹⁵³ and a dielectric constant of around 5.5–5.9.¹⁵⁴ Thermal oxidation resulted in Ge/GeO₂ interfaces with D_{it} values down to $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.¹⁵⁴ Even higher quality Ge/GeO₂ interfaces were reported for GeO₂ obtained by electron-cyclotron-resonance oxygen plasma treatments, resulting in D_{it} values down to $6 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$.¹⁵⁵ These high-quality GeO₂ layers can serve as an interlayer for passivation schemes, an approach similar to passivation of silicon. It was, for example, found that the good passivation quality of GeO₂ is retained when combined with high- κ dielectrics, such as Al₂O₃ and HfO₂.^{156–158}

D. High- κ dielectrics

The high charge carrier mobilities of germanium have made it a promising candidate to use as a channel material in FETs, and therefore, the use of high- κ dielectrics on germanium has been investigated quite extensively.¹⁷⁵ This can be seen in Fig. 13, which provides an overview of reported interface defect densities (D_{it}) of

29 April 2025 18:47:46

several passivation schemes on germanium. Many of these passivation schemes combine interlayers or surface treatments with high- κ dielectrics. Typical D_{it} values of high- κ dielectrics on germanium are around 10^{11} – 10^{12} cm $^{-2}$ eV $^{-1}$. The investigations in controlling and obtaining high-quality germanium interfaces with high- κ dielectrics for FET devices are now also enabling the use of germanium in quantum technologies.²¹

E. Si-based passivation schemes

Thin epitaxial silicon layers have been used for germanium surface passivation, mainly as an interlayer for high- κ dielectrics in transistor applications.^{158,166–168} This strained Si interlayer may not be too thick, as otherwise, it may relax, which can lead to the formation of defects. It also cannot be too thin, as otherwise, it may be fully oxidized by subsequent oxide (gate dielectric) deposition.¹⁵⁸ The optimal Si layer thickness is between four and eight monolayers. If the defects at the Ge/Si interface are not limiting, the passivation of these epitaxial Si layers reduces back to passivation of silicon surfaces. It is shown that very low interface defect density values on the order of 10^{10} cm $^{-2}$ eV $^{-1}$ can be achieved,¹⁶⁶ but also, significantly higher values for D_{it} on the order of 10^{12} cm $^{-2}$ eV $^{-1}$ have been reported.^{167,168}

Passivation of germanium by SiN $_x$ has recently been investigated and may be used in infrared photodetectors and multijunction solar cells.^{150,176} As discussed previously, SiN $_x$ leads to relatively low defect densities on silicon, along with a moderate positive fixed charge. On germanium, the defect density of the Ge/SiN $_x$ interface is determined to be around 4×10^{11} cm $^{-2}$ eV $^{-1}$.¹⁵⁰ However, interestingly, SiN $_x$ on germanium results in a negative fixed

charge.^{150,176} The use of a SiN $_x$ /Al $_2$ O $_3$ stack and subsequent annealing treatments further improved the effective charge carrier lifetimes, suggesting hydrogen passivation of the Ge interface defects, although it did appear to be less efficient than hydrogenation of the Si interface by the same stack.¹⁵⁰

Similar as to silicon, a-Si:H thin-films can be used as a passivation layer and as an interlayer for germanium. They have, for example, been used as passivation layers for Si/SiGe quantum wells.¹⁷⁷ Furthermore, stacks of a-Si:H with Al $_2$ O $_3$ were highly effective for passivation of germanium, as discussed in Sec. IV F.¹⁴⁹

F. Aluminum oxide (Al $_2$ O $_3$)

Passivation of germanium by Al $_2$ O $_3$ is investigated not only for its role as a high- κ dielectric in transistors,^{153,157,171} but may also be used in radiation detectors, and hexagonal Ge-based LEDs and lasers.^{148,149,178,179} Isometsä *et al.* reported that using a HF pretreatment and subsequent deposition of Al $_2$ O $_3$ by ALD followed by annealing in N $_2$ resulted in an S_{eff} of 14.9 cm/s.¹⁷⁸ Using a HCl pretreatment instead led to an S_{eff} of 6.6 cm/s. This improvement was shown to be mainly due to an increase in the negative Q_f of Al $_2$ O $_3$. Berghuis *et al.* reported a significantly higher S_{eff} of 1000 cm/s for ALD Al $_2$ O $_3$ on germanium, which was also pretreated by HF.¹⁴⁸ Later, a very low S_{eff} value of 2.7 cm/s was obtained by using HF pretreatment and an a-Si:H interlayer prior to deposition of Al $_2$ O $_3$.¹⁴⁹

The use of an a-Si:H interlayer mainly resulted in a higher Q_f , which is suggested to be related to the formation of a SiO $_x$ interlayer between the a-Si:H and Al $_2$ O $_3$ layers.¹⁴⁹ Using thermal ALD instead of plasma-enhanced ALD for deposition of the Al $_2$ O $_3$ layer resulted in a lower Q_f , which may be related to the thinner SiO $_x$ layer that forms between the a-Si:H and Al $_2$ O $_3$.¹⁴⁹ This can be seen in Fig. 14, where the SiO $_x$ layer in Fig. 14(a) is thicker than in Fig. 14(b).

These examples of germanium passivation by Al $_2$ O $_3$ underline that pretreatments and interface control are highly important in obtaining excellent passivation quality of germanium. In these cases, the improvement of passivation quality was mainly attributed to an increase in the negative fixed charge, rather than a decrease in the interface defect density. It is noted that many passivation schemes—such as Al $_2$ O $_3$ and SiN $_x$ —provide a negative fixed charge on germanium. In contrast, the PO $_x$ /Al $_2$ O $_3$ stacks were found to provide a positive fixed charge on germanium.¹⁵¹ Additionally, the deposition of PO $_x$ /Al $_2$ O $_3$ stacks appears to lead to removal and reduction of the GeO $_x$.¹⁵¹ This may explain why low S_{eff} values were more straightforward to obtain with PO $_x$ /Al $_2$ O $_3$ on germanium as compared to Al $_2$ O $_3$ on germanium (Fig. 12) since for Al $_2$ O $_3$ on germanium, a GeO $_x$ interlayer was present.¹⁴⁸

G. Surface nitridation

Another approach for surface passivation is to use nitridation of the surface (analogous to the use of SiN $_x$ on silicon), resulting in a GeO $_x$ N $_y$ or GeN $_x$ surface layer.^{159–162} The general idea is that GeN $_x$ is thermally stable and insoluble in water, unlike the GeO $_x$. Nitridation of the surface can be achieved by thermal or plasma processes using NH $_3$ or N $_2$ gas. The GeO $_x$ N $_y$ layers can serve as an interlayer for other passivation layers or can serve as a dielectric passivation layer by itself. The range of D_{it} values for various

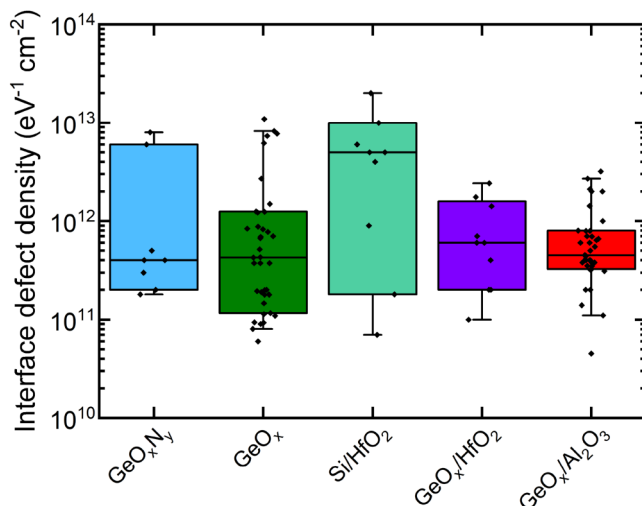


FIG. 13. Overview of interface defect density (D_{it}) values reported in the literature of GeO $_x$ N $_y$ (Refs. 159–164), GeO $_x$ (Refs. 12, 154, 155, and 165), Si/HfO $_2$ (Refs. 166–169), GeO $_x$ /HfO $_2$ (Refs. 14, 157, and 170), and GeO $_x$ /Al $_2$ O $_3$ (Refs. 149, 153, 157, 163, and 171–174) on germanium. The colored bars show $\pm 30\%$ of data points from the median, while the error bars show where $\pm 45\%$ of data points from the median are located.

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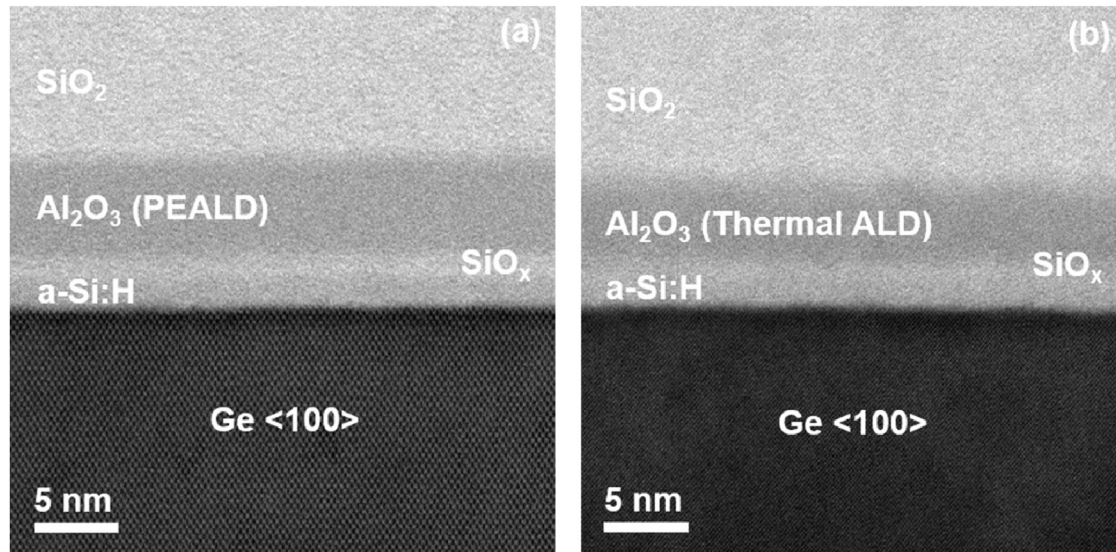


FIG. 14. Cross-sectional bright-field scanning transmission electron microscopy images of a-Si:H/Al₂O₃ stacks on *n*-type <100> germanium, where the a-Si:H was deposited by PECVD and the Al₂O₃ was deposited by (a) plasma-enhanced ALD and (b) thermal ALD. Reprinted with permission from Berghuis *et al.*, J. Appl. Phys. **130**, 135303 (2021). Copyright 2021 AIP Publishing LLC.

GeO_xN_y/Ge interfaces is given in Fig. 13. Note that different capping layers were used on top of the GeO_xN_y, such as Ta₂O₅,¹⁵⁹ HfO₂,¹⁶⁰ and SiN_x,¹⁶¹ which may also affect the resulting D_{it} values. It is reported that surface nitridation leads to a positive Q_f , indicated by a negative flatband voltage shift.¹⁶³ Annealing was reported to lead to a reduction of the fixed charge.¹⁶³

H. Sulfur passivation

Passivation of germanium surfaces by sulfur has been investigated quite intensively.¹⁴ Sulfur passivation may be achieved by using an (NH₄)₂S solution^{180–182} or H₂S gas.^{183,184} Desorption of S from the germanium surfaces without a capping layer occurs at temperatures above 320 °C in an ultrahigh vacuum (UHV). It was, however, found that S-passivated germanium with an HfO₂ capping layer results in a D_{it} of $2.4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, which was lower than the D_{it} of $5.9 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for a nitridated germanium reference.¹⁸⁰ Furthermore, the S-passivated germanium resulted in a less flatband voltage shift compared to the nitridated reference, indicating the presence of a less fixed charge at the interface. For germanium capacitors with a HfON gate dielectric, it was found that the EOT and D_{it} were both lower for S-passivated samples as compared to those without S-passivation.¹⁸¹ It is noted that sulfur passivation also works on silicon¹⁸⁵ but is generally not frequently used.

V. III-V SEMICONDUCTORS

A. Surface and defects

Surfaces of III-V semiconductors have been quite challenging to passivate, which has significantly hampered the development of III-V based devices.^{15–18} One of the challenges is the native oxides forming

interfaces with a high number of defects, which can lead to Fermi-level pinning.¹⁸⁶ Spicer *et al.*¹⁸⁷ suggested that these defects form indirectly as a result of adatoms on the surface, which was based on the observation that the Fermi-level pinning was similar for metals and oxygen adatoms. In this section, first GaAs and InP will be treated as general representatives of III-V semiconductors, and then GaN will be discussed to illustrate the effect of passivation layers in devices.

At the interfaces of GaAs and InP, several structural defects—which may result in Fermi-level pinning—have been suggested to occur. At GaAs interfaces, the presence of As_{Ga}⁺ antisites (an arsenic atom replacing a gallium atom in the lattice), Ga and As dangling bonds, As-As dimers, and several defect complexes has been suggested.^{15,16,18,188} The As-As dimers and the As_{Ga}⁺ antisite are thought to be some of the main defects occurring at the GaAs interface.^{16,189} At the InP interfaces, the presence of phosphorus and indium vacancies (V_P and V_{In}), interstitials, antisites (P_{In} and In_P), and dangling bonds has been suggested.^{190,191} In a phosphorus-rich material, V_{In} and P_{In} antisites appear to dominate, while in an indium-rich material, the dominant defect appears to be the V_P .¹⁹²

B. Passivation

Although some of the defects occurring at the III-V surfaces and interfaces may be passivated by hydrogen,^{15,193–195} the main approaches for passivation of III-V semiconductors focus on management of the interface and avoiding the formation of the defects in the first place, similar to passivation of germanium. Clearly, avoiding the formation of defects is always preferred, even on silicon, but it is much more critical for semiconductor interface defects that are not easily passivated by hydrogen. This also illustrates why silicon is more straightforward to passivate as compared

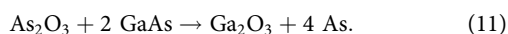
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to germanium and III–V semiconductors. On silicon, a good interface can be obtained with SiO₂ (or a-Si:H) as an interlayer, which can be used together with a wide variety of passivation layers. The defects at those interfaces can often be further passivated by hydrogen. On germanium and III–V semiconductors, the passivation layer itself needs to provide a good interface, and the possibility to repair defects at the interface by hydrogen is limited. Furthermore, oxidation of the semiconductor during processing should typically be avoided, as this may lead to additional defects at the interface. This puts significantly higher requirements on the passivation schemes and processing methods for germanium and III–V semiconductors as compared to silicon and, therefore, makes interface management significantly more important.

The various surface passivation approaches used for III–V semiconductors include the deposition of (high- κ) dielectrics, Si-based interlayers, S-based surface treatments, plasma treatments, and nitridation.^{16–19,53} Furthermore, wet-chemical etching steps of the native oxides, such as those involving HF, HCl, or NH₄OH, are often used prior to other passivation approaches.¹⁹⁶ The S-based surface treatments also effectively remove the native oxides and lead to passivation by forming S-based covalent bonds at the surface for many III–V semiconductors.¹⁹⁷ These approaches bear significant similarities to those used for silicon and germanium.

C. Native oxide

The native oxides of III–V semiconductors may form as an oxide of either element or a combination of both. For GaAs, based on phase diagrams, the native oxides are expected to be mixtures of As₂O₃, As₂O₅, and Ga₂O₃.²¹⁹ It has been shown that the compositions of the oxides can vary greatly depending on the oxidation conditions and on chemical, thermodynamic, and kinetic factors.²¹⁹ For thermal oxidation (350–460 °C) of GaAs, the oxide layers are gallium rich, with a composition close to Ga₂O₃, and As³⁺ is the dominant arsenide component in these oxides.²¹⁹ Relatively large quantities of elemental As are also present at the surface after thermal oxidation. The formation of elemental As at the surface is expected to occur through the following reaction:²¹⁹



This reaction is thought to be favorable in weak oxidation conditions, and the elemental As may act as a defect at the native oxide surface.

For InP, it has been shown for many different methods of oxidation of InP surfaces that the oxides are a mixed InP_xO_y state, which is thought to be present as a nonstoichiometric amorphous phase.²²⁰ Interestingly, for InP, it is shown that devices with a low interface defect density can be obtained by utilizing the native oxide.^{221,222} Specifically, phosphorus-rich oxides, such as In(PO₃)₃, grown by chemical or electrochemical treatments, were used.²²² Such phosphorus-rich oxides can also reduce the out-diffusion of phosphorus from the InP, and thereby reduce the formation of phosphorus vacancy-related defects at the interface. It is also reported that further modification of the native oxide can lead to decreased surface recombination, for example, by further oxidation or nitridation.²²³ It is quite unique that some native oxides of InP

appear to form a good-quality interface with low defect density, as this is generally not the case for other III–V/oxide interfaces.

D. High- κ dielectrics

There has been quite some interest in III–V semiconductors for CMOS applications due to their high mobilities. Therefore, deposition of high- κ dielectrics on III–V, often by ALD, has been investigated quite extensively. This was not only investigated for GaAs and InP, but also, for example, for InGaAs.^{224,225} This is visualized in Fig. 15, where an overview of reported interface defect densities (D_{it}) of Al₂O₃ and HfO₂ on GaAs, InP, and InGaAs surfaces is shown. As can be seen in the figure, D_{it} for these interfaces is still relatively high on the order of 10¹² eV cm^{−2} eV^{−1} or above. To obtain D_{it} lower than 10¹² cm^{−2} eV^{−1} with high- κ dielectrics, typically, NH₄OH and (NH₄)₂S surface treatments are used.^{198,206,210} On InGaAs, it appeared to be difficult to get a low D_{it} using HfO₂ only. This problem may be circumvented by using Al₂O₃ interlayers^{217,218,226} (not shown in Fig. 15).

E. Interfacial “self-cleaning”

An interesting observation was reported by Frank *et al.*,²²⁷ who investigated Al₂O₃ and HfO₂ for III–V FET applications, and found that ALD of Al₂O₃ on GaAs led to thinning of the native oxide. This was found to occur by using trimethylaluminum [Al(CH₃)₃] and H₂O.²²⁷ In the same work, deposition of HfO₂ on GaAs using HfCl₄ and H₂O did not result in thinning of the native oxide. The (partial) removal or reduction of the native oxide during deposition of the passivation layer is termed “self-cleaning” and was later also shown to occur for ALD of HfO₂ using tetrakis

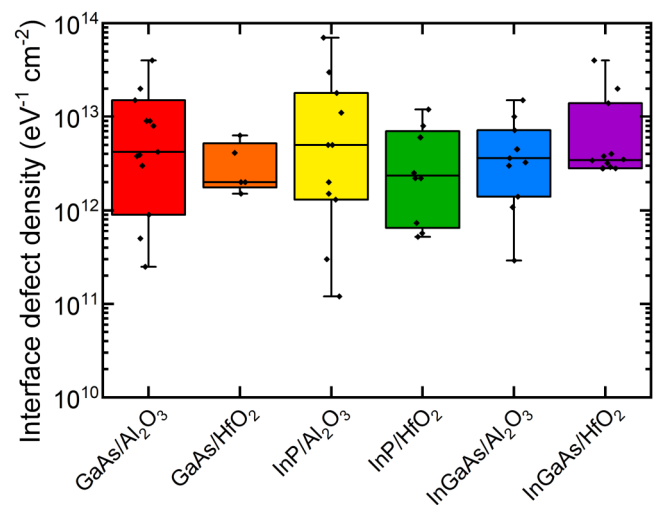


FIG. 15. Overview of the interface defect density (D_{it}) reported in the literature of GaAs/Al₂O₃ (Refs. 198–203), GaAs/HfO₂ (Refs. 198, 201, 204, and 205), InP/Al₂O₃ (Refs. 206–209), InP/HfO₂ (Refs. 210 and 211), InGaAs/Al₂O₃ (Refs. 212–216), and InGaAs/HfO₂ (Refs. 213, 217, and 218). The colored bars show $\pm 30\%$ of data points from the median, while the error bars show where $\pm 45\%$ of data points from the median are located.

29 April 2025 18:47:46

(ethylmethylamino)hafnium $[(\text{CH}_3)(\text{C}_2\text{H}_5)\text{N}]_4\text{Hf}$ as a precursor.²²⁸ This is visualized in the x-ray photoelectron spectroscopy (XPS) spectra in Fig. 16, where it can be seen that the intensities of the oxide peaks are significantly reduced after deposition of either Al_2O_3 and HfO_2 by ALD. It is noted that various combinations of precursors with native oxides of III–V semiconductors can result in the removal of the native oxide, as discussed by Klejna and Elliot.²²⁹

Recently, Richard *et al.*²³² reported that low-frequency plasma-enhanced chemical vapor deposition (LF-PECVD) of SiN_x also leads to removal and reduction of the native oxides of the GaAs surfaces. Such processes may be used to better control the native oxides and improve the resulting surface passivation. An example of this is reported by Jacob *et al.*²³³ using the combined effects of native oxide removal and sulfurization of the surface by $(\text{NH}_4)_2\text{S}$, followed by further native oxide removal by deposition of LF-PECVD SiN_x . This combination resulted in up to a 29-fold increase in the PL intensity of GaAs-based nanopillars as compared to the unpassivated reference.²³³

F. Epitaxial growth

Another passivation approach is epitaxially growing a layer on the semiconductor surface since this can result in an interface with a very low number of defects. This type of approach was already mentioned for germanium by using epitaxial silicon, but it has also been investigated for high- κ gate dielectrics on III–V semiconductors. For these gate dielectrics, it is important that the epitaxial layer has proper conduction and valence band offsets (typically larger than 1 eV) with respect to the semiconductor.²³⁴ La_2O_3 epitaxially grown on GaAs has, for example, shown to lead to a high-quality interface with a D_{it} of $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.²³⁵ Another example is Gd_2O_3 on GaAs, which resulted in a D_{it} of $\sim 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.²³⁶ In principle, passivation by epitaxial growth can be used for any semiconductor, but there will be challenges in avoiding a lattice mismatch, which can lead to strain and relaxation, possibly leading to the formation of defects at the interface.

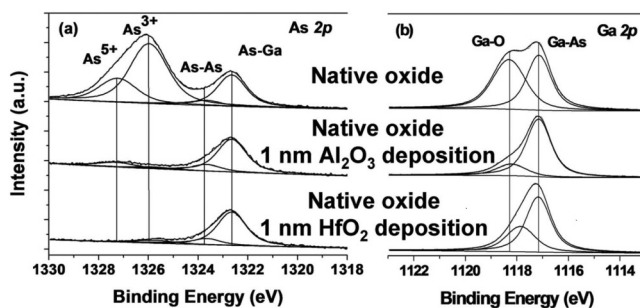


FIG. 16. XPS spectra for (a) As2p and (b) Ga2p of the GaAs native oxide and after deposition of 1 nm Al_2O_3 and 1 nm HfO_2 by ALD. Reprinted with permission from Hinkle *et al.*, Appl. Phys. Lett. **92**, 071901 (2008). Copyright 2008 AIP Publishing LLC.

G. GaAs/ Ga_2O_3

Although the native oxides of GaAs are typically seen as unwanted, it was demonstrated by Passlack *et al.*²³⁷ that deposition of Ga_2O_3 on GaAs using molecular beam epitaxy (MBE) resulted in a very low D_{it} . The resulting D_{it} values were in the upper $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ for Ga_2O_3 deposited on GaAs after thermal desorption of the native oxide in UHV. At the resulting GaAs/ Ga_2O_3 interface, As_2O_3 and As_2O_5 were not detected and it seems that elimination of As-oxides in general appears to be important for Fermi-level unpinning of GaAs.¹⁸⁹ However, the leakage current of FETs with Ga_2O_3 is quite high, and the usefulness of Ga_2O_3 for FET applications is limited.²³⁸ This could be improved by adding gadolinium to the Ga_2O_3 , but the resulting $\text{Gd}_x\text{Ga}_{0.4-x}\text{O}_{0.6}$ layers deposited directly on GaAs resulted in a lower quality interface. A solution was to use $\text{Ga}_2\text{O}_3/\text{Gd}_x\text{Ga}_{0.4-x}\text{O}_{0.6}$ stacks,²³⁹ where the Ga_2O_3 serves as an interfacial layer to lead to a high-quality interface.

H. InP/ $\text{PO}_x/\text{Al}_2\text{O}_3$

For passivation of InP, a similar interesting case is also using one of the native oxides, in this case phosphorus oxide (PO_x).²⁴⁰ The PO_x layer was capped by Al_2O_3 due to its hygroscopic nature, resulting in the $\text{PO}_x/\text{Al}_2\text{O}_3$ stacks. The use of phosphorus-rich oxides is expected to reduce the formation of phosphorus vacancy-related defects at the interface, which can form due to desorption of phosphorus at elevated temperatures.¹⁰⁷ It was indeed found that using $\text{PO}_x/\text{Al}_2\text{O}_3$ stacks on InP nanowires led to improved stability of the nanowires at elevated temperatures and a factor 20 increase in the PL intensity.²⁴⁰ This work was the inspiration for the use of the previously discussed $\text{PO}_x/\text{Al}_2\text{O}_3$ stacks for passivation of silicon and germanium surfaces. A TEM image of an InP nanowire passivated by $\text{PO}_x/\text{Al}_2\text{O}_3$ stacks can be seen in Fig. 17. Note that the native oxide is still present on the nanowire.

I. GaN passivation

Over the recent years, GaN has become a mature semiconductor with applications in power electronics and LEDs.²⁷ As can be seen in Fig. 2, research on passivation of GaN picked up somewhat later than that of InP and GaAs but has now overtaken both of them in terms of the number of publications. In order to further illustrate the benefits of passivation layers in devices, we will look at the passivation of GaN-based devices in more detail. The representative GaN-based devices are high-electron-mobility transistors (HEMTs) and μLEDs , whose basic structures are schematically shown in Fig. 18.

GaN-based power devices, such as AlGaIn/GaN HEMTs, can suffer from challenges, such as current collapse and threshold voltage instability, which are attributed to charge trapping at interface and surface states.^{241–243} In order to mitigate these problems, several passivation approaches have been used to reduce the number of surface states. Similar as for the previously discussed semiconductors, Al_2O_3 and SiN_x were some of the main investigated passivation layers.^{242,243} It was shown that both Al_2O_3 and SiN_x passivation layers could reduce current collapse.²⁴³ However, using SiN_x can lead to large leakage currents;²⁴² on the other hand,

29 April 2025 18:47:46

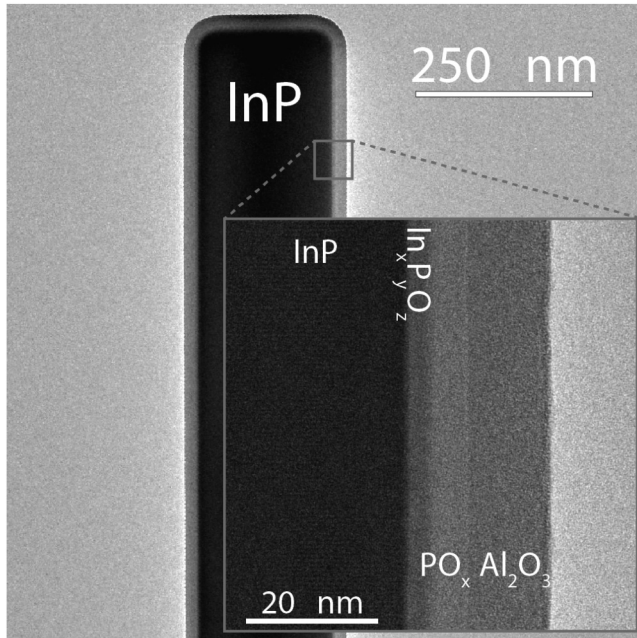


FIG. 17. Bright-field transmission electron microscopy images of an InP nanowire with native oxide passivated by $\text{PO}_x/\text{Al}_2\text{O}_3$. Adapted from Theeuwes *et al.*, *Sol. Energy Mater. Sol. Cells* **246**, 111911 (2022). Copyright 2022 Author(s), licensed under a Creative Commons License.

using Al_2O_3 can result in threshold voltage instability.²⁴³ The use of HfO_2 often resulted in high leakage currents or threshold voltage instability;^{242,243} thus, its application for GaN-based HEMTs does not appear straightforward. Nevertheless, GaN devices with good characteristics have been obtained using passivation layers, often in conjunction with interface control layers, or through the use of stacks.²⁴³ In particular, AlN has shown to suppress current collapse and reduce the dynamic ON-resistance at high drain-bias switching conditions, demonstrating effective passivation of GaN.²⁴⁴ AlN/ SiN_x stacks could retain effective passivation, even after high temperature processing.²⁴⁵ Gao *et al.*²³⁰ have compared stacks of $\text{Al}_2\text{O}_3/\text{SiN}_x$ and $\text{NiO}_x/\text{SiN}_x$ with single layer SiN_x as combined gate dielectric and passivation layers for GaN-based HEMTs. They reported that both stacks were able to increase the breakdown voltage, reduce the leakage current, and reduce current collapse as compared to the single layer SiN_x . This was attributed to a lower D_{it} achieved by these stacks by minimizing damage at the (Al)/GaN surface.

GaN-based μLEDs , such as InGaN/GaN μLEDs , typically suffer from defects at the sidewalls, which can lead to nonradiative recombination. It has been observed that this is more severe for smaller μLED devices,²⁴⁶ underlining the importance of surface passivation with continued device scaling. In order to mitigate this problem, several passivation treatments have been attempted, including the use of chemical treatments and/or dielectric materials.¹⁹⁷ In a similar vein as for the HEMTs, some of the used dielectrics include Al_2O_3 , SiO_2 , and SiN_x . Recently, Son *et al.*²³¹ compared these three different passivation layers for InGaN/

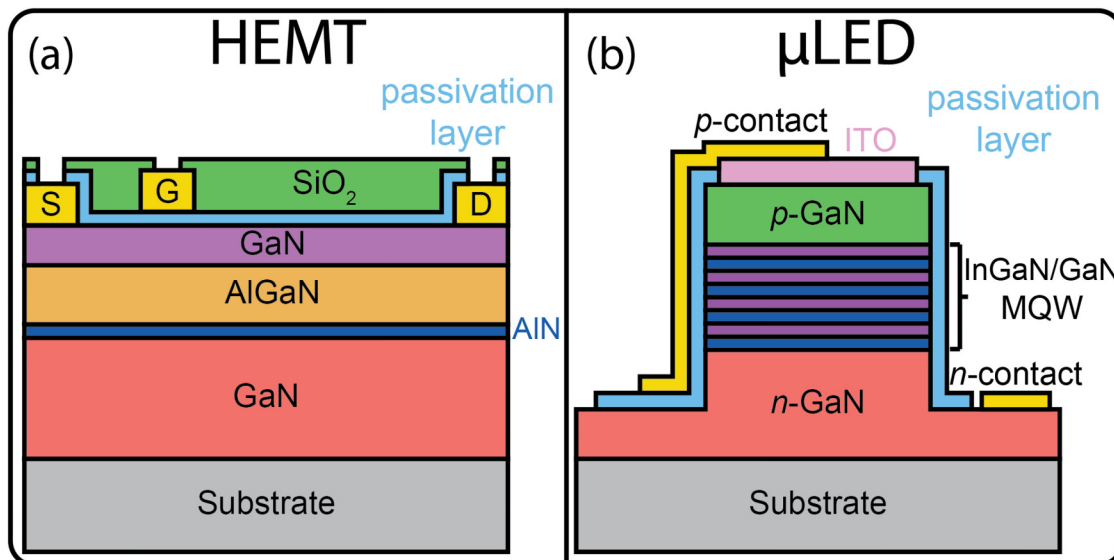


FIG. 18. Schematic illustrations of GaN-based (a) HEMT (Ref. 230) and (b) μLED (Ref. 231) devices. The typical position of the passivation layer (light blue) is shown for both devices. Note that the layer thicknesses are not to scale.

29 April 2025 18:47:46

GaN-based μ LEDs. The passivation layers also acted as an antireflection coating in this case. They showed that the SiO_2 and Al_2O_3 were the most effective passivation layers for reducing sidewall defects. The reported PL efficiencies of the μ LEDs were 25.1% (SiO_2), 21.1% (Al_2O_3), 15.4% (SiN_x), and 10.5% (no passivation).²³¹

VI. CONCLUSION AND OUTLOOK

Defects occurring at the surfaces and interfaces of semiconductors can significantly hamper the development and performance of semiconductor devices and should, therefore, be passivated. Semiconductor surface passivation focuses on obtaining high-quality interfaces with low interface defect density. For silicon, it is relatively straightforward to obtain a high-quality interface, and the remaining defects can typically be further passivated by hydrogen. For germanium and III–V semiconductors, it is often significantly more challenging to form a high-quality interface, and the role of hydrogen passivating the remaining defects occurring at these interfaces is less clear.

In general, the approaches for surface passivation of various semiconductors are highly similar and focus on interface management by removal of the native oxide, followed by surface treatments and/or deposition of passivating (inter)layers, while avoiding the formation of defects. When exploring surface passivation schemes for a novel semiconductor, it can be beneficial to use known passivation schemes of another semiconductor. For example, passivation schemes involving Al_2O_3 , SiN_x , HfO_2 , and $\text{PO}_x/\text{Al}_2\text{O}_3$ have already been investigated on silicon, germanium, and III–V semiconductors. However, due to the high complexity of the interactions between the semiconductor, the passivation scheme, and their interfaces, this can lead to varying degrees of success. Therefore, it is recommended to tailor the passivation schemes to the semiconductor and the application. These types of investigations will allow for the toolbox of semiconductor surface passivation to be further extended and understood.

In the near future, it is likely that continued advances in semiconductor devices will lead to the requirements of passivation schemes to become more stringent. This is likely exacerbated by the current trends of continuous scaling of semiconductor devices and a switch to 3D structured devices. To fulfill these more stringent requirements, the use of stacks of passivation layers is likely to become more commonplace since this provides additional control over the properties of a passivation scheme as compared to the use of a single passivation layer. Furthermore, it is not a given that the currently used passivation approaches are directly compatible with 3D structured devices. Continued research is, therefore, required, in order to achieve proper passivation of semiconductor surfaces with highly stringent requirements. This will allow for further improvement of performance, stability, and reliability of current and future semiconductor devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Roel J. Theeuwes: Conceptualization (equal); Investigation (equal); Visualization (equal); Writing – original draft (equal). **Wilhelmus M. M. Kessels:** Funding acquisition (equal); Supervision (equal); Writing – review & editing (equal). **Bart Macco:** Funding acquisition (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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29 April 2025 18:47:46