

Capping Tools Tame Electromigration

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Interconnects return as problem area as conventional materials run out of steam; new approaches in the works.

By Mark LaPedus
The shift towards the 28nm node and beyond has put the spotlight back on the interconnect in semiconductor manufacturing.

In chip scaling, the big problem in the interconnect is resistance-capacitance (RC). Another, and sometimes forgotten, issue is electromigration. "Electromigration gets worse in device scaling," said Daniel Edelstein, an IBM Fellow and manager of BEOL technology strategy at IBM Corp. "Some of the issues on the table are becoming limiting problems."

Electromigration, which can cause voids and failures in a device, refers to the displacement of the atoms as a result of current flowing through a conductor. To suppress electromigration in the interconnect part of the equation, chipmakers typically use a capping or etch stop layer of material on a dual-damascene structure.

But some warn the conventional capping layer of materials in advanced designs—silicon carbon nitride (SiCN) and a copper alloy—could run out of steam at 20nm and beyond, prompting the need for a new solution. "At 20nm, customers will have to bite the bullet," said Sree Kesapragada, global product manager for metal deposition products at Applied Materials. "Copper does not adhere very well to the dielectric layer. Cobalt is needed for the nanoline."

In fact, there are several new capping layer options for advanced designs. One solution is to somehow extend the current materials. Another option is Lam Research's electroless deposition technology, which deposits cobalt-tungsten-phosphide (CoWP) or a related material. This is already in production in at least one foundry vendor at 32nm.

And a newer option is Applied Materials' in-situ metal/dielectric tool technology for use in depositing cobalt and SiCN. Cobalt-related materials are said to boost electromigration lifetimes by up to hundredfold.

Electromigration in the interconnect

It's still too early to tell which capping technology will prevail in the long run. The capping layer process takes place during the formation of the interconnect in the dual-damascene flow. The interconnects themselves are becoming more compact at each node, causing unwanted RC. To address the problem, the industry must make advances on two fronts: [metallization and low-k dielectrics](#).

The dual-damascene flow includes the following steps: via and trench patterning, barrier layer and copper seed deposition, electroplating and chemical mechanical polishing. Using a deposition technique, the final step in the process is the addition of a capping layer. This is because the interface between the copper line and capping layer is susceptible to electromigration.

Prior to the 90nm node, IC makers generally used silicon nitride (SiN) as the capping layer material. At 130nm and 90nm, chip makers also moved to low-k materials. The trouble was that the dielectric constant of SiN was more than double that of low-k films, which impacted the overall effective k value of the stack.

This, in turn, prompted chipmakers to switch to SiCN materials for the capping layer as a means to reduce capacitance at or around 90nm. SiN has a dielectric constant of 7.0, while SiCN is around 5.0.

Subramani Kengeri, head of advanced technology architecture at GlobalFoundries, said electromigration became more of an issue for the interconnect at the 45nm and 40nm nodes. So to help suppress electromigration, many chipmakers deposited a tiny percentage of a material such as manganese in the copper seed layer using physical vapor deposition (PVD). Manganese or other types of alloys work in conjunction with SiCN. In effect, these types of alloys "find their way to the top and act like a capping layer," said IBM's Edelstein.

At 32nm and beyond, chipmakers would prefer to extend SiCN and the alloy approach without moving to new tool technologies and materials. The problem with this approach is that some of the alloys "diffuse and some of them don't," said Applied's Kesapragada.

The next big material, cobalt, has been proposed because it adheres well to copper. In a structure, IC makers would still use SiCN as the outside metal capping layer. A thin layer of cobalt serves as the interface between the copper and SiCN. Cobalt helps to suppress electromigration, but it adds cost to the equation.

New solutions

Cobalt is getting some traction. For its 32nm processors, Advanced Micro Devices is using a CoWP capping layer, based on Lam Research's electroless deposition tools. These tools reside within GlobalFoundries, which is making the processors on a foundry basis for AMD.

Electroless is a process of depositing a material with the aid of a chemical reducing agent. The origins of Lam's electroless tools can be traced back to Blue29, a startup that developed this technology. One of Blue29's original investors was KLA-Tencor.

In 2004, KLA-Tencor and Dainippon Screen Manufacturing Co. Ltd. formed a joint electroless tool venture and invested in Blue29. But in 2006, KLA-Tencor exited the venture, and subsequently, Lam Research acquired Blue29's intellectual property.

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property.

Electroless deposition "is already running in production at 32nm," said David Hemker, chief technology officer in the corporate technology development group at Lam Research. "The beauty of electroless is that it's selective. It's also more flexible."

Electroless can deposit various materials, such as CoWP, nickel molybdenum phosphide (NoMP) and others. "Regarding the topic of electromigration, there are a lot of ways to address it," Hemker said. "There are so many variants. It's a trade-off between integration and performance."

The electroless approach adds processing steps and increases wafer cost, according to a paper from IBM and Applied Materials at the recent International Interconnect Technology Conference (IITC) in San Jose, Calif. In the paper, the companies also described another capping layer option being developed at Applied Materials for use at 20nm and beyond.

In one possible approach, the capping layer could be handled by two separate machines. One tool provides the SiCN metal capping layer. A separate system deposits cobalt for the interface layer. The problem with this approach is that the structure could suffer from oxidation.

Applied proposes to combine the metal and the dielectric capping layer depositions in a single vacuum platform, according to the paper. The SiCN layer would be provided in one chamber, while the cobalt material would be deposited in a separate chamber.

In one experiment, patterned wafers were fabricated using 32nm CMOS test vehicles. This test was carried out in a copper structure with about 50nm wide lines and spaces as well as 1.5nm and 3nm cobalt films. This method had five to 10 times longer electromigration lifetimes, compared to a method without using cobalt. Module-level time-dependent dielectric breakdown (TDDb) testing was performed. It confirmed no line-to-line dielectric breakdown occurred from the in-situ capping process, according to the paper.

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