

CVD of Nonmetals

Edited by
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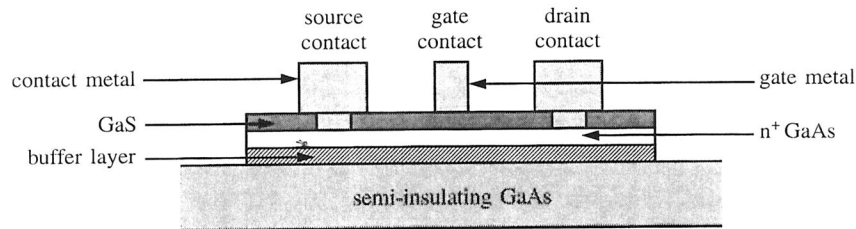


Figure 5-2. Schematic diagram of the GaS/GaAs FETISH.

ductor selected. Recently a new class of GaAs FET using CVD GaS (Sect. 5.6.1) as the gate insulator has been fabricated which satisfies many of these criteria, see Figure 5-2.

5.2.2 Passivation

Passivation is often defined as a process whereby a film is grown on the surface of a semiconductor to either (a) chemically protect it from the environment, or (b) provide electronic stabilization of the surface.

From the earliest days of solid state electronics it has been recognized that the presence or absence of surface states plays a decisive role in the usefulness of any semiconducting material. On the surface of any solid state material there are sites in which the coordination environment of the atoms is incomplete. These sites, commonly termed "dangling bonds", are the cause of the electronically active states which allow for the recombination of holes and electrons. This recombination occurs at energies below the bulk value and interferes with the inherent properties of the semiconductor. In order to optimize the properties of a semiconductor device it is desirable to covalently satisfy all these surface bonds, thereby shifting the surface states out of the band gap and into the valence or conduction bands. Electronic passivation may therefore be described as a process which reduces the density of available electronic states present at the surface of a semiconductor, thereby limiting hole and electron recombination possibilities. Both Si and GaAs require passivation. In the case of silicon both the native oxide (Sect. 5.4.1) and other oxides (Sects. 5.4.2 and 5.4.3) admirably fulfill these requirements. However, GaAs does not grow a suitable oxide [8], and typically employed dielectrics have failed to provide adequate passivation. There has thus been substantial effort targeted at chemical passivation of the surface of GaAs, in particular by gallium sulfides (Sect. 5.6.1).

Chemical passivation requires a material that inhibits the diffusion of oxygen, water, or other species to the surface of the underlying semiconductor. In addition, the material is ideally hard and resistant to chemical attack. In this regard silicon nitride, Si_3N_4 (Sect. 5.5.1), is one of the most widely used materials, and finds applications in both Si and GaAs devices, e.g., Figure 5-1b. A perfect passivation material would satisfy both electronic and chemical passivation requirements, however, while oxide coatings

on silicon are excellent passivation materials, GaAs has until recently not had a suitable material to provide electronic passivation.

5.2.3 Planarization

For the vast majority of electronic devices, the starting point is a substrate consisting of a flat single crystal wafer of semiconducting material. During processing, which includes the growth of both insulating and conducting films, the surface becomes increasingly non-planar. For example, a gate oxide in a typical MOSFET (see Fig. 5-1a) may be typically 100–250 Å thick, while the isolation or field oxide may be 10000 Å. In order for the successful subsequent deposition of conducting layers (metallization) to occur without breaking metal lines (often due to the difficulty in maintaining step coverage), the surface must be flat and smooth. This process is called planarization [9], and can be carried out by a technique known as sacrificial etchback. The steps for this process are outlined in Figure 5-3. An abrupt step (Fig. 5-3a) is coated with a conformal layer of a low melting dielectric, e.g., borophosphosilicate glass (Figure 5-3b), and subsequently a sacrificial organic resin (Fig. 5-3c). The sample is then plasma

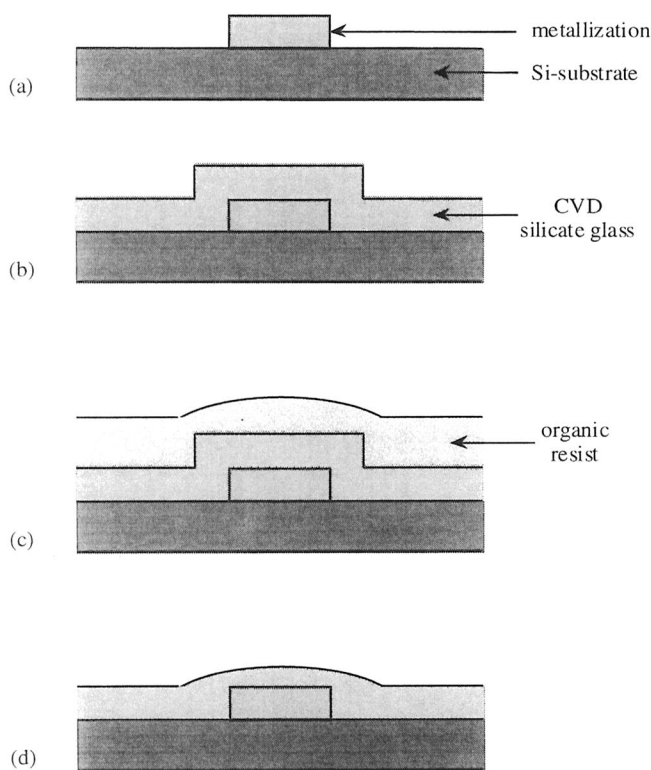


Figure 5-3. Schematic representation of the planarization process. (a) A metallization feature is CVD covered with silicate glass (b), and (c) subsequently coated with an organic resin. (d) After etching the resist a smooth silicate surface is produced.

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Figure 5-
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