

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., LTD.
Petitioner

v.

Optronic Sciences LLC
Patent Owner

Inter Partes Review No.: IPR2024-01133

**DECLARATION OF DR. R. JACOB BAKER IN SUPPORT OF PETITION
FOR INTER PARTES REVIEW OF U.S. PATENT NO. 9,263,509**

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Exhibit No.	Description
1001	U.S. Patent No. 9,263,509
1002	File History of U.S. Patent No. 9,263,509
1003	Declaration of R. Jacob Baker, Ph.D., P.E.
1004	U.S. Patent Publication No. 2004/0079945 (“Weaver”)
1005	U.S. Patent Publication No. 2012/0162053 (“Lee053”)
1006	U.S. Patent Publication No. 2014/0183502 (“Song”)
1007	Korean Patent Publication No. 10-2014-0088369 (“Song KR”)
1008	Certified Translation of Song KR
1009	U.S. Patent 9,088,003 (“Gupta”)
1010	U.S. Patent Publication No. 2011/0248309 (“Han”)
1011	U.S. Patent Publication No. 2009/0015149 (“Lee149”)
1012	U.S. Patent Publication 2006/0119259 (“Bae”)
1013	Wiley Electrical and Electronics Engineering Dictionary (2004)

CHART OF CLAIMS	
[1pre]	A pixel structure, comprising:
[1a]	a data line and a scan line;
[1b]	at least one active device electrically connected with the data line and the scan line, and each active device comprising a gate, a channel layer, a source, and a drain;
[1c]	a first auxiliary electrode electrically insulated from the active device; and
[1d]	a light emitting device disposed above the first auxiliary electrode, wherein the light emitting device comprises:
[1e]	a first electrode layer electrically connected with the first auxiliary electrode;
[1f]	a light emitting layer disposed on the first electrode layer; and
[1g]	a second electrode layer disposed on the light emitting layer, wherein the second electrode layer is electrically connected with the active device.
[2]	The pixel structure according to claim 1, further comprising a first insulating layer covering the active device and the first auxiliary electrode, and the first electrode layer of the light emitting device being disposed on the first insulating layer, wherein the first insulating layer has a first contact window opening that exposes the first auxiliary electrode, and the first electrode layer is electrically connected with the first auxiliary electrode via the first contact window opening.
[3]	The pixel structure according to claim 2, further comprising a second insulating layer covering the first insulating layer and the first electrode layer of the light emitting device, and the second electrode layer of the light emitting device being disposed on the second insulating layer, wherein the second insulating layer has an opening that exposes the first electrode layer, and the light emitting layer of the light emitting device is disposed in the opening.
[4]	The pixel structure according to claim 3, wherein the first insulating layer and the second insulating layer further comprise a second contact window opening that exposes a portion of the active device, and the second electrode layer of the light emitting device is electrically connected with the active device via the second contact window opening.
[5]	The pixel structure according to claim 1, wherein the first auxiliary electrode is a single electrode layer.
[6pre]	The pixel structure according to claim 1, wherein the first auxiliary electrode comprises:
[6a]	a bottom electrode layer; and

CHART OF CLAIMS
[6b] a top electrode layer electrically connected with the bottom electrode layer, wherein the first electrode layer of the light emitting device is electrically connected with the top electrode layer of the first auxiliary electrode.
[7] The pixel structure according to claim 6, wherein the bottom electrode layer and the gate of the active device belong to the same layer.
[8] The pixel structure according to claim 6, wherein the top electrode layer and the source and the drain of the active device belong to the same layer.
[9] The pixel structure according to claim 1, further comprising an isolating structure disposed around the second electrode layer of the light emitting device, wherein a gap exists between the second electrode layer and the isolating structure.
[10] The pixel structure according to claim 1, further comprising a second auxiliary electrode electrically insulated from the active device and disposed at a side of the light emitting device, wherein the second auxiliary electrode is electrically connected with the first electrode layer of the light emitting device.
[11] The pixel structure according to claim 10, wherein the second auxiliary electrode and the second electrode layer of the light emitting device belong to the same layer, and the second auxiliary electrode and the second electrode layer of the light emitting device are electrically insulated from each other.
[12] The pixel structure according to claim 1, wherein the light emitting device is a top-emission organic electroluminescent device.
[13] The pixel structure according to claim 1, wherein a vertical projection of the light emitting layer of the light emitting device at least partially overlaps the first auxiliary electrode.

I. INTRODUCTION

I, R. Jacob Baker, declare as follows:

1. My name is R. Jacob Baker. I have been asked by Petitioners BOE Technology Group Co., LTD. to provide my expert opinions in support of the above-identified petition for inter partes review of claims 1-13 (“Challenged Claims”) of U.S. Patent No. 9,263,509 (“509 patent,” EX1001), owned by Optronix Sciences LLC (“PO”), pursuant to 35 U.S.C. §§311–19 and 37 C.F.R. §42.100.

2. I currently hold the opinions set forth in this declaration.

3. In summary, it is my opinion that the references cited below anticipate or render obvious the Challenged Claims. My detailed opinions on the claims are set forth below.

4. I am being compensated for my time at the rate of \$765 per hour. This compensation is not contingent upon my performance, the outcome of this matter, or any issues involved in or related to this matter.

II. BACKGROUND AND QUALIFICATION

A. Background

5. My qualifications generally are set forth in my Curriculum Vitae, which is attached as **Appendix B**. Appendix B also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

6. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (“UNLV”).

7. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

8. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled “Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

B. Industry Experience

9. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for

underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

10. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

11. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. ("MTI") in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts

resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and

2010. This work entailed the design of low-power, high-speed, and wide interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

12. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density 3D packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc. From 1994 to 1996, I worked on the design of displays at Micron Display and

Micron Technology, Inc. (“Micron”) in Boise, Idaho. This work was at a time when cathode ray tubes (CRTs) were still the dominant type of display. Flat panel displays were being developed with the hope of replacing CRTs in the consumer market. I worked on flat panel displays which resulted in 5 patents: 5,598,156, 5,638,085, 5,818,365, 5,894,293, and 5,909,201. I worked on the design of the pixels, both active and passive, as well as the supporting electronics for processing video signals. I was involved with the evaluation of display technologies including liquid crystal displays (LCDs), light-emitting diodes, plasma displays, and organic light emitting diode (OLED) displays; the display technologies that were looking to displace CRTs in the consumer market. I was also involved with the packaging of the displays including the vacuum sealing and deposition of the phosphors for light wavelength conversion. I also taught display design as a topic in my courses and did display design consulting again in industry for Cirque in 2013.

13. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (Light Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The

knowledge and experience gained from this effort are reflected in my textbook CMOS Mixed-Signal Circuit Design and a presentation, which I have present-ed at several universities and companies,

http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf.

C. Academic Experience

14. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University (“BSU”), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university’s second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

15. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the “Father of Silicon

Valley”). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

16. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). I contributed as an editor and co-author on several other electrical and computer engineering books.

D. Other Relevant Experience

17. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

18. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-2024). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

19. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

III. DOCUMENTS AND OTHER MATERIALS RELIED UPON

20. In forming the opinions set forth in this declaration, I have reviewed the documents in the following table:

Exhibit No.	Description
1001	U.S. Patent No. 9,263,509
1002	File History of U.S. Patent No. 9,263,509
1004	U.S. Patent Publication No. 2004/0079945 (“Weaver”)
1005	U.S. Patent Publication No. 2012/0162053 (“Lee053”)
1006	U.S. Patent Publication No. 2014/0183502 (“Song”)
1007	Korean Patent Publication No. 10-2014-0088369 (“Song KR”)
1008	Certified Translation of Song KR
1009	U.S. Patent 9,088,003 (“Gupta”)
1010	U.S. Patent Publication No. 2011/0248309 (“Han”)
1011	U.S. Patent Publication No. 2009/0015149 (“Lee149”)
1012	U.S. Patent Publication 2006/0119259 (“Bae”)
1013	Wiley Electrical and Electronics Engineering Dictionary (2004)

21. Additionally, I have utilized my own experience and expertise, including regarding the knowledge and capabilities of a person of ordinary skill in the relevant art in the timeframe of the claimed priority date of the 509 patent.

IV. STATUTORY GROUNDS FOR CHALLENGE

22. In this declaration, I offer opinions on the following grounds that are the basis for this IPR proceeding:

Ground	Claims	Stat. Basis	Prior Art
1	1-5, 9, 12-13	35 U.S.C. § 102	Weaver
2	6-8	35 U.S.C. § 103	Weaver and Lee053
3	6-8	35 U.S.C. § 103	Weaver and Song
4	10-11	35 U.S.C. § 103	Weaver and Lee149
5	10-11	35 U.S.C. § 103	Weaver and Bae
6	1-5, 9, 12-13	35 U.S.C. § 103	Weaver in view of Gupta or Han
7	6-8	35 U.S.C. § 103	Weaver and Lee053, in view of Gupta or Han
8	6-8	35 U.S.C. § 103	Weaver and Song, in view of Gupta or Han
9	10-11	35 U.S.C. § 103	Weaver and Lee149, in view of Gupta or Han
10	10-11	35 U.S.C. § 103	Weaver and Bae, in view of Gupta or Han

V. RELEVANT PATENT LAW AND LEGAL STANDARDS

A. Date of Invention

23. I have been asked to use the date of the filing of the earliest application to which priority is claimed (i.e., September 12, 2013) as the date of invention for purposes of my analysis.

B. Anticipation

24. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 102 if a prior art disclosure teaches every element required by the claim, either expressly or inherently. The identical invention must be shown in as complete detail as is contained in the claim. When a claim covers several structures

or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art.

C. Obviousness

25. I am informed and understand that a patent claim is invalid under 35 U.S.C. § 103 if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art to which the subject matter pertains. Obviousness, as has been explained to me, is based on (i) the scope and content of the prior art, (ii) the differences between the prior art and the claim, (iii) the level of ordinary skill in the art, and (iv) any secondary indicia of non-obviousness (*e.g.*, “secondary considerations” such as commercial success in the marketplace of the claimed invention), to the extent that they exist.

26. I further understand that obviousness may be demonstrated by showing that it would have been obvious to combine the teachings of more than one item of prior art. In determining whether a piece of prior art could have been combined with other prior art or with other information within the knowledge of a person having ordinary skill in the art, the following are examples of approaches and rationales that may be considered:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of a known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- Applying a technique or approach that would have been obvious to try (choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success);
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a person having ordinary skill in the art; and
- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

27. I further understand that an invention may be obvious if one of ordinary skill in the art, facing a wide range of needs created by developments in the field, would have seen an obvious benefit to the solutions tried by the applicant. When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, it may be obvious to a person of ordinary skill to try the known options. If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious.

28. I further understand that a person of ordinary skill in the art is a hypothetical person who is presumed to be aware of all of the relevant art at the time of the invention. The person of ordinary skill may be able to fit together the teachings of multiple patents and/or printed publications employing ordinary creativity and the common sense that familiar items may have uses in another context or beyond their primary purposes.

29. I also understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when combining or modifying the prior art. I understand this test should not be applied rigidly, but that the test can be important to avoid such hindsight.

30. I also understand that one of ordinary skill in the art must have a reasonable expectation of success in combining or modifying prior art references.

31. I also understand that all elements of a claim must be considered in an obviousness analysis.

D. Claim Construction

32. I understand that claim construction is solely a matter for the Administrative Law Judge (ALJ) to decide and, in general, the ordinary meaning of the claim terms used in the patent to one of ordinary skill in the art is determined in the context of the patent's specification and the file history.

33. I understand that ultimately the ALJ will determine how specific terms shall be construed. The intent of this report is to help inform the ALJ about how a person of ordinary skill in the art would have understood the meaning of certain disputed claim terms at the time of the claimed inventions in the context of the Asserted Patents' claims, specifications, and prosecution histories in a manner that will assist the ALJ in the process of construing the claims.

34. I understand that claims are construed from the perspective of a person of ordinary skill as of the effective filing date of the patent application. A "person of ordinary skill in the art" is a hypothetical person who is presumed to have known the relevant art at the time of the invention.

35. I understand that persons of ordinary skill in the art are deemed to read the claims in the context of the entire patent, including the specification and prosecution history. In other words, the terms are not considered in a vacuum.

36. I understand that the claims define the invention and the terms used in the claims are generally given the plain and ordinary meanings they would have to a person of ordinary skill in the art at the time of the effective filing date of the application. The context of a claim can be particularly helpful, and other claims may inform the meaning of a term in a particular claim. Terms are normally used consistently throughout a patent. Thus, the meaning of a term may help inform the meaning of the same term in other claims. Differences between claims may also help define the terms, although this may not be the case where the specification or prosecution history indicate that such differences do not impact the scope of the claims.

37. I understand that a patentee can act as its own lexicographer by defining a term, in the patent specification, to have specific meaning. It is my understanding that statements made to the patent office by the patentee or its legal representative during prosecution can serve to illuminate, or possibly narrow the proper scope of claim terms, and that such statements must be considered when construing the claim terms. This is sometimes referred to as disclaimer. I have taken into account these principles in my analysis.

38. I understand that reference materials that were publicly available at the time that the patent application was filed, such as dictionaries, treatises or other technical references, may provide context and background for deciphering how one of ordinary skill in the art would have considered the terms used in the claims. However, I understand that such references, as well as testimony (including this report) are generally known as “extrinsic evidence,” and are accorded less weight than evidence found within the patent and prosecution history. In addition, I understand that extrinsic evidence that is inconsistent with the claims, specification, or prosecution history should not be considered in the claim construction process.

E. Section 112(f) Means Plus Function

39. I understand that under pre-America Invents Act (AIA) 35 U.S.C. § 112(6) and post-AIA § 112(f) “*An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.*”

40. I understand that when claim terms use the words “means . . . for” and recites a function, and the term does not recite any structure for performing that function, the term should be construed pursuant to Section 112(f) looking for a

corresponding structure, material, or act described in the specification and equivalents.

F. Section 112 Definiteness

41. I understand that “[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.”¹

42. I understand that that claims must be definite. This means that the claims must particularly point out and distinctly claim the subject matter that the applicant regards as her invention. I understand that indefiniteness is evaluated from the perspective of a person of ordinary skill in the art at the time of a patent’s filing. I understand that a patent claim is indefinite if the claim, when read in light of the specification and the prosecution history, fails to inform, with reasonable certainty, a person of ordinary skill in the art of the scope of the invention.

Absolute or mathematical precision in claim language is not required and even if more than one interpretation is presented for a claim term, the term may still be definite if an informed and confident choice is available among the contending alternative definitions.

¹ I understand that the quoted text comes from the patent statute, 35 U.S.C. § 112 ¶ 2.

G. Standard of Proof

43. I understand that the standard to prove unpatentability in an *inter partes* review proceeding is by a preponderance of the evidence, which means more likely than not.

VI. LEVEL OF ORDINARY SKILL IN THE ART

44. I have considered the level of ordinary skill in the art relevant to the 509 patent. I understand that factors such as the education level of those working in the field, the sophistication of the technology, the types of problems encountered in the art, the prior art solutions to those problems, and the speed at which innovations are made may help establish the level of skill in the art.

45. After reviewing the 509 patent, the relevant portions of the prosecution history of the 509 patent and its reexamination, and cited references, it is my opinion that the relevant art of the 509 patent is in the field of electronic and optoelectronic system design.

46. Based upon my knowledge of this field, I conclude that a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the 509 patent (September 12, 2013), and for that matter, at all subsequent times through the present, would have had a Bachelors’ degree in electrical engineering or a comparable field of study, plus approximately one or more years of professional experience with electronic and optoelectronic system design. Additional graduate

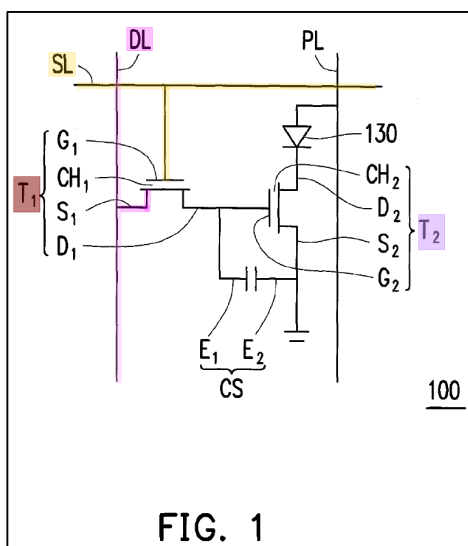
education could substitute for professional experience, and significant experience in the field could substitute for formal education.

47. I am and was at the time of the earliest filing date at least a person of skill in the relevant art and I am able to provide insight and opinions into the understandings of such persons at all relevant times by virtue of my education, training and experience.

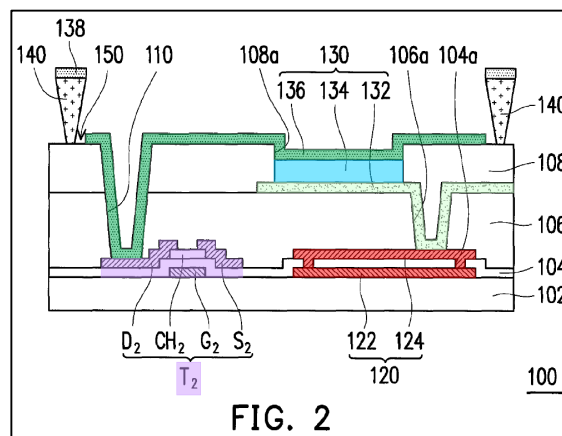
VII. THE 509 PATENT AND ITS PROSECUTION HISTORY

A. Overview of the 509 Patent

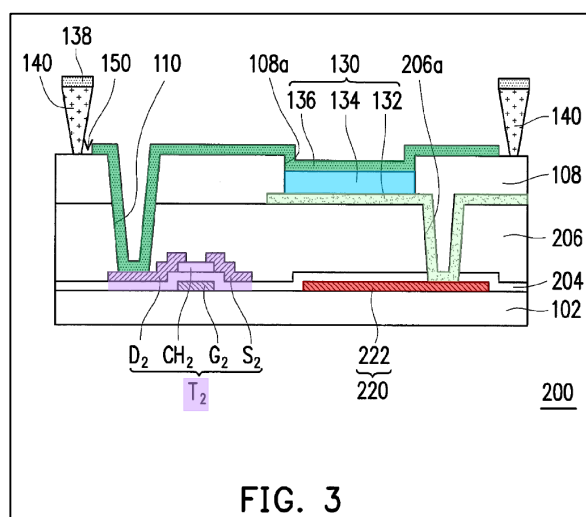
48. The 509 patent is directed to a pixel structure for solving the purported problem of poor overall luminous uniformity that occurs in traditional electroluminescent devices. EX1001, 1:48-50. The 509 patent discloses a pixel structure 100 that includes a data line DL, a scan line SL, active device T1, active device T2, a capacitor CS, a power line PL, and a light emitting device 130. *Id.*, 2:65-3:1 and Fig. 1.



49. The light emitting device 130 includes a first electrode layer 132, a light emitting layer 134, and a second electrode layer 136. *Id.*, 4:36-38. The purported novelty is the inclusion of a first auxiliary electrode 120 that is electrically connected with the first electrode layer 132, where the light emitting device 130 is located above the first auxiliary electrode 120. *Id.*, 4:35-36, 47-49; Fig. 2.

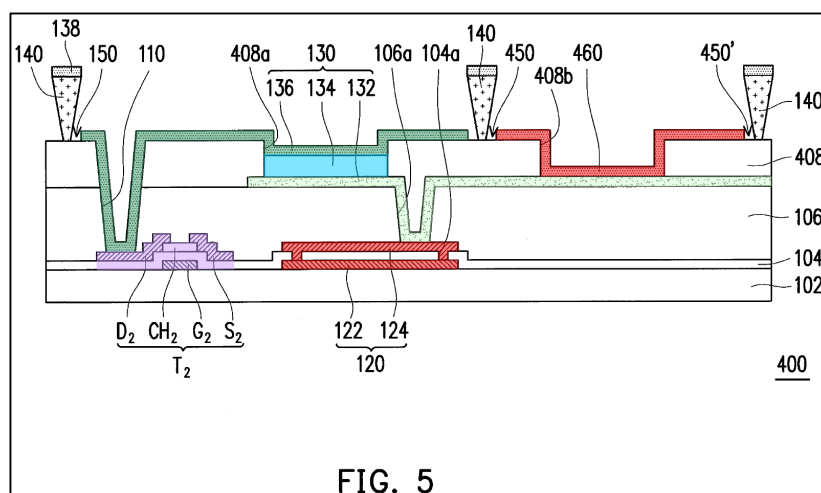


50. In one embodiment, the first auxiliary electrode 120 includes a bottom electrode layer 122 and a top electrode layer 124. *Id.*, 4:6-8; Fig. 2. In another embodiment, the first auxiliary electrode 120 includes only a bottom electrode layer 222. *Id.*, 6:29-34; Fig. 3.



51. In yet another embodiment, the pixel structure additionally includes a second auxiliary electrode 460 that is located at a side of the light emitting device 130 and also is electrically connected to the first electrode layer 132. *Id.*, 7:1-5;

Fig. 5.



B. Overview of the 509 patent's File History

52. I have found at least the following from the file history that may be relevant.

53. On July 31, 2014, PO filed U.S. Appl. No. 14/447,620, claiming priority to Tawain application 102133040, filed September 12, 2013. Ex1001, cover.

54. On March 16, 2015, the Examiner issued an office action, finding patentably distinct species corresponding to Figures 2 and 6. EX1002, PDF pages 411-417.

55. On May 7, 2015, PO submitted a response electing Species I corresponding to Figure 2, with a traverse of the restriction requirement. EX1002, PDF pages 399-407.

56. On June 24, 2015, the Examiner issued an office action, finding the restriction requirement proper. EX1002, PDF pages 382-387.

57. On August 21, 2015, PO submitted a response cancelling claims 14-18. EX1002, PDF pages 364-371.

58. On October 7, 2015, the Examiner issued a notice of allowance. EX1002, PDF pages 180-188.

59. On February 16, 2016, the '620 application issued as the 509 patent. EX1001, cover.

VIII. CLAIM CONSTRUCTION

60. I have been asked to consider and apply the claim constructions discussed below. For any claim terms not listed below I have applied their plain and ordinary meaning to a POSITA at the time of the 509 patent.

A. “auxiliary electrode” (claims 1-2, 5-6, 10-11, 13)

61. “Auxiliary electrode” should be construed either broadly as “supplemental electrode” or narrowly as “supplemental electrode to reduce the total resistance of the pixel structure.” As I set forth below, I have applied the broad construction in Grounds 1-5 and the narrow construction in Grounds 1-10.

62. The claims do not explicitly state what the “auxiliary electrode” is auxiliary to, i.e., the claims do not explicitly recite what function or characteristic existed without the auxiliary electrode that has been supplemented with the auxiliary electrode. If the absence of this recitation in the claim sufficiently begs the question such that a POSITA would have turned to the specification to understand the nature of the claimed “auxiliary electrode,” or if other statements in the specification sufficiently limit the term, then a narrow construction is appropriate. The prosecution history provides no guidance on this issue.

63. In support of the broad construction, the plain meaning of “auxiliary” is “supplemental” and is not limited to any particular type of supplemental functionality. EX1013, p. 51 (“supplementary” or “supplemental”

included in each of the definitions of “auxiliary anode,” “auxiliary channel,” “auxiliary circuit,” “auxiliary contacts,” “auxiliary device,” “auxiliary equipment,” “auxiliary function,” “auxiliary power,” “auxiliary relay”). In the Summary of the Invention section, the 509 patent includes the following sentence:

Based on the above, in the pixel structure of the invention, the first electrode layer of the light emitting device is electrically connected with the auxiliary electrode.

EX1001, 2:15-17. The Description of the Embodiments section contains similar statements. *Id.*, 4:47-49, 5:63-6:4, 6:53-58; 7:1-5 and 43-45. These statements are consistent with the broad construction that encompasses any supplemental electrode for any purpose.

64. In support of the narrow construction, the 509 patent follows the above sentence in the Summary of the Invention section with the following:

Therefore, the design of the invention that coordinates the first electrode layer of the light emitting device with the auxiliary electrode decreases the resistance of the first electrode layer through parallel connection, so as to significantly reduce the total resistance of the pixel structure, thereby improving the overall luminous uniformity of the display panel.

EX1001, 2:15-23. The Description of the Embodiments section contains similar statements. *Id.*, 5:63-6:8; 7:45-56. To the extent a POSITA reads the claim and finds “auxiliary” ambiguous, such that the POSITA would turn to the specification to understand what makes the claimed auxiliary electrode “auxiliary,” these statements would resolve that ambiguity and would limit the claim. Additionally,

these statements refer to “the invention” which a POSITA would have understood can limit the term as well. However, it should be noted that each of the two statements in the Description of the Embodiments section cited above is followed by the explicit disclaimer that “the invention is not limited thereto.” *Id.*, 6:8-9; 7:56-57.

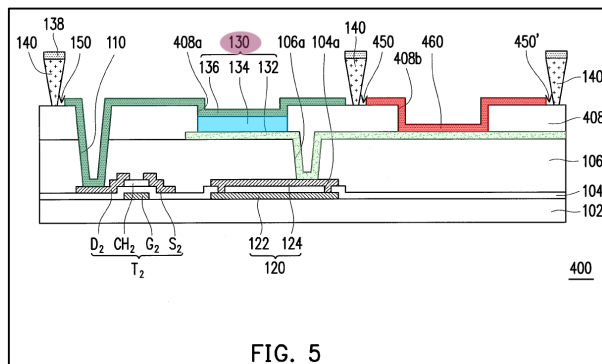
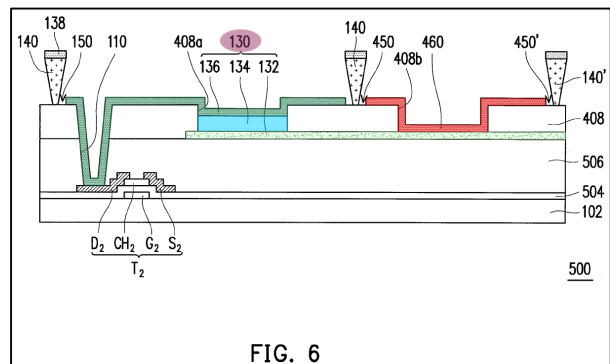
65. I do not include “decreases the resistance of the first electrode layer” or “decreases the resistance of the first electrode layer through parallel connection” in the proposed narrow construction because a POSITA would have known that adding an auxiliary electrode cannot literally perform that function. The first electrode layer has a resistance determined by its physical properties (material, dimensions, etc.), which cannot be changed by adding an electrode (even if connected in parallel). A POSITA would have understood that adding an electrode connected in parallel with the first electrode would decrease the resistance of the combined parallel circuit by allowing current to flow in parallel through the first electrode and the added electrode, but would not reduce the resistance of the first electrode itself. Thus, a POSITA would have interpreted this passage in the specification as imprecisely referring to the concept of reducing overall resistance, not the impossibility of reducing the resistance of the unaltered first electrode itself. A construction that literally requires that the auxiliary electrode reduce the resistance of the first electrode itself is not disclosed or enabled by the 509 patent.

B. “disposed at a side of” (claim 10)

66. This phrase in the context of claim 10 means the auxiliary electrode “overlaps in the horizontal direction” with the light emitting device (LED). This phrase should not be interpreted to include a negative limitation that precludes the auxiliary electrode from also vertically overlapping with some part of the LED.

This is a comprising claim, so the auxiliary electrode could do both.

67. Any construction that precludes any amount of overlap in the vertical direction, or requires complete overlap in the horizontal direction, should be rejected because it would exclude all disclosed embodiments. In the only two embodiments of the 509 patent that include the **second auxiliary electrode 460** “at a side” of the **light emitting device 130** (which is defined as **first electrode layer 132**, **light emitting layer 134** and **second electrode layer 136**), there is partial vertical overlap of the **second auxiliary electrode 460** and the **first electrode layer 132** of the light emitting device 130 (i.e., a portion of the **second auxiliary electrode 460** is formed on a portion of the **first electrode layer 132**). EX1001, Figs. 5 and 6.



Further, there is also no complete overlap of the **second auxiliary electrode 460** and the LED in the horizontal direction, because there is no overlap of the **second auxiliary electrode 460** and the **first electrode layer 132** in the horizontal direction.

Id.

68. Yet, second auxiliary electrode 460 in Figs. 5 and 6 is disclosed as being “located at a side of the light emitting device 130.” *Id.*, 7:1-5; 8:4-8. Therefore, an electrode disposed “at a side of the light emitting device” as used in the 509 patent does not preclude partial vertical overlap of the electrode and at least one of the layers of the light emitting device, nor does it require complete horizontal overlap of the electrode and all of the layers of the light emitting device. If an electrode disposed “at a side of” precluded any vertical overlap of the electrode with any of the three layers that define the light emitting device 130, or required complete horizontal overlap therebetween, then claim 1 would not read on any of the disclosed embodiments.

IX. OVERVIEW OF THE PRIOR ART REFERENCES

A. EX1004 – Weaver

69. U.S. Patent Publication No. 2004/0079945 (“Weaver”) was filed on 10/28/2002, and published on 4/29/2004. Weaver is prior art under post-AIA 35 U.S.C. § 102(a)(1).

B. EX1005 – Lee053

70. U.S. Patent Publication No. 2012/0162053 (“Lee053”) was filed on 12/22/2011, and published on 6/28/2012. Lee 053 is prior art under post-AIA 35 U.S.C. § 102(a)(1).

C. EX1006 – Song

71. U.S. Patent Publication No. 2014/0183502 (“Song”) was filed on 12/26/2013, and published on 7/3/2014.

72. Song claims priority to Korean Application 10-2013-0000181, filed on 1/2/2013, and published as 10-2014-0088369 (EX1007 – “Song KR”). A certified translation of Song KR is provided as EX1008. In reviewing Song KR, it includes an enabling disclosure of all the relevant features disclosed in Song relied upon herein. Therefore, Song has an effective filing date of 1/2/2013, and is prior art under post-AIA 35 U.S.C. § 102(a)(2).

D. EX1009 – Gupta

73. U.S. Patent No. 9,088,003 (“Gupta”) was filed on 3/6/2013, and issued on 7/21/2015. Gupta is prior art under post-AIA 35 U.S.C. § 102(a)(2).

E. EX1010 – Han

74. U.S. Patent Publication No. 2011/0248309 (“Han”) was filed on 4/1/2011, and issued on 10/13/2011. Han is prior art under post-AIA 35 U.S.C. § 102(a)(1).

F. EX1011 – Lee149

75. U.S. Patent Publication No. 2009/0015149 (“Lee149”) was filed on 07/09/2008, and published on 1/15/2009. Lee149 is prior art under post-AIA 35 U.S.C. § 102(a)(1).

G. EX1012 – Bae

U.S. Patent Publication No. 2006/0119259 (“Bae”) was filed on 11/29/2005, and published on 06/08/2006. Bae is prior art under post-AIA 35 U.S.C. § 102(a)(1).

X. GROUND 1: CLAIMS 1-5, 9, 12-13 ARE ANTICIPATED BY WEAVER

76. The format I use for the discussion of each claim limitation begins with a quote of the claim language in which parentheticals have been added which include exemplary arguments and evidence. This quote of the claim language is to orient the reader and the parentheticals are exemplary of my opinions. However, my opinions additionally include all of the following discussion and any cross-referenced sections.

77. The construction of “auxiliary electrode” I applied for Ground 1 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

A. Claim 1

1. [1pre]

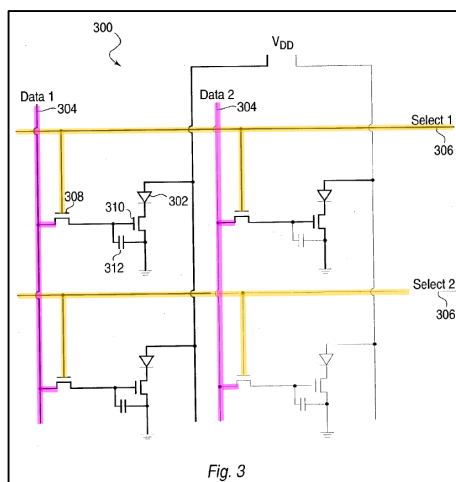
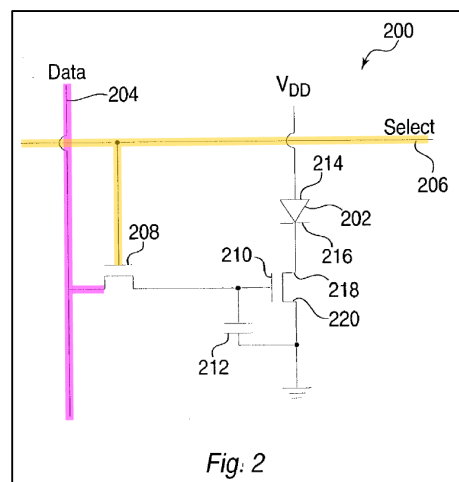
78. To the extent that the preamble is limiting, Weaver discloses “a pixel structure (Weaver’s circuit/array 300).”

79. Weaver discloses circuit 300 that includes OLEDs and transistors in an array configuration that may be used in devices such as displays, and a process flow for forming “a pixel” that includes the OLEDs and transistors. EX1004, [0021], [0022], [0032], Figs. 3-8.

2. [1a]

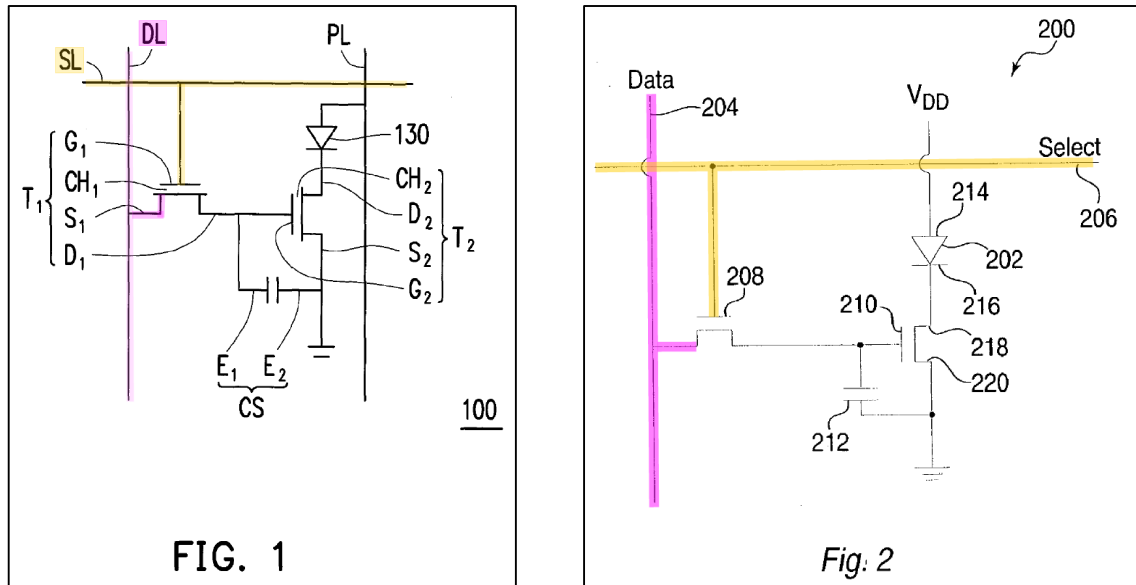
80. Weaver discloses “a data line (data line 304) and a scan line (select line 306).”

81. Weaver discloses that each circuit of Fig. 3 is connected to a data line 304 and a select line 306. EX1004, Fig. 3, [0021], *see also*, Fig. 2, [0019] (data line 204 and select line 206).



A voltage applied to the **select line 306** will turn on transistor 308. *Id.*, Fig. 3, [0017].

82. Fig. 1 of the 509 patent and Fig. 2 of Weaver are reproduced below:

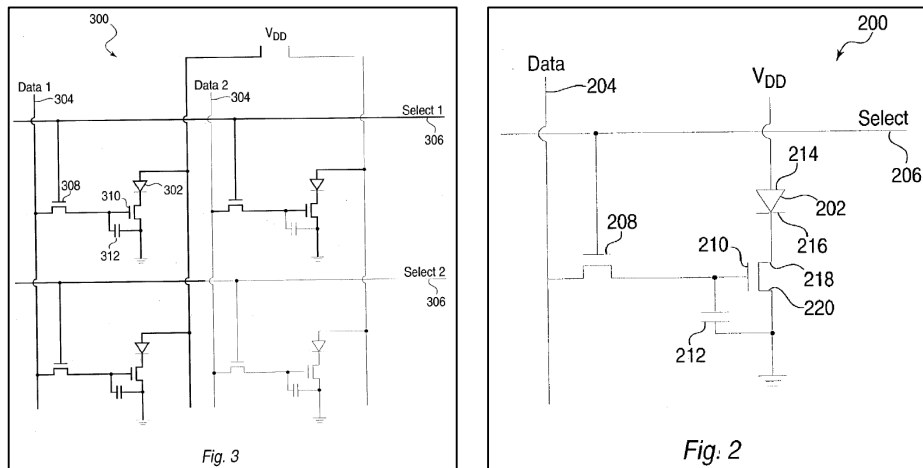


The circuit designs are essentially identical in both configuration and function with respect to the line configuration. A POSITA would have understood that the data line 204/304 of Weaver performs the same function as the data line DL of the 509 patent, namely, providing image data to the pixel (shorthand for picture element). Similarly, a POSITA would have understood that the select line 206/306 of Weaver performs the same function as the scan line SL of the 509 patent, namely, accessing a row of pixels to allow the image data to be written into the pixel via the data line DL.

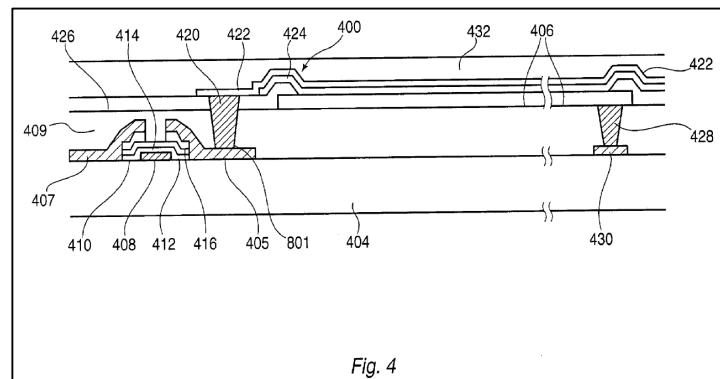
3. [1b]

83. Weaver discloses “at least one active device (transistor 208/308 and transistor 210/310/410) electrically connected with the data line (204/304) and the scan line (206/306), and each active device comprising a gate (gate 408), a channel layer (a-Si layer 414), a source (source 220/405), and a drain (drain 218/407).”

84. Weaver discloses that each of the circuits in Fig. 3 is a circuit such as that shown in Fig. 2. EX1004, [0021].

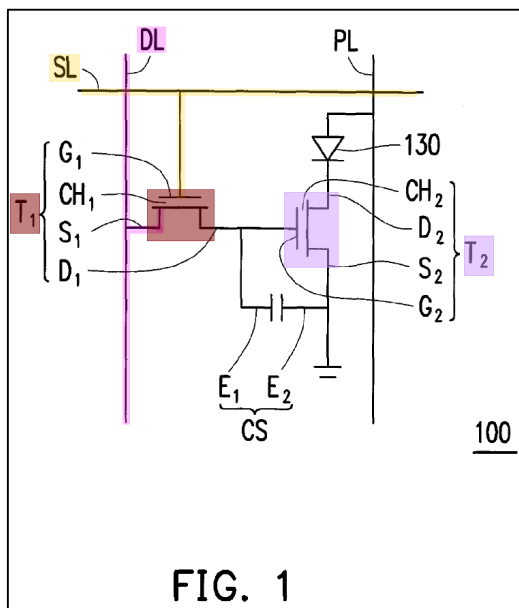
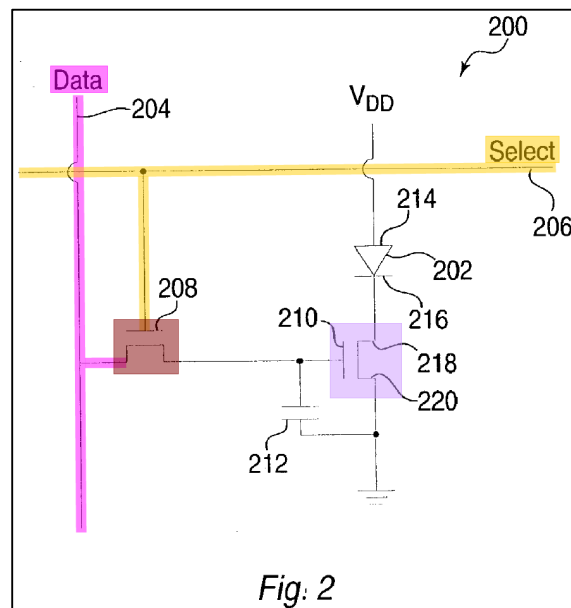


Weaver also discloses that the OLED 400 and transistor 410 in Fig. 4 may be the elements of an array such as shown in Fig. 3. *Id.*, [0022].

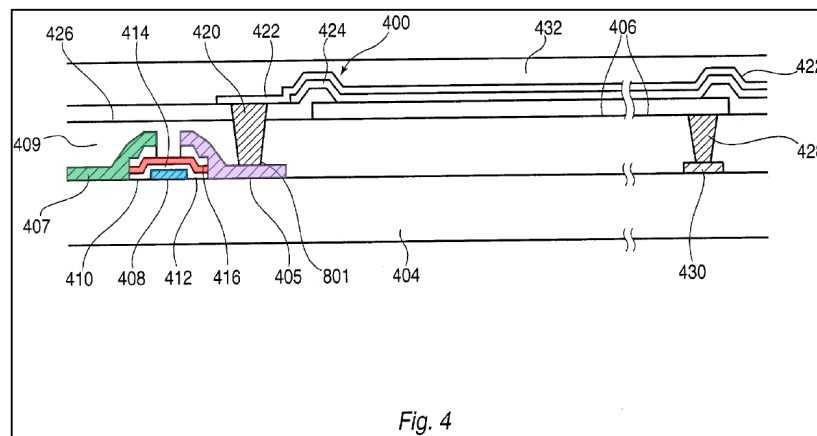


Therefore, transistor 210 in Fig. 2, transistor 310 in Fig. 3 and transistor 410 in Fig. 4 refer to the same transistor. Similarly, transistor 208 in Fig. 2 and transistor 308 in Fig. 3 refer to the same transistor. Further, OLED 202 in Fig. 2, OLED 302 in Fig. 3 and OLED 400 in Fig. 4 refer to the same OLED. Finally, data lines 204 and 304 refer to the same data line and select lines 206 and 306 refer to the same select line.

85. Weaver discloses at least one active device (transistor 208/308 and transistor 210/310/410) that are electrically connected with a data line 204/304 and a scan (select) line 206/306. *Id.*, [0019], [0021], Figs. 2-4. It should be noted that Weaver discloses a pixel structure circuit (with transistors 208/308 and 210/310/410) that is identical to the only disclosed pixel structure circuit embodiment in the 509 patent (with transistors T1 and T2), as evidence from a comparison of Fig. 1 of the 509 patent (EX1001, Fig. 1) and Fig. 2 of Weaver (EX1004, Fig. 2):



86. The active device (transistor 210/310/410) includes a gate 408, an a-Si layer 414, a source 220, 405, and a drain 218, 407. *Id.*, [0019], [0024], Fig. 2-4.



A POSITA would have understood that the a-Si layer 414 forms a channel layer for transistor 410. The 509 patent discloses that transistors are active devices. EX1001, 3:33-59.

87. Weaver acknowledges that transistor 210/310/410 (having a gate, a channel layer, a source and a drain) is also referred to as a thin film transistor.

EX1004 [0008], [0019]. Weaver discloses that in the embodiment of Fig. 2 (which shows two transistors 208 and 210), “n-type thin film transistors are also used, which may be n-type thin film transistors.” *Id.*, [0018]. Given this disclosure regarding plural “transistors” with respect to Fig. 2, a POSITA would have understood that transistor 208/308 is also a thin film transistor (i.e., one that has a gate, a channel layer, a source and a drain).

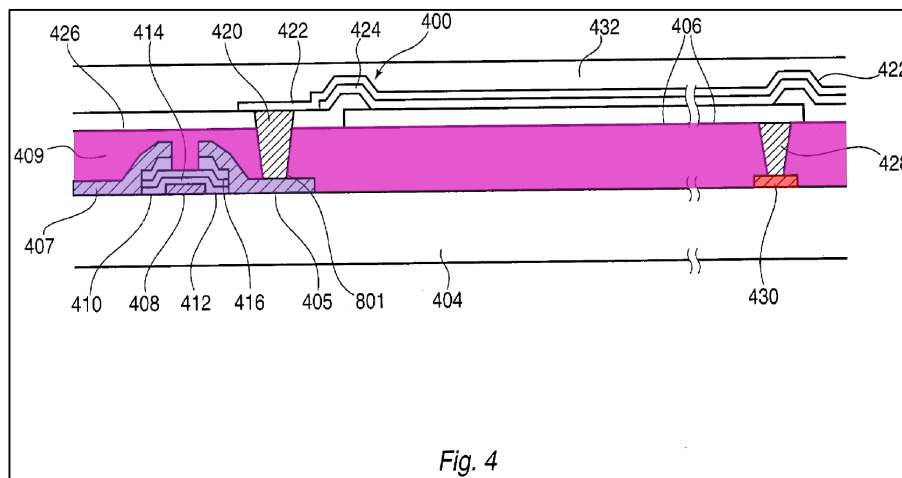
88. Further, Weaver discloses that Figs. 5-8 illustrate a processing flow for forming a pixel that includes OLED 400, transistor 410, and a switching transistor 502. EX1004, [0032]. A POSITA would have understood that transistor 502 corresponds to the transistor 208/308, because the pixel of Weaver only includes two transistors. Weaver further discloses that “the active regions 505 and 506 are deposited, which may be formed from the three layer SiNx layer, an intrinsic a-Si layer, and a N+a-Si layer as described above.” Here, Weaver is teaching that the same channel layer (a-Si layer 414) used for transistor 410 is used for transistor 208/308. Therefore, a POSITA would have understood that each active device (transistor 208/308 and transistor 210/310/410) of the “at least one active device” of Weaver comprises a gate, a channel layer, a source and a drain.

4. [1c]

89. Weaver discloses “a first auxiliary electrode (bus line 430) electrically insulated from the active device (transistor 410); and.”

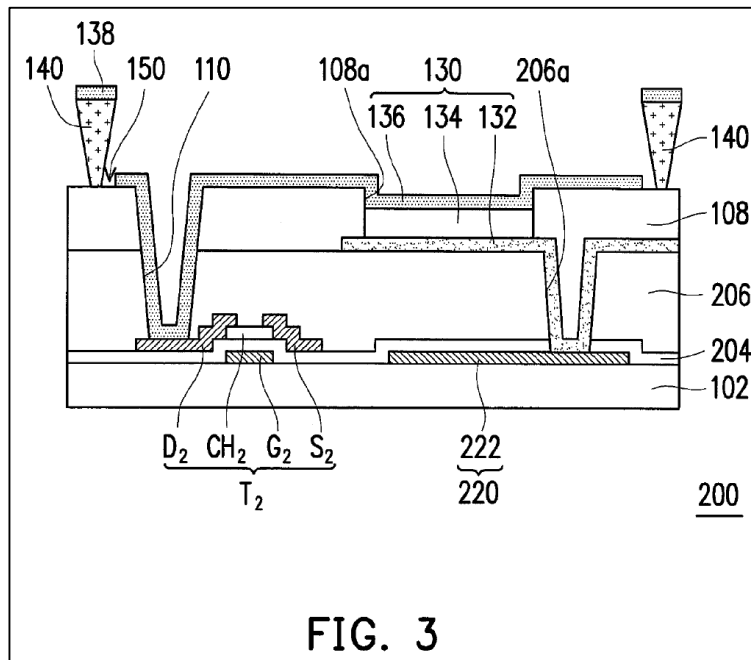
90. Claim 1 does not previously recite “an active device.” Rather, claim 1 previously recites “at least one active device.” Therefore, a POSITA would have understood that reciting “the active device” (singular) in claim 1 or in claims dependent thereon refers to one of the “at least one active device” of claim 1 if there is more than one. This interpretation is consistent with the 509 specification. EX1001, 2:66-67 (“at least one active device T1 and T2”), 3:7 (“the active device T1”), 3:8-9 (“[t]he active device T2”).

91. Weaver discloses **bus line 430** is electrically insulated from **transistor 410** by **passivation layer 409**. EX1004, [0026], Fig. 4.



Organic layer 424 is disposed between the anode 406 (connected to **bus line 430**) and the cathode 422 (connected to the transistor 410). The organic layer 424 also serves to electrically insulate the **bus line 430** from the transistor 410 for the same reason that light emitting layer 130 of the 509 patent (disposed between first electrode layer 132 which is connected to auxiliary electrode 220, and second

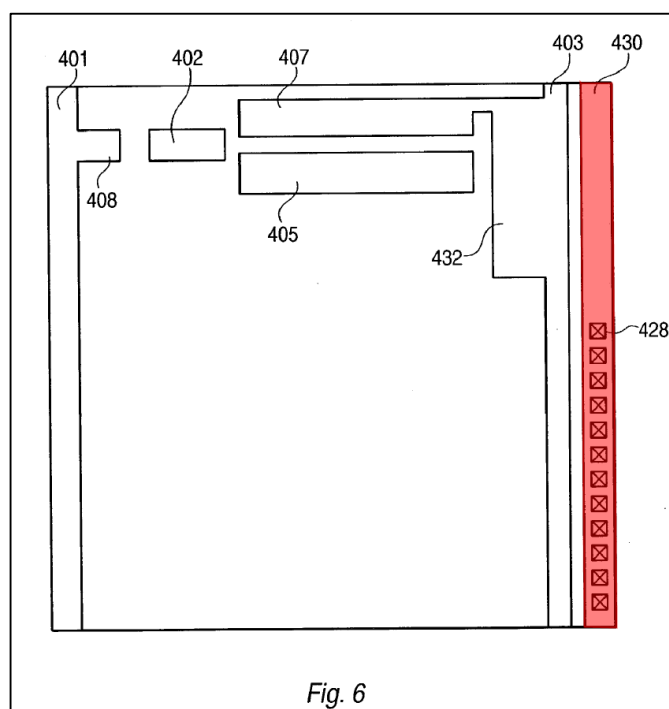
electrode layer 136 which is connected to active device T2) serves to electrically insulate the first auxiliary electrode 220 from the active device T2. See Fig. 3 of 509 patent. Otherwise, claim 1 would not read on any of the 509 disclosed embodiments.



The 509 patent teaches that this arrangement provides the claimed electrically insulated configuration. EX1001, 4:5-6.

92. Weaver discloses that **bus line 430** is an electrode that is supplemental to other electrodes in the structure. EX1004, [0026], Fig. 4.

93. Weaver also discloses that in forming the pixel, a source/drain level metal is deposited and patterned to form, among other things, **bus line 430**. EX1004, [0034], Fig. 6. Via holes 428 are formed in the passivation layer to **bus line 430**. *Id.*

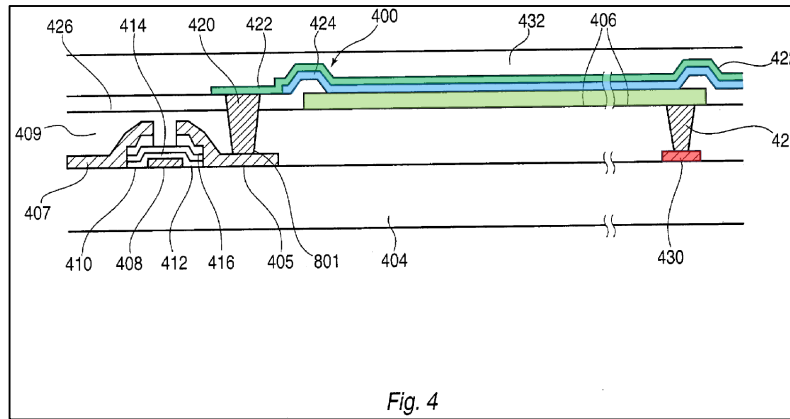


94. An ITO layer is deposited and patterned to form anode 406, where “Anode 406 is formed so as to cover vias 428 as shown in FIG. 6 to contact ITO bus line 430. *Id.*, [0036], Fig. 7. A POSITA would have understood that the plural electrical connections provided by vias 428 between anode 406 and bus line 430 means that the anode 406 and bus line 430 are connected in parallel, which means that bus line 430 is a supplemental electrode that reduces the total resistance of the pixel structure.

5. [1d]

95. Weaver discloses “a light emitting device (OLED 202, 302, 400) disposed above the first auxiliary electrode (bus line 430), wherein the light emitting device comprises.”

96. Weaver discloses that OLED stands for organic light emitting device. EX1004, [0014]. OLED 400 includes three layers (cathode 422, organic layer 424, anode 406), which are disposed above bus line 430. *Id.*, [0026], Fig. 4.

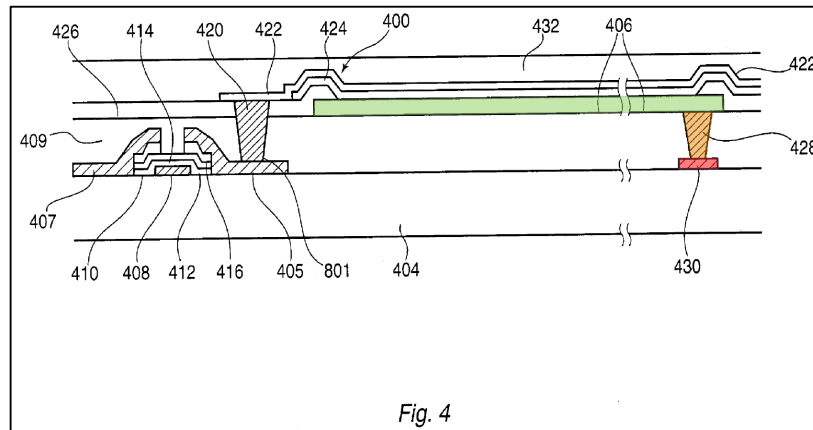


OLED 400 is considered “above” the bus line 430 because a portion (but not all) of OLED 400 vertically overlaps with bus line 430, in the same way that a portion (but not all) of light emitting device 130 vertically overlaps with first auxiliary electrode 120 for the embodiments of the 509 patent. EX1001, Figs. 2-5.

6. [1e]

97. Weaver discloses “a first electrode layer (anode 406) electrically connected with the first auxiliary electrode (bus line 430).”

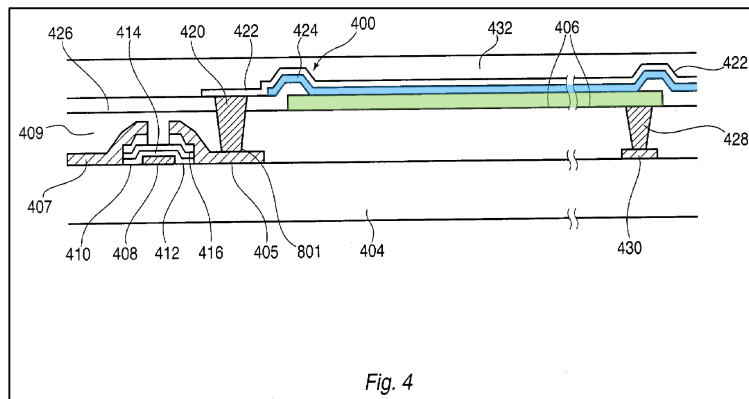
98. Weaver discloses that OLED 400 includes anode 406, which is electrically connected to bus line 430 by via 428. EX1004, [0026] (“Via 428 connects the anode 406 of OLED 400 to bus line 430.”), Fig. 4.



7. [1f]

99. Weaver discloses “a light emitting layer ([organic layer 424](#)) disposed on the first electrode layer ([anode 406](#)).”

100. Weaver discloses that OLED 400 includes [organic layer 424](#), which is disposed on [anode 406](#). EX1004, [0026], Fig. 4.



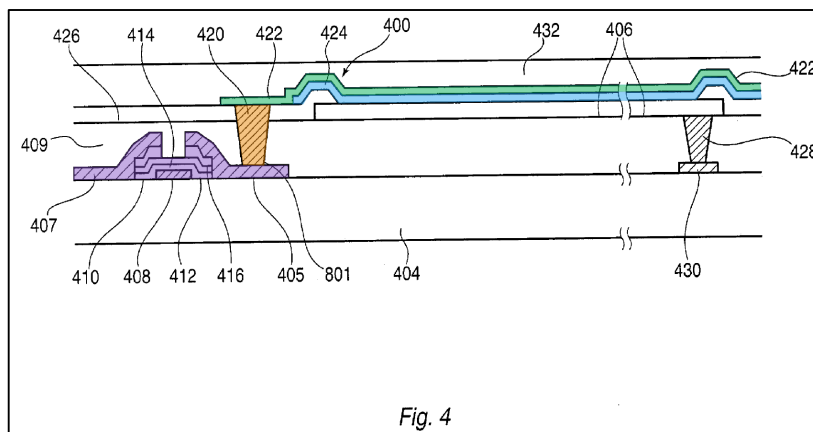
[Organic layer 424](#) emits light when sufficient current is passed between the [anode 406](#) and cathode 422. *Id.*, [0027].

8. [1g]

101. Weaver discloses “a second electrode layer (cathode 422) disposed on the light emitting layer (organic layer 424), wherein the second electrode layer is electrically connected with the active device (transistor 410).”

102. A POSITA would have understood that reciting “the active device” (singular) in claim 1 or in claims dependent thereon refers to one of the “at least one active device” of claim 1 if there is more than one. *See* ¶89, §X.A.4

103. Weaver discloses that OLED 400 includes cathode 422, which is disposed on the organic layer 424. EX1004, [0026], Fig. 4.



Cathode 422 is electrically connected to the source region 405 of transistor 410 by a metal plug filling via 420. *Id.*, [0025], Fig. 4.

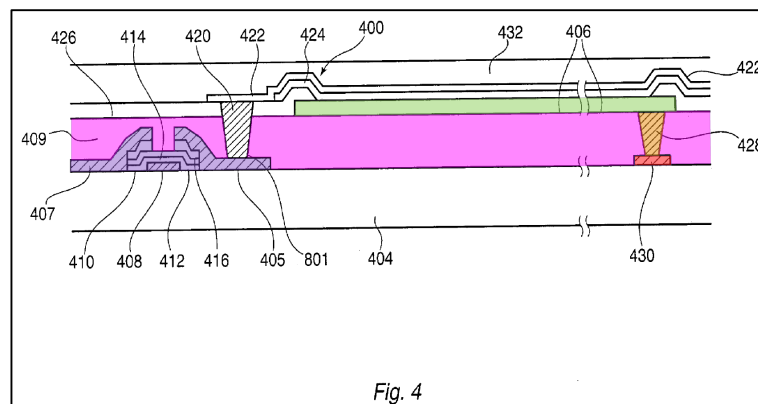
B. Claim 2

104. Weaver discloses “the pixel structure according to claim 1 (*see* claim 1), further comprising a first insulating layer (passivation layer 409) covering the active device (transistor 410) and the first auxiliary electrode (bus line 430), and

the first electrode layer (anode 406) of the light emitting device (OLED 400) being disposed on the first insulating layer (passivation layer 409), wherein the first insulating layer (passivation layer 409) has a first contact window opening (via hole 428) that exposes the first auxiliary electrode (bus line 430), and the first electrode layer (anode 406) is electrically connected with the first auxiliary electrode (bus line 430) via the first contact window opening (by a metal plug formed in via hole 428).”

105. A POSITA would have understood that reciting “the active device” (singular) in claim 1 or in claims dependent thereon refers to one of the “at least one active device” of claim 1 if there is more than one. *See* ¶89, §X.A.4

106. Fig. 4 of Weaver shows passivation layer 409 covering transistor 410 and bus line 430, where anode 406 is disposed on passivation layer 409.

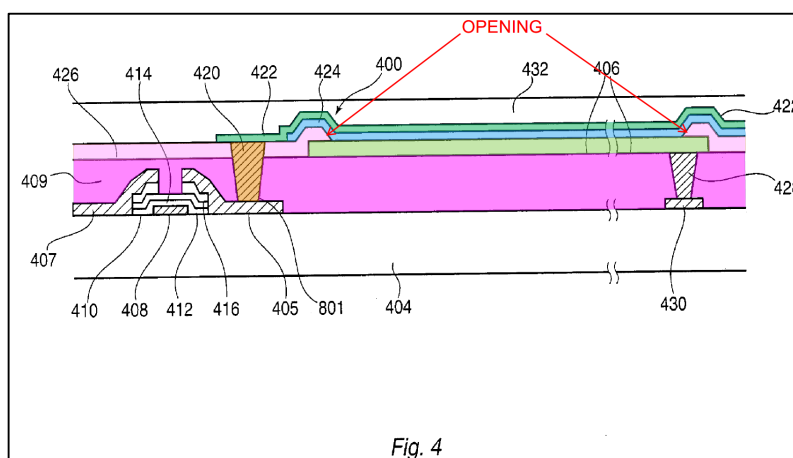


Weaver discloses that via holes 428 are formed in the passivation layer to the bus line 430, and metal plugs are formed therein (to electrically connect bus line 430 to anode 406). EX1004, [0035], Fig. 4.

C. Claim 3

107. Weaver discloses “the pixel structure according to claim 2 (*see* claim 2), further comprising a second insulating layer (**dielectric layer 426**) covering the first insulating layer (**passivation layer 409**) and the first electrode layer (**anode 406**) of the light emitting device (OLED 400), and the second electrode layer (**cathode 422**) of the light emitting device being disposed on the second insulating layer (**dielectric layer 426**), wherein the second insulating layer (**dielectric layer 426**) has an opening that exposes the first electrode layer (**anode 406**), and the light emitting layer (**organic layer 424**) of the light emitting device is disposed in the opening.”

108. Weaver discloses that **dielectric layer 426** may define boundaries of the OLED, and is formed on and covers **passivation layer 409**. EX1004, [0026], Fig. 4. **Cathode layer 422** is disposed on **dielectric layer 426** in the vicinity of **via 420**. *Id.*, Fig. 4. **Dielectric layer 426** has an opening indicated by the red arrows added to annotated Fig. 4 below that exposes the **anode 406**, where **organic layer 424** is disposed in the opening.



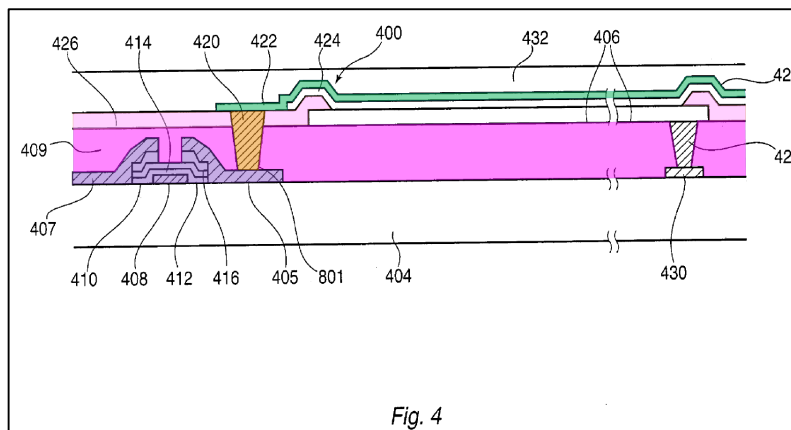
D. Claim 4

109. Weaver discloses “the pixel structure according to claim 3 (*see* claim 3), wherein the first insulating layer (**passivation layer 409**) and the second insulating layer (**dielectric layer 426**) further comprise a second contact window opening (**via hole 420**) that exposes a portion of the active device (source 405 of **transistor 410**), and the second electrode layer (**cathode 422**) of the light emitting device is electrically connected with the active device (**transistor 410**) via the second contact window opening (by the metal plug in **via 420**).”

110. A POSITA would have understood that reciting “the active device” (singular) in claim 1 or in claims dependent thereon refers to one of the “at least one active device” of claim 1 if there is more than one. *See* ¶89, §X.A.4

111. Weaver discloses that **transistor 410** is connected to the OLED 400 through **via 420**, which may be filled with a metal plug. EX1004, [0025]. Weaver

shows that via 420 extends through both passivation layer 409 and dielectric layer 426 forming a contact window opening. *Id.*, Fig. 4.



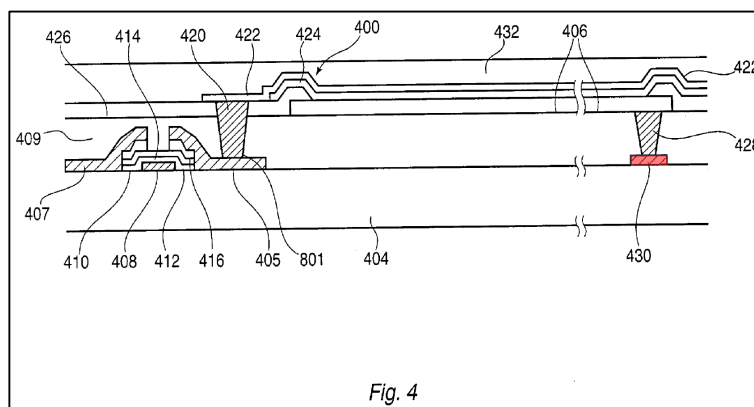
Weaver discloses via 420 with metal plug therein connects the source region 405 of transistor 410 to the cathode 422 of OLED 400. *Id.*, [0025], Fig. 4.

E. Claim 5

112. Weaver discloses “the pixel structure according to claim 1 (*see* claim 1), wherein the first auxiliary electrode (bus line 430) is a single electrode layer.”

113. Weaver discloses that bus line 430 is a single electrode layer.

EX1004, [0026], [0036], Figs. 4 and 7.

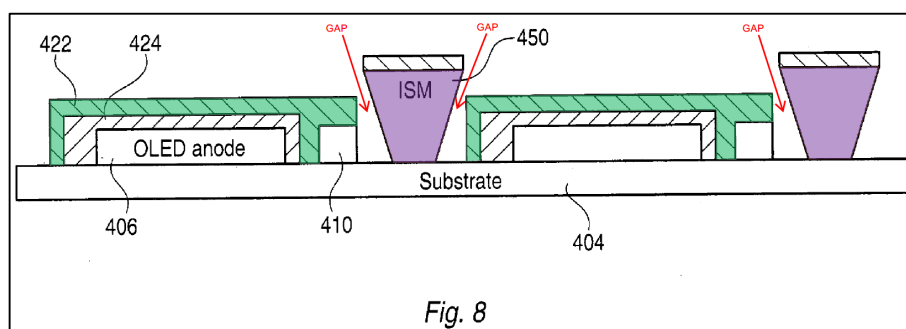


F. Claim 9

114. Weaver discloses “the pixel structure according to claim 1 (*see* claim 1), further comprising an isolating structure (integrated shadow mask - ISM) disposed around the second electrode layer (cathode 422) of the light emitting device, wherein a gap exists between the second electrode layer and the isolating structure.”

115. Claim 9 only recites the location of the isolating structure, but not its structure or function. The 509 patent discloses “A material of the first isolating structure 140 is a photoresist or other suitable materials, for example.” EX1001, 5:37-42. However, the 509 patent does not expressly disclose what if anything is being isolated by the first isolating structure. *Id.*, 5:37-62. Therefore, a POSITA would have understood that the plain meaning of “isolating structure” is a structure of insulation material.

116. Weaver discloses that shadow masks can be formed around the OLED opening. EX1004, [0037]. An integrated shadow mask (ISM) is fabricated prior to OLED fabrication, after which the layers of OLED including cathodes 422 are formed. *Id.*, [0038]. The ISM's are isolating structures disposed around cathodes 422, with gaps indicated by the red arrows added to annotated Fig. 8 between the cathodes 422 and ISM's. *Id.*, Fig. 8.



G. Claim 12

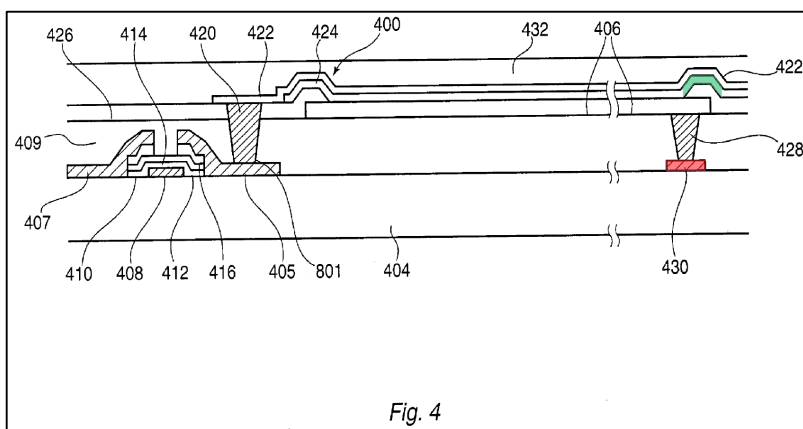
117. Weaver discloses “the pixel structure according to claim 1 (*see* claim 1), wherein the light emitting device (OLED 202, 302, 400) is a top-emission organic electroluminescent device.”

118. Weaver discloses that cathode 422 may be sufficiently transparent to create a top emitting device. EX1004, [0029]. Organic layer 424 may be any suitable organic material that emits light when sufficient current is passed between anode 406 and cathode 422, and can include phosphorescent materials for higher luminescent efficiencies. *Id.*, [0027]-[0028].

H. Claim 13

119. Weaver discloses “the pixel structure according to claim 1 (*see* claim 1), wherein a vertical projection of the light emitting layer (**organic layer 424**) of the light emitting device (OLED 400) at least partially overlaps the first auxiliary electrode (**bus line 430**).”

120. Weaver discloses that the organic layer 424 has a **vertical projection** that at least partially overlaps with **bus line 430**. EX1004, Fig. 4.



XI. GROUND 2: CLAIMS 6-8 RENDERED OBVIOUS BY WEAVER AND LEE053

121. The construction of “auxiliary electrode” I applied for Ground 2 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

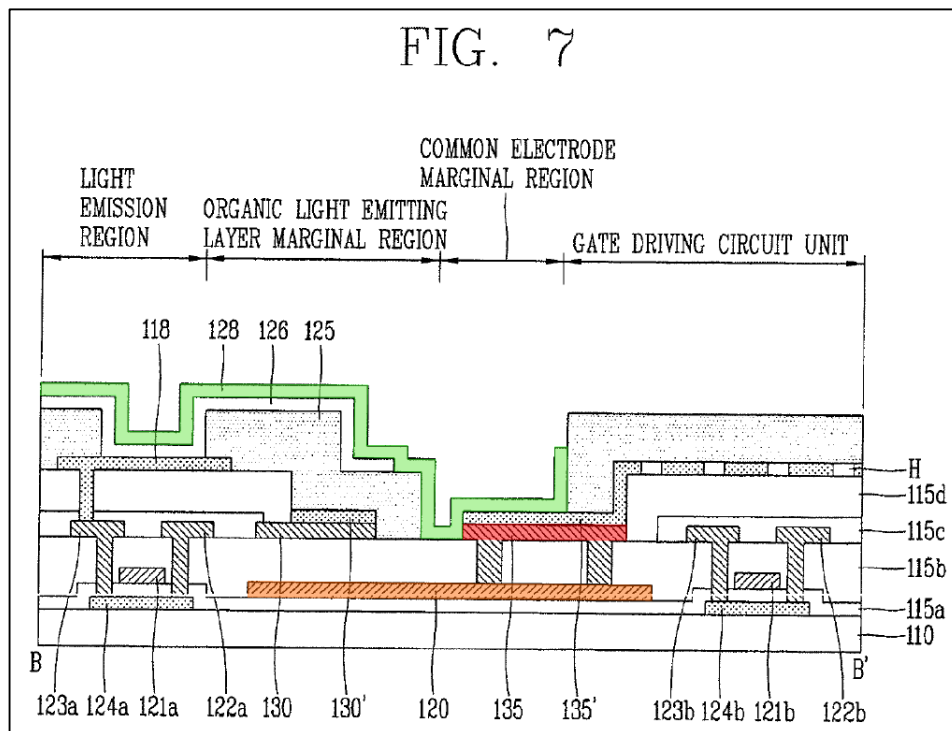
A. Claim 6

122. The Weaver-Lee053 combination renders obvious “the pixel structure (Weaver’s pixel structure) according to claim 1 (*see* claim 1), wherein the first auxiliary electrode (Weaver’s bus line 430) comprises: a bottom electrode layer (Weaver’s bus line 430 modified to comprise Lee053’s **dummy wiring 120**); and a top electrode layer (Weaver’s bus line 430 corresponding to Lee053’s **second power wiring 135**) electrically connected with the bottom electrode layer (Weaver’s bus line 430 modified to include connection between Lee053’s dual layers), wherein the first electrode layer (Weaver’s **anode 406**) of the light emitting

device (Weaver's OLED 400) is electrically connected with the top electrode layer of the first auxiliary electrode (by Weaver's metal plug in via 428)."

123. Weaver discloses a first auxiliary electrode (bus line 430) wherein the first electrode layer 406 of the light emitting device (OLED 400) is electrically connected to the first auxiliary electrode (bus line 430). See §§X.A.4, X.A.6.

124. Lee053 discloses **dummy wiring 120**, which is made of metal. EX1005, [0073], Fig. 7.



A light emitting device includes electrode 118 as an anode, an organic light emitting layer 126 on electrode 118, and **electrode 128** as a cathode on the organic light emitting layer 126. EX1005, [0081], [0089], [0091], Fig. 7. Lee053 discloses a first auxiliary electrode having a top electrode layer (**second power**

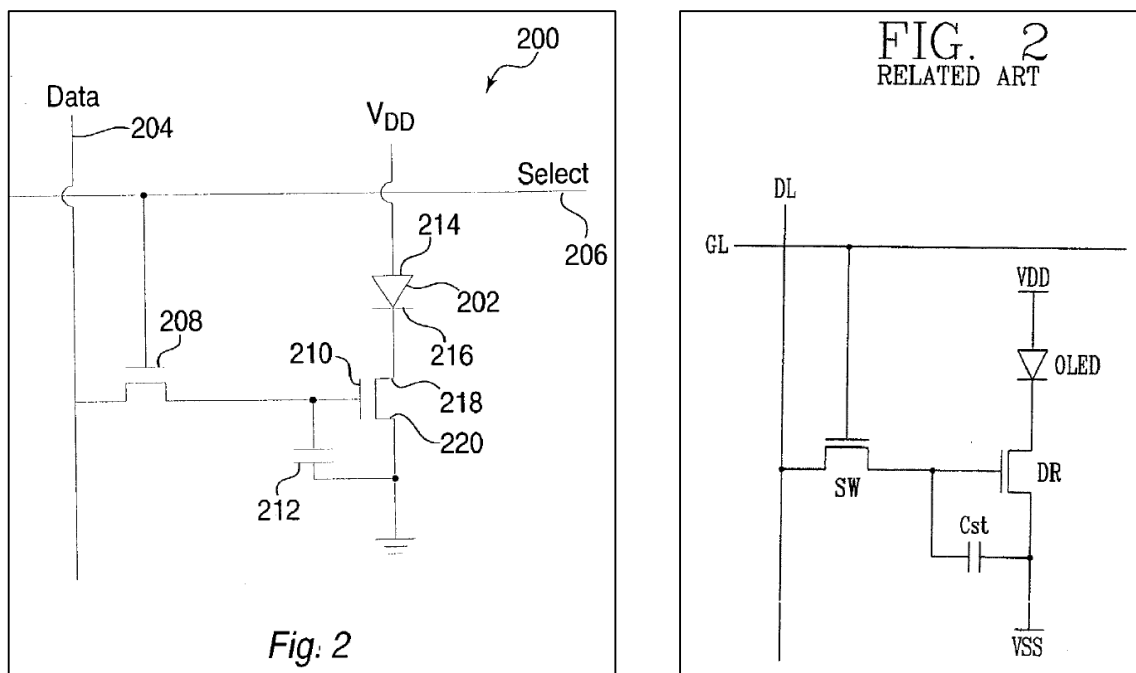
wiring 135) and a bottom electrode layer (dummy wiring 120), which is made of metal. *Id.*, [0073], Fig. 7. The second power wiring 135 is electrically connected to underlying dummy wiring 120 through a third contact hole. *Id.*, [0077], Fig. 7. Lee053 discloses that dummy wiring 120 and second power wiring 135 collectively are an electrode that is supplemental to other electrodes in the structure. *Id.*.

125. The top electrode layer (second power wiring 135) is electrically connected to the cathode (electrode 128) by second power wiring pattern 135'. EX1005, [0092], Fig. 7. Therefore, Lee053 discloses that it was known to electrically connect an auxiliary electrode to one of the electrode layers of a light emitting device, where that auxiliary electrode includes a top electrode layer (second power wiring 135) and a bottom electrode layer (dummy wiring 120) electrically connected together. Lee053 discloses that providing the dummy wiring 120 at a lower side of, and connected to, the second power wiring 135, reduces wiring resistance, and also allows for the widths of the wirings to be reduced while having the same wiring resistance. EX1005, [0093], [0085].

126. It would have been obvious to a POSITA to combine the teachings of Weaver and Lee053 to reconfigure the bus line 430 of Weaver with a bottom electrode layer (akin to Lee053's dummy wiring 120) that is electrically connected with a top electrode layer (akin to Lee053's second power wiring 135), wherein the

first electrode layer (anode 406) of the light emitting device 400 of Weaver is electrically connected with the top electrode layer.

127. Weaver and Lee053 are analogous prior art to the 509 patent, as each relates to organic light emitting devices with an organic light emitting layer disposed between an anode electrode layer and a cathode electrode layer, as well as the surrounding layers and circuits to operate the light emitting devices. Both references disclose the same OLED circuit design (compare Fig. 2 of Weaver and Fig. 2 of Lee053).



128. A POSITA would have understood the problem involved, namely that higher resistance between the power or ground line to the light emitting device would consume more power and require higher operating voltages, and can require larger wiring widths in order to achieve a desired performance. EX1005, [0085],

[0093]. To overcome this problem, Lee053 discloses the solution of providing the auxiliary electrode, (electrically connected to one of the LED electrodes) configured as two electrode layers (top electrode layer and bottom electrode layer) that are electrically connected together. Doing so reduces resistance, and can allow for reduced wiring widths as disclosed in Lee053. A POSITA would have been motivated to implement the solution of Lee053 in the Weaver device to lower the resistance between anode 406 and the voltage source VDD, and/or allow for reduced wiring widths that enables scaling down the size of the circuit.

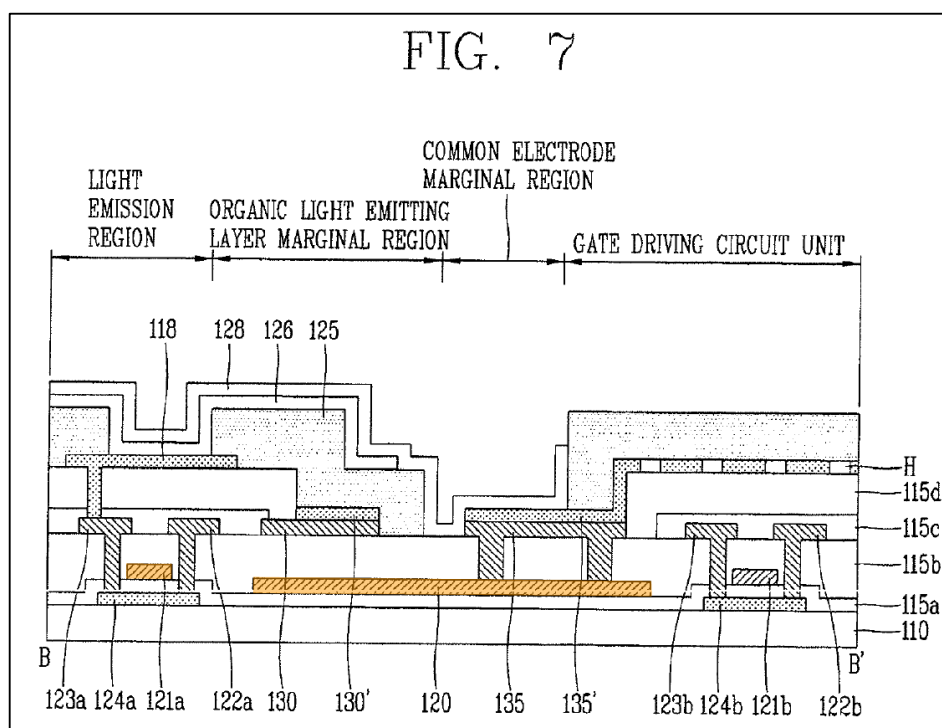
129. The modification to Weaver could be implemented, for example, by adding an **additional electrode layer** electrically connected to the **bus line 430**, whereby the **additional electrode layer** is the bottom electrode layer, and the **bus line 430** is the top electrode layer.

130. Modified Fig. 4 of Weaver below shows an example of such a straightforward implementation, with the **additional electrode layer** added as part of the same layer of conductive material used to form **gate 408**, the **additional insulation layer** is added as part of the **insulation layer 412** (i.e., as part of the SiNx layer described in [0024] and shown as layer 412 of the transistor 410 in Fig. 4), and **bus line 430** formed as part of the same layer of conductive material used to form **source/drain regions 405/407** on top of **insulation layer 412**, where the

modified with the **additional electrode layer**) and the gate (Weaver's **gate 408**) of the active device belong to the same layer."

133. As set forth above for claim 6, it would have been obvious to a POSITA to combine the teachings of Weaver and Lee053 to reconfigure the bus line 430 of Weaver with a bottom electrode layer (akin to Lee053's **dummy wiring 120**) that is electrically connected with a top electrode layer (akin to Lee053's **second power wiring 135**), wherein the first electrode layer (anode 406) of the light emitting device 400 of Weaver is electrically connected with the top electrode layer. *See* §XI.A.

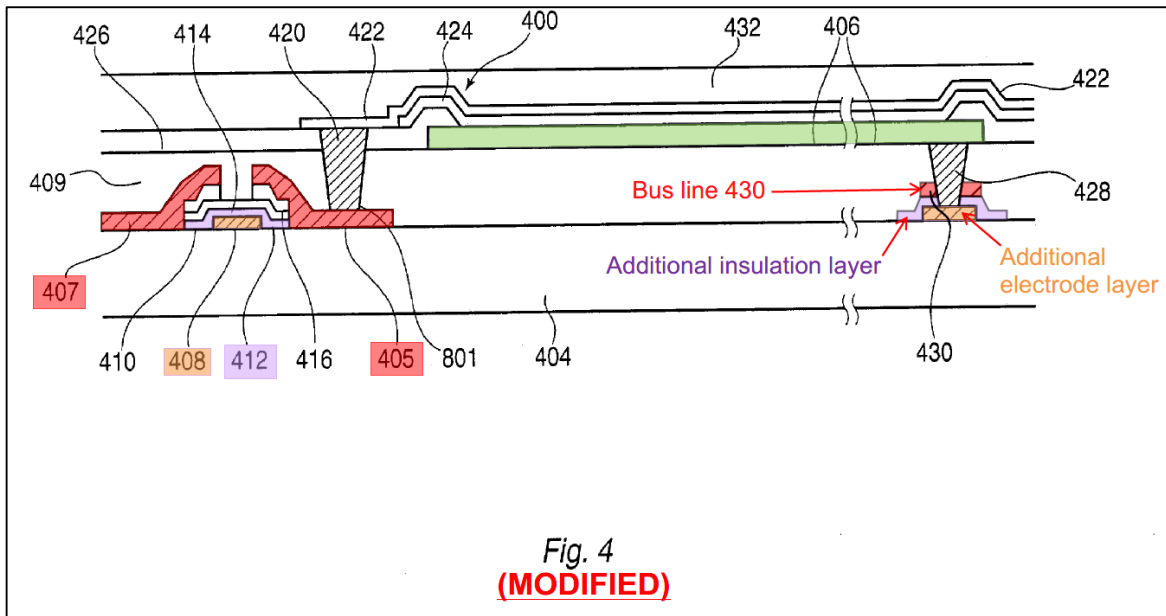
134. Lee053 discloses that OLED display devices are driven by thin film transistor (TFT) switching elements (i.e., active devices), including a TFT formed in the light emission region and electrically connected to the anode electrode 118. EX1005, [0008], [0069], Fig. 7. The TFT in the light emission region includes a first active layer 124a, a **first gate electrode 121a**, and first source and drain electrodes 122a and 123a. *Id.*, [0074], [0076], Fig. 7.



Lee053 discloses that the **first gate electrode 121a** is included in “gate wiring.” *Id.*, [0071]. Lee053 also discloses that the **dummy wiring 120** is “made of the metal for a gate wiring.” *Id.*, [0073]. The **first gate electrode 121a** and the **dummy wiring 120** are both formed on layer 115a. *Id.*, Fig. 7. Therefore, Lee053 discloses or at least renders obvious that the **dummy wiring 120** and the **first gate electrode 121a** of the TFT active device belong to the same layer.

135. In combining the teachings of Weaver and Lee053 as set forth above in §XI.A, it would have been obvious to a POSITA to add the **additional electrode layer** as part of the same layer of conductive material used to form **gate 408**, to add the **additional insulation layer** as part of the **insulation layer 412**, and to form **bus**

line 430 as part of the same layer of conductive material used to form source/drain regions 405/407, as shown in the modified Fig. 4 of Weaver below.



136. Weaver and Lee053 are analogous prior art to the 509 patent. *See* §XI.A.

137. A POSITA would have understood the problem involved, namely how to efficiently form the various layers of the device. To overcome this problem, Lee053 discloses or renders obvious the solution of using the same layer of conductive material to form both the dummy wiring 120 and the first gate electrode 121a of the same metal layer. Doing so simplifies semiconductor manufacturing steps to more efficiently form the device, reducing the number of the processing steps necessary to fabricate the device. A POSITA would have been motivated to

implement the solution of Lee053 in the Weaver device to manufacture the device more efficiently.

138. A POSITA would have had a reasonable expectation of success in combining Weaver and Lee053, as both references disclose the various layers for connecting to and operating an organic light emitting device with an anode and a cathode, and techniques for their manufacture. The modification to Weaver to implement the solution taught or rendered obvious in Lee053 involves modifications of only routine skill in the art. Specifically, both the **additional electrode layer** and the **gate 408** are formed on substrate 404, so their formation using the same conductive layer would have involved routine skill in the art. Because combining the teachings of Weaver and Lee053 would involve known methods, it would have yielded predictable results.

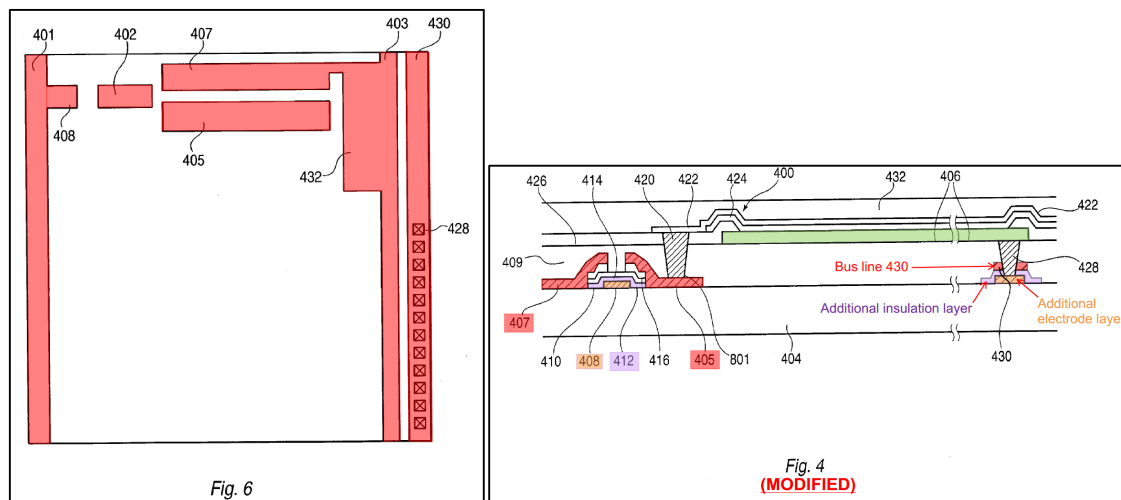
C. Claim 8

139. The Weaver-Lee053 combination renders obvious “the pixel structure according to claim 6 (*see* claim 6), wherein the top electrode layer (Weaver’s **bus line 430** as modified by Lee053) and the source and the drain of the active device (Weaver’s **source region 405 and the drain region 407** of transistor 410) belong to the same layer.”

140. As set forth above for claim 6, it would have been obvious to a POSITA to combine the teachings of Weaver and Lee053 to reconfigure the **bus**

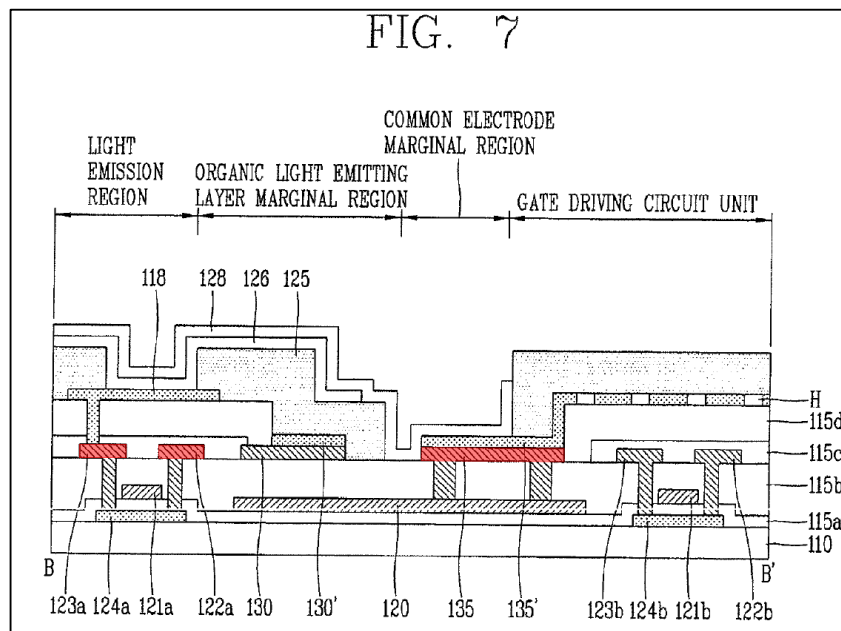
line 430 of Weaver with a bottom electrode layer (akin to Lee053's dummy wiring 120) that is electrically connected with a top electrode layer (akin to Lee053's second power wiring 135). See §XI.A.

141. Weaver discloses that bus line 430, and source region 405 and drain region 407 of transistor 410 are formed in the same layer. Specifically, Weaver discloses that in forming the device of Fig. 4, a source/drain level metal (e.g. Mo) is deposited and patterned to form data line 401, source/drain 408, contact 402, drain 405 and source 407, ground line 403, a top electrode 432 of the storage capacitor and ITO bus line 430. EX1004, [0034], Fig. 6.



A POSITA would have understood that reference to drain 405 and source 407 in ¶[0034] is referring to source region 405 and drain region 407 of Fig. 4 (i.e., it is evident that the numbers were inadvertently transposed).

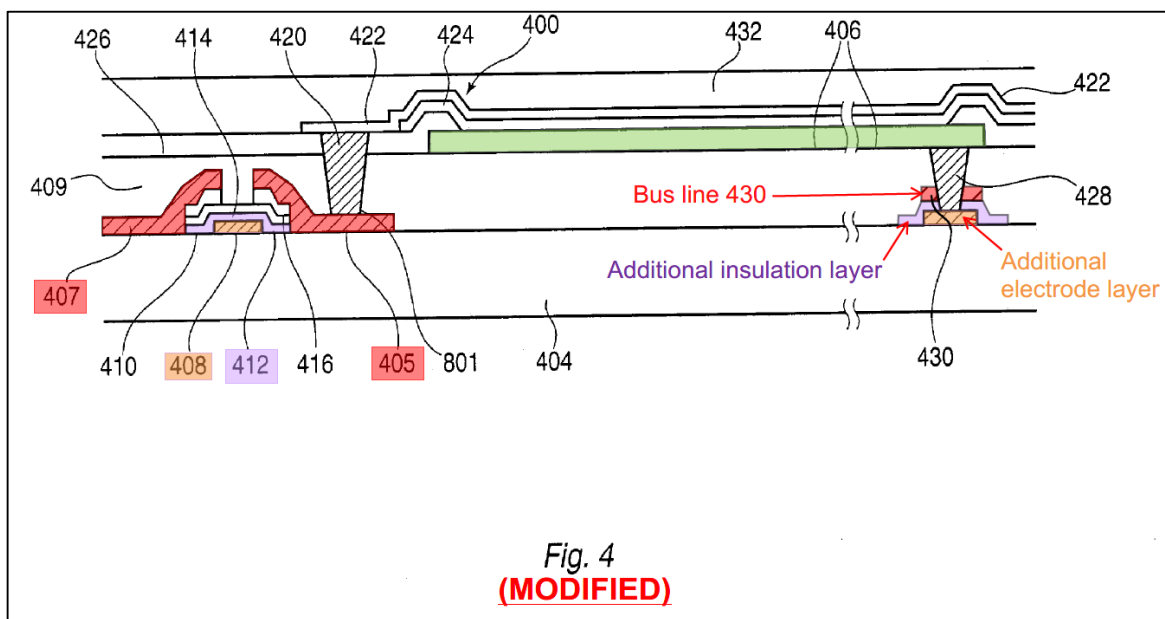
142. Lee053 discloses the TFT (active device) in the light emission region includes first source and drain electrodes 122a and 123a. EX1005, [0074], Fig. 7.



Lee053 further discloses that the **first source and drain electrodes 122a and 123a** are included as part of the “data wiring” that are formed on first passivation layer 115b. *Id.*, ¶0074, Fig. 7. Lee053 also discloses that **second power wiring 135** is “made of metal for a data wiring,” and is also formed on passivation layer 115b. *Id.*, ¶0077, Fig. 7. Therefore, Lee053 discloses or at least renders obvious forming **first source and drain electrodes 122a and 123a** and **second power wiring 135** whereby they belong to the same conductive layer.

143. In combining the teachings of Weaver and Lee053 as set forth above in §XI.A, it would have been obvious to a POSITA to form the top electrode layer of the first auxiliary electrode (i.e. **bus line 430**), and the **source region 405** and the **drain region 407** of transistor 410 in Weaver, so they belong to the same layer.

EX1004, [0034], Fig.4, Fig. 6.



144. Weaver and Lee053 are analogous prior art to the 509 patent. *See* §XI.A.

145. A POSITA would have understood the problem involved, namely how to efficiently form the various layers of the device. To overcome this problem, Lee053 discloses or renders obvious the solution of forming **first source and drain electrodes 122a and 123a** and **second power wiring 135** whereby they belong to the same metal layer, and Weaver discloses **bus line 430**, and **source region 405** and **drain region 407** of transistor 410 are formed in the same layer. Doing so simplifies semiconductor manufacturing steps to form the device, reducing the number of the processing steps necessary to fabricate the device. In combining the teachings of Weaver and Lee053 as set forth above in §XI.A, a POSITA would

have been motivated to implement the solutions of Lee053 and Weaver to manufacture the device more efficiently.

146. A POSITA would have had a reasonable expectation of success in combining Weaver and Lee053, as both references disclose the various layers for connecting to and operating a light emitting device with an anode and a cathode, and techniques for their manufacture. The modification to Weaver to implement the solution taught in Lee053 and Weaver involves modifications of only routine skill in the art. Moreover, because combining the teachings of Weaver and Lee053 would involve known methods, it would have yielded predictable results.

XII. GROUND 3: CLAIMS 6-8 RENDERED OBVIOUS BY WEAVER AND SONG

147. The construction of “auxiliary electrode” I applied for Ground 3 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

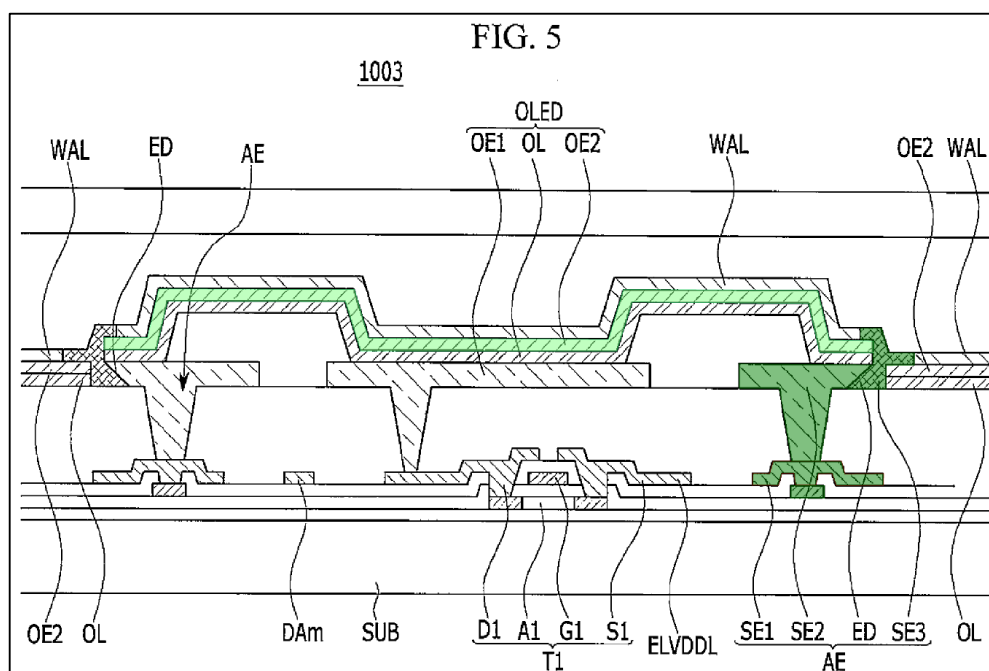
A. Claim 6

148. The Weaver-Song combination renders obvious “the pixel structure (Weaver’s pixel structure) according to claim 1 (*see* claim 1), wherein the first auxiliary electrode (Weaver’s bus line 430) comprises: a bottom electrode layer (Weaver’s bus line 430 modified to comprise Song’s **bottom electrode layer** of first auxiliary electrode portion SE1); and a top electrode layer (Weaver’s bus line 430 corresponding to Song’s **top electrode layer** of first auxiliary electrode portion

SE1) electrically connected with the bottom electrode layer (Weaver's bus line 430 modified to include connection between Song's dual layers), wherein the first electrode layer (Weaver's **anode 406**) of the light emitting device (Weaver's OLED 400) is electrically connected with the top electrode layer of the first auxiliary electrode (by Weaver's metal plug in via 428)."

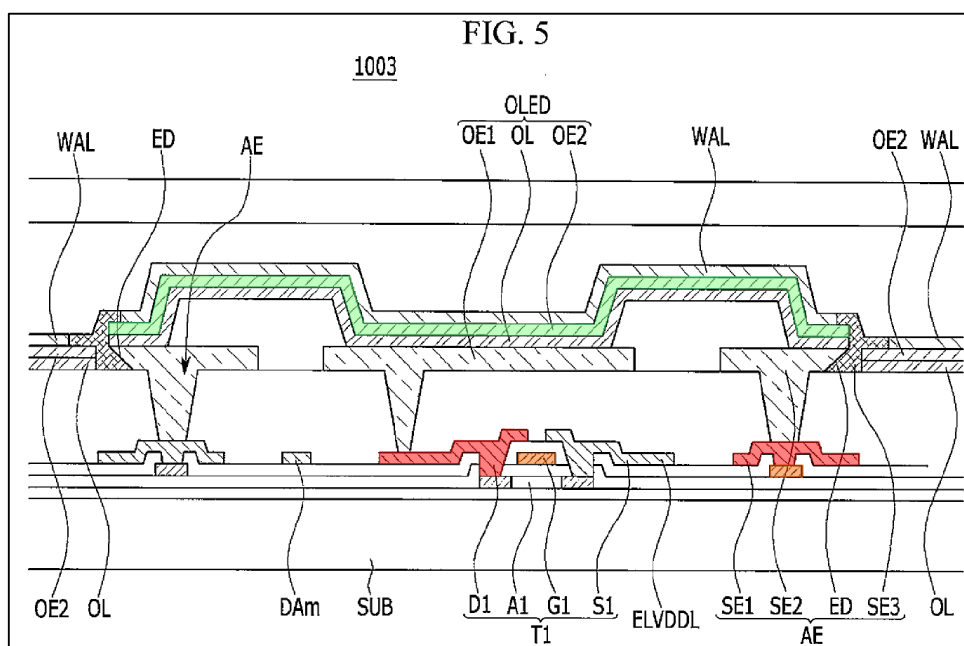
149. Weaver discloses a first auxiliary electrode (bus line 430) wherein the first electrode layer 406 of the light emitting device (OLED 400) is electrically connected to the first auxiliary electrode (bus line 430). *See* §§X.A.4, X.A.6.

150. Song discloses an organic light emitting diode OLED that includes first electrode OE1 as an anode, an organic emission layer OL disposed on first electrode OE1, and **second electrode OE2** as a cathode disposed on the organic emission layer OL. EX1006, [0069]; Fig. 5. Thin film transistor T1 (i.e., an active device) is electrically connected to the OLED and includes a first source electrode S1, a first drain electrode D1, a first active layer A1, and a first gate electrode G1. *Id.*, [0059]. Fig. 5. An **auxiliary electrode AE** of the OLED display includes a first auxiliary electrode portion SE1, a second auxiliary electrode portion SE2, and a third auxiliary electrode portion SE3 (which is electrically connected to the **second electrode OE2**). *Id.*, [0090], Fig. 5.



The first auxiliary electrode portion SE1, the second auxiliary electrode portion SE2 and the third auxiliary electrode portion SE3 (of auxiliary electrode AE) wholly thickens second electrode OE2 to reduce sheet resistance and voltage drop. *Id.*, [0098].

151. Song discloses first auxiliary electrode portion SE1 is located (or disposed) in the same layer as that of a first gate electrode G1 and a first drain electrode D1 on substrate SUB. EX1006, [0090]-[0091], Fig. 5. However, Fig 5 shows that the first drain electrode D1 overlaps first gate electrode G1, and the first auxiliary electrode portion SE1 is formed of two sublayers (a top electrode layer and a bottom electrode layer). *Id.*



Further, the **first gate electrode G1** and the **bottom electrode layer** of the first auxiliary electrode portion SE1 are both formed on one of the insulation layers, and the **first drain electrode D1** and the **top electrode layer** of the first auxiliary electrode portion SE1 are both formed on a different one of the insulation layers.

Id. Therefore, a POSITA would have understood Song as disclosing that the **first gate electrode G1** and the **bottom electrode layer** of the first auxiliary electrode portion SE1 are formed of one sublayer, and the **first drain electrode D1** and the **top electrode layer** of the first auxiliary electrode portion SE1 are formed of a different sublayer. Song discloses that first auxiliary electrode portion SE1 is an electrode that is supplemental to other electrodes in the structure.

152. The first auxiliary electrode portion SE1 is electrically connected to the cathode (second electrode OE2) by second auxiliary electrode portion SE2 and

third auxiliary electrode portion SE3. *Id.*, [0098], Fig. 5. Therefore, Song discloses that it was known to electrically connect an auxiliary electrode to one of the electrode layers of a light emitting device, where the that auxiliary electrode (first auxiliary electrode portion SE1) includes a **top electrode layer** (in the same layer as the **first drain electrode D1**) and a **bottom electrode layer** (in the same layer as the **first gate electrode G1**).

153. It would have been obvious to a POSITA to combine the teachings of Weaver and Song to reconfigure the bus line 430 of Weaver with a top electrode layer (akin to Song's **top electrode layer** of first auxiliary electrode portion SE1) that is electrically connected with a bottom electrode layer (akin to Song's **bottom electrode layer** of first auxiliary electrode portion SE1), wherein the first electrode layer (anode 406) of the light emitting device 400 of Weaver is electrically connected with the top electrode layer.

154. Weaver and Song are analogous prior art to the 509 patent, as each relates to organic light emitting devices with an organic light emitting layer disposed between an anode electrode layer and a cathode electrode layer, as well as the surrounding layers and circuits to operate the light emitting devices.

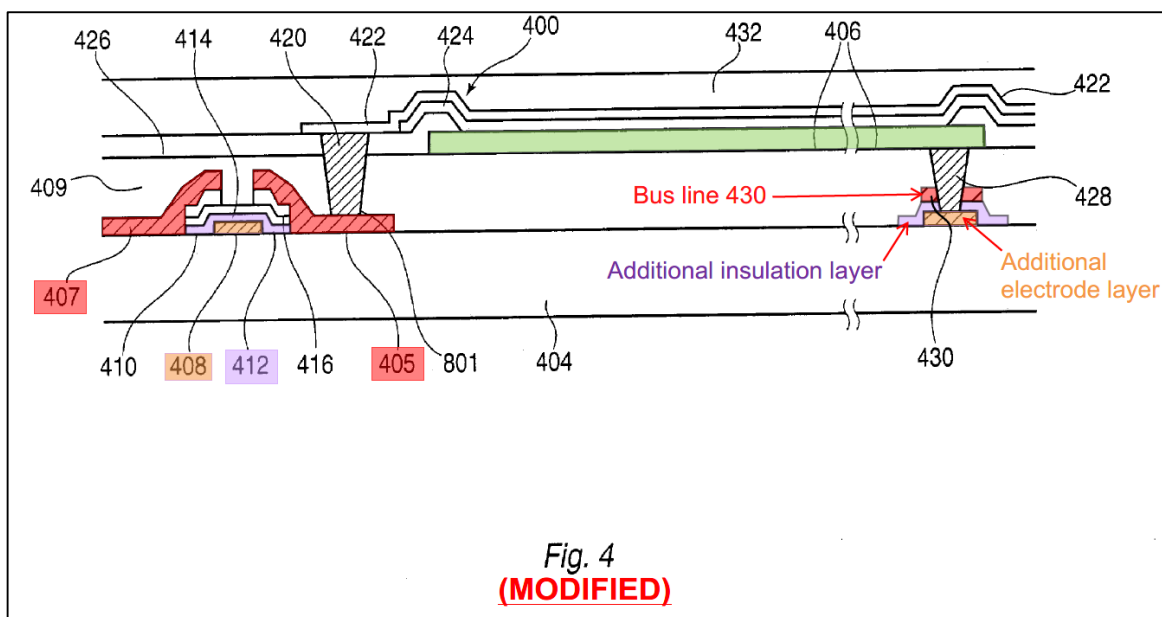
155. A POSITA would have understood the problem involved, namely that higher sheet resistance between the power or ground line to the light emitting device would consume more power and require higher operating voltages because

of the higher voltage drop of the OLED display. EX1006, [0098]. To overcome this problem, Song discloses the solution of providing the auxiliary electrode, (electrically connected to one of the LED electrodes) configured as two electrode layers (top electrode layer and bottom electrode layer) that are electrically connected together. Doing so reduces resistance and voltage drop as disclosed in Song. A POSITA would have been motivated to implement the solution of Song in the Weaver device to lower the resistance and voltage drop between anode 406 and the voltage source VDD of Weaver.

156. The modification to Weaver could be implemented, for example, by adding an **additional electrode layer** electrically connected to the **bus line 430**, whereby the **additional electrode layer** is the bottom electrode layer, and the **bus line 430** is the top electrode layer.

157. Modified Fig. 4 of Weaver below shows an example of such a straightforward implementation, with the **additional electrode layer** added as part of the same layer of conductive material used to form **gate 408**, the **additional insulation layer** is added as part of the **insulation layer 412** (i.e., as part of the SiN_x layer described in [0024] and shown as layer 412 of the transistor 410 in Fig. 4), and **bus line 430** formed as part of the same layer of conductive material used to form **source/drain regions 405/407** on top of **insulation layer 412**, where the

additional electrode layer and the bus line 430 are electrically connected, and the bus line 430 and anode 406 are electrically connected.



This implementation would provide for an efficient manufacturing process flow.

158. A POSITA would have had a reasonable expectation of success in combining Weaver and Song, as both references disclose the various layers for connecting to and operating a light emitting device with an anode and a cathode, and the modification to Weaver to implement the solution taught in Song involves modifications of only routine skill in the art. Moreover, because combining the teachings of Weaver and Song would involve known methods, it would have yielded predictable results.

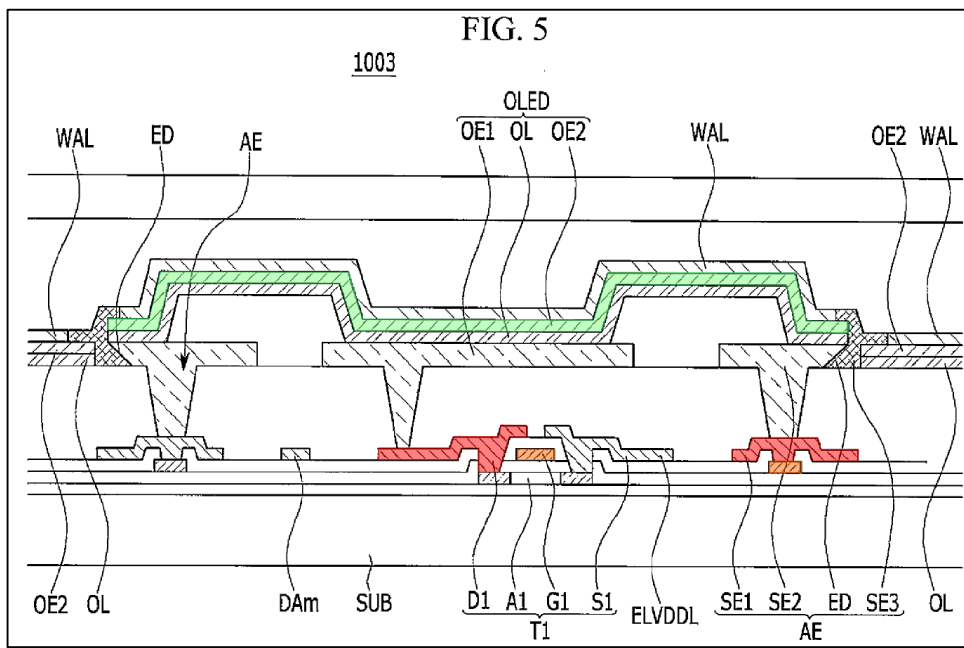
B. Claim 7

159. The Weaver-Song combination renders obvious “the pixel structure according to claim 6 (*see* claim 6), wherein the bottom electrode layer (modified

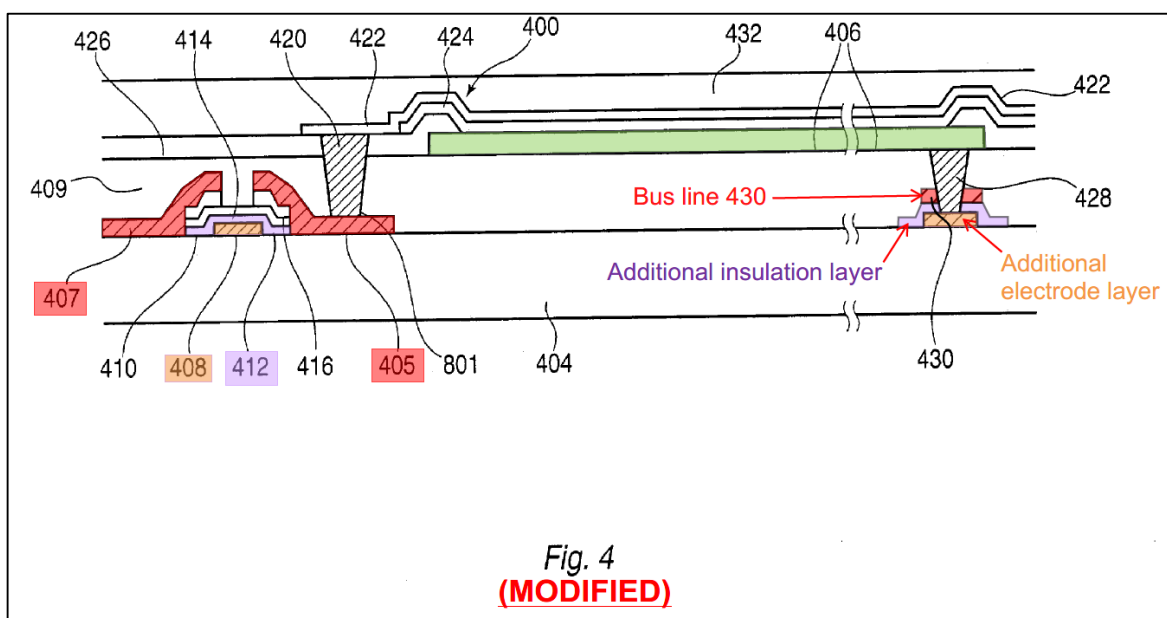
Weaver's bus line 430) and the gate (Weaver's gate 408) of the active device belong to the same layer."

160. As set forth above for claim 6, it would have been obvious to a POSITA to combine the teachings of Weaver and Song to reconfigure the bus line 430 of Weaver with a bottom electrode layer (akin to Song's **bottom electrode layer** of first auxiliary electrode portion SE1) that is electrically connected with a top electrode layer (akin to Song's **top electrode layer** of first auxiliary electrode portion SE1), wherein the first electrode layer (anode 406) of the light emitting device 400 of Weaver is electrically connected with the top electrode layer. *See* §XII.A.

161. Song discloses that the **first gate electrode G1** and the **bottom electrode layer** of the first auxiliary electrode portion SE1 are formed of the same sublayer. *See* §XII.A.



162. In combining the teachings of Weaver and Song as set forth above in §XII.A, it would have been obvious to a POSITA to add the **additional electrode layer** as part of the same layer of conductive material used to form **gate 408**, to add the **additional insulation layer** as part of the **insulation layer 412**, and to form **bus line 430** as part of the same layer of conductive material used to form **source/drain regions 405/407**, as shown in the modified Fig. 4 of Weaver below.



163. Weaver and Song are analogous prior art to the 509 patent. *See* §XII.A.

164. A POSITA would have understood the problem involved, namely how to efficiently form the various layers of the device. To overcome this problem, Song discloses the solution of using the same layer of conductive material to form both the first gate electrode G1 and the bottom electrode layer of the first auxiliary electrode portion SE1. Doing so simplifies semiconductor manufacturing steps to form the device, reducing the number the processing steps necessary to fabricate the device. A POSITA would have been motivated to implement the solution of Song in the Weaver device to manufacture the device more efficiently.

165. A POSITA would have had a reasonable expectation of success in combining Weaver and Song, as both references disclose the various layers for

connecting to and operating an organic light emitting device with an anode and a cathode, and techniques for their manufacture. The modification to Weaver to implement the solution taught in Song involves modifications of only routine skill in the art. Specifically, both the **additional electrode layer** and the **gate 408** are formed on substrate 404, so their formation using the same conductive layer would have involved routine skill in the art. EX1004, Fig. 4. Because combining the teachings of Weaver and Song would involve known methods, it would have yielded predictable results.

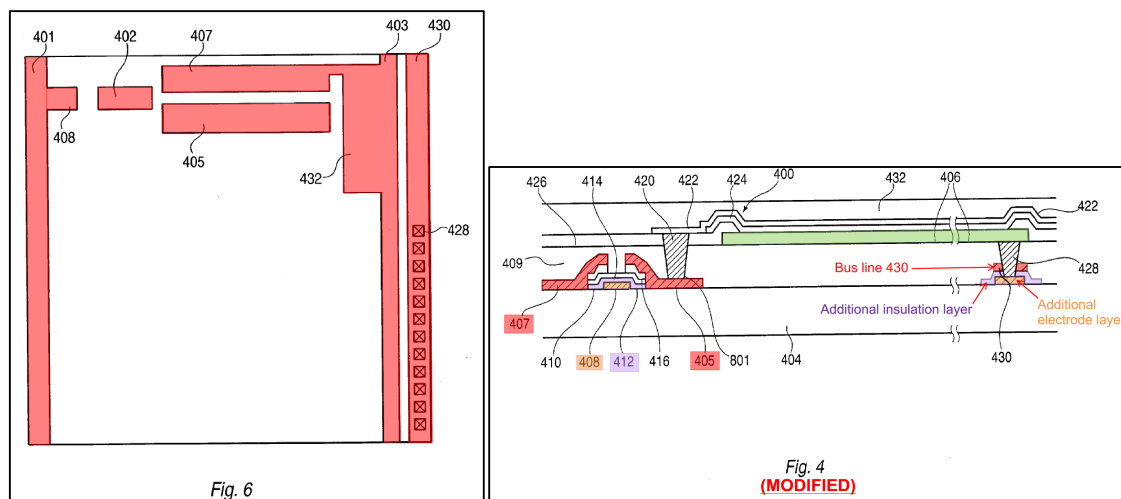
C. Claim 8

166. The Weaver-Song combination renders obvious “the pixel structure according to claim 6 (*see* claim 6), wherein the top electrode layer (Weaver’s **bus line 430** as modified by Song) and the source and drain of the active device (Weaver’s **source region 405 and the drain region 407** of transistor 410) belong to the same layer.”

167. As set forth above for claim 6, it would have been obvious to a POSITA to combine the teachings of Weaver and Song to reconfigure the bus line 430 of Weaver with a bottom electrode layer (akin to Song’s **bottom electrode layer** of first auxiliary electrode portion SE1) that is electrically connected with a top electrode layer (akin to Song’s **top electrode layer** of first auxiliary electrode portion SE1), wherein the first electrode layer (anode 406) of the light emitting

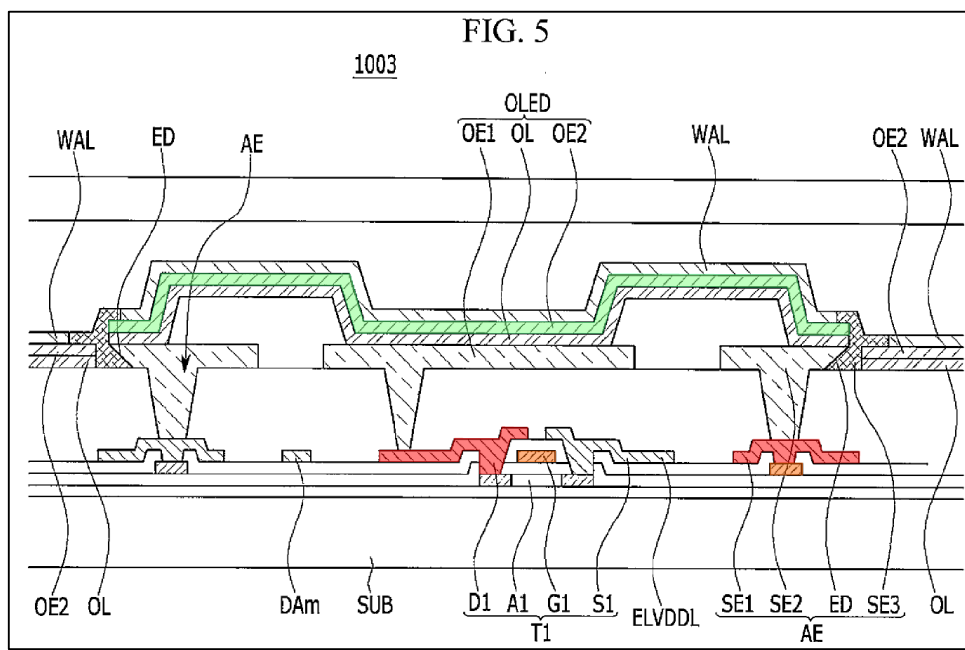
device 400 of Weaver is electrically connected with the top electrode layer. See §XII.A.

168. As explained in §XI.C, Weaver discloses that **bus line 430**, and **source region 405** and **drain region 407** of transistor 410 are formed in the same layer. Specifically, Weaver discloses that in forming the device of Fig. 4, a source/drain level metal (e.g. Mo) is deposited and patterned to form data line 401, source/drain 408, contact 402, **drain 405 and source 407**, ground line 403, a top electrode 432 of the storage capacitor and **ITO bus line 430**. EX1004, [0034], Fig. 6.



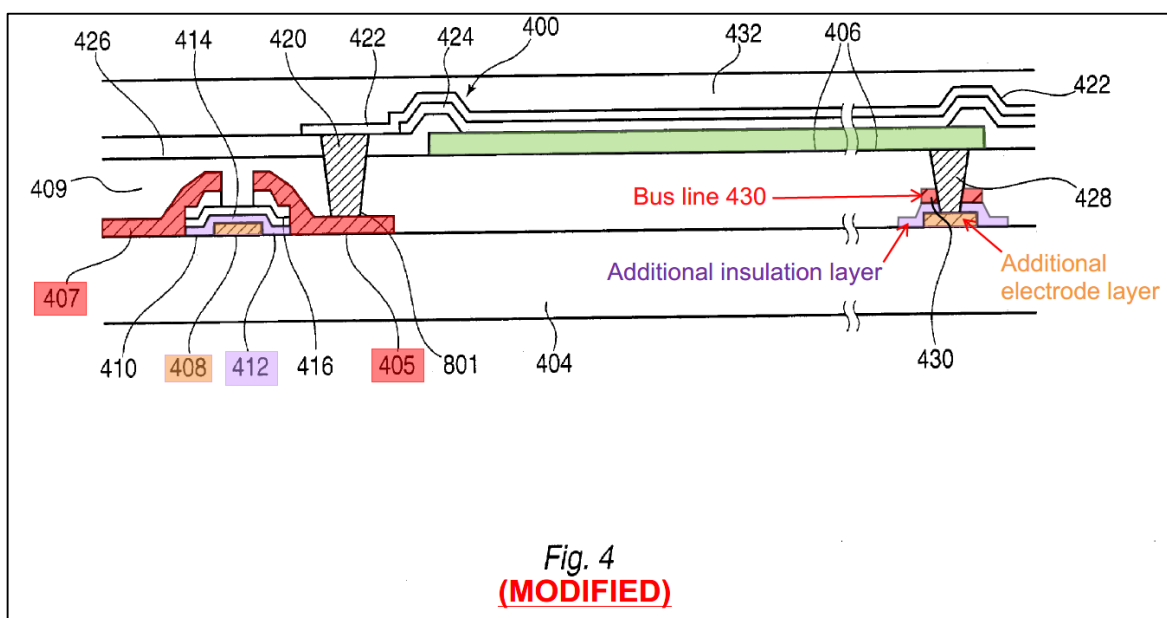
A POSITA would have understood that reference to drain 405 and source 407 in ¶[0034] is referring to source region 405 and drain region 407 of Fig. 4 (i.e., it is evident that the numbers were inadvertently transposed).

169. Song discloses that the **first drain electrode D1** and the **top electrode layer** of the first auxiliary electrode portion SE1 are formed of the same sublayer. See §XII.A.



170. In combining the teachings of Weaver and Song as set forth above in §XII.A, it would have been obvious to a POSITA to form the top electrode layer of the first auxiliary electrode (i.e. **bus line 430**), and the **source region 405** and the **drain region 407** transistor 410 in Weaver, so they belong to the same layer.

EX1004, [0034], Fig.4, Fig. 6.



171. Weaver and Song are analogous prior art to the 509 patent. *See* §XII.A.

172. A POSITA would have understood the problem involved, namely how to efficiently form the various layers of the device. To overcome this problem, Song discloses the solution of forming the **first drain electrode D1** and the **top electrode layer** of the first auxiliary electrode portion SE1 of the same layer. Doing so simplifies semiconductor manufacturing steps to form the device, reducing the number of the processing steps necessary to fabricate the device. In combining the teachings of Weaver and Song as set forth above in §XII.A, a POSITA would have been motivated to implement the solutions of Song and Weaver to manufacture the device more efficiently.

173. A POSITA would have had a reasonable expectation of success in combining Weaver and Song, as both references disclose the various layers for connecting to and operating a light emitting device with an anode and a cathode, and techniques for their manufacture. The modification to Weaver to implement the solution taught in Song and Weaver involves modifications of only routine skill in the art. Moreover, because combining the teachings of Weaver and Song would involve known methods, it would have yielded predictable results.

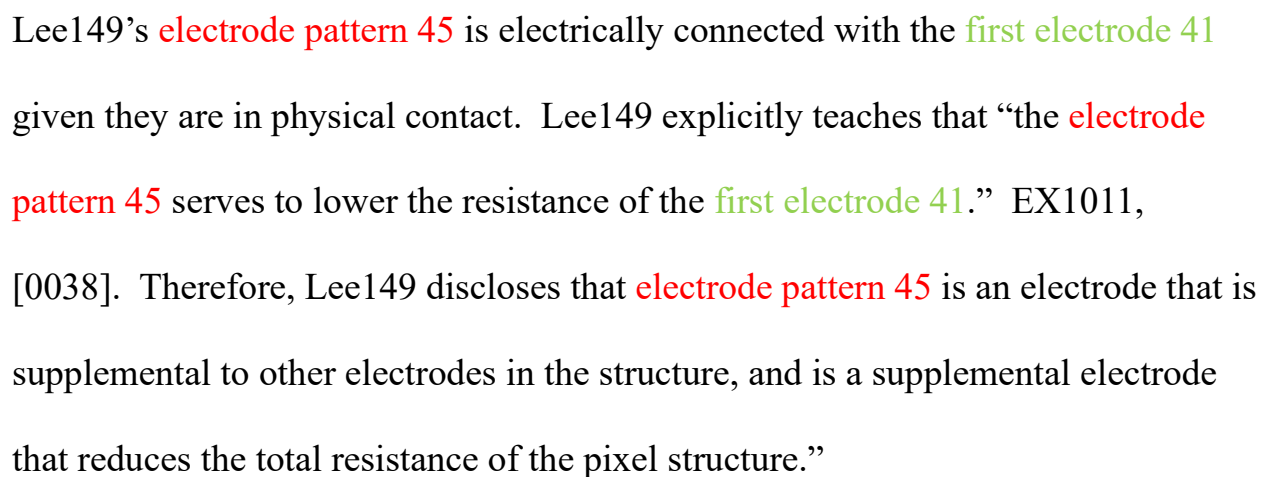
XIII. GROUND 4: CLAIMS 10-11 RENDERED OBVIOUS BY WEAVER AND LEE149

174. The construction of “auxiliary electrode” I applied for Ground 4 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

A. Claim 10

175. The Weaver-Lee149 combination renders obvious “the pixel structure (Weaver’s pixel structure) according to claim 1 (*see* claim 1), further comprising a second auxiliary electrode (Weaver modified with Lee149’s **electrode pattern 45**) electrically insulated from the active device (Weaver’s transistor 410) and disposed at a side of the light emitting device (Weaver’s OLED 400), wherein the second auxiliary electrode is electrically connected with the first electrode layer (Weaver’s anode 406) of the light emitting device (Weaver’s OLED 400).”

177. Lee149 discloses a light emitting diode that includes **first electrode 41**, **organic electroluminescent layer 60**, and **second electrode 70**. EX1011, [0027], Fig. 1. Lee149 discloses “An **electrode pattern 45** is formed on the **first electrode 41** at a central region of the buffer layer 50.” *Id.*, [0027].



178. **Electrode pattern 45** is electrically insulated from **TFT Tr** by planarization layer 29. EX1011, Fig. 1. A POSITA would have understood that planarization layer 29 is made of insulating material, so that electrical features such as source electrode 27a, drain electrode 27b and **first electrode 41** (which are all shown in Fig. 1 in physical contact with planarization layer 29) are not electrically shorted together by planarization layer 29, which would render the device inoperable.

179. Lee149's **electrode pattern 45** is disposed at a side (i.e., the left side) of the light emitting device (light emitting diode that includes **first electrode 41**, **organic electroluminescent layer 60**, **second electrode 70**). EX1011, Fig. 1. Specifically, **electrode pattern 45** overlaps in the horizontal direction with the **organic electroluminescent layer 60** and **second electrode 70** of the light emitting diode which satisfies this term under the proper construction. The partial vertical overlap of **electrode pattern 45** and **first electrode 41** does not preclude a finding that Lee149 discloses the **electrode pattern 45** is disposed "at a side" of the light emitting diode under the proper construction.

180. It would have been obvious to a POSITA to combine the teachings of Weaver and Lee149 to add a second auxiliary electrode to the side of the OLED 400 of Weaver (akin to Lee149's **electrode pattern 45**), wherein the first electrode

layer (anode 406) of the light emitting device 400 of Weaver is electrically connected with the second auxiliary electrode.

181. Weaver and Lee149 are analogous prior art to the 509 patent, as each relates to organic light emitting devices with an organic light emitting layer disposed between an anode electrode layer and a cathode electrode layer, as well as the surrounding layers and circuits to operate the light emitting devices.

182. A POSITA would have understood the problem involved, namely that higher sheet resistance between the power or ground line to the light emitting device would consume more power and require higher operating voltages because of the higher voltage drop of the OLED display. To overcome this problem, Lee149 discloses the solution of providing the second auxiliary electrode (electrode pattern 45) disposed at a side of the light emitting device and electrically connected to the light emitting device's first electrode layer (first electrode 41). Lee149 explicitly teaches that "the electrode pattern 45 serves to lower the resistance of the first electrode 41." EX1011, [0038]. The first electrode layer 41a and third electrode layer 41c are formed of a transparent material such as ITO, IZO, or ITZO. *Id.*, [0025], [0038]. A POSITA would have been motivated to implement the solution of Lee149 in the Weaver device to lower the resistance and voltage drop between anode 406 and the VDD line of Weaver. This is consistent with the teachings of Weaver, which discloses concerns about non-uniformities

caused by voltage drops across the OLED, and using highly conductive material (indium tin oxide – ITO) for the **anode 406** and the **bus line 430**. EX1004, [0017], [0030], [0034], [0036].

183. The modification to Weaver could be implemented, for example, by forming a contact window with an undercut (similar to that of Lee’s buffer layer 50) over the anode 406 before forming the cathode 422, so that when the conductive layer for cathode 422 is formed, it would result in a first portion of the conductive layer as the cathode 422 of OLED 400 and a separate second portion of the conductive layer in the contact window as the second auxiliary electrode at a side of the OLED 400.

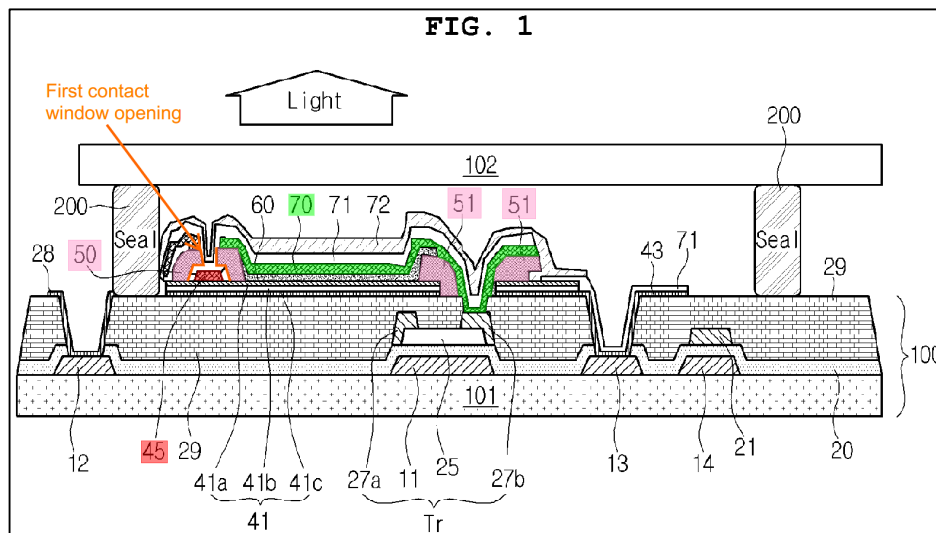
184. A POSITA would have had a reasonable expectation of success in combining Weaver and Lee149, as both references disclose the various layers for connecting to and operating a light emitting device with an anode and a cathode, and the modification to Weaver to implement the solution taught in Lee149 involves modifications of only routine skill in the art. Moreover, because combining the teachings of Weaver and Lee149 would involve known methods, it would have yielded predictable results.

B. Claim 11

185. The Weaver-Lee149 combination renders obvious “the pixel structure (Weaver’s pixel structure) according to claim 10 (*see* claim 10), wherein the

second auxiliary electrode (Weaver modified with Lee149's **electrode pattern 45**) and the second electrode layer (Weaver's cathode 422) of the light emitting device (Weaver's OLED 400) belong to the same layer, and the second auxiliary electrode and the second electrode layer of the light emitting device are electrically insulated from each other."

186. Fig. 1 of Lee149 shows that the **electrode pattern 45** is electrically insulated from the **second electrode 70** by **buffer layer 50**.



187. Lee149 further discloses:

"When the **buffer layer 50** is formed as described above, the organic electroluminescent layer 60 is formed at the sub-pixel region and subsequently a metal layer is formed on the dielectric substrate 101 to form the **second electrode 70** on the organic electroluminescent layer 60. The metal layer is separated from the undercut region to form the **second electrode 70** in the sub-pixel unit. At this point, the **electrode**

pattern 45 is formed on the first electrode 41 at the undercut region of the buffer layer 50.” EX1011, [0038].

A POSITA would have understood that Lee149 is disclosing that the metal layer deposited to form second electrode 70 is also deposited through the first contact window opening of buffer layer 50, which has the undercut region. The undercut region of first contact window opening is what serves to separate the second electrode 70 from the electrode pattern 45. Therefore, a POSITA would have understood that the second electrode 70 and the electrode pattern 45 belong to the same metal layer.

188. A POSITA would have understood forming different features in or at a same layer simplifies manufacturing, making it more efficient. In combining the teachings of Weaver and Lee149 as set forth above in §XIII.A for claim 10 (i.e., including a second auxiliary electrode to the side of OLED 400 and connected to the anode 406 of Weaver), it would have been obvious to a POSITA to form such a second auxiliary electrode (to the side of OLED 400) of a same layer as the cathode 422 (of OLED 400) in order to simplify manufacturing, as taught by Lee149. Further, because the second auxiliary electrode would be electrically connected with the first electrode layer of the light emitting device (*see* §XIII.A for claim 10), it would have also been obvious to have the second auxiliary electrode and the second electrode layer of the light emitting device be electrically insulated

from each other (otherwise the electrode layers of the light emitting device would be shorted together and non-operational).

189. Weaver and Lee149 are analogous prior art to the 059 patent. *See* §XIII.A.

190. A POSITA would have understood the problem involved, namely how to efficiently form the various features of the OLED device in a semiconductor process flow. To overcome this problem, Lee149 discloses the solution of forming the second electrode layer of the light emitting device (second electrode 70) and the second auxiliary electrode (electrode pattern 45) so that they belong to the same metal layer. A POSITA would have been motivated to implement the solution of Lee149 in the Weaver device to more efficiently form the OLED device.

191. The modification to Weaver could be implemented, for example, by forming a contact window with an undercut (similar to that of Lee's buffer layer 50) over the anode 406 before forming the cathode 422, so that when the conductive layer for cathode 422 is formed, it would result in a first portion of the conductive layer as the cathode 422 of OLED 400 and a separate second portion of the conductive layer in the contact window as the second auxiliary electrode at a side of the OLED 400.

192. A POSITA would have had a reasonable expectation of success in combining Weaver and Lee149, as both references disclose the various layers for connecting to and operating a light emitting device with an anode and a cathode, and the modification to Weaver to implement the solution taught in Lee149 involves modifications of only routine skill in the art. Moreover, because combining the teachings of Weaver and Lee149 would involve known methods, it would have yielded predictable results.

XIV. GROUND 5: CLAIMS 10-11 RENDERED OBVIOUS BY WEAVER AND BAE

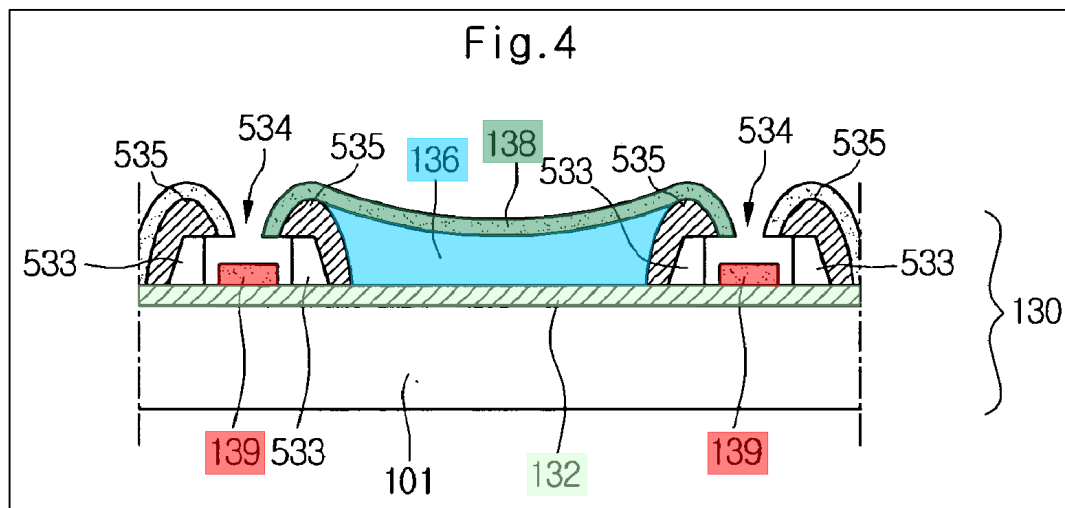
193. The construction of “auxiliary electrode” I applied for Ground 5 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

A. Claim 10

194. The Weaver-Bae combination renders obvious “the pixel structure (Weaver’s pixel structure) according to claim 1 (*see* claim 1), further comprising a second auxiliary electrode (Weaver modified with Bae’s **auxiliary electrodes 139**) electrically insulated from the active device (Weaver’s transistor 410) and disposed at a side of the light emitting device (Weaver’s OLED 400), wherein the second auxiliary electrode is electrically connected with the first electrode layer (Weaver’s anode 406) of the light emitting device (Weaver’s OLED 400).”

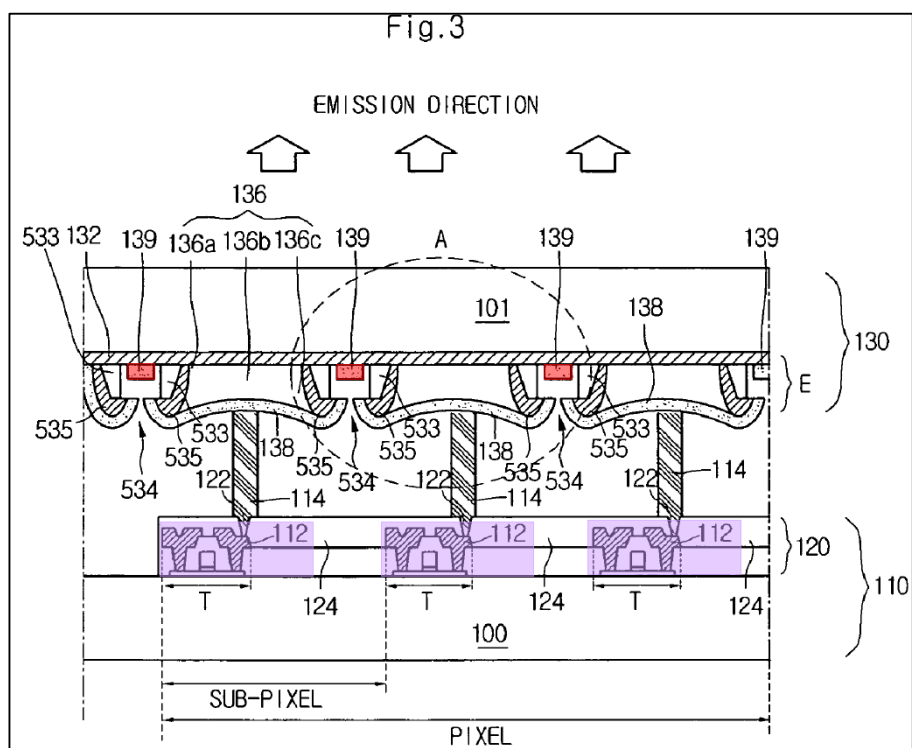
195. A POSITA would have understood that reciting “the active device” (singular) in claim 1 or in claims dependent thereon refers to one of the “at least one active device” of claim 1 if there is more than one. See ¶89, §X.A.4

196. Bae discloses an organic electro-luminance diode E that includes a first electrode 132, an organic electro-luminescent layer 136, and a second electrode 138. EX1012, [0041]-[0043], Fig. 4. Bae discloses auxiliary electrodes 139 arranged around the sub-pixels in a grid shape, and in contact with the first electrode 132 to commonly apply a voltage to the sub-pixels, and “serves to lower the resistance of the first electrode 132.” *Id.*, [0037], [0059].



Bae discloses that auxiliary electrodes 139 is an electrode that is supplemental to other electrodes in the structure, and is a supplemental electrode that reduces the total resistance of the pixel structure.”

197. Auxiliary electrodes 139 is electrically insulated from TFT T by at least passivation layer 124. EX1012, [0048], Fig. 3.



A POSITA would have understood that passivation layer 124 is made of insulating material, so that electrical features of TFT T are not electrically shorted together which would render the device in operatable.

198. Bae's **auxiliary electrode 139** is disposed at a side of the light emitting device (**first electrode 132**, **organic electro-luminescent layer 136**, and **second electrode 138**). EX1012, Fig. 4. Specifically, **auxiliary electrode 139** overlaps in the horizontal direction with **organic electro-luminescent layer 136** of the organic electro-luminance diode E which satisfies the term under the proper construction. The partial vertical overlap of **auxiliary electrode 139** with **first electrode 132** and **second electrode 138** does not preclude a finding that Bae discloses the **auxiliary**

electrode 139 is disposed “at a side” of the light emitting device under the proper construction.

199. It would have been obvious to a POSITA to combine the teachings of Weaver and Bae to add a second auxiliary electrode to the side of the OLED 400 of Weaver (akin to Bae’s auxiliary electrode 139), wherein the first electrode layer (anode 406) of the light emitting device 400 of Weaver is electrically connected with the second auxiliary electrode.

200. Weaver and Bae are analogous prior art to the 509 patent, as each relates to organic light emitting devices with an organic light emitting layer disposed between an anode electrode layer and a cathode electrode layer, as well as the surrounding layers and circuits to operate the light emitting devices.

201. A POSITA would have understood the problem involved, namely that higher resistance between the power or ground line to the light emitting device would consume more power and require higher operating voltages because of the higher voltage drop of the OLED display. To overcome this problem, Bae discloses the solution of providing the second auxiliary electrode (auxiliary electrode 139) disposed at a side of the light emitting device and electrically connected to the light emitting device’s first electrode layer (first electrode 132). Bae explicitly teaches that the “auxiliary electrodes 139 contact the first electrode 132 to commonly apply a voltage to the sub-pixels” and the “auxiliary electrode

139 reduces the resistance of the first electrode 132.” EX1012, [0037], [0059]. A POSITA would have been motivated to implement the solution of Bae in the Weaver device to lower the resistance and voltage drop between anode 406 and the VDD line of Weaver. This is consistent with the teachings of Weaver, which discloses concerns about non-uniformities caused by voltage drops across the OLED, and using highly conductive material (indium tin oxide – ITO) for the anode 406 and the bus line 430. EX1004, [0017], [0030], [0034], [0036].

202. The modification to Weaver could be implemented, for example, by forming a contact window with an undercut (similar to that of Bae’s buffer layer 535) over the anode 406 before forming the cathode 422, so that when the conductive layer for cathode 422 is formed, it would result in a first portion of the conductive layer as the cathode 422 of OLED 400 and a separate second portion of the conductive layer in the contact window as the second auxiliary electrode at a side of the OLED 400.

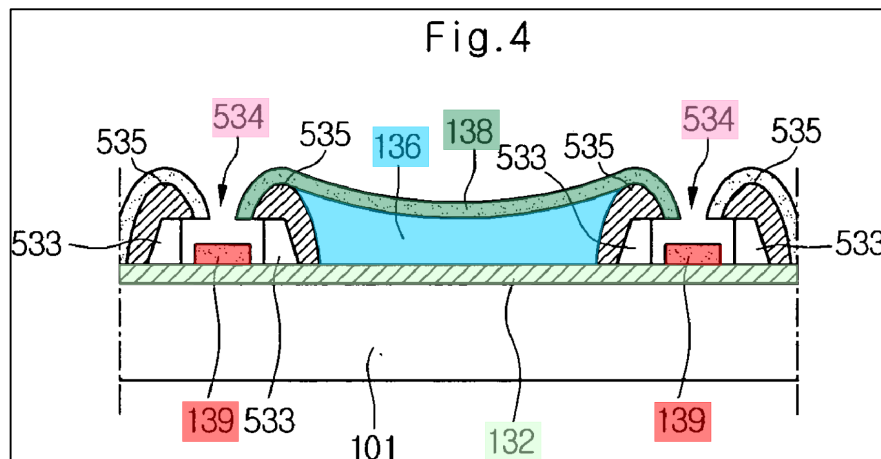
203. A POSITA would have had a reasonable expectation of success in combining Weaver and Bae, as both references disclose the various layers for connecting to and operating a light emitting device with an anode and a cathode, and the modification to Weaver to implement the solution taught in Bae involves modifications of only routine skill in the art. Moreover, because combining the

teachings of Weaver and Bae would involve known methods, it would have yielded predictable results.

B. Claim 11

204. The Weaver-Bae combination renders obvious “the pixel structure (Weaver’s pixel structure) according to claim 10 (*see* claim 10), wherein the second auxiliary electrode (Weaver modified with Bae’s **auxiliary electrode 139**) and the second electrode layer (Weaver’s cathode 422) of the light emitting device (Weaver’s OLED 400) belong to the same layer, and the second auxiliary electrode and the second electrode layer of the light emitting device are electrically insulated from each other.”

205. Fig. 4 of Bae shows that **auxiliary electrode 139** is electrically insulated from the **second electrode 138** by **space 534**.



206. Bae further discloses that the “auxiliary electrodes 139, which are formed of the same material as the second electrode 138, is formed on the first electrode.” *Id.*, [0039]. Bae explains:

“Also, the auxiliary electrode 139 is formed on the first electrode 132 in the space 534 formed by the undercut structure. The auxiliary electrode 139 is formed during the process of forming the second electrode 138. The auxiliary electrode 139 reduces the resistance of the first electrode 132. Specifically, at least one surface of the first buffer 533 is formed inwardly from the second buffer 535 with a gap greater than 0.1 μm .”

207. A POSITA would have understood that Bae is disclosing that the material deposited to form second electrode 138 is also deposited through the space 534 in second buffer 535 which has the undercut region. The undercut region and space 534 of second buffer 535 is what serves to separate the second electrode 138 from the auxiliary electrode 139. Therefore, a POSITA would have understood that the second electrode 138 and the auxiliary electrode 139 belong to the same metal layer.

208. A POSITA would have understood forming different features in or at a same layer simplifies manufacturing, making it more efficient. In combining the teachings of Weaver and Bae as set forth above in §XIV.A for claim 10 (i.e.,

including a second auxiliary electrode to the side of OLED 400 and connected to the anode 406 of Weaver), it would have been obvious to a POSITA to form such a second auxiliary electrode (to the side of OLED 400) of a same layer as the cathode 422 (of OLED 400) in order to simplify manufacturing, as taught by Bae. Further, because the second auxiliary electrode would be electrically connected with the first electrode layer of the light emitting device (*see* §XIV.A), it would have also been obvious to have the second auxiliary electrode and the second electrode layer of the light emitting device be electrically insulated from each other (otherwise the electrode layers of the light emitting device would be shorted together and non-operational).

209. Weaver and Bae are analogous prior art to the 059 patent. *See* §XIV.A.

210. A POSITA would have understood the problem involved, namely how to efficiently form the various features of the OLED device in a semiconductor process flow. To overcome this problem, Bae discloses the solution of forming the second electrode layer of the light emitting device (**second electrode 138**) and the second auxiliary electrode (**auxiliary electrode 139**) so that they belong to the same metal layer. A POSITA would have been motivated to implement the solution of Bae in the Weaver device to more efficiently form the OLED device.

211. The modification to Weaver could be implemented, for example, by forming a contact window with an undercut (similar to the undercut of Bae's second buffer 535) over the anode 406 before forming the cathode 422, so that when the conductive layer for cathode 422 is formed, it would result in a first portion of the conductive layer as the cathode 422 of OLED 400 and a separate second portion of the conductive layer in the contact window as the second auxiliary electrode at a side of the OLED 400.

212. A POSITA would have had a reasonable expectation of success in combining Weaver and Bae, as both references disclose the various layers for connecting to and operating a light emitting device with an anode and a cathode, and the modification to Weaver to implement the solution taught in Bae involves modifications of only routine skill in the art. Moreover, because combining the teachings of Weaver and Bae would involve known methods, it would have yielded predictable results.

XV. GROUND 6: CLAIMS 1-5, 9, 12-13 RENDERED OBVIOUS BY WEAVER IN VIEW OF GUPTA OR HAN

213. The construction of “auxiliary electrode” I applied for Ground 6 is “supplemental electrode to reduce the total resistance of the pixel structure.”

A. Claim 1

1. [1pre]

214. *See* §X.A.1.

2. [1a]

215. *See* §X.A.2.

3. [1b]

216. *See* §X.A.3.

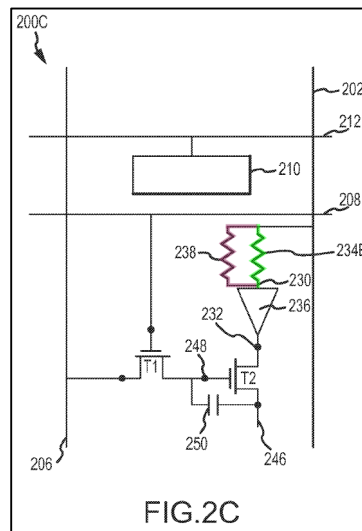
4. [1c]

217. *See* §X.A.4.

218. Should the PO argue, or the Board conclude, that Weaver does not disclose an auxiliary electrode under the narrow construction (“supplemental electrode to reduce the total resistance of the pixel structure”), Weaver in combination with Gupta or Han renders obvious “a first auxiliary electrode (Weaver’s **bus line 430** modified with a parallel connection with **anode 406**) electrically insulated from the active device (Weaver’s **transistor 410**)”

219. Gupta discloses that an organic light emitting diode (OLED) “generally includes an anode, one or more organic layers, and a cathode.” EX1009, 1:25-27. Gupta identifies the need to reduce the sheet resistance of the common OLED electrode (a transparent conductive material like indium-tin-oxide ITO) in top emission OLEDs such that less power may be required from a power supply to operate the OLEDs. *Id.*, 1:44-61. Specifically, for inverted top emission OLEDs, “An additional voltage is required from the VDD due to the high sheet resistance 234B on the anode 230 which is the common electrode 232 in the inverted OLED.” *Id.*, 8:6-8.

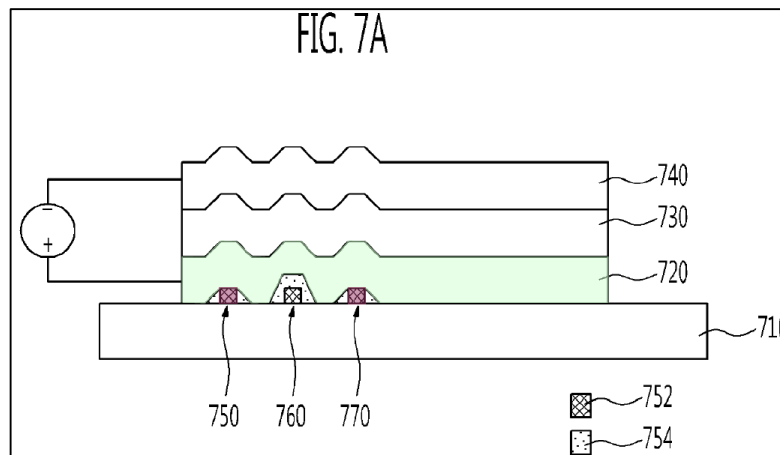
220. Gupta discloses a solution for an OLED sub-pixel 236 as shown in Fig. 2C, where the anode 230 (having an anode sheet resistance 234B) is connected to power supply VDD 202, and “a resistor 238 is added to be in parallel with the anode sheet resistance 234B to reduce the total resistance between anode 230 and VDD 202.” *Id.*, 8:3-14, Fig. 2C.



221. The resistor 238 may be formed of a conductive mesh or strip. *Id.*, 7:42-43. For AMOLED displays having such a conductive mesh or strip coupled to the common electrode (i.e., the anode 230) to reduce its sheet resistance, the “reduced sheet resistance of the common electrode helps save power consumption in operating the AMOLED displays.” *Id.*, 4:55-60. Resistor 238 is a supplemental electrode that reduces the total resistance of the pixel structure that includes OLED sub-pixel 236 by providing an additional electrode (and additional current path) connected in parallel with the anode 230 and its sheet resistance 234B to the power

supply VDD 202. Gupta discloses this solution can be implemented in both inverted OLEDs and standard (non-inverted) OLEDs. EX1009, 5:8-9, Figs. 2A and 2B.

222. Han discloses that an organic light emitting diode (OLED) can include an organic emission layer (EML) between an anode and a cathode, where the organic EML emits light when power is applied between the anode and the cathode. EX1010, [0008]. Specifically, organic EML (emission layer) 730 is interposed between an anode 720 and a cathode 740. *Id.*, [0030]-[0031], Fig. 7A.



One problem with OLED's is that IR-drop that may occur due to resistance of components such as the anode and the cathode. *Id.*, [0009]. Han discloses a solution that includes the addition of “first and third subsidiary electrodes 750 and 770, which may be bonded to the anode 720 and function to reduce a resistance component of the anode 720.” *Id.*, [0032]. Han further discloses that “each of the first and third subsidiary electrodes 750 and 770 may be electrically connected in

parallel to the **anode 720** in the emission region and function to reduce the influence of IR-drop due to a driving current.” *Id.*, [0033]. **First and third subsidiary electrodes 750 and 770** are supplemental electrodes that reduce the total resistance of the pixel structure that includes the OLED by providing additional electrodes (and additional current paths) connected in parallel with the **anode 720**.

223. It would have been obvious to a POSITA to combine the teachings of Weaver and either Gupta or Han so that bus line 430 of Weaver is connected in parallel with anode 406 to voltage supply line VDD in order to reduce the overall resistance of the pixel structure that includes OLED 400.

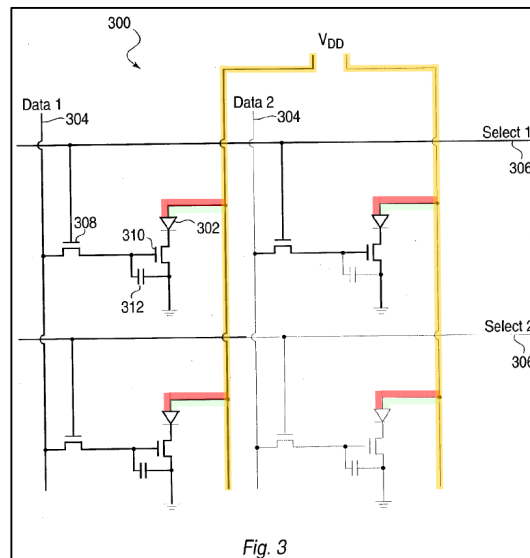
224. Gupta, Han and Weaver are analogous prior art to the 509 patent, as each relates to organic light emitting devices with an organic light emitting layer disposed between an anode electrode layer and a cathode electrode layer, as well as the surrounding layers and circuits to operate the light emitting devices.

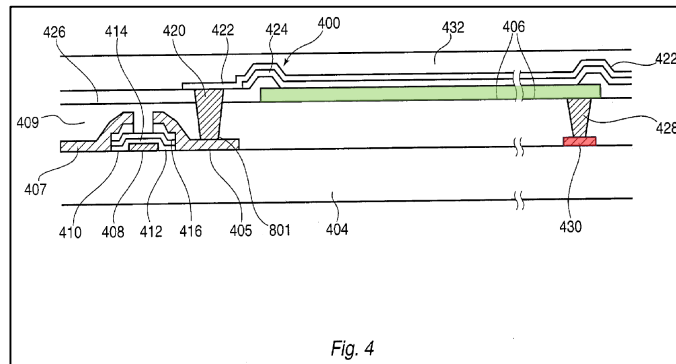
225. A POSITA would have understood the problem involved, namely that higher resistance between the power or ground line to the light emitting device would increase the IR-drop and power consumption to operate the OLEDs. EX1009, 1:58-61; EX1010, [0009].

226. To overcome this problem, Gupta and Han disclose the solution of connecting the auxiliary electrode and the anode in parallel so as to reduce the total resistance of the pixel structure that includes the OLED. A POSITA would have

been motivated to implement the solution of Gupta or Han in the Weaver device to lower the resistance and voltage drop between anode 406 and the VDD line of Weaver. This is consistent with the teachings of Weaver, which discloses concerns about non-uniformities caused by voltage drops across the OLED, and using highly conductive material (indium tin oxide – ITO) for the anode 406 and the bus line 430. EX1004, [0017], [0030], [0034], [0036].

227. The modification to Weaver could be implemented, for example, by connecting the bus line 430 and anode 406 of OLED 302/400 in parallel to the VDD line of Weaver. *Id.*, Figs. 3 and 4.





Alternately, **bus line 430** could be connected in parallel to just a portion of the **anode 406**, which would still result in **bus line 430** serving as a supplemental electrode to reduce the total resistance of the pixel structure.

228. A POSITA would have had a reasonable expectation of success in combining Weaver with Gupta or Han, as all these references disclose the various electrodes and connections for operating an organic light emitting device with an anode and a cathode and an organic light emitting layer, and the modification to Weaver to implement the solution taught in Gupta or Han involves modifications of only routine skill in the art. Moreover, because combining the teachings of Weaver and Gupta or Han would involve known methods, it would have yielded predictable results.

5. [1d]

229. See §X.A.5 and §XV.A.4.

6. [1e]

230. See §X.A.6 and §XV.A.4.

7. [1f]

231. *See* §X.A.7 and §XV.A.4.

8. [1g]

232. *See* §X.A.8 and §XV.A.4.

B. Claim 2

233. *See* §X.B and §XV.A.4.

C. Claim 3

234. *See* §X.C and §XV.A.4.

D. Claim 4

235. *See* §X.D and §XV.A.4.

E. Claim 5

236. *See* §X.E and §XV.A.4.

F. Claim 9

237. *See* §X.F and §XV.A.4.

G. Claim 12

238. *See* §X.G and §XV.A.4.

H. Claim 13

239. *See* §X.H and §XV.A.4.

XVI. GROUND 7: CLAIMS 6-8 RENDERED OBVIOUS BY WEAVER AND LEE053, IN VIEW OF GUPTA OR HAN

240. The construction of “auxiliary electrode” I applied for Ground 7 is “supplemental electrode to reduce the total resistance of the pixel structure.”

A. Claim 6

241. *See* §XI.A and §XV.A.4.

B. Claim 7

242. *See* §XI.B and §XV.A.4.

C. Claim 8

243. *See* §XI.C and §XV.A.4.

XVII. GROUND 8: CLAIMS 6-8 RENDERED OBVIOUS BY WEAVER AND SONG, IN VIEW OF GUPTA OR HAN

244. The construction of “auxiliary electrode” I applied for Ground 8 is “supplemental electrode to reduce the total resistance of the pixel structure.”

A. Claim 6

245. *See* §XII.A and §XV.A.4.

B. Claim 7

246. *See* §XII.B and §XV.A.4.

C. Claim 8

247. *See* §XII.C and §XV.A.4.

XVIII. GROUND 9: CLAIMS 10-11 RENDERED OBVIOUS BY WEAVER AND LEE149, IN VIEW OF GUPTA OR HAN

248. The construction of “auxiliary electrode” I applied for Ground 9 is “supplemental electrode to reduce the total resistance of the pixel structure.”

A. Claim 10

249. *See* §XIII.A and §XV.A.4.

250. Should the PO argue, or the Board conclude, that Weaver and Lee149 do not disclose the second auxiliary electrode under the narrow construction (“supplemental electrode to reduce the total resistance of the pixel structure”), then all of the reasons set forth in §X.A.4 for why it would have been obvious to connect Weaver’s bus line 430 in parallel with anode 406 to voltage supply line VDD in order to reduce the overall resistance of the pixel structure that includes OLED 400 equally applies to second auxiliary electrode added to the side of the OLED 400 in view of Lee149 as set forth in §VIII.A (i.e., it would have been obvious to connect the second auxiliary electrode added to Weaver in parallel with anode 406 to voltage supply line VDD in order to reduce the overall resistance of the pixel structure). This is especially so given that Lee149 discloses its “the electrode pattern 45 serves to lower the resistance of the first electrode 41.” EX1011, [0038].

B. Claim 11

251. *See* §XIII.B and §XV.A.4.

XIX. GROUND 10: CLAIMS 10-11 RENDERED OBVIOUS BY WEAVER AND BAE, IN VIEW OF GUPTA OR HAN

252. The construction of “auxiliary electrode” I applied for Ground 10 is “supplemental electrode to reduce the total resistance of the pixel structure.”

A. Claim 10

253. *See* §XIV.A and §XV.A.4.

254. Should the PO argue, or the Board conclude, that Weaver and Bae do not disclose the second auxiliary electrode under the narrow construction (“supplemental electrode to reduce the total resistance of the pixel structure”), then all of the reasons set forth in §X.A.4 for why it would have been obvious to connect Weaver’s bus line 430 in parallel with anode 406 to voltage supply line VDD in order to reduce the overall resistance of the pixel structure that includes OLED 400 equally applies to second auxiliary electrode added to the side of the OLED 400 in view of Bae as set forth in §IX.A (i.e., it would have been obvious to connect the second auxiliary electrode added to Weaver in parallel with anode 406 to voltage supply line VDD in order to reduce the overall resistance of the pixel structure). This is especially so given that Bae discloses its “auxiliary electrode 139 serves to lower the resistance of the first electrode 132.” EX1012, [0059].

B. Claim 11

255. *See* §XIV.B and §XV.A.4.

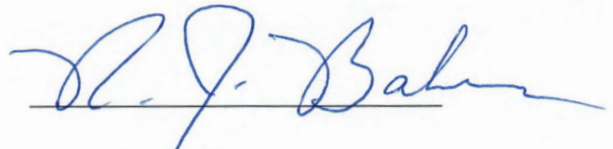
XX. CONCLUSION

256. My opinions are based upon the information that I have considered to date. I am unaware of any evidence of secondary considerations with respect to the 509 patent that would render any of the asserted claims non-obvious. I reserve the right, however, to supplement my opinions in the future to respond to any arguments raised by the patent owner of the 509 patent and to consider new information that becomes available to me.

257. I hereby declare under penalty of perjury under the laws of the United States of America that the following is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code.

July 5, 2024

Date


Dr. R. Jacob Baker

APPENDIX B

R. JACOB BAKER, PH.D., P.E.

professor emeritus of electrical and computer engineering

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PROFESSIONAL SUMMARY

Russel Jacob Baker (R. Jacob Baker), Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas (UNLV) in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno (UNR) in 1993. His Google Scholar profile is [here](#) and his ResearchGate profile is [here](#).

From 1981-1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985-1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time he designed, and oversaw the fabrication and the electrical/mechanical manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs for high-speed imaging, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1993 he was an adjunct faculty member in the Departments of Electrical Engineering at UNLV and UNR. From 1993-2000 he served on the faculty in the Department of Electrical Engineering at the University of Idaho (UI), first as an untenured assistant professor and then from 1998 as a tenured associate professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to professor in 2002. He then served as the ECE department chair from 2004-2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he rejoined the faculty at UNLV as a tenured full professor of ECE. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than [100 graduate students](#).

Dr. Baker has done consulting for over [200 companies](#). His [research/development](#) activities are in: photonics, circuit design for wireless and wired communications, analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, design of digital processors for signal processing, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of [online engineering education](#). As a result of this work, he is the named inventor on over [150 US patents](#) and the author of over [100 publications](#).

He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over [50 invited talks](#) around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society,

the 2007 Frederick Emmons Terman Award, the 2011 IEEE Circuits and Systems Education Award, and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2024).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpel Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonic application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded processors, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project

between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and processors.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho:** Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
 - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
 - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
 - Design of high-voltage and energy switching circuits
 - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
 - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
 - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
 - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
 - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
 - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
 - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
 - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
 - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
 - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
 - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
 - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering; May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 22 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMETS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. J., (2023-2024) "Silicon Germanium (SiGe) Avalanche Photo Diode (APD) Chip," Department of Energy, Mission Support and Test Services (MSTS), LLC, \$120,000
- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, \$29,999 (Phase I), \$225,238 (Phase II), and \$79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, \$50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, \$149,998
- Baker, R. Jacob, (2018-2020) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, \$99,996

- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, \$29,999
- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, \$29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), \$266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, \$299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, \$299,665

DOCTORAL STUDENT SUPERVISION

10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyang Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

91. Jazmine Bolor – Survey of how Irregular Pathways in the Electrical System of the Human Heart Link to Different Heart Arrhythmias (2023)
90. Abraham Lopez – An Avalanche-Transistor-Based Pulse Generator Design For Infrared Laser Applications (2023)
89. David Santiago – Development of an Automated GPIB System for Characterization of SiGe Avalanche Photodiodes (2023)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)
77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)

73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I_O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
39. Rudi Rashwand (2008)
38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)
36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikarla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)

30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
27. Soumya Narasimhan (2006)
26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
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INVITED TALKS (PARTIAL LISTING)

- Harvard, Q. I. and Baker, R. J., "Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design," a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a "Nano-Module."
- Baker, R. J., and Campbell, K. A., "Reconfigurable Analog Electronics using the Memristor."
- Baker, R. J., and Saxena, V., "A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion."
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."
- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."

- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
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EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 105 times, given expert testimony at 13 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., 1 D. Ore., and 1 E.D. Tex.), and participated in 1 mediation.

Banner Witcoff (Chicago, IL and Washington, DC)

Case – ZF Friedrichshafen AG, ZF Active Safety and Electronics US LLC, AND Nissan Motor Company, Ltd. v. Foras Technologies, Ltd.

Case Number – IPR2024-00969. Petition filed on June 24, 2024.

Case Subject Matter – Detecting loss of lockstep between pairs of processors and loss of lockstep recovery

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (San Diego, CA and Boston, MA)

Case – Vicor Corporation v. Delta Electronics, Inc.

Case Numbers – IPR2024-00704, IPR2024-00705, IPR2024-00706, and IPR2024-00715. Petitions filed on March 25, 2024.

Case Subject Matter – Power converters including design, packaging, heatsinking and manufacturing. Resonant converters with overcurrent protection.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA and Redwood City, CA)

Case – Silicon Motion, Inc. v. Unification Technologies LLC

Case Number – IPR2024-00199. Petition filed on December 18, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Garlick & Markison, LLC (Austin, TX)

Case – NXP USA, Inc. v. Bell Semiconductor, LLC

Case Numbers – IPR2024-00167 and IPR2024-00168. Petitions filed on November 9, 2023.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019288. Request filed on October 20, 2023.

Case Subject Matter – Power conversion device to drive an alternating-current motor for an electric vehicle.

Work Performed – Provided expert consulting services and wrote declaration.

Haynes and Boone, LLP (Dallas, TX)

Case – Western Digital Technologies, Inc. v. Longitude Licensing LTD.

Case Number – IPR2023-01200. Petition filed on July 14, 2023.

Case Subject Matter – Communications between a memory controller and memory.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Mojo Mobility, Inc.

Case Numbers – IPR2023-01094, IPR2023-01095, IPR2023-01096, IPR2023-01097, IPR2023-01098, IPR2023-01099, IPR2023-01100, and IPR2023-01124. Petitions filed on June 30, 2023.

Case Numbers – IPR2023-01101 and IPR2023-01102. Petitions filed on June 29, 2023.

Case Numbers – IPR2023-01091, IPR2023-01092, and IPR2023-01093. Petitions filed on June 28, 2023.

Case Numbers – IPR2023-01086, IPR2023-01087, IPR2023-01088, IPR2023-01089, and IPR2023-01090. Petitions filed on June 27, 2023.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA, Redwood City, CA, Chicago, IL, and Houston, TX)

Case – Unification Technologies LLC v. Silicon Motion, Inc.

Case Number – Texas, ED (Marshall) 2:23-cv-00267. Complaint filed June 2, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – Current Lighting Solutions, LLC d/b/a GE Current v. Jiaying Super Lighting Electric Appliance Co., Ltd.

Case Numbers – IPR2023-00979 and IPR2023-00980. Petitions filed on May 31, 2023.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Baker Botts LLP (Dallas, TX)

Case – Lennox Industries Inc. v. Rosen Technologies LLC

Case Numbers – IPR2023-00715, IPR2023-00716, IPR2023-00717, IPR2023-00718, and IPR2023-00719. Petitions filed on March 29, 2023.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Cooley LLP (Palo Alto, CA)

Case – Nintendo Co., Ltd. and Nintendo of America Inc. v. Polaris PowerLED Technologies, LLC

Case Number – IPR2023-00778. Petition filed on March 28, 2023.

Case Subject Matter – Visual displays, circuit design, and related technologies.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Bracewell LLP (New York, NY and Seattle, WA)

Case – Kioxia America, Inc. and Kioxia Corporation v. BITMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a super capacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Bookoff McAndrews, PLLC (Washington, DC)

Case – Lenovo Inc. and Motorola Mobility LLC v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA)

Case – Semiconductor Design Technologies LLC v. Cadence Design Systems, Inc.

Case Number – California, ND 3:23-cv-01001. Complaint filed March 6, 2023.

Case Subject Matter – Semiconductor design support device/method and manufacturing method for semiconductor integrated circuit.

Work Performed – Provided expert consulting services.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – Xilinx, Inc. v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC. v. Synopsys, Inc.

Case Number – California, SD 3:22-cv-00594. Complaint filed on January 31, 2023.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services and wrote expert reports.

Fish & Richardson P.C. (Washington, DC, Atlanta, GA, and Boston, MA)

Case – Element Capital Commercial Company PTE. LTD v. BOE Technology Group Co. LTD and Motorola (Wuhan) Mobility

Case Number – Texas, ED (Marshall) 2:22-cv-00118. Complaint filed January 11, 2023.

Case Subject Matter – Display technology, layout, circuit design, pixel design and fabrication.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Baker Botts LLP (San Francisco, CA and New York, NY) and O'Melveny & Myers LLP (Los Angeles, CA)

Case – Polaris PowerLED, LLC v. Samsung Electronics and Samsung Display

Case Number – Texas, ED (Marshall) 2:22-cv-00469. Complaint filed December 12, 2022.

Case Subject Matter – active matrix organic light-emitting diode (AMOLED) displays, controlling the intensity of light-emitting diodes in backlights of displays, control circuits for adjusting current delivery based upon temperature.

Work Performed – Provided expert consulting services including writing a declaration for claim construction.

Arnold & Porter (Los Angeles and Palo Alto, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Synopsys, Inc. and Cadence Design Systems, Inc. v. Bell Semiconductor, LLC.

Case Number – Delaware, 1:22-cv-01512. Complaint filed on November 18, 2022.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

Russ August & Kabat (Los Angeles, CA)

Case – Resonant Systems, Inc. v. Sony

Case Number – Texas, ED (Marshall) 2:22-cv-00424. Complaint filed on October 26, 2022.

Case Subject Matter – Linear vibration modules and linear-resonant vibration modules.

Work Performed – Provided expert consulting services and wrote claim construction disclosure.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC v. NXP, SMC, Micron, Nvidia, Advanced Micro Devices (AMD), Acer, Infineon, Qualcomm, Motorola Mobility, and Western Digital

Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.

Case Subject Matter – Electronic devices, semiconductor devices, and components.

Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. Samsung Electronics and Qualcomm Inc.

Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.

Case Subject Matter – Semiconductor devices, mobile devices, and components.

Work Performed – Provided expert consulting services.

Fish & Richardson P.C. (Boston, MA, Houston, TX, and Washington, DC)

Case – Sonrai Memory LTD. v. Micron Technology, Inc.

Case Number – Texas, WD (Waco) 6:22-cv-00855 and Texas, WD (Waco) 1:23-cv-01407. Complaint filed August 16, 2022.

Case Subject Matter – Portable RAM drive and variable charge pump circuit with dynamic load.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Russ August & Kabat (Los Angeles, CA and New York, NY)

Case – NextGen Innovations, LLC v. Infinera, Fujitsu, AT&T, and Nokia

Case Number – Texas, ED (Marshall) 2:22-cv-00306, Texas, ED (Marshall) 2:22-cv-00307, Texas, ED (Marshall) 2:22-cv-00308, and Texas, ED (Marshall) 2:22-cv-00309. Complaints filed on August 9, 2022.

Case Subject Matter – optical transmission systems including optical components for encoding, transmission (fiber optic transmitters and receivers), and decoding of data and related standards and concepts.

Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed twice.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. SolarEdge Technologies, Inc.

Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.

Case Subject Matter – Solar power optimizers, inverters, and components.

Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Signify North America Corporation v. Shenzhen Intellirocks Tech Co.

Case Number – Texas, WD (Waco) 6:22-cv-00760. Complaint filed on July 8, 2022.

Case Subject Matter – LED packaging, circuits, and systems.

Work Performed – Provided expert consulting services including writing declaration for claim construction. Was deposed.

Baker Botts LLP (Dallas, TX)

Case – Rosen Technologies LLC v. Lennox Industries Inc.

Case Number – Texas, ND (Dallas) 3:22-cv-00732. Complaint filed on June 7, 2022.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Scramoge Technology Ltd.

Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.

Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.

Case Number – IPR2022-00939. Petition filed on April 29, 2022.

Case Subject Matter – An antenna that supports wireless charging using switching power supplies such as flyback converters.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations

Case Number – 90/015020. Request filed on May 2, 2022.

Case Number – 90/014906. Request filed on November 12, 2021.

Case Number – 90/014899. Request filed on November 10, 2021.

Case Number – 90/014888. Request filed on October 21, 2021.

Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.

Case Number – 90/014885. Request filed on October 19, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging.

Work Performed – Provided expert consulting services and wrote declarations.

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – SolarEdge Technologies, Inc. v. Fronius International GMBH

Case Number – IPR2022-00849. Petition filed on April 14, 2022.

Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a “rotate-and-lift” feature.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – Samsung Electronics Co. v. Sonrai Memory Ltd.

Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.

Case Subject Matter – USB devices and circuits for saving power.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – Unified Patents, LLC v. Arigna Technology Limited

Case Number – IPR2022-00285. Petition filed on December 9, 2021.

Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).

Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Samsung Electronics Co., Ltd. v. Lynk Labs, Inc.

Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021.

Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.

Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.

Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.

Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.

Case Subject Matter – Circuit design, including switching power supply design (e.g., flyback), rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).

Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – Pure Storage, Inc. v. Digital Cache, LLC

Case Number – IPR2022-00121. Petition filed on October 29, 2021.

Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – SolarEdge Technologies Ltd. v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung Electronics Co., Ltd. v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – SOLiD, Inc. v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. Sanho Corporation

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. Samsung Electronics Co. LTD.

Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.

Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. Google LLC

Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).

Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).

Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect

Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – TCT Mobile Inc. and TCL Communication, Inc. v. Fundamental Innovation Systems International LLC

Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.

Case Number – IPR2021-00428. Petition filed on January 13, 2021.

Case Number – IPR2021-00410. Petition filed on January 11, 2021.

Case Number – IPR2021-00395. Petition filed on December 31, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. Pictos Technologies, Inc.

Case Number – IPR2021-00557. Petition filed on February 18, 2021.

Case Number – IPR2021-00436. Petition filed on January 19, 2021.

Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. BOE Technology Group Co. Ltd. and Samsung Electronics

Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.

Case Subject Matter – Active matrix OLED display devices and components

Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – Samsung, Inc. v. Garrity Power Services LLC

Case Number – IPR2021-00389. Petition filed on December 31, 2020.

Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.

Morgan, Lewis & Bockius LLP (Palo Alto, CA and Shanghai, CN)

Case – Monolithic Power Systems, Inc. v. Meraki Integrated Circuit Technology, Inc. and Promate Electronic Company, LTD.

Case Number – Texas, WD (Waco) 6:20-cv-00876. Complaint filed on December 24, 2020.

Case Subject Matter – Design of switching power supplies including synchronous rectification.

Work Performed – Provided expert consulting services including declaration for claim construction, trade secret analysis and declaration, and Markman tutorial.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC; Dell Technologies Inc.; Dell Inc.; and HP Inc. v. Unification Technologies LLC

Case Numbers – IPR2021-00343, IPR2021-00344, and IPR2021-00345. Petitions filed on December 22, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews, wrote declarations, and was deposed.

Jones Day (Chicago, IL and Dallas, TX)

Case – WSOU Investments, LLC d/b/a Brazos Licensing and Development v. Xilinx, Inc.

Case Numbers – Delaware, 1:20-cv-01231 and Delaware, 1:20-cv-01233. Complaints filed on November 23, 2020 and September 16, 2020.

Case Subject Matter – Controlling power cycles in communication devices and transferring multiple asynchronous clock signals.

Work Performed – Provided expert consulting services, wrote claim construction declaration, wrote expert reports, and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Cosemi Technologies, Inc. v. EverPro Technologies, Fibbr Technologies, Logitech, Inc., and Facebook Technologies

Case Number – ITC Investigation No. 337-TA-1233. Complaint filed October 28, 2020.

Case Subject Matter – Data cables, including HDMI, Display Port, and USB Type A, USB Type C and USB Type A/C data cables.

Work Performed – Provided expert consulting services.

Kirkland & Ellis LLP (Boston, MA and New York, NY)

Case – Pictos Technologies, Inc. v. Samsung Electronics Co., LTD. and Samsung Semiconductor, Inc.

Case Number – ITC Investigation No. 337-TA-1231. Complaint filed September 25, 2020.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, correction of bad pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote expert report.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. TCT Mobile Inc. and TCL Communication, Inc.

Case Number – Delaware, 1:20-cv-00552. Complaint filed on September 11, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations, expert report on invalidity, and was deposed.

Walters Wilson LLP (Redwood City, CA)

Case – Western Digital Corporation and SanDisk, LLC v. Martin Kuster

Case Numbers – IPR2020-01410 and IPR2020-01411. Petitions filed on August 3, 2020.

Case Subject Matter – Computer connectors such as universal serial bus (USB) that connect to peripheral devices such as mice, keyboards, displays, printers, external storage, etc.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Advanced Micro Devices, Inc. v. Monterey Research, LLC

Case Number – IPR2020-01315. Petition filed on July 16, 2020.

Case Number – IPR2020-00985. Petition filed on May 26, 2020.

Case Subject Matter – Reading and writing to semiconductor memory such as SRAM and double data rate (DDR) DRAM. Buffer circuits with variable current supplies for controlling the rise and fall times of output signals.

Work Performed – Provided expert consulting services for inter partes review, wrote declarations and was deposed twice.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – Unification Technologies LLC v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC

Case Number – Texas, WD (Waco) 6:20-cv-00500. Complaint filed June 5, 2020.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and was deposed.

Ari Law, P.C. (Palo Alto, CA) and Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Sanho Corporation v. Kaijet Technology, Magic Control Technology, and Star View Global

Case Numbers – Georgia, ND (Atlanta) 1:18-cv-05385 (third amended complaint filed November 14, 2019) and Georgia, ND (Atlanta) 1:20-cv-02150 (filed May 19, 2020).

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services, wrote declaration for claim construction, and expert reports. Was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Fundamental Innovation Systems International LLC v. Coolpad Group Limited, Coolpad Technologies, Inc., and Yulong Computer Telecommunication Scientific Co. Ltd.

Case Number – Texas, ED (Marshall) 2:20-cv-00117. Complaint filed on April 23, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA and Shanghai, China)

Case – SMIC, Americas v. Innovative Foundry Technologies LLC

Case Numbers – IPR2020-00837 and IPR2020-00839. Petitions filed on April 14, 2020.

Case Subject Matter – Methods of manufacturing a semiconductor component, such as a short-channel MOS device, including forming graded-junctions using spacers along the sidewalls of a transistor's gate.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Russ August & Kabat (Los Angeles, CA)

Case – Oyster Optics, LLC v. Ciena Corporation

Case Number – California, ND (Oakland) 3:20-cv-02354. Complaint filed on April 7, 2020.

Case Subject Matter – Fiber optic telecommunication systems.

Work Performed – Provided expert consulting services, wrote claim construction declaration, and was deposed.

Russ August & Kabat (Los Angeles, CA)

Case – Seoul Semiconductor Co., Ltd. v. Document Security Systems, Inc.

Case Number – IPR2020-00938. Petition filed on May 18, 2020.

Case – Nichia Corporation v. Document Security Systems, Inc.

Case Number – IPR2020-00908. Petition filed on May 18, 2020.

Case – Cree, Inc. v. Document Security Systems, Inc.

Case Number – IPR2020-00557. Petition filed on February 11, 2020.

Case Subject Matter – Light emitting diodes (LEDs) as a light source, extraction of light.

Work Performed – Provided expert consulting services, wrote declaration for inter partes reviews, and was deposed three times.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Flex Logix Technologies, Inc. v. Konda Technologies Inc.

Case Numbers – IPR2020-00260, IPR2020-00261, and IPR2020-00260. Petitions filed on December 16, 2019.

Case Numbers – PGR2019-00037, PGR2019-00040, and PGR2019-00042. Petitions filed on March 18, 2019.

Case Subject Matter – FPGA layout routing for integrated circuits and networks, electrical and computer engineering.

Work Performed – Provided expert consulting services and wrote declarations for post grant and inter partes reviews.

DLA Piper (Chicago, IL, Houston, TX, and Washington, DC) and White & Case LLP (New York, NY and Washington, DC)

Case – M-Red Inc. v. Panasonic Corporation

Case Number – Texas, ED (Marshall) 2:19-cv-00251. Complaint filed on July 16, 2019.

Case Subject Matter – Integrated circuit electronics adjustment, such as ring oscillators, using auto calibration. Evaluating a known good die using both wire and flip-chip interconnects.

Work Performed – Provided expert consulting services and wrote declaration for claim construction.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – Samsung, Inc. v. NuCurrent, Inc.

Case Number – IPR2019-01217. Petition filed on June 19, 2019.

Case Numbers – PGR2019-00049 and PGR2019-00050. Petitions filed on May 28, 2019.

Case Numbers – IPR2019-00858, IPR2019-00859, IPR2019-00860, IPR2019-00861, IPR2019-00862, and IPR2019-00863. Petitions filed on March 22, 2019.

Case Subject Matter – Wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declarations for post grant and inter partes reviews. Was deposed five times.

DLA Piper (East Palo Alto, CA)

Case – Invensas Corporation and Tessera Advanced Technologies, Inc. v. NVIDIA Corporation

Case Number – Delaware, 1:19-cv-00861. Complaint filed on May 8, 2019.

Case Subject Matter – Reference voltage circuits (programmable bandgaps) having a substantially zero temperature coefficient using bipolar and MOS transistors.

Work Performed – Provided expert consulting services.

Irell & Manella LLP (Los Angeles, CA)

Case – VLSI Technology LLC v. Intel Corporation

Case Number – Texas, WD (Waco) 6:19-cv-00256. Complaint filed on April 11, 2019.

Case Subject Matter – Static Random Access Memory (SRAM) having a variable power supply using charge-sharing capacitors, methods for designing digital systems, and hardware managed interrupt control.

Work Performed – Provided expert consulting services, wrote expert reports, declaration, and was deposed.