

SECOND EDITION
COMPREHENSIVE
DICTIONARY
OF

ELECTRICAL ENGINEERING

EDITOR-IN-CHIEF
Phillip A. Laplante



Taylor & Francis
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bulb generator a free-standing generator contained in a streamlined, waterproof bulb-shaped enclosure and driven by a water-wheel resembling a ship's propeller on a shaft which extends from one end of the enclosure. They are used in tidal power installations. *See* tidal power.

bulk power a term inclusive of the generation and transmission portions of the power system.

bulk scattering scattering at the volume of an inhomogeneous medium, generally also possessing rough boundaries. It is due to inhomogeneities in the refractive index.

bulk substation a substation located on a high-voltage transmission line which supplies bulk power to a non-generating utility.

bulldog an attachment for a wire or hoist.

bump a localized orbit displacement created by vertical or horizontal correction element dipoles used to steer a beam through an available aperture or around obstacles.

bunch a group of particles captured in a phase space bucket.

bundle the practice of paralleling several conductors per phase in an overhead transmission line for the purpose of increasing ampacity and decreasing inductive reactance.

bundle spacer a rigid structure which is used to maintain the spacing of wires in a bundled conductor on an overhead electric power transmission line. *See* bundle.

bundled services utility services which are sold together, like power transmission and distribution services in non-deregulated electric utilities.

buried via a via connected to neither the primary side nor the secondary side of a multilayer packaging and interconnecting structure, i.e., it connects only internal layers.

burndown breakage of an overhead electric power line due to heating from excess current.

burnup a measure (e.g., megawatt-days/ton) of the amount of energy extracted from each unit of fissile material invested in a nuclear reactor.

burn-in component testing where infant mortality failures (defective or weak parts) are screened out by testing at elevated voltages and temperatures for a specified length of time.

burst refresh in DRAM, carrying out all required refresh actions in one continuous sequence—a *burst*. *See also* [distributed refresh](#).

burst transfer the sending of multiple related transmissions across an interconnect, with only one initialization sequence that takes place at the beginning of the burst.

burstiness factor used in traffic description, the ratio of the peak bit rate to the average bit rate.

bus (1) a data path connecting the different subsystems or modules within a computer system. A computer system will usually have more than one bus; each bus will be customized to fit the data transfer needs between the modules that it connects.

(2) a conducting system or supply point, usually of large capacity. May be composed of one or more conductors, which may be wires, cables, or metal bars (busbars).

(3) a node in a power system problem

(4) a heavy conductor, typically used with generating and substation equipment.

bus acquisition the point at which a bus arbiter grants bus access to a specific requester.

to one or more levels of larger buses), used to increase the number of elements that may be connected to a high-performance bus structure.

bus idle the condition that exists when the bus is not in use.

bus impedance matrix See [Z-bus](#).

bus interface unit in modern CPU implementations, the module within the CPU directly responsible for interactions between the CPU and the memory bus.

bus line one of the wires or conductors that constitute a bus. A bus line may be used for data, address, control, or timing.

bus locking the action of retaining control of a bus after an operation which would normally release the bus at completion. In the manipulation of memory locks, a memory read must be followed by a write to the same location with a guarantee of no intervening operation. The bus must be locked from the initial read until after the update write to give an indivisible read/write to memory.

bus master a bus device whose request is granted by the bus controller and thereby gains control of the bus for one or more cycles or transfers. The bus master may always reside with one subsystem, or may be transferred between subsystems, depending on the architecture of the bus control logic. See also [bus controller](#), [bus cycle](#).

bus owner the entity that has exclusive access to a bus at a given time.

bus phase a term applying especially to synchronous buses, controlled by a central clock, with alternating “address” and “data” transfers. A single transfer operation requires the two phases to transfer first the address and then the associated data. Bus arbitration may be overlapped with preceding operations.

bus priority rules for deciding the precedence of devices in having bus requests honored.

Devices issue requests on one of several bus request lines, each with a different bus priority. A high priority request then “wins” over a simultaneous request at a lower priority.

The request grant signals then “daisy chains” through successive devices along the bus or is sent directly to devices in appropriate order. The requesting device closest to the bus controller then accepts the grant and blocks its propagation along the bus.

Buses may have handle interrupts and direct memory accesses with separate priority systems.

bus protocol (1) a set of rules that two parties use to communicate.

(2) the set of rules that define precisely the bus signals that have to be asserted by the master and slave devices in each phase of a bus operation.

bus request an input signal to a processor that requests access to the bus; a hold signal. Competing bus requests are resolved by the bus controller. See also [bus controller](#).

bus slave a device that responds to a request issued by the bus master. See also [bus master](#).

bus snooping the action of monitoring all traffic on a bus, irrespective of the address. Bus snooping is required where there are several caches with the same or overlapping address ranges. Each cache must then “snoop” on the bus to check for writes to addresses it holds; conflicting addresses may be updated or may be purged from the cache.

Bus snooping is also useful as a diagnostic tool.

bus state triggering a data acquisition mode initiated when a specific digital code is selected.

bus tenure the time for which a device has control of the bus, so locking out other requesters. In most buses, the bus priority applies only when a device completes its tenure; even a low priority