

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., LTD.
Petitioner

v.

Optronic Sciences LLC
Patent Owner

Inter Partes Review No. IPR2024-01133

**DECLARATION OF DR. R. JACOB BAKER IN SUPPORT OF
PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE FOR INTER
PARTES REVIEW OF U.S. PATENT NO. 9,263,509**

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I. INTRODUCTION

I, R. Jacob Baker, Ph.D., P.E., declare as follows:

1. My name is R. Jacob Baker. I have been asked by Petitioners BOE Technology Group Co., LTD. to provide my expert opinions in support of the above-identified reply to Patent Owners response for inter partes review of claims 1-13 (“Challenged Claims”) of U.S. Patent No. 9,263,509 (“509 patent,” EX1001), owned by Optronic Sciences LLC (“PO”), pursuant to 35 U.S.C. §§311–19 and 37 C.F.R. §42.100.

2. I currently hold the opinions set forth in this declaration.

3. I am being compensated for my time at the rate of \$765 per hour.

This compensation is not contingent upon my performance, the outcome of this matter, or any issues involved in or related to this matter.

II. DOCUMENTS AND OTHER MATERIALS RELIED UPON

4. In forming the opinions set forth in this declaration, in addition to the documents identified in my July 5, 2024 declaration (which I am informed is EX1003), I have additionally reviewed Patent Owner’s Response, the supporting declaration thereto by Dr. Bretschneider, and his deposition of July 15, 2025 for this matter.

5. Additionally, I have utilized my own experience and expertise, including regarding the knowledge and capabilities of a person of ordinary skill in the relevant art in the timeframe of the claimed priority date of the 509 patent.

III. LEVEL OF ORDINARY SKILL IN THE ART

A. Patent Owner's POSITA Definition Is Flawed

6. Patent Owner asserts a POSITA for the 509 patent “would have at least a Bachelors’ degree in a field of engineering or physics and at least two years of professional experience related to the design and manufacture of LED or OLED pixels for flat panel displays.” In my opinion, this definition is flawed.

7. A bachelor’s degree in (unspecified) engineering incorrectly encompasses engineering fields clearly having nothing to do with displays, such as biomedical, civil, environmental or chemical engineering. A POSITA for the 509 patent would have knowledge in the design of optoelectronic circuits at least at the system level where components such as LEDs and transistors are put together to form a working optoelectronic circuit (i.e., one that converts current flow to generated light). For example, the circuit design and corresponding cross-sectional view of the layout of the pixel as seen in Figs. 1 and 2 of the 509 patent would require circuit design knowledge. This knowledge would be attained by obtaining a degree having a required curriculum of circuit and electronics courses such as Electrical Engineering. This knowledge would not fall within the scope of a

person having knowledge in other fields of engineering such as biomedical, civil, environmental or chemical engineering.

8. Second, separately identifying “design” and “manufacture” is divorced from the reality that design experience with respect to electronic and optoelectronic system design (or LED or OLED pixels for flat panel displays) necessarily involves some manufacturing experience, because designers must design products that can be manufactured. Circuit designers typically work closely with fabs in an iterative manner to test, modify, and finalize product designs for production. This is evidenced by Dr. Bretschneider’s repeated characterization of his experience: “designed and transferred into manufacturing” various products. EX2026 at ¶¶11. Pure manufacturing experience (involving how to set the parameters such as temperature, partial gas pressures, time, etc. of the various machines when developing the process flow, i.e., process steps) is not needed for, nor contemplated by, the 509 patent.

9. Finally, Patent Owner criticizes the definition of POSITA I provided in my previous declaration for not requiring the professional experience to be more focused on the design of LED or OLED pixels for flat panel displays. Yet, the alleged novelty of the 509 patent is not the design of the light emitting portion of the pixel, but rather adding an auxiliary electrode connected to the pixel’s anode (i.e., adding a connected wire), which can be coordinated through parallel

connection to reduce the resistance of the anode. EX1001 at 6:4-9. The problem and solution are common to any electrical circuit, and to any optoelectronic system irrespective of the light emitting mechanism.

10. I do note that none of my opinions would change should the Board adopt Patent Owner's definition of a POSITA.

B. Patent Owner's Criticism of My Expertise is Groundless

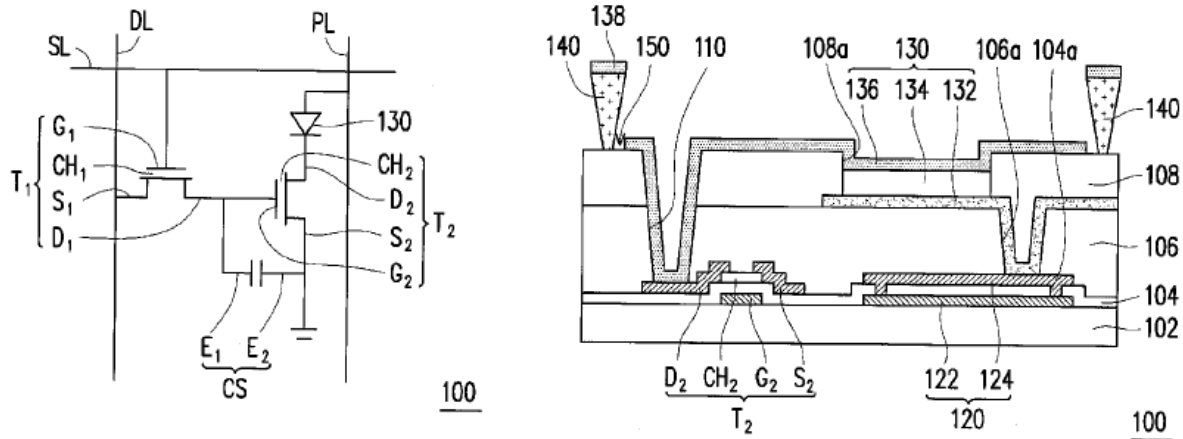
11. Patent owner, and their expert Dr. Bretschneider, opine that I am not a POSITA because: 1) "Petitioner's expert does not have experience in the design and manufacture of LED and OLED displays." POR at 10 and 2) "In my opinion, Dr. Baker has not had the necessary experience working with LEDs and OLEDs for displays." EX2026 at ¶65. I don't feel these are reasonable opinions and therefore disagree.

12. As an initial observation, none of the claims specifically claim a light emitting device that is an LED, OLED, or even "diode." In fact, the terms "diode," "LED," or "OLED" are not found anywhere in the '509 patent's specification. Not claiming the type of light emitting device used is understandable. The '509 patent is about the circuit design and physical layout of a pixel. The 509 patent claims are agnostic to the type of light emitting device the pixel uses, so long as it includes a light emitting layer.

13. While the anode and cathode connections discussed in the 509 patent could correspond to a light emitting diode (LED), including LEDs made using organic materials (OLEDs), these anode/cathode connections could also correspond to other light emitting devices such as those found in field emission displays, see US Patent 5,894,293 (EX1019).

14. Figures 1 and 2 from the information page of the 509 patent are pasted below. These images show the electrical schematic (left) and cross-sectional view of the layout (right) of an embodiment taught in the 509 patent for reducing the resistance of the conductor supplying power to the pixel. As discussed in my original declaration and discussed in more detail below, a POSITA would have understood that by changing the layout, the location, as seen in the cross-sectional view below, of an etching (opening or hole) in the dielectric, where the materials are deposited, the location of transistors and the connections of conductors, transistors and the light emitting device, for example, can be varied to implement the schematic of the pixel. Changes in the fabrication process flow are not required to etch another hole, change the size of the etch, move the location of a material or add a material that is already present in the process flow to an additional location in the physical layout of the pixel. Rather, only changes in the layout are required for the modifications, a least in Ground 2, that I provided in my original declaration. It's my opinion that the patent owner and their expert Dr.

Bretschneider fail to understand this latter point and believe I am suggesting changes to the manufacturing process flow in all Grounds.



15. The 509 patent is concerned with the “pixel structure, including a data line, a scan line, at least one active device, a first auxiliary electrode, and a light emitting device, is provided.” EX1001 at Abstract. The physical location of the scan line, SL, data line, DL, power line, PL, connection to the light emitting device, and transistors are of concern in the 509 patent. These lines are basic to the structure of most flat-panel pixels and are positioned in the physical implementation by changing the layout of the pixel. The point is that changes, such as moving the physical location of the scan line SL, are not accomplished by changing the process flow or fabrication process. The layout of the pixel is changed to change the location of physical implementation of the pixel.

16. Putting aside Patent owner and their expert's clear misunderstandings of what the 509 patent is teaching, and to support my expertise in flat panel display pixel design, my US patent 5,894,293 (EX1019) teaches a pixel design using a "field emitting" (light emitting) device. Figure 5A from this patent, pasted below, has a column line (V_{col} corresponding to the DL line in the pixel from Fig. 1 of the 509 patent), row line (V_{row} corresponding to the SL line in the pixel from Fig. 1 of the 509 patent), and a connection to the light emitting device's tip, 46, which is the cathode of the device. The connection to power for the light emitting device, the anode, is not shown in this pixel schematic but is located, as discussed in this patent, above the dashed lines (grid) at the top of the light emitting device's tip 46 (the cathode of the light emitting device).

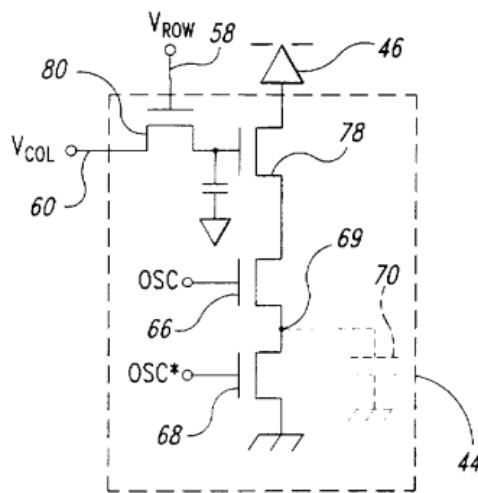


Fig. 5A

17. The flat panel display pixel I designed back in the 1990s, and patented in US Patent 5,894,293, also had additional inputs, labeled OSC and OSC*, to

implement a switched-capacitor resistor. But the basic schematic of the pixel I designed having row, column, and power connections are common to the pixels used in flat panel displays.

C. Dr. Bretschneider is NOT a POSITA

18. In my opinion, Dr. Bretschneider lacks the undergraduate degree of a POSITA for the 509 patent, namely an electrical engineering degree. Dr. Bretschneider degrees are in Chemical Engineering. EX2026, ¶¶25-26. After reviewing Dr. Bretschneider's CV, I see no work experience or supplemental education in the areas of circuit design or circuit layout. The word "circuit" doesn't appear in his CV. Further, I reviewed Dr. Bretschneider's deposition transcript and when, for example, he was questioned about the design of flat panel pixels on pages 47 and 48 of the transcript he indicated that software "could" be used in the circuit design process. At the time of the alleged invention, and well before, software tools were an absolute necessity given the complexity and manufacturing requirements (such as verifying that the layout matches the schematic of a flat panel circuit design). During this same line of questioning when asked what software tools he would use, he indicated "SolidWorks." SolidWorks is a software program for mechanical design. While one might use SolidWorks to design an electrical enclosure, such as a light bulb housing, or an electrical connection, such as a light bulb socket, SolidWorks has no use in an electrical circuit design in a

semiconductor device requiring schematics, layouts, and the verification that a schematic matches a layout. His answers support my opinion that he does not have circuit design knowledge.

19. As I said above, the circuit design and the layout of the pixel as seen in Figs. 1 and 2 of the 509 patent would require circuit design knowledge, something that is provided by a degree in Electrical Engineering or, at least, some work experience in the area of optoelectronic circuit design. This knowledge would not fall within the scope of a person having knowledge in chemical engineering at any level. Simply knowing about the chemical properties used in the layers of the optoelectronic circuit would not be sufficient to understand the circuit design and layout of a pixel. This is especially the case for the 509 patent, where the alleged novelty is one or more auxiliary electrodes electrically connected to the first electrode layer. Therefore, Dr. Bretschneider is not a POSITA and certainly not an expert in the field of circuit design and layout for a flat panel pixel.

IV. CLAIM CONSTRUCTION

20. As stated in my earlier declaration, “auxiliary electrode” should be construed either broadly as “supplemental electrode” or narrowly as “supplemental electrode to reduce the total resistance of the pixel structure.” I applied the broad construction in Grounds 1-5 and the narrow construction in Grounds 1-10.

A. “auxiliary”

21. Patent Owner argues the term “auxiliary” should be afforded its plain and ordinary meaning, which allegedly includes the following negative limitation: “which does not include primary and essential.” POR at 25. In my opinion, this construction is incorrect.

22. I disagree that a POSITA would consider the plain and ordinary meaning of “auxiliary” to have the negative limitation proposed by Patent Owner. I do not find any support for Patent Owner’s construction. The words “primary” and “essential” (and any form of the word “function”) are not found in the 509 patent. Instead, Patent Owner cites to the function of reducing total resistance, an alleged enhancement to the primary and essential functionality of the first electrode layer to provide power to the pixel. POR at 24. I disagree. First, the specification twice disclaims that the invention is limited to this function. Ex. 1001, at 6:4-10 (“However, the invention is not limited thereto.”); 7:52-57 (same). Second, other language cited by the Patent Owner merely says that the auxiliary electrode “can be” coordinated to reduce resistance, leaving Patent Owner reading in limitations from the specification that are unambiguously disclosed as optional. POR at 23. Third, the claims only recite that the first and second auxiliary electrodes are electrically connected to the first electrode layer, with no limitation that such electrical connection be limited to a parallel electrical connection or otherwise

reduce resistance. EX1001 at claims 1 and 10. Fourth, there is nothing in claim 1 that requires the auxiliary electrode reduce the resistance of the first electrode layer, or requires a parallel arrangement that would reduce resistance. Fifth, the 509 patent is silent as to which of the first electrode layer and the auxiliary electrode is physically connected to power. Therefore, in my opinion, it is pure speculation by Patent Owner and its expert to conclude that without the auxiliary electrode, the first electrode layer would still result in an operable pixel. POR at 24.

23. The extrinsic evidence I have reviewed confirms the plain meaning of “auxiliary” is “supplemental” and is not limited to any particular type of supplemental functionality. The Patent Owner argues the auxiliary electrode “is not simply an **additional** electrode,” yet its own dictionary defines “auxiliary” as “**additional**; supplementary; reserve.” Compare POR at 23 to EX2015 at 94. In fact, in that same dictionary, one of the definitions of “supplementary” is “**additional**.” EX1018 at 1345. Even Patent Owner’s expert appears to have admitted the 509 patent merely requires the auxiliary electrode be “**in addition to**” the first and second electrode layers:

Indeed, in the ’509 Patent, the claims require an “auxiliary electrode” **in addition to** a “first electrode layer” and a “second electrode layer.” EX2026, ¶98 (emphasis added).

In my opinion, the Patent Owner's expert appears to confirm my construction is correct.

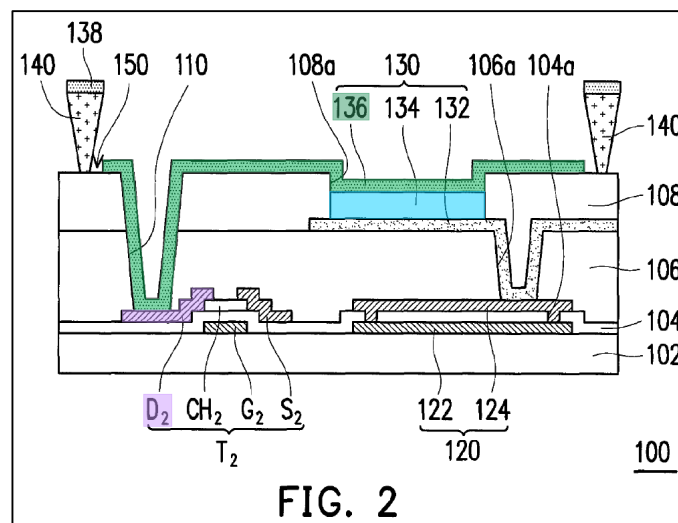
24. Patent Owner and its expert argue that the plain meaning of "auxiliary" and the specification "tell a POSITA that the 'function or characteristic' being supplemented by the 'auxiliary electrode' is the 'function or characteristic' of the first electrode layer." POR at 24. See also EX1017, 72:1-4. Yet, their proposed construction does not mention the first electrode layer, nor does it identify which of its functions or characteristics are being supplemented. I note that at Dr. Bretschneider's deposition, the only function that Patent Owner's expert could identify was reduced resistance. EX1017, 91:20-92:15. Yet, as noted above, the specification twice disclaims that the invention is limited to this function. Ex. 1001, at 6:4-10. In my opinion, the plain and ordinary meaning of "auxiliary" to a POSITA would not be the one proposed by Patent Owner and its expert.

25. In fact, in my opinion, Patent Owner's proposed construction is indefinite. There is nothing in the Patent Owner's proposed construction, or the 509 patent specification, or even anything allegedly known in the art, that would dictate to a POSITA with reasonable certainty what functionalities or characteristics rise to the level of being "primary and essential."

B. “electrode”

26. Patent Owner argues that the term ‘electrode’ should be afforded its plain and ordinary meaning, *which means end structure of a conductor for making electrical contact.*” POR at 25. In my opinion, this construction is incorrect.

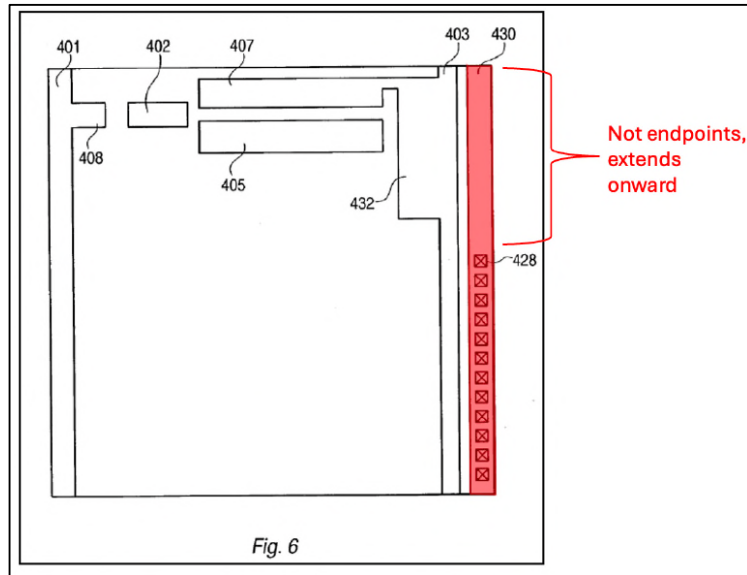
27. The 509 patent uses the term “electrode” for an entire conductor, not just its end structures for making electrical contact. For example, the light emitting device 130 is described as including a “second electrode layer 136” that extends between and electrically connects to the light emitting layer 134 and the drain D₂ of the active device T₂. EX1001, 5:25-36; Fig. 2.



Yet, the entirety of layer 136 is referred to as “second electrode layer.” Id., 5:25-36; Fig. 2. The 509 patent does not refer to only the end structures of layer 136 making electrical contact with drain D₂ and light emitting layer 134 as “electrode

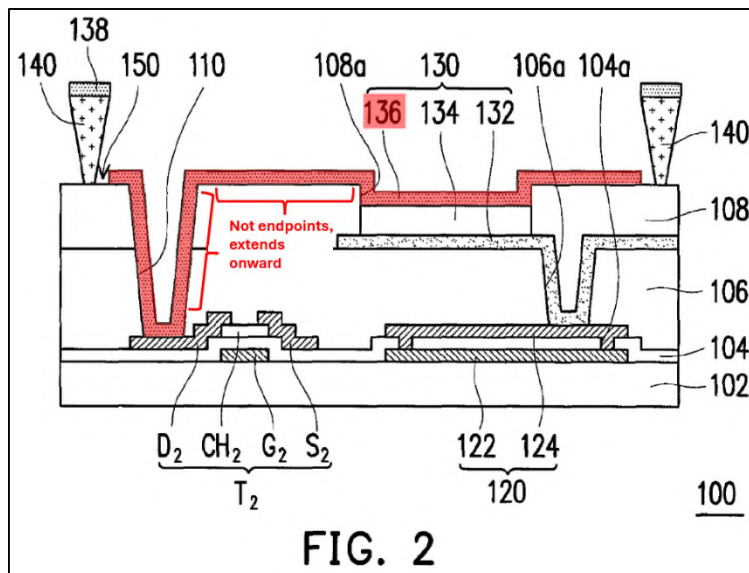
layer,” with a conductor therebetween. The entire conductor that is layer 136 is referred to as “second electrode layer.” Therefore, in my opinion it is wrong to say “‘electrode’ is used as an end point, but not the road to get to an end point.” POR at 26. The 509 patent unambiguously discloses electrode layer 136 as not just including the two points making electrical contact with light emitting layer 134 and drain D₂, but also including the road between those two points. The labeling and description of second electrode layer 136 in the 509 patent directly contradicts Plaintiff’s construction that “electrode” only refers to an end structure of a conductor for making electrical contact.

28. I find that Patent Owner’s arguments under Ground 1 relating to the Weaver reference evidences a remarkable contradiction with its own construction. Patent Owner argued that Weaver’s bus line 430 is not an electrode because it includes far more than just the end structure of a conductor for making electrical contact, illustrated by the following drawing annotated by Patent Owner:



POR at 32.

29. Yet, applying this same argument to the 509 patent embodiments would mean that the “second electrode layer 136” is not an electrode layer (see Fig. 2 of the 509 patent below annotated with Patent Owner’s argument):



30. Therefore, Patent Owner's construction of "electrode" results in "second electrode layer" of claim 1 not reading on any disclosed embodiment of the 509 patent.

31. Patent Owner's construction also fails for the first electrode layer 132, first auxiliary electrode 120 and second auxiliary electrode 460. In each case the entirety of the conductor that is disclosed as layer 132, layer 120 (with both top and bottom electrode layers 122, 124, or single layer 222) and layer 460 is referred to as "electrode layer" or "electrode." Ex. 1001, at 4:5-20 and 35-42; 7:1-16; Figs. 2-6. Nowhere does the 509 patent use the term "electrode" to indicate only the end structure of these conductors. I have not found a single instance where Patent Owner identifies a single conductor disclosed in the 509 patent for which any of the electrodes or electrode layers are an end structure. I also note that in his deposition, Patent Owner's expert, Dr. Bretschneider, could not identify the conductor for which the auxiliary electrode is an end structure. EX1017, 123:19-124:16. I do not believe any such conductors exist in the 509 patent.

32. With respect to the circuit diagram of Fig. 1, the 509 patent makes reference to "an electrode end E1" and "an electrode end E2." 509 patent, 3:26-31. If "electrode" was only an end structure, then the 509 patent would not use the term "electrode end."

33. In my opinion, a POSITA would have understood that the plain and ordinary meaning of electrode is a conductor. This is consistent with dictionaries at the time, such as the Wiley Electrical and Electronics Engineering Dictionary, IEEE Press, 2004, that broadly defines electrode as “A conductor which serves to deliver, receive, collect, emit, deflect, or control electric charge carriers.” Ex. 2012, at p. 237. This definition is consistent with the sole use of the term “electrode” as a conductor in the 509 patent.

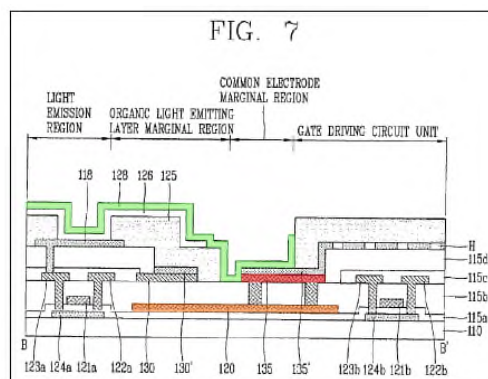
V. PATENT OWNER IS WRONG ON THE MOTIVATIONS OF A POSITA AND WHAT A POSITA WOULD HAVE DONE

34. Patent Owner argues repeatedly that without hindsight, there is no reason to modify Weaver to reduce resistance as proposed (along with what Patent Owner argues as unnecessarily complex extraneous features proposed by Petitioner), as opposed to simply changing the width of the bus line (i.e., a POSITA would simply have made them “a little wider”). POR at 17, 19-20, 34, 41, 48. In my opinion, this argument is simply wrong, as it ignores the basic realities of light emitting displays: there is a constant effort to maximize the number of pixels in the display for high resolution. Reducing the resistance of the conductors supplying power to pixels will reduce the voltage variation between the pixels in the display and thus improve image uniformity.

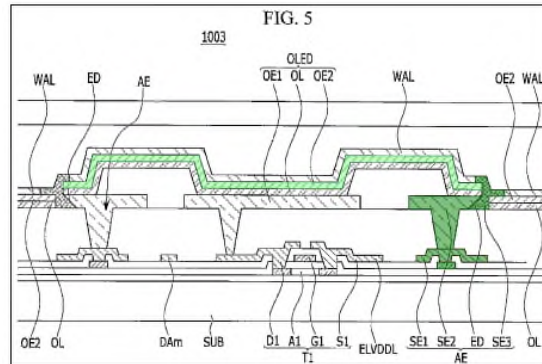
35. A POSITA would have understood that this is desirable and that there is only so much space in and around the pixels to route all the various lines to the

pixels (which often number in the millions). Therefore, the various lines supplying power to a pixel can only be made so wide. A POSITA would have understood that when making the Weaver device, the various lines would already be as wide as they can be while providing the desired density of pixels. The circuit design of a pixel can always benefit from reducing the resistance of the wires powering and supplying signals to the pixel, i.e., decreased pixel resistance, beyond what can be provided by existing possible line widths. Making millions of lines “a little wider” would result in an unwanted reduction in pixel density and resolution (larger area pixels). A POSITA would have understood that by putting wires in parallel, for example stacked on top of each other in full or partially, the pixel resistance can be reduced without reducing pixel density and that this is desirable. Therefore, I disagree that hindsight was used.

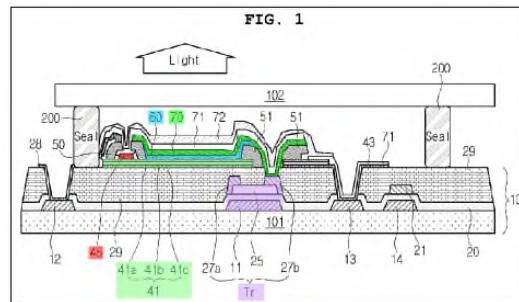
36. This reality of display devices is evidenced by the prior art I have already addressed. Lee053 discloses connecting two electrode layers 120, 135 in parallel.



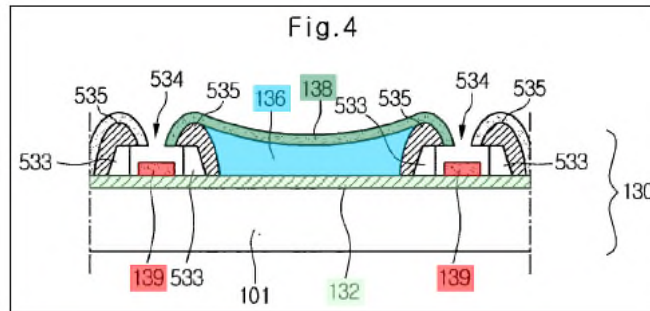
37. Song discloses its auxiliary electrode AE as having four different portions (SE1, SE2, ED, SE3) involving multiple metal layers.



38. Lee149 discloses an electrode pattern 45 in addition to its first electrode 41 that “serves to lower the resistance of the first electrode 41.” EX1011, [0038], Fig. 1.



39. Bae discloses auxiliary electrodes 139 in contact with first electrode 132 which “serves to lower the resistance of first electrode 132.” EX1012, [0059], Fig. 4



40. All of these prior art references evidence the reality of displays: the lines can be made only so wide, and there is a need to lower pixel resistance beyond what available line widths can provide. Yet, according to Patent Owner and its expert, these inventors should never have considered their “unnecessary, complex, extraneous” solutions because they simply should have made the one electrode “a little wider.”

41. The error of Patent Owner’s argument is exposed simply by applying it to the 509 patent itself: there would be no need to add an auxiliary electrode connected to the lower electrode layer to lower pixel resistance given that the lower electrode layer could simply be made “a little wider.” Patent Owner’s argument fails because arguing a POSITA would only consider increasing the widths of various lines is contrary to the realities of display devices and what actually motivates POSITAs in this art.

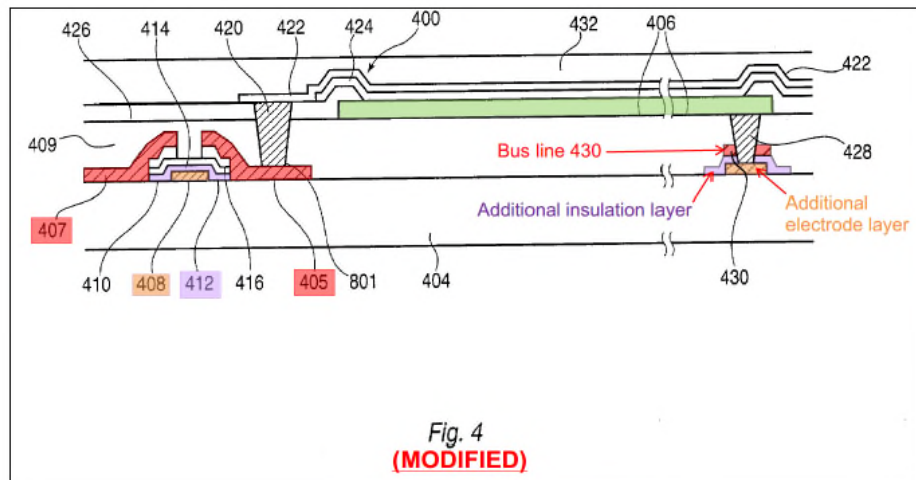
VI. GROUND 2: CLAIMS 6-8 RENDERED OBVIOUS BY WEAVER AND LEE053

42. The construction of “auxiliary electrode” I applied for Ground 2 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

43. Patent Owner and its expert argue that a POSITA would not combine Weaver and Lee053 because it would involve changing the process. POR at 33-35. Specifically, Patent Owner and Dr. Bretschneider argue that I testified the process cannot be changed, and then argue my opinions require a process change.

44. Patent Owner and its expert fail to understand that what I am discussing in my combination for Ground 2 is that the *layout* of the pixel be modified by forming the red annotated “Bus line 430” seen below from my original declaration, Ex. 1003 ¶130 using the same material/layer as used to form the source/drain regions 405/407 of the transistor also annotated in red. In other words, a POSITA would draw boxes *in the layout* of the pixel for the red annotated “Bus line 430” in the desired locations (on the right and left sides of Weaver’s metal plug in via 428 seen in the cross-sectional view below) on the source/drain layer 405/407. Adding these boxes to the layout can be done without modifying the fabrication process steps. As discussed above and in my original declaration, a POSITA would have known that reducing the pixel resistance is

desirable in Weaver and would have looked to the teachings of Lee053 to stack, and connect, layers towards this goal.



45. I also point to EX2026 ¶131 to support my opinion that Patent Owner and its expert do not understand the difference between process changes and changes in the layout of a circuit. Changing the **thickness** of a layer, in a process flow, is a process change that the circuit designer implementing the layout of a pixel may have no control over. The **thickness** of a layer used in the fabrication of a display, for example, may be related to the amount of time a deposition (of a material) process step is run while fabricating the display. Changing the lithography of existing layers to provide additional components from the same layers is a layout change that a POSITA would have been able to perform without changing the process. A POSITA would have been able to add a box, or boxes, in a layout on a specific layer following the layout design rules.

46. While modifications to Weaver that do require a change to the process could be obvious, I didn't need to render that opinion because the point I was making in my testimony for Ground 2 is that the modifications to Weaver could be made without a process change making them even more obvious than if a change in the process were also needed, and I supported my opinion that there is a motivation to combine these references. [See my original declaration, ¶¶126-131].

47. In my original declaration, I set forth how the modifications to the Weaver device to incorporate the teachings of Lee053 could be implemented *using the “same layers” already formed in the Weaver device*:

“130. Modified Fig. 4 of Weaver below shows an example of such a straightforward implementation, with the additional electrode layer added as part of the **same layer of conductive material** used to form gate 408, the additional insulation layer is added **as part of the insulation layer 412** (i.e., as part of the SiNx layer described in [0024] and shown as layer 412 of the transistor 410 in Fig. 4), and bus line 430 formed **as part of the same layer of conductive material used to form source/drain regions 405/407** on top of insulation layer 412, where the additional electrode layer and the bus line 430 are electrically connected, and the bus line 430 and anode 406 are electrically connected. This implementation would provide for an efficient manufacturing process flow.” EX1003, ¶130; Pet. at 33-34.

Therefore, Patent Owner is simply wrong that process changes are necessary.

48. Finally, Patent Owner argues that there is no reason to modify Weaver if changing the width of the bus line alone would accomplish the same thing. POR at 34. This argument fails as discussed above because there is a limit on the layout

size of the pixel. Increasing the width of bus line is limited to the allowable size of the pixel. See §V.

VII. GROUND 3: CLAIMS 6-8 RENDERED OBVIOUS BY WEAVER AND SONG

49. The construction of “auxiliary electrode” I applied for Ground 3 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

50. Patent Owner argues that the combination of Weaver and either Lee053 or Song would not result in the same modification to Weaver without hindsight mapping due to the differences between Song and Lee053. POR at 36-38. I disagree because Song and Lee053 both teach the well-known technique of forming electrodes having multiple interconnected electrode layers. Lee teaches second power wiring 135 interconnected with dummy wiring 120. Song teaches an auxiliary electrode AE with different portions SE1, SE2 and SE3 formed as different layers. Therefore, these general teachings would result in the same modification to Weaver.

51. Patent Owner repeats its argument that a POSITA would not make the proposed modification to Weaver and Song because it involves changing the process. POR at 38-39. That argument is wrong for the same reasons it fails for Weaver combined with Lee053. See §VI.

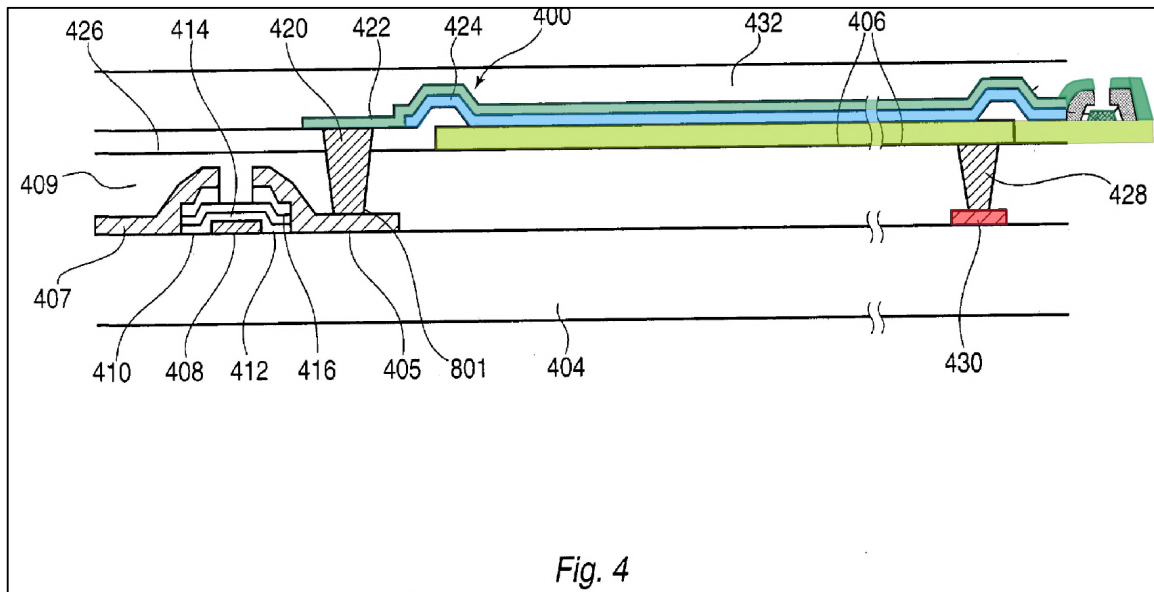
VIII. GROUND 4: CLAIMS 10-11 RENDERED OBVIOUS BY WEAVER AND LEE149

52. The construction of “auxiliary electrode” I applied for Ground 4 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

53. Patent Owner faults me for lacking an illustration of the resulting combination. POR at 39. I don’t believe that criticism is well founded. I described in detail precisely how I believe the obvious modification would be implemented:

“183. The modification to Weaver could be implemented, for example, by forming a contact window with an undercut (similar to that of Lee’s buffer layer 50) over the anode 406 before forming the cathode 422, so that when the conductive layer for cathode 422 is formed, it would result in a first portion of the conductive layer as the cathode 422 of OLED 400 and a separate second portion of the conductive layer in the contact window as the second auxiliary electrode at a side of the OLED 400.” EX1003, ¶183

The simplicity of the modification can be understood by the above description (i.e., literally form Lee149’s buffer layer 50 with its contact window on anode 406 of Weaver, so a portion of layer 422 is separately formed in the contact window). A simple copy and paste could suffice, as illustrated below.



This description sets forth exactly how the modification is implemented, including both the method of formation and the resulting structure (i.e., segregating a portion of the cathode layer to serve as the second auxiliary electrode as taught by Lee149).

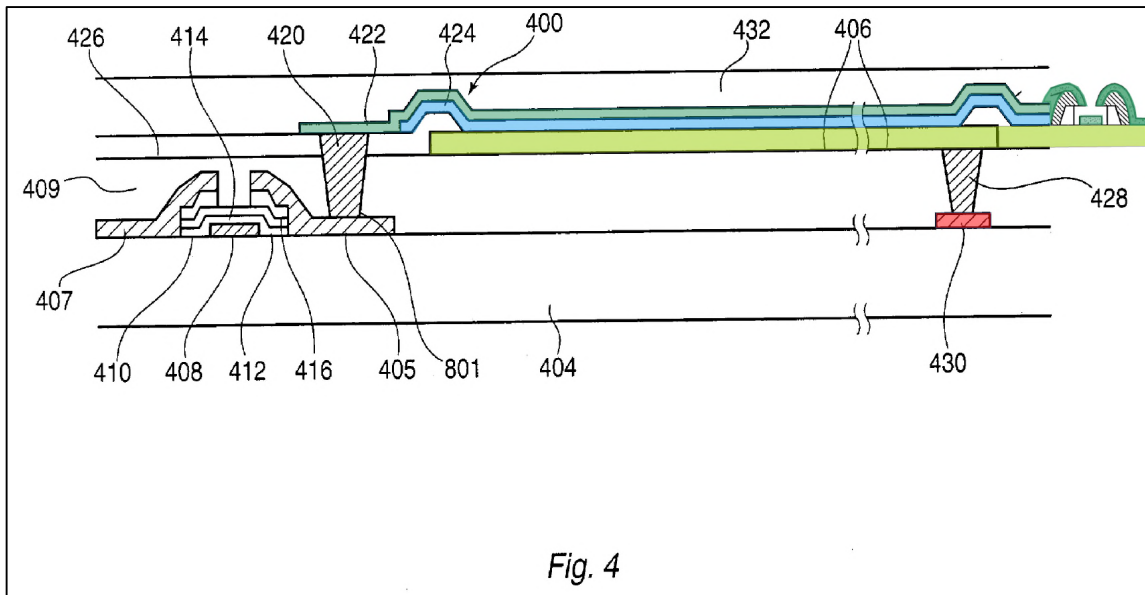
IX. GROUND 5: CLAIMS 10-11 RENDERED OBVIOUS BY WEAVER AND BAE

54. The construction of “auxiliary electrode” I applied for Ground 5 is “supplemental electrode” and “supplemental electrode to reduce the total resistance of the pixel structure.”

55. Patent Owner faults me for lacking an illustration of the resulting combination. POR at 43. I don’t believe that criticism is well founded. I described in detail precisely how I believe the obvious modification would be implemented:

“202. The modification to Weaver could be implemented, for example, by forming a contact window with an undercut (similar to that of Bae’s buffer layer 535) over the anode 406 before forming the cathode 422, so that when the conductive layer for cathode 422 is formed, it would result in a first portion of the conductive layer as the cathode 422 of OLED 400 and a separate second portion of the conductive layer in the contact window as the second auxiliary electrode at a side of the OLED 400.” EX1003, ¶202.

The simplicity of the modification can be understood by the above description (i.e., literally form Bae’s buffer layer 535 with its contact window on anode 406 of Weaver, so a portion of layer 422 is separately formed in the contact window). A simple copy and paste could suffice, as illustrated below.



This description sets forth exactly how the modification is implemented, including both the method of formation and the resulting structure (i.e., segregating a portion of the cathode layer to serve as the second auxiliary electrode as taught by Bae).

X. GROUND 6: CLAIMS 1-5, 9, 12-13 RENDERED OBVIOUS BY WEAVER IN VIEW OF GUPTA OR HAN

56. Patent Owner argues Han is not analogous art because its OLED devices are larger than the pixels in a display. In my opinion, this is incorrect. The problems with OLEDs (high resistance of their anodes and cathodes causing unwanted IR drop) and solutions (adding electrodes in parallel to and pixel's anodes and cathodes) exist at any size. In fact, Han expressly discloses this:

“Hereinafter, construction and operation of each of the subsidiary electrodes 750, 760, and 770 will be described in detail.
0033. Each of the first and third subsidiary electrodes 750 and 770 may be electrically connected in parallel to the anode 720 in the emission region and function to reduce the influence of IR-drop due to a driving current. That is, the first and third subsidiary electrodes 750 and 770 may supply additional power to the anode 720 and reduce the influence of IR-drop.” EX1010, ¶[0033]

Therefore, in my opinion, Han is analogous art to the 509 patent. It addresses the same problems identified in the 509 patent.

57. Patent Owner also misrepresents the teachings of Gupta, and specifically appears to exploit Gupta's choice of words for resistor 238, arguing that a resistor is not an electrode. POR at 52-53. I believe this argument has no

merit. An electrode is simply a conductor. See §IV.B. Gupta states resistor 238 may be formed of a conductive mesh or strip, and connected to the anode in parallel to reduce sheet resistance. Pet. at 73, EX1009 at 7:42-43 and 4:55-60. In my opinion, Gupta referring to the element 238 as a resistor merely acknowledges that any conductive mesh or strip has a resistance associated with it. Patent Owner's expert admitted this in his deposition, and admitted that Gupta's conductive strip is a conductor. EX1017, 184:15-186:2.

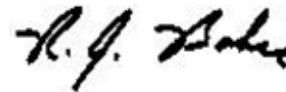
58. Patent Owner argues that Gupta teaches that resistor 238 is a mesh, and that in no way suggests that Weaver's bus line should be put in parallel with Weaver's anodes. In my opinion, the Patent Owner is wrong. First, Gupta expressly discloses: "The resistor 238 may be formed of a conductive mesh *or strip*." EX1009 at 7:42-43 (emphasis added). A strip of conductive material is a conductor, and therefore an electrode. Second, even if Gupta only disclosed a mesh configuration (which it does not), that mesh configuration is connected "in parallel with the cathode sheet resistance 234A, such that the total resistance between cathode 238 and node 240 is reduced." EX1009 at 7:39-42. This parallel connection is precisely the obvious modification that is proposed for Weaver.

59. I am informed that in the related district court litigation, the Court issued a preliminary construction at the July 23, 2025 claim construction hearing for "auxiliary electrode" as "electrode that works in unison with another

electrode.” EX1021, p.3. If the Board were to adopt this construction, it would not change any of my opinions. Regarding Grounds 1-10 (first auxiliary electrode), Weaver’s bus line 430 meets this construction because it is an electrode that is electrically connected to, and therefore works in unison with, another electrode, namely anode 406. Regarding Grounds 4-5 (second auxiliary electrode), the resulting second portion of the conductive layer formed in the contact window is an electrode that is electrically connected to, and therefore works in unison with, another electrode, namely anode 406.

60. I hereby declare under penalty of perjury under the laws of the United States of America that the following is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code.

July 30, 2025
Date



Dr. R. Jacob Baker