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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/842,879	03/15/2013	Andreas Bibl	026057.24379U1

CONFIRMATION NO. 7403

150365
Apple Inc. / Rutan & Tucker, LLP
611 Anton Boulevard, Suite 1400
COSTA MESA, CA 92626

POA ACCEPTANCE LETTER

OC000000097485782

Date Mailed: 02/20/2018

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/12/2018.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtdinh/

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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/842,879	03/15/2013	Andreas Bibl	9299.P24379US1

CONFIRMATION NO. 7403

45217
WOMBLE BOND DICKINSON (US) LLP/ APPLE INC.
Attn: IP Docketing
P.O. Box 7037
Atlanta, GA 30357-0037

POWER OF ATTORNEY NOTICE

OC000000097485778

Date Mailed: 02/20/2018

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/12/2018.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtdinh/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	13/842,879
Filing Date	03-15-2013
First Named Inventor	Andreas Bibl
Title	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
Art Unit	2823
Examiner Name	NGUYEN, KHIEM D
Attorney Docket Number	026057.24379U1

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jacob Aikin/	Date (Optional)	February 12, 2018
Name	Jacob T. Aikin	Registration Number	62787
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Apple Inc.

Application No./Patent No.: 8,791,474 Filed/Issue Date: 07-29-2014

Titled: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

Apple Inc., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: INVENTORS To: LUXVUE TECHNOLOGY CORPORATION

   The document was recorded in the United States Patent and Trademark Office at

   Reel 030036, Frame 0089, or for which a copy thereof is attached.

2. From: LUXVUE TECHNOLOGY CORPORATION To: APPLE INC.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 038521, Frame 0255, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jacob T. Aikin/	February 12, 2018
Signature	Date
Jacob T. Aikin	62,787
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 150365

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒ The address associated with Customer Number: 150365

OR

☐	Firm or Individual Name			
	Address			
	City		State	Zip
	Country			
	Telephone		Email	

Assignee Name and Address: Apple Inc.
1 Infinite Loop
Cupertino, CA 95014

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	Aug. 14 2017
Name	BJ Watrous	Telephone	1-408-862-5229
Title	Vice President and Chief IP Counsel		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	31762208
Application Number:	13842879
International Application Number:	
Confirmation Number:	7403
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Customer Number:	45217
Filer:	Jacob T. Aikin/Loretta Sandoval
Filer Authorized By:	Jacob T. Aikin
Attorney Docket Number:	9299.P24379US1
Receipt Date:	12-FEB-2018
Filing Date:	15-MAR-2013
Time Stamp:	13:07:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	P24379U1_POA_TRANSMITTAL_2018.pdf	143787 633fa884d81d6737b5090cdbf7407c956c1ec9dc	no	1
Warnings:					

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	P24379U1_POA_373_2018.pdf	119681 d6b628fe741dbac3a5a1db1a26776b9147aad581	no	3
Warnings:					
Information:					
3	Power of Attorney	P24379U1_POA.pdf	1406350 dfcf305b45ab7c424c11f73c84eaf9fc47545bb7	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	1669818	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
13/842,879	8791474	2823	6433

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 45217 on 10/28/2015 via Private PAIR in view of the certification copied below that authorized the change.

- Correspondence Address

The address for Customer Number 45217 is:
45217
APPLE INC./BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/Jacob Aikin/
Name:	Jacob T. Aikin
Registration Number:	62787

PTO/SB/47 (03-09)
Approved for use through 03/31/2012. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 00197

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
8,791,474	13/842,879

Completed by (check one):

☐ Applicant/Inventor — /Jacob Aikin/ (Signature)

☑ Attorney or Agent of record 62,787 (Reg. No.) — Jacob T. Aikin (Typed or printed name)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) — 408-720-8300 (Requester's telephone number)

☐ Assignee recorded at Reel _____ Frame_____ — August 12, 2014 (Date)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ *** Total of _____forms are submitted.**

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	19841668
Application Number:	13842879
International Application Number:	
Confirmation Number:	7403
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Customer Number:	8791
Filer:	Jacob T. Aikin/Betty Scaletta
Filer Authorized By:	Jacob T. Aikin
Attorney Docket Number:	9299P027
Receipt Date:	12-AUG-2014
Filing Date:	15-MAR-2013
Time Stamp:	15:48:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Maintenance Fee Address Change	9299P24379US1_FeeAddress_081214.pdf	312518 87b27b5637a45400ee92118b9cb18c66b8dbd035	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	312518

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/842,879	07/29/2014	8791474	9299P027	7403

8791 7590 07/09/2014

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Andreas Bibl, Los Altos, CA;
Kapil V. Sakariya, Sunnyvale, CA;
Charles R. Griggs, San Jose, CA;
James Michael Perkins, Mountain View, CA;
LUXVUE TECHNOLOGY CORPORATION, Santa Clara, CA

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	3	**of**	7	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
			Number-Kind Code[2] (If known)			
/KN/		US-	2003/0010975	01-16-2003	Gibb et al.	
		US-	2003/0177633 A1	09-25-2003	Haji et al.	
		US-	2006/0160276	07-20-2006	Brown et al.	
		US-	2006/0214299	09-28-2006	Fairchild et al.	
		US-	2007/0166851	07-19-2007	Tran et al.	
		US-	2007/0194330	08-23-2007	Ibbetson et al.	
		US-	2008/0163481	07-10-2008	Shida et al.	
		US-	2009/0068774	03-12-2009	Slater et al.	
		US-	2009/0146303	06-11-2009	Kwon, Jinsu	
		US-	2009/0303713	12-10-2009	Chang et al.	
		US-	2009/0314991 A1	12-24-2009	Cho et al.	
Change(s) applied to document, /RF/ 5/6/2014		US-	~~2010/00248484~~	09-30-2010	Bower, Christopher; et al.	20100248484
		US-	2010/0188794 A1	07-29-2010	Park et al.	
		US-	2010/0203661	08-12-2010	Hodota, Takashi	
		US-	2010/0276726	11-04-2010	Cho et al.	
		US-	2011/0003410 A1	01-06-2011	Tsay et al.	
		US-	2011/0151602	06-23-2011	Speier, Ingo	
		US-	2012/0064642	03-15-2012	Huang et al.	
		US-	7,160,633 B2	01-09-2007	Tai et al.	
		US-	7,482,696 B2	~~07-27-2009~~	Shei et al.	January 27, 2009
Change(s) applied to document, /RF/ 5/7/2014		US-	2003/0017360 A1	01-23-2003	Tai et al.	
		US-	2005/0274959 A1	12-15-2005	Kim et al.	
		US-	2010/0051910 A1	03-04-2010	Choi	
		US-	6,911,666 B2	06-28-2005	Voutsas	
		US-	7,795,804 B2	09-14-2010	Kim	
/KN/		US-	8,049,410 B2	11-01-2011	Suh et al.	

Examiner Signature	/Khiem Nguyen/	Date Considered	09/11/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KN/

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	~~2874~~ 2823
				Examiner Name	~~Not yet assigned~~ K. Nguyen
Sheet	1	**of**	1	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/KN/		US-	2012/0134065 A1	05-31-2012	Furuya et al.	
/KN/		US-	2013/0126081 A1	~~03-23-2013~~	Hu et al.	May 23, 2013
/KN/		US-	2013/0126891 A1	~~03-23-2013~~	Bibl et al.	May 23, 2013
		US-				
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		US-				
		US-				

Change(s) applied to document, /RF/ 5/7/2014

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	/Khiem Nguyen/	Date Considered	09/11/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/842,879	03/15/2013	Andreas Bibl	9299P027	7403

7590 06/27/2014

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
06/27/2014	PAPER

NOTICE OF NON-COMPLIANT INFORMATION DISCLOSURE STATEMENT

An Information Disclosure Statement (IDS) filed 06-18-14 in the above-identified application fails to meet the requirements of 37 CFR 1.97(d) for the reason(s) specified below. Accordingly, the IDS will be placed in the file, but the information referred to therein has not been considered.

The IDS is not compliant with 37 CFR 1.97(d) because:

☒ The IDS lacks a statement as specified in 37 CFR 1.97(e).

☐ The IDS lacks the fee set forth in 37 CFR 1.17(p).

☐ The IDS was filed after the issue fee was paid. Applicant may wish to consider filing a petition to withdraw the application from issue under 37 CFR 1.313(c) to have the IDS considered. See MPEP 1308.

Hung Gezhegn for

571-272-4200 or 1-888-786-0101
Application Assistance Unit
Office of Data Management

FORM PTOM327-B (Rev. 02/08)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

8791 7590 04/08/2014
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Betty Scaletta	(Depositor's name)
Betty Scaletta	(Signature)
June 18, 2014	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/842,879	03/15/2013	Andreas Bibl	9299P027	7403

TITLE OF INVENTION: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	07/08/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, KHIEM D	2823	257-089000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Blakely Sokoloff Taylor & Zafman LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: LuxVue Technology Corporation
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Santa Clara, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

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☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 02-2666 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date June 18, 2014
Typed or printed name Jacob T. Aikin Registration No. 62,787

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

IPR2024-01134 - BOE
Exhibit 1009 - Page 19

Electronic Patent Application Fee Transmittal

Application Number:	13842879
Filing Date:	15-Mar-2013
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Filer:	Jacob T. Aikin
Attorney Docket Number:	9299P027

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	19343774
Application Number:	13842879
International Application Number:	
Confirmation Number:	7403
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Customer Number:	8791
Filer:	Jacob T. Aikin/Betty Scaletta
Filer Authorized By:	Jacob T. Aikin
Attorney Docket Number:	9299P027
Receipt Date:	18-JUN-2014
Filing Date:	15-MAR-2013
Time Stamp:	19:16:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$960
RAM confirmation Number	5772
Deposit Account	022666
Authorized User	
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Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	9299P027_IDS_LTR_06-18-14.pdf	15440 b543e562efde23245a149e2f1e027d6e31fb24c1	no	1
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	9299P027_IDS_SB08_06-18-14.pdf	51729 a313e00769add8331d092e3ebb30b4a03acfe2ae	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Issue Fee Payment (PTO-85B)	9299P027_IssueFeeTrans_06-18-14.PDF	82705 b291ad94d8b6f09fc7d12d6b2587e018e8bbce5e	no	1
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30585 c69fa5e3eec092792a71a8cb2db0a723f8fc0045	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	180459		

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<u>National Stage of an International Application under 35 U.S.C. 371</u>
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<u>New International Application Filed with the USPTO as a Receiving Office</u>
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Docket No: 9299P027 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	)	
	)	Examiner: Nguyen, Khiem D.
Andreas Bibl	)	
	)	Art Unit: 2823
Application No.: 13/842,879	)	
	)	
Filing Date: March 15, 2013	)	Confirmation No.: 7403
	)	
For: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. Applicants respectfully request that the Examiner make these references part of the official record in this application.

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge Deposit Account No. 02-2666 for any fee which may be required.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: June 18, 2014

/Jacob Aikin/
Jacob T. Aikin
Reg. No. 62,787

1279 Oakmead Parkway
Sunnyvale, CA 94085
(408) 720-8300

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06-18-2014.
Date of Deposit

/Betty Scaletta/
Betty Scaletta

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2823
				Examiner Name	Nguyen, Khiem D.
Sheet	1	**of**	1	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	2014/0084482 A1	03-27-2014	Hu et al.	
		US-				
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

8791 7590 04/08/2014

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/08/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/842,879	03/15/2013	Andreas Bibl	9299P027	7403

TITLE OF INVENTION: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	07/08/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

IPR2024-01134 - BOE
Exhibit 1009 - Page 26

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

8791 7590 04/08/2014
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

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13/842,879	03/15/2013	Andreas Bibl	9299P027	7403

TITLE OF INVENTION: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	07/08/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, KHIEM D	2823	257-089000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

IPR2024-01134 - BOE
Exhibit 1009 - Page 27

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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8791 7590 04/08/2014

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	13/842,879	BIBL ET AL.	
	Examiner	Art Unit	
	KHIEM D. NGUYEN	2823	

All participants (applicant, applicant's representative, PTO personnel):

(1) *KHIEM D. NGUYEN*. (3)_____.

(2) *MR. JACOB AIKIN*. (4)_____.

Date of Interview: *02 April 2014*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1,24 and 26*.

Identification of prior art discussed: *N/A*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Mr. Jacob Aikin, attorney for applicants, has confirmed/authorized changes in the claims as shown in the Examiner's Amendment. In addition, it is not necessary for Applicants to provide a separate record of the substance of the interview, since the interview resulted in the allowance of the application .

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/KHIEM D NGUYEN/ Primary Examiner, Art Unit 2823	04/02/2014

Notice of Allowability	Application No. 13/842,879	Applicant(s) BIBL ET AL.	
	Examiner KHIEM D. NGUYEN	Art Unit 2823	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment filed on March 10th, 2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-23,25 and 27-29*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   Certified copies:
   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20140402* .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/KHIEM D NGUYEN/ Primary Examiner, Art Unit 2823	04/02/2014

The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

   Authorization for this Examiner's Amendment was given in a telephone interview with Mr. Jacob Aikin on April 02nd, 2014.

2. The application has been amended as follows:

   In the claims:

   Please cancel claims 24 and 26.

   Please change claim 1 to --A display panel with redundancy scheme comprising: a display substrate including a pixel area and a non-pixel area, wherein the pixel area includes an array of subpixels and a corresponding array of bottom electrodes within the array of subpixels; an array of redundant micro LED device pairs bonded to the array of bottom electrodes, wherein each subpixel includes a bottom electrode and a redundant micro LED device pair bonded to the bottom electrode, and each redundant micro LED device pair within a respective subpixel is designed to emit a same primary color emission; and one or more top electrode layers in electrical contact with the array of redundant micro LED device pairs; wherein the array of redundant micro LED

device pairs comprises a first array of redundant micro LED device pairs, a second array of redundant micro LED device pairs, and a third array of redundant micro LED device pairs, wherein the first, second, and third arrays of redundant micro LED device pairs are designed to emit different primary color emissions.--.

Please change claim 25 to --The display panel of claim 1, wherein the first array of redundant micro LED device pairs is designed to emit a red primary color emission, the second array of redundant micro LED device pairs is designed to emit a green primary color emission, and the third array of emitting redundant micro LED device pairs is designed to emit a blue primary color emission.--.

Please change claim 27 to --The display panel of claim 1, wherein each micro LED device is bonded to a bottom electrode with an electrically conductive bonding layer directly between the micro LED device and the bottom electrode.--.

Allowable Subject Matter

3. Claim 1-23, 25, and 27-29 are allowed over prior art of record.

Reasons For Allowance

4. The following is an examiner's statement of reasons for allowance:

After further search and consideration of Applicants' response filed on March 10th, 2014 (see Applicants' argument in page 8, line 1 to page 11, line 15), it is determined that the prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art of record does not teach or suggest "each redundant micro LED device pair within a respective subpixel is

designed to emit a same primary color emission…wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs, a second array of redundant micro LED device pairs, and a third array of redundant micro LED device pairs, wherein the first, second, and third arrays of redundant micro LED device pairs are designed to emit different primary color emissions", as recited in independent claim 1.

Claim 2-23, 25, and 27-29 are also allowed as being directly or indirectly dependent of the allowed independent base claim.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KHIEM D NGUYEN/

Primary Examiner, Art Unit 2823

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	13/842,879	BIBL ET AL.	
	Examiner	Art Unit	
	KHIEM D. NGUYEN	2823	

All participants (applicant, applicant's representative, PTO personnel):

(1) *KHIEM D. NGUYEN*. (3)_____.

(2) *MR. JACOB AIKIN*. (4)_____.

Date of Interview: *02 April 2014*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1,24 and 26*.

Identification of prior art discussed: *N/A*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Mr. Jacob Aikin, attorney for applicants, has confirmed/authorized changes in the claims as shown in the Examiner's Amendment. In addition, it is not necessary for Applicants to provide a separate record of the substance of the interview, since the interview resulted in the allowance of the application .

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/KHIEM D NGUYEN/ Primary Examiner, Art Unit 2823	04/02/2014

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	Art Unit
	KHIEM D NGUYEN	2823

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/162, H01L31/173, H01L31/1884, H01L31/1896, H01L33/00, H01L33/42	9/12/2013	/KN/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	88,89,99,100,E33.001	9/12/2013	/KN/
438	22,28,30,34,38,42,44	9/12/2013	/KN/
257	89, 100	4/2/2014	/KN/
349	192	4/2/2014	/KN/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST text searched (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB), see attached search history.	9/11/2013	/KN/
EAST text searched (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB), see attached search history.	1/28/2014	/KN/
EAST text searched (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB), see attached search history.	4/2/2014	/KN/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Claims interference searched (US-PGPUB; USPAT; UPAD), see attached search history.	4/2/2014	/KN/

	/KHIEM D NGUYEN/ Primary Examiner.Art Unit 2823

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	**Art Unit**
	KHIEM D NGUYEN	2823

CPC		
Symbol	**Type**	**Version**

CPC Combination Sets				
Symbol	**Type**	**Set**	**Ranking**	**Version**

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	27	
/KHIEM D NGUYEN/ Primary Examiner.Art Unit 2823	04/02/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6C

U.S. Patent and Trademark Office — Part of Paper No. 20140402

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	**Art Unit**
	KHIEM D NGUYEN	2823

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
257	89	H	0	1	L	29 / 20 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	100				
349	192				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	27	
/KHIEM D NGUYEN/ Primary Examiner.Art Unit 2823	04/02/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6C

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	**Art Unit**
	KHIEM D NGUYEN	2823

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
5	5	21	21												
6	6	22	22												
7	7	23	23												
8	8		24												
9	9	24	25												
10	10		26												
11	11	25	27												
12	12	26	28												
13	13	27	29												
14	14														
15	15														
16	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 27	
/KHIEM D NGUYEN/ Primary Examiner.Art Unit 2823 (Primary Examiner)	04/02/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6C

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2280	(257/89).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/04/02 18:06
L2	3075	(257/100).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/04/02 18:07
L3	673	(349/192).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/04/02 18:07
L4	5857	1 or 2 or 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 18:08
L6	116	4 and (subpixel or sub-pixel) and ((coupl$4 or pair) and (LED or light-emitting-device or light-emitting-diode or light-emitting-element or (light near emitting near (diode or device or element))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 18:09
L7	10	("5041326" | "5693962" | "5736754" | "5962970").PN. OR ("6627332").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/02 18:34
L8	22	(Luxvue near Technology near Corporation).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 18:39
L9	1447	(Andreas near Bibl).in. or (Kapil near2 Sakariya).in. or (Charles near2 Griggs).in. or (James near2 Perkins).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 18:39
L10	1447	8 or 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/04/02 18:40

			IBM_TDB			
L11	2	10 and display and (subpixel or sub-pixel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 18:40
L12	1438	(display near panel) and ((subpixel or sub-pixel) near8 (pair or coupl$4)) and (RGB or (red near8 green near8 blue))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 18:58
L13	116	12 and (redundant or redundancy)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 18:58
L14	69	13 and electrode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/04/02 18:58

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L15	2	((subpixel or sub-pixel) and (pair or coupl$4) and (LED or light-emitting-device or light-emitting-diode or light-emitting-element or (light near emitting near (diode or device or element))) and (bottom near electrode) and (top near electrode)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/02 19:27

4/2/2014 7:28:59 PM
C:\Users\knguyen20\Documents\EAST\Workspaces\13842879.wsp

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BIB DATA SHEET

CONFIRMATION NO. 7403

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/842,879	03/15/2013 RULE	257	2823	9299P027

APPLICANTS
LUXVUE TECHNOLOGY CORPORATION, Santa Clara, CA

INVENTORS
Andreas Bibl, Los Altos, CA;
Kapil V. Sakariya, Sunnyvale, CA;
Charles R. Griggs, San Jose, CA;
James Michael Perkins, Mountain View, CA;

** CONTINUING DATA ********** None /KN/

** FOREIGN APPLICATIONS ********** None /KN/

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
05/18/2013

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /KHIEM D NGUYEN/ Examiner's Signature	☐ Met after Allowance /KN/ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	30	27 ~~20~~	1

ADDRESS
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
UNITED STATES

TITLE
LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

FILING FEE RECEIVED		
2280	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Attorney's Docket No.: 9299P027 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Examiner: Nguyen, Khiem D.
Andreas Bibl	Art Unit: 2823
Application No.: 13/842,879	Confirmation No.: 7403
Filed: March 15, 2013	**AMENDMENT UNDER 37 C.F.R. § 1.116 EXPEDITED PROCEDURE EXAMINING GROUP 2823**
For: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME	

Filed via EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE TO FINAL OFFICE ACTION

Sir:

This is in response to the Final Office Action mailed February 3, 2014. Applicants respectfully request the Examiner to enter this Amendment and consider the following remarks.

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office via electronic filing through the United States Patent and Trademark Electronic Filing System on:

03-10-2014
Date of Deposit

/Betty Scaletta/
Betty Scaletta

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	Art Unit
	KHIEM D NGUYEN	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/12/2013	01/29/2014	04/02/2014						
1	1	✓	✓	=						
2	2	✓	✓	=						
3	3	✓	✓	=						
4	4	✓	✓	=						
5	5	✓	✓	=						
6	6	✓	✓	=						
7	7	✓	✓	=						
8	8	✓	✓	=						
9	9	✓	✓	=						
10	10	✓	✓	=						
11	11	✓	✓	=						
12	12	✓	✓	=						
13	13	✓	✓	=						
14	14	✓	✓	=						
15	15	✓	✓	=						
16	16	✓	✓	=						
17	17	✓	✓	=						
18	18	✓	✓	=						
19	19	✓	✓	=						
20	20	✓	✓	=						
21	21		✓	=						
22	22		✓	=						
23	23		✓	=						
	24		✓	-						
24	25		✓	=						
	26		✓	-						
25	27		✓	=						
26	28		✓	=						
27	29		✓	=						

Attorney's Docket No.: 9299P027 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Examiner: Nguyen, Khiem D.
Andreas Bibl	Art Unit: 2823
Application No.: 13/842,879	Confirmation No.: 7403
Filed: March 15, 2013	**AMENDMENT UNDER 37 C.F.R. § 1.116 EXPEDITED PROCEDURE**
For: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME	**EXAMINING GROUP 2823**

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03-10-2014
Date of Deposit

/Betty Scaletta/
Betty Scaletta

IN THE CLAIMS

Please amend the following claims.

1. (Previously presented) A display panel with redundancy scheme comprising:

a display substrate including a pixel area and a non-pixel area, wherein the pixel area includes an array of subpixels and a corresponding array of bottom electrodes within the array of subpixels;

an array of redundant micro LED device pairs bonded to the array of bottom electrodes, wherein each subpixel includes a bottom electrode and a redundant micro LED device pair bonded to the bottom electrode, and each redundant micro LED device pair within a respective subpixel is designed to emit a same primary color emission; and

one or more top electrode layers in electrical contact with the array of redundant micro LED device pairs.

2. (Original) The display panel of claim 1, wherein each micro LED device is formed of a semiconductor material.

3. (Original) The display panel of claim 2, wherein each micro LED device has a maximum width of 1 to 100 μm.

4. (Original) The display panel of claim 2, wherein the display substrate is a thin film transistor substrate.

5. (Original) The display panel of claim 4, further comprising a ground line in the non-pixel area of the thin film transistor substrate, wherein the one or more top electrode layers are electrically connected to the ground line.

IPR2024-01134 - BOE
Exhibit 1009 - Page 47

6. (Currently amended) The display panel of claim 5, wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a redundant micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the redundant micro LED device pair to the ground line.

7. (Original) The display panel of claim 2, further comprising an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip.

8. (Original) The display panel of claim 7, wherein each micro controller chip is connected to a scan driver circuit and a data driver circuit.

9. (Original) The display panel of claim 8, further comprising a ground line in the non-pixel area of the display substrate, wherein the one or more top electrode layers are electrically connected to the ground line.

10. (Currently amended) The display panel of claim 9, wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a redundant micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the redundant micro LED device pair to the ground line.

11. (Currently amended) The display panel of claim 2, further comprising:

IPR2024-01134 - BOE
Exhibit 1009 - Page 48

a plurality of micro LED device irregularities within the array of redundant micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and

a passivation layer material covering the plurality of irregularities.

12. (Currently amended) The display panel of claim 11, wherein the one or more top electrode layers do not make electrical contact with the plurality of irregularities.

13. (Currently amended) The display panel of claim 12, wherein the one or more top electrode layers are formed directly over the plurality of irregularities.

14. (Currently amended) The display panel of claim [[13]]12, wherein the one or more top electrode layers are not formed directly over the plurality of irregularities.

15. (Original) The display panel of claim 12, wherein the plurality of micro LED device irregularities are missing micro LED devices.

16. (Original) The display panel of claim 15, further comprising an array of bonding layers on the array of bottom electrodes corresponding to the plurality of missing micro LED devices, wherein the passivation layer material covers the array of bonding layers.

17. (Original) The display panel of claim 12, wherein the plurality of micro LED device irregularities are defective micro LED devices and the passivation layer material covers the defective micro LED devices.

18. (Original) The display panel of claim 12, wherein the plurality of micro LED device irregularities are contaminated micro LED devices and the passivation layer material covers the contaminated micro LED devices.

19. (Previously presented) The display panel of claim 11, wherein the passivation layer material covers sidewalls of the array of redundant micro LED device pairs.

20. (Original) The display panel of claim 11, further comprising a repair micro LED device bonded to one of the bottom electrodes including one of the micro LED device irregularities.

21. (Previously presented) The display panel of claim 4, wherein each subpixel and corresponding redundant micro LED device pair bonded to a corresponding bottom electrode is independently addressable by the thin film transistor substrate.

22. (Previously presented) The display panel of claim 7, wherein each subpixel and corresponding redundant micro LED device pair bonded to a corresponding bottom electrode is independently addressable by a micro controller chip.

23. (Previously presented) The display panel of claim 22, wherein each micro controller chip is bonded to the display substrate within the pixel area, and the each micro controller chip is connected to a scan driver circuit and a data driver circuit that is not bonded to the display substrate within the pixel area.

24. (Previously presented) The display panel of claim 1, wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs, a

second array of redundant micro LED device pairs, and a third array of redundant micro LED device pairs, wherein the first, second, and third arrays of redundant micro LED device pairs are designed to emit different primary color emissions.

25. (Previously presented) The display panel of claim 24, wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs designed to emit a red primary color emission, a second array of redundant micro LED device pairs designed to emit a green primary color emission, and a third array of emitting redundant micro LED device pairs designed to emit a blue primary color emission.

26. (Previously presented) The display panel of claim 1, wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs and a second array of redundant micro LED device pairs, wherein the first and second arrays of redundant micro LED device pairs are designed to emit different primary color emissions.

27. (Previously presented) The display panel of claim 24, wherein each micro LED device is bonded to a bottom electrode with an electrically conductive bonding layer directly between the micro LED device and the bottom electrode.

28. (Previously presented) The display panel of claim 27, wherein the electrically conductive bonding layer comprises a solder material.

29. (Previously presented) The display panel of claim 11, wherein the display substrate is a thin film transistor substrate.

REMARKS

The enclosed is responsive to the Final Office Action mailed on February 3, 2014. By way of the present response claims 6 and 10-14 have been amended. No claims have been canceled. No new claims have been added. Applicants respectfully request reconsideration of the present application and the allowance of all claims now presented.

Claim Objections

The Examiner has objected to claim 13 for omission of the claim dependency. Applicants thank the Examiner for pointing out the informality. Appropriate correction has been made.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 1-6, 21 and 24-28 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over *Tomoda et al.* (U.S. Publication No. 2005/0176190), *Kim* (U.S. Publication No. 2007/0063644) and *Matthies et al.,* (U.S. Publication No. 2005/0078104).

It is respectfully submitted that the cited references do not disclose or suggest each and every feature of independent claim 1, and that one of ordinary skill in the art would not have been motivated upon review of the cited references to arrive at the invention taught and claimed in independent claim 1.

Independent claim 1 recites a display panel with redundancy scheme comprising, *inter alia*, "an array of redundant micro LED device pairs bonded to the array of bottom electrodes, wherein each subpixel includes a bottom electrode and a redundant micro LED device pair bonded to the bottom electrode, and each redundant micro LED device pair within a respective subpixel is designed to emit a same primary color emission."

Tomoda et al. describes a display device including a red light emitting diode 74 (see paragraph [0130]) and a blue light emitting diode 52 (see paragraph [0106]) bonded to a substrate 71 including a wiring layer 72 using adhesives 73, 65. It is respectfully submitted, that *Tomoda et al.* is unconcerned with and does not disclose a redundancy scheme as recited in amended independent claim 1.

Kim describes a selective deposition method for an organic light emitting diode (OLED) display, where charged materials are selectively deposited into the R, G, and B subpixels. It is respectfully submitted that *Kim* does not remedy the deficiencies of *Tomoda et al.* described above.

Matthies et al. describes a tiled electronic OLED display structure. As illustrated in Fig. 8B, the structure may include a RGBG pixel arrangement. As described in paragraph [0128] "This structure is known as a quad sub-pixel structure. This structure uses two green sub-pixels because more of the luminance information in a color display is in the green pixels than is in either of the red or blue pixels" (emphasis by Applicants). Importantly, the two green sub-pixels are separate, discrete sub-pixels. **They are not the same sub-pixel**. Furthermore, it is Applicants' understanding that the two green sub-pixels additionally include **separate, discrete bottom electrodes**.

Therefore, it is respectfully submitted that the cited references do not disclose or suggest, and are completely unconcerned with LED redundancy within sub-pixels including "an array of redundant micro LED device pairs bonded to the array of bottom electrodes, wherein each subpixel includes a bottom electrode and a redundant micro LED device pair bonded to the bottom electrode, and each redundant micro LED device pair within a respective subpixel is designed to emit a same primary color emission" as recited in independent claim 1.

Applicants thus respectfully submit that claim 1, and claims 2-6, 21, and 24-28 which depend directly or indirectly upon claim 1 are patentable over *Tomoda et al.* in view of *Kim* and *Matthies et al.*, and request that the rejection under 35 U.S.C. §103(a) be withdrawn.

With regard to claims 24-26, the Examiner again points to paragraph [0128] of *Matthies et al.* as allegedly disclosing the disclosed feature of multiple arrays of redundant (red, green, and blue emitting) LED device pairs. However, as described above, *Matthies et al.* does not disclose, and is completely unconcerned with LED redundancy ***within sub-pixels***. Furthermore, *Matthies et al.* only describes pixel arrangements in which certain sub-pixels within a pixel can emit the same color to increase brightness of that color relative to the other colors. In the example described in paragraph [0128], the display emits more green light than red or blue light.

Accordingly, not only is *Matthies et al.* unconcerned with LED redundancy ***within sub-pixels***, *Matthies et al.* does not disclose or suggest LED redundancy for different primary color emissions (claims 24, 26) or for both red, green, and blue emitting LED device pairs (claim 25). To the contrary, *Matthies et al.* advocates inclusion of more sub-pixels of one color (e.g. green) compared to other colors (e.g. red, blue).

Applicants thus respectfully submit that in addition to the reasons discussed above with regard to claim 1, that claims 24-26 are patentable over *Tomoda et al.* in view of *Kim* and *Matthies et al.*, and request that the rejections under 35 U.S.C. §103(a) be withdrawn.

The Examiner has rejected claims 7-10, 22, and 23 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over *Tomoda et al.*, *Kim* and *Matthies et al., and Kwak* (U.S. Publication No. 2005/0243039).

Kwak describes a display panel 100 and a data driver 400, scan driver 200, and emit controller 300 coupled to the display panel 100 outside of a pixel area of the display panel. See Fig. 2. In no part does *Kwak* describe an array of micro controller chips bonded to the display substrate. As shown in Fig. 2, chips 200, 300, 400 are located off of the display panel 100. Accordingly, the cited references do not disclose or suggest each and every feature of claim 7. Claims 8-10, 22, and 23 are directly or indirectly dependent upon claim 7 and are patentable for at least the same reasons.

With regard to claim 8, in no part does *Kwak* describe an array of micro controller chips connected to the data driver 400 and scan driver 200.

Applicants thus respectfully submit that claims 7-10, 22, and 23 are patentable over *Tomoda et al.* in view of *Kim* and *Kwak*, and request that the rejection under 35 U.S.C. §103(a) be withdrawn.

The Examiner has rejected claims 11-20 and 29 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over *Tomoda et al., Kim, Matthies et al.,* and *Tran et al.* (U.S. Publication No. 2006/0154390).

Tran et al. describes using laser ablation to destroy defective LEDs so that only good LEDs are packaged. However, *Tran et al.* is unconcerned with, and does not disclose or suggest a redundancy scheme as recited in claim 11. *Tran et al.* does not advocate manners for managing micro LED device irregularities in a display panel. To the contrary, *Tran et al.* advocates destroying unpackaged defective LEDs so that they are not packaged. See paragraph [0009]. In view of this, one of ordinary skill in the art would not have been motivated upon review of *Tran et al.* to arrive at the features of claims 11-20 and 29 because *Tran et al.* advocates destroying defective LEDs before being packaged.

Applicants thus respectfully submit that claims 11-20 are patentable over *Tomoda et al.* in view of *Kim* and *Tran et al.* and request that the rejection under 35 U.S.C. §103(a) be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 1-10 and 21-28 stand rejected under pre-AIA 35 U.S.C. § 102(e) as being anticipated by *Hu et al.,* (U.S. Publication No. 2013/0285086).

As described in paragraph [0099] and Fig. 15 of *Hu et al.*, a plurality of micro LEDs may be placed on driver contacts 410 and arranged into pixel groups (e.g. R,G,B). As illustrated in Fig. 15, each micro LED is placed onto a separate driver contact 410. *Hu et al.* does not describe or illustrate a driver contact 410 including a redundant pair of micro LEDs bonded to it. Therefore, *Hu et al.* does not disclose each and every feature of independent claim 1.

Accordingly, Applicants respectfully submit that claim 1, and claims 2-10 and 21-28 which depend on it, are patentable over *Hu et al.,* and request that the rejection under 35 U.S.C. §102(e) be withdrawn.

IPR2024-01134 - BOE
Exhibit 1009 - Page 56

Pursuant to 37 C.F.R. § 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. §§ 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: March 10, 2014

/Jacob Aikin/
Jacob T. Aikin
Reg. No. 62,787

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300

Electronic Acknowledgement Receipt	
EFS ID:	18419575
Application Number:	13842879
International Application Number:	
Confirmation Number:	7403
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Customer Number:	8791
Filer:	Jacob T. Aikin/Betty Scaletta
Filer Authorized By:	Jacob T. Aikin
Attorney Docket Number:	9299P027
Receipt Date:	10-MAR-2014
Filing Date:	15-MAR-2013
Time Stamp:	15:42:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		9299P027_AF_03-10-14.pdf	77578 35b42cae4ad60f83bf5927f724209ea14707 33c0	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	12
Warnings:			
Information:			
	Total Files Size (in bytes):	77578	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/842,879	Filing Date 03/15/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/10/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 29	Minus	** 29	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ANITA JOHNSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/842,879	03/15/2013	Andreas Bibl	9299P027	7403

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
02/03/2014	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/842,879	Applicant(s) BIBL ET AL.	
	Examiner KHIEM D. NGUYEN	Art Unit 2823	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/16/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-29* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-29* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *12/16/2013*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Remarks

1. The Amendment filed on December 16th, 2013 is acknowledged. By this amendment, claims 1, 6, 10, 11, and 19 have been amended. Claims 21-29 are newly added. Accordingly, claims 1-29 are pending in this application in which claim 1 is in independent form. Newly submitted IDS filed on December 16th, 2013 has been considered.

Claim Objections

2. Claim 13 is objected to because of the following informalities: In claim 13, Applicants removed "13" to overcome the dependency issue but the Applicants had not provided to which claim does claim 13 depends to.

   Claim 13 recites the limitation "the plurality of irregularities" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 11 recited “the plurality of irregularities”. Therefore, it appears that claim 13 should be dependent on claim 11.

   Appropriate correction is required.

New Grounds of Rejection

Claim Rejections - 35 USC § 103

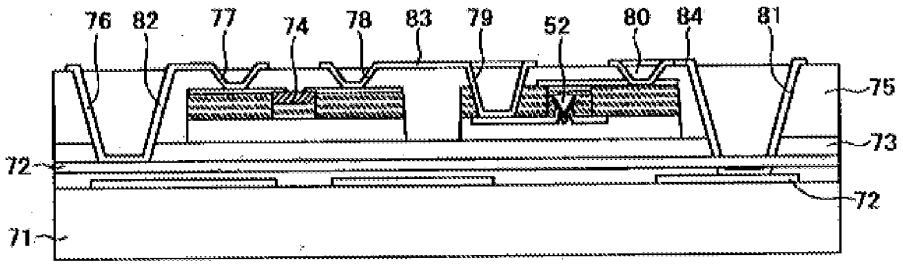
3. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 21, and 24-28 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomoda et al. (U.S. Pub. 2005/0176190) in view of Kim (U.S. Pub. 2007/0063644), both of record, and Matthies et al. (U.S. Pub. 2005/0078104), newly cited.

In re claim 1, Tomoda discloses a display panel with redundancy scheme comprising: a display substrate including a pixel area, wherein the pixel area includes an array of subpixels and a corresponding array of bottom electrodes 72 within the array of subpixels (see paragraph [0129] and FIG. 38); an array of redundant micro LED device pairs 52, 74, bonded to the array of bottom electrodes72 (via adhesive material 73), wherein each subpixel includes a bottom electrode and a redundant micro LED device pair bonded to the bottom electrode 72; and one or more top electrode layers82, 83, 84 in electrical contact with the array of redundant micro LED device pairs 52, 74 (see paragraph [0132] and FIG. 38).

FIG. 38



Tomoda is silent with respect to that the display substrate including a pixel area and a non-pixel area.

However, Kim discloses a display panel including inter-alia, the display substrate having a pixel area and a non-pixel area (see paragraph [0045] and claim 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of Applicants' claimed invention was made to modify Tomoda reference with the feature as taught by Kim to enable the display substrate including a pixel area and a non-pixel area in Tomoda to be formed because it is well-known in the art for the display substrate to include a pixel area and a non-pixel area so that conductive line can be formed in the non-pixel area. Furthermore, it would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention. *KSR*

International Co. v. Teleflex Inc. (KSR), 550 U.S. 398 (2007). "If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill." *Id.*

Furthermore, Tomoda does not specifically disclose that each redundant micro LED device pair within a respective subpixel is designed to emit a same primary color emission.

However, Matthies discloses a display panel including, inter-alia, that each redundant micro LED device pair (830, 836) within a respective subpixel is designed to emit a same primary color emission (green) (see paragraph [0128] and FIG. 8B).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of Applicants' claimed invention was made to modify Tomoda reference with the feature as taught by Matthies in order to enable each redundant micro LED device pair within a respective subpixel is designed to emit a same primary color emission in Tomoda to be formed because in doing so the two green sub-pixels allows for a brighter display (see paragraph [0128] of Matthies). Furthermore, it would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention. *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. 398 (2007). "If a technique has been used to improve one device, and a person of ordinary skill in the

art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill." *Id.*

In re claim 2, as applied to claim 1 above, Tomoda in combination with Kim and Matthies discloses wherein each micro LED device is formed of a semiconductor material (see paragraph [0122] of Tomoda).

In re claim 3, as applied to claim 2 above, Tomoda in combination with Kim and Matthies discloses wherein each micro LED device has a maximum width of 1 to 100 μm (20μm) (see paragraph [0108] of Tomoda).

Furthermore, it is respectfully submitted that there is no evidence indicating the size of each micro LED device is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990); In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966); In re Aller, 220 F.2d 454, 456, 105 USPQ 233,235 (CCPA 1955).

In re claim 4, as applied to claim 2 above, Tomoda in combination with Kim and Matthies discloses wherein the display substrate is a thin film transistor substrate (see paragraph [0096] of Tomoda and paragraph [0062] of Kim).

In re claim 5, as applied to claim 4 above, Tomoda in combination with Kim and Matthies discloses wherein the display panel further comprising a ground line in the non-pixel area of the thin film transistor substrate, wherein the one or more top electrode layers are electrically connected to the ground line (see paragraph [0045] and claim 1 of Kim).

In re claim 6, as applied to claim 5 above, Tomoda in combination with Kim and Matthies discloses wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a redundant micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the redundant micro LED device pair to the ground line (see paragraphs [0132] of Tomoda and paragraph [0045] of Kim).

In re claim 21, as applied to claim 4 above, Tomoda in combination with Kim and Matthies discloses wherein each subpixel and corresponding redundant micro LED device pair bonded to a corresponding bottom electrode is independently addressable by the thin film transistor substrate (see paragraph [0100] of Tomoda).

In re claim 24, as applied to claim 1 above, Tomoda in combination with Kim and Matthies discloses wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs, a second array of redundant micro LED device pairs, and a third array of redundant micro LED device pairs, wherein the first, second, and third arrays of redundant micro LED device

pairs are designed to emit different primary color emissions (red, green, blue) (see paragraph [0128] of Matthies).

In re claim 25, as applied to claim 24 above, Tomoda in combination with Kim and Matthies discloses wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs designed to emit a red primary color emission, a second array of redundant micro LED device pairs designed to emit a green primary color emission, and a third array of emitting redundant micro LED device pairs designed to emit a blue primary color emission (RGB) (see paragraph [0128] of Matthies).

In re claim 26, as applied to claim 1 above, Tomoda in combination with Kim and Matthies discloses wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs and a second array of redundant micro LED device pairs, wherein the first and second arrays of redundant micro LED device pairs are designed to emit different primary color emissions (see paragraph [0128] of Matthies).

In re claim 27, as applied to claim 24 above, Tomoda in combination with Kim and Matthies discloses wherein each micro LED device is bonded to a bottom electrode with an electrically conductive bonding layer directly between the micro LED device and the bottom electrode (see paragraph [0129] of Tomoda).

In re claim 28, as applied to claim 27 above, Tomoda in combination with Kim and Matthies discloses wherein the electrically conductive bonding layer comprises a solder material (see paragraph [0128] of Matthies).

5. Claims 7-10, 22, and 23 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomoda et al. (U.S. Pub. 2005/0176190) in view of Kim (U.S. Pub. 2007/0063644) and Matthies et al. (U.S. Pub. 2005/0078104) as applied to claim 2 above, and further in view of Kwak (U.S. Pub. 2005/0243039).

In re claims 7 and 8, as applied to claim 2 paragraph 4 above, Tomoda and Kim does not specifically disclose wherein the display panel further comprising an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip wherein each micro controller chip is connected to a scan driver circuit and a data driver circuit.

However, Kwak discloses a display panel including, inter-alia, an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip wherein each micro controller chip is connected to a scan driver circuit 200 and a data driver circuit 400.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of Applicants' claimed invention was made to modify Tomoda reference with the feature as taught by Kwak to enable an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip wherein each micro controller chip is connected to a scan driver circuit and a data driver circuit in Tomoda to be formed. Furthermore, it would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements

as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention. *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. 398 (2007). "If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill." *Id.*

In re claim 9, as applied to claim 8 above, Tomoda in combination with Kim, Matthies, and Kwak discloses wherein the display panel further comprising a ground line in the non-pixel area of the display substrate, wherein the one or more top electrode layers are electrically connected to the ground line (see paragraph [0045] and claim 1 of Kim).

In re claim 10, as applied to claim 9 above, Tomoda in combination with Kim, Matthies, and Kwak discloses wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a redundant micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the redundant micro LED device pair to the ground line (see paragraphs [0132] of Tomoda and paragraph [0045] of Kim).

In re claim 22, as applied to claim 7 above, Tomoda in combination with Kim, Matthies, and Kwak discloses wherein each subpixel and corresponding redundant

micro LED device pair bonded to a corresponding bottom electrode is independently addressable by a micro controller chip (see paragraph [0100] of Tomoda).

In re claim 23, as applied to claim 22 above, Tomoda in combination with Kim, Matthies, and Kwak discloses wherein each micro controller chip is bonded to the display substrate within the pixel area, and the each micro controller chip is connected to a scan driver circuit and a data driver circuit that is not bonded to the display substrate within the pixel area (see paragraph [0133] of Tomoda).

6. Claims 11-20 and 29 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomoda et al. (U.S. Pub. 2005/0176190) in view of Kim (U.S. Pub. 2007/0063644) and Matthies et al. (U.S. Pub. 2005/0078104) as applied to claim 2 above, and further in view of Tran et al. (U.S. Pub. 2006/0154390).

In re claim 11, as applied to claim 2 paragraph 4 above, Tomoda does not specifically disclose wherein the display further comprising: a plurality of micro LED device irregularities within the array of redundant micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and a passivation layer material covering the plurality of irregularities.

However, Tran discloses a display panel including, inter-alia, a plurality of micro LED device irregularities within the array of redundant micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and a

passivation layer material covering the plurality of irregularities (see paragraphs [0004], [0030]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of Applicants' claimed invention was made to modify Tomoda reference with the feature as taught by Tran to enable a plurality of micro LED device irregularities within the array of micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and a passivation layer material covering the plurality of irregularities in Tomoda to be formed because in doing so LEDs array can be evaluate for defects and repair. Furthermore, it would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention. *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. 398 (2007). “If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person’s skill.” *Id.*

In re claim 12, as applied to claim 11 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the one or more top electrode layers do not make electrical contact with the plurality of irregularities (see paragraph [0132] of Tomoda).

In re claim 13, as applied to claim 11 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the one or more top electrode layers are formed directly over the plurality of irregularities (see paragraph [0132] of Tomoda).

In re claim 14, as applied to claim 13 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the one or more top electrode layers are not formed directly over the plurality of irregularities (see paragraph [0132] of Tomoda).

In re claim 15, as applied to claim 12 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the plurality of micro LED device irregularities are missing micro LED devices (see paragraph [0010] of Tran).

In re claim 16, as applied to claim 15 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the display panel further comprising an array of bonding layers on the array of bottom electrodes corresponding to the plurality of missing micro LED devices, wherein the passivation layer material covers the array of bonding layers (see paragraph [0010] of Tran).

In re claim 17, as applied to claim 12 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the plurality of micro LED device irregularities are defective micro LED devices and the passivation layer material covers the defective micro LED devices (see paragraph [0010] of Tran).

In re claim 18, as applied to claim 12 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the plurality of micro LED device

irregularities are contaminated micro LED devices and the passivation layer material covers the contaminated micro LED devices (see paragraph [0004] of Tran).

In re claim 19, as applied to claim 11 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the passivation layer material covers sidewalls of the array of redundant micro LED device pairs (see paragraph [0025] of Tran).

In re claim 20, as applied to claim 11 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the display panel further comprising a repair micro LED device bonded to one of the bottom electrodes including one of the micro LED device irregularities (see paragraph [0004] of Tran).

In re claim 29, as applied to claim 11 above, Tomoda in combination with Kim, Matthies, and Tran discloses wherein the display substrate is a thin film transistor substrate (see paragraph [0100] of Tomoda).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-10 and 21-28 are rejected under pre-AIA 35 U.S.C. 102(e) as being anticipated by Hu et al. (U.S. Pub. 2013/0285086).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under pre-AIA 35 U.S.C. 102(e). This rejection under pre-AIA 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131(a).

In re claim 1, Hu discloses a display panel with redundancy scheme comprising: a display substrate including a pixel area and a non-pixel area, wherein the pixel area includes an array of subpixels and a corresponding array of bottom electrodes 410 within the array of subpixels; an array of redundant micro LED device pairs 150 bonded to the array of bottom electrodes 410, wherein each subpixel includes a bottom electrode 410 and a redundant micro LED device pair 150 bonded to the bottom electrode 410, and each redundant micro LED device pair 150 within a respective subpixel is designed to emit a same primary color emission: and one or more top electrode layers 420 in electrical contact with the array of redundant micro LED device pairs 150 (see paragraph [0099] and FIG. 15).

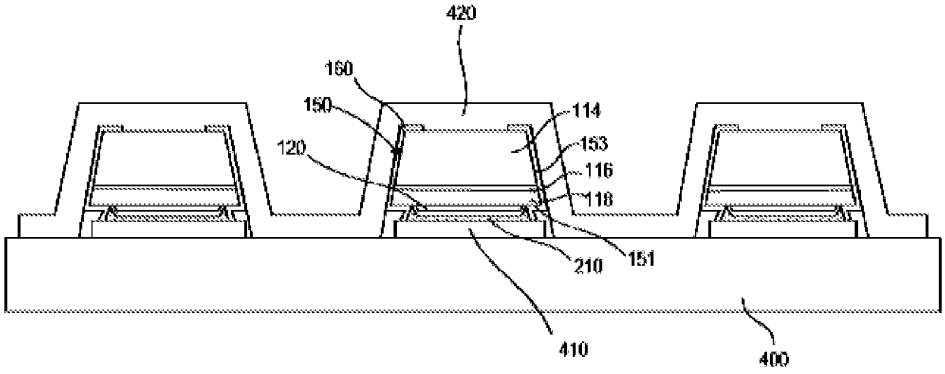


FIG. 15

In re claim 2, as applied to claim 1 above, Hu discloses wherein each micro LED device 150 is formed of a semiconductor material (see paragraph [0099]).

In re claim 3, as applied to claim 2 above, Hu discloses wherein each micro LED device has a maximum width of 1 to 100 μm (10 μm) (see paragraph [0099]).

In re claim 4, as applied to claim 2 above, Hu discloses wherein the display substrate is a thin film transistor substrate (see paragraph [0099]).

In re claim 5, as applied to claim 4 above, Hu discloses wherein the display panel further comprising a ground line in the non- pixel area of the thin film transistor substrate, wherein the one or more top electrode layers are electrically connected to the ground line (see paragraph [0113]).

In re claim 6, as applied to claim 5 above, Hu discloses wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a redundant micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro

LED device of the redundant micro LED device pair to the ground line (see paragraph [0113]).

In re claim 7, as applied to claim 2 above, Hu discloses wherein the display panel further comprising an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip (see paragraph [0099]).

In re claim 8, as applied to claim 7 above, Hu discloses wherein the display panel further comprising each micro controller chip is connected to a scan driver circuit and a data driver circuit (see paragraph [0099]).

In re claim 9, as applied to claim 8 above, Hu discloses wherein the display panel further comprising a ground line in the non- pixel area of the display substrate, wherein the one or more top electrode layers are electrically connected to the ground line (see paragraph [0113]).

In re claim 10, as applied to claim 9 above, Hu discloses wherein the display panel further comprising wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a redundant micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the redundant micro LED device pair to the ground line (see paragraph [0113]).

In re claim 21, as applied to claim 4 above, Hu discloses wherein the display panel further comprising wherein each subpixel and corresponding redundant micro

LED device pair bonded to a corresponding bottom electrode is independently addressable by the thin film transistor substrate (see paragraph [0099]).

In re claim 22, as applied to claim 7 above, Hu discloses wherein the display panel further comprising wherein each subpixel and corresponding redundant micro LED device pair bonded to a corresponding bottom electrode is independently addressable by a micro controller chip (see paragraph [0099]).

In re claim 23, as applied to claim 22 above, Hu discloses wherein the display panel further comprising wherein each micro controller chip is bonded to the display substrate within the pixel area, and the each micro controller chip is connected to a scan driver circuit and a data driver circuit that is not bonded to the display substrate within the pixel area (see paragraph [0099]).

In re claim 24, as applied to claim 1 above, Hu discloses wherein the display panel further comprising wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs, a second array of redundant micro LED device pairs, and a third array of redundant micro LED device pairs, wherein the first, second, and third arrays of redundant micro LED device pairs are designed to emit different primary color emissions (see paragraph [0099]).

In re claim 25, as applied to claim 24 above, Hu discloses wherein the display panel further comprising wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs designed to emit a red primary color emission, a second array of redundant micro LED device pairs designed to emit a green primary color emission, and a third array of emitting

redundant micro LED device pairs designed to emit a blue primary color emission (see paragraph [0099]).

In re claim 26, as applied to claim 1 above, Hu discloses wherein the display panel further comprising wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs and a second array of redundant micro LED device pairs, wherein the first and second arrays of redundant micro LED device pairs are designed to emit different primary color emissions (see paragraph [0099]).

In re claim 27, as applied to claim 24 above, Hu discloses wherein the display panel further comprising wherein each micro LED device 150 is bonded to a bottom electrode 410 with an electrically conductive bonding layer 210 directly between the micro LED device 150 and the bottom electrode 410 (see paragraph [0119] and FIG. 15).

In re claim 28, as applied to claim 27 above, Hu discloses wherein the display panel further comprising wherein the electrically conductive bonding layer 210 comprises a solder material (see paragraph [0119]).

Response to Applicants' Amendment and Arguments

9. Applicants' arguments with respect to claims 1-29 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Conclusion

10. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KHIEM D NGUYEN/

Primary Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 13/842,879	Applicant(s)/Patent Under Reexamination BIBL ET AL.	
	Examiner KHIEM D. NGUYEN	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0176190	08-2005	Tomoda et al.	438/166
*	B	US-2007/0063644	03-2007	Kim, Jong Yun	313/506
*	C	US-2005/0078104	04-2005	Matthies et al.	345/204
*	D	US-2005/0243039	11-2005	Kwak, Won-Kyu	345/076
*	E	US-2006/0154390	07-2006	Tran et al.	438/022
*	F	US-2013/0285086	10-2013	Hu et al.	257/98
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	Art Unit
	KHIEM D NGUYEN	2823

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/162, H01L31/173, H01L31/1884, H01L31/1896, H01L33/00, H01L33/42	9/12/2013	/KN/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	88,89,99,100,E33.001	9/12/2013	/KN/
438	22,28,30,34,38,42,44	9/12/2013	/KN/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST text searched (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB), see attached search history.	9/11/2013	/KN/
EAST text searched (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB), see attached search history.	1/28/2014	/KN/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/KHIEM D NGUYEN/ Primary Examiner.Art Unit 2823

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S94	4	(("20130210194") or ("20130285086")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/28 13:44
S95	817	(display near panel) and (LED near2 pair)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 16:40
S96	50	S95 and (redundancy or redundant)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 16:41
S97	1427	(Andreas near Bibl).in. or (Kapil near2 Sakariya).in. or (Charles near2 Griggs).in. or (James near2 Perkins).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 17:26
S98	17	(Luxvue near Technology near Corporation).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 17:26
S99	1427	S97 or S98	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 17:26
S100	0	S99 and ((redundant or redundancy) near2 scheme) and (display near panel) and (subpixel or sub-pixel or sub$pixel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 17:34
S102	1	S99 and (display near panel) and	US-PGPUB;	OR	ON	2014/01/28

		(subpixel or sub-pixel or sub$pixel)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			17:35
S103	17791	(257/88,89,99,100,E33.001).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/28 17:36
S104	11810	(438/22,28,30,34,38,42,44).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/28 17:36
S105	27278	S103 or S104	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 17:36
S106	9109	H01L31/162.CPC. or H01L31/173.CPC. or H01L31/1884 or H01L31/1896.CPC. or H01L33/00.CPC. or H01L33/42.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 17:37
S108	35559	S105 or S106	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 17:43
S109	21467	S108 and (LED or (light near emit$4 near (device or diode)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 18:06
S110	16	S109 and (subpixel or sub-pixel) and (redundant or redundancy)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 18:07
S111	125130	(organic near light$4 near emit$4 near (diode or device)) or (organic near light-emit$4 near (diode or device)) or OLED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/01/28 18:56

			IBM_TDB			
S113	7	TFT same LED same (redundant or redundanc$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:09
S114	298630	(TFT or (thin near film near transistor) or thin-film-transistor or T-F-T)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:12
S115	538	(subpixel or sub-pixel) near10 LED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:24
S116	164	S114 and S115	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:24
S117	14	S108 and S116	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:24
S118	4909	AMLED or AMOLED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:25
S119	3	subpixel same LED same (redundant or redundanc$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:40
S120	7581	(defect$4 or contaminat$4) near8 LED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:44
S122	653	S120 and pixel	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2014/01/28 19:44

			JPO; DERWENT; IBM_TDB			
S123	58	S122 and (redundant or redundanc$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/28 19:45
S124	9109	H01L31/162.CPC. or H01L31/173.CPC. or H01L31/1884 or H01L31/1896.CPC. or H01L33/00.CPC. or H01L33/42.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 10:01
S125	425	(pixel near area) same (non-pixel near area)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 10:03
S126	4	S125 and subpixel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 10:03
S127	659	(349/192).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/29 11:39
S128	63	S127 and (redundant$4 or redundanc$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 11:44
S129	4835	AMOLED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:11
S130	139	S129 and (redundant or redundanc$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:11
S131	2659308	(LED or light-emit$4 or light-emit$4-device or light-emit$4-diode	US-PGPUB; USPAT;	OR	ON	2014/01/29 13:12

IPR2024-01134 - BOE
Exhibit 1009 - Page 88

		or light-emit$4-element or (light near emit$4))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S132	136	S130 and S131	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:12
S133	6498	AMOLED or (active near matrix near organic near light near emit$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:18
S134	162	S133 and (redundant or redundanc$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:18
S135	95988	PMOLED or AMOLED or OLED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:28
S136	29583	S135 and (display near panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:29
S137	22791	defect$4 same (redundant or redundanc$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:29
S138	57	S136 and S137	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 13:29
S139	4313	H01L25/167.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 15:17

S141	6	S139 and subpixel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/01/29 15:18
S142	5	(("20130126081") or ("8349116")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2014/01/29 18:00

EAST Search History (Interference)

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1/29/2014 10:25:03 PM
C:\Users\knguyen20\Documents\EAST\Workspaces\13842879.wsp

IPR2024-01134 - BOE
Exhibit 1009 - Page 90

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	Art Unit
	KHIEM D NGUYEN	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/12/2013	01/29/2014							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
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	27		✓							
	28		✓							
	29		✓							

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2823
				Examiner Name	Nguyen, Khiem D.
Sheet	1	**of**	1	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/KN/		US-	2013/0210194 A1	08-15-2013	Bibl et al.	
/KN/		US-	2013/0285086 A1	10-31-2013	Hu et al.	
		US-				
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	/Khiem Nguyen/	Date Considered	01/28/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KN/

Attorney's Docket No.: 9299P027 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Examiner: Nguyen, Khiem D.
Andreas Bibl	Art Unit: 2823
Application No.: 13/842,879	Confirmation No.: 7403
Filed: March 15, 2013	
For: Light Emitting Diode Display with Redundancy Scheme	

Filed via EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE

Sir:

This is in response to the Office Action mailed September 17, 2013. Applicants respectfully request the Examiner to enter the following amendments and consider the following remarks.

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office via electronic filing through the United States Patent and Trademark Electronic Filing System on:

12-16-2013
Date of Deposit

/Betty Scaletta/
Betty Scaletta

IN THE CLAIMS

Please amend the following claims.

1. (Currently amended) A display panel with redundancy scheme comprising:

a display substrate including a pixel area and a non-pixel area, wherein the pixel area includes an array of subpixels and a corresponding array of bottom electrodes within the array of subpixels;

an array of redundant micro LED device pairs bonded to the array of bottom electrodes, wherein each subpixel includes a bottom electrode and a redundant micro LED device pair bonded to the bottom electrode, and each redundant micro LED device pair within a respective subpixel is designed to emit a same primary color emission; and

one or more top electrode layers in electrical contact with the array of redundant micro LED device pairs.

2. (Original) The display panel of claim 1, wherein each micro LED device is formed of a semiconductor material.

3. (Original) The display panel of claim 2, wherein each micro LED device has a maximum width of 1 to 100 μm.

4. (Original) The display panel of claim 2, wherein the display substrate is a thin film transistor substrate.

5. (Original) The display panel of claim 4, further comprising a ground line in the non-pixel area of the thin film transistor substrate, wherein the one or more top electrode layers are electrically connected to the ground line.

IPR2024-01134 - BOE
Exhibit 1009 - Page 94

6. (Currently amended) The display of claim 5, wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a redundant micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the redundant micro LED device pair to the ground line.

7. (Original) The display panel of claim 2, further comprising an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip.

8. (Original) The display panel of claim 7, wherein each micro controller chip is connected to a scan driver circuit and a data driver circuit.

9. (Original) The display panel of claim 8, further comprising a ground line in the non-pixel area of the display substrate, wherein the one or more top electrode layers are electrically connected to the ground line.

10. (Currently amended) The display of claim 9, wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a redundant micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the redundant micro LED device pair to the ground line.

11. (Currently amended) The display of claim 2, further comprising:

IPR2024-01134 - BOE
Exhibit 1009 - Page 95

a plurality of micro LED device irregularities within the array of redundant micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and

a passivation layer material covering the plurality of irregularities.

12. (Original) The display of claim 11, wherein the one or more top electrode layers do not make electrical contact with the plurality of irregularities.

13. (Currently amended) The display of claim [[13]], wherein the one or more top electrode layers are formed directly over the plurality of irregularities.

14. (Original) The display of claim 13, wherein the one or more top electrode layers are not formed directly over the plurality of irregularities.

15. (Original) The display panel of claim 12, wherein the plurality of micro LED device irregularities are missing micro LED devices.

16. (Original) The display panel of claim 15, further comprising an array of bonding layers on the array of bottom electrodes corresponding to the plurality of missing micro LED devices, wherein the passivation layer material covers the array of bonding layers.

17. (Original) The display panel of claim 12, wherein the plurality of micro LED device irregularities are defective micro LED devices and the passivation layer material covers the defective micro LED devices.

18. (Original) The display panel of claim 12, wherein the plurality of micro LED device irregularities are contaminated micro LED devices and the passivation layer material covers the contaminated micro LED devices.

19. (Currently amended) The display panel of claim 11, wherein the passivation layer material covers sidewalls of the array of redundant micro LED device pairs.

20. (Original) The display panel of claim 11, further comprising a repair micro LED device bonded to one of the bottom electrodes including one of the micro LED device irregularities.

21. (New) The display panel of claim 4, wherein each subpixel and corresponding redundant micro LED device pair bonded to a corresponding bottom electrode is independently addressable by the thin film transistor substrate.

22. (New) The display panel of claim 7, wherein each subpixel and corresponding redundant micro LED device pair bonded to a corresponding bottom electrode is independently addressable by a micro controller chip.

23. (New) The display panel of claim 22, wherein each micro controller chip is bonded to the display substrate within the pixel area, and the each micro controller chip is connected to a scan driver circuit and a data driver circuit that is not bonded to the display substrate within the pixel area.

24. (New) The display panel of claim 1, wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs, a second array of

redundant micro LED device pairs, and a third array of redundant micro LED device pairs, wherein the first, second, and third arrays of redundant micro LED device pairs are designed to emit different primary color emissions.

25. (New) The display panel of claim 24, wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs designed to emit a red primary color emission, a second array of redundant micro LED device pairs designed to emit a green primary color emission, and a third array of emitting redundant micro LED device pairs designed to emit a blue primary color emission.

26. (New) The display panel of claim 1, wherein the array of redundant micro LED device pairs comprises a first array of redundant micro LED device pairs and a second array of redundant micro LED device pairs, wherein the first and second arrays of redundant micro LED device pairs are designed to emit different primary color emissions.

27. (New) The display panel of claim 24, wherein each micro LED device is bonded to a bottom electrode with an electrically conductive bonding layer directly between the micro LED device and the bottom electrode.

28. (New) The display panel of claim 27, wherein the electrically conductive bonding layer comprises a solder material.

29. (New) The display panel of claim 11, wherein the display substrate is a thin film transistor substrate.

REMARKS

The enclosed is responsive to the Office Action mailed on September 17, 2013. By way of the present response Applicants have amended claims 1, 6, 10, 11, 13, and 19 in order to more particularly point out and distinctly claim the subject matter which Applicants regard as the invention. No claims have been canceled. New claims 21-29 have been added. Applicants respectfully request reconsideration of the present application and the allowance of all claims now presented.

Interview Summary

Applicants thank the Examiner for the courtesies extended by the Examiner during the telephone interview held with Applicants' representative Jacob T. Aikin on November 26, 2013. During the interview, *Tomoda et al.* (U.S. Publication No. 2005/0176190) was discussed as it relates to the redundancy scheme described in the instant application. During the interview, Applicants' representative proposed amending independent claim 1 to further clarify the redundant micro LED device pairs with regard to bonding to the bottom electrodes of the subpixels and color emission. The Examiner indicated that further consideration of *Tomoda et al.* would be required upon receiving the formal response with proposed claim amendment. Accordingly, an agreement was not reached during the telephone interview.

Claim Objections

The Examiner has objected to claim 13 for depending upon itself. Applicants thank the Examiner for pointing out the informality. Appropriate correction has been made.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 1-6 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over *Tomoda et al.* (U.S. Publication No. 2005/0176190) in view of *Kim* (U.S.

Publication No. 2007/0063644). It is respectfully submitted that the cited references do not disclose or suggest each and every feature of amended independent claim 1, and that one of ordinary skill in the art would not have been motivated upon review of the cited references to arrive at the invention taught and claimed in amended independent claim 1.

By way of the present response, independent claim 1 has been amended to recite a display panel with redundancy scheme comprising, *inter alia*, "an array of redundant micro LED device pairs bonded to the array of bottom electrodes, wherein each subpixel includes a bottom electrode and a redundant micro LED device pair bonded to the bottom electrode, and each redundant micro LED device pair within a respective subpixel is designed to emit a same primary color emission."

Tomoda et al. describes a display device including a red light emitting diode 74 (see paragraph [0130]) and a blue light emitting diode 52 (see paragraph [0106]) bonded to a substrate 71 including a wiring layer 72 using adhesives 73, 65. It is respectfully submitted, that *Tomoda et al.* is unconcerned with and does not disclose a redundancy scheme as recited in amended independent claim 1. Specifically, it is respectfully submitted that one of ordinary skill in the art would understand that the red and blue LEDs 74, 52 are not a redundant pair of LEDs within a subpixel, are not bonded to the bottom electrode of the subpixel, and are not designed to emit a same primary color emission.

Kim describes a selective deposition method for an organic light emitting diode (OLED) display, where charged materials are selectively deposited into the R, G, and B sub pixels. It is respectfully submitted that *Kim* does not remedy the deficiencies of *Tomoda et al.* described above.

Applicants thus respectfully submit that claim 1, and claims 2-5 which depend directly or indirectly upon claim 1 are patentable over *Tomoda et al.* in view of *Kim*, and request that the rejection under 35 U.S.C. §103(a) be withdrawn.

The Examiner has rejected claims 7-10 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over *Tomoda et al.* in view of *Kim* and *Kwak* (U.S. Publication No. 2005/0243039).

Kwak describes a display panel 100 and a dada driver 400, scan driver 200, and emit controller 300 coupled to the display panel 100 outside of a pixel area of the display panel. See Fig. 2. It is respectfully submitted that *Kwak* does not remedy the deficiencies of *Tomoda et al.* and *Kim* described above with regard to independent claim 1.

Applicants thus respectfully submit that claims 7-10 are patentable over *Tomoda et al.* in view of *Kim* and *Kwak*, and request that the rejection under 35 U.S.C. §103(a) be withdrawn.

The Examiner has rejected claims 11-20 under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over *Tomoda et al.* in view of *Kim* and *Tran et al.* (U.S. Publication No. 2006/0154390).

Tran et al. describes using laser ablation to destroy defecting LEDs on a metal substrate. It is respectfully submitted that *Tran et al.* does not remedy the deficiencies of *Tomoda et al.* and *Kim* described above with regard to independent claim 1.

Applicants thus respectfully submit that claims 11-20 are patentable over *Tomoda et al.* in view of *Kim* and *Tran et al.* and request that the rejection under 35 U.S.C. §103(a) be withdrawn.

New Claims

New claims 21-29 have been added. It is respectfully submitted that new claims 21-29 are patentable for at least the same reasons as independent claim 1.

IPR2024-01134 - BOE
Exhibit 1009 - Page 101

Pursuant to 37 C.F.R. § 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. §§ 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: December 16, 2013

/Jacob Aikin/
Jacob T. Aikin
Reg. No. 62,787

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:

Andreas Bibl

Application No.: 13/842,879

Filed: March 15, 2013

For: Light Emitting Diode Display with Redundancy Scheme

Examiner: Nguyen, Khiem D.

Art Unit: 2823

Confirmation No.: 7403

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08a together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed for applications filed after June 30, 2003). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08a be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office via electronic filing through the United States Patent and Trademark Electronic Filing System on:

12-16-2013
Date of Deposit

/Betty Scaletta/
Betty Scaletta

IPR2024-01134 - BOE
Exhibit 1009 - Page 103

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

_____ 37 C.F.R. §1.97(b).

__X__ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

____ A statement pursuant to 37 C.F.R. §1.97(e) or

__X__ The Director is authorized to charge our Deposit Acct. No. 02-2666 in the amount of $180.00 for the fee under 37 C.F.R. § 1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

(1) A statement pursuant to 37 C.F.R. §1.97(e); and

(2) Authorization to charge our Deposit Acct. No. 02-2666 in the amount of $180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: December 16, 2013 /Jacob Aikin/
Jacob T. Aikin
Reg. No. 62,787

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300

Customer No.: 08791

IPR2024-01134 - BOE
Exhibit 1009 - Page 104

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2823
				Examiner Name	Nguyen, Khiem D.
Sheet	1	**of**	1	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	2013/0210194 A1	08-15-2013	Bibl et al.	
		US-	2013/0285086 A1	10-31-2013	Hu et al.	
		US-				
		US-				
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		US-				
		US-				

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Based on Form PTO/SB/08A (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03.

Electronic Patent Application Fee Transmittal

Application Number:	13842879
Filing Date:	15-Mar-2013
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Filer:	Jacob T. Aikin
Attorney Docket Number:	9299P027

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	9	80	720
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**900**

Electronic Acknowledgement Receipt	
EFS ID:	17671587
Application Number:	13842879
International Application Number:	
Confirmation Number:	7403
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Customer Number:	8791
Filer:	Jacob T. Aikin/Betty Scaletta
Filer Authorized By:	Jacob T. Aikin
Attorney Docket Number:	9299P027
Receipt Date:	16-DEC-2013
Filing Date:	15-MAR-2013
Time Stamp:	16:43:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$900
RAM confirmation Number	4665
Deposit Account	022666
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		9299P027_R-OA_12-16-13.pdf	54454 d2fbc19d573d540408491e47be3881dad6f368b0	yes	10

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	6
Applicant Arguments/Remarks Made in an Amendment	7	10

Warnings:

Information:

2	Transmittal Letter	9299P027_IDS_LTR_12-16-13.pdf	18664 edd8aef5a77693314c0d70e788e30c64a0b6b761	no	2

Warnings:

Information:

3	Information Disclosure Statement (IDS) Form (SB08)	9299P027_IDS_SB08_12-16-13.pdf	51783 04d630802ae2e7acef5ae0abbd9479daad026348	no	1

Warnings:

Information:

This is not an USPTO supplied IDS fillable form

4	Fee Worksheet (SB06)	fee-info.pdf	32223 7d0d687f316d5e0d65453afae94185d84f2eb47d	no	2

Warnings:

Information:

Total Files Size (in bytes):	157124

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/842,879	Filing Date 03/15/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT	12/16/2013	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 29	Minus	** 20	= 9	X $80 =	720
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**720**

		(Column 1)		(Column 2)	(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/BRENDA J. DENNY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/842,879	03/15/2013	Andreas Bibl	9299P027	7403

8791 7590 12/03/2013

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	
MAIL DATE	DELIVERY MODE
12/03/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	13/842,879	BIBL ET AL.	
	Examiner	Art Unit	
	KHIEM D. NGUYEN	2823	

All participants (applicant, applicant's representative, PTO personnel):

(1) *KHIEM D. NGUYEN*. (3)_____.

(2) *MR.JACOB AIKIN* . (4)_____.

Date of Interview: *26 November 2013*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *Tomoda et al. (U.S. Pub. 2005/0176190) and Kim (U.S. Pub. 2007/0063644)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Independent claim 1 and the 103(a) rejection based on Tomoda in view of Kim were discussed. Applicants' representative proposes to amend independent claim 1 to include the limitation of "wherein each subpixel including redundancy micro LED device pairs…wherein the redundancy micro LED device pairs emit the same color emission". No agreement has been reached and examiner will fully consider Applicants' formal response in due course.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/KHIEM D NGUYEN/ Primary Examiner, Art Unit 2823	11/26/2013

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/842,879	03/15/2013	Andreas Bibl	9299P027	7403

8791 7590 09/17/2013

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	
MAIL DATE	DELIVERY MODE
09/17/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/842,879	Applicant(s) BIBL ET AL.	
	Examiner KHIEM D. NGUYEN	Art Unit 2823	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/15/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *03/15/2013* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/03/13,07/16/13*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The IDS filed on 07/16/2013 and 04/03/2013 had been considered.

Claim Objections

2. Claim 13 is objected to because of the following informalities: Claim 13 depends on itself. Appropriate correction is required.

Claim Rejections - 35 USC § 103

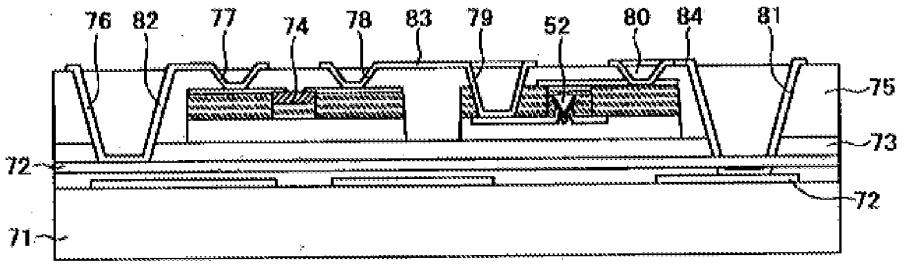
3. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomoda et al. (U.S. Pub. 2005/0176190) in view of Kim (U.S. Pub. 2007/0063644).

In re claim 1, Tomoda discloses a display panel with redundancy scheme comprising: a display substrate including a pixel area, wherein the pixel area includes an array of subpixels and a corresponding array of bottom electrodes 72 within the array of subpixels (see paragraph [0129] and FIG. 38); an array of micro LED device pairs 52, 74 bonded to the array of bottom electrodes 72 (via adhesive material 73); and one or more top electrode layers82, 83, 84 in electrical contact with the array of micro LED device pairs 52, 74 (see paragraph [0132] and FIG. 38).

FIG. 38



Tomoda is silent with respect to that the display substrate including a pixel area and a non-pixel area.

However, Kim discloses a display panel including inter-alia, the display substrate having a pixel area and a non-pixel area (see paragraph [0045] and claim 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of Applicants' claimed invention was made to modify Tomoda reference with the feature as taught by Kim to enable the display substrate including a pixel area and a non-pixel area in Tomoda to be formed because it is well-known in the art for the display substrate to include a pixel area and a non-pixel area so that conductive line can be formed in the non-pixel area. Furthermore, it would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention. *KSR*

International Co. v. Teleflex Inc. (KSR), 550 U.S. 398 (2007). "If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill." *Id.*

In re claim 2, as applied to claim 1 above, Tomoda in combination with Kim discloses wherein each micro LED device is formed of a semiconductor material (see paragraph [0122] of Tomoda).

In re claim 3, as applied to claim 2 above, Tomoda in combination with Kim discloses wherein each micro LED device has a maximum width of 1 to 100 μm (20μm) (see paragraph [0108] of Tomoda).

Furthermore, it is respectfully submitted that there is no evidence indicating the size of each micro LED device is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990); In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966); In re Aller, 220 F.2d 454, 456, 105 USPQ 233,235 (CCPA 1955).

In re claim 4, as applied to claim 2 above, Tomoda in combination with Kim discloses wherein the display substrate is a thin film transistor substrate (see paragraph [0096] of Tomoda and paragraph [0062] of Kim).

In re claim 5, as applied to claim 4 above, Tomoda in combination with Kim discloses wherein the display panel further comprising a ground line in the non-pixel area of the thin film transistor substrate, wherein the one or more top electrode layers are electrically connected to the ground line (see paragraph [0045] and claim 1 of Kim).

In re claim 6, as applied to claim 5 above, Tomoda in combination with Kim discloses wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the micro LED device pair to the ground line (see paragraphs [0132] of Tomoda and paragraph [0045] of Kim).

5. Claims 7-10 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomoda et al. (U.S. Pub. 2005/0176190) in view of Kim (U.S. Pub. 2007/0063644) as applied to claim 2 above, and further in view of Kwak (U.S. Pub. 2005/0243039).

In re claims 7 and 8, as applied to claim 2 paragraph 4 above, Tomoda and Kim does not specifically disclose wherein the display panel further comprising an array of micro controller chips bonded to the display substrate, wherein each bottom

electrode is electrically connected to a micro controller chip wherein each micro controller chip is connected to a scan driver circuit and a data driver circuit.

However, Kwak discloses a display panel including, inter-alia, an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip wherein each micro controller chip is connected to a scan driver circuit 200 and a data driver circuit 400.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of Applicants' claimed invention was made to modify Tomoda reference with the feature as taught by Kwak to enable an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip wherein each micro controller chip is connected to a scan driver circuit and a data driver circuit in Tomoda to be formed. Furthermore, it would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention. *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. 398 (2007). “If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person’s skill.” *Id.*

In re claim 9, as applied to claim 8 above, Tomoda in combination with Kim and Kwak discloses wherein the display panel further comprising a ground line in the non-pixel area of the display substrate, wherein the one or more top electrode layers are electrically connected to the ground line (see paragraph [0045] and claim 1 of Kim).

In re claim 10, as applied to claim 9 above, Tomoda in combination with Kim and Kwak discloses wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the micro LED device pair to the ground line (see paragraphs [0132] of Tomoda and paragraph [0045] of Kim).

6. Claims 11-20 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Tomoda et al. (U.S. Pub. 2005/0176190) in view of Kim (U.S. Pub. 2007/0063644) as applied to claim 2 above, and further in view of Tran et al. (U.S. Pub. 2006/0154390).

In re claim 11, as applied to claim 2 paragraph 4 above, Tomoda does not specifically disclose wherein the display further comprising: a plurality of micro LED device irregularities within the array of micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and a passivation layer material covering the plurality of irregularities.

However, Tran discloses a display panel including, inter-alia, a plurality of micro LED device irregularities within the array of micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and a passivation layer material covering the plurality of irregularities (see paragraphs [0004], [0030]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of Applicants' claimed invention was made to modify Tomoda reference with the feature as taught by Tran to enable a plurality of micro LED device irregularities within the array of micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and a passivation layer material covering the plurality of irregularities in Tomoda to be formed because in doing so LEDs array can be evaluate for defects and repair. Furthermore, it would have been obvious because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention. *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. 398 (2007). “If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person’s skill.” *Id.*

In re claim 12, as applied to claim 11 above, Tomoda in combination with Kim and Tran discloses wherein the one or more top electrode layers do not make electrical contact with the plurality of irregularities (see paragraph [0132] of Tomoda).

In re claim 13, as applied to claim 13 above, Tomoda in combination with Kim and Tran discloses wherein the one or more top electrode layers are formed directly over the plurality of irregularities (see paragraph [0132] of Tomoda).

In re claim 14, as applied to claim 13 above, Tomoda in combination with Kim and Tran discloses wherein the one or more top electrode layers are not formed directly over the plurality of irregularities (see paragraph [0132] of Tomoda).

In re claim 15, as applied to claim 12 above, Tomoda in combination with Kim and Tran discloses wherein the plurality of micro LED device irregularities are missing micro LED devices (see paragraph [0010] of Tran).

In re claim 16, as applied to claim 15 above, Tomoda in combination with Kim and Tran discloses wherein the display panel further comprising an array of bonding layers on the array of bottom electrodes corresponding to the plurality of missing micro LED devices, wherein the passivation layer material covers the array of bonding layers (see paragraph [0010] of Tran).

In re claim 17, as applied to claim 12 above, Tomoda in combination with Kim and Tran discloses wherein the plurality of micro LED device irregularities are defective micro LED devices and the passivation layer material covers the defective micro LED devices (see paragraph [0010] of Tran).

In re claim 18, as applied to claim 12 above, Tomoda in combination with Kim and Tran discloses wherein the plurality of micro LED device irregularities are contaminated micro LED devices and the passivation layer material covers the contaminated micro LED devices (see paragraph [0004] of Tran).

In re claim 19, as applied to claim 11 above, Tomoda in combination with Kim and Tran discloses wherein the passivation layer material covers sidewalls of the array of micro LED device pairs (see paragraph [0025] of Tran).

In re claim 20, as applied to claim 11 above, Tomoda in combination with Kim and Tran discloses wherein the display panel further comprising a repair micro LED device bonded to one of the bottom electrodes including one of the micro LED device irregularities (see paragraph [0004] of Tran).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHIEM D. NGUYEN whose telephone number is (571)272-1865. The examiner can normally be reached on Monday-Friday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KHIEM D NGUYEN/

Primary Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 13/842,879	Applicant(s)/Patent Under Reexamination BIBL ET AL.	
	Examiner KHIEM D. NGUYEN	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0176190	08-2005	Tomoda et al.	438/166
*	B	US-2007/0063644	03-2007	Kim, Jong Yun	313/506
*	C	US-2005/0243039	11-2005	Kwak, Won-Kyu	345/076
*	D	US-2006/0154390	07-2006	Tran et al.	438/022
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	Q					
	R					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	~~2871~~ 2823
				Examiner Name	~~Not yet assigned~~ K. Nguyen
Sheet	1	**of**	7	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/KN/		US-	5,592,358	01-07-1997	Shamouilian et al.	
		US-	5,839,187	11-24-1998	Sato et al.	
		US-	5,851,664	12-22-1998	Bennett et al.	
		US-	5,888,847	03-30-1999	Rostoker et al.	
		US-	5,903,428	05-11-1999	Grimard et al.	
		US-	5,996,218	12-07-1999	Shamouilian et al.	
		US-	6,071,795	06-06-2000	Cheung et al.	
		US-	6,335,263 B1	01-01-2002	Cheung et al.	
		US-	6,403,985	06-11-2002	Fan, et al.	
		US-	6,420,242 B1	07-16-2002	Cheung et al.	
		US-	6,521,511	02-18-2003	Inoue et al.	
		US-	6,558,109	05-06-2003	Gibbel, David S.	
		US-	6,613,610	09-02-2003	Iwafuchi, et al.	
		US-	6,629,553	10-07-2003	Odashima et al.	
/KN/		US-	6,670,038 B2	12-30-2003	Sun et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
/KN/		JP 3406207	05-28-1999	Sharp Corp.		
/KN/		WO 2011/123285	10-06-2011	SEMPRIUS INC		

Examiner Signature	/Khiem Nguyen/	Date Considered	09/11/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KN/

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	2	**of**	7	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/KN/		US-	6,786,390	09-07-2004	Yang et al.	
		US-	6,878,607	04-12-2005	Inoue et al.	
		US-	7,033,842	04-25-2006	Haji et al.	
		US-	7,148,127	12-12-2006	Oohata, et al.	
		US-	7,208,337 B2	04-24-2007	Eisert et al.	
		US-	7,353,596	04-08-2008	Shida et al.	
		US-	7,358,158	04-15-2008	Aihara et al.	
		US-	7,585,703 B2	09-08-2009	Matsumura et al.	
		US-	7,723,764	05-25-2010	Oohata, et al.	
		US-	7,795,629 B2	09-14-2010	Watanabe, et al.	
		US-	7,797,820	09-21-2010	Shida et al.	
		US-	7,838,410	11-23-2010	Hirao, et al.	
		US-	7,880,184 B2	02-01-2011	Iwafuchi, et al.	
		US-	7,884,543	02-08-2011	Doi	
		US-	7,888,690 B2	02-15-2011	Iwafuchi, et al.	
		US-	7,906,787 B2	03-15-2011	Kang	
		US-	7,910,945 B2	03-22-2011	Donofrio et al.	
		US-	7,927,976	04-19-2011	Menard	
		US-	7,928,465 B2	04-19-2011	Lee et al.	
		US-	7,972,875	07-05-2011	Rogers, et al.	
		US-	7,999,454	08-16-2011	Winters, et al.	
		US-	8,023,248 B2	09-20-2011	Yonekura et al.	
		US-	8,333,860	12-18-2012	Bibl, et al.	
		US-	8,349,116	01-08-2013	Bibl, et al.	
		US-	2001/0029088	10-11-2001	Odajima et al.	
/KN/		US-	2002/0076848	06-20-2002	Spooner et al.	

Examiner Signature	/Khiem Nguyen/	Date Considered	09/11/2013

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	3	of	7	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/KN/		US-	2003/0010975	01-16-2003	Gibb et al.	
		US-	2003/0177633 A1	09-25-2003	Haji et al.	
		US-	2006/0160276	07-20-2006	Brown et al.	
		US-	2006/0214299	09-28-2006	Fairchild et al.	
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/KN/		US-	8,049,410 B2	11-01-2011	Suh et al.	

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Sheet	4	**of**	7	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code[2] (If known)				
/KN/		US-	2003/0094615 A1	05-22-2003	Yamazaki et al.	
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
/KN/	NPL1	ASANO, Kazutoshi, et al., "Fundamental Study of an Electrostatic Chuck for Silicon Wafer Handling" IEEE Transactions on Industry Applications, Vol. 38, No. 3, May/June 2002, pp. 840-845.	
	NPL2	BOWER, C.A., et al., "Active-Matrix OLED Display Backplanes Using Transfer-Printed Microscale Integrated Circuits", IEEE, 2010 Electronic Components and Technology Conference, pgs. 1339-1343	
	NPL3	"Characteristics of electrostatic Chuck(ESC)" Advanced Materials Research Group, New Technology Research Laborotory, 2000, pp. 51-53 accessed at http://www.socnb.com/report/ptech_e/2000p51_e.pdf	
	NPL4	GUERRE, Roland, et al, "Selective Transfer Technology for Microdevice Distribution" Journal of Microelectromechanical Systems, Vol. 17, No. 1, February 2008, pp. 157-165.	
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	NPL6	HARRIS, Jonathan H., "Sintered Aluminum Nitride Ceramics for High-Power Electronic Applications" Journal of the Minerals, Metals and Materials Society, Vol. 50, No. 6, June 1998, pg. 56.	
	NPL7	HORWITZ, Chris M., "Electrostatic Chucks: Frequently Asked Questions" Electrogrip, 2006, 10 pgs, accessed at www.electrogrip.com.	
	NPL8	HOSSICK-SCHOTT, Joachim, "Prospects for the ultimate energy density of oxide-based capacitor anodes" Proceedings of CARTS Europe, Barcelona, Spain, 2007, 10 pgs.	
	NPL9	LEE, San Youl, et al., "Wafer-level fabrication of GAN-based vertical light-emitting diodes using a multi-functional bonding material system" Semicond. Sci. Technol. 24, 2009, 4 pgs.	
	NPL10	"Major Research Thrust: Epitaxial Layer Transfer by Laser Lift-off" Purdue University, Heterogeneous Integration Research Group, accessed at https://engineering.purdue.edu/HetInt/project_epitaxial_layer_transfer_llo.htm, last updated August 2003.	
/KN/	NPL11	MEI, Zequn, et al., "Low-Temperature Solders" Hewlett-Packard Journal, Article 10, August 1996, pp. 1-10.	

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/KN/	NPL12	MERCADO, Lei, L., et al., "A Mechanical Approach to Overcome RF MEMS Switch Stiction Problem" 2003 Electronic Components and Technology Conference, pp. 377-384.	
	NPL13	MISKYS, Claudio R., et al., "Freestanding GaN-substrates and devices" phys. Stat. sol. © 0, No. 6, 2003, pp. 1627-1650.	
	NPL14	"Principles of Electrostatic Chucks: 1 - Techniques for High Performance Grip and Release" ElectroGrip, Principles1 rev3 May 2006, 2 pgs, accessed at www.electrogrip.com.	
	NPL15	STEIGERWALD, Daniel, et al., "III-V Nitride Semiconductors for High-Performance Blue and Green Light-Emitting Devices" article appears in journal JOM 49 (9) 1997, pp. 18-23. Article accessed 11/2/2011 at http://www.tms.org/pubs/journals/jom/9709/setigerwald-9709.html, 12 pgs.	
	NPL16	WIDAS, Robert, "Electrostatic Substrate Clamping For Next Generation Semiconductor Devices" April 21, 1999, 4 pgs.	
	NPL17	GEFFROY, et al., "Organic light-emitting diode (OLED) technology: materials, devices and display technologies," 2006 Society of Chemical Industry, pp. 572-582.	
	NPL18	GOHDA, et al., "58.3: A 3.6-in. 202-ppi Full-Color AMPLED Display Fabricated by Ink-Jet Method," 2006 SID Digest, pp. 1767-1770.	
	NPL19	OHARA, et al., "4.0-inch Active-Matrix Organic Light-Emitting Diode Display Integrated with Driver Circuits Using Amorphous IN-Ga-Zn-Oxide Thin-Film Transistors with Suppressed Variation," 2010 The Japan Society of Applied Physics, pp 1-6.	
	NPL20	BOWER, et al., "Active-Matrix OLED Display Backplanes Using Transfer-Printed Microscale Integrated Circuits," IEEE, 2010 Electronic Components and Technology Conference, pp. 1339-1343.	
	NPL21	HEKMATSHOAR, et al., "A novel TFT-OLED integration for OLED-independent pixel programming in amorphous-Si AMOLED pixels," 2008, Society for Information Display, Journal of the SID 16/1, pp. 183-188.	
/KN/	NPL22	SARMA, et al., "Active Matrix OLED Using 150°C a-Si TFT Backplane Built on Flexible Plastic Substrate," SPIE Symp. On Aerospace/Defense Sending, Orlando, FL, April 2003, and to be published in SPIE Proc., Vol. 5080, paper 24 (2003), 12 pgs.	

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/KN/	NPL23	"LINE SCAN IMAGING BASICS – Application Note," DALSA – Technology with vision, 11 pgs., [n.d.], PDF metadata indicates document creation date 1/21/2003.	
/KN/	NPL24	KIPMAN, Yair, "Dot placement Analysis Using a Line Scan Camera and Rigid Body Rotation," ImageXpert Inc., Nashua, NH, USA, 4 pgs., [n.d.], PDF metadata indicates document creation date 5/10/2004.	

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	429121	(display near panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:03
S2	350	(pixel near area) same (non-pixel near area)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:03
S3	127	S1 and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:04
S4	13	S3 and (subpixel or sub-pixel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 18:04
S5	15375	(257/88,89,99,100,E33.001).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/11 22:34
S6	10320	(438/22,28,30,34,38,42,44).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/11 22:36
S7	23846	S5 or S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 22:36
S8	838	micro near LEDs	US-PGPUB;	OR	ON	2013/09/11

IPR2024-01134 - BOE
Exhibit 1009 - Page 135

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			22:41
S9	30	S8 near20 (recess or groove or trench)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 22:41
S10	30330	LED near20 (recess or groove or trench)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 23:44
S11	225	S10 same micro	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 23:44
S12	4	S11 same (contaminat$4 or defect$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 23:45
S13	519	(Andreas near Bibl).in. or (Kapil near2 Sakariya).in. or (Charles near2 Griggs).in. or (James near2 Perkins).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 23:58
S14	12	(Luxvue near Technology near Corporation).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/11 23:58
S15	18	S13 and ((micro near LED) or micro-led)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 00:02
S16	14568	LED near4 pair	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/09/12 00:06

IPR2024-01134 - BOE
Exhibit 1009 - Page 136

			IBM_TDB			
S17	1352	S16 same electrode	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 00:06
S18	54	S17 same pixel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 00:06
S19	154	("20090314991" | "5903428" | "7838410" | "7910945" | "7927976" | "8049410" | "20030177633" | "20050104530" | "20060238463" | "20090068774" | "6420242" | "6911666" | "20030017360" | "20060160276" | "20100188794" | "6335263" | "7928465" | "20030010975" | "20030094615" | "20070194330" | "20090303713" | "20100248484" | "5592358" | "5839187" | "7160633" | "7585703" | "7999454" | "8349116" | "20120134065" | "20130126081" | "20010029088" | "20040227704" | "20050274959" | "20090284501" | "20100276726" | "6403985" | "6558109" | "6613610" | "6629553" | "7208337" | "7482696" | "7797820" | "8023248" | "20020076848" | "20060214299" | "20070166851" | "20100051910" | "20100203661" | "20120064642" | "5996218" | "6071795" | "6878607" | "7033842" | "7358158" | "7880184" | "8333860" | "20130126891" | "20100309100" | "20110151602" | "5888847" | "6670038" | "7353596" | "7884543" | "7888690" | "7972875" | "20080163481" | "20090146303" | "20110003410" | "5851664" | "6521511" | "6786390" | "7148127" | "7642710" | "7723764" | "7795629" | "7795804" | "7906787").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 00:07
S20	2	("7795804").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 00:14
S21	4	("20030038594" | "20050116236" | "20060273715" | "7489072").PN. OR ("7795804").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 00:15
S22	2	("7723764").PN.	US-PGPUB; USPAT; USOCR;	OR	OFF	2013/09/12 09:37

IPR2024-01134 - BOE
Exhibit 1009 - Page 137

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S23	11	("4914731" | "5997152").PN. OR ("7723764").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 09:37
S24	186	(Khiem near Nguyen) and ((light near emit$4) or LED) and (recess$4 or groove)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 10:07
S25	50	S24 and wiring	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 10:08
S26	2	("7482696").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 10:09
S27	5	("20020008325" | "5298768" | "6445011").PN. OR ("7482696").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 10:09
S28	2	("5298768").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 10:14
S29	56	("4013915" | "5035483" | "5089861").PN. OR ("5298768").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 10:14
S30	2	("7524097").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 10:19
S31	54	("3875456" | "4152624" | "4211955" | "4298869" | "4377768" | "4450512" | "4580196" | "4646210" | "4733336" | "4807096" | "4849803" | "4853598" | "4882565" | "4929866" | "4947291" | "4992704" | "5008595" | "5083192" | "5136483" | "5143433" | "5255171" | "5289082" | "5298768" | "5303037" | "5325271" | "5371659" | "5384519" | "5441918" | "5477436" | "5497305" | "5500635" | "5564819" | "5613751" | "5699044" | "5752766" | "5836676" | "5865529" | "5895115" | "5921652" |	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 10:19

IPR2024-01134 - BOE
Exhibit 1009 - Page 138

		"5944408" | "6126298" | "6184629").PN. OR ("7524097").URPN.				
S32	2	("5608553").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 10:33
S33	56	("4013915" | "5035483" | "5089861").PN. OR ("5298768").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 10:38
S34	932284	display and panel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 11:24
S35	201912	S34 and pixel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 11:25
S36	863	(microled or micro-led or (micro near led))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 11:25
S37	70	S35 and S36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 11:25
S38	32	S37 and (defect$4 or repair$4 or test$4 or check$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 11:25
S39	2	("20050176190").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 11:35
S40	4	("2003/0170971").URPN.	USPAT	OR	ON	2013/09/12 11:52
S41	49	("20020096994" | "20020115265" | "20020171089" | "20030011377" | "20030034120" | "20030057425" | "20030087476" | "20030160258" |	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 11:53

		"20030162463" | "20030170971" | "20040080032" | "20040183133" | "20060038182" | "20060055864" | "20060138541" | "20070032089" | "20070235734" | "20090199960" | "20090269907" | "20090294803" | "20100002402" | "20100072577" | "20100289124" | "20110136296" | "4846931" | "4883561" | "5691230" | "6093623" | "6143582" | "6309950" | "6414783" | "6424020" | "6521940" | "6538330" | "6627953" | "6656819" | "6700631" | "7244990" | "7427526" | "7557367" | "7585703" | "7622367" | "7659178" | "7662545" | "7799699" | "7919392" | "7973336" | "7982296").PN. OR ("8198148").URPN.				
S42	2	("5608553").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 12:00
S43	1725940	(light near emit$4 near (diode or device or element)) or LED or micro-led	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:14
S44	342085	S43 and transmission	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:17
S45	33736	S44 and (display near panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:18
S46	12890	S45 and driver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:18
S47	5298	S46 and TFT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 12:18
S48	4	S47 and ground and pixel and non-pixel	US-PGPUB; USPAT; USOCR;	OR	ON	2013/09/12 12:19

IPR2024-01134 - BOE
Exhibit 1009 - Page 140

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S49	4583	AMOLED or (active near matrix near organic near light near emit$4 near (diode or device or element))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 13:32
S50	2357	S49 and TFT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 13:33
S51	403	S50 and micro and LED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 13:34
S53	93	S51 and (Display near Substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 13:52
S54	82329	(TFT near substrate) or backplane or back-plane or (back adj plane)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 15:25
S55	657	S54 and AMOLED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 15:27
S56	2364	H01L31/162.CPC. or H01L31/173.CPC. or H01L31/1884 or H01L31/1896.CPC. or H01L33/00.CPC. or H01L33/42.CPC.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 16:50
S57	1734	S56 and (LED or (light near emit$4 near (diode or device)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 16:59
S58	12	S57 and repair$4 and (defect$4 or	US-PGPUB;	OR	ON	2013/09/12

IPR2024-01134 - BOE
Exhibit 1009 - Page 141

		short$4 or imperfect$4 or damag$4)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			17:00
S59	12	S57 and repair$4 and (defect$4 or short$4 or imperfect$4 or damag$4 or contaminat$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 17:01
S60	705	pixel and non-pixel and TFT	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 17:04
S61	534	S60 and (pair or array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 17:05
S62	305	S61 and (display near panel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 17:05
S63	94	S62 and (LED or (light near emit$4 near (diode or device)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 17:05
S64	2	("20070114521").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 17:34
S65	11	("20020048829" | "20030017297" | "20030085654" | "20030164674" | "20030209708" | "20040066137" | "20040212759" | "20050084214" | "20050110020" | "20050242720" | "7109653").PN. OR ("RE43442").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2013/09/12 17:36
S66	1873	pixel same non-pixel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 18:07

IPR2024-01134 - BOE
Exhibit 1009 - Page 142

S68	25	S66 same ground	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 18:08
S69	12	S68 and (LED or (light near emit$4 near (diode or device)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 18:11
S70	33	S66 and LED and ground	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 18:14
S71	31	S70 not S69	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 18:14
S72	2	("20070063644").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/09/12 18:24
S73	0	(controller near chips) near10 (display near substrate) near20 driver near20 scan$4 near20 data	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 21:50
S74	11	(controller) near10 (display near substrate) near20 driver near20 scan$4 near20 data	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 21:50
S75	22	(US-20130141678-$ or US-20090179556-$ or US-20090135103-$ or US-20050161740-$ or US-20030017360-$ or US-20100207849-$ or US-20070176185-$ or US-20070170859-$ or US-20070170605-$ or US-20070114519-$ or US-20090045733-$).did. or (US-8049410-$ or US-7795804-$ or US-7642710-$ or US-7482696-$ or US-8529104-$ or US-8203218-$ or US-8044412-$ or US-7160633-$ or US-7148127-$ or US-5608553-$ or US-RE43442-$).did.	US-PGPUB; USPAT	OR	ON	2013/09/12 22:14

IPR2024-01134 - BOE
Exhibit 1009 - Page 143

S76	1	S75 and ((defect$4 or missing or contaminat$4) near4 LED)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:14
S77	1	(defect$4 same missing same contaminat$4) same LED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:16
S78	4214	(defect$4 or missing or contaminat$4) near4 LED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:18
S79	3	(defect$4 or missing or contaminat$4) near4 (micro near LED)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:18
S80	490	(irregularities near4 LED)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:21
S81	7	S80 same defect$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:21
S82	44	(defect$4 near8 contaminat$4) near4 LED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:24
S83	4	S82 and display and panel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:25
S84	47	defect$4 near10 (plurality near4 LED)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/09/12 22:28

IPR2024-01134 - BOE
Exhibit 1009 - Page 144

			DERWENT; IBM_TDB			
S85	12	S84 and display and panel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:28
S86	548	redundan$4 near4 LED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:34
S87	24	S86 same defect$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:34
S88	2684	defect$4 near4 LED	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:40
S89	156	S88 same array	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:40
S90	4	S89 same passivation	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/09/12 22:40

EAST Search History (Interference)

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IPR2024-01134 - BOE
Exhibit 1009 - Page 145

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CONFIRMATION NO. 7403

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/842,879	03/15/2013	257	2823	9299P027

APPLICANTS

Andreas Bibl, Los Altos, CA;
Kapil V. Sakariya, Sunnyvale, CA;
Charles R. Griggs, San Jose, CA;
James Michael Perkins, Mountain View, CA;
LUXVUE TECHNOLOGY CORPORATION, Santa Clara, CA

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
05/18/2013

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /KHIEM D NGUYEN/ Examiner's Signature	☐ Met after Allowance /KN/ Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	30	20	1

ADDRESS

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
UNITED STATES

TITLE

LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

FILING FEE RECEIVED		
1560	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	Art Unit
	KHIEM D NGUYEN	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/12/2013								
	1	✓								
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	20	✓								

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	~~2874~~ 2823
				Examiner Name	~~Not yet assigned~~ K. Nguyen
Sheet	1	**of**	1	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/KN/		US-	2012/0134065 A1	05-31-2012	Furuya et al.	
/KN/		US-	2013/0126081 A1	03-23-2013	Hu et al.	
/KN/		US-	2013/0126891 A1	03-23-2013	Bibl et al.	
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Examiner Signature	/Khiem Nguyen/	Date Considered	09/11/2013

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KN/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13842879	BIBL ET AL.
	Examiner	Art Unit
	KHIEM D NGUYEN	2823

CPC- SEARCHED		
Symbol	Date	Examiner
H01L31/162, H01L31/173, H01L31/1884, H01L31/1896, H01L33/00, H01L33/42	9/12/2013	/KN/

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	88,89,99,100,E33.001	9/12/2013	/KN/
438	22,28,30,34,38,42,44	9/12/2013	/KN/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST text searched (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB), see attached search history.	9/11/2013	/KN/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/KHIEM D NGUYEN/ Primary Examiner.Art Unit 2823

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	1	**of**	1	Attorney Docket Number	9299P027

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		US-	2012/0134065 A1	05-31-2012	Furuya et al.	
		US-	2013/0126081 A1	03-23-2013	Hu et al.	
		US-	2013/0126891 A1	03-23-2013	Bibl et al.	
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Examiner Signature		Date Considered	

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Based on Form PTO/SB/08A (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03.

Electronic Acknowledgement Receipt

EFS ID:	16332100
Application Number:	13842879
International Application Number:	
Confirmation Number:	7403
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Customer Number:	8791
Filer:	Jacob T. Aikin/Betty Scaletta
Filer Authorized By:	Jacob T. Aikin
Attorney Docket Number:	9299P027
Receipt Date:	16-JUL-2013
Filing Date:	15-MAR-2013
Time Stamp:	18:14:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	9299P027_IDS_LTR_07-16-13.pdf	18845 edf5ac15b83a11411549bb4b377d9443f814150d	no	2

Warnings:	
Information:	

2	Information Disclosure Statement (IDS) Form (SB08)	9299P027_IDS_SB08_07-16-13.pdf	51841 ba3dfeb181e3da4128c535f85c7895bd1cbb1a86	no	1

Warnings:

Information:

This is not an USPTO supplied IDS fillable form

Total Files Size (in bytes):	70686

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	
Andreas Bibl	Examiner: Not yet assigned
Application No.: 13/842,879	Art Unit: 2871
Filed: March 15, 2013	Confirmation No.: 7403
For: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08a together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed for applications filed after June 30, 2003). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08a be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office via electronic filing through the United States Patent and Trademark Electronic Filing System on:

07-16-2013
Date of Deposit

/Betty Scaletta/
Betty Scaletta

IPR2024-01134 - BOE
Exhibit 1009 - Page 153

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

X 37 C.F.R. §1.97(b).

_____ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

_____ A statement pursuant to 37 C.F.R. §1.97(e) or

_____ The Director is authorized to charge our Deposit Acct. No. 02-2666 in the amount of $180.00 for the fee under 37 C.F.R. § 1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

(1) A statement pursuant to 37 C.F.R. §1.97(e); and

(2) Authorization to charge our Deposit Acct. No. 02-2666 in the amount of $180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: July 16, 2013

/Jacob Aikin/
Jacob T. Aikin
Reg. No. 62,787

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300

Customer No.: 08791

IPR2024-01134 - BOE
Exhibit 1009 - Page 154

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE CA 94085-4040

MAILED
JUN 03 2013
OFFICE OF PETITIONS

Doc Code: TRACK1.GRANT

Decision Granting Request for Prioritized Examination (Track I or After RCE)	Application No.: 13/842,879

1. THE REQUEST FILED March 15, 2013 IS **GRANTED**.

The above-identified application has met the requirements for prioritized examination
A. ☒ for an original nonprovisional application (Track I).
B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination.** The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

A. filing a **petition for extension of time** to extend the time period for filing a reply;
B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims**, or a multiple dependent claim;
C. filing a **request for continued examination**;
D. filing a notice of appeal;
E. filing a request for suspension of action;
F. mailing of a notice of allowance;
G. mailing of a final Office action;
H. completion of examination as defined in 37 CFR 41.102; or
I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to **Michelle R. Eason** at (571) 272-4231. In his/her absence, calls may be directed to Brian W. Brown at (571) 272-5338.

/Michelle R. Eason/
(*Signature*)

Paralegal Specialist, Office of Petitions
(Title)

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/842,879	03/15/2013	2871	1560	9299P027	20	1

CONFIRMATION NO. 7403

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

FILING RECEIPT

OC000000061352511

Date Mailed: 05/29/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Andreas Bibl, Los Altos, CA;
Kapil V. Sakariya, Sunnyvale, CA;
Charles R. Griggs, San Jose, CA;
James Michael Perkins, Mountain View, CA;

Applicant(s)

LUXVUE TECHNOLOGY CORPORATION, Santa Clara, CA

Assignment For Published Patent Application

LUXVUE TECHNOLOGY CORPORATION, Santa Clara, CA

Power of Attorney: The patent practitioners associated with Customer Number 08791

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 05/18/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/842,879**

Projected Publication Date: 09/18/2014

Non-Publication Request: No

Early Publication Request: No

Title

LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

Preliminary Class

349

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/842,879

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/842,879	03/15/2013	Andreas Bibl	9299P027

CONFIRMATION NO. 7403

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

POA ACCEPTANCE LETTER



Date Mailed: 05/29/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/15/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/btsebhatu/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	1	**of**	7	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	5,592,358	01-07-1997	Shamouilian et al.	
		US-	5,839,187	11-24-1998	Sato et al.	
		US-	5,851,664	12-22-1998	Bennett et al.	
		US-	5,888,847	03-30-1999	Rostoker et al.	
		US-	5,903,428	05-11-1999	Grimard et al.	
		US-	5,996,218	12-07-1999	Shamouilian et al.	
		US-	6,071,795	06-06-2000	Cheung et al.	
		US-	6,335,263 B1	01-01-2002	Cheung et al.	
		US-	6,403,985	06-11-2002	Fan, et al.	
		US-	6,420,242 B1	07-16-2002	Cheung et al.	
		US-	6,521,511	02-18-2003	Inoue et al.	
		US-	6,558,109	05-06-2003	Gibbel, David S.	
		US-	6,613,610	09-02-2003	Iwafuchi, et al.	
		US-	6,629,553	10-07-2003	Odashima et al.	
		US-	6,670,038 B2	12-30-2003	Sun et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		JP 3406207	05-28-1999	Sharp Corp.		
		WO 2011/123285	10-06-2011	SEMPRIUS INC		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Based on Form PTO/SB/08A (08-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 09/10/03.

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	2	**of**	7	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	6,786,390	09-07-2004	Yang et al.	
		US-	6,878,607	04-12-2005	Inoue et al.	
		US-	7,033,842	04-25-2006	Haji et al.	
		US-	7,148,127	12-12-2006	Oohata, et al.	
		US-	7,208,337 B2	04-24-2007	Eisert et al.	
		US-	7,353,596	04-08-2008	Shida et al.	
		US-	7,358,158	04-15-2008	Aihara et al.	
		US-	7,585,703 B2	09-08-2009	Matsumura et al.	
		US-	7,723,764	05-25-2010	Oohata, et al.	
		US-	7,795,629 B2	09-14-2010	Watanabe, et al.	
		US-	7,797,820	09-21-2010	Shida et al.	
		US-	7,838,410	11-23-2010	Hirao, et al.	
		US-	7,880,184 B2	02-01-2011	Iwafuchi, et al.	
		US-	7,884,543	02-08-2011	Doi	
		US-	7,888,690 B2	02-15-2011	Iwafuchi, et al.	
		US-	7,906,787 B2	03-15-2011	Kang	
		US-	7,910,945 B2	03-22-2011	Donofrio et al.	
		US-	7,927,976	04-19-2011	Menard	
		US-	7,928,465 B2	04-19-2011	Lee et al.	
		US-	7,972,875	07-05-2011	Rogers, et al.	
		US-	7,999,454	08-16-2011	Winters, et al.	
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Examiner Signature		Date Considered	

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	3	**of**	7	Attorney Docket Number	9299P027

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	2003/0010975	01-16-2003	Gibb et al.	
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		US-	8,049,410 B2	11-01-2011	Suh et al.	

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	13/842,879
				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	4	**of**	7	Attorney Docket Number	9299P027

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		Number-Kind Code[2] (If known)				
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				Examiner Name	Not yet assigned
Sheet	5	**of**	7	Attorney Docket Number	9299P027

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	NPL1	ASANO, Kazutoshi, et al., "Fundamental Study of an Electrostatic Chuck for Silicon Wafer Handling" IEEE Transactions on Industry Applications, Vol. 38, No. 3, May/June 2002, pp. 840-845.	
	NPL2	BOWER, C.A., et al., "Active-Matrix OLED Display Backplanes Using Transfer-Printed Microscale Integrated Circuits", IEEE, 2010 Electronic Components and Technology Conference, pgs. 1339-1343	
	NPL3	"Characteristics of electrostatic Chuck(ESC)" Advanced Materials Research Group, New Technology Research Laborotory, 2000, pp. 51-53 accessed at http://www.socnb.com/report/ptech_e/2000p51_e.pdf	
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	NPL11	MEI, Zequn, et al., "Low-Temperature Solders" Hewlett-Packard Journal, Article 10, August 1996, pp. 1-10.	

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				Filing Date	March 15, 2013
				First Named Inventor:	Andreas Bibl
				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	6	**of**	7	Attorney Docket Number	9299P027

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	NPL12	MERCADO, Lei, L., et al., "A Mechanical Approach to Overcome RF MEMS Switch Stiction Problem" 2003 Electronic Components and Technology Conference, pp. 377-384.	
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	NPL20	BOWER, et al., "Active-Matrix OLED Display Backplanes Using Transfer-Printed Microscale Integrated Circuits," IEEE, 2010 Electronic Components and Technology Conference, pp. 1339-1343.	
	NPL21	HEKMATSHOAR, et al., "A novel TFT-OLED integration for OLED-independent pixel programming in amorphous-Si AMOLED pixels," 2008, Society for Information Display, Journal of the SID 16/1, pp. 183-188.	
	NPL22	SARMA, et al., "Active Matrix OLED Using 150°C a-Si TFT Backplane Built on Flexible Plastic Substrate," SPIE Symp. On Aerospace/Defense Sending, Orlando, FL, April 2003, and to be published in SPIE Proc., Vol. 5080, paper 24 (2003), 12 pgs.	

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				Filing Date	March 15, 2013
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				Art Unit	2871
				Examiner Name	Not yet assigned
Sheet	7	**of**	7	Attorney Docket Number	9299P027

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	NPL23	"LINE SCAN IMAGING BASICS – Application Note," DALSA – Technology with vision, 11 pgs., [n.d.], PDF metadata indicates document creation date 1/21/2003.	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	
Andreas Bibl	Examiner: Not yet assigned
Application No.: 13/842,879	Art Unit: 2871
Filed: March 15, 2013	Confirmation No.: 7403
For: LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08a together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed for applications filed after June 30, 2003). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08a be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

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04-03-2013
Date of Deposit

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Betty Scaletta

IPR2024-01134 - BOE
Exhibit 1009 - Page 168

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Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

X 37 C.F.R. §1.97(b).

_____ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

_____ A statement pursuant to 37 C.F.R. §1.97(e) or

_____ The Director is authorized to charge our Deposit Acct. No. 02-2666 in the amount of $180.00 for the fee under 37 C.F.R. § 1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

(1) A statement pursuant to 37 C.F.R. §1.97(e); and

(2) Authorization to charge our Deposit Acct. No. 02-2666 in the amount of $180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: April 3, 2013

/Jacob Aikin/
Jacob T. Aikin
Reg. No. 62,787

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(408) 720-8300

Customer No.: 08791

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Exhibit 1009 - Page 169

Electronic Acknowledgement Receipt	
EFS ID:	15405521
Application Number:	13842879
International Application Number:	
Confirmation Number:	7403
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Customer Number:	8791
Filer:	Jacob T. Aikin/Betty Scaletta
Filer Authorized By:	Jacob T. Aikin
Attorney Docket Number:	9299P027
Receipt Date:	03-APR-2013
Filing Date:	
Time Stamp:	16:40:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	FR1_JP11142878A.pdf	1579548 bb2b9d87b0944c9448eefa1948a2701eb84b1c9a	no	14

Warnings:
Information:

2	Foreign Reference	FR2_WO2011123285A1.pdf	2796282 144a771f0223f82d0421c671ed12292b0e682d38	no	53
Warnings:					
Information:					
3	Non Patent Literature	NPL1_Asano_6pgs.pdf	1431197 ec57dff680fe4a7912c878067ce16f92cf0a6119	no	6
Warnings:					
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4	Non Patent Literature	NPL2_Bower_5pgs.pdf	1697867 6db3535bc54270f9ef7cee170683656363ba40cf	no	5
Warnings:					
Information:					
5	Non Patent Literature	NPL3_CharacteristicsElectrostaticChuck_3pgs.pdf	266300 c1757f281662a7d4191e93597d124ed64b481cbd	no	3
Warnings:					
Information:					
6	Non Patent Literature	NPL4_Guerre_9pgs.pdf	3868252 c7b0d752fb3fde900f1b1769ffcc3ed092ad6c12	no	9
Warnings:					
Information:					
7	Non Patent Literature	NPL5_Han_6pgs.pdf	1097972 12a319a32110a313cf0dd6e144a75e4097884916	no	6
Warnings:					
Information:					
8	Non Patent Literature	NPL6_Harris_1pg.pdf	137293 b90fe7c042cfdbd2dc7b01853ad92928b91171a8	no	1
Warnings:					
Information:					
9	Non Patent Literature	NPL7_Horwitz_10pgs.pdf	2100496 737b6b419ebbef14ea25f1784f9bd6e47b544b88	no	10
Warnings:					
Information:					
10	Non Patent Literature	NPL8_Hossik-Schott_10pgs.pdf	227881 b34ae97a4909578406c8bc44aacd3b7b3d199031	no	10
Warnings:					
Information:					

11	Non Patent Literature	NPL9_Lee_5pgs.pdf	339459 c88aa0b53d355548701550e72ff4fe7d7b171d28	no	5
Warnings:					
Information:					
12	Non Patent Literature	NPL10_Purdue_6pgs.pdf	1360738 a31c7563bb17a3b05f93c5274062b5b4357fca9c	no	6
Warnings:					
Information:					
13	Non Patent Literature	NPL11_Mei_10pgs.pdf	1035737 e090aeb7aa0e4060a47001eef8daa2a7c3e20ee6	no	10
Warnings:					
Information:					
14	Non Patent Literature	NPL12_MERCADO_8pgs.pdf	1035290 bd5258efa065379ee6ba22bdfdd61c7d75f25d31	no	8
Warnings:					
Information:					
15	Non Patent Literature	NPL13_Miskys_24pgs.pdf	3572085 bcdf5ee9ea01a812858f834dd0aa38d7783a11df	no	24
Warnings:					
Information:					
16	Non Patent Literature	NPL14_PrinciplesOfElectrostaticChucks_2pgs.pdf	342191 c0d5fef4c2027cf59285634e280ebf1a57d4bda5	no	2
Warnings:					
Information:					
17	Non Patent Literature	NPL15_Steigerwald_12pgs.pdf	3555784 6f7f8b89bc0860cc533308187377f589f7fa3403	no	12
Warnings:					
Information:					
18	Non Patent Literature	NPL16_WIDAS_waybackmachine_4pgs.pdf	72810 55d2302f1561102dd7cb8d53962bbe7fd7521f5a	no	4
Warnings:					
Information:					
19	Non Patent Literature	NPL17_Geffroy.pdf	744623 182c12a43a30b70b4c495a80c18a7f40627a2809	no	11
Warnings:					
Information:					

20	Non Patent Literature	NPL18_Godha.pdf	355292 70b5227d2c5c7c5a01a4535bfbfb668f2d9aca51	no	4
Warnings:					
Information:					
21	Non Patent Literature	NPL19_Ohara.pdf	520578 9975ede6311ae4869d7c52ec9d1ac56a22aa7ae7	no	6
Warnings:					
Information:					
22	Non Patent Literature	NPL20_Bower.PDF	736339 4edc869853ba2ef0818df0eecb167b00bdffb92a	no	5
Warnings:					
Information:					
23	Non Patent Literature	NPL21_Hekmatshoar.PDF	465091 1ec10b582267f8c828a049896c143a6341453beb	no	6
Warnings:					
Information:					
24	Non Patent Literature	NPL22_Sarma.PDF	722837 33738b8acb5afbe46a7de547ad8ff8de96462252	no	12
Warnings:					
Information:					
25	Non Patent Literature	NPL23_DALSA.PDF	555930 bc6b3696b34bc66ee9d47393f4fa2c183a197b97	no	11
Warnings:					
Information:					
26	Non Patent Literature	NPL24_Kipman.PDF	228688 9ca5b6b09606f2980eb9dafdf15e80d93c73603a	no	4
Warnings:					
Information:					
27	Information Disclosure Statement (IDS) Form (SB08)	9299P027_IDS_SB08_04-03-13.pdf	129196 a29086fd4f384aeaf1ee4f9d7f09fcf37fc38cc1	no	7
Warnings:					
Information:					
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28	Transmittal Letter	9299P027_IDS_LTR_04-03-13.pdf	18803 e5659b687d64e159854ac7ce5a9d0255f4e15f52	no	2

Warnings:	
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Total Files Size (in bytes):	30994559

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PATENT ABSTRACTS OF JAPAN

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(71)Applicant : **SHARP CORP**

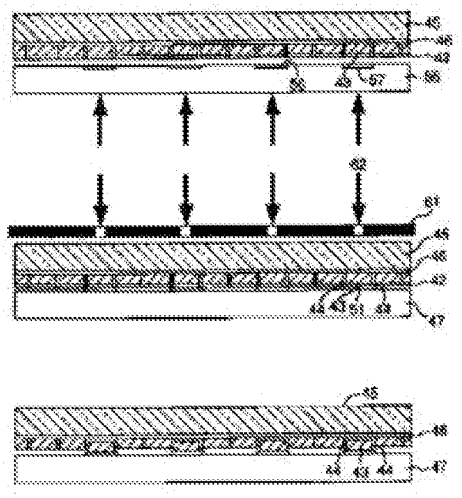
(72)Inventor : **SHIMIZU MASABUMI**

(54) FORMATION OF DISPLAY TRANSISTOR ARRAY PANEL

(57)Abstract:

PROBLEM TO BE SOLVED: To sharply reduce a manufacturing cost.

SOLUTION: Plural TFT elements 43 are formed on a 1st substrate consisting of a Si substrate at pitches dx/m, dy/n with respective element separation grooves 44 intervened. The dx and dy are array pitches of pixels and each of (m) and (n) is a natural number of ≥2. A 2nd substrate 45 is stuck to the 1st substrate with UV peeling resin 46, and after removing the 1st substrate by etching, respective TFT elements 43 are separated. Only TFT elements 43 to be transferred are selectively stuck with adhesive resin 51, and selectively irradiated with ultraviolet rays 62 from the side of the 2nd substrate 45 to selectively be transferred to a 3rd substrate 47. Thus, the same selected TFT element 43 can be transferred to (m×n) pieces of panel substrates 47 while forming (m×n) times as many as a necessary number of TFT elements 43 on one piece of 2nd substrate 45, so that cost required for forming TFT elements 43 on the 1st substrate can be reduced approximately to become 1/(m×n).



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(43)公開日　平成11年(1999)５月28日

(51)Int.Cl.[6]	識別記号	ＦＩ
Ｇ０２Ｆ　1/136	５００	Ｇ０２Ｆ　1/136　５００

審査請求　未請求　請求項の数13　ＯＬ　（全 13 頁）

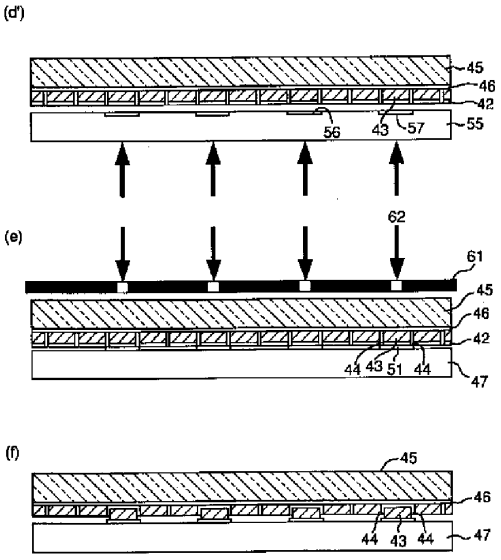
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(71)出願人　000005049
シャープ株式会社
大阪府大阪市阿倍野区長池町22番22号
(72)発明者　清水　正文
大阪府大阪市阿倍野区長池町22番22号　シャープ株式会社内
(74)代理人　弁理士　青山　葆　（外１名）

(54)【発明の名称】　表示用トランジスタアレイパネルの形成方法

(57)【要約】
【課題】　製造コストの大幅な削減を図る。
【解決手段】　Ｓｉ基板で成る第１の基板上に、ＴＦＴ素子４３を素子分離溝４４を隔ててピッチdx/m, dy/nで形成する。dx, dyは画素の配列ピッチであり、m, nは ２」以上の自然数である。さらに、ＵＶ剥離樹脂４６で第２の基板４５を張り付け、第１の基板をエッチング除去した後各ＴＦＴ素子４３を分離させる。そして、第３の基板４７に、接着樹脂５１で転写対象のＴＦＴ素子４３のみを選択的に接着させ、第２の基板４５側から紫外線６２を選択的に照射して転写対象のＴＦＴ素子４３のみを第３の基板４７に選択転写する。こうして、１枚の第２の基板４５上に必要数の(m×n)倍のＴＦＴ素子４３を作成して、(m×n)枚のパネル用基板４７に同一の選択転写を行うことができ、第１の基板上にＴＦＴ素子４３を形成するコストを概略1/(m×n)にできる。



IPR2024-01134 - BOE
Exhibit 1009 - Page 176

【特許請求の範囲】
【請求項１】　基板上に、画素の一方向への配列ピッチｄｘを２以上の自然数ｍで除したｄｘ/ｍのピッチ、および、他方向への配列ピッチｄｙを２以上の自然数ｎで除したｄｙ/ｎのピッチで素子を設ける工程と、
上記基板上に設けられた素子のうち、上記画素の配列ピッチｄｘ，ｄｙに対応する素子のみを選択的に他の基板に転写する工程を備えたことを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項２】　第１の基板上に、画素の一方向への配列ピッチｄｘを２以上の自然数ｍで除したｄｘ/ｍのピッチ、および、他方向への配列ピッチｄｙを２以上の自然数ｎで除したｄｙ/ｎのピッチで素子を形成する工程と、
上記第１の基板上に形成された素子を第２の基板上に全体転写する工程と、
上記第１の基板を除去して、上記素子を上記第２の基板上に孤立配列させる工程と、
上記第２の基板上に転写された素子のうち、上記画素の配列ピッチｄｘ，ｄｙに対応する素子のみを選択的に表示用トランジスタアレイ用の第３の基板に転写する工程を備えたことを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項３】　請求項１あるいは請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記素子が選択転写される基板上の位置には、上記素子が嵌合される凹部が形成されていることを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項４】　請求項１あるいは請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記素子が選択転写される基板上の位置には、接着剤層が選択的に形成されていることを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項５】　請求項１あるいは請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記素子は、順スタガ型の薄膜トランジスタであることを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項６】　請求項１あるいは請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記素子は、逆スタガ型の薄膜トランジスタであることを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項７】　請求項１あるいは請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記素子は、コプレーナ型の薄膜トランジスタであることを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項８】　請求項５乃至請求項７の何れか一つに記載の表示用トランジスタアレイパネルの形成方法において、
上記素子は、配線交差部をも含んでいることを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項９】　請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記第１の基板はシリコン基板であることを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項１０】　請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記第１の基板はガラス基板であることを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項１１】　請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記第１の基板上の素子の上記第２の基板上への全体転写は、光によって接着力が低下する接着剤によって行い、
上記第２の基板上の素子の上記第３の基板上への選択転写は、上記第２の基板の裏面から上記画素の配列ピッチｄｘ，ｄｙに対応する素子の箇所への光照射によって転写の対象となる素子のみを選択的に上記第２の基板から剥離することによって行うことを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項１２】　請求項２に記載の表示用トランジスタアレイパネルの形成方法において、
上記第１の基板上にフッ化水素酸に対して耐性を有する透明絶縁膜を形成し、この透明絶縁膜上に上記素子を形成することを特徴とする表示用トランジスタアレイパネルの形成方法。
【請求項１３】　請求項１２に記載の表示用トランジスタアレイパネルの形成方法において、
上記フッ化水素酸に対して耐性を有する透明絶縁膜は、酸化タンタル膜あるいはダイヤモンド膜の何れ一方であることを特徴とする表示用トランジスタアレイパネルの形成方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は、薄膜トランジスタ(以下、ＴＦＴと言う)等のスイッチング素子を有して、ディスプレイに使用される表示用トランジスタアレイパネルに関する。
【０００２】
【従来の技術】従来、コンピュータやテレビジョン装置等のディスプレイに使用される表示用トランジスタアレイパネルの形成方法として、特開平１－３８７２７号公報(以下、従来例１と言う)やＵＳＰ５４３８２４１(以下、従来例２と言う)に開示されているようなものがある。この表示用トランジスタアレイパネルの形成方法では、シリコン単結晶基板上に単結晶シリコンのＴＦＴアレイを形成し、これを別のパネル用ガラスあるいは透明有機フィルム基板に転写して表示用トランジスタアレイパネルを得ている。

IPR2024-01134 - BOE
Exhibit 1009 - Page 177

【０００３】上記従来例１では、単結晶シリコン薄膜にＴＦＴアレイおよび周辺回路を形成し、ガラス基板上にこの単結晶シリコン薄膜の各辺を互いに密着させて複数枚を平面的に敷き詰めて広い画面を得ている。また、従来例２では、ＳＯＩ技術を使用して第１の基板上に酸化物層を介して薄いシリコン単結晶フィルムを形成し、このシリコン単結晶フィルム上にＴＦＴアレイを作成する。続いて、このＴＦＴアレイをガラス等の第２の透明絶縁基板上に転写し、上記シリコン単結晶フィルムが形成された上記基板全体を除去することで第１の転写プロセスを完了する。また、必要な場合には第２の転写プロセスに移行し、第３のディスプレイパネル基板に転写して表示用ＴＦＴアレイパネルとしている。

【０００４】ここで、上記シリコン単結晶フィルムが形成された基板全体を除去する方法には、図１０に示すような基板とディバイスとの間に剥離層を設けエッチングによって剥離層を除去する方法、あるいは、図１１に示すような基板全体をエッチバック工程によってエッチ除去する方法がある。

【０００５】上記基板下の剥離層を除去する方法では、先ず、半導体基板１の表面側から剥離層２を介してディバイス３を形成する(図１０(a))。そして、ディバイス３上にＵＶ(紫外線)キュアエポキシ４を塗布し(図１０(b))、上記ディバイス３の箇所である残し部６とこの残し部６間で成るエッチング用溝５とを形成する(図１０(c))。こうして、剥離層２除去用のエッチング溶液導入用アクセスストリート構造を得る。次に、上記ＵＶキュアエポキシ３側から透明基板等で成る支持板７を張り合わせてチャネルを形成する(図１０(d))。そして、このチャネルに、矢印(Ａ)で示すようにエッチング溶液を走らせることによって剥離層２を除去し、半導体基板１からディバイス３をリフトオフする。

【０００６】また、上記基板全体をエッチ除去する方法では、図１１(a)に示すように、ディバイス１１が形成されたＳＯＩ構造シリコンウエハ１２を接着剤１３でガラス等の透明絶縁体で成る支持板としての上部基板１４に接着する。このウエハをＫＯＨ(水酸化カリウム)または同等溶液に入れ、酸化物層１５との高い選択比２００：１を利用して図１１(b)に示すようにシリコン基板１６をエッチ除去する。尚、１７は、薄いシリコン単結晶フィルムである。

【０００７】さらに、上記従来例２には、ＧｅＳｉ(シリ化ゲルマニュウム)を中間エッチストップ層としたシリコン薄膜転写法が開示されている(図１２)。このシリコン薄膜転写法においては、図１２(a)に示すように、ＧｅＳｉ層２１を介してディバイス（ＴＦＴ）２２が形成されたシリコンウエハ２３を、図１２(b)に示すように、エポキシ接着剤２４によってガラスまたは他の基板２５にマウントする。そして、ＫＯＨに浸漬して、先ずシリコンウエハ２３のみに選択エッチを行い、次にＧｅＳｉ層２１を別途選択エッチする。

【０００８】また、上記従来例２には、上述の基板から支持板への転写と上記支持板からディスプレイパネル基板への転写との２つの転写方法として、ＵＶ照射によって剥離する性質を有するＵＶ剥離接着剤をテープの両面に塗布したＵＶ剥離両面テープを上記支持板との接着に使用する方法が開示されている(図１３)。この転写方法では、上記支持板からディスプレイパネル基板への転写の場合には、透明支持板２６にＵＶ剥離両面テープ２７によってディバイス２８を転写した後にディバイス２８が形成されていた基板を除去して図１３(a)の状態にする。そうした後に、図１３(b)に示すように、別のＵＶ剥離両面テープ２９にディバイス２８を当接させて透明支持板２６側からＵＶ照射してＵＶ剥離両面テープ２７の接着力を低下させて、ディバイス２８をＵＶ剥離両面テープ２９に転写する。または、図１３(b')に示すように、エポキシ樹脂３０を塗布した基板３１上にディバイス２８を当接させて、透明支持板２６側からＵＶ照射しつつ転写する。

【０００９】さらに、上記従来例２には、基板上に密に形成したディバイスを粗に配置し直す転写方法が開示されている(図１４)。先ず、図１４(a)に示すように、接着剤付きの伸縮性基板３５にディバイス３６を転写した後に、図１４(b)に示すように、各ディバイス３６毎にディバイス３６の間隔と位置とをモニタしながら、伸縮性基板３５をＸ方向へ伸張してＸ方向のディバイス３６の間隔を所定間隔にする。次に、図１４(c)に示すように、伸縮性基板３５をＹ方向へ伸張してＹ方向のディバイス３６の間隔を所定間隔にする。そうした後、ディバイス３６をディスプレイパネル基板(図示せず)に転写する。他の方法として、テープ上のディバイスチップを回転ドラム上の他のテープ上に転写することによって、機械的にディバイス間隔を変換させる方法も開示されている。

【００１０】

【発明が解決しようとする課題】しかしながら、上記従来の表示用トランジスタアレイパネルの形成方法には、以下のような問題がある。

【００１１】すなわち、従来例１では、パネルの高輝度化,高精細化,広視野角化の点で問題がある。すなわち、能動素子(ＴＦＴ)および受動素子(画素電極,補助電極,電極配線等)を同時に形成した複数枚の単結晶シリコン薄膜を、ガラス基板上に敷き詰めている。ところが、従来の張り合わせ材料や精度では、ダイシング加工精度や接着加工精度の点で張り合わせ箇所の余裕代を目的とする素子ピッチの半分にできない。そのために、各単結晶シリコン薄膜のつなぎ目部における透過光量とつなぎ目以外の箇所における透過光量とが異なることになり、例えば視野角によって表示むら等が発生する。したがって、パネルの輝度,精細度,視野角を確保するのに技術的

IPR2024-01134 - BOE
Exhibit 1009 - Page 178

に困難なのである。

【００１２】また、従来例１および従来例２に開示された単結晶シリコン薄膜に形成されたＴＦＴアレイをパネル用基板に転写する方法は、単結晶シリコン薄膜上のＴＦＴ数とパネル用基板上のＴＦＴ数とが１：１の関係に在り、パネル用基板に直接ＴＦＴアレイを作り込む方法に比べて工数が転写プロセス分だけ増加することになり、コストがアップするという問題がある。

【００１３】また、従来例２に開示されている基板上に密に形成したディバイスを粗に配置し直す転写方法は、伸縮性基板の伸長時の不動点(支点)がディバイスチップの接着面のどの位置になるかによって、ディバイス位置が最小でチップサイズ(≧２０μm)だけずれるという本質的な問題を抱えている。そのために、ディバイスチップ毎の精密位置制御が不可欠になる。したがって、少なくとも１μm程度の位置合わせ精度が必要な高精細ＴＦＴアレイパネルの形成には、ＴＦＴディバイスチップ毎の位置計測と制御を含む位置合わせに多大な時間を要する。さらに、熱膨張係数の大きな樹脂フィルムへの転写の場合には、位置決め前後の温度/応力変動によって位置合わせ精度が損なわれ易い。以上の理由から、量産技術として採用することには極めて大きな問題がある。

【００１４】そこで、この発明の目的は、製造コストの大幅な削減を可能にする表示用トランジスタアレイパネルの形成方法を提供することにある。

【００１５】

【課題を解決するための手段】上記目的を達成するため、請求項１に係る発明の表示用トランジスタアレイパネルの形成方法は、基板上に,画素の一方向への配列ピッチｄxを２以上の自然数mで除したｄx/mのピッチ,および,他方向への配列ピッチｄyを２以上の自然数ｎで除したｄy/ｎのピッチで素子を設ける工程と、上記基板上に設けられた素子のうち,上記画素の配列ピッチｄx,ｄyに対応する素子のみを選択的に他の基板に転写する工程を備えたことを特徴としている。

【００１６】上記構成によれば、最終的に表示用トランジスタアレイに形成される画素数の(ｍ×ｎ)倍の素子が基板上に設けられている。したがって、上記素子が設けられた１枚の基板から(ｍ×ｎ)枚の表示用トランジスタアレイパネルを形成することが可能となり、上記素子を形成する場合のコストが１/(ｍ×ｎ)に低減される。

【００１７】さらに、上記構成によれば、上記素子が設けられた１枚の基板から他の基板上への素子の選択転写を(ｍ×ｎ)回繰り返すことによって、上記素子の一方向への配列ピッチがｄxであり、他方向への配列ピッチがｄyであると共に、上記素子が形成設けられていた基板の大きさの(ｍ×ｎ)倍の大きさの上記他の基板が得られる。こうして、上記素子の形成に要する材料費が低減される。

【００１８】また、請求項２に係る発明の表示用トランジスタアレイパネルの形成方法は、第１の基板上に,画素の一方向への配列ピッチｄxを２以上の自然数mで除したｄx/mのピッチ,および,他方向への配列ピッチｄyを２以上の自然数ｎで除したｄy/ｎのピッチで素子を形成する工程と、上記第１の基板上に形成された素子を第２の基板上に全体転写する工程と、上記第１の基板を除去して上記素子を上記第２の基板上に孤立配列させる工程と、記第２の基板上に転写された素子のうち,上記画素の配列ピッチｄx,ｄyに対応する素子のみを選択的に表示用トランジスタアレイ用の第３の基板に転写する工程を備えたことを特徴としている。

【００１９】上記構成によれば、最終的に表示用トランジスタアレイ用の第３の基板上に形成される画素数の(ｍ×ｎ)倍の素子が、第１の基板上に形成されている。したがって、上記素子が形成された１枚の第１の基板から(ｍ×ｎ)枚の第３の基板を形成することが可能となり、上記第１の基板上への素子形成コストが１/(ｍ×ｎ)に低減される。

【００２０】また、請求項３に係る発明は、請求項１あるいは請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記素子が選択転写される基板上の位置には、上記素子が嵌合される凹部が形成されていることを特徴としている。

【００２１】上記構成によれば、上記素子が選択転写される基板上の位置には凹部が形成されているので、上記凹部に接着剤層を形成することによって、上記素子の選択転写が更に容易に行われる。

【００２２】また、請求項４に係る発明は、請求項１あるいは請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記素子が選択転写される基板上の位置には、接着剤層が選択的に形成されていることを特徴としている。

【００２３】上記構成によれば、上記素子が選択転写される基板上の位置に接着剤層が選択的に形成されているので、上記素子の選択転写が更に容易に行われる。

【００２４】また、請求項５に係る発明は、請求項１あるいは請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記素子は順スタガ型のＴＦＴであることを特徴としている。

【００２５】上記構成によれば、基板上への順スタガ型ＴＦＴの形成コストが１/(ｍ×ｎ)に低減される。

【００２６】また、請求項６に係る発明は、請求項１あるいは請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記素子は逆スタガ型のＴＦＴであることを特徴としている。

【００２７】上記構成によれば、上記基板上への逆スタガ型ＴＦＴの形成コストが１/(ｍ×ｎ)に低減される。

【００２８】また、請求項７に係る発明は、請求項１あるいは請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記素子はコプレーナ型の

IPR2024-01134 - BOE
Exhibit 1009 - Page 179

ＴＦＴであることを特徴としている。

【００２９】上記構成によれば、上記基板上へのコプレーナ型ＴＦＴの形成コストが１/(ｍ×ｎ)に低減される。

【００３０】また、請求項８に係る発明は、請求項５乃至請求項７の何れか一つに係る発明の表示用トランジスタアレイパネルの形成方法において、上記素子は配線交差部をも含んでいることを特徴としている。

【００３１】上記構成によれば、上記基板上への配線交差部をも含むＴＦＴの形成コストが１/（ｍ×ｎ）に低減される。

【００３２】また、請求項９に係る発明は、請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記第１の基板はシリコン基板であることを特徴としている。

【００３３】上記構成によれば、上記第１の基板はシリコン基板であるから上記素子を高密度に形成できる。したがって、上記自然数ｍ，ｎを容易に大きくすることが可能となり、上記第１の基板上への素子形成コストが大幅に低減される。

【００３４】また、請求項１０に係る発明は、請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記第１の基板はガラス基板であることを特徴としている。

【００３５】上記構成によれば、上記第１の基板はガラス基板であるから、大型の第１の基板の形成が可能となり、大型の表示用トランジスタアレイパネルが容易に形成される。

【００３６】また、請求項１１に係る発明は、請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記第１の基板上の素子の上記第２の基板上への全体転写は，光によって接着力が低下する接着剤によって行い、上記第２の基板上の素子の上記第３の基板上への選択転写は，上記第２の基板の裏面から上記画素の配列ピッチｄｘ，ｄｙに対応する素子の箇所への光照射によって転写の対象となる素子のみを選択的に上記第２の基板から剥離することによって行うことを特徴としている。

【００３７】上記構成によれば、光によって接着力が低下する接着剤の塗布および上記第２の基板の裏面からの光の選択照射という簡単な方法によって、上記第２の基板上の素子の上記第３の基板上への選択転写が行われる。

【００３８】また、請求項１２に係る発明は、請求項２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記第１の基板上にフッ化水素酸に対して耐性を有する透明絶縁膜を形成し、この透明絶縁膜上に上記素子を形成することを特徴としている。

【００３９】上記構成によれば、上記第１の基板の除去に際して、エッチャントとしてフッ化水素酸が使用された場合に、フッ化水素酸に対して耐性を有する透明絶縁膜の存在によって上記素子が保護される。

【００４０】また、請求項１３に係る発明は、請求項１２に係る発明の表示用トランジスタアレイパネルの形成方法において、上記フッ化水素酸に対して耐性を有する透明絶縁膜は、酸化タンタル膜あるいはダイヤモンド膜の何れ一方であることを特徴としている。

【００４１】上記構成によれば、上記第１の基板除去用のエッチャントとしてフッ化水素酸が使用された場合に、酸化タンタル膜あるいはダイヤモンド膜の何れ一方の存在によって上記素子が確実に保護される。

【００４２】

【発明の実施の形態】以下、この発明を図示の実施の形態により詳細に説明する。

【００４３】＜第１実施の形態＞図１および図２は、本実施の形態の表示用トランジスタアレイパネルの形成方法における手順を示す図である。本実施の形態においては、第１の基板としてシリコン(Ｓｉ)基板を用いている。

【００４４】図１(a)に示すように、上記第１の基板としてのＳｉ基板４１上に透明絶縁膜としてＳｉ酸化膜４２を形成した後、ｉ線スパッタを用いたフォトプロセスを含む公知の素子形成プロセスを行って、ＴＦＴ素子４３を素子分離溝４４を隔てて所定のピッチで形成する。ここで、上記ピッチは、目的とする表示用トランジスタアレイパネルの画素ドットの配列ピッチｄｘ，ｄｙを、２」以上の自然数ｍ，ｎで除した値ｄｘ/ｍ，ｄｙ/ｎである。また、形成するＴＦＴ素子４３は、例えばＴＦＴと周辺電極配線の一部を含むものであるが、画素電極は含まない。尚、形成するＴＦＴの構造については後に詳述する。

【００４５】次に、図１(b)に示すように、上記ＴＦＴ素子４３側にＵＶ剥離樹脂４６を塗布し、第２の基板である光透過性基板としてのガラス基板４５を張り付ける。ここで、ＵＶ剥離樹脂４６としては、シリコン(メタ)アクリレート添加のアクリル系樹脂や紫外線照射で接着力が低下するＵＶ硬化型粘着剤等を用いる。次に、図１(c)に示すように、Ｓｉ基板(第１の基板)４１をＫＯＨでエッチング除去した後に、ＴＦＴ素子分離溝４４の箇所のＳｉ酸化膜４２に対してＴＦＴ素子分離エッチングを行って個々のＴＦＴ素子４３を孤立した状態にする。

【００４６】次に、図１(d)に示すように、ＴＦＴパネル用の第３の基板であるガラス基板４７に接着樹脂４８を塗布したものを、アライメントを行いつつガラス基板(第２の基板)４５に近接させる。そして、フォトマスク４９を用いて、接着樹脂４８における転写の対象となる(後に画素を構成する)ＴＦＴ素子４３の箇所に位置する部分を紫外線５０を照射して半硬化させて接着性を高め、その半硬化部分５１を転写対象のＴＦＴ素子４３に

IPR2024-01134 - BOE
Exhibit 1009 - Page 180

押し付けてガラス基板(第３の基板)４７を貼り合わせる。尚、接着樹脂４８としては、例えばアクリレート系のＵＶ硬化樹脂やＵＶ硬化エポキシ系樹脂等を用いる。

【００４７】また、上記第３の基板を貼り合わせる方法として、図２(d')に示す方法を用いても差し支えない。すなわち、第３の基板５５における転写対象のＴＦＴ素子４３の箇所に位置する部分を、例えばCF_4やCHF_3を用いたドライエッチ(ＲＩＥ)によって、ＴＦＴ素子４３のチップが入るサイズの凹部５６を形成し、この凹部５６のみに予め接着樹脂５７を塗布しておく。そして、凹部５６に転写対象のＴＦＴ素子４３を嵌合して第３の基板５５を貼り合わせるのである。

【００４８】次に、図２(e)に示すように、フォトマスク６１を用いて、ガラス基板４５(第２の基板：光透過性基板)側から、ＵＶ剥離樹脂４６における転写対象のＴＦＴ素子４３の箇所の部分に紫外線６２を選択的に照射して、ＵＶ剥離樹脂４６の接着力を低下させてＴＦＴ素子４３との密着性を低減させる。

【００４９】以上の処理によって、上記転写対象のＴＦＴ素子４３は隣接しているＴＦＴ素子４３とは孤立しており、ガラス基板(第２の基板)４５との間のＵＶ剥離樹脂４６は接着力が低下している。したがって、図２(f)に示すように、パネル用のガラス基板(第３の基板)４７に転写対象のＴＦＴ素子４３のみが移し取られる(転写接着)される。そして、未露光のＴＦＴ素子４３は、ガラス基板(第３の基板)４７に転写接着されない。尚、未露光の接着樹脂４８は選択転写後に除去しておく。

【００５０】最後に、受動素子部形成プロセスを行う。この受動素子部形成プロセスでは、図３に示すように、上記パネル用のガラス基板(第３の基板)４７上に画素ドットの配列ピッチdx, dyで転写接着されたＴＦＴ素子４３に、データ信号線６５に接続するためのソース電極配線６６,走査信号線６７に接続するためのゲート電極配線６８およびドレイン電極配線６９を配線する。さらに、ドレイン電極配線６９に接続される液晶駆動用の画素電極７０を形成する。その場合の配線間絶縁膜として、例えばポリイミド膜を用いる。そして、上述の図１(c)におけるＴＦＴ素子分離エッチング等の際にＴＦＴ素子４３を保護するためにＴＦＴ素子４３を覆って形成されている例えばＳｉ酸化膜(図示せず)に、電極接続用のコンタクトホールを穴あけエッチングで形成する。そして、ガラス基板(第３の基板)４７上のデータ信号線６５や走査信号線６７とＴＦＴ素子４３の電極との接続等を行う。

【００５１】こうして、図４に示すような表示用トランジスタアレイパネルが形成される。尚、７１はカラーフィルタガラス基板であり、７２はＲＧＢのカラーフィルタである。また、上記配線６５～６９および画素電極７０は、ＴＦＴ素子４３が転写接着される前に、予めガラス基板(第３の基板)４７上に形成しておいても構わない。

【００５２】従来より、表示用トランジスタアレイパネルに採用されているＴＦＴ素子の構造として、順スタガ構造,逆スタガ構造およびコプレーナ構造の３種類がある。図５は順スタガＴＦＴの構造の一例を示し、図５(a)は断面図であり、図５(b)は平面図である。順スタガＴＦＴでは、ゲート電極８１が、ソース電極８２下のオーミック コンタクト層８３とドレイン電極８４下のオーミック コンタクト層８５とに接続するチャネル層８６の上側に、ゲート絶縁膜８７を介して形成されている。尚、８９は、上記選択転写後の配線プロセスにおいてＳｉ酸化膜８８に形成されるゲート電極７１に対するコンタクトホールである。同様に、９０はソース電極８２に対するコンタクトホールであり、９１はドレイン電極８４に対するコンタクトホールである。

【００５３】また、図６は、上記逆スタガＴＦＴの構造の一例の断面図を示す。逆スタガＴＦＴでは、ゲート電極１０１が、ソース電極１０２とドレイン電極１０３とに接続するチャネル層１０４の下側に、ゲート絶縁膜１０５及び金属酸化膜１０６を介して形成されている。尚、１０７,１０８はオーミック コンタクト層であり、１１０はＳｉ酸化膜１０９に形成されたソース電極１０２に対するコンタクトホールであり、１１１はドレイン電極１０３に対するコンタクトホールである。

【００５４】また、図７は、上記コプレーナＴＦＴの構造の断面図を示す。コプレーナＴＦＴでは、ゲート電極１２１が、ソース電極１２２とドレイン電極１２３とを接続するオーミック コンタクト層１２４の中間部に形成されるチャネル層１２５の上側に、ゲート絶縁膜１２６を介して形成されている。尚、１２８はＳｉ酸化膜１２７に形成されたソース電極１２２に対するコンタクトホールであり、１２９はドレイン電極１２３に対するコンタクトホールである。

【００５５】上記順スタガＴＦＴ,逆スタガＴＦＴおよびコプレーナＴＦＴの何れの場合にも、ガラス基板(第２の基板)４５への全体転写後におけるＮａＯＨ(水酸化ナトリウム)あるいはＫＯＨをエッチャントとしたＳｉ基板(第１の基板)４１への選択エッチングを行う際に、上記エッチャントに耐性のあるＳｉ酸化膜４２でＴＦＴが保護される構成になっている。したがって、何れの構成の場合も、本実施の形態の表示用トランジスタアレイパネルの形成方法が適用可能である。尚、上記保護膜４２は、Ｓｉ酸化膜に限定されるものではなく、第１の基板に対する選択エッチング時に使用されるエッチャントに対して耐性を有する膜であればよい。例えば、第１の基板がガラス基板である場合には、エッチャントとしてのフッ化水素酸に対して耐性を有する酸化タンタル膜あるいはダイアモンド膜を上記保護膜として上記ガラス基板とＴＦＴとの間に形成すればよい。尚、上記保護膜は、上記第１の基板とＴＦＴとの間のみならず、図５～図７

IPR2024-01134 - BOE
Exhibit 1009 - Page 181

に示すように、ＴＦＴの表面および側面にも形成することが望ましい。

【００５６】尚、図８は、図６に示す逆スタガＴＦＴにおけるソース電極１０２に接続されたソース電極配線１１５とゲート電極配線１１６との交差部１１５の断面図である。このようなソース電極配線１１５とゲート電極配線１１６との交差部１１５も、ＴＦＴ素子４３に含めて、第３の基板４７上に選択転写することが可能である。

【００５７】上述のように、本実施の形態においては、Ｓｉ基板で成る第１の基板４１上にＴＦＴ素子４３を素子分離溝４４を隔ててピッチｄｘ/ｍ，ｄｙ/ｎで形成する。ここで、ｄｘ，ｄｙは画素ドットの配列ピッチであり、ｍ，ｎは ２」以上の自然数である。そして、ＴＦＴ素子４３側にＵＶ剥離樹脂４６で第２の基板４５を張り付けた後、第１の基板４１をエッチング除去し、ＴＦＴ素子分離エッチングを行って各ＴＦＴ素子４３を分離させる。そして、第３の基板４７に接着樹脂４８で転写対象のＴＦＴ素子４３のみを選択的に接着させ、第２の基板４５側から転写対象のＴＦＴ素子４３の箇所に紫外線６２を選択的に照射してＵＶ剥離樹脂４６の接着力を低下させて、転写対象の(つまり、画素を構成する)ＴＦＴ素子４３のみを第３の基板４７に選択転写するのである。

【００５８】したがって、上記第２の基板４５上のＴＦＴ素子４３のピッチｄｘ/ｍ，ｄｙ/ｎの第３の基板４７上でのピッチｄｘ，ｄｙへの拡大を、従来例２の如く伸縮性基板を用いる転写方法に比して正確に行うことができる。したがって、１枚の第２の基板４５を用いて、この第２の基板４５から第３の基板(パネル用基板)４７への選択転写を、第２の基板４５をｘ方向へｄｘ/ｍあるいはｙ方向へｄｙ/ｎだけ移動させながら(ｍ×ｎ)枚の第３の基板４７に対して行うことによって、第１の基板４１を１枚作成すれば、(ｍ×ｎ)枚のパネル用基板４７に対して同一の選択転写を行うことができる。すなわち、本実施の形態によれば、第１の基板４１上にＴＦＴ素子４３を形成するコストを概略１/(ｍ×ｎ)にできる。

【００５９】このように、本実施の形態によれば、表示用トランジスタアレイパネルとして必要な画素数のｍ，ｎ倍のＴＦＴ素子を第１の基板４１上に形成することが可能となる。したがって、必要画素数と第１の基板上のＴＦＴ素子数とが同数の従来の表示用トランジスタアレイパネルの形成方法に比して、第１の基板４１に形成するＴＦＴ素子密度を１０倍～１００倍にできる。したがって、表示用トランジスタアレイパネル製造設備におけるイニシャルコストの約３０％を占める成膜工程設備および約２６％を占めるフォト工程設備のスループットを、実質的に１０倍～１００倍程度向上させることができる。また、ＴＦＴ素子４３の形成に要する材料費も１/１０～１/１００に低減できる。結果として、表示用トランジスタアレイパネルの製造コストの大幅な削減が可能となるのである。

【００６０】ところで、上記第１の基板４１としてＳｉ基板を用いた場合には、基板サイズに制限があるもののＴＦＴ素子を高密度に形成できる。そこで、以下のようにして、上記基板サイズの制限を超えたサイズの第３の基板４７を形成することができる。すなわち、ＴＦＴ素子４３が高密度で形成されたＳｉ基板(第１の基板)４１を複数枚形成する。そして、この複数枚のＳｉ基板(第１の基板)４１の位置をずらして第２の基板４５に全体転写することによって、ＴＦＴ素子４３が高密度で転写された(つまり、自然数ｍ，ｎが大きい)第２の基板４５を形成するのである。

【００６１】上記ガラス基板(第２の基板)４５に、複数枚のＳｉ基板(第１の基板)４１上のＴＦＴ素子４３を転写する場合には、図１(ａ)～図１(ｃ)に示す第１の基板４１から第２の基板４５への転写プロセスに従って、１枚の第１の基板４１毎にアライメントしつつ第１の基板４１の枚数だけ転写を繰り返して行えばよい。こうすることによって、複数枚の第１の基板４１上のＴＦＴ素子４３を１０μｍ以下の間隔で第２の基板４５上に転写することが可能となる。従来例１の如く、複数枚の第１の基板を第２の基板上に敷き詰める方法の場合には、第１の基板形成時のダイシング加工精度や第２の基板への接着加工精度の点で、各素子を１０μｍ以下の間隔で配列することは一般には困難である。ところが、本実施の形態の場合には、第１の基板４１の枚数だけ第２の基板４５への転写を繰り返せば、ＴＦＴ素子４３を１０μｍ以下の間隔で第２の基板４５上に配列することは簡単にできるのである。

【００６２】上述の場合、上記第１の基板４１から第２の基板４５への全体転写の回数が増加する。しかしながら、ＴＦＴ素子４３は高密度に形成されているために自然数ｍ，ｎの値は大きく、１枚の第２の基板４５から多数の第３の基板４７を形成できる。したがって、上記全体転写によるコストアップを埋めて、尚且つコストダウンを図ることができるのである。

【００６３】尚、上記実施の形態においては 紫外線に対するＵＶ剥離樹脂の性質を利用して選択転写を行っている。しかしながら、この発明はこれに限定されるものではなく、例えば、転写側の基板の一方側，他方側あるいは両側からの静電引力や電磁力を利用して選択転写を行っても差し支えない。

【００６４】＜第２実施の形態＞図９は、本実施の形態の表示用トランジスタアレイパネルの形成方法における手順を示す図である。本実施の形態においては、第１の基板としてガラス基板を用いている。

【００６５】図９(ａ)に示すように、上記第１の基板としてのガラス基板１３１上に、例えばＳｉ膜１３２とＳｉ窒化膜(あるいはＳｉ酸化膜)１３３との２層構造で成る

IPR2024-01134 - BOE
Exhibit 1009 - Page 182

犠牲層１３４を形成する。そうした後、ｉ線スパッタを用いたフォトプロセスを含む公知の素子形成プロセスを行って、ＴＦＴ素子１３５を素子分離溝１３６を隔てて所定のピッチで形成する。ここで、上記ピッチは、目的とする表示用トランジスタアレイパネルの画素ドットの配列ピッチdx,dyを、２以上の自然数m,nで除した値dx/m,dy/nである。また、形成するＴＦＴ素子１３５は、例えばＴＦＴと周辺電極配線の一部を含むものであるが、画素電極は含まない。尚、形成するＴＦＴの構造は、上述の順スタガＴＦＴ,逆スタガＴＦＴおよびコプレーナＴＦＴの何れかである。

【００６６】次に、図９(b)に示すように、上記ＴＦＴ素子１３５側にＵＶ剥離樹脂１３７を塗布し、第２の基板である光透過性基板としてのガラス基板１３８を張り付ける。次に、図９(c)に示すように、例えばバッファフッ酸等のSiとの選択比が大きな選択エッチング液１３９を、真空吸入法によってＴＦＴ素子分離溝１３６に均一に充填する。こうして、犠牲層１３４におけるSi窒化膜(あるいはSi酸化膜)１３３のみを選択エッチングして除去する。

【００６７】次に、図９(d)に示すように、上記ガラス基板(第１の基板)１３１を取り外して、各ＴＦＴ素子１３５をガラス基板(第２の基板)１３８上に孤立した状態にする。

【００６８】以下、第１実施の形態における図１(d)～図２(f)に示す手順によって、ＴＦＴパネル用の第３の基板であるガラス基板の張り合わせ、ガラス基板(第２の基板)１３８上のＴＦＴ素子１３５の第３の基板(パネル用基板)上への選択転写を行うのである。

【００６９】上述のように、本実施の形態においては、上記ガラス基板(第１の基板)１３１上に、Si膜１３２とSi窒化膜(またはSi酸化膜)１３３とで成る犠牲層１２４を介してＴＦＴ素子１３５を素子分離溝１３６を隔てて、ピッチdx/m,dy/nで形成する。ここで、dx,dyは画素ドットの配列ピッチであり、m,nは２以上の自然数である。そして、ＴＦＴ素子１３５側にＵＶ剥離樹脂１３７で第２の基板１３８を張り付けた後、Siとの選択比が大きな選択エッチング液１３９を真空吸入法でＴＦＴ素子分離溝１３６に充填して犠牲層１３４のSi窒化膜(あるいはSi酸化膜)１３３のみを選択エッチングし、ガラス基板(第１の基板)１３１を除去する。そうした後、第１実施の形態と同様にして、転写対象の(つまり、画素を構成する)ＴＦＴ素子１３５のみを第３の基板に選択転写するのである。

【００７０】したがって、第１実施の形態と同じ効果を奏する表示用トランジスタアレイパネルの形成方法を、ガラス基板を上記第１の基板とする場合にも適用できる。ところで、第１の基板１３１としてガラス基板を用いた場合には、通常は基板サイズに制限は無く大型の基板を形成できる。したがって、dx/m,dy/nのピッチでＴＦＴ素子１３５が形成された大型のガラス基板(第１の基板)１３１を形成することによって、大型の表示用トランジスタアレイパネルを容易に形成できるのである。

【００７１】そして、本実施の形態においても、１枚の第２の基板１３８を用いて、この第２の基板１３８から第３の基板(パネル用基板)への選択転写を、第２の基板１３８をｘ方向へdx/mあるいはｙ方向へdy/nだけ移動させながら(m×n)枚の第３の基板に対して行うことによって、第１の基板１３１を１枚作成すれば、(m×n)枚のパネル用基板に同一の選択転写を行うことができる。すなわち、本実施の形態によれば、第１の基板１３１上にＴＦＴ素子１３５を形成するコストを概略1/(m×n)にできるのである。

【００７２】例えば、１３.３インチＸＧＡ(Extended Graphics Array)－ＬＣＤ(液晶ディスプレイ)パネルに適用した場合には、パネルサイズ２０３×２７０＝５４,８１０㎟の中にＲＧＢ合計で７６８×１０２４＝２,３５９,３００個のＴＦＴ素子を内蔵しており、ＴＦＴ素子１３５の縦横夫々の配列ピッチnは、概略８８μm,２６４μmである。ここで、m＝４,n＝１２を選択して第１の基板１３１上へのＴＦＴ素子１３５の配列ピッチを２２μmとした場合には、ＴＦＴ素子１３５が全体転写された第２の基板１３８上のＴＦＴ素子１３５の配列ピッチは、表示用ＬＣＤパネルに比して縦４倍,横１２倍であるために、１枚の第２の基板１２８から４×１２＝４８枚の表示用ＬＣＤパネルを形成できる。したがって、プロセスコストの大幅な削減を図ることができるのである。

【００７３】こうして、本実施の形態においても、第１実施の形態と同様に、表示用トランジスタアレイパネル製造設備におけるイニシャルコストの約３０％を占める成膜工程設備および約２６％を占めるフォト工程設備のスループットを、実質的に１０倍～１００倍程度向上させることができる。また、ＴＦＴ素子４３の形成に要する材料費も1/１０～1/１００に低減できる。結果として、表示用トランジスタアレイパネルの製造コストの大幅な削減が可能となるのである。

【００７４】<第３実施の形態>上記各実施の形態においては、一つの基板上のＴＦＴ素子の他の基板への選択転写を、第２の基板４５,１３８から第３の基板４７への転写に適用している。しかしながら、上記選択転写は、第１の基板から第２の基板への転写に適用することも可能である。

【００７５】すなわち、第１実施の形態における図１(a)あるいは第２実施の形態における図９(a)と同様にして、第１の基板上に、画素の一方向への配列ピッチdxおよび他方向への配列ピッチdyを２以上の自然数m,nで除した値dx/m,dy/nのピッチで第１の基板上にＴＦＴ素子を１枚形成する。そして、上記１枚の第１の

IPR2024-01134 - BOE
Exhibit 1009 - Page 183

基板から上記第２の基板上へのＴＦＴ素子の選択転写を、アライメントを行って(ｍ×ｎ)回繰り返す。こうして、上記ＴＦＴ素子の上記一方向への配列ピッチがｄｘであり、他方向への配列ピッチがｄｙであり、且つ、上記第１の基板の大きさの(ｍ×ｎ)倍の大きさの第２の基板を得るのである。以後は、この第２の基板上のＴＦＴ素子を第３の基板上に全体転写すればよい。

【００７６】こうすることによって、上記第１の基板が基板サイズに制限のあるＳｉ基板である場合でも、上記制限を越えた大きさの表示用トランジスタアレイパネルの形成が可能となるのである。上記第１の基板は、Ｓｉ基板に限らずガラス基板であっても差し支えない。

【００７７】尚、本実施の形態を適用する場合には、上記第１の基板とＴＦＴ素子との間に形成される透明絶縁膜下に、例えば、紫外線照射で接着力が低下するＵＶ硬化型粘着剤等を形成して、上記第１の基板からＴＦＴ素子を選択的に剥離可能にする必要がある。また、場合によっては、第３の基板への全体転写は無くとも構わない。

【００７８】

【発明の効果】以上より明らかなように、請求項１に係る発明の表示用トランジスタアレイパネルの形成方法は、画素の一方向への配列ピッチｄｘ及び他方向への配列ピッチｄｙを２以上の自然数ｍ，ｎで除したｄｘ/ｍ，ｄｙ/ｎのピッチで基板上に素子を設ける工程と、上記基板上に設けられた素子のうち上記画素の配列ピッチｄｘ，ｄｙに対応する素子のみを選択的に他の基板に転写する工程を備えたので、転写元の基板上には、表示用トランジスタアレイパネルに形成される画素数の(ｍ×ｎ)倍の素子が設けられている。したがって、上記転写元の１枚の基板から(ｍ×ｎ)枚の表示用トランジスタアレイパネルを形成することができる。

【００７９】すなわち、この発明によれば、基板上への素子形成コストを、基板上に形成される素子数と上記画素数とが同数である従来の表示用トランジスタアレイパネルの形成方法に比較して１/(ｍ×ｎ)に低減できる。したがって、表示用トランジスタアレイパネル製造設備におけるイニシャルコストの約３０％を占める成膜工程設備および約２６％を占めるフォト工程設備のスループットを、実質的に(ｍ×ｎ)倍に向上させることができる。また、上記素子の形成に要する材料費を１/(ｍ×ｎ)に低減できる。結果として、表示用トランジスタアレイパネルの製造コストの大幅な削減が可能となるのである。

【００８０】さらに、上記素子が設けられた１枚の基板から他の基板上への素子の選択転写を(ｍ×ｎ)回繰り返すことによって、上記素子の一方向への配列ピッチがｄｘであり、他方向への配列ピッチがｄｙであると共に、上記転写元の基板の大きさの（ｍ×ｎ)倍の大きさの表示用トランジタアレイパネルを得ることができる。したがって、この場合には、上記従来の表示用トランジスタアレイパネルの形成方法によって同じ大きさの表示用トランジスタアレイパネルを形成する場合に比較して、上記素子の形成に要する材料費を低減できる。

【００８１】また、請求項２に係る発明の表示用トランジスタアレイパネルの形成方法は、画素の一方向への配列ピッチｄｘおよび他方向への配列ピッチｄｙを２以上の自然数ｍ，ｎで除した値ｄｘ/ｍ，ｄｙ/ｎのピッチで第１の基板上に素子を形成する工程と、上記第１の基板上に形成された素子を第２の基板上に全体転写する工程と、上記第１の基板を除去して上記素子を第２の基板上に孤立配列させる工程と、記第２の基板上に転写された素子のうち上記画素の配列ピッチｄｘ，ｄｙに対応する素子のみを選択的に表示用トランジスタアレイ用の第３の基板に転写する工程を備えたので、上記第１の基板上には、表示用トランジスタアレイ用の第３の基板に形成される画素数の(ｍ×ｎ)倍の素子が形成されている。したがって、上記素子が形成された１枚の第１の基板から(ｍ×ｎ)枚の第３の基板を形成することができる。

【００８２】すなわち、この発明によれば、第１の基板上への素子形成コストを、上記第１の基板上に形成される素子数と上記第３の基板に形成される画素数とが同数である従来の表示用トランジスタアレイパネルの形成方法に比較して１/(ｍ×ｎ)に低減できる。特に、上記第１の基板がＳｉ基板である場合には、上記第１の基板上に従来の１０倍～１００倍の素子を形成することができ、表示用トランジスタアレイパネルの製造コストの大幅な削減が可能となるのである。

【００８３】また、請求項３に係る発明の表示用トランジスタアレイパネルの形成方法は、上記素子が選択転写される基板上の位置には上記素子が嵌合される凹部が形成されているので、上記凹部に接着剤層を形成することによって、上記素子の選択転写を更に容易に行うことができる。

【００８４】また、請求項４に係る発明の表示用トランジスタアレイパネルの形成方法は、上記素子が選択転写される基板上の位置に接着剤層が選択的に形成されているので、上記素子の選択転写を更に容易に行うことができる。

【００８５】また、請求項５に係る発明の表示用トランジスタアレイパネルの形成方法における上記素子は順スタガ型のＴＦＴであるので、基板上への上記順スタガ型ＴＦＴの形成コストを１/(ｍ×ｎ)に低減できる。

【００８６】また、請求項６に係る発明の表示用トランジスタアレイパネルの形成方法における上記素子は逆スタガ型のＴＦＴであるので、基板上への上記逆スタガ型ＴＦＴの形成コストを１/(ｍ×ｎ)に低減できる。

【００８７】また、請求項７に係る発明の表示用トランジスタアレイパネルの形成方法における上記素子はコプレーナ型のＴＦＴであるので、基板上への上記コプレー

IPR2024-01134 - BOE
Exhibit 1009 - Page 184

ナ型ＴＦＴの形成コストを１/(ｍ×ｎ)に低減できる。

【００８８】また、請求項８に係る発明の表示用トランジスタアレイパネルの形成方法における上記素子は配線交差部をも含んでいるので、基板上への上記配線交差部をも含むＴＦＴの形成コストを１/(ｍ×ｎ)に低減できる。

【００８９】また、請求項９に係る発明の表示用トランジスタアレイパネルの形成方法における上記第１の基板はシリコン基板であるので上記素子を高密度に形成できる。したがって、上記自然数ｍ，ｎを容易に大きくすることが可能となり、上記第１の基板上への素子形成コストを大幅に低減できる。

【００９０】また、請求項１０に係る発明の表示用トランジスタアレイパネルの形成方法における上記第１の基板はガラス基板であるので、上記第１の基板を大型に形成できる。したがって、この発明によれば、上記第１の基板上への素子形成コストを１/(ｍ×ｎ)に低減でき、且つ、大型の表示用トランジスタアレイパネルを容易に形成できる。

【００９１】また、請求項１１に係る発明の表示用トランジスタアレイパネルの形成方法では、上記第１の基板上の素子の上記第２の基板上への全体転写を、光で接着力が低下する接着剤によって行い、上記第２の基板上の素子の上記第３の基板上への選択転写を、上記第２の基板の裏面から転写対象の素子の箇所への選択的な光照射によって行うので、上記接着剤の塗布および上記第２の基板の裏面からの光の選択照射という簡単な方法によって、上記第２の基板上の素子の上記第３の基板上への選択転写を行うことできる。

【００９２】また、請求項１２に係る発明の表示用トランジスタアレイパネルの形成方法では、上記第１の基板上にフッ化水素酸に対して耐性を有する透明絶縁膜を形成しているので、上記第１の基板の除去に際してエッチャントとしてフッ化水素酸を使用する場合に、上記透明絶縁膜の存在によって上記素子を保護できる。

【００９３】また、請求項１３に係る発明の表示用トランジスタアレイパネルの形成方法では、上記フッ化水素酸に対して耐性を有する透明絶縁膜は酸化タンタル膜あるいはダイヤモンド膜の何れ一方であるので、上記第１の基板除去用のエッチャントとしてフッ化水素酸が使用する場合に、酸化タンタル膜あるいはダイヤモンド膜の何れ一方の存在によって上記素子を確実に保護できる。

【図面の簡単な説明】

【図１】この発明の表示用トランジスタアレイパネルの形成方法における手順を示す図である。

【図２】図１に続く表示用トランジスタアレイパネルの形成方法における手順を示す図である。

【図３】図２に続く受動素子部形成プロセスの説明図である。

【図４】図１～図３に示す形成方法によって形成された表示用トランジスタアレイパネルの外観図である。

【図５】順スタガＴＦＴの構造を示す図である。

【図６】逆スタガＴＦＴの構造を示す図である。

【図７】コプレーナＴＦＴの構造を示す図である。

【図８】逆スタガＴＦＴにおけるソース電極配線とゲート電極配線との交差部の断面図である。

【図９】図１とは異なる表示用トランジスタアレイパネルの形成方法における手順の一部を示す図である。

【図１０】従来の表示用トランジスタアレイパネルの形成方法において剥離層をエッチング除去して第１の基板全体を除去する方法の手順を示す図である。

【図１１】従来の表示用トランジスタアレイパネルの形成方法においてエッチバック工程によって第１の基板全体を除去する方法の手順を示す図である。

【図１２】従来の表示用トランジスタアレイパネルの形成方法において中間エッチストップ層を用いたシリコン薄膜転写法の手順を示す図である。

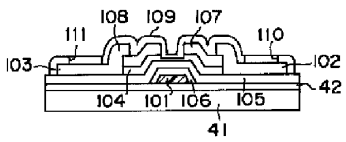
【図１３】従来の表示用トランジスタアレイパネルの形成方法においてＵＶ剥離両面テープを用いた転写方法の手順を示す図である。

【図１４】従来の表示用トランジスタアレイパネルの形成方法において基板上に密に形成したディバイスを粗に配置し直す転写方法の手順を示す図である。

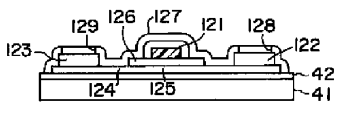
【符号の説明】

４１…Ｓｉ基板(第１の基板)、　４２…Ｓｉ酸化膜、４３，１２５…ＴＦＴ素子、　４４，１２６…素子分離溝、４５，１２８…ガラス基板(第２の基板)、４６，１２７…ＵＶ剥離樹脂、　４７，５５…ガラス基板(第３の基板)、４８，５７…接着樹脂、　５０，６２…紫外線、６６…ソース電極配線、　６８…ゲート電極配線、６９…ドレイン電極配線、　７０…画素電極、１３１…ガラス基板(第１の基板)、　１３２…Ｓｉ膜、１３３…Ｓｉ窒化膜(あるいはＳｉ酸化膜)、１３４…犠牲層。

【図６】

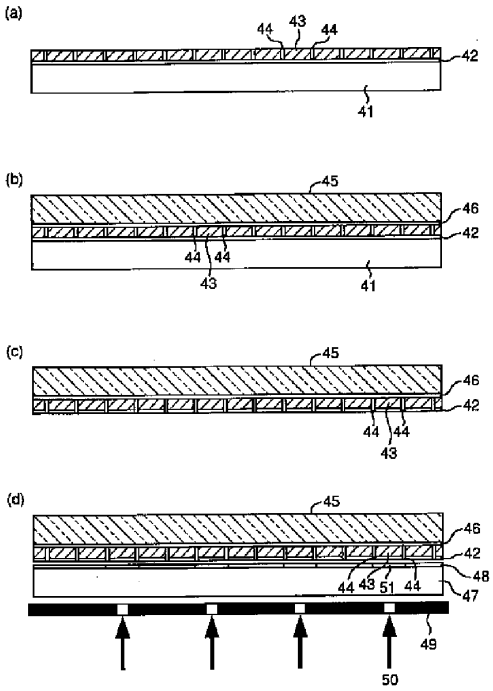


【図７】

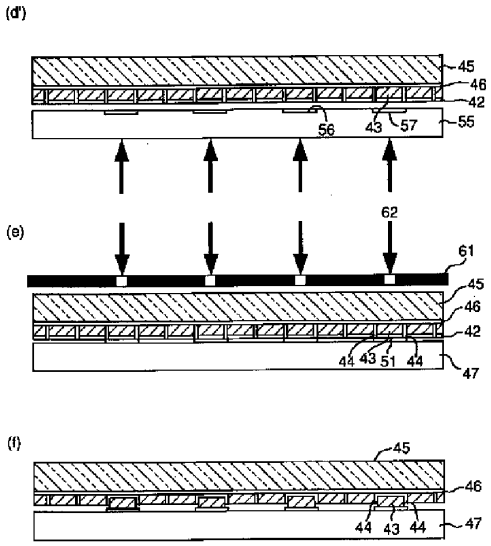


IPR2024-01134 - BOE
Exhibit 1009 - Page 185

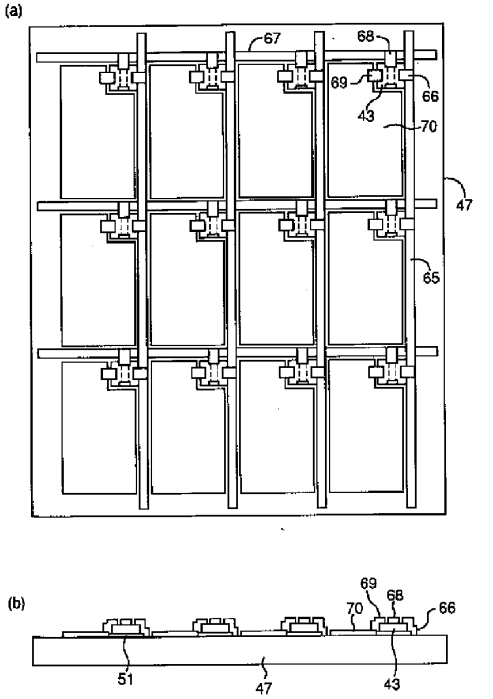
【図１】


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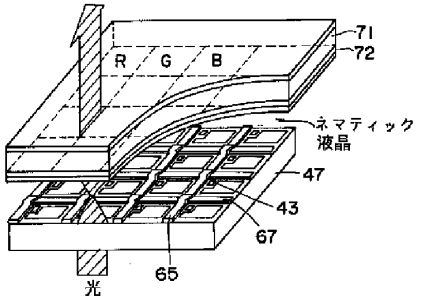
【図２】


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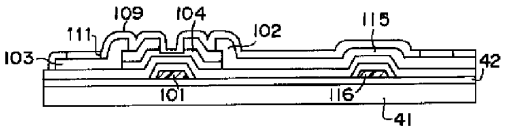
【図３】


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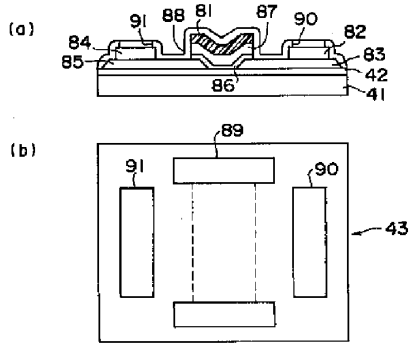
【図４】


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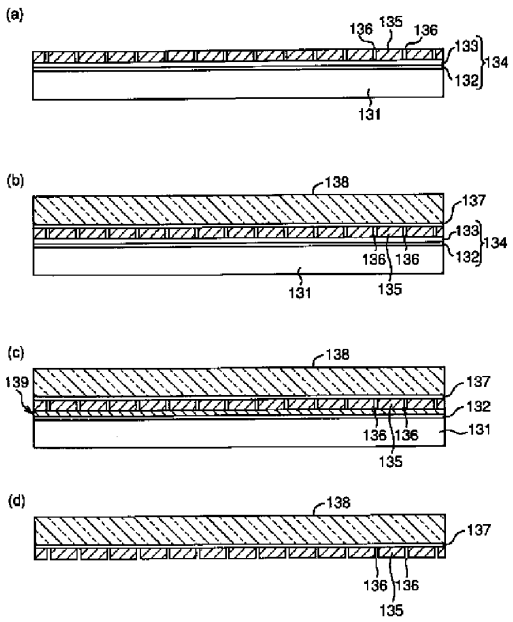
【図８】


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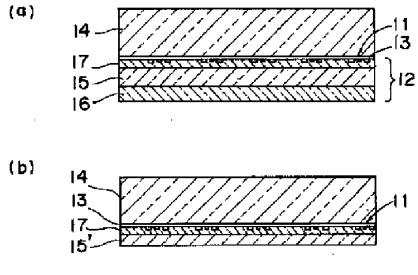
【図５】


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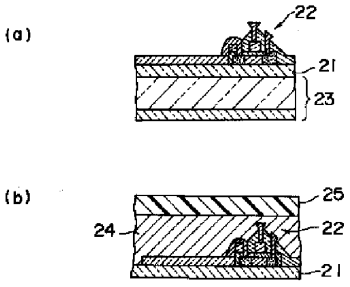
【図９】


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136
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131
135
(c)
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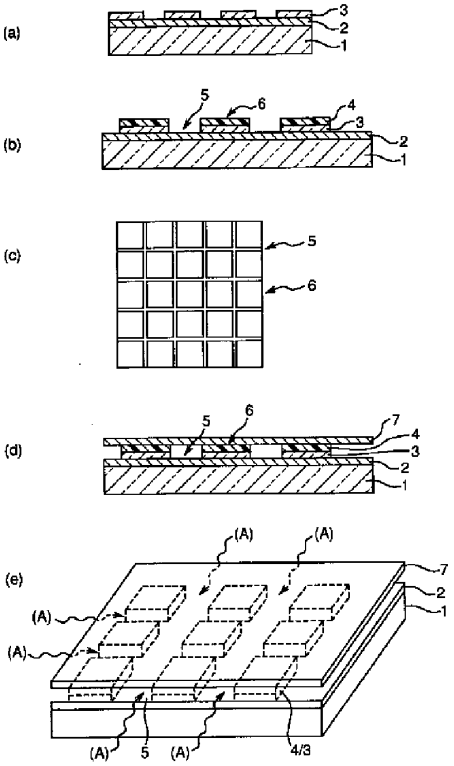
【図１１】


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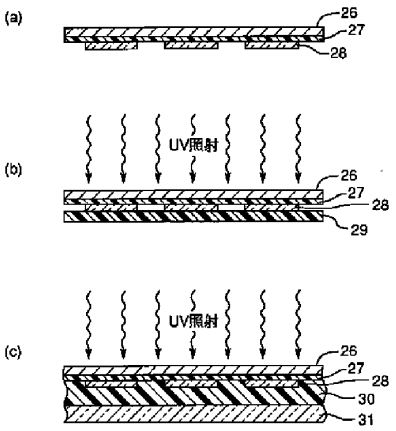
【図１２】


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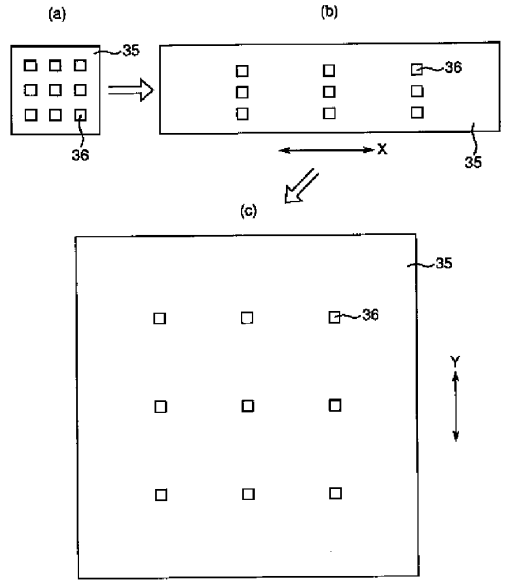
【図１０】


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【図１３】


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(b)
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(c)
UV照射
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【図１４】


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(71) Applicant *(for all designated States except US)*: **SEMPRIUS, INC.** [US/US]; 4915 Prospectus Drive, Suite C, Durham, North Carolina 27713 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **MENARD, Etienne** [FR/US]; 5215 Newhall Road, Durham, North Carolina 27713 (US). **CARR, Joseph** [US/US]; 204 Forest Ridge Drive, Chapel Hill, North Carolina 27514 (US).

(74) Agent: **SABAPATHYPILLAI Rohan G.**; MYERS BIGEL SIBLEY & SAJOVEC, P.A., P.O. Box 37428, Raleigh, North Carolina 27627 (US).

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[Continued on next page]

(54) Title: SELECTIVE TRANSFER OF ACTIVE COMPONENTS

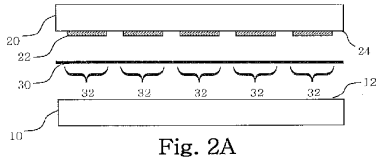


Fig. 2A

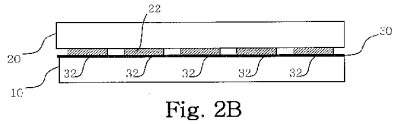


Fig. 2B

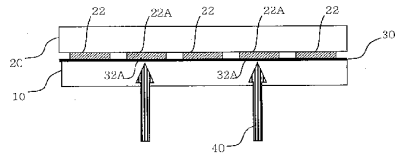


Fig. 2C

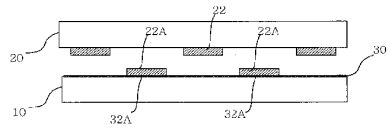


Fig. 2D

(57) Abstract: A method for selectively transferring active components (22) from a source substrate (20) to a destination substrate (10) includes providing a source substrate with one or more active components located on the source substrate, providing a destination substrate, locating a selectively curable adhesive layer (30) between and adjacent to the destination substrate and the source substrate, selecting one or more active components (22A), selectively curing area(s) (32A) of the adhesive layer corresponding to the selected active components to adhere the selected active components to the destination substrate, and removing the source substrate from the destination substrate leaving the selected active components adhered to the destination substrate in the selected areas.

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SELECTIVE TRANSFER OF ACTIVE COMPONENTS

CLAIM OF PRIORITY

The present application claims priority from U.S. Provisional Patent Application No. 61/318,508 entitled "*Selective Transfer of Active Components*," filed on March 29, 2010 with the United States Patent and Trademark Office, the disclosure of which is incorporated by reference herein.

FIELD OF THE INVENTION

The present invention is a method for providing substrates having electrically active components distributed thereon.

BACKGROUND OF THE INVENTION

Large substrates with electronically active components distributed over the extent of the substrate are useful in a variety of electronic systems, for example flat-panel imaging devices such as flat-panel liquid crystal or OLED display devices and in digital radiographic plates. Large substrates with electrically active components are also found in flat-panel solar cells.

The electronically active components are typically formed by sputtering a layer of inorganic semiconductor material or by spin-coating organic material over the entire substrate. Inorganic semiconductor materials can be processed to improve their electronic characteristics, for example amorphous silicon can be treated to form low-temperature or high-temperature poly-crystalline silicon. In other process methods, microcrystalline semiconductor layers can be formed by using an underlying seeding layer. These methods typically improve the electron mobility of the semiconductor. The substrate and layer of semiconductor material are typically photo-lithographically processed to define electronically active components, such as transistors. Such transistors are known as thin-film transistors (TFTs) since they are formed in a thin layer of semiconductor material, typically silicon. In these devices, the substrate is often made of glass, for example Corning Eagle or Jade glass designed for display applications. Photo-lithographic methods used to form the active components are known in the art.

These traditional techniques have significant limitations. Despite processing methods used to improve the performance of thin-film transistors, such

IPR2024-01134 - BOE
Exhibit 1009 - Page 191

transistors have performance that is lower than the performance of traditional integrated circuits formed in mono-crystalline semiconductor material. Also, semiconductor material and active components can be needed only on portions of the substrate, leading to wasted material and increased material and processing costs. The substrate materials can be limited by the processing steps necessary to process the semiconductor material and the photo-lithographic steps used to pattern the active components. For example, plastic substrates have a limited chemical and heat tolerance and do not readily survive photo-lithographic processing. Furthermore, the manufacturing equipment needed to process large substrates with thin-film circuitry is relatively expensive.

In an alternative manufacturing technique, a mono-crystalline semiconductor wafer is employed as the substrate. While this approach can provide substrates with similar performance as integrated circuits, the size of such substrates may be limited, for example, to a 12-inch diameter circle, and the wafers are relatively expensive compared to other substrate materials such as glass or polymer.

In yet another approach, thin layers of semiconductor are bonded to a substrate and then processed. Such a method is known as semiconductor-on-glass or silicon-on-glass (SOG) and is described, for example, in U.S. Patent Application 20080224254, dated September 18, 2004. If the semiconductor material is crystalline, high-performance thin-film circuits can be obtained. However, the bonding technique can be expensive and the processing equipment for the substrates to form the thin-film active components on large substrates remains relatively expensive.

Publication number 11-142878 of the Patent Abstracts of Japan entitled "Formation of Display Transistor Array Panel" describes etching a substrate to remove it from a thin-film transistor array on which the TFT array was formed. TFT circuits formed on a first substrate can be transferred to a second substrate by adhering the first substrate and the TFTs to the surface of the second substrate and then etching away the first substrate, leaving the TFTs bonded to the second substrate. This method requires etching a significant quantity of material and risks damaging the exposed TFT array.

An alternative method of locating material on a substrate is described in U.S. Patent 7,127,810. In this method, a first substrate carries a thin-film object to be transferred to a second substrate. An adhesive is applied to the object to be transferred or to the second substrate in the desired location of the object. The

IPR2024-01134 - BOE
Exhibit 1009 - Page 192

substrates are aligned and brought into contact. A laser beam irradiates the object to abrade the transferring thin film so that the transferring thin film adheres to the second substrate. The first and second substrates are separated, peeling the film in the abraded areas from the first substrate and transferring it to the second substrate. In one embodiment, a plurality of objects are selectively transferred by employing a plurality of laser beams to abrade selected area. Objects to be transferred can include thin-film circuits. In addition, U.S. Patent 6,969,624 describes a method of transferring a device from a first substrate onto a holding substrate by selectively irradiating an interface with an energy beam. The interface is located between a device for transfer and the first substrate and includes a material that generates ablation upon irradiation, thereby releasing the device from the substrate. For example, a light-emitting device (LED) may be made of a nitride semiconductor on a sapphire substrate. The energy beam is directed to the interface between the sapphire substrate and the LED nitride semiconductor releasing the LED and allowing the LED to adhere to a holding substrate coated with an adhesive. The adhesive is then cured. These methods, however, typically require the patterned deposition of adhesive on the object(s) or on the second substrate. Moreover, the laser beam that irradiates the object should be shaped to match the shape of the object, and the laser abrasion can damage the object to be transferred. Furthermore, the adhesive cure takes time, which typically reduces the throughput of the manufacturing system.

In another method for transferring active components from one substrate to another, described in "AMOLED Displays using Transfer-Printed Integrated Circuits" published in the Proceedings of the 2009 Society for Information Display International Symposium June 2-5, 2009, in San Antonio Texas, US, vol. 40, Book 2, ISSN 0009-0966X, paper 63.2 p. 947, small integrated circuits are formed in a wafer and released from the wafer by etching beneath the circuits. A PDMS stamp is pressed against the wafer and the circuits adhered to the stamp. The circuits are then pressed against a substrate coated with an adhesive, adhered to the substrate, and the adhesive is subsequently cured. This method, however, is susceptible to particulate contamination that can affect the adhesion of the integrated circuits to the stamps, the adhesion of the integrated circuits to the coated substrate, and the position of the integrated circuits on the substrate.

IPR2024-01134 - BOE
Exhibit 1009 - Page 193

SUMMARY OF THE INVENTION

It should be appreciated that this Summary is provided to introduce a selection of concepts in a simplified form, the concepts being further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of this disclosure, nor is it intended to limit the scope of the disclosure.

According to some embodiments of the present invention, a method for selectively transferring active components includes providing a curable adhesive layer between a receiving surface and a surface of a substrate including the active components thereon; assembling the substrate on the receiving surface such that the curable adhesive layer contacts the active components and the receiving surface; selectively curing portions of the curable adhesive layer in contact with ones of the active components without curing other portions thereof; and then separating the substrate from the receiving surface such that the ones of the active components on the cured portions of the curable adhesive layer are transferred to the receiving surface.

In some embodiments, an adhesive strength of the cured portions of the adhesive layer is greater than that used to releasably adhere the active components to the substrate.

In some embodiments, the cured portions respectively comprise less than an entirety of a contact area between the respective ones of the active components and the adhesive layer.

In some embodiments, the substrate is a source substrate, and the active components are releasably adhered to the source substrate by a plurality of tethers.

In some embodiments, the method further includes providing a sacrificial layer and an active layer on the source substrate; processing the active layer to define the active components and the plurality of tethers connecting the active components to anchor areas of the active layer; removing portions of the sacrificial layer between the active components and the source substrate such that the active components are releasably adhered to the source substrate by the plurality of tethers.

In some embodiments, the plurality of tethers include an etch-resistant material, and removing the portions of the sacrificial layer includes selectively etching the sacrificial layer without substantially etching the plurality of tethers.

IPR2024-01134 - BOE
Exhibit 1009 - Page 194

In some embodiments, separating the substrate from the receiving surface includes breaking ones of the plurality of tethers that are connected to the ones of the active components in contact with the cured portions of the adhesive layer.

In some embodiments, selectively curing includes selectively irradiating the portions of the curable adhesive layer with light, heat, and/or electromagnetic energy.

In some embodiments, selectively irradiating includes providing a mask that exposes the portions of the curable adhesive layer in contact with the ones of the active components; and selectively irradiating the portions of the curable adhesive layer exposed by the mask.

In some embodiments, the receiving surface is a surface of an at least partially transparent destination substrate, and selectively irradiating includes selectively transmitting a laser through the destination substrate to selectively irradiate the portions of the curable adhesive layer in contact with the ones of the active components.

In some embodiments, the substrate and the active components are at least partially transparent, and selectively irradiating includes selectively transmitting a laser through the source substrate and the ones of the active components to selectively irradiate the portions of the curable adhesive layer.

In some embodiments, the receiving surface is a flexible and/or a polymer destination substrate.

In some embodiments, the active layer is a crystalline, microcrystalline, polycrystalline, or amorphous semiconductor layer.

In some embodiments, the active layer has a thickness of greater than about 5 microns.

In some embodiments, the substrate is a stamp, and assembling the substrate on the receiving surface includes pressing the stamp on the receiving surface.

In some embodiments, the method further includes pressing the stamp on a source substrate including the active components releasably adhered thereto; and separating the stamp from the source substrate to transfer the active components from the source substrate to the stamp prior to pressing the stamp on the receiving surface.

In some embodiments, the active components are releasably adhered to the source substrate by a plurality of tethers, and pressing the stamp on the source

IPR2024-01134 - BOE
Exhibit 1009 - Page 195

substrate breaks ones of the plurality of tethers that are connected to the active components.

In some embodiments, the stamp includes a second curable adhesive layer thereon, the active components are first active components releasably adhered to the source substrate, and the source substrate further includes second active components releasably adhered thereto. The method further includes contacting the second curable adhesive layer with the first and second active components on the source substrate when pressing the stamp on the source substrate; and selectively disabling portions of the second adhesive layer in contact with the second active components to delaminate the second active components from the stamp prior to separating the stamp from the source substrate.

In some embodiments, the curable adhesive layer is a first adhesive layer, and the stamp includes a second adhesive layer thereon that releasably adheres the active components to the stamp. The method further includes selectively disabling portions of the second adhesive layer in contact with the ones of the active components prior to separating the stamp from the receiving surface such that an adhesive strength of the cured portions of the first adhesive layer is greater than that of the disabled portions of the second adhesive layer.

In some embodiments, the ones of the active components transferred to the receiving surface are first ones of the active components transferred to a first area of the receiving surface. After separating the substrate from the receiving surface, the method further includes: aligning the substrate with a second area of the receiving surface, the substrate including second ones of the active components remaining thereon; assembling the substrate on the second area of the receiving surface such that the curable adhesive layer contacts second ones of the active components and the receiving surface; selectively curing second portions of the curable adhesive layer in contact with the second ones of the active components; and then separating the substrate from the second area of the receiving surface such that the second ones of the active components on the cured second portions of the curable adhesive layer are transferred to the second area of the receiving surface.

In some embodiments, aligning the substrate includes moving the substrate in one or two dimensions relative to the receiving surface such that the first and second ones of the active components thereon define a one- or two-dimensional array of active components.

IPR2024-01134 - BOE
Exhibit 1009 - Page 196

In some embodiments, the curable adhesive layer is provided on the receiving surface or on the active components on the substrate.

In some embodiments, the adhesive layer is provided on the active components, and the ones of the active components transferred to the receiving surface are first ones of the active components. After separating the substrate from the receiving surface, the method further includes: assembling the substrate including second ones of the active components remaining thereon on a second receiving surface such that the adhesive layer is in contact with the second ones of the active components and the second receiving surface; and selectively curing portions of the adhesive layer in contact with the second ones of the active components and then separating the substrate from the second receiving surface to transfer the second ones of the active components to the second receiving surface.

In some embodiments, the adhesive layer is provided on the receiving surface, and the active components are first active components. The method further includes: assembling a second substrate including second active components thereon on the receiving surface such that the adhesive layer contacts the second active components; and selectively curing second portions of the adhesive layer in contact with the second active components and then separating the second substrate from the receiving surface to transfer the second active components to the receiving surface.

In some embodiments, after separating the substrate from the receiving surface, the method further includes: cleaning the substrate; and providing second active components on the surface of the substrate for transfer to the receiving surface and/or another receiving surface.

According further embodiments of the present invention, a method for selectively transferring active components from a source substrate to a destination substrate comprises the steps of: a) providing a source substrate having an active side and one or more active components located on the active side of the source substrate; b) providing a destination substrate having a receiving side; c) locating a selectively curable adhesive layer between and adjacent to the receiving side of the destination substrate and the active side of the source substrate, the selectively curable adhesive layer having separate areas between each of the active component(s) and the receiving side of the destination substrate; d) selecting one or more active components having corresponding selected areas; e) selectively curing the adhesive layer in the selected area(s) of the adhesive layer corresponding to the selected active components to

IPR2024-01134 - BOE
Exhibit 1009 - Page 197

adhere the selected active components to the receiving side of the destination substrate in the selected areas; and f) removing the source substrate from the destination substrate leaving the selected active components adhered to the receiving side of the destination substrate in the selected areas.

In some embodiments, step a) comprises the steps of: g) providing a source substrate having a sacrificial layer formed over the source substrate and an active layer formed on the sacrificial layer; h) processing the source substrate to form one or more active component(s) in or on the active layer and a trench around each of the active component(s), the trench extending through the active layer to the sacrificial layer; i) removing the sacrificial layer except for breakable tethers to release the active components from the source substrate, wherein step f) breaks the tethers of the selected active components.

In some embodiments, the method further includes the steps of stripping any sacrificial layer material or active layer material from the source substrate, cleaning the source substrate, forming a second sacrificial layer over the source substrate, forming a second active layer over the second sacrificial layer, and, after step f), repeating steps c) through f).

In some embodiments, step a) comprises the steps of: j) forming one or more active components and; k) releasably adhering the active components to the active side of the source substrate with a releasable adhesive, wherein step f) releases the releasable adhesive in the selected area(s).

In some embodiments, the selectively curable adhesive layer is an adhesive film having a selectively curable adhesive coated on an adhesive carrier.

In some embodiments, the selectively curable adhesive layer is an adhesive coated on the receiving side of the destination substrate or an adhesive coated on the active components.

In some embodiments, the selected area(s) are cured by exposure to a pattern of electromagnetic radiation or a pattern of heat.

In some embodiments, the pattern of electromagnetic radiation or heat is provided by a laser.

In some embodiments, the pattern of electromagnetic radiation is provided by an electromagnetic radiation source through a mask.

IPR2024-01134 - BOE
Exhibit 1009 - Page 198

In some embodiments, the destination substrate is at least partially transparent and the electromagnetic radiation is provided through the destination substrate.

In some embodiments, the source substrate is at least partially transparent, the active components are at least partially transparent, and the electromagnetic radiation is provided through the source substrate and the selected active components.

In some embodiments, the destination substrate is flexible.

In some embodiments, the destination substrate is a polymer.

In some embodiments, the source substrate is a semiconductor wafer.

In some embodiments, the source substrate is a silicon or a gallium arsenide wafer.

In some embodiments, the active layer is a crystalline, microcrystalline, polycrystalline, or amorphous semiconductor layer.

In some embodiments, the active layer has a thickness greater than 5 microns.

In some embodiments, the selected active components form a regular array in one or two dimensions.

In some embodiments, the method further includes the steps of: l) after step f), moving the source substrate and the destination substrate relative to each other; and m) repeating steps d), e), and f).

According to still further embodiments, a method for selectively transferring active components from a source substrate to a destination substrate, comprises the steps of: a) providing a source wafer having a sacrificial layer formed over the source wafer and an active layer formed on the sacrificial layer; b) processing the source wafer to form one or more active component(s) in or on the active layer and a trench around each of the active component(s), the trench extending through the active layer to the sacrificial layer; c) removing the sacrificial layer except for breakable tethers to release the active components from the source substrate; d) providing a destination substrate having a receiving side; e) locating a selectively curable adhesive layer between and adjacent to the receiving side of the destination substrate and the active component side of the source wafer, the selectively curable adhesive layer having separate areas between each of the active component(s) and the receiving side of the destination substrate; f) selecting one or more active

IPR2024-01134 - BOE
Exhibit 1009 - Page 199

components; g) selectively curing the adhesive layer in selected area(s) of the adhesive layer corresponding to the selected active components to adhere the selected active components to the receiving side of the destination substrate in the selected area(s); and h) breaking the tethers by removing the source substrate and the adhesive layer from the destination substrate leaving the selected active components adhered to the receiving side of the destination substrate in the selected area(s).

In some embodiments, the active layer is a crystalline semiconductor having thickness equal to or greater than 5 microns.

According to yet further embodiments, a method for selectively transferring active components from a source substrate to a destination substrate, comprises the steps of: a) providing a source substrate having an active side and one or more active components located on the active side of the source substrate; b) providing a destination substrate having a receiving side coated with a selectively curable adhesive; c) providing a stamp; d) pressing the stamp against the active components to adhere the active components to the stamp; e) stamping the active components onto the receiving side of the destination substrate to adhere the first active components to the receiving side of the destination substrate; f) selectively curing the selectively curable adhesive layer in the areas corresponding to the active components; g) removing the stamp from the destination substrate leaving the first active components adhered to the receiving side of the destination substrate.

In some embodiments, the method further includes the step of selectively curing the selectively curable adhesive after the stamp is removed from the receiving side of the destination substrate.

In some embodiments, the method further includes the step of selectively curing the selectively curable adhesive before the stamp is removed from the receiving side of the destination substrate.

In some embodiments, the method further includes the step of selectively curing the adhesive layer by exposing the selectively curable adhesive layer to electromagnetic radiation incident on the selectively curable adhesive layer through the stamp in the areas of the first active components.

According to yet still further embodiments, a method for selectively transferring active components from a source substrate to a destination substrate, comprises the steps of: a) providing a source substrate having an active side and one or more active components located on the active side of the source substrate; b)

IPR2024-01134 - BOE
Exhibit 1009 - Page 200

providing a destination substrate having a receiving side; c) providing a stamp; d) locating a selectively adhesive layer between and adjacent to the stamp and the active side of the source substrate, the selectively adhesive layer having separate areas between each of the active component(s) and the stamp, thereby laminating the active components to the stamp; e) selecting one or more first active components having corresponding first selected areas and one or more remaining second active components having corresponding second selected areas; f) selectively delaminating the selectively adhesive layer in the second selected area(s) and removing the stamp from the source substrate leaving the first active components laminated to the stamp; and g) stamping the first active components onto the receiving side of the destination substrate to adhere the first active components to the receiving side of the destination substrate; h) removing the stamp from the destination substrate leaving the first active components adhered to the receiving side of the destination substrate.

In some embodiments, the method further includes the step of providing a receiving adhesive layer over the receiving side of the destination substrate.

In some embodiments, the receiving adhesive is curable and the method further includes the step of curing the receiving adhesive layer before the stamp is removed from the receiving side of the destination substrate.

In some embodiments, the receiving adhesive layer is selectively curable and the method further includes the step of selectively curing the receiving adhesive layer by exposing the receiving adhesive layer to electromagnetic radiation incident on the receiving adhesive layer through the stamp in the areas of the first active components.

In some embodiments, the method further includes the step of selectively delaminating the selectively curable adhesive layer in the first selected area(s) before removing the stamp from the destination substrate.

Embodiments of the present invention provide higher-performance active components over large substrates at a reduced cost in materials and manufacturing equipment.

Other methods and/or devices according to some embodiments will become apparent to one with skill in the art upon review of the following drawings and detailed description. It is intended that all such additional embodiments, in addition to any and all combinations of the above embodiments, be included within

IPR2024-01134 - BOE
Exhibit 1009 - Page 201

this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a flow diagram illustrating an embodiment of the method of the present invention;

Figs. 2A-2D are cross sections of the elements of a device at different stages of construction according to an embodiment of the method of the present invention;

Fig 3 is a perspective of the device elements illustrated in the cross section of Fig. 2A;

Fig. 4 is a cross section depicting the exposure of selected areas of an adhesive layer according to an embodiment of the method of the present invention;

Fig. 5 is a cross section depicting an alternative exposure of selected areas of an adhesive layer according to an alternative embodiment of the method of the present invention;

Fig. 6 is a flow diagram illustrating a portion of an embodiment of the method of the present invention;

Fig. 7 is a flow diagram illustrating a portion of an alternative embodiment of the method of the present invention;

Figs. 8A-8D are cross sections of elements of a source substrate at different stages of construction according to an embodiment of the method of the present invention;

Fig. 9 is a top view depicting the structure of Fig. 8D;

Fig. 10A is a photomicrograph of an active component before release from a source wafer according to an embodiment of the method of the present invention;

Fig. 10B is a photomicrograph of an active component adhered to a destination wafer according to an embodiment of the method of the present invention;

Fig. 11 is a flow diagram illustrating a method of reusing a source substrate according to an embodiment of the method of the present invention;

Figs. 12A-12D are cross sections of the elements of a device at different stages of construction according to an iterative embodiment of the method of the present invention;

IPR2024-01134 - BOE
Exhibit 1009 - Page 202

Fig. 13 is a flow diagram illustrating an iterative method according to an embodiment of the method of the present invention;

Fig. 14 is a flow diagram illustrating an alternative method according to an embodiment of the present invention; and

Fig. 15 is a flow diagram illustrating an alternative method according to an embodiment of the present invention.

The figures are not drawn to scale since the individual elements of the drawings have too great a size variation to permit depiction to scale.

IPR2024-01134 - BOE
Exhibit 1009 - Page 203

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. However, this invention should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout.

It will be understood that when an element such as a layer, region or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

It will also be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present invention.

Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another element as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in one of the figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on "upper" sides of the other elements. The exemplary term "lower", can therefore, encompasses both an orientation of "lower" and "upper," depending of the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be

IPR2024-01134 - BOE
Exhibit 1009 - Page 204

oriented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

The terminology used in the description of the invention herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used in the description of the invention and the appended claims, the singular forms "a", "an " and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

Embodiments of the invention are described herein with reference to cross-section illustrations that are schematic illustrations of idealized embodiments (and intermediate structures) of the invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. In other words, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of the invention.

Unless otherwise defined, all terms used in disclosing embodiments of the invention, including technical and scientific terms, have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs, and are not necessarily limited to the specific definitions known at the time of the present invention being described. Accordingly, these terms can include equivalent terms that are created after such time. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the present specification and in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein. All publications, patent applications,

IPR2024-01134 - BOE
Exhibit 1009 - Page 205

patents, and other references mentioned herein are incorporated by reference in their entireties.

Referring to the flow diagram of Fig. 1 and to the illustrations of Figs. 2A-2D, one embodiment of the present invention provides a source substrate **20** having an active side **24** of the source substrate **20** in step **100**. As shown in Fig. 2A, one or more active components **22** are located on the active side **24** of the source substrate **20** in step **105**. A destination substrate or receiving substrate **10** having a receiving side **12** is also provided in step **110**. The source substrate **20** and destination substrate **10** can be made separately and at different times or in different temporal orders. The active components **22** can be made separately and then located on the source substrate **20** or can be formed in or on the source substrate **20**. Referring also to Fig. 2B, a selectively curable adhesive layer **30** is located between and adjacent to the receiving side **12** of the destination substrate **10** and the active side **24** of the source substrate **20** in step **115**. The selectively curable adhesive layer **30** has separate areas **32** between each of the active component(s) **22** and the receiving side **12** of the destination substrate **10.** Note that the selectively curable adhesive layer **30** areas **32** are portions of the selectively curable adhesive layer **30** areas that would be in contact with the active components **22** and the receiving side of the destination substrate **10** if the layers are all in contact together in a stack, as illustrated in Fig. 2B.

One or more active components **22** are selected in step **120** and, in step **122**, the adhesive layer **30** is selectively cured in selected area(s) **32A** of the adhesive layer **30** corresponding to the selected active components **22A** to adhere the selected active components **22A** to the receiving side **12** of the destination substrate in the selected areas **32A**. However, other areas of the adhesive layer 30 (for example, areas corresponding to unselected ones of the active components 22) are not cured. As shown in Fig. 2C, for example, the selectively curable adhesive layer **30** is selectively curable through the patterned application of laser light **40**. Referring to Fig. 2D, once the adhesive is cured in the selected areas **32A**, the source substrate **20** is removed from the destination substrate **10** in step **125**, leaving the selected active components **22A** adhered to the receiving side of the destination substrate **10** in the selected areas **32A**.

Fig. 3 is an exploded perspective showing the layers of Fig. 2A. In this embodiment, the active components **22** are arranged in a two-dimensional array on the active side **24** of the source substrate **20**. The selectively curable adhesive layer

IPR2024-01134 - BOE
Exhibit 1009 - Page 206

30 is located between the active components **22** and the receiving side **12** of the destination substrate **10**.

The adhesive layer **30** can be located on the receiving side **10** of the destination substrate **12** (as illustrated in Figs. 2A-2D, or it can be applied to the active components **22** and component side **24** of the source substrate **20**. When the source substrate **20** is removed from the destination substrate **10** in step **125**, the selectively curable adhesive layer **30** can either remain in place on the receiving side **12** of the destination substrate **10** or it can be kept in place on the active component(s) **22** and active side **24** of the source substrate **20**.

Suitable selectively curable adhesive layers may include, for example, UV-curable adhesive resins used in the photo-lithographic industry. Adhesives can be applied, for example, as a film on a carrier that is applied to a substrate and the carrier subsequently removed, for example by peeling, leaving an adhesive film on the substrate. Alternatively, uncured liquid adhesives can be coated on the destination substrate, for example by spin coating or curtain coating, or other coating means known in the art. The selectively curable adhesive layer can also be applied to the active components and on the source substrate. A selectively curable adhesive, as used herein, is a material (dry or liquid) that can be cured in some areas, but not others, for example by the patterned application of energy (e.g. electromagnetic energy such as ultra-violet radiation or light, or patterned heat). A laser can be used to provide light or heat to selected areas.

As shown in Fig. 4, the selected adhesive layer areas can be irradiated through the source substrate **20**. In this case, the source substrate **20** must be at least partially transparent, as must the active components **22**. In the case (referring back to Fig. 2C) in which the selected adhesive layer areas are irradiated through the destination substrate **10**, the destination substrate **10** must be at least partially transparent, while the active components **22** are not necessarily transparent. Alternatively, electromagnetic radiation **40** can be applied through a mask **70**, as shown in Fig. 5, to selectively irradiate the selected curable adhesive layer areas.

The selectively curable adhesive can include materials that improve the absorption of light or heat, to improve the rate of curing, for example dyes. The radiation pattern corresponds to the spatial area cured. The selected areas/cured portions may not necessarily correspond exactly to the shape of the active components in some embodiments. Rather, adhesion can be provided to at least a portion of the

IPR2024-01134 - BOE
Exhibit 1009 - Page 207

active component, in contrast to traditional methods that require adhesion of almost the entire surface of the active component to enable transfer. For example, a smaller dot of cured adhesive attached to a larger rectangular active component can be sufficient to effect transfer from the source substrate to the destination substrate in accordance with some embodiments of the present invention. A wide variety of substrate materials are known in the art and can be employed, for example glass, polymers, quartz, and silicon. In particular, glass substrates are widely used in various industries such as display, radiography, and photovoltaics. A variety of active components are also known, for example formed in layers of silicon. In one embodiment of an active component, thin-film transistors are photo-lithographically formed on a thin silicon layer sputtered and possibly processed on a glass substrate. However, such active components typically have lower performance and are mechanically fragile, leading to damage during the transfer process and can lack adequate mechanical robustness.

In some embodiments, the active components are small integrated circuits formed in a semiconductor wafer substrate, for example gallium arsenide or silicon, which can have a crystalline structure. Processing technologies for these materials typically employ high heat and reactive chemicals. However, by employing transfer technologies that do not stress the active component or substrate materials, more benign environmental conditions can be used compared to thin-film manufacturing processes. Thus, the present invention has an advantage in that flexible substrates that are intolerant of extreme processing conditions (e.g. heat, chemical, or mechanical processes) can be employed either for the source or destination substrates. Furthermore, it has been demonstrated that crystalline silicon substrates have strong mechanical properties and, in small sizes, can be relatively flexible and tolerant of mechanical stress. This is particularly true for substrates of 5 micron, 10 micron, 20 micron, 50 micron, or even 100-micron thicknesses. Alternatively, the active layer can be a microcrystalline, polycrystalline, or amorphous semiconductor layer.

Referring to the flow diagram of Fig. 6, small integrated circuits can be made using traditional means in step **150** and then releasably adhered to a source substrate in step **155**. As used herein, releasably adhered means that a small integrated circuit is sufficiently adhered to a substrate so that ordinary handling of the substrate does not dislodge the small integrated circuit but that the small integrated circuit can be readily removed from the source substrate by using a stronger adhesive or by

IPR2024-01134 - BOE
Exhibit 1009 - Page 208

mechanical handling to pull it off without damaging the small integrated circuit and without the use of chemical processing, for example etching. The process described above can then be applied to transfer the small integrated circuits (active components) to a destination substrate. Note that the releasable adhesive must be strong enough to adhere the small integrated circuits to the source substrate during transport and handling, but weak enough to separate during the step **125** (Fig. 1) of removing the source substrate. The cure of the adhesive layer (step **122**) in selected area(s) must provide relatively more adhesion than the releasable adhesive or any other means of adhering the active component(s) to the source substrate, but the adhesive cure does not have to be complete. In a later step, the adhesive layer could be baked to bring the device to a complete state of robust adhesion suitable for a product.

Fig. 7 is a flow diagram of further methods of providing a source substrate with active components (step **105** of Fig. 1); Figs. 8A-8D illustrate the method. As shown in Figs. 7 and 8A, a sacrificial layer **26** is formed on the source substrate **20** and an active layer **28** formed on the sacrificial layer **26** in step **106**. The substrate can be, for example, a silicon wafer. The sacrificial layer **26** can be an oxide layer deposited on the wafer. The active layer **28** can be mono-crystalline silicon formed on the oxide layer. Both the sacrificial layer **26** and the active layer **28** can be deposited on the source substrate **20** using standard wafer-processing methods known in the art.

Referring to Fig. 8B, after the sacrificial layer **26** and the active layer **28** are deposited on the source substrate **20**, the source substrate **20** can be processed in step **107** to form active components **22** in or on the active layer **28**, for example using silicon foundry fabrication process known in the art, Additional layers of material can be added as well as other materials such as metals, oxides, nitrides and other materials known in the integrated-circuit art. Each active component **22** can be complete semiconductor integrated circuits and include, for example, transistors. The active components **22** can have different sizes, for example, 1000 square microns or 10,000 square microns, 100,000 square microns, or 1 square mm, or larger, and can have variable aspect ratios, for example 2:1, 5:1, or 10:1.

After the active components **22** are formed, as shown in Fig. 8C, trenches **60** can be formed in step **108** around the active components **22** to structurally isolate them from each other. The trench **60** extends through the active layer **28** to the

IPR2024-01134 - BOE
Exhibit 1009 - Page 209

sacrificial layer **26**. The trenches **60** can be formed before the active components **22** are processed, or can be formed as a part of the active component formation process.

The sacrificial layer **26** is then removed in step **109**, for example by etching with hydrofluoric acid and as shown in Fig. 8D. Care must be taken to ensure that the active components **22** are completely detached from the source substrate **20**, except for tethers **62** (illustrated in Fig. 9 in a top view) while at the same time anchoring the tethers to an anchor portion **29** of the active layer **28** that remains attached to the source substrate **20** and sacrificial layer **26**. To ensure this result, the relative width of the space between the active components **22** in the active layer **28** and the relative size and aspect ratio of the active components **22** must be carefully chosen, together with the etch rate and conditions to properly separate the active components **22** from the source substrate **20** without removing the anchor areas **29**. The tethers can be protected from the etch step by coating the tethers **62** with an etch-resistant material or forming the tethers **62** from different, etch-resistant materials (using photo-lithographic processes). Fig. 10A is a photomicrograph of a silicon-based integrated circuit of approximately 40 microns by 140 microns by 10 microns in size having a trench **60** width of approximately 15 microns and tethers **62** anchoring the active component **22** to an anchor area **29** affixed to the source substrate **20** between the active components **22**. The active component **22** includes metal wiring layers and electrical connection pads as well as interlayer dielectric (ILD) elements.

Referring back to Figs. 1 and 7, once the active components are located on the source substrate (step **105**), the active components can be applied to the selectively curable adhesive layer and the destination substrate (steps **110** and **115**). The adhesive is selectively cured in the areas of selected active components (steps **120** and **122**). The source substrate is then removed from the destination substrate in step **126** (analogous to step **125**), breaking the tethers **62**. Fig. 10B is a photomicrograph of the integrated circuit active component **22** of Fig. 10A showing the broken tethers or "tabs" **64**.

Therefore, as illustrated in the Figures, a method for selectively transferring active components from a source substrate to a destination substrate according to some embodiments, can comprise the steps of providing a source wafer having a sacrificial layer formed over the source wafer and an active layer formed on the sacrificial layer, processing the source wafer to form one or more active

IPR2024-01134 - BOE
Exhibit 1009 - Page 210

component(s) in or on the active layer and a trench around each of the active component(s), the trench extending through the active layer to the sacrificial layer, and removing the sacrificial layer except for breakable tethers to release the active components from the source substrate. A destination substrate having a receiving side, is provided and a selectively curable adhesive layer located between and adjacent to the receiving side of the destination substrate and the active component side of the source wafer. The selectively curable adhesive layer has separate areas between each of the active component(s) and the receiving side of the destination substrate. One or more active components are selected, and the adhesive layer selectively cured in selected area(s) of the adhesive layer corresponding to the selected active components to adhere the selected active components to the receiving side of the destination substrate in the selected area(s). The tethers are broken by removing the source substrate and the adhesive layer from the destination substrate leaving the selected active components adhered to the receiving side of the destination substrate in the selected area(s).

Referring to Fig. 11, once all of the active components to be used in a process are transferred, the source substrate can be stripped of the remaining active layer and sacrificial layer materials and cleaned in step **130**. A second sacrificial layer can be formed over the source substrate in step **135** and a second active layer formed over the second sacrificial layer in step **140**. The process of constructing new active components and adhering them to a new destination substrate can then be repeated, thereby reusing the source substrate. Likewise, if the active components were releasably adhered to a source substrate, the substrate could be cleaned of any remaining releasable adhesive and active components after the transfer processes are complete, and the source substrate reused.

Referring to Fig. 14, in still further embodiments of the present invention, active components are transferred from a source substrate to a destination substrate by providing a source substrate having an active side and one or more active components located on the active side of the source substrate, providing a destination substrate having a receiving side coated with a selectively curable adhesive, and providing a stamp in step **200**. The active components can be released from the source substrate by photolithographic processing so that they are connected to the source substrate only by small tethers. The stamp is pressed against the active components, breaking the tethers and adhering the active components to the stamp in step **205**. The

IPR2024-01134 - BOE
Exhibit 1009 - Page 211

stamp and active components are then pressed against a destination substrate coated with an unpatterned adhesive in step **210**. The adhesive in the areas of the active components is selectively cured, for example by exposure to laser light, adhering the active components to the destination substrate in step **215**. The exposure to light can be done through the destination substrate or through the stamp, if it is at least partially transparent. The stamp is then removed from the destination substrate in step **220**. The process can be repeated as described above in Figs. 12A-12D.

The stamp can be flat or structured, for example with protrusions matched to the shapes, sizes, and locations of the active components to enhance lamination. The stamp can be elastomeric, made of PDMS, rubber, or a reinforced composite.

The adhesion between the active components and the receiving side of the destination substrate is greater than the adhesion between the active components and the stamp. When the stamp is removed from the receiving side of the destination substrate, the active components must adhere more strongly to the receiving side than to the stamp, to transfer the active components from the stamp to the receiving side.

In one embodiment of the method illustrated in Fig. 14, the stamp adheres only a subset of the active components, for example a subset array of the available active components on the source substrate. When the adhesive is selectively cured, it is selectively cured in the areas of all of the active components transferred by the stamp. Subsequent stamping steps can then remove different subset arrays of active components from the source substrate and stamp them in different locations on the destination substrate to form a sparse array of active components adhered to the receiving side of the destination substrate.

In an alternative embodiment of the method of Fig. 14, all of the active components within an array on the source wafer are removed from the source wafer and adhered to the stamp. Likewise, all of the removed active components are stamped onto the receiving side of the destination wafer. However, only selected active components, for example a subset array of the active components on the stamp are adhered to the destination substrate by selectively curing the areas of the adhesive corresponding to the selected active components. The stamp is then removed from the destination substrate and can be reapplied elsewhere on the destination substrate to selectively adhere another, different subset array of active components to another different destination substrate area. In this embodiment, there is no need to repeatedly

IPR2024-01134 - BOE
Exhibit 1009 - Page 212

press the stamp against the source wafer, but the adhesion of the active components to the stamp must be stronger than the uncured adhesion to the destination substrate and weaker than the cured adhesion to the destination substrate.

Referring to Fig. 15, in an alternative method of the present invention, active components are transferred from a source substrate to a destination substrate by providing a source substrate having an active side and one or more active components located on the active side of the source substrate, providing a destination substrate having a receiving side, and providing a stamp in step **300**. A selectively adhesive layer is located between and adjacent to the stamp and the active side of the source substrate, the selective adhesive layer having separate areas between each of the active component(s) and the stamp, thereby laminating the active components to the stamp in step **305**. One or more first active components having corresponding first selected areas and one or more remaining second active components having corresponding second selected areas are selected in step **310**.

The adhesive layer in the second selected area(s) is selectively delaminated and the stamp removed from the source substrate leaving the first active components laminated to the stamp in step **315**. In contrast to the methods described above, in this method the adhesive is selectively disabled in the areas in which active components are not to be transferred, leaving the laminated first active components adhered to the stamp for transfer to a destination substrate. The first active components are stamped onto the receiving side of the destination substrate to adhere the first active components to the receiving side of the destination substrate in step **320**. The stamp is removed from the destination substrate leaving the first active components adhered to the receiving side of the destination substrate in step **335**.

The stamp can be flat or structured, for example with protrusions matched to the shapes and locations of the active components to enhance lamination. The stamp can be elastomeric, made of PDMS, rubber, or a reinforced composite.

The adhesion between the first active components and the receiving side is greater than the adhesion between the first active components and the stamp. When the stamp is removed from the receiving side of the destination substrate, the active components must adhere more strongly to the receiving side than to the stamp, to transfer the active components from the stamp to the receiving side.

To assist in the transfer process, in one embodiment of the present invention, the first areas corresponding to the first active components can be selectively delaminated to

IPR2024-01134 - BOE
Exhibit 1009 - Page 213

reduce the first active component adhesion to the stamp in optional step **325**. Delamination of the selectively curable adhesive can be done by exposure to electromagnetic radiation, either through the stamp (if at least partially transparent) or through the back side of the active components. A selectively curable receiving adhesive, similar to that used in the methods described above can also be used to increase the adhesion between the first active components and the receiving side of the destination substrate before the stamp is removed from the receiving side by curing the receiving adhesive in the areas of the first active components in step **330**. Note that the selectively curable adhesive between the stamp and the active components can be selectively delaminated to decrease the adhesive strength while the selectively curable receiving adhesive between the receiving side and the first active components can be selectively cured to increase the adhesive strength between the first active components and the receiving side. Adhesives that increase or decrease their adhesion in response to heat or radiation are known in the art.

Referring to the illustrations of Figs. 12A-12D and the flow diagram of Fig. 13, the method of the present invention can be iteratively applied to a single or multiple destination substrates **10**. As shown in Fig. 12A, after the source substrate **20** is removed from the destination substrate **10** (step **125** of Fig. 13), one or more active components **22A** remain affixed to the destination substrate **10**. In one embodiment of the present invention, all of the active components **22** on the source substrate **20** can be adhered to the destination substrate **10**. In another embodiment of the present invention, only one, or more than one, active component(s) **22** can be adhered to the destination substrate **10**. As shown in Fig. 12A, a subset of the active components **22** is transferred to the destination substrate **10**. The subset includes a regular array of active components **22** that are not adjacent to each other, for example every other active component **22** (as shown in Fig. 12A), every third active component **22**, every tenth active component **22**, and so on, forming a sub-array of active components **22**. The sub-array can, but need not, be regular.

Once the subset of active components **22** is transferred and the source and destination substrates **20**, **10** are separated (step **125** in Fig. 13), the source and destination substrates **20**, **10** are moved relative to each other in a direction **50** in step **150**, as indicated with the arrow in a Fig. 12A, to a position indicated in Fig. 12B. The process of adhering remaining active components **22** on the source substrate **20** can be repeated by locating the selectively curable adhesive layer **30** between and

IPR2024-01134 - BOE
Exhibit 1009 - Page 214

adjacent the active components **22** and the destination substrate **10** (in step **115**), selecting desired active components **22** and the corresponding selected adhesive layer areas (step **121**), selectively curing the selected areas with, for example laser light **40**, as illustrated in Fig. 12C and step **122**, and removing the source and destination substrate **20**, **10**, from each other, as shown in Fig. 12D (step **125** again). By ensuring that the relative movement of the source and destination substrates **20**, **11** is equal to the spacing of the selected active components **22**, a regular array of transferred active components **22A** can be distributed over the destination substrate **10** in an iterative process as shown in Fig. 13. Although the illustrations of Figs. 12A-12D are shown in cross section and the array of active components **22** is shown distributed in one dimension, the selection of active components **22** can be two-dimensional (as shown in Fig. 3), the relative movement of the source and destination substrates **20**, **11** can likewise be two-dimensional, and the resulting array of transferred active components **22A** adhered to the destination substrate **10** can likewise be two-dimensional and the array of transferred active components can be a regular two-dimensional array. Therefore, by repeatedly transferring sub-arrays of active components **22** from a source substrate **20** to a destination substrate **10** and relatively moving the source and destination substrates **20**, **11** a distance equal to the spacing of the selected active components **22** in the transferred sub-array between each transfer of active components **22**, an array of active components **22** formed at a high density on a source substrate **20** can be transferred to a destination substrate **10** at a much lower density. In practice, the source substrate **20** is likely to be expensive, and forming active components **22** with a high density on the source substrate **20** will reduce the cost of the active components **22**, especially as compared to forming active components on the destination substrate. Transferring the active components **22** to a lower-density destination substrate **10** can be useful, for example, if the active components **22** manage elements distributed over the destination array, for example in a display, digital radiographic plate, or photovoltaic system.

According to various embodiments of the present invention, the adhesive layer can be located adjacent to or adhered to the destination substrate before the selected areas are cured. In an iterative process such as that described in Figs. 12 and 13, the selectively curable layer can be left in place for repeated transfers of selected active components onto the same destination substrate from the same or different source substrates. Similarly, the selectively adhesive layer can be located

IPR2024-01134 - BOE
Exhibit 1009 - Page 215

adjacent to or adhered to the source substrate before the selected areas are cured and left in place for repeated transfers of selected active components from the same source substrate to the same or different destination substrates.

The selective curing of the selectively curable adhesive layer need not cure the adhesive over the entire selected area corresponding to the area taken by each of the entire selected active component(s). It is only necessary to cure enough adhesive over a sufficient area to adhere the active components to the destination substrate when the source substrate is removed. In particular, for an active component that has sufficient mechanical robustness and cohesion, only a portion of the active component need be adhered to the destination substrate. As the source substrate is removed, the adhered portion will keep the remainder of the active components adjacent to the destination substrate rather than tearing the active component into separate portions, one of which remains adhered to the destination substrate and another that remains with the source substrate. An active component can have multiple adhered portions adhered to the destination substrate.

In particular, in the case wherein the active component is an integrated circuit formed in a crystalline semiconductor material, the integrated circuit substrate provides sufficient cohesion, strength, and flexibility that it can adhere to the destination substrate without breaking as the source substrate is removed. In one embodiment of the present invention in which an integrated circuit active component is formed in a wafer substrate and released from the wafer by etching except for tethers connecting the integrated circuit to anchor areas in the source substrate (as shown in Figs. 10A and 10B), the active component can be advantageously adhered in the selected areas adjacent to the tethers to minimize the strain experienced by the active component integrated circuit when the source substrate is removed from the destination substrate to which the integrated circuit active component is adhered. Therefore, in some cases of the present invention, it is not necessary to adhere the entire selected active component to the destination substrate, providing an advantage as compared to some methods of the prior art.

In various methods of the present invention, laser beams are used to selectively cure the selected adhesive areas. In one embodiment, the selected areas can be sequentially exposed. In another embodiment, multiple areas can be simultaneously exposed; thereby increasing the number of selected active components simultaneously adhered. An alternative method employing a mask can also adhere

IPR2024-01134 - BOE
Exhibit 1009 - Page 216

multiple selected active components at one time, thereby increasing the rate at which destination substrates can be populated. Means known in the art for scanning and controlling lasers can be employed, as well as light sources used in conjunction with aligned masks, particularly as are known in the photo-lithographic arts.

The present invention provides advantages in comparison to other transfer methods that may be known in the art. For example, by locating an entire layer of selectively curable adhesive adjacent to the active components and destination substrate and only curing selected areas, there is no need for patterning adhesive over a substrate, a particularly important advantage for a large substrate. By employing adhesion over selected areas and active components capable of withstanding transfer stress, there is no need for ablation of material on which an active component is formed or that is formed on an active component, thereby reducing the likelihood of damage to the active components and rendering a difficult-to-control process unnecessary. Furthermore, there is no need to accurately shape or locate the energy used for ablation since the transferring active component can have sufficient mechanical cohesion to avoid cracking or breaking under the stress of transfer. Furthermore, the methods of the present invention can be robust in the presence of particulate contamination that is problematic for other traditional transfer methods.

In comparison to thin-film manufacturing methods, using densely populated source substrates and transferring active components to a destination wafer that requires only a sparse array of active components located thereon does not waste or require active layer material on a destination wafer. The present invention is also useful in transferring active components made with crystalline semiconductor materials that have much higher performance than thin-film active components. Furthermore, the flatness, smoothness, chemical stability, and heat stability requirements for a destination substrate useful in the present invention are greatly reduced because the adhesion and transfer process is not significantly limited by the destination substrate material properties. Manufacturing and material costs are reduced because of high utilization rates of expensive materials (e.g. the source substrate) and reduced material and processing requirements for the destination substrate.

IPR2024-01134 - BOE
Exhibit 1009 - Page 217

The invention has been described in detail herein with particular reference to certain embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

IPR2024-01134 - BOE
Exhibit 1009 - Page 218

CLAIMS:

1. A method for selectively transferring active components, the method comprising:

providing a curable adhesive layer between a receiving surface and a surface of a substrate including the active components thereon;

assembling the substrate on the receiving surface such that the curable adhesive layer contacts the active components and the receiving surface;

selectively curing portions of the curable adhesive layer in contact with ones of the active components without curing other portions thereof; and then

separating the substrate from the receiving surface such that the ones of the active components on the cured portions of the curable adhesive layer are transferred to the receiving surface.

2. The method of Claim 1, wherein an adhesive strength of the cured portions of the adhesive layer is greater than that used to releasably adhere the active components to the substrate.

3. The method of Claim 2, wherein the cured portions respectively comprise less than an entirety of a contact area between the respective ones of the active components and the adhesive layer.

4. The method of Claim 2, wherein the substrate comprises a source substrate, and wherein the active components are releasably adhered to the source substrate by a plurality of tethers.

5. The method of Claim 4, wherein providing a curable adhesive layer is preceded by:

providing a sacrificial layer and an active layer on the source substrate;

processing the active layer to define the active components and the plurality of tethers connecting the active components to anchor areas of the active layer;

removing portions of the sacrificial layer between the active components and the source substrate such that the active components are releasably adhered to the source substrate by the plurality of tethers.

IPR2024-01134 - BOE
Exhibit 1009 - Page 219

6. The method of Claim 5, wherein the plurality of tethers include an etch-resistant material, and wherein removing the portions of the sacrificial layer comprises:

selectively etching the sacrificial layer without substantially etching the plurality of tethers.

7. The method of Claim 4, wherein separating the substrate from the receiving surface comprises breaking ones of the plurality of tethers that are connected to the ones of the active components in contact with the cured portions of the adhesive layer.

8. The method of Claim 1, wherein selectively curing comprises selectively irradiating the portions of the curable adhesive layer with light, heat, and/or electromagnetic energy.

9. The method of Claim 8, wherein selectively irradiating comprises:

providing a mask that exposes the portions of the curable adhesive layer in contact with the ones of the active components; and

selectively irradiating the portions of the curable adhesive layer exposed by the mask.

10. The method of Claim 8, wherein the receiving surface comprises an at least partially transparent destination substrate, and wherein selectively irradiating comprises:

selectively transmitting a laser through the destination substrate to selectively irradiate the portions of the curable adhesive layer in contact with the ones of the active components.

11. The method of Claim 8, wherein the substrate and the active components are at least partially transparent, and wherein selectively irradiating comprises:

selectively transmitting a laser through the source substrate and the ones of the active components to selectively irradiate the portions of the curable adhesive layer.

12. The method of Claim 1, wherein the receiving surface comprises a a flexible and/or a polymer destination substrate.

13. The method of Claim 5, wherein the active layer comprises a crystalline, microcrystalline, polycrystalline, or amorphous semiconductor layer.

IPR2024-01134 - BOE
Exhibit 1009 - Page 220

14. The method of Claim 13, wherein the active layer has a thickness of greater than about 5 microns.

15. The method of Claim 1, wherein the substrate comprises a stamp, and wherein assembling the substrate on the receiving surface comprises pressing the stamp on the receiving surface.

16. The method of Claim 15, further comprising:

pressing the stamp on a source substrate including the active components releasably adhered thereto; and

separating the stamp from the source substrate to transfer the active components from the source substrate to the stamp prior to pressing the stamp on the receiving surface.

17. The method of Claim 16, wherein the active components are releasably adhered to the source substrate by a plurality of tethers, and wherein pressing the stamp on the source substrate comprises breaking ones of the plurality of tethers that are connected to the active components.

18. The method of Claim 16, wherein the stamp includes a second curable adhesive layer thereon, wherein the active components comprise first active components releasably adhered to the source substrate, wherein the source substrate further includes second active components releasably adhered thereto, and further comprising:

contacting the second curable adhesive layer with the first and second active components on the source substrate when pressing the stamp on the source substrate; and

selectively disabling portions of the second adhesive layer in contact with the second active components to delaminate the second active components from the stamp prior to separating the stamp from the source substrate.

19. The method of Claim 15, wherein the curable adhesive layer comprises a first adhesive layer, wherein the stamp includes a second adhesive layer thereon that releasably adheres the active components to the stamp, and further comprising:

selectively disabling portions of the second adhesive layer in contact with the ones of the active components prior to separating the stamp from the receiving surface,

IPR2024-01134 - BOE
Exhibit 1009 - Page 221

wherein an adhesive strength of the cured portions of the first adhesive layer is greater than that of the disabled portions of the second adhesive layer.

20. The method of Claim 1, wherein the ones of the active components transferred to the receiving surface comprise first ones of the active components transferred to a first area of the receiving surface, and further comprising the following after separating the substrate from the receiving surface:

aligning the substrate with a second area of the receiving surface, the substrate including second ones of the active components remaining thereon;

assembling the substrate on the second area of the receiving surface such that the curable adhesive layer contacts second ones of the active components and the receiving surface;

selectively curing second portions of the curable adhesive layer in contact with the second ones of the active components; and then

separating the substrate from the second area of the receiving surface such that the second ones of the active components on the cured second portions of the curable adhesive layer are transferred to the second area of the receiving surface.

21. The method of Claim 20, wherein aligning the substrate comprises moving the substrate in one or two dimensions relative to the receiving surface such that the first and second ones of the active components thereon define a one- or two-dimensional array of active components.

22. The method of Claim 1, wherein the curable adhesive layer is provided on the receiving surface or on the active components on the substrate.

23. The method of Claim 22, wherein the adhesive layer is provided on the active components, wherein the ones of the active components transferred to the receiving surface comprise first ones of the active components, and further comprising the following after separating the substrate from the receiving surface:

assembling the substrate including second ones of the active components remaining thereon on a second receiving surface such that the adhesive layer is in contact with the second ones of the active components and the second receiving surface; and

IPR2024-01134 - BOE
Exhibit 1009 - Page 222

selectively curing portions of the adhesive layer in contact with the second ones of the active components and then separating the substrate from the second receiving surface to transfer the second ones of the active components to the second receiving surface.

24. The method of Claim 22, wherein the adhesive layer is provided on the receiving surface, wherein the active components comprise first active components, and further comprising:

assembling a second substrate including second active components thereon on the receiving surface such that the adhesive layer contacts the second active components; and

selectively curing second portions of the adhesive layer in contact with the second active components and then separating the second substrate from the receiving surface to transfer the second active components to the receiving surface.

25. The method of Claim 1, wherein, after separating the substrate from the receiving surface, the method further comprises:

cleaning the substrate; and

providing second active components on the surface of the substrate for transfer to the receiving surface and/or another receiving surface.

26. A method for selectively transferring active components from a source substrate to a destination substrate, comprising the steps of:

a) providing a source substrate having an active side and one or more active components located on the active side of the source substrate;

b) providing a destination substrate having a receiving side;

c) locating a selectively curable adhesive layer between and adjacent to the receiving side of the destination substrate and the active side of the source substrate, the selectively curable adhesive layer having separate areas between each of the active component(s) and the receiving side of the destination substrate;

d) selecting one or more active components having corresponding selected areas;

e) selectively curing the adhesive layer in the selected area(s) of the adhesive layer corresponding to the selected active components to adhere the selected active components to the receiving side of the destination substrate in the selected areas; and

IPR2024-01134 - BOE
Exhibit 1009 - Page 223

f) removing the source substrate from the destination substrate leaving the selected active components adhered to the receiving side of the destination substrate in the selected areas.

27. A method for selectively transferring active components from a source substrate to a destination substrate, comprising the steps of:

a) providing a source wafer having a sacrificial layer formed over the source wafer and an active layer formed on the sacrificial layer;

b) processing the source wafer to form one or more active component(s) in or on the active layer and a trench around each of the active component(s), the trench extending through the active layer to the sacrificial layer;

c) removing the sacrificial layer except for breakable tethers to release the active components from the source substrate;

d) providing a destination substrate having a receiving side;

e) locating a selectively curable adhesive layer between and adjacent to the receiving side of the destination substrate and the active component side of the source wafer, the selectively curable adhesive layer having separate areas between each of the active component(s) and the receiving side of the destination substrate;

f) selecting one or more active components;

g) selectively curing the adhesive layer in selected area(s) of the adhesive layer corresponding to the selected active components to adhere the selected active components to the receiving side of the destination substrate in the selected area(s); and

h) breaking the tethers by removing the source substrate and the adhesive layer from the destination substrate leaving the selected active components adhered to the receiving side of the destination substrate in the selected area(s).

28. A method for selectively transferring active components from a source substrate to a destination substrate, comprising the steps of:

a) providing a source substrate having an active side and one or more active components located on the active side of the source substrate;

b) providing a destination substrate having a receiving side coated with a selectively curable adhesive;

c) providing a stamp;

IPR2024-01134 - BOE
Exhibit 1009 - Page 224

d) pressing the stamp against the active components to adhere the active components to the stamp;

e) stamping the active components onto the receiving side of the destination substrate to adhere the first active components to the receiving side of the destination substrate;

f) selectively curing the selectively curable adhesive layer in the areas corresponding to the active components;

g) removing the stamp from the destination substrate leaving the first active components adhered to the receiving side of the destination substrate.

29. A method for selectively transferring active components from a source substrate to a destination substrate, comprising the steps of:

a) providing a source substrate having an active side and one or more active components located on the active side of the source substrate;

b) providing a destination substrate having a receiving side;

c) providing a stamp;

d) locating a selectively adhesive layer between and adjacent to the stamp and the active side of the source substrate, the selectively adhesive layer having separate areas between each of the active component(s) and the stamp, thereby laminating the active components to the stamp;

e) selecting one or more first active components having corresponding first selected areas and one or more remaining second active components having corresponding second selected areas;

f) selectively delaminating the selectively adhesive layer in the second selected area(s) and removing the stamp from the source substrate leaving the first active components laminated to the stamp; and

g) stamping the first active components onto the receiving side of the destination substrate to adhere the first active components to the receiving side of the destination substrate;

h) removing the stamp from the destination substrate leaving the first active components adhered to the receiving side of the destination substrate.

IPR2024-01134 - BOE
Exhibit 1009 - Page 225

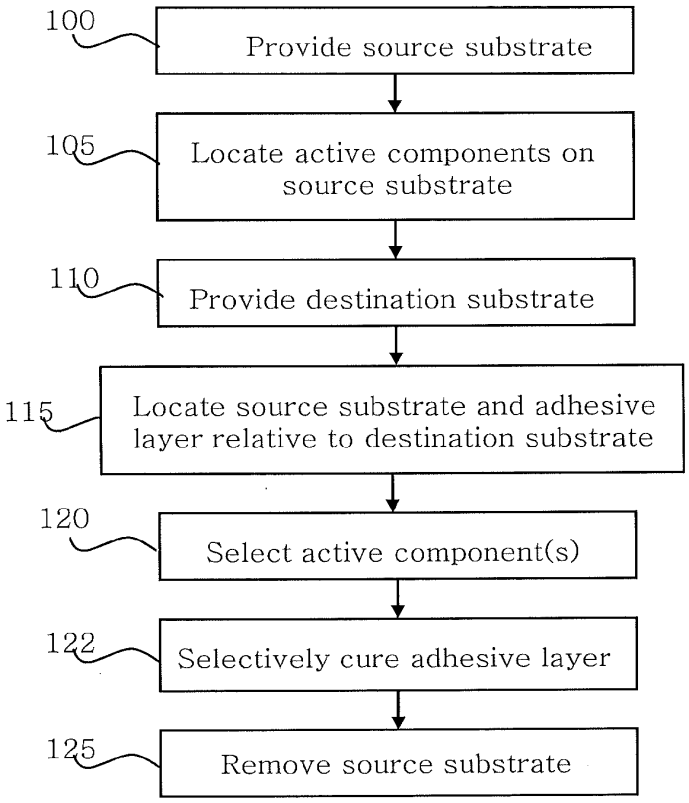

100
Provide source substrate
105
Locate active components on source substrate
110
Provide destination substrate
115
Locate source substrate and adhesive layer relative to destination substrate
120
Select active component(s)
122
Selectively cure adhesive layer
125
Remove source substrate

Fig. 1

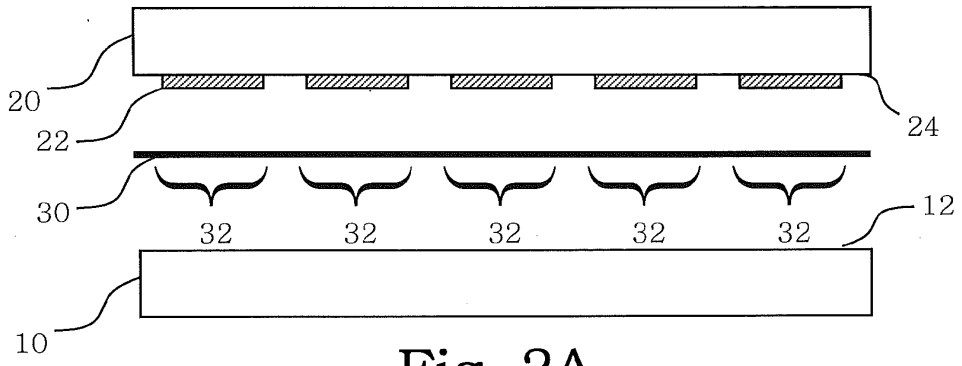


Fig. 2A

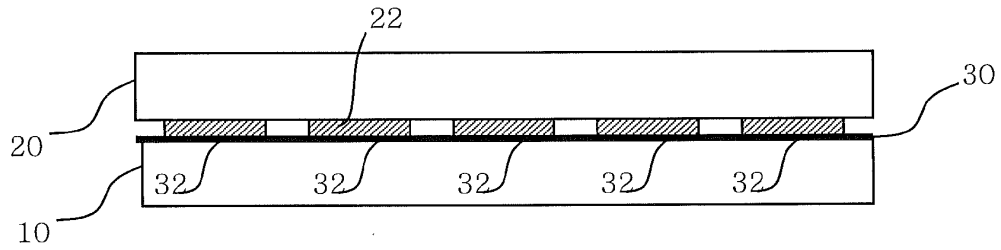


Fig. 2B

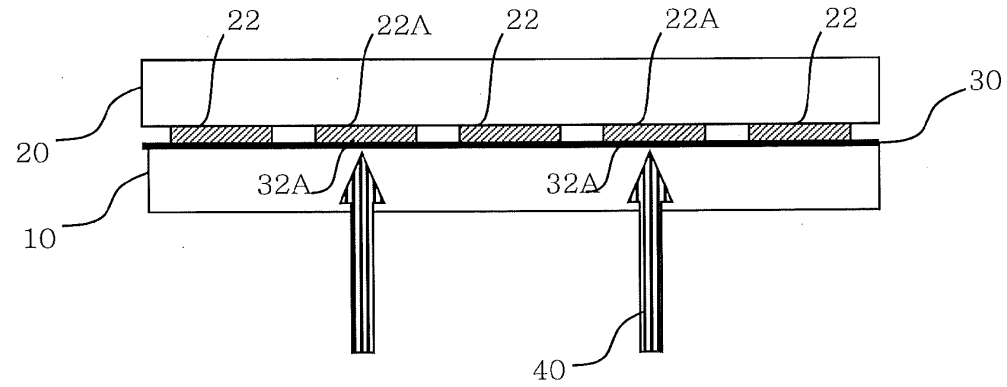


Fig. 2C

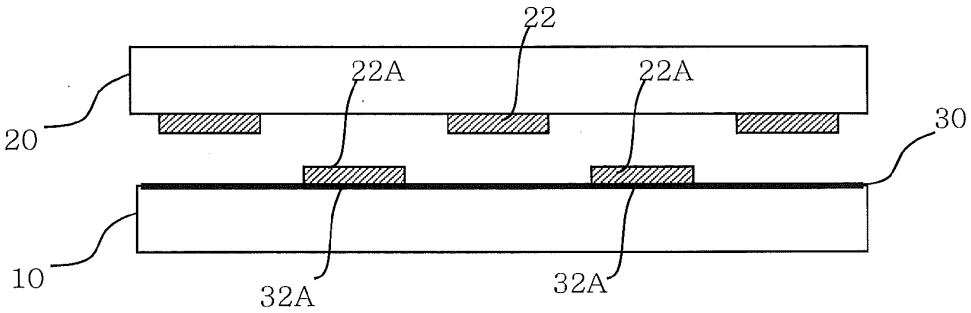


Fig. 2D

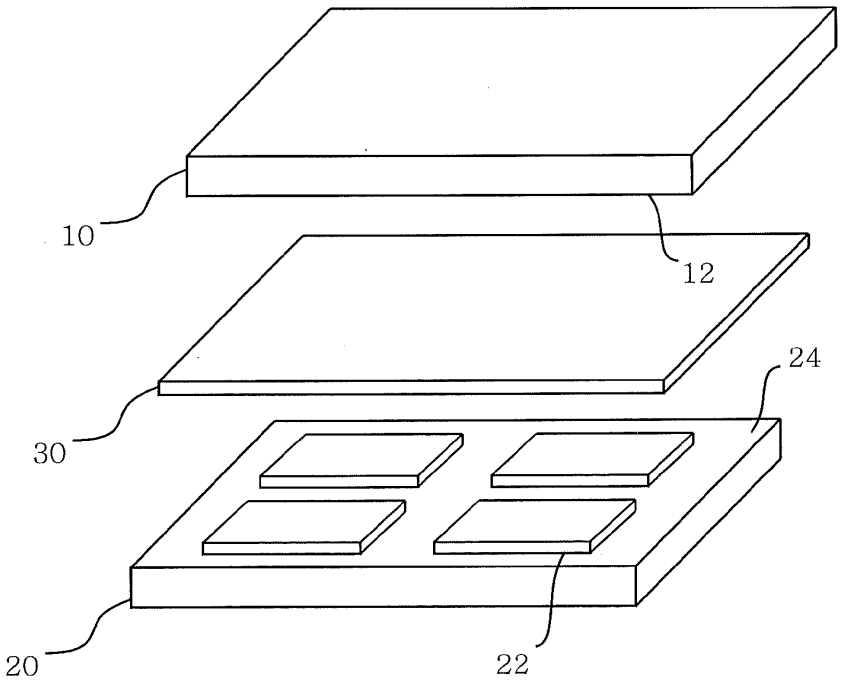


Fig. 3

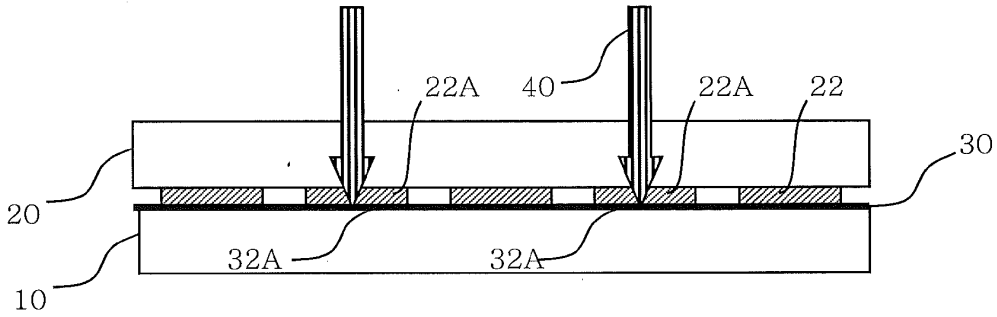


Fig. 4

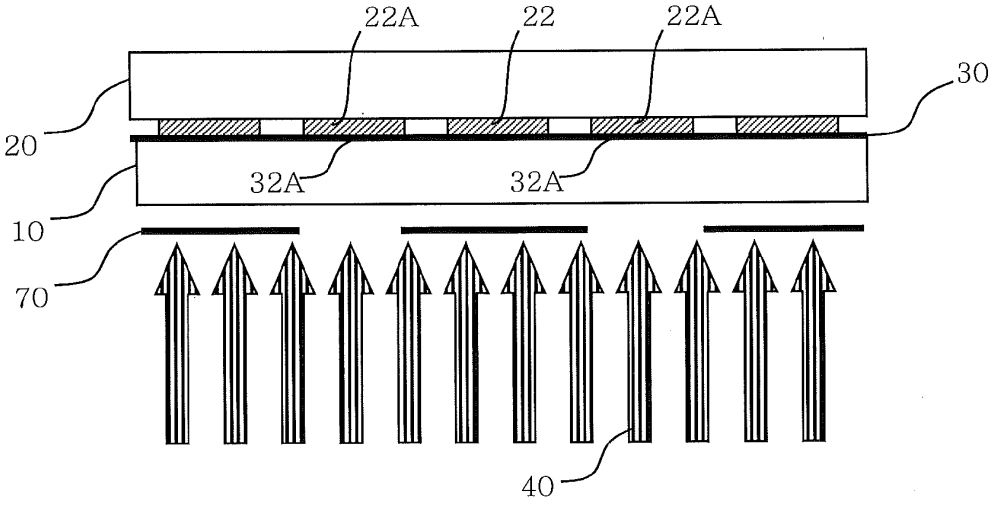


Fig. 5

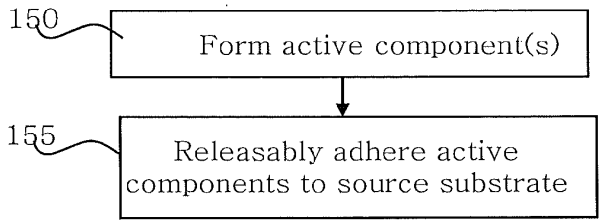

150
Form active component(s)
155
Releasably adhere active components to source substrate

Fig. 6

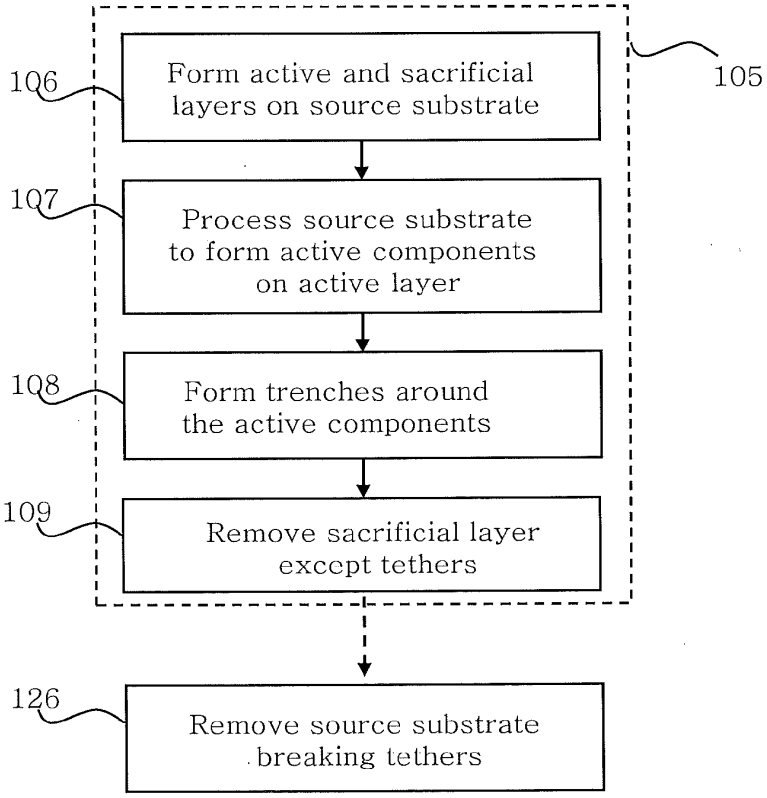

105
106
Form active and sacrificial layers on source substrate
107
Process source substrate to form active components on active layer
108
Form trenches around the active components
109
Remove sacrificial layer except tethers
126
Remove source substrate breaking tethers

Fig. 7

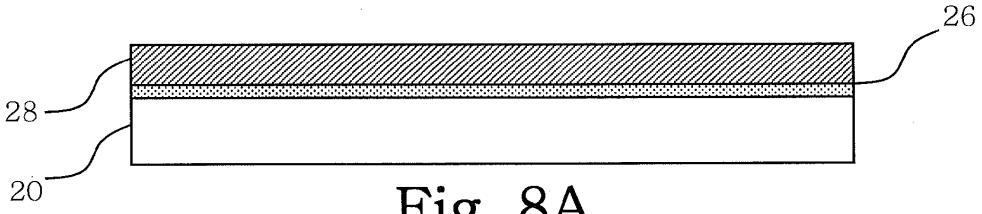


Fig. 8A

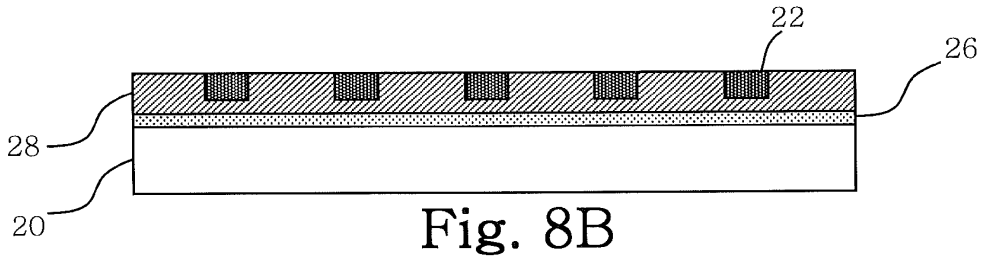


Fig. 8B

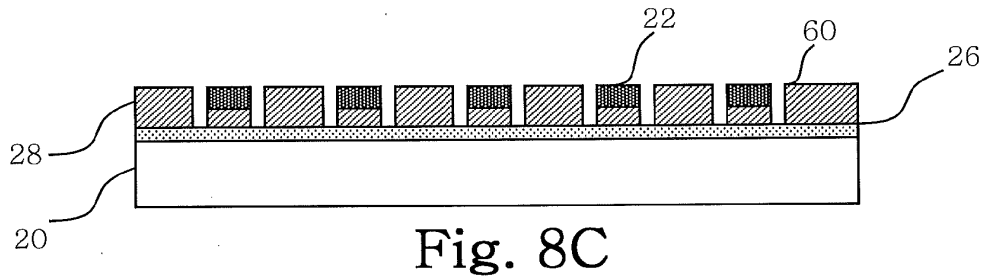


Fig. 8C

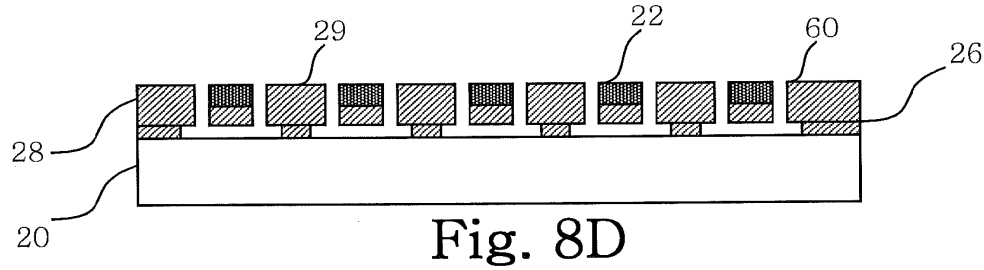


Fig. 8D

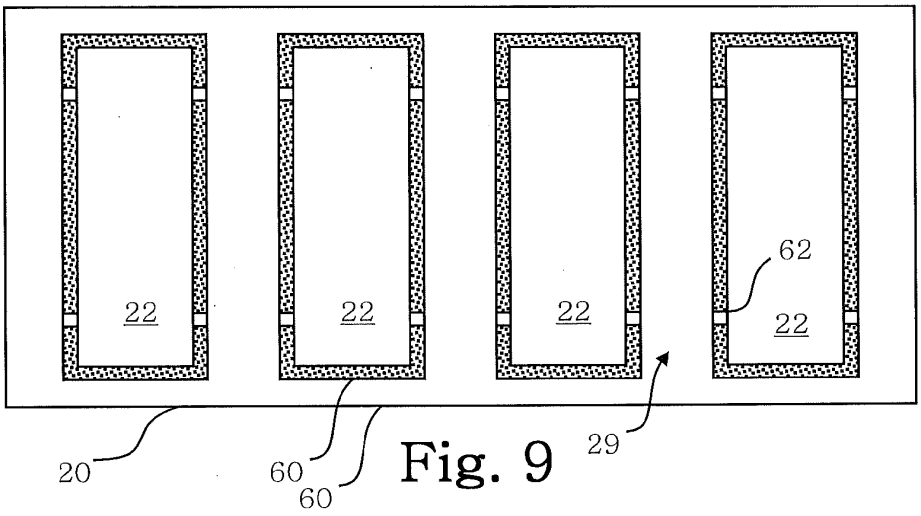


Fig. 9

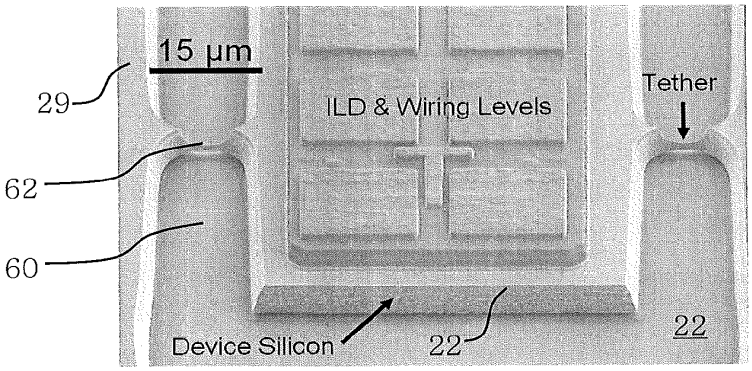


Fig. 10A

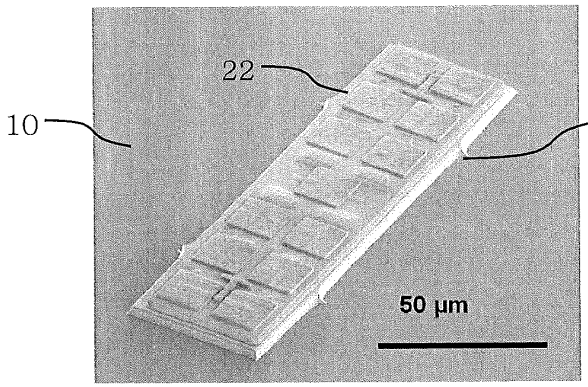


Fig. 10B

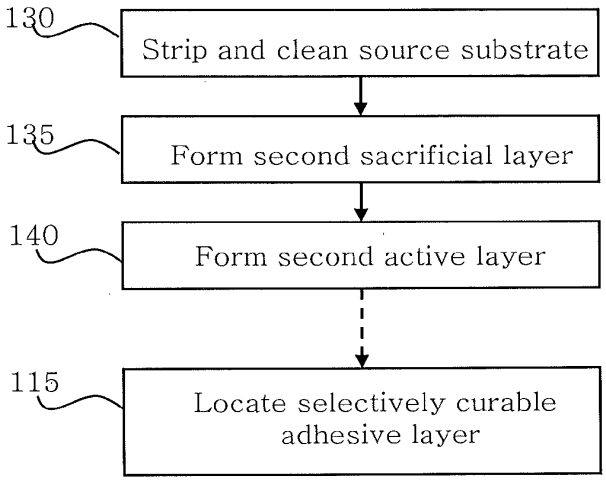

130
Strip and clean source substrate
135
Form second sacrificial layer
140
Form second active layer
115
Locate selectively curable adhesive layer

Fig. 11

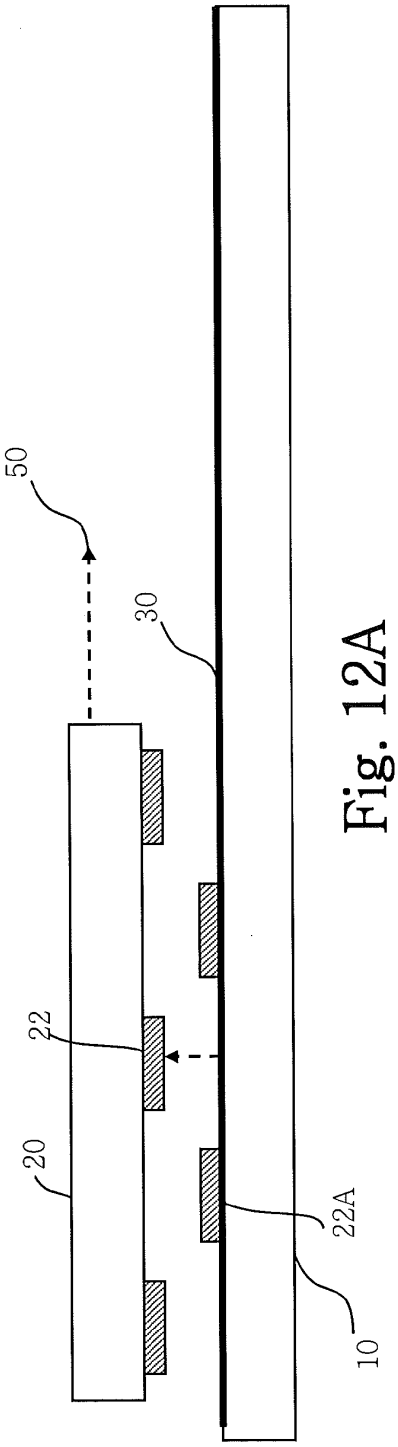


Fig. 12A

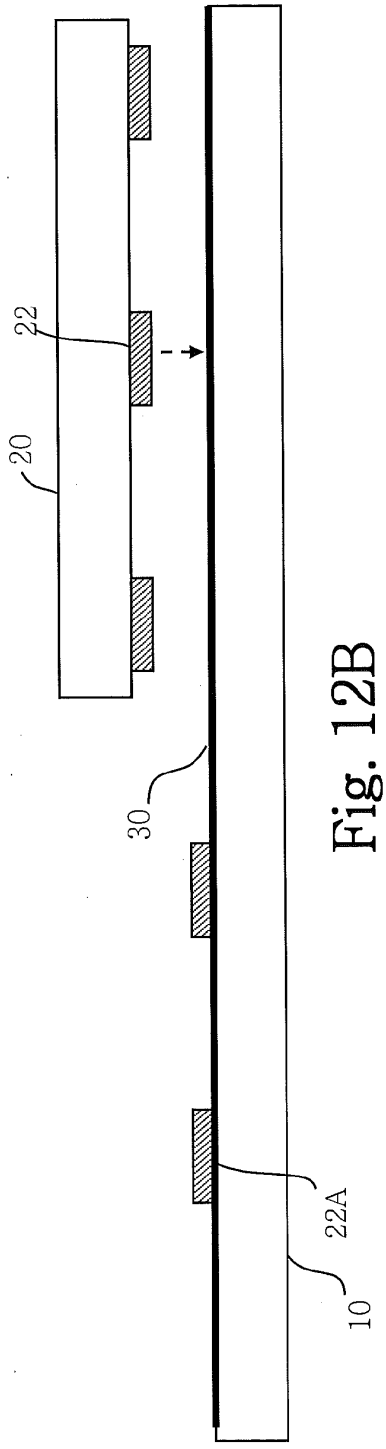


Fig. 12B

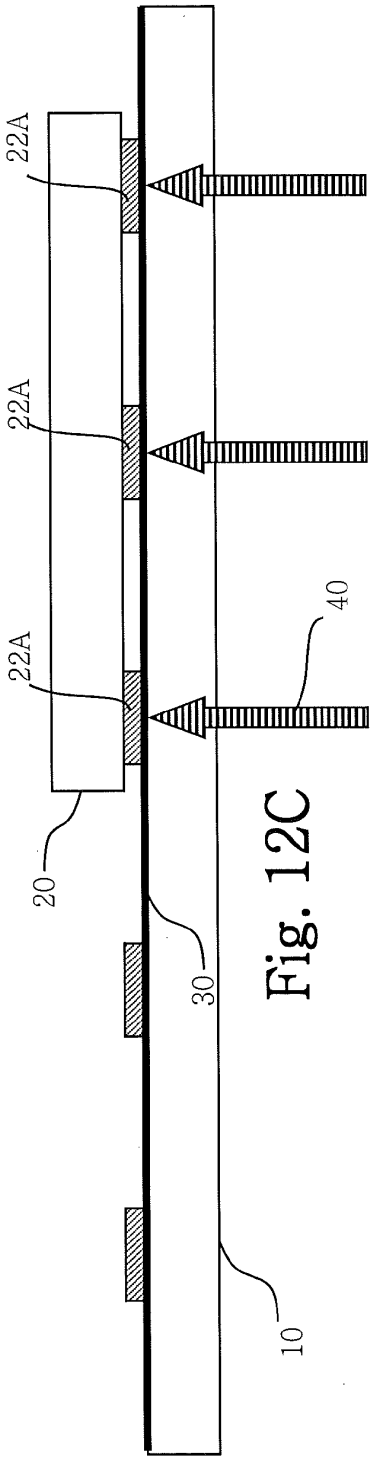


Fig. 12C

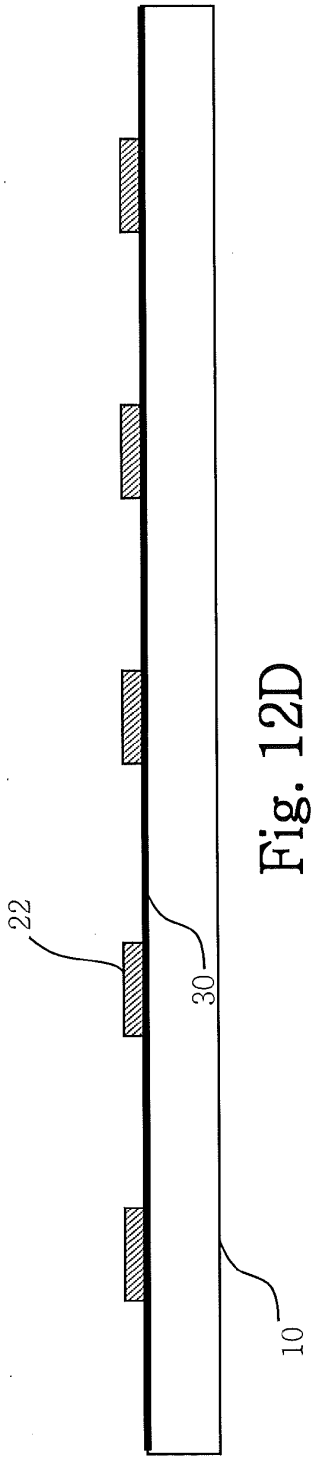


Fig. 12D

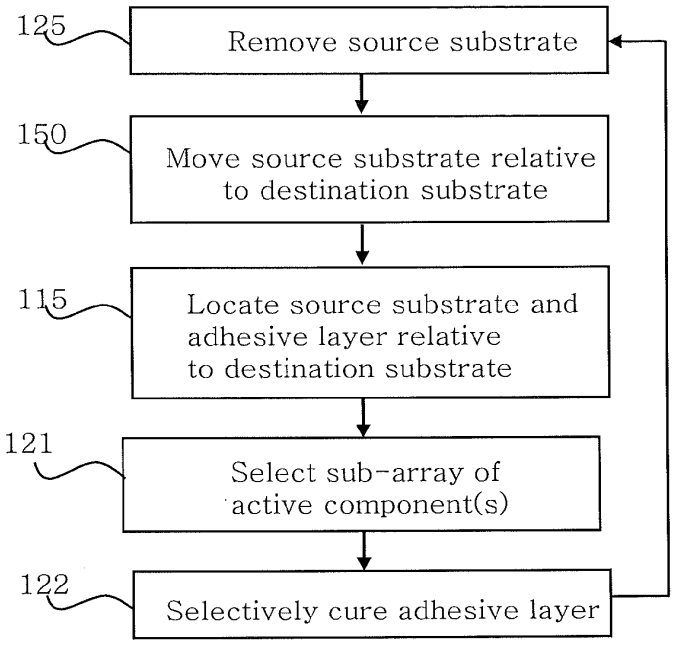

125
Remove source substrate
150
Move source substrate relative to destination substrate
115
Locate source substrate and adhesive layer relative to destination substrate
121
Select sub-array of active component(s)
122
Selectively cure adhesive layer

Fig. 13

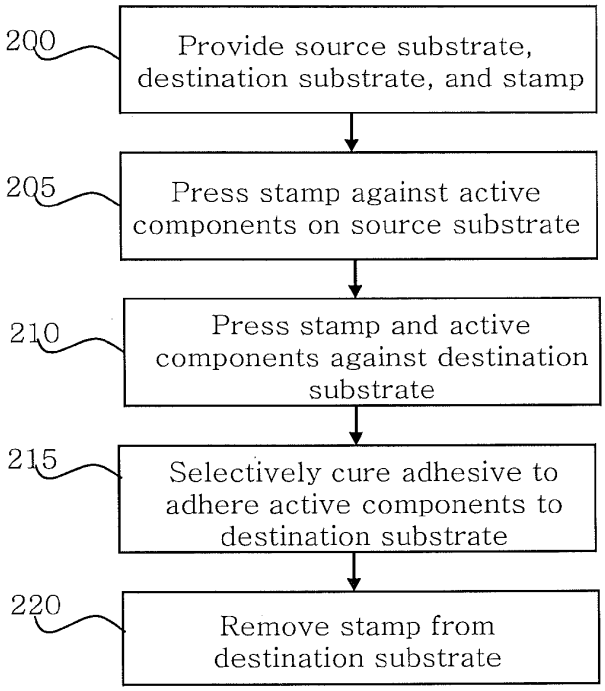

200
Provide source substrate, destination substrate, and stamp
205
Press stamp against active components on source substrate
210
Press stamp and active components against destination substrate
215
Selectively cure adhesive to adhere active components to destination substrate
220
Remove stamp from destination substrate

Fig. 14

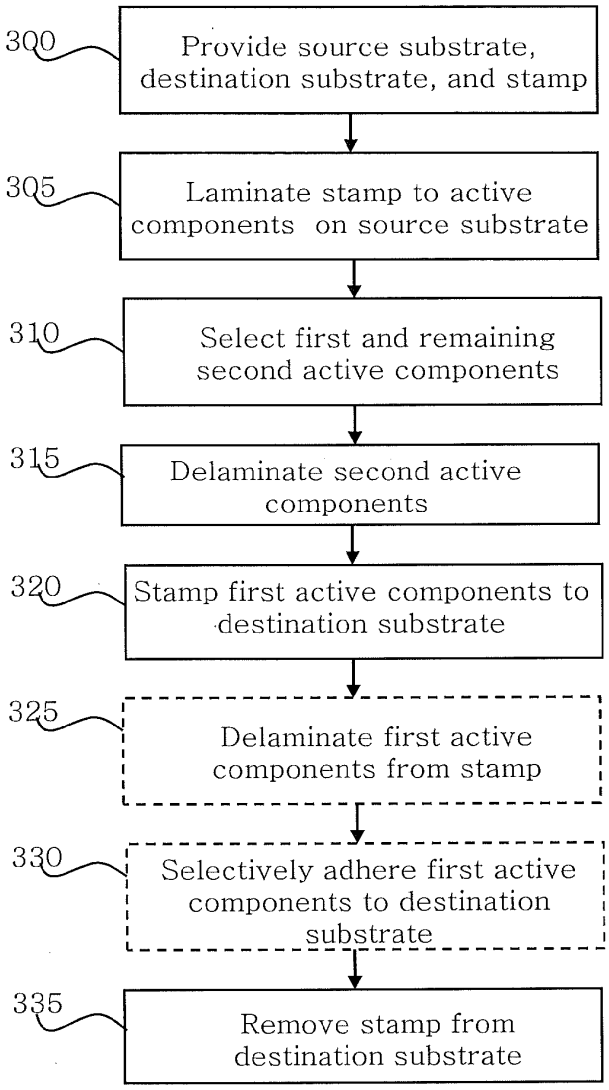

300
Provide source substrate, destination substrate, and stamp
305
Laminate stamp to active components on source substrate
310
Select first and remaining second active components
315
Delaminate second active components
320
Stamp first active components to destination substrate
325
Delaminate first active components from stamp
330
Selectively adhere first active components to destination substrate
335
Remove stamp from destination substrate

Fig. 15

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/029357

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/683
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/233546 A1 (OOHATA TOYOHARU [JP] ET AL) 20 October 2005 (2005-10-20)	1-3, 8-12,14, 15,19, 22,25,26
Y	figure 2 paragraphs [0002], [0064] - [0071]	4-7,13, 16,17, 20,21, 23,24, 27,28
	----- -/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 July 2011	27/07/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Crampin, Nicola

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/029357

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JOHN W HAMER RONALD S COK GARY J PARRETT DUSTIN WINTERS AND BRUNO PRIMERANO ET AL: "63.2: AMOLED Displays using Transfer-Printed Integrated Circuits", SID 2009, 2009 SID INTERNATIONAL SYMPOSIUM, SOCIETY FOR INFORMATION DISPLAY, LOS ANGELES, USA, vol. XXXX, 31 May 2009 (2009-05-31), pages 947-950, XP007017229, ISSN: 0009-966X cited in the application Section 1. - Section 2. -----	4-7,13, 16-18, 27-29
Y	US 2010/071206 A1 (KERR ROGER S [US] ET AL) 25 March 2010 (2010-03-25) figures 3, 4 paragraphs [0033], [0039] - [0057] -----	20,21, 23,24
Y	WO 2008/033680 A2 (AVERY DENNISON CORP [US]; KIAN KOUROCHE [US]; HE XIAOMING [US]; MEHRAB) 20 March 2008 (2008-03-20) figures 2-5 paragraphs [0046] - [0051] -----	18,29

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2011/029357

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005233546 A1	20-10-2005	JP 2003077940 A	14-03-2003
		US 2003087476 A1	08-05-2003
US 2010071206 A1	25-03-2010	WO 2010036324 A2	01-04-2010
WO 2008033680 A2	20-03-2008	US 2008122119 A1	29-05-2008

Form PCT/ISA/210 (patent family annex) (April 2005)

Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (09-12)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Andreas Bibl	Nonprovisional Application Number (if known):	
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i), the prioritized examination fee set forth in 37 CFR 1.17(c), and if not already paid, the publication fee set forth in 37 CFR 1.18(d) have been filed with the request. The basic filing fee, search fee, examination fee, and any required excess claims and application size fees are filed with the request or have been already been paid.

2. The application contains or is amended to contain no more than four independent claims and no more than thirty total claims, and no multiple dependent claims.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. The executed inventor's oath or declaration is filed with the application. (37 CFR 1.63 and 1.64)

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Jacob Aikin/	Date March 15, 2013
Name (Print/Typed) Jacob T. Aikin	Practitioner Registration Number 62,787

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

☐ *Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	9299P027
	Application Number	
Title of Invention	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME	

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Legal Name

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	Andreas		Bibl	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Los Altos	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	588 Harrington Ave.		
Address 2			
City	Los Altos	State/Province	CA
Postal Code	94024	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kapil	V.	Sakariya	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Sunnyvale	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	720 Sequoia Drive		
Address 2			
City	Sunnyvale	State/Province	CA
Postal Code	94086	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Charles	R.	Griggs	

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City	San Jose	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	2365 Cherrystone Dr.		
Address 2			
City	San Jose	State/Province	CA
Postal Code	95128	Country i	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	James	Michael	Perkins	

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City	Mountain View	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	707 Continental Cir.		
Address 2	Apt. 612		
City	Mountain View	State/Province	CA
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Title of the Invention	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME		
Attorney Docket Number	9299P027	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	30	Suggested Figure for Publication (if any)	

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Mailing Address Information:			
Address 1	1705 Wyatt Drive		
Address 2			
City	Santa Clara	**State/Province**	CA
Country i	US	Postal Code	95054
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UNITED STATES UTILITY PATENT APPLICATION

for

LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

Inventors:

Andreas Bibl, Kapil V. Sakariya, Charles R. Griggs, James Michael Perkins

Prepared by:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

1279 Oakmead Parkway

Sunnyvale, CA 94085-4040

(408) 720-8300

Attorney Docket No.: 9299P027

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LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

BACKGROUND

FIELD

[0001] Embodiments of the present invention relate to display systems. More particularly embodiments of the present invention relate to display systems incorporating micro light emitting diodes.

BACKGROUND INFORMATION

[0002] Flat panel displays are gaining popularity in a wide range of electronic devices. Common types of flat panel displays include active matrix displays and passive matrix displays. Each pixel in an active matrix display panel is driven by active driving circuitry, while each pixel in a passive matrix display panel does not use such driving circuitry. High-resolution color display panels, such as modern computer displays, smart phones and televisions typically use an active matrix display panel structure for better image quality.

[0003] One kind of display panel that is finding commercial application is an active matrix organic light emitting diode (AMOLED) display panel. FIG. 1 is a top view illustration of a top emission AMOLED display panel. FIG. 2 is a cross-sectional side view illustration of FIG. 1 taken along line X-X in the pixel area 104 and line Y-Y crossing the ground ring 116 in the non-pixel area which is any area on the substrate 102 not within the pixel area 104. The AMOLED display panel 100 illustrated in FIGS. 1-2 generally includes a thin film transistor (TFT) substrate 102 supporting a pixel area 104 and non-pixel area outside of the pixel area 102. A TFT substrate 102 is also referred to as a backplane. A TFT substrate which has been further processed to additionally include the pixel area and non-pixel area is also often referred to as a backplane. Two primary TFT substrate technologies used in AMOLEDs include polycrystalline silicon (poly-Si) and amorphous silicon (a-Si). These technologies offer the potential for fabricating the active matrix backplanes at low temperatures (below 200°C) directly onto flexible plastic substrates for producing flexible AMOLED displays. The pixel area 104 generally includes pixels 106 and subpixels 108 arranged in a matrix, and a set of TFTs and capacitors connected to each subpixel for driving and switching the subpixels. The non-pixel area generally includes a data driver circuit 110 connected to a data line

IPR2024-01134 - BOE
Exhibit 1009 - Page 252

of each subpixel to enable data signals (Vdata) to be transmitted to the subpixels, a scan driver circuit 112 connected to scan lines of the subpixels to enable scan signals (Vscan) to be transmitted to the subpixels, a power supply line 114 to transmit a power signal (Vdd) to the TFTs, and a ground ring 116 to transmit a ground signal (Vss) to the array of subpixels. As shown, the data driver circuit, scan driver circuit, power supply line, and ground ring are all connected to a flexible circuit board (FCB) 113 which includes a power source for supplying power to the power supply line 114 and a power source ground line electrically connected to the ground ring 116.

[0004] In the exemplary AMOLED backplane configuration an organic thin film 120 and top electrode 118 are deposited over every subpixel 108 in the pixel area 104. The organic thin film 120 may include multiple layers such as a hole injection layer, hole transport layer, light emitting layer, electron transport layer, and electron injection layer. The multiple layers of the organic thin film 120 are typically formed over the entire pixel area 104, however, the light emitting layer is often deposited with aid of a shadow mask only within the subpixel openings 127 and on the bottom electrode layer 124 corresponding to the emission area for the array of subpixels 108. A top electrode layer 118 is then deposited over the organic thin film within both the pixel area 104 and also within the non-pixel area so that the top electrode 118 layer overlaps the ground ring 116 in the in order to transfer the ground signal to the array of subpixels. In this manner, each of the subpixels 108 can be individually addressed with the corresponding underlying TFT circuitry while a uniform ground signal is supplied to the top of the pixel area 104.

[0005] In the particular implementation illustrated, the TFT substrate 102 includes a switching transistor T1 connected to a data line 111 from the data driver circuit 110 and a driving transistor T2 connected to a power line 115 connected to the power supply line 114. The gate of the switching transistor T1 may also be connected to a scan line (not illustrated) from the scan driver circuit 112. A planarization layer 122 is formed over the TFT substrate, and openings are formed to expose the TFT working circuitry. As illustrated, a bottom electrode layer 124 is formed on the planarization layer in electrical connection with the TFT circuitry. Following the formation of the electrode layer a pixel defining layer 125 is formed including an array of subpixel openings 127 corresponding to the emission area for the array of subpixels 108, followed by deposition of the organic layer 120 and top electrode layer 118 over the patterned pixel defining layer, and within subpixel openings 127 of the patterned pixel defining layer 125. The top electrode layer 118 additionally is formed in the non-pixel area and in electrical connection with the ground ring 116.

IPR2024-01134 - BOE
Exhibit 1009 - Page 253

[0006] The planarization layer 122 may function to prevent (or protect) the organic layer 120 and the bottom electrode layer 124 from shorting due to a step difference. Exemplary planarization layer 122 materials include benzocyclobutene (BCB) and acrylic. The pixel defining layer 125 can be formed of a material such as polyimide. The bottom electrode 124 is commonly formed on indium tin oxide (ITO), ITO/Ag, ITO/Ag/ITO, ITO/Ag/indium zinc oxide (IZO), or ITO/Ag alloy/ITO. The top electrode layer 118 is formed of a transparent material such as ITO for top emission.

[0007] While AMOLED display panels generally consume less power than liquid crystal display (LCD) panels, an AMOLED display panel can still be the dominant power consumer in battery-operated devices. To extend battery life, it is necessary to reduce the power consumption of the display panel.

SUMMARY OF THE INVENTION

[0008] A display panel with redundancy scheme and method of manufacture are described. In an embodiment, a display panel includes a display substrate with a pixel area and a non-pixel area. The pixel area includes an array of subpixels and a corresponding array of bottom electrodes within the array of subpixels. An array of micro LED devices pairs are bonded to the array of bottom electrodes, and one or more top electrodes are formed in electrical contact with the array of micro LED device pairs. The micro LED devices may be formed of a semiconductor material, and may have a maximum width of 1 to 100 μm.

[0009] In one application, the display substrate can be a TFT substrate. A ground line may be formed in the non-pixel area of the TFT substrate, and the one or more of the top electrode layers are electrically connected to the ground line. In one embodiment, a first to electrode layer electrically connects a first micro LED device of a micro LED device pair to the ground line, and a separate second top electrode layer electrically connects a second micro LED device of the micro LED device pair to the ground line.

[0010] In one application, an array of micro controller chips are bonded to the display substrate, with each bottom electrode electrically connected to a micro controller chip. Each micro controller chip can be connected to a scan driver circuit and a data driver circuit. A ground line may run in the non-pixel area of the display substrate, and the one or more of the top electrode layers are electrically connected to the ground line. In one embodiment, a first top electrode layer electrically connects a first micro LED device of a micro LED device pair to the ground line, and a separate

IPR2024-01134 - BOE
Exhibit 1009 - Page 254

second top electrode layer electrically connects a second micro LED device of the micro LED device pair to the ground line.

[0011] In an embedment, a plurality of micro LED device irregularities are within the array of micro LED device pairs. For example, the irregularities can be missing micro LED devices, defective micro LED devices, and contaminated micro LED devices. A passivation layer material can be used to cover the plurality of irregularities, and to electrically insulate the plurality of irregularities. The passivation layer material may also be used to cover sidewalls (e.g. including a quantum well structure) of the array of micro LED device pairs. In one embodiment the one or more top electrode layers do not make electrical contact with the plurality of irregularities, even where the one or more tope electrode layers are formed directly over the plurality of irregularities. The one or more top electrode layers may also be formed elsewhere, or formed around the plurality of irregularities so that they are not formed directly over the plurality of irregularities. In an embodiment, a repair micro LED device is bonded to one of the bottom electrodes including one of the micro LED device irregularities.

[0012] In an embodiment, a method of forming a display panel includes an integrated test to detect irregularities in the array of micro LED devices. An array of micro LED deivces can be electrostatically transferred from one or more carrier substrates to a corresponding array of bottom electrodes within a corresponding array of subpixels on a display substrate. The surface of the display substrate is then imaged to detect irregularities in the array of micro LED devices, and a passivation layer material is then formed over a plurality of detected irregularities to electrically insulate the plurality of irregularities. One or more top electrode layers can then be formed in electrical contact with the array of micro LED devices without making electrical contact with the plurality of irregularities. In some embodiment, the passivation layer material is formed over the plurality of irregularities by ink jet printing or screen printing, and the one or more top electrode layers are formed by ink jet printing or screen printing. In an embodiment, the one or more top electrode layers are separate top electrode layers. In another embodiment, one of the separate top electrode layers is scribed to cut off an electrical path to a ground line.

[0013] Imaging the surface of the display substrate may be performed with a camera. In an embodiment, an image produced from the camera is used to detect irregularities such as missing micro LED devices or contaminated micro LED devices. In an embodiment, imaging includes illuminating the surface of the display substrate with a light source to cause the array of micro LED devices to fluoresce, and imaging the fluorescence of the array of micro LED devices with the

camera. An image produced form the camera imaging fluorescence can be used to detect defective micro LED devices.

[0014] In an embodiment, a plurality of repair micro LED devices can be transferred to the display substrate adjacent (e.g. on the same bottom electrodes) the plurality of irregularities prior to forming the passivation layer material over the plurality of irregularities. This can then be followed by forming one or more top electrode layers in electrical contact with the array of micro LED devices and the plurality of repair micro LED devices, without making electrical contact with the plurality of irregularities.

[0015] In an embodiment a method of forming a display panel with redundancy scheme includes electrostatically transferring an array of micro LED device pairs from one or more carrier substrates to a corresponding array of bottom electrodes within a corresponding array of subpixels on a display substrate. The surface of the display substrate is then imaged to detect irregularities in the array of micro LED device pairs. A passivation layer material may then be formed over a plurality of detected irregularities to electrically insulate the plurality of irregularities. One or more top electrode layers are then formed in electrical contact with the array of micro LED device pairs.

[0016] One manner for electrostatic transfer includes electrostatically transferring a first array of micro LED devices from a first area of a first carrier substrate to the display substrate, and electrostatically transferring a second array of micro LED devices from a second area of the first carrier substrate to the display substrate. For example, the first and second areas do not overlap in one embodiment to reduce the probability of correlated defects being transferred to the same subpixel. Another manner for electrostatic transfer includes electrostatically transferring the first and second arrays of micro LED devices from different carrier substrates. In accordance with embodiments of the invention, electrostatic transfer can include electrostatically transferring each micro LED device with a separate electrostatic transfer head.

[0017] In an embodiment, imaging the surface of the display surface comprises imaging with a camera. For example, a line scan camera may be used. In an embodiment, an image produced from the camera is used to detect irregularities in the array of micro LED device pairs, such as missing micro LED devices or contaminated micro LED devices. In an embodiment, imaging the surface of the display substrate further includes illuminating the surface of the display substrate with a light source to cause the array of micro LED device pairs to fluoresce, and imaging the fluorescence of the array of micro LED device pairs with the camera to detect defective micro LED devices.

[0018] In an embodiment, a single top electrode layer is formed over the array of micro LED device pairs, including the irregularities. The passivation layer material can cover the irregularities so that the top electrode layer is not in electrical contact the irregularities.

[0019] In an embodiment, a plurality of separate top electrode layers are formed over the array of micro LED device pairs. The passivation layer material can be used to electrically insulate the irregularities from the top contact layers when formed directly over the irregularities. The top contact layers can also be formed around the irregularities so that they are not directly over the irregularities. Ink jet printing and screen printing may be suitable deposition methods for forming both the passivation layer material, as well as the top electrode layers. In an embodiment, a plurality of repair micro LED devices are transferred to the display substrate adjacent the plurality of irregularities prior to forming the passivation layer material over the plurality of irregularities. The top electrode layers may also be formed over and in electrical contact with the repair micro LED devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 is a top view illustration of a top emission AMOLED display panel.

[0021] FIG. 2 is a side-view illustration of the top emission AMOLED display panel of FIG. 1 taken along lines X-X and Y-Y.

[0022] FIG. 3A is a top view illustration of an active matrix display panel in accordance with an embodiment of the invention.

[0023] FIG. 3B is a side-view illustration of the active matrix display panel of FIG. 3A taken along lines X-X and Y-Y in accordance with an embodiment of the invention.

[0024] FIG. 3C is a side-view illustration of the active matrix display panel of FIG. 3A taken along lines X-X and Y-Y in accordance with an embodiment of the invention in which ground tie lines and ground ring are formed within a patterned bank layer.

[0025] FIG. 3D is a side-view illustration of the active matrix display panel of FIG. 3A taken along lines X-X and Y-Y in accordance with an embodiment of the invention in which ground tie lines and ground ring are formed below a patterned bank layer.

[0026] FIGS. 4A-4H are cross-sectional side view illustrations for a method of transferring an array of micro LED devices to a TFT substrate in accordance with an embodiment of the invention.

[0027] FIGS. 5A-5F are top view illustrations for a sequence of transferring an array of micro LED devices with different color emissions in accordance with an embodiment of the invention.

IPR2024-01134 - BOE
Exhibit 1009 - Page 257

[0028] FIG. 6A is a top view illustration of an active matrix display panel after the formation of a top electrode layer in accordance with an embodiment.

[0029] FIG. 6B is a top view illustration of an active matrix display panel after the formation of separate top electrode layers in accordance with an embodiment.

[0030] FIG. 6C is a side-view illustration of the active matrix display panel of either FIG. 6A or FIG. 6B taken along lines X-X and Y-Y in accordance with an embodiment of the invention.

[0031] FIG. 6D is a side-view illustration of the active matrix display panel of either FIG. 6A or FIG. 6B taken along lines X-X and Y-Y in accordance with an embodiment of the invention.

[0032] FIG. 7 is a top view schematic illustration of a smart pixel display including a redundancy and repair site configuration in accordance with an embodiment of the invention.

[0033] FIG. 8A is a schematic side view illustration of testing apparatus including a light source and camera in accordance with an embodiment of the invention.

[0034] FIG. 8B is a schematic top view illustration of a scanning pattern in accordance with an embodiment of the invention.

[0035] FIG. 9 is a cross-sectional side view illustration of an exemplary structure that can be formed after detection of a defective micro LED device in accordance with an embodiment of the invention.

[0036] FIG. 10 is a cross-sectional side view illustration of an exemplary structure that can be formed after detection of a missing micro LED device in accordance with an embodiment of the invention.

[0037] FIG. 11 is a cross-sectional side view illustration of an exemplary structure that can be formed after detection of a defective micro LED device in accordance with an embodiment of the invention

[0038] FIG. 12 is a cross-sectional side view illustration of an exemplary structure that can be formed after detection of a missing micro LED device in accordance with an embodiment of the invention.

[0039] FIG. 13 is a top schematic view illustration of a top electrode layer formed over an array of micro LED devices including a variety of configurations in accordance with an embodiment of the invention.

[0040] FIG. 14 is a top schematic view illustration of a plurality of separate top electrode layers formed over an array of micro LED devices including a variety of configurations in accordance with an embodiment of the invention.

[0041] FIG. 15 is a top schematic view illustration of a plurality of separate top electrode layers formed over an array of micro LED devices including a variety of configurations in accordance with an embodiment of the invention.

[0042] FIG. 16 is a top schematic view illustration of a scribed top electrode layer in accordance with an embodiment of the invention.

[0043] FIG. 17 is a top schematic view illustration of a scribed bottom electrode layer in accordance with an embodiment of the invention.

[0044] FIG. 18 is a schematic illustration of a display system in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0045] Embodiments of the present invention relate to display systems. More particularly embodiments of the present invention relate to a display with a redundancy scheme of light emitting diodes.

[0046] In one aspect, embodiments of the invention describe an active matrix display panel including wafer-based emissive micro LED devices. A micro LED device combines the performance, efficiency, and reliability of wafer-based LED devices with the high yield, low cost, mixed materials of thin film electronics used to form AMOLED backplanes. The terms "micro" device or "micro" LED structure as used herein may refer to the descriptive size of certain devices or structures in accordance with embodiments of the invention. As used herein, the terms "micro" devices or structures are meant to refer to the scale of 1 to 100 μm. However, it is to be appreciated that embodiments of the present invention are not necessarily so limited, and that certain aspects of the embodiments may be applicable to larger, and possibly smaller size scales. In an embodiment, a display panel is similar to a typical OLED display panel, with a micro LED device having replaced the organic layer of the OLED display panel in each subpixel. Exemplary micro LED devices which may be utilized with some embodiments of the invention are described in U.S. Patent Application No. 13/372,222, U.S. Patent Application No. 13/436,260, U.S. Patent Application No. 13/458,932, U.S. Patent Application No. 13/711,554, and U.S. Patent Application No. 13/749,647 all of which are incorporated herein by reference. The micro LED devices are highly efficient at light emission and consume very little power (e.g., 250 mW for a 10 inch diagonal display) compared to 5-10 watts for a 10 inch diagonal LCD or OLED display, enabling reduction of power consumption of the display panel.

[0047] In another aspect, embodiments of the invention describe a redundancy scheme in which a plurality of bonding sites are available for bonding a plurality of micro LED devices on each bottom electrode, for example, within each bank opening for a subpixel. In an embodiment, the redundancy scheme includes at one or more bonding layers (e.g. indium posts) at bonding sites on the bottom electrode within a bank opening, with each bonding layer designed to receive a separate micro LED device. In an embodiment, the redundancy scheme can also include a repair bonding site within the bank opening that is large enough to receive a micro LED device. The repair bonding site may also optionally include a bonding layer. In this manner, in an embodiment, each bank opening may correspond to a single emission color of a subpixel, and receives a plurality of micro LED devices of the emission color. If one of the micro LED devices bonded to one of the bonding layers is defective, then the other micro LED device compensates for the defective micro LED device. In addition, the repair bonding site may be used to bond an additional micro LED device if desired. In this manner, a redundancy and repair configuration is integrated into a backplane structure which can improve emission uniformity across the display panel without having to alter the underlying TFT architecture already incorporated in conventional AMOLED displays.

[0048] In another aspect, embodiments of the invention describe an integrated test method for detecting defective, missing, or contaminated micro LED devices after transfer of the micro LED devices from a carrier substrate to display substrate. In this manner, detection of defective, missing, or contaminated micro LED devices can be used to potentially transfer replacement micro LED devices where required, alter subsequent processing involved with passivating the micro LED devices and bottom electrodes, or alter subsequent processing involved with forming the top electrode layers. Furthermore, the integrated test method can be implemented into the fabrication process so that it is not necessary to provide a top electrical contact on the micro LED devices for testing, and a testing can be performed without separate electrical tests.

[0049] In various embodiments, description is made with reference to figures. However, certain embodiments may be practiced without one or more of these specific details, or in combination with other known methods and configurations. In the following description, numerous specific details are set forth, such as specific configurations, dimensions and processes, etc., in order to provide a thorough understanding of the present invention. In other instances, well-known semiconductor processes and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the present invention. Reference throughout this specification to "one embodiment" means that a particular feature, structure, configuration, or characteristic described in

IPR2024-01134 - BOE
Exhibit 1009 - Page 260

connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase "in one embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, configurations, or characteristics may be combined in any suitable manner in one or more embodiments.

[0050] The terms "spanning", "over", "to", "between" and "on" as used herein may refer to a relative position of one layer with respect to other layers. One layer "spanning", "over" or "on" another layer or bonded "to" or in "contact" with another layer may be directly in contact with the other layer or may have one or more intervening layers. One layer "between" layers may be directly in contact with the layers or may have one or more intervening layers.

[0051] It is to be appreciated that the following description is made specifically with regard to active matrix display panels. However, embodiments are not so limited. In particular, embodiments describing a redundancy scheme, repair site, and testing method for detecting defective, missing, or contaminated micro LED devices can also be implemented into passive matrix display panels, as well as substrates for lighting purposes.

[0052] Referring now to FIGS. 3A-3B an embodiment is illustrated in which a backplane similar to an AMOLED backplane is modified to receive emissive micro LED devices rather than an organic emission layer. FIG. 3A is a top view illustration of an active matrix display panel in accordance with an embodiment, and FIG. 3B is a side-view illustration of the active matrix display panel of FIG. 3A taken along lines X-X and Y-Y in accordance with an embodiment of the invention. In such an embodiment, the underlying TFT substrate 102 can be similar to those in a typical AMOLED backplane described with regard to FIGS. 1-2 including working circuitry (e.g. T1, T2) and planarization layer 122. Openings 131 may be formed in the planarization layer 122 to contact the working circuitry. The working circuitry can include traditional 2T1C (two transistors, one capacitor) circuits including a switching transistor, a driving transistor, and a storage capacitor. It is to be appreciated that the 2T1C circuitry is meant to be exemplary, and that other types of circuitry or modifications of the traditional 2T1C circuitry are contemplated in accordance with embodiments of the invention. For example, more complicated circuits can be used to compensate for process variations of the driver transistor and the light emitting device, or for their instabilities. Furthermore, while embodiments of the invention are described and illustrated with regard to top gate transistor structures in the TFT substrate 102, embodiments of the invention also contemplate the use of bottom gate transistor structures. Likewise, while embodiments of the invention are

described and illustrated with regard to a top emission structure, embodiments of the invention also contemplate the use of bottom, or both top and bottom emission structures. In addition, embodiments of the invention are described and illustrated below specifically with regard to a high side drive configuration including ground tie lines and ground ring. In a high side drive configuration a LED may be on the drain side of a PMOS driver transistor or a source side of an NMOS driver transistor so that the circuit is pushing current through the p-terminal of the LED. Embodiments of the invention are not so limited may also be practiced with a low side drive configuration in which case the ground tie lines and ground ring become the power line in the panel and current is pulled through the n-terminal of the LED.

[0053] A patterned bank layer 126 including bank openings 148 is then formed over the planarization layer 122. Bank layer 126 may be formed by a variety of techniques such as ink jet printing, screen printing, lamination, spin coating, CVD, and PVD. Bank layer 126 may be may be opaque, transparent, or semi-transparent to the visible wavelength. Bank layer 126 may be formed of a variety of insulating materials such as, but not limited to, photo-definable acrylic, photoresist, silicon oxide (SiO_2), silicon nitride (SiN_x), poly(methyl methacrylate) (PMMA), benzocyclobutene (BCB), polyimide, acrylate, epoxy, and polyester. In an embodiment, bank player is formed of an opaque material such as a black matrix material. Exemplary insulating black matrix materials include organic resins, glass pastes, and resins or pastes including a black pigment, metallic particles such as nickel, aluminum, molybdenum, and alloys thereof, metal oxide particles (e.g. chromium oxide), or metal nitride particles (e.g. chromium nitride).

[0054] In accordance with embodiments of the invention, the thickness of the bank layer 126 and width of the bank openings 128 described with regard to the following figures may depend upon the height of the micro LED devices to be mounted within the opening, height of the transfer heads transferring the micro LED devices, and resolution. In an embodiment, the resolution, pixel density, and subpixel density of the display panel may account for the width of the bank openings 128. For an exemplary 55 inch television with a 40 PPI (pixels per inch) and 211 μm subpixel pitch, the width of the bank openings 128 may be anywhere from a few microns to 206 μm to account for an exemplary 5 μm wide surrounding bank structure. For an exemplary display panel with 440 PPI and a 19 μm subpixel pitch, the width of the bank openings 128 may be anywhere from a few microns to 14 μm to account for an exemplary 5 μm wide surrounding bank structure. Width of the bank structure (i.e. between bank openings 128) may be any suitable size, so long as the structure supports the required processes and is scalable to the required PPI.

IPR2024-01134 - BOE
Exhibit 1009 - Page 262

[0055] In accordance with embodiments of the invention, the thickness of the bank layer 126 is not too thick in order for the bank structure to function. Thickness may be determined by the micro LED device height and a predetermined viewing angle. For example, where sidewalls of the bank openings 128 make an angle with the planarization layer 122, shallower angles may correlate to a wider viewing angle of the system. In an embodiment, exemplary thicknesses of the bank layer 126 may be between 1 μm – 50 μm.

[0056] A patterned conductive layer is then formed over the patterned bank layer 126. Referring to FIG. 3B, in one embodiment the patterned conductive layer includes bottom electrodes 142 formed within the bank openings 148 and in electrical contact with the working circuitry. The patterned conductive layer may also optionally include the ground tie lines 144 and/or the ground ring 116. As used herein the term ground "ring" does not require a circular pattern, or a pattern that completely surrounds an object. Rather, the term ground "ring" means a pattern that at least partially surrounds the pixel area on three sides. In addition, while the following embodiments are described and illustrated with regard to a ground ring 116, it is to be appreciated that embodiments of the invention can also be practiced with a ground line running along one side (e.g. left, right, bottom, top), or two sides (a combination of two of the left, right, bottom, top) of the pixel area. Accordingly, it is to be appreciated that in the following description the reference to and illustration of a ground ring, could potentially be replaced with a ground line where system requirements permit.

[0057] The patterned conductive layer may be formed of a number of conductive and reflective materials, and may include more than one layer. In an embodiment, a patterned conductive layer comprises a metallic film such as aluminum, molybdenum, titanium, titanium-tungsten, silver, or gold, or alloys thereof. The patterned conductive layer may include a conductive material such as amorphous silicon, transparent conductive oxides (TCO) such as indium-tin-oxide (ITO) and indium-zinc-oxide (IZO), carbon nanotube film, or a transparent conducting polymer such as poly(3,4-ethylenedioxythiophene) (PEDOT), polyaniline, polyacetylene, polypyrrole, and polythiophene. In an embodiment, the patterned conductive layer includes a stack of a conductive material and a reflective conductive material. In an embodiment, the patterned conductive layer includes a 3-layer stack including top and bottom layers and a reflective middle layer wherein one or both of the top and bottom layers are transparent. In an embodiment, the patterned conductive layer includes a conductive oxide-reflective metal-conductive oxide 3-layer stack. The conductive oxide layers may be transparent. For example, the patterned conductive layer may include an ITO-

IPR2024-01134 - BOE
Exhibit 1009 - Page 263

silver-ITO layer stack. In such a configuration, the top and bottom ITO layers may prevent diffusion and/or oxidation of the reflective metal (silver) layer. In an embodiment, the patterned conductive layer includes a Ti-Al-Ti stack, or a Mo-Al-Mo-ITO stack. In an embodiment, the patterned conductive layer includes a ITO-Ti-Al-Ti-ITO stack. In an embodiment, the patterned conductive layer is 1 μm or less in thickness. The patterned conductive layer may be deposited using a suitable technique such as, but not limited to, PVD.

[0058] Following the formation of bottom electrodes 142, ground tie lines 144, and ground ring 116, an insulator layer 146 may then optionally be formed over the TFT substrate 102 covering the sidewalls of the pattered conductive layer. The insulator layer 146 may at least partially cover the bank layer 126 and the reflective layer forming the bottom electrodes 142, ground tie lines 144, and/or ground ring 116. In the embodiment illustrated the insulator layer 146 completely covers the ground ring 116, however, this is optional.

[0059] In an embodiment, the insulator layer 146 is formed by blanket deposition using a suitable technique such as lamination, spin coating, CVD, and PVD, and then patterned using a suitable technique such as lithography to form openings exposing the bottom electrodes 142 and openings 149 exposing the ground tie lines 149. In an embodiment, ink jet printing or screen printing may be used to form the insulator layer 146 and openings 149 without requiring lithography. Insulator layer 146 may be formed of a variety of materials such as, but not limited to, SiO_2, SiN_x, PMMA, BCB, polyimide, acrylate, epoxy, and polyester. For example, the insulator layer 146 may be 0.5 μm thick. The insulator layer 146 may be transparent or semi-transparent where formed over the reflective layer on sidewalls of bottom electrode 142 within the bank openings 128 as to not significantly degrade light emission extraction of the completed system. Thickness of the insulator layer 146 may also be controlled to increase light extraction efficiency, and also to not interfere with the array of transfer heads during transfer of the array of light emitting devices to the reflective bank structure. As will become more apparent in the following description, the patterned insulator layer 146 is optional, and represents one manner for electrically separating conductive layers.

[0060] In the embodiment illustrated in FIG. 3B, the bottom electrodes 142, ground tie lines 144, and ground ring 116 can be formed of the same conductive layer. In another embodiment, the ground tie lines 144 and/or ground ring 116 can be formed of a conductive material different from the bottom electrodes 142. For example, ground tie lines 14 and ground ring 116 may be formed with a material having a higher conductivity than the bottom electrodes 142. In another embodiment, ground tie lines 14 and/or ground ring 116 can also be formed within different layers

from the bottom electrodes. FIGS. 3C-3D illustrate embodiments where the ground tie lines 144 and ground ring 116 can be formed within or below the patterned bank layer 126. For example, in the embodiment illustrated in FIG. 3C, openings 149, 130 may be formed through the patterned bank layer 126 when forming the ground tie lines 144 and ground ring 116. In the embodiment illustrated in FIG. 3D openings 149 may be formed through the patterned bank layer 126 and planarization layer 122 to contact the ground tie lines 144. In the embodiment, illustrated openings are not formed to expose the ground ring, however, in other embodiments openings could be formed to expose the ground ring. In the embodiment illustrated in FIG. 3D, the ground ring and ground tie lines 144 may have been formed during formation of the working circuitry of the TFT substrate 102. In such an embodiment the conductive layer used to form the bottom electrode 142 may also optionally include via opening layers 145 to further enable electrical contact of the top electrode layer yet to be formed with the ground tie lines 144 through openings 149. Accordingly, it is to be appreciated that the embodiments illustrated in FIGS. 3A-3D are not limiting and that a number of possibilities exist for forming the ground tie lines 144 and ground ring 116, as well as openings 149, 130.

[0061] Still referring to embodiments illustrated in FIG. 3A-3D, a plurality of bonding layers 140 may be formed on the bottom electrode layer 142 to facilitate bonding of micro LED devices. In the specific embodiment illustrated two bonding layers 140 are illustrated for bonding two micro LED devices. In an embodiment, the bonding layer 140 is selected for its ability to be inter-diffused with a bonding layer on the micro LED device (yet to be placed) through bonding mechanisms such as eutectic alloy bonding, transient liquid phase bonding, or solid state diffusion bonding as described in U.S. Patent Application No. 13/749,647. In an embodiment, the bonding layer 140 has a melting temperature of 250 ^{o}C or lower. For example, the bonding layer 140 may include a solder material such as tin (232 ^{o}C) or indium (156.7 ^{o}C), or alloys thereof. Bonding layer 140 may also be in the shape of a post, having a height greater than width. In accordance with some embodiments of the invention, taller bonding layers 140 may provide an additional degree of freedom for system component leveling, such as planarity of the array of micro LED devices with the TFT substrate during the micro LED device transfer operation and for variations in height of the micro LED devices, due to the change in height of the liquefied bonding layers as they spread out over the surface during bonding, such as during eutectic alloy bonding and transient liquid phase bonding. The width of the bonding layers 140 may be less than a width of a bottom surface of the micro

IPR2024-01134 - BOE
Exhibit 1009 - Page 265

LEDs to prevent wicking of the bonding layers 140 around the sidewalls of the micro LEDs and shorting the quantum well structures.

[0062] In addition to bonding layers 140, the embodiments illustrated in FIGS. 3A-3D include a repair bonding site 401 within each bank opening 128 that is large enough to receive a micro LED device. In this manner, the plurality of bonding layers 140 and repair bonding site 401 create a redundancy and repair configuration within each bank opening 128. In the particular embodiments illustrated in FIGS. 3A-3D the repair bonding site 401 is illustrated as being a bare surface on the bottom electrode layer 142. However, embodiments of the invention are not limited to such. In other embodiments, the repair bonding site 401 may also include a bonding layer 140 similarly as the other two bonding layers 140 described and illustrated for the preexisting redundancy scheme. Accordingly, in some embodiments, bonding layers 140 are provided on the bottom electrode layer 142 at the sites of all of the intended micro LED devices in the redundancy scheme, as well as at the repair site 401.

[0063] In the embodiments illustrated an arrangement of ground tie lines 144 may run between bank openings 128 in the pixel area 104 of the display panel 100. In addition, a plurality of openings 149 expose the plurality of ground tie lines 144. The number of openings 149 may or may not have a 1:1 correlation to the number of columns (top to bottom) of bank openings 128. For example, in the embodiment illustrated in FIG. 3A, a ground tie opening 149 is formed for each column of bank openings 128, however, this is not required and the number of ground tie openings 149 may be more or less than the number of columns of bank openings 128. Likewise, the number of ground tie lines 144 may or may not have a 1:1 correlation to the number of rows (left to right) of bank openings. For example, in the embodiment illustrated a ground tie line 144 is formed for every two rows of bank openings 128, however, this is not required and the number of ground tie lines 144 may have a 1:1 correlation, or any 1:n correlation to the number (n) of rows of bank openings 128.

[0064] While the above embodiments have been described an illustrated with ground tie lines 144 running left and right horizontally across the display panel 100, embodiments are not so limited. In other embodiments, the ground tie lines can run vertically, or both horizontally and vertically to form a grid. A number of possible variations are envisioned in accordance with embodiments of the invention. It has been observed that operation of AMOLED configurations such as those previously illustrated and described with regard to FIGS. 1-2 may result in dimmer emission from the subpixels in the center of the pixel area, where the subpixels are furthest from the ground ring 116, compared

to the emission from subpixels at the edges of the pixel area closer to the ground ring 116. In accordance with embodiments of the invention, ground tie lines are formed between the bank openings 128 in the pixel area and are electrically connected to the ground ring 116 or ground line in the non-display area. In this manner, the ground signal may be more uniformly applied to the matrix of subpixels, resulting in more uniform brightness across the display panel 100. In addition, by forming the ground tie lines 144 from a material having better electrical conductivity than the top electrode layer (which is yet to be formed), this may reduce the contact resistance in the electrical ground path.

[0065] FIGS. 4A-4H are cross-sectional side view illustrations for a method of transferring an array of micro LED devices to the TFT substrate 102 in accordance with an embodiment of the invention. Referring to FIG. 4A, an array of transfer heads 302 supported by a transfer head substrate 300 are positioned over an array of micro LED devices 400 supported on a carrier substrate 200. A heater 306 and heat distribution plate 304 may optionally be attached to the transfer head substrate 300. A heater 204 and heat distribution plate 202 may optionally be attached to the carrier substrate 200. The array of micro LED devices 400 are contacted with the array of transfer heads 302, as illustrated in FIG. 4B, and picked up from the carrier substrate 200 as illustrated in FIG. 4C. In an embodiment, the array of micro LED devices 400 are picked up with an array of transfer heads 302 operating in accordance with electrostatic principles, that is, they are electrostatic transfer heads.

[0066] FIG. 4D is a cross-sectional side view illustration of a transfer head 302 holding a micro LED device 400 over a TFT substrate 102 in accordance with an embodiment of the invention. In the embodiment illustrated, the transfer head 302 is supported by a transfer head substrate 300. As described above, a heater 306 and heat distribution plate 304 may optionally be attached to the transfer head substrate to apply heat to the transfer head 302. A heater 152 and heat distribution plate 150 may also, or alternatively, optionally be used to transfer heat to the bonding layer 140 on the TFT substrate 102 and/or optional bonding layer 410 on a micro LED device 400 described below.

[0067] Still referring to FIG. 4D, a close-up view of an exemplary micro LED device 400 is illustrated in accordance with an embodiment. It is to be appreciated, that the specific micro LED device 400 illustrated is exemplary and that embodiments of the invention are not limited. In the particular embodiment illustrated, the micro LED device 400 includes a micro p-n diode 450 and a bottom conductive contact 420. A bonding layer 410 may optionally be formed below the bottom conductive contact 420, with the bottom conductive contact 420 between the micro p-n diode 450

IPR2024-01134 - BOE
Exhibit 1009 - Page 267

and the bonding layer 410. In an embodiment, the micro LED device 400 further includes a top conductive contact 452. In an embodiment, the micro p-n diode 450 includes a top n-doped layer 414, one or more quantum well layers 416, and a lower p-doped layer 418. In other embodiments, the arrangement of n-doped and p-doped layers can be reversed. The micro p-n diodes can be fabricated with straight sidewalls or tapered sidewalls. In certain embodiments, the micro p-n diodes 450 possess outwardly tapered sidewalls 453 (from top to bottom). In certain embodiments, the micro p-n diodes 450 possess inwardly tapered sidewall (from top to bottom). The top and bottom conductive contacts 420, 452. For example, the bottom conductive contact 420 may include an electrode layer and a barrier layer between the electrode layer and the optional bonding layer 410. The top and bottom conductive contacts 420, 452 may be transparent to the visible wavelength range (e.g. 380 nm – 750 nm) or opaque. The top and bottom conductive contacts 420, 452 may optionally include a reflective layer, such as a silver layer. The micro p-n diode and conductive contacts may each have a top surface, a bottom surface and sidewalls. In an embodiment, the bottom surface 451 of the micro p-n diode 450 is wider than the top surface of the micro p-n diode, and the sidewalls 453 are tapered outwardly from top to bottom. The top surface of the micro p-n diode 450 may be wider than the bottom surface of the p-n diode, or approximately the same width. In an embodiment, the bottom surface 451 of the micro p-n diode 450 is wider than the top surface of the bottom conductive contact 420. The bottom surface of the micro p-n diode may also be approximately the same width as the top surface of the bottom conductive contact 420. In an embodiment, the micro p-n diode 450 is several microns thick, such as 3 μm or 5 μm, the conductive contacts 420, 452 are 0.1 μm - 2 μm thick, and the optional bonding layer 410 is 0.1 μm – 1μm thick. In an embodiment, a maximum width of each micro LED device 400 is 1-100 μm, for example, 30 μm, 10 μm, or 5 μm. In an embodiment, the maximum width of each micro LED device 400 must comply with the available space in the bank opening 128 for a particular resolution and PPI of the display panel.

[0068] FIG. 4E is a cross-sectional side view illustration of an array of transfer heads holding an array micro LED devices 400 over a TFT substrate 102 accordance with an embodiment of the invention. FIG. 4E is substantially similar to the structure illustrated in FIG. 4D with the primary difference being the illustration of the transfer of an array of micro LED devices as opposed to a single micro LED device within the array of micro LED devices.

[0069] Referring now to FIG. 4F the TFT substrate 102 is contacted with the array of micro LED devices 400. In the embodiment illustrated, contacting the TFT substrate 102 with the array of

IPR2024-01134 - BOE
Exhibit 1009 - Page 268

micro LED devices 400 includes contacting bonding layer 140 with a micro LED device bonding layer 410 for each respective micro LED device. In an embodiment, each micro LED device bonding layer 410 is wider than a corresponding bonding layer 140. In an embodiment energy is transferred from the electrostatic transfer head assembly and through the array of micro LED devices 400 to bond the array of micro LED devices 400 to the TFT substrate 102. For example, thermal energy may be transferred to facilitate several types of bonding mechanisms such as eutectic alloy bonding, transient liquid phase bonding, and solid state diffusion bonding. The transfer of thermal energy may also be accompanied by the application of pressure from the electrostatic transfer head assembly.

[0070] Referring to FIG. 4G, in an embodiment, the transfer of energy liquefies bonding layer 140. The liquefied bonding layer 140 may act as a cushion and partially compensate for system uneven leveling (e.g. nonplanar surfaces) between the array of micro devices 400 and the TFT substrate during bonding, and for variations in height of the micro LED devices. In the particular implementation of transient liquid phase bonding the liquefied bonding layer 140 inter-diffuses with the micro LED device bonding layer 410 to form an inter-metallic compound layer with an ambient melting temperature higher than the ambient melting temperature of the bonding layer 140. Accordingly, transient liquid phase bonding may be accomplished at or above the lowest liquidus temperature of the bonding layers. In some embodiments of the invention, the micro LED device bonding layer 410 is formed of a material having a melting temperature above 250 ^{o}C such as bismuth (271.4 ^{o}C), or a melting temperature above 350 ^{o}C such as gold (1064 ^{o}C), copper (1084 ^{o}C), silver (962 ^{o}C), aluminum (660 ^{o}C), zinc (419.5 ^{o}C), or nickel (1453 ^{o}C), and the TFT substrate bonding layer 140 has a melting temperature below 250 ^{o}C such as tin (232 ^{o}C) or indium (156.7 ^{o}C).

[0071] In this manner, the substrate 150 supporting the TFT substrate 102 can be heated to a temperature below the melting temperature of the bonding layer 140, and the substrate 304 supporting the array of transfer heads is heated to a temperature below the melting temperature of bonding layer 410, but above the melting temperature of bonding layer 140. In such an embodiment, the transfer of heat from the electrostatic transfer head assembly through the array of micro LED devices 400 is sufficient to form the transient liquid state of bonding layer 140 with subsequent isothermal solidification as an inter-metallic compound. While in the liquid phase, the lower melting temperature material both spreads out over the surface and diffused into a solid solution of the higher melting temperature material or dissolves the higher melting temperature

IPR2024-01134 - BOE
Exhibit 1009 - Page 269

material and solidifies as an inter-metallic compound. In a specific embodiment, the substrate 304 supporting the array of transfer heads is held at 180 °C, bonding layer 410 is formed of gold, and bonding layer 140 is formed of indium.

[0072] Following the transfer of energy to bond the array of micro LED devices 400 to the TFT substrate, the array of micro LED devices 400 are released onto the receiving substrate and the array of electrostatic transfer heads are moved away as illustrated in FIG. 4H. Releasing the array of micro LED devices 400 may be accomplished with a variety of methods including turning off the electrostatic voltage sources, lowering the voltage across the electrostatic transfer head electrodes, changing a waveform of an AC voltage, and grounding the voltage sources.

[0073] Referring now to FIGS. 5A-5F, a sequence of transferring an array of micro LED devices 400 with different color emissions is illustrated in accordance with an embodiment of the invention. In the particular configuration illustrated in FIG. 5A, a first transfer procedure has been completed for transferring an array of red-emitting micro LED devices 400R from a first carrier substrate to the TFT substrate 102. For example, where the micro LED devices 400R are designed to emit a red light (e.g.620-750 nm wavelength) the micro p-n diode 450 may include a material such as aluminum gallium arsenide (AlGaAs), gallium arsenide phosphide (GaAsP), aluminum gallium indium phosphide (AlGaInP), and gallium phosphide (GaP). Referring to FIG. 5B, a second transfer procedure has been completed for transferring a redundant array of red-emitting micro LED devices 400R. For example, the redundant array could be transferred from a different carrier substrate, or from a different area (e.g. from opposite side, different areas do not overlap, or random selection) of the first carrier substrate in order to decrease the probability of transferring a second array from a same correlated defect area or contaminated area (e.g. particulates) of the first carrier substrate. In this manner, by transferring from two uncorrelated areas it may be possible to reduce the likelihood of transferring two defective micro LED devices 400 to the same bank structure 128, or alternatively transferring no micro LED devices 400 to a single bank structure 128 because it was not possible to pick up the micro LED devices in a defective or contaminated area of a carrier substrate. In yet another embodiment, by using a redundant array from two different wafers it may be possible to obtain a mix of both colors, and tune the average power consumption of the display based upon a pre-existing knowledge of the primary emission wavelength of the micro LED devices on different wafers. For example, where the first wafer is known to have an average red emission of 630 nm with a first power consumption while a second wafer is known to have an average red emission of 610 emission with a second power consumption, the redundancy array can be composed

IPR2024-01134 - BOE
Exhibit 1009 - Page 270

of micro LED devices from both wafers to obtain an average power consumption or alternate color gamut.

[0074] Referring to FIG. 5C, a third transfer procedure has been completed for transferring an array of green-emitting micro LED devices 400G from a second carrier substrate to the TFT substrate 102. For example, where the micro LED devices 400G are designed to emit a green light (e.g.495-570 nm wavelength) the micro p-n diode 450 may include a material such as indium gallium nitride (InGaN), gallium nitride (GaN), gallium phosphide (GaP), aluminum gallium indium phosphide (AlGaInP), and aluminum gallium phosphide (AlGaP). A fourth transfer procedure for transferring a redundant array of green-emitting micro LED devices 400G is illustrated in FIG. 5D, similarly as before.

[0075] Referring to FIG. 5E, a fifth transfer procedure has been completed for transferring an array of blue-emitting micro LED devices 400B from a third carrier substrate to the TFT substrate 102. For example, where the micro LED devices 400B are designed to emit a blue light (e.g.450-495 nm wavelength) the micro p-n diode 450 may include a material such as gallium nitride (GaN), indium gallium nitride (InGaN), and zinc selenide (ZnSe). A sixth transfer procedure for transferring a redundant array of blue-emitting micro LED devices 400B is illustrated in FIG. 5F, similarly as before.

[0076] In the particular embodiments described above with regard to FIGS. 5A-5F, the first and second micro LED devices 400 for each subpixel are separately transferred. For example, this may reduce the probability of correlated defects. However, in other embodiments it is possible to simultaneously transfer the first and second micro LED devices from the same carrier substrate. In this manner, simultaneous transfer may increase production throughput while still offering some of the benefits of a redundancy scheme at the expense of the possibility of correlated defects due to transferring micro LED devices from the same area of a carrier substrate. In such an embodiment the processing sequence would resemble the sequence in the following order of FIG. 5B, 5D, 5F.

[0077] In accordance with embodiments of the invention, the transfer heads are separated by a pitch (x, y, and/or diagonal) that matches a pitch of the bank openings on the backplane corresponding to the pixel or subpixel array. Table 1 provides a list of exemplary implementations in accordance with embodiments of the invention for various red-green-blue (RGB) displays with 1920 x 1080p and 2560x1600 resolutions. It is to be appreciated that embodiments of the invention are not limited to RGB color schemes or the 1920 x 1080p or 2560x1600 resolutions, and that the specific resolution and RGB color scheme is for illustrational purposes only.

IPR2024-01134 - BOE
Exhibit 1009 - Page 271

Table 1.

Display Substrate	Pixel Pitch (x, y)	Sub-Pixel pitch (x,y)	Pixels per inch (PPI)	Possible transfer head array pitch
55" 1920x1080	(634 μm, 634 μm)	(211 μm, 634 μm)	40	X: Multiples or fractions of 211 μm Y: Multiples or fractions of 634 μm
10" 2560x1600	(85 μm, 85 μm)	(28 μm, 85 μm)	299	X: Multiples or fractions of 28 μm Y: Multiples or fractions of 85 μm
4" 640x1136	(78 μm, 78 μm)	(26 μm, 78 μm)	326	X: Multiples or fractions of 26 μm Y: Multiples or fractions of 78 μm
5" 1920x1080	(58 μm, 58 μm)	(19 μm, 58 μm)	440	X: Multiples or fractions of 19 μm Y: Multiples or fractions of 58 μm

[0078] In the above exemplary embodiments, the 40 PPI pixel density may correspond to a 55 inch 1920 x 1080p resolution television, and the 326 and 440 PPI pixel density may correspond to a handheld device with RETINA (RTM) display. In accordance with embodiments of the invention, thousands, millions, or even hundreds of millions of transfer heads can be included in a micro pick up array of a mass transfer tool depending upon the size of the micro pick up array. In accordance with embodiments of the invention, a 1 cm x 1.12 cm array of transfer heads can include 837 transfer heads with a 211 μm, 634 μm pitch, and 102,000 transfer heads with a 19 μm, 58 μm pitch.

[0079] The number of micro LED devices picked up with the array of transfer heads may or may not match the pitch of transfer heads. For example, an array of transfer heads separated by a pitch of 19 μm picks up an array of micro LED devices with a pitch of 19 μm. In another example, an array of transfer heads separated by a pitch of 19 μm picks up an array of micro LED devices with a pitch of approximately 6.33 μm. In this manner the transfer heads pick up every third micro LED device for transfer to the backplane. In accordance with some embodiments, the top surface of the array of light emitting micro devices is higher than the top surface of the insulating layer so as to prevent the transfer heads from being damaged by or damaging the insulating layer (or any intervening layer) on the blackplane during placement of the micro LED devices within bank openings.

IPR2024-01134 - BOE
Exhibit 1009 - Page 272

[0080] FIG. 6A is a top view illustration of an active matrix display panel in accordance with an embodiment after the formation of a top electrode layer. FIG. 6B is a top view illustration of an active matrix display panel in accordance with an embodiment after the formation of separate top electrode layers. FIGS. 6C-6D are side-view illustrations of the active matrix display panel of either FIG. 6Aor FIG. 6B taken along lines X-X and Y-Y in accordance with embodiments of the invention. In accordance with the embodiments illustrated in FIGS. 6A-6B, one or more top electrode layers 118 are formed over the pixel area 104 including the array of micro LED devices 400, as well as formed within the openings 149 and in electrical contact with the ground tie lines 144 running between the bank openings 128 in the pixel area 104.

[0081] Referring now to FIGS. 6C-6D, prior to forming the one or more top electrode layers 118 the micro LED devices 400 are passivated within the bank openings 128 in order to prevent electrical shorting between the top and bottom electrode layers 118, 142, or shorting at the one or more quantum wells 416. As illustrated, after the transfer of the array micro LED devices 400, a passivation layer 148 may be formed around the sidewalls of the micro LED devices 400 within the array of bank openings 128. In an embodiment, where the micro LED devices 400 are vertical LED devices, the passivation layer 148 covers and spans the quantum well structure 416. The passivation layer 148 may also cover any portions of the bottom electrode layer 142 not already covered by the optional insulator layer 146 in order to prevent possible shorting. Accordingly, the passivation layer 148 may be used to passivate the quantum well structure 416, as well as the bottom electrode layer 142. In accordance with embodiments of the invention, the passivation layer 148 is not formed on the top surface of the micro LED devices 400, such as top conductive contact 452. In one embodiment, a plasma etching process, e.g. O_2 or CF_4 plasma etch, can be used after forming the passivation layer 148 to etch back the passivation layer 148, ensuring the top surface of the micro LED devices 400, such as top conductive contacts 452, are exposed to enable the top conductive electrode 118 layers 118 to make electrical contact with the micro LED devices 400.

[0082] In accordance with embodiments of the invention, the passivation layer 148 may be transparent or semi-transparent to the visible wavelength so as to not significantly degrade light extraction efficiency of the completed system. Passivation layer may be formed of a variety of materials such as, but not limited to epoxy, acrylic (polyacrylate) such as poly(methyl methacrylate) (PMMA), benzocyclobutene (BCB), polyimide, and polyester. In an embodiment, passivation layer 148 is formed by ink jet printing or screen printing around the micro LED devices 400.

IPR2024-01134 - BOE
Exhibit 1009 - Page 273

[0083] In the particular embodiment illustrated in FIG. 6C, the passivation layer 148 is only formed within the bank openings 128. However, this is not required, and the passivation layer 148 may be formed on top of the bank structure layer 126. Furthermore, the formation of insulator layer 146 is not required, and passivation layer 148 can also be used to electrically insulate the conductive layers. As shown in the embodiment illustrated in FIG. 6D, the passivation layer 148 may also be used to passivate sidewalls of the conductive layer forming the bottom electrode 142 and ground tie lines 144. In an embodiment, passivation layer 148 may optionally be used to passivate ground ring 116. In accordance with some embodiments, the formation of openings 149 can be formed during the process of ink jet printing or screen printing the passivation layer 148 over the ground tie lines 144. Openings may also optionally be formed over the ground ring 116. In this manner, a separate patterning operation may not be required to form the openings.

[0084] In accordance with some embodiments of the invention a canal 151, or well structure, can be formed within the bank layer 126 as illustrated in FIG. 6C in order to capture or prevent the passivation layer 148 from spreading excessively and overflowing over the ground tie lines 149, particularly when the passivation layer 148 is formed using a solvent system such as with ink jet printing or screen printing. Accordingly, in some embodiments, a canal 151 is formed within the bank layer 126 between the bank opening 128 and an adjacent ground tie line 144.

[0085] Still referring to FIGS. 6C-6D, after formation of passivation layer 148 one or more top conductive electrode layers 118 are formed over each micro LED device 400 and in electrical contact with the top contact layer 452, if present. Depending upon the particular application in the following description, top electrode layers 118 may be opaque, reflective, transparent, or semi-transparent to the visible wavelength. For example, in top emission systems the top electrode layer 118 may be transparent, and for bottom emission systems the top electrode layer may be reflective. Exemplary transparent conductive materials include amorphous silicon, transparent conductive oxides (TCO) such as indium-tin-oxide (ITO) and indium-zinc-oxide (IZO), carbon nanotube film, or a transparent conductive polymer such as poly(3,4-ethylenedioxythiophene) (PEDOT), polyaniline, polyacetylene, polypyrrole, and polythiophene. In an embodiment, the top electrode layer 118 includes nanoparticles such as silver, gold, aluminum, molybdenum, titanium, tungsten, ITO, and IZO. In a particular embodiment, the top electrode layer 118 is formed by ink jet printing or screen printing ITO or a transparent conductive polymer such as PEDOT. Other methods of formation may include chemical vapor deposition (CVD), physical vapor deposition (PVD), spin coating. The top electrode layer 118 may also be reflective to the visible wavelength. In an

IPR2024-01134 - BOE
Exhibit 1009 - Page 274

embodiment, a top conductive electrode layer 118 comprises a reflective metallic film such as aluminum, molybdenum, titanium, titanium-tungsten, silver, or gold, or alloys thereof, for example for use in a bottom emission system.

[0086] In accordance with some embodiments of the invention the ground tie lines 144 may be more electrically conductive than the top electrode layer 118. In the embodiment illustrated in FIG. 3D, the ground tie lines 144 can be formed from the same metal layer used to formed the source/drain connections or gate electrode to one of the transistors (e.g. T2) in the TFT substrate 102. For example, the ground tie lines 144 can be formed from a common interconnect material such as copper or aluminum, including their alloys. In the embodiments illustrated in FIGS. 3B-3C and FIGS. 6C-6D, the ground tie lines 144 may also be formed from the same material as the bottom electrode layers 142. For example, the ground tie lines 144 and bottom electrode layers 142 include a reflective material, which may also improve the electrical conductivity of the layers. In a specific example, the ground tie lines 144 and bottom electrodes may include a metallic film or metal particles. In accordance with some embodiments, the top electrode layer 118 is formed of a transparent or semi-transparent material such as amorphous silicon, transparent conductive oxides (TCO) such as indium-tin-oxide (ITO) and indium-zinc-oxide (IZO), carbon nanotube film, or a transparent conductive polymer such as poly(3,4-ethylenedioxythiophene) (PEDOT), polyaniline, polyacetylene, polypyrrole, and polythiophene, all of which may have a lower electrical conductivity than a conductive and reflective bottom electrode layer including a metallic film within a film stack.

[0087] Referring back to FIG. 6A again, in the particular embodiment illustrated a top electrode layer 118 is formed over the pixel area 104 including the array of micro LED devices 400. The top electrode layer 118 may also be formed within the openings 149, if present, and in electrical contact with the ground tie lines 149 running between the bank openings 128 in the pixel area 104. In such an embodiment, since the ground tie lines 144 are in electrical connection with the ground ring 116, it is not necessary to form the top electrode layer 118 outside of the pixel area 104. As illustrated, the ground ring 116 may be buried beneath an electrically insulating layer such as such as insulator layer 146, passivation layer 148, or even bank structure layer 126 or planarization layer 122. While FIG. 6A is described and illustrates as including the top electrode layer 118 only over the pixel area 104, and including ground tie lines 144 embodiments of the invention are not so limited. For example, ground tie lines 144 are not necessary to establish a redundancy scheme and repair site, nor is it required that the top electrode layer not be formed over and in electrical contact with the ground ring 116, or ground line.

[0088] FIG. 6B illustrates an alternative embodiment in which separate top electrode layers 118 are formed connecting one or more micro LED devices 400 with one or more ground tie lines 144. In the particular embodiment illustrated in FIG. 6B, the top electrode layers 118 only need to provide the electrical path from a micro LED device 400 to a nearby ground tie line 144. Accordingly, it is not required for the top electrode layers 118 to cover the entire pixel area 104, or even the entire bank openings 128 for that matter. In the particular embodiment illustrated, each top electrode layer 118 connects the micro LED devices 400 within a pair of bank openings on opposite sides of an intermediate ground tie line 144. However, this particular configuration is exemplary and a number of different arrangements are possible. For example, a single top electrode layer 118 may run over, and electrically connect an n-number of rows of micro LED devices, or bank openings 128, to the ground tie lines or ground ring. As illustrated, the top electrode layer 118 may be formed within openings 149 to the ground tie lines 144. In such an embodiment, since the ground tie lines 144 are in electrical connection with the ground ring 116, it is not necessary to form the top electrode layer 118 outside of the pixel area 104.

[0089] As illustrated, the ground ring 116 may be buried beneath an electrically insulating layer such as such as insulator layer 146 in accordance with the embodiments illustrated in FIGS. 6A-6B. In the particular embodiments illustrated in FIG. 6B, topmost row of micro LED devices 400 are illustrated as being connected to the ground ring 116 with individual top electrode layers 118. In such an embodiment, each top electrode layer 118 may contact the ground ring 116 through one or more openings as previously described. Accordingly, while the embodiments illustrated in FIGS. 6A-6B provide one manner for connecting the micro LED devices 400 to ground tie lines 144 within the pixel area 104, this does not preclude using separate top electrode layers 118 to connect to the ground ring 116 without going through a ground tie line 144.

[0090] As illustrated in FIGS. 6A-6B, line width for the top electrode layers 118 can vary depending upon application. For example, the line width may approach that of the pixel area 104. Alternatively, the line width may be minimal. For example, line widths as low as approximately 15 μm may be accomplished with commercially available ink jet printers, and line widths as low as approximately 30 μm may be accomplished with commercially available screen printers. Accordingly, the line width of the top electrode layers 118 may be more or less than the maximum width of the micro LED devices.

[0091] In another aspect, the embodiments of the invention may be particularly suitable for localized formation of the top electrode layers 118 with ink jet printing or screen printing. Ink jet

IPR2024-01134 - BOE
Exhibit 1009 - Page 276

printing in particular may be suitable since it is a non-contact printing method. Conventional AMOLED backplane processing sequences such as those used for the fabrication of the display panels in FIGS. 1-2 typically blanket deposit the top electrode layer in deposition a chamber, followed by singulation of the individual backplanes 100 from a larger substrate. In accordance with some embodiments, the display panel 100 backplane is singulated from a larger substrate prior to transferring the array of micro LED devices 400. In an embodiment, ink jet printing or screen printing provides a practical approach for patterning the individual top electrode layers 118 without requiring a separate mask layer for each separate display panel 100.

[0092] FIG. 7 is a top view schematic illustration of a smart pixel display including a redundancy and repair site configuration in accordance with an embodiment of the invention. As shown the display panel 200 includes a substrate 201 which may be opaque, transparent, rigid, or flexible. A smart pixel area 206 may include separate subpixels of different emission colors, and a micro controller chip 208 including the working circuitry described above with regard to the TFT substrate. In this manner, rather than forming the pixel area on a TFT substrate including the working circuitry, the micro LED devices 400 and micro controller chip 208 are both transferred to the same side or surface of the substrate 201. Electrical distribution lines can connect the micro controller chip 208 to the data driver circuit 110 and scan driver circuit 112 similarly as with a TFT substrate. Likewise, bank layer structures can be formed on the substrate 201 similarly as described above for the TFT substrate to contain the micro LED devices 400 and repair bonding site 401. Similarly, a top electrode layer 118, or separate top electrode layers 118 can connect the micro LED devices 400 to a ground tie line 144 or ground ring 116 similarly as described above with regard to the TFT substrate configuration. Thus, similar redundancy and repair site configurations can be formed with the smart pixel configuration as described above for the TFT substrate configurations.

[0093] Up until this point the redundancy and repair site configurations have been described without regard to whether any testing has been performed to detect defective, missing, or contaminated micro LED devices, or whether any repair options have been performed. Thus, up until this point embodiments of the invention have been described and illustrated assuming 100% transfer success of the micro LED devices to the display substrate, with no repair required. However, in practical application, it is not expected to always achieve 100% transfer success, and with no defective, missing, or contaminated micro LED devices. In accordance with embodiments of the invention, micro LED devices may be of 1 to 100 μm in scale, for example, having a maximum width of approximately 20 μm, 10 μm, or 5μm. Such micro LED devices are fabricated

IPR2024-01134 - BOE
Exhibit 1009 - Page 277

so that they are poised for pick up from a carrier substrate and transfer to the display substrate, for example, using an array of electrostatic transfer heads. Defective micro LED devices may result from a variety of reasons, such as contamination, stress fractures, and shorting between conductive layers. Micro LED devices also may not be picked up during the transfer operation due to a variety of reasons, such as non-planarity of the carrier substrate, contamination (e.g. particulates), or irregular adhesion of the micro LED devices to the carrier substrate.

[0094] FIGS. 8A-8B illustrate an integrated testing method in accordance with embodiments of the invention for detecting defective, missing, or contaminated micro LED devices after transfer of the micro LED devices from the carrier substrate to display substrate, such as the transfer operations illustrated in FIGS. 5A-5F, and prior to formation of the passivation layer 148 and top electrode layers 118. In this manner, detection of defective, missing, or contaminated micro LED devices can be used to potentially alter the deposition patterns of the passivation layer 148 and top electrode layers 118, and to potentially transfer replacement micro LED devices where required. Referring now to FIG. 8A, a carriage 802 supporting a light source 804 and camera 806 are scanned over the display substrate carrying the array of micro LED devices 400 which have been transferred and bonded to the bottom electrode layer 142.

[0095] In an embodiment, camera 806 is a line scan camera. For example, line scan cameras typically have a row of pixel sensors that can be used to provide a continuous feed to a computer system that joins the frames to make an image as the line scan camera is passed over an imaging surface. In an embodiment, camera 806 is a two dimensional (2D) camera having both x-y dimensions of pixels. In accordance with embodiments of the invention, camera 806 should have a resolution capable of imaging the micro LED devices 400, for example, having a maximum width of 1-100 μm. Resolution may be determined by the pixel size in the pixel sensors, and may be aided by the use of optics to increase the resolution. By way of example, in one embodiment, the micro LED devices 400 have a maximum width of approximately 5 μm. One exemplary line scan camera 806 which may be used is the BASLER RUNNER SERIES CAMERA (available from Basler AG of Ahrensburg, Germany) having a pixel size of 3.5 μm. With the addition of optics, this can allow for resolution down to approximately 1.75 μm for a 3.5 μm pixel size. Line scan cameras can also be selected for their line scan speed, and line scan width. For example, line scan speeds are achievable up to several meters per second, and line scan widths of are commonly available between 10 and 50 mm.

IPR2024-01134 - BOE
Exhibit 1009 - Page 278

[0096] In one embodiment, the light source 804 is used for illuminating the surface to be scanned. For example, in one embodiment, the camera 806 is scanned over the substrate 201, 102 surface in order to verify whether or a micro LED device 400 has been placed in an intended location. In this manner, the camera 806 can be used to detect successful transfer for each micro LED device 400 from a carrier substrate to the display substrate 201, 102.

[0097] In another embodiment, light source 804 is used to emit an excitation wavelength of light to induce photoluminescence of the micro LED devices 400. The light source 804 may be a variety of light sources such as, but not limited to, LED lighting or excimer laser. In this manner, the line scan camera 808 can be used to detect specific emission wavelengths from the micro LED devices 400 that exhibit either no emission, or irregular emission. Accordingly, this information can be used to detect defects in the micro LED devices 400 that are otherwise not easily curable on the carrier substrate. As described above, the carrier substrate may include thousands, or millions of micro LED devices 400 that are poised for pick up and transfer. A variety of defects can arise during processing and integration of the micro LED devices 400 on the carrier substrate. These defects could potentially cause shorting or non-uniform emission once transferred to the display substrate 201, 102. However, it may not be optimal to cure individual defective micro LED devices 400 when they are on the carrier substrate. If a micro LED device 400 is defective on the carrier substrate, it may simply be more efficient to cure the defect with a redundancy scheme or repair site on the display substrate 201, 102 in accordance with embodiments of the invention.

[0098] In an embodiment, light source 804 emits a shorter wavelength of light than the wavelength of light that the target micro LED devices are designed to emit, to induce red shifting or fluorescence of light from the micro LED devices. In accordance with embodiments of the invention, the light source 804 may be tunable, or multiple light sources set to a desired wavelength are provided. For example, an excitation wavelength of 500-600 nm may be used to induce emission of red light (e.g.620-750 nm wavelength) from the red-emitting micro LED devices 400R, an excitation wavelength of 430- 470 nm may be used to induce emission of green light (e.g.495-570 nm wavelength) from a the green-emitting micro LED devices 400G, and an excitation wavelength of 325-425 nm may be used to induce emission of blue light (e.g.450-495 nm wavelength) from the blue-emitting micro LED devices 400B. However, these ranges are exemplary and not exclusive. In some instances it may be useful to provide a color filter 808 over the line scan camera 806 so that only a select range of wavelengths are detected. This can reduce dilution resulting from light emission from micro LED devices of different colors.

IPR2024-01134 - BOE
Exhibit 1009 - Page 279

[0099] Referring now to FIG. 8B, an embodiment is illustrated for scanning a substrate 201, 102 after bonding of the array of micro LED devices. In such an embodiment, the exemplary substrate is approximately 100 mm wide, and a line scan camera with line scan width of approximately 20 mm is provided. As illustrated, the substrate 201, 102 can be scanned using a total of 3 passes to cover the entire surface of the substrate 201, 102. In one embodiment, the line scan camera 806 is a multi-color camera and is capable of simultaneously imaging all of the red, green, and blue micro LED devices 400 assuming the light source(s) 204 provide the required excitation wavelengths to excite all of the micro LED devices. In another embodiment, only a single excitation wavelength or range is provided to target a specific micro LED device emission color. In such an embodiment, it may be required to scan the substrate 201, 102 three separate times, at the three separate excitation wavelengths to image all of the micro LED devices 400. However, at line scan speeds of up to several meters per second, the practical difference in time required for multiple scans may be inconsequential.

[00100] In an embodiment, substrate 201, 102 is scanned using a stepped image capture method. For example, the camera is moved a known distance between subpixels, or moved a known distance between the known bonding sites of the micro LED devices between image capture. In such an embodiment, the camera can be a line scan camera. In an embodiment, the camera can be a camera including an x-y array of pixels to capture mosaics or selected tiles. Stepped image capture operation of the camera allows for testing flexibility for specific regions of the substrate surface, and may be particularly suitable for comparing measured spaced apart micro LED devices to nominal patterns. Accordingly, the camera can be moved in a pattern to capture specific locations rather than scanning in a line.

[00101] A number of possible processing variations can follow based upon the results of the integrated detection test described with regard to FIGS. 8A-8B. Specifically, in some embodiments, the patterning of passivation layer 148 and top electrode layer 118 can be tailored to the specific results, particularly when deposited by ink jet printing.

[00102] FIG. 9 is a cross-sectional side view illustration of an exemplary structure that can be formed after detection of a defective or contaminated micro LED device 400X, in accordance with an embodiment of the invention. In the embodiment illustrated, micro LED device 400 was found functional (e.g. proper emission) in a detection test, and micro LED device 400X was found defective. Alternatively, or in addition, a detection test indicated that micro LED device 400X was contaminated (e.g. particle on top surface could prevent obtaining contact with top electrode layer).

IPR2024-01134 - BOE
Exhibit 1009 - Page 280

Since the defect detection test does not necessarily determine what the defect is, in the embodiment illustrated, the passivation layer 148 may simply be formed over the micro LED device 400X to fully passivate the micro LED device 400X so that it is not possible for the top electrode layer 118 to make electrical contact with the defective or contaminated micro LED device 400X.

[00103] FIG. 10 is a cross-sectional side view illustration of an exemplary structure that can be formed after detection of a missing micro LED device, in accordance with an embodiment of the invention. In the embodiment illustrated, the detection test indicated that a micro LED device was not transferred. As a result, passivation layer 118 is formed over the bonding layer 140 to that it is not possible for the top electrode layer 118 to make electrical contact with the bottom electrode 142.

[00104] FIG. 11 is a cross-sectional side view illustration of an exemplary structure that can be formed after detection of a defective or contaminated micro LED device 400X, in accordance with an embodiment of the invention. As illustrated, prior to forming the passivation layer 148, a replacement micro LED device 400 can be bonded to the previously open repair bonding site 401 on the bottom electrode 142. As previously described, the repair bonding site 401 may be a bare surface on the bottom electrode layer 142, or alternatively may include a bonding layer 140. Following placement of the replacement micro LED device 400, the passivation layer 148 may be formed to passivate the quantum well structures of the micro LED devices 400, bottom electrode 142, and optionally the exposed surfaces of the defective or contaminated micro LED device 400X as described above with regard to FIG. 9. Top electrode 118 may then be formed to make electrical contact with the micro LED device 400 and replacement micro LED device 400.

[00105] FIG. 12 is a cross-sectional side view illustration of an exemplary structure that can be formed after detection of a missing micro LED device, in accordance with an embodiment of the invention. As illustrated, prior to forming the passivation layer 148, a replacement micro LED device 400 can be bonded to the previously open repair bonding site 401 on the bottom electrode 142. Following placement of the replacement micro LED device 400, the passivation layer 148 may be formed over the bonding layer 140 to that it is not possible for the top electrode layer 118 to make electrical contact with the bottom electrode 142. Top electrode 118 may then be formed to make electrical contact with the micro LED device 400 and replacement micro LED device 400.

[00106] FIG. 13 is a top schematic view illustration of an array of micro LED devices including a variety of configurations described in FIGS. 9-12 in accordance with embodiments of the invention. In the particular embodiments illustrated in FIG. 13, a top electrode layer 118 is formed over a plurality of bank openings 128, and may be formed over a plurality of subpixels or

IPR2024-01134 - BOE
Exhibit 1009 - Page 281

pixels 106. In an embodiment, the top electrode layer 118 is formed over all of the micro LED devices 400 in the pixel area.

[00107] The embodiment illustrated in FIG. 9 is also illustrated as one of the blue-emitting subpixels in FIG. 13 where the top electrode layer 118 is formed over both the blue emitting micro LED device 400, and the defective or contaminated micro LED device 400X, where the defective or contaminated micro LED device 400X is covered with the passivation layer 148.

[00108] The embodiment illustrated in FIG. 10 is also illustrated as one of the red-emitting subpixels in FIG. 13 where the top electrode layer 118 is formed over both the red-emitting micro LED device 400, and the bonding layer 140, where the bonding layer 140 is covered with the passivation layer 148.

[00109] The embodiment illustrated in FIG. 11 is also illustrated as one of the red-emitting subpixels in FIG. 13 in which a replacement red-emitting micro LED device 400 is bonded to the previously open repair bonding site 401. As previously described, the open repair bonding site 401 may have been a bare surface on the bottom electrode layer 142, or alternatively may have included a bonding layer 140. Similar to FIG. 9, the top electrode layer 118 is formed over both the red-emitting micro LED devices 400, and the defective or contaminated micro LED device 400X, where the defective or contaminated micro LED device 400X is covered with the passivation layer 148.

[00110] The embodiment illustrated in FIG. 12 is also illustrated as one of the blue-emitting subpixels in FIG. 13 in which a replacement blue-emitting micro LED device 400 is bonded to the previously open repair bonding site 401. Similar to FIG. 10, the top electrode layer 118 is formed over both the blue-emitting micro LED devices 400, and the bonding layer 140, where the bonding layer 140 is covered with the passivation layer 148.

[00111] FIG. 14 is a top schematic view illustration of an array of micro LED devices including a variety of configurations described in FIGS. 9-12 in accordance with embodiments of the invention. In the particular embodiments illustrated in FIG. 13, the arrangements of micro LED devices 400 are the same as those described above with regard to FIG. 13. The embodiments illustrated in FIG. 14 differ from those illustrated in FIG. 13 particularly in formation of a plurality of separate top electrode layers 118. In one embodiment, such as those illustrated in the labeled pixel 106 where a micro LED device 400 is not placed on the repair bonding site 401, it is not required for the top electrode layers 118 to be formed thereon. Accordingly, the length of the top electrode layer 118 can be determined based upon whether or not a replacement micro LED device is added. In addition, the blue-emitting subpixel in the labeled pixel 106 shows a defective or

IPR2024-01134 - BOE
Exhibit 1009 - Page 282

contaminated micro LED device 400X on the bonding site further away from the ground tie line. In such an embodiment, the top electrode layer 118 may be formed over only the blue-emitting micro LED device 400, or over both the blue-emitting micro LED device 400 and the defective or contaminated micro LED device 400X. The top electrode layer 118 may also be formed over the bonding site 401.

[00112] FIG. 15 is a top schematic view illustration of an array of micro LED devices including a variety of configurations described in FIGS. 9-12 in accordance with embodiments of the invention. In the particular embodiments illustrated in FIG. 15, the arrangements of micro LED devices 400 are the same as those described above with regard to FIGS. 13-14. The embodiments illustrated in FIG. 15 differ from those illustrated in FIG. 14 particularly in formation of the plurality of separate top electrode layers 118. The embodiments illustrated in FIG. 14 were shown as altering the length of the top electrode layers 118, while the embodiments illustrated in FIG. 15 are shown as altering the path of the top electrode layers 118, and/or number of top electrode layers 118. For example, in many of the embodiments illustrated in FIG. 15, a separate top electrode layer 118 can be formed for every micro LED device 400. In the embodiment illustrated in the bottom-most blue-emitting subpixel, a single top electrode layer 118 can be formed for multiple micro LED devices 400 where the path is adjusted to avoid a bonding layer 140, or alternatively a defective or contaminated micro LED device. In this manner, adjusting the path of the top electrode layers 118 can be used in the alternative to, or in addition to, adjusting deposition of the passivation layer 148 to cover defective or contaminated micro LED devices or the bonding sites of missing micro LED devices.

[00113] The formation of separate top electrode layer(s) 118 may provide an additional benefit during electrical testing of the panel 100 after formation of the top electrode layer(s) 118. For example, prior to formation of the top electrode layer 118 it may not have been possible to detect certain defects resulting in shorting of a micro LED device 400S. The implication of a shorted micro LED device 400S could result in a dark subpixel in which all of the current flows through the shorted micro LED devices 400S rather than any of the other micro LED devices in the subpixel. In the embodiment illustrated in FIG. 16 the top electrode layer 118 connected to a shorted micro LED device 400S is cut using a suitable technique such as laser scribing. In this manner, electrical shorts that could not have been or were not detected during the integrated testing method previously described could potentially be detected during an electrical test with the application of electrical current through the display after formation of the top electrode layer 118.

IPR2024-01134 - BOE
Exhibit 1009 - Page 283

In such an embodiment, if a micro LED device 400S is shorted, the top electrode layer 118 to the micro LED device 400S can be cut, allowing the redundant and/or repair micro LED device to provide the emission from the subpixel.

[00114] FIG. 17 illustrates an alternative embodiment where rather that cutting or scribing the top electrode layer 118, the bottom electrode layer 124 can be cut using a suitable technique such as laser scribing to segregate irregular micro LED devices. In the particular embodiment illustrated, the bottom electrode layer 124 includes separate landing areas for the micro LED devices. In the particular embodiment illustrated, the bottom electrode 124 landing area supporting the micro LED device 400S is cut using a suitable technique such as laser scribing to segregate the irregular micro LED device so that it is not in electrical communication with the underlying TFT circuitry through filled opening 131.

[00115] FIG. 18 illustrates a display system 1800 in accordance with an embodiment. The display system houses a processor 1810, data receiver 1820, a display panel 100, 200, such as any of the display panels described above. The data receiver 1820 may be configured to receive data wirelessly or wired. Wireless may be implemented in any of a number of wireless standards or protocols including, but not limited to, Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond.

[00116] Depending on its applications, the display system 1800 may include other components. These other components include, but are not limited to, memory, a touch-screen controller, and a battery. In various implementations, the display system 1800 may be a television, tablet, phone, laptop, computer monitor, kiosk, digital camera, handheld game console, media display, ebook display, or large area signage display.

[00117] In utilizing the various aspects of this invention, it would become apparent to one skilled in the art that combinations or variations of the above embodiments are possible for integrating a redundancy scheme and repair site into an active matrix display panel, as well as integrating a testing method for detecting irregularities in the array of micro LED devices such as missing, defective, or contaminated micro LED devices.

[00118] While the above embodiments have been described with regard to active matrix display panels, the redundancy scheme, repair site, and testing method for detecting missing, defective, or contaminated micro LED device can also be implemented into passive matrix display

IPR2024-01134 - BOE
Exhibit 1009 - Page 284

panels, as well as substrates for lighting purposes. In addition, while the above embodiments have been described with regard to a top emission structure, embodiments of the invention are also applicable to bottom emission structures. Similarly, while top gate transistor structures have been described, embodiments of the invention may also be practiced with bottom gate transistor structures. Furthermore, while embodiments of the invention have been described and illustrated with regard to a high side drive configuration, embodiments may also be practiced with a low side drive configuration in which the ground tie lines and ground ring described above become the power line in the panel. Although the present invention has been described in language specific to structural features and/or methodological acts, it is to be understood that the invention defined in the appended claims is not necessarily limited to the specific features or acts described. The specific features and acts disclosed are instead to be understood as particularly graceful implementations of the claimed invention useful for illustrating the present invention.

IPR2024-01134 - BOE
Exhibit 1009 - Page 285

CLAIMS

What is claimed is:

1. A display panel with redundancy scheme comprising:

a display substrate including a pixel area and a non-pixel area, wherein the pixel area includes an array of subpixels and a corresponding array of bottom electrodes within the array of subpixels;

an array of micro LED device pairs bonded to the array of bottom electrodes; and

one or more top electrode layers in electrical contact with the array of micro LED device pairs.

2. The display panel of claim 1, wherein each micro LED device is formed of a semiconductor material.

3. The display panel of claim 2, wherein each micro LED device has a maximum width of 1 to 100 μm.

4. The display panel of claim 2, wherein the display substrate is a thin film transistor substrate.

5. The display panel of claim 4, further comprising a ground line in the non-pixel area of the thin film transistor substrate, wherein the one or more top electrode layers are electrically connected to the ground line.

6. The display of claim 5, wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the micro LED device pair to the ground line.

7. The display panel of claim 2, further comprising an array of micro controller chips bonded to the display substrate, wherein each bottom electrode is electrically connected to a micro controller chip.

IPR2024-01134 - BOE
Exhibit 1009 - Page 286

8. The display panel of claim 7, wherein each micro controller chip is connected to a scan driver circuit and a data driver circuit.

9. The display panel of claim 8, further comprising a ground line in the non-pixel area of the display substrate, wherein the one or more top electrode layers are electrically connected to the ground line.

10. The display of claim 9, wherein the one or more top electrode layers comprise a first top electrode layer electrically connecting a first micro LED device of a micro LED device pair to the ground line, and a separate second top electrode layer electrically connecting a second micro LED device of the micro LED device pair to the ground line.

11. The display of claim 2, further comprising:

a plurality of micro LED device irregularities within the array of micro LED device pairs, the irregularities selected from the group consisting of missing micro LED devices, defective micro LED devices, and contaminated micro LED devices; and

a passivation layer material covering the plurality of irregularities.

12. The display of claim 11, wherein the one or more top electrode layers do not make electrical contact with the plurality of irregularities.

13. The display of claim 13, wherein the one or more top electrode layers are formed directly over the plurality of irregularities.

14. The display of claim 13, wherein the one or more top electrode layers are not formed directly over the plurality of irregularities.

15. The display panel of claim 12, wherein the plurality of micro LED device irregularities are missing micro LED devices.

IPR2024-01134 - BOE
Exhibit 1009 - Page 287

16. The display panel of claim 15, further comprising an array of bonding layers on the array of bottom electrodes corresponding to the plurality of missing micro LED devices, wherein the passivation layer material covers the array of bonding layers.

17. The display panel of claim 12, wherein the plurality of micro LED device irregularities are defective micro LED devices and the passivation layer material covers the defective micro LED devices.

18. The display panel of claim 12, wherein the plurality of micro LED device irregularities are contaminated micro LED devices and the passivation layer material covers the contaminated micro LED devices.

19. The display panel of claim 11, wherein the passivation layer material covers sidewalls of the array of micro LED device pairs.

20. The display panel of claim 11, further comprising a repair micro LED device bonded to one of the bottom electrodes including one of the micro LED device irregularities.

IPR2024-01134 - BOE
Exhibit 1009 - Page 288

ABSTRACT OF THE INVENTION

A display panel and method of manufacture are described. In an embodiment, a display substrate includes a pixel area and a non-pixel area. An array of subpixels and corresponding array of bottom electrodes are in the pixel area. An array of micro LED devices are bonded to the array of bottom electrodes. One or more top electrode layers are formed in electrical contact with the array of micro LED devices. In one embodiment a redundant pair of micro LED devices are bonded to the array of bottom electrodes. In one embodiment, the array of micro LED devices are imaged to detect irregularities.

IPR2024-01134 - BOE
Exhibit 1009 - Page 289

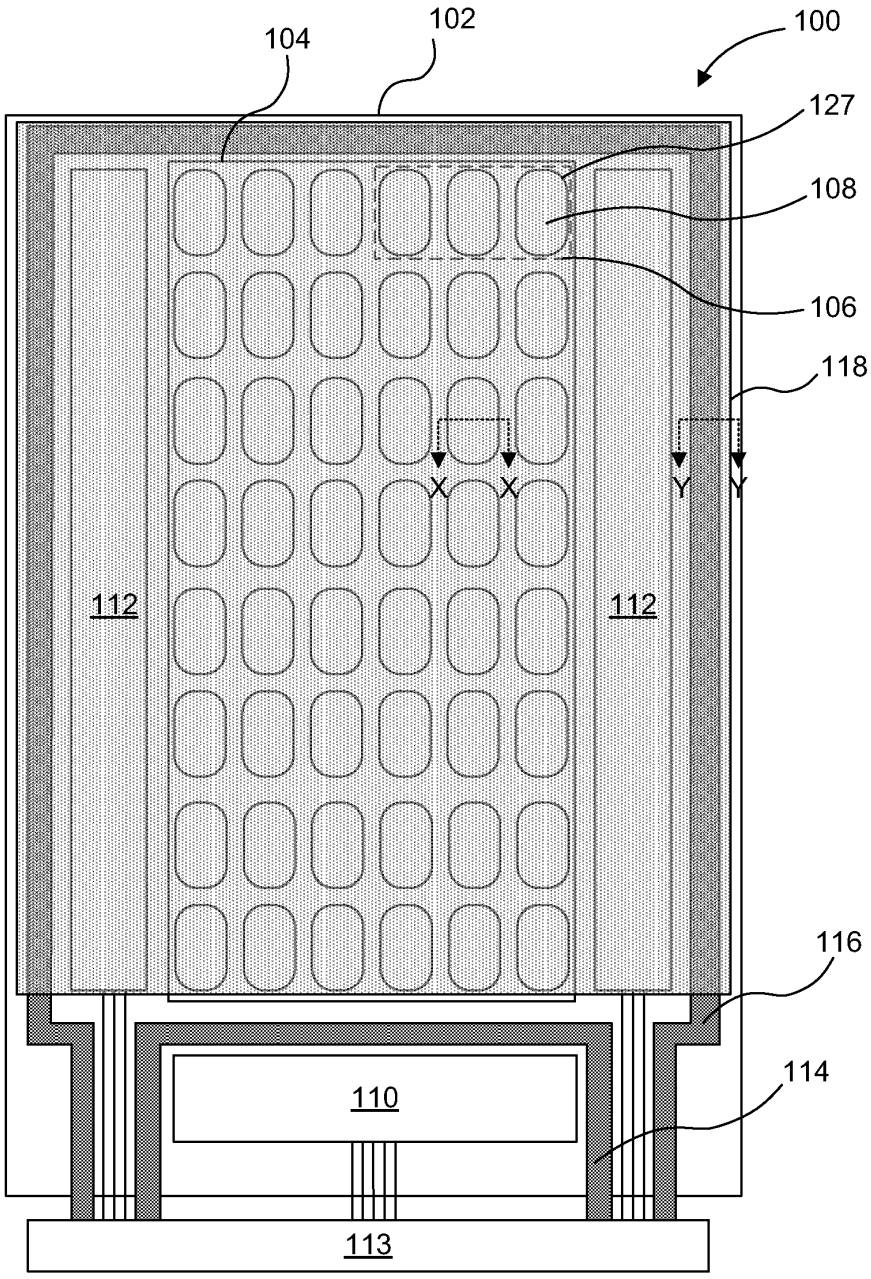


FIG. 1
PRIOR ART

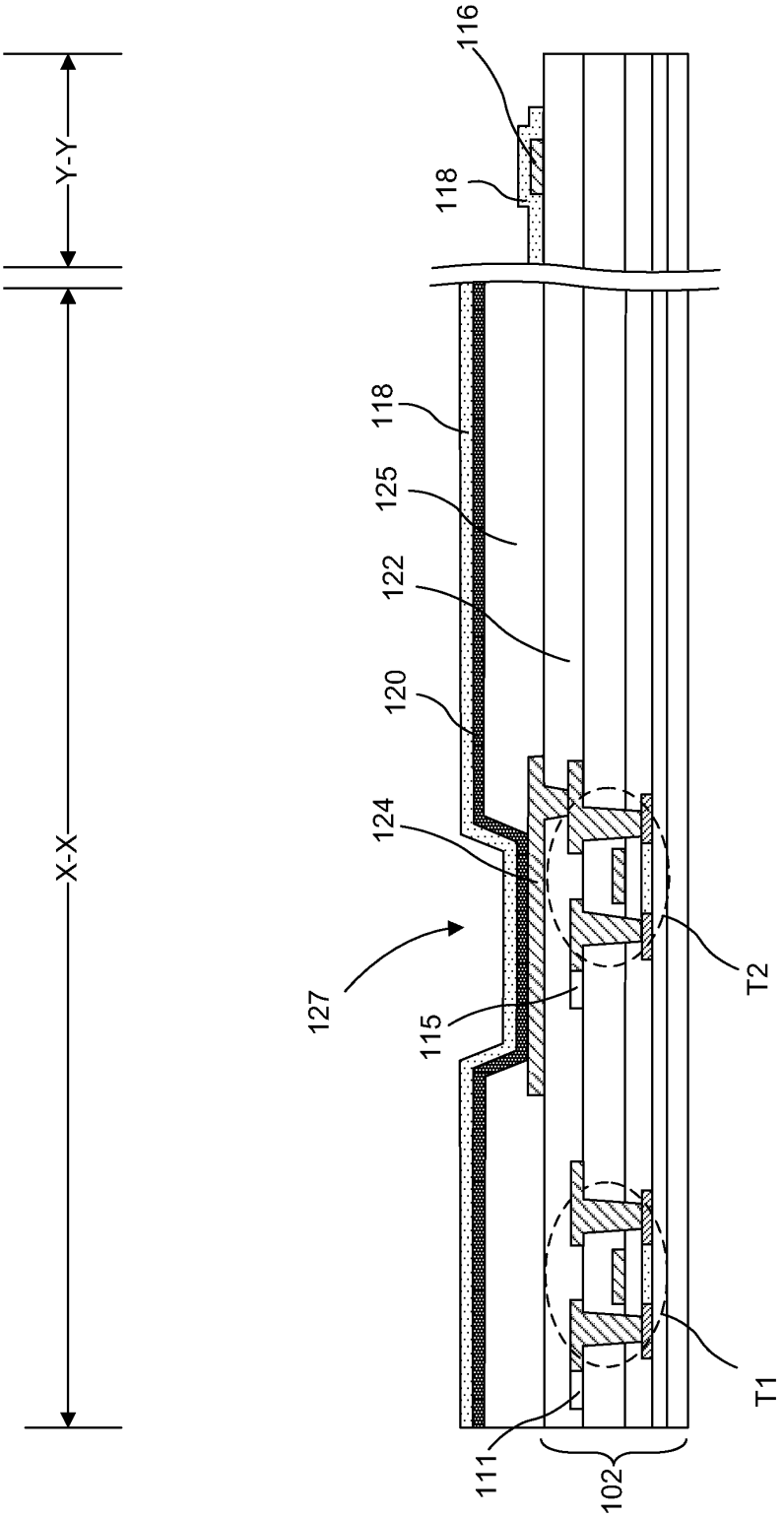


FIG. 2
PRIOR ART

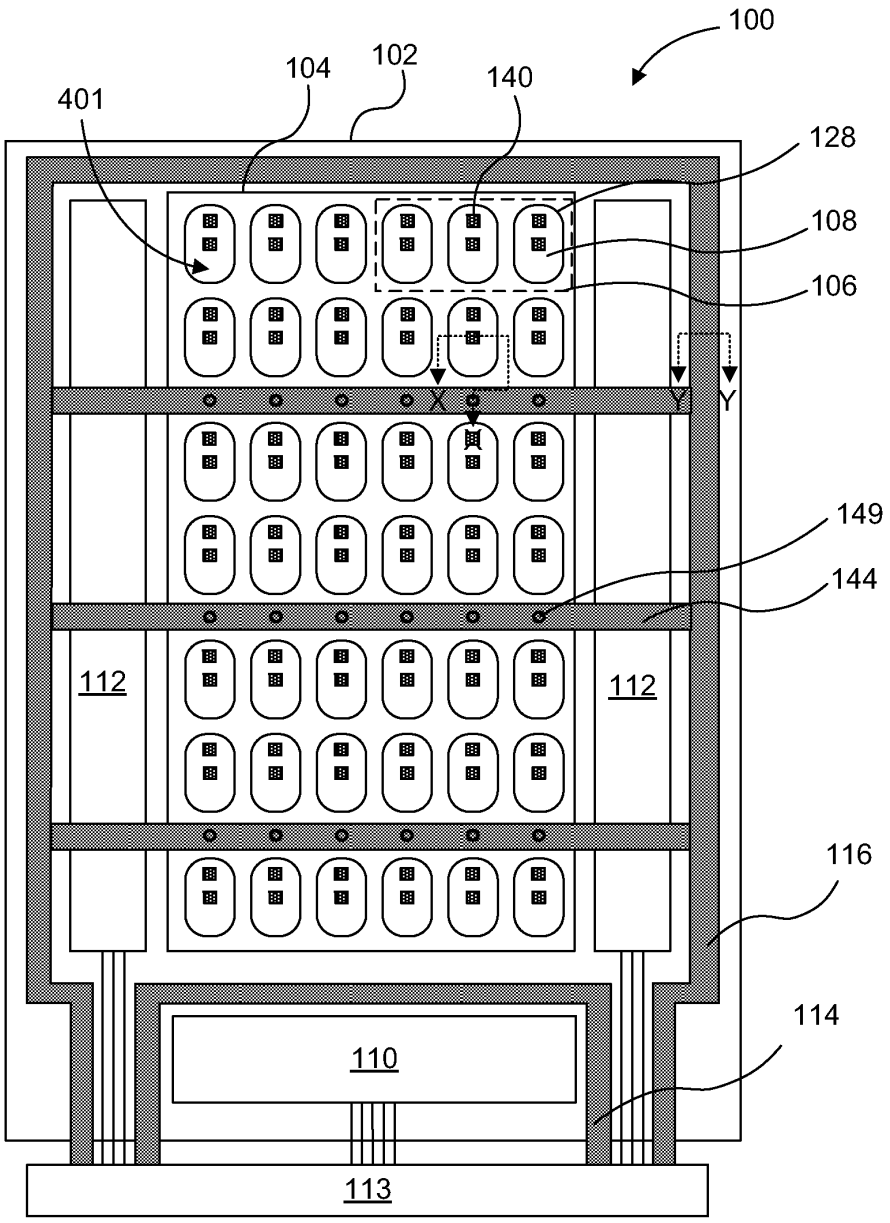

100
104
102
140
401
128
108
106
X
X
Y
Y
149
144
112
112
116
114
110
113

FIG. 3A

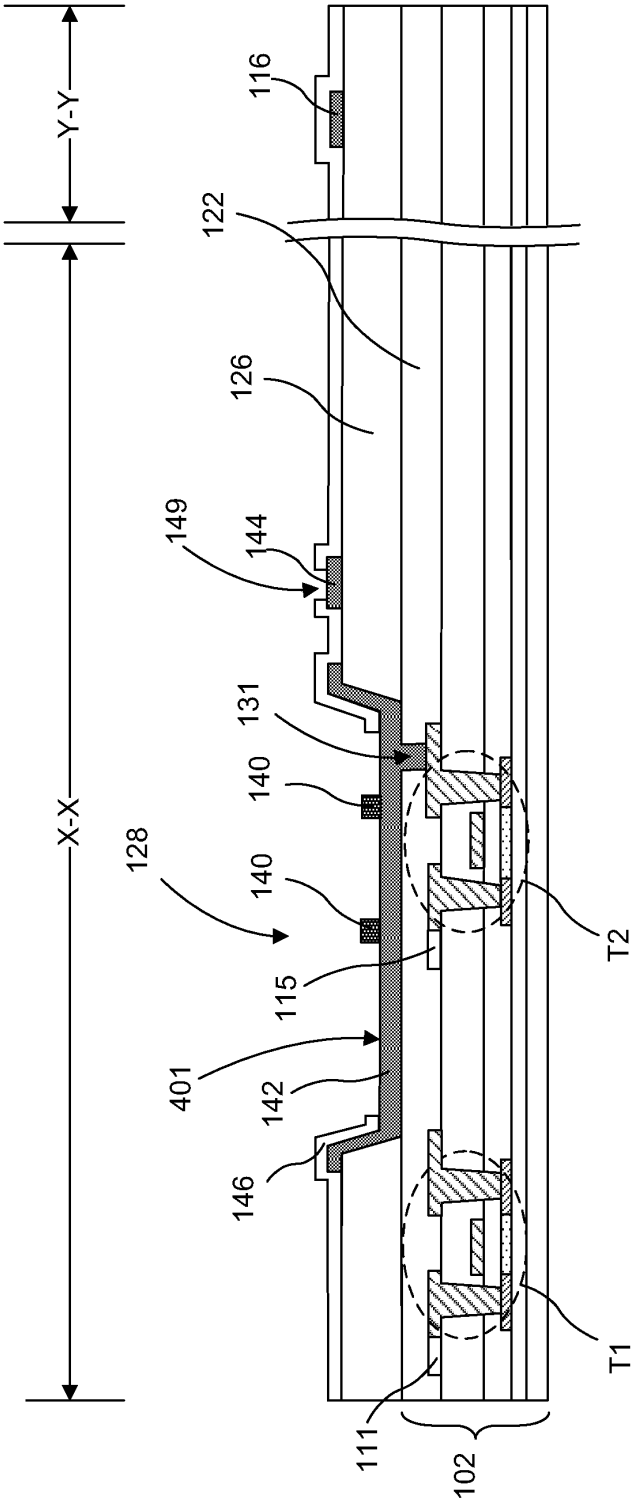

Y-Y
X-X
116
122
126
149
144
131
140
128
140
115
401
142
146
T2
T1
111
102

FIG. 3B

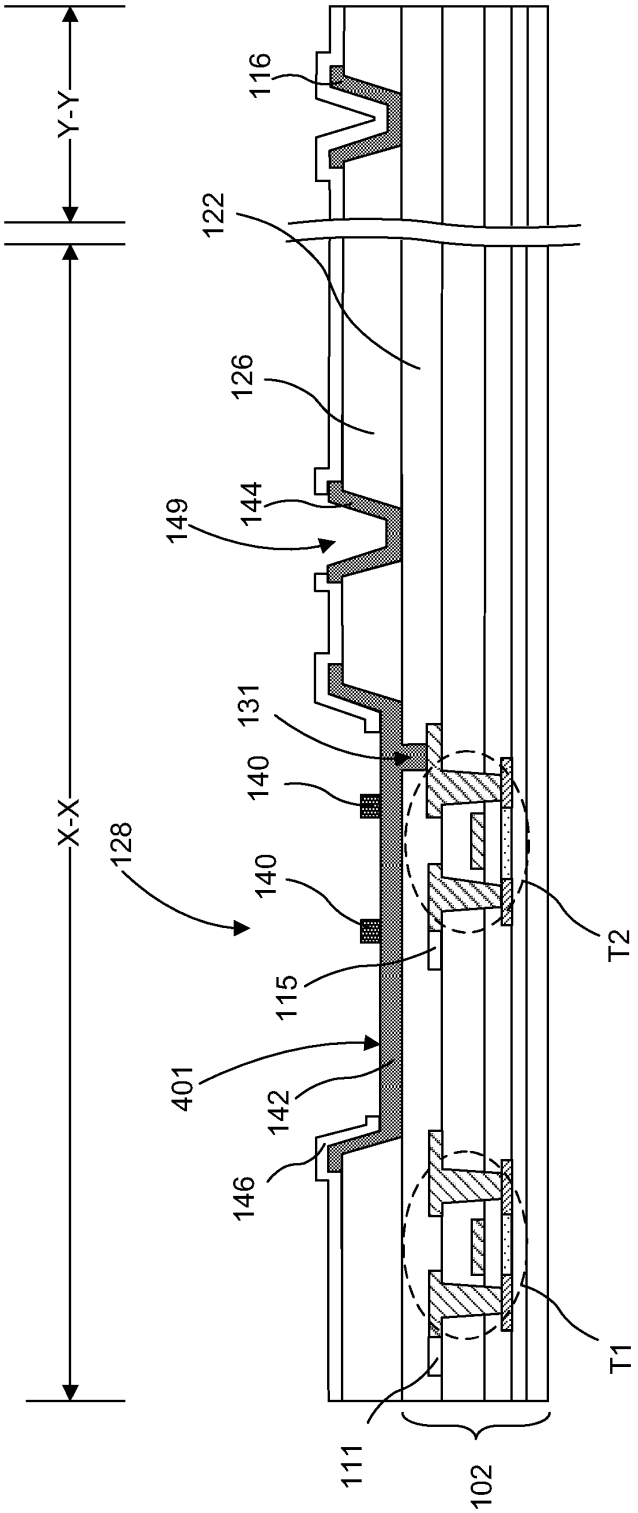

Y-Y
X-X
116
122
126
144
149
131
140
128
140
115
401
142
146
T2
T1
111
102

FIG. 3C

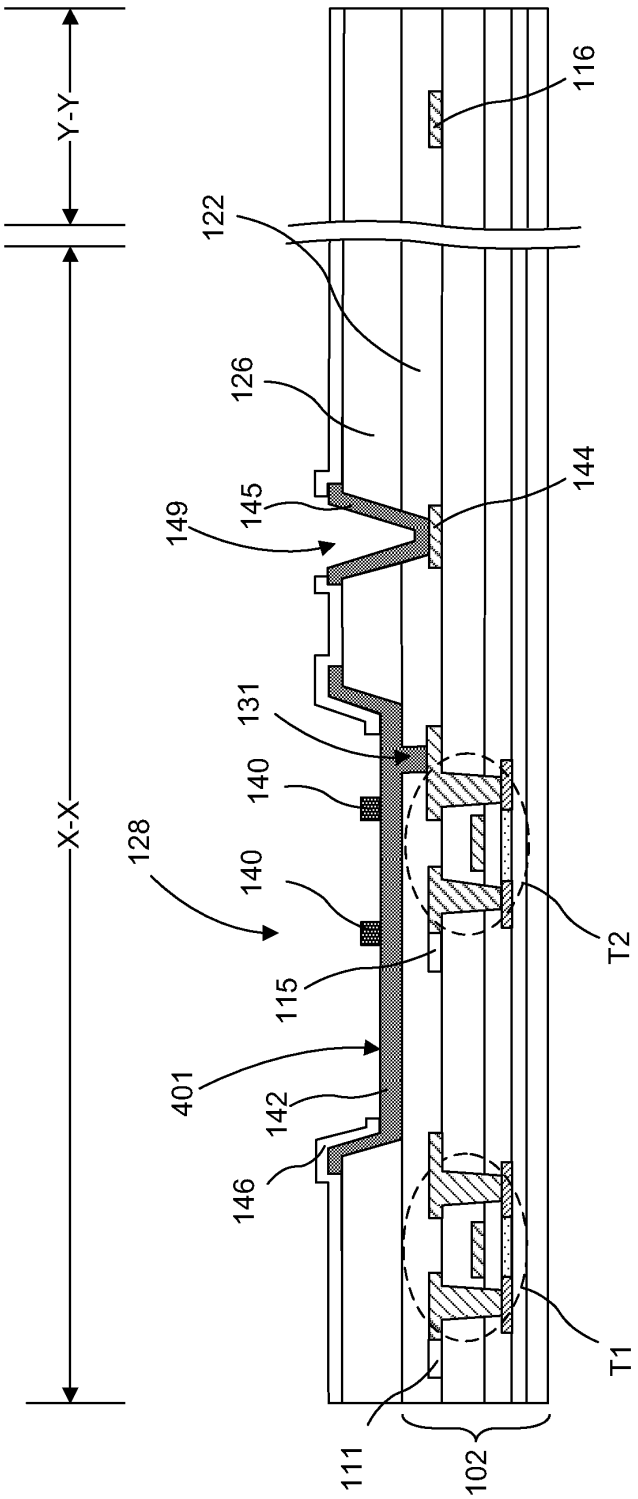

Y-Y
X-X
116
122
126
144
145
149
131
140
128
140
115
T2
401
142
146
T1
111
102

FIG. 3D

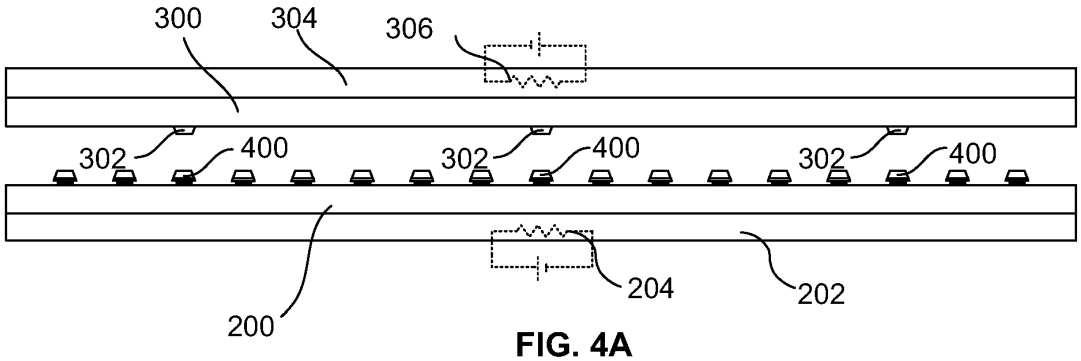


FIG. 4A

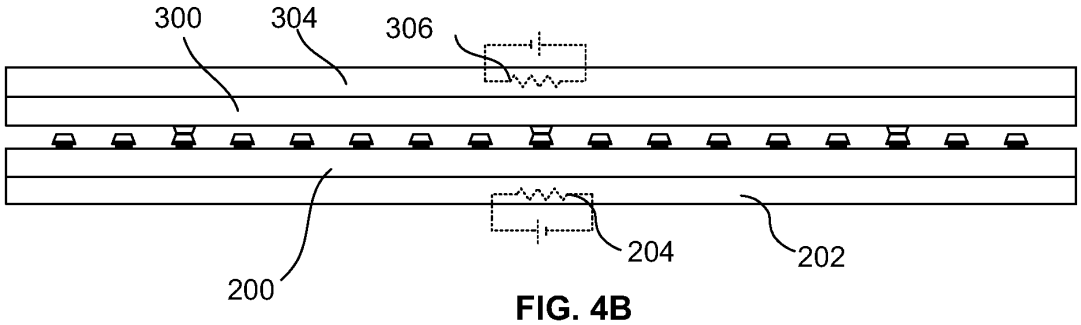


FIG. 4B

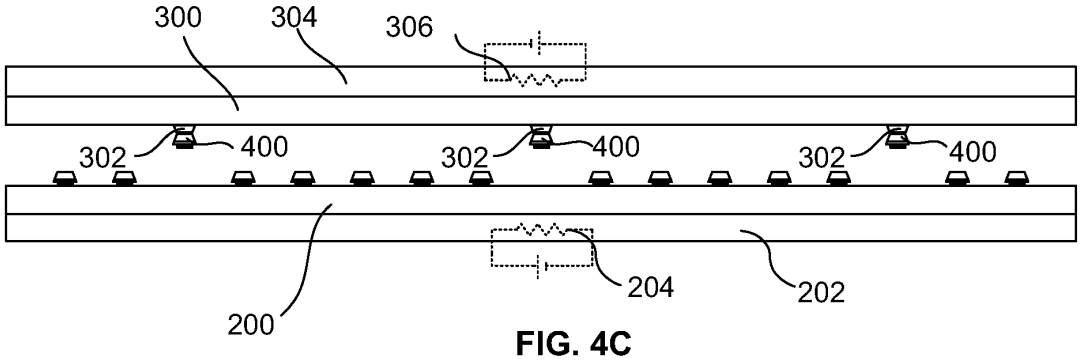


FIG. 4C

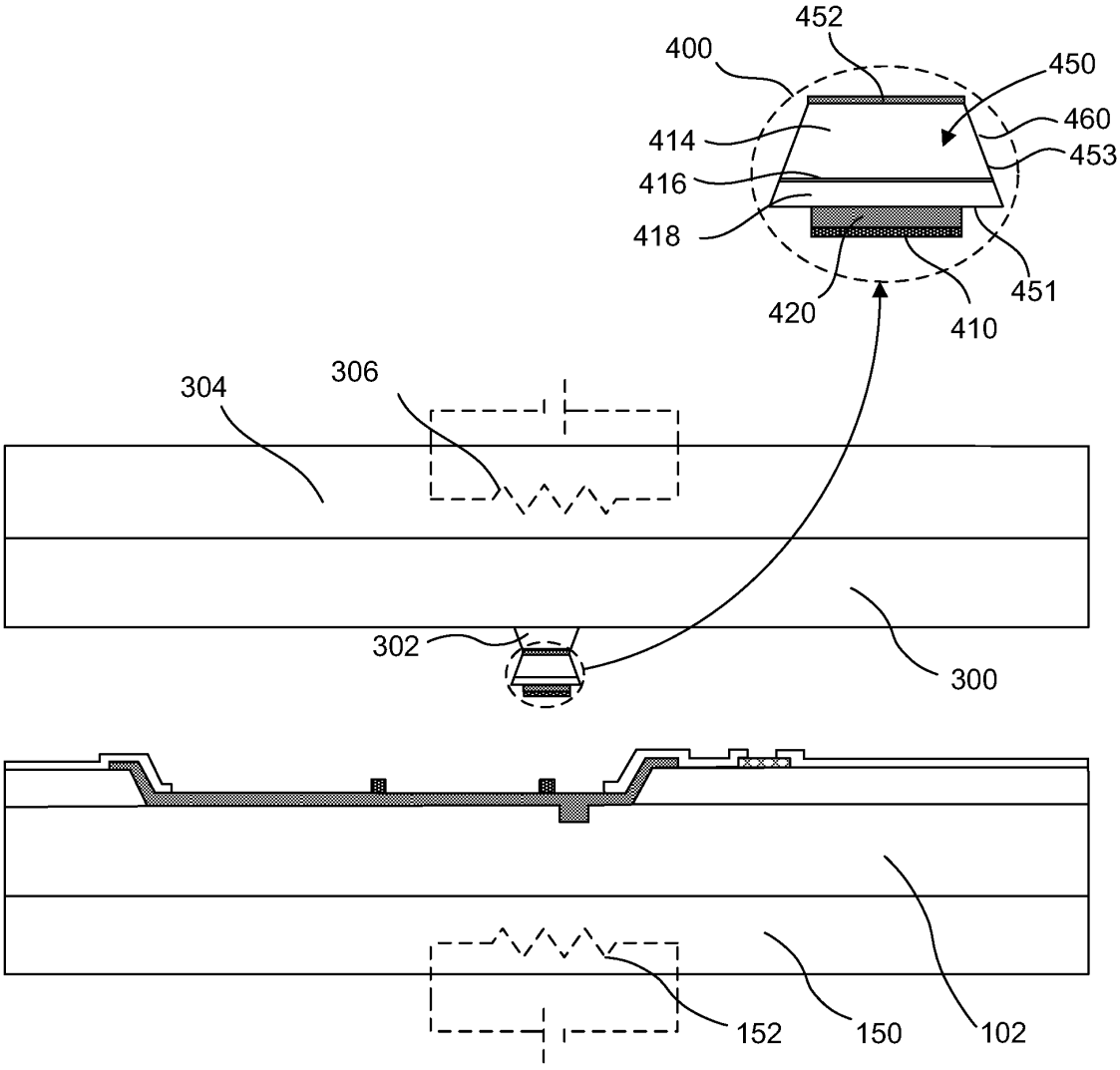

452
400
450
460
414
453
416
418
451
420
410
304
306
302
300
152
150
102

FIG. 4D

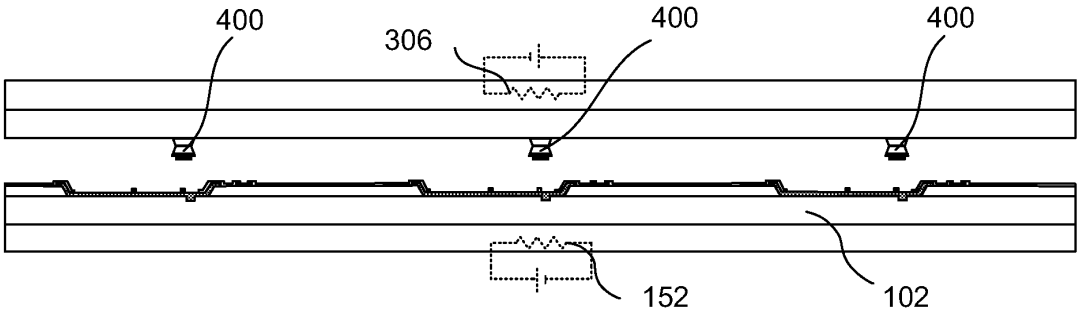

400
306
400
400
152
102

FIG. 4E

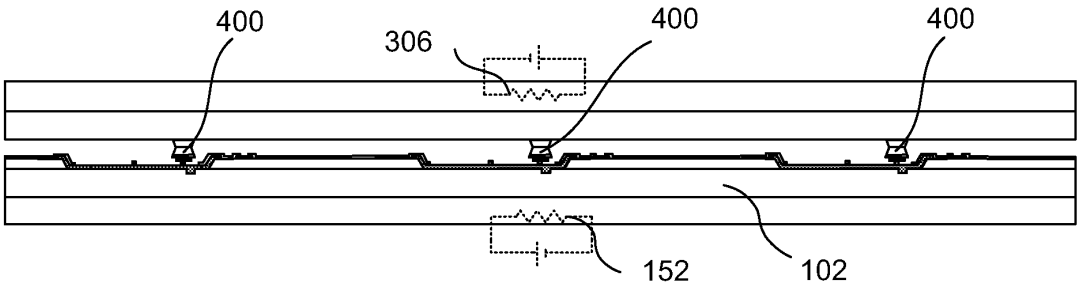


FIG. 4F

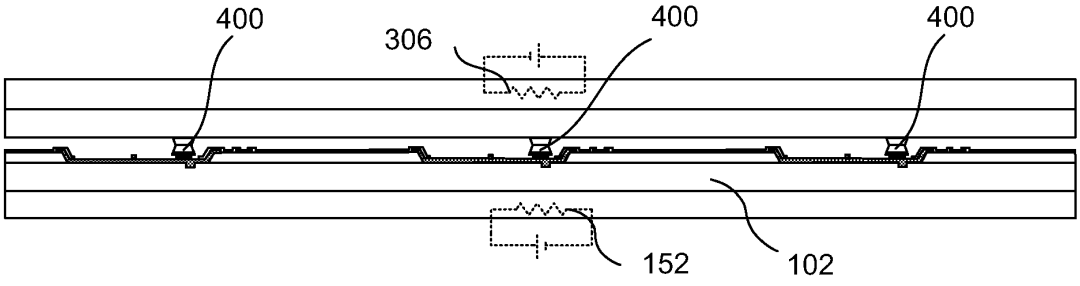


FIG. 4G

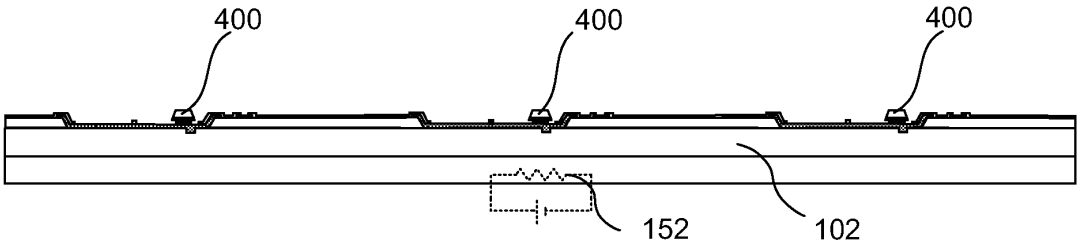


FIG. 4H

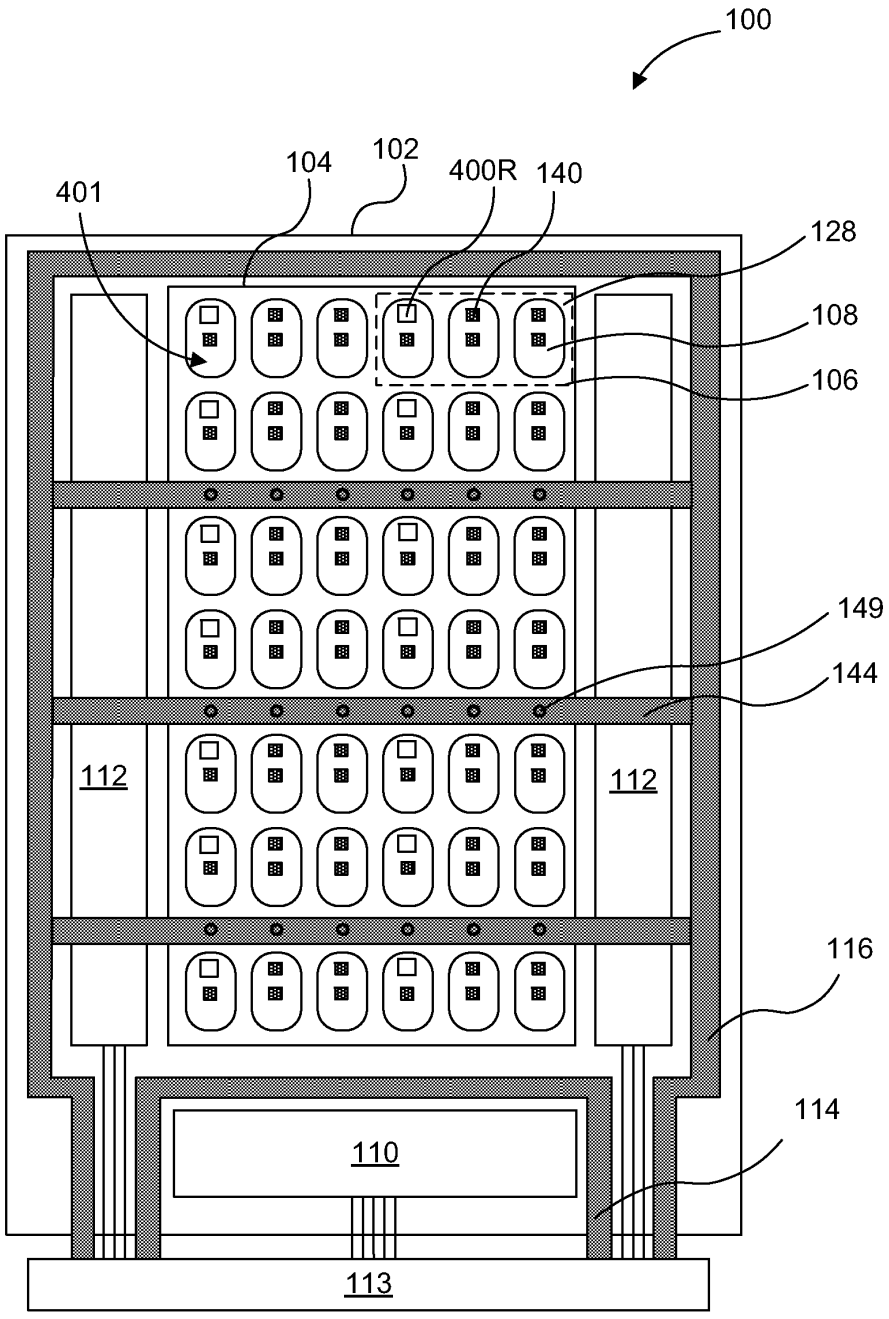

100
104
102
400R
140
401
128
108
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149
144
112
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116
114
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113

FIG. 5A

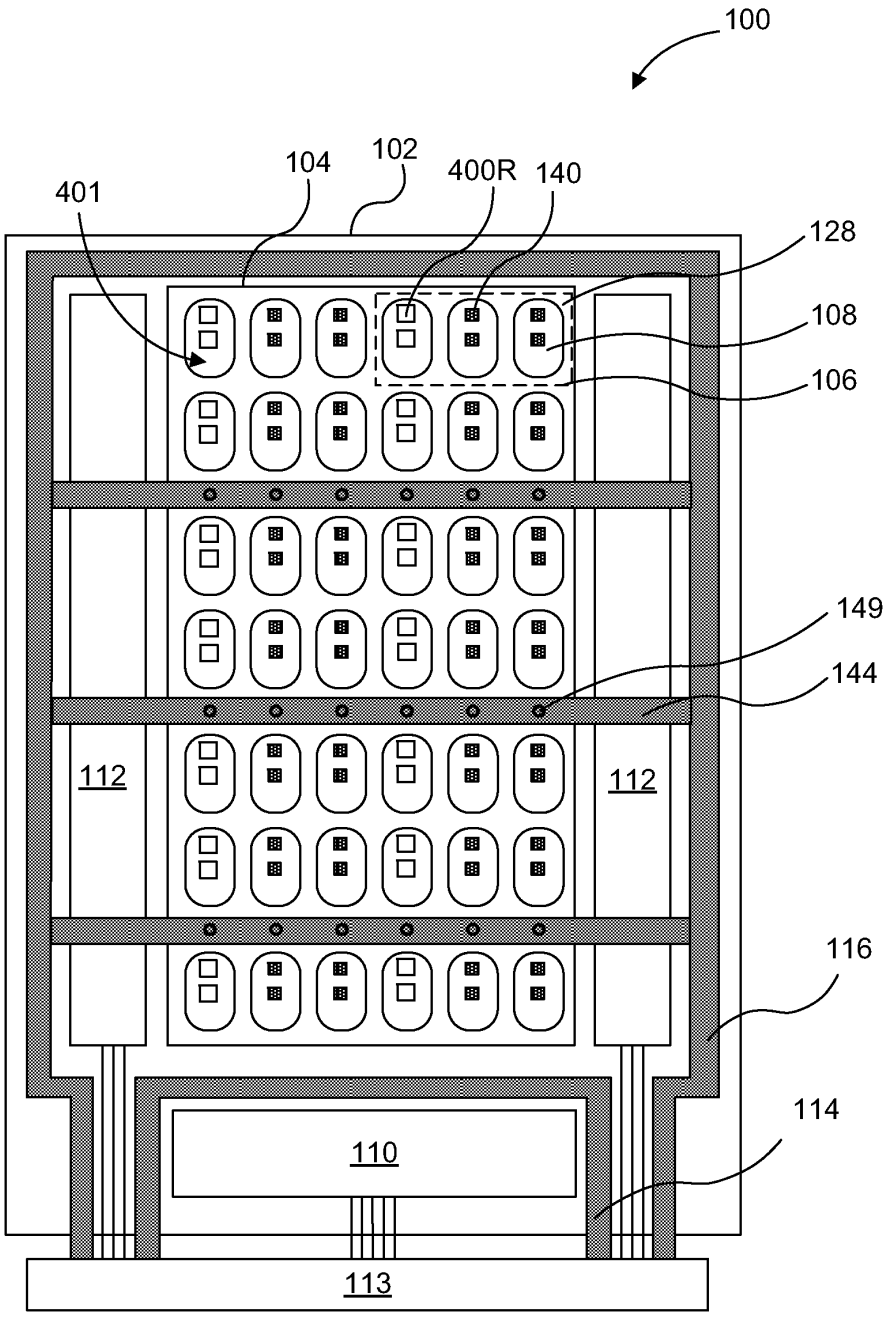

100
104
102
400R
140
401
128
108
106
149
144
112
112
116
114
110
113

FIG. 5B

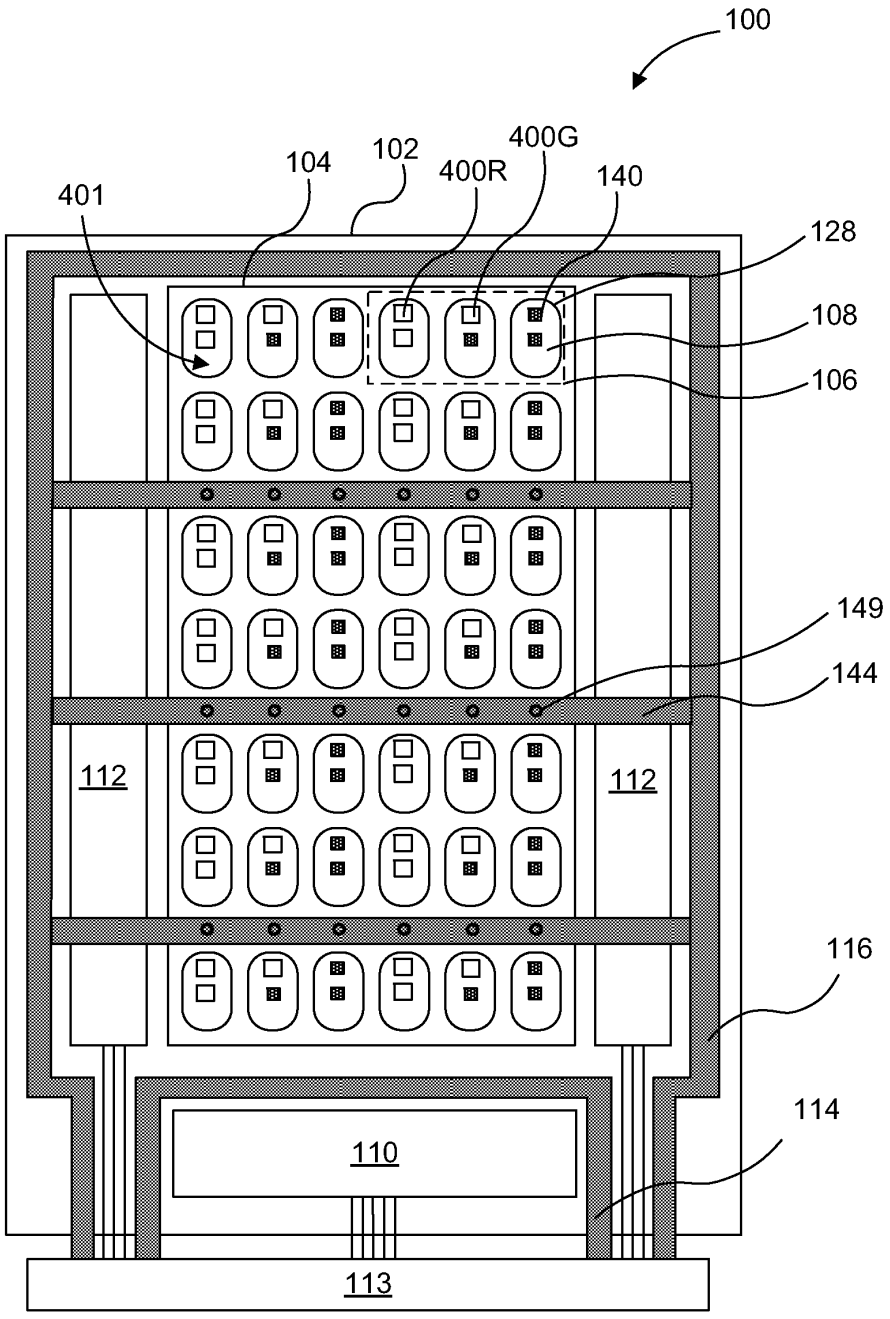

100
104
102
400G
400R
140
401
128
108
106
149
144
112
112
116
114
110
113

FIG. 5C

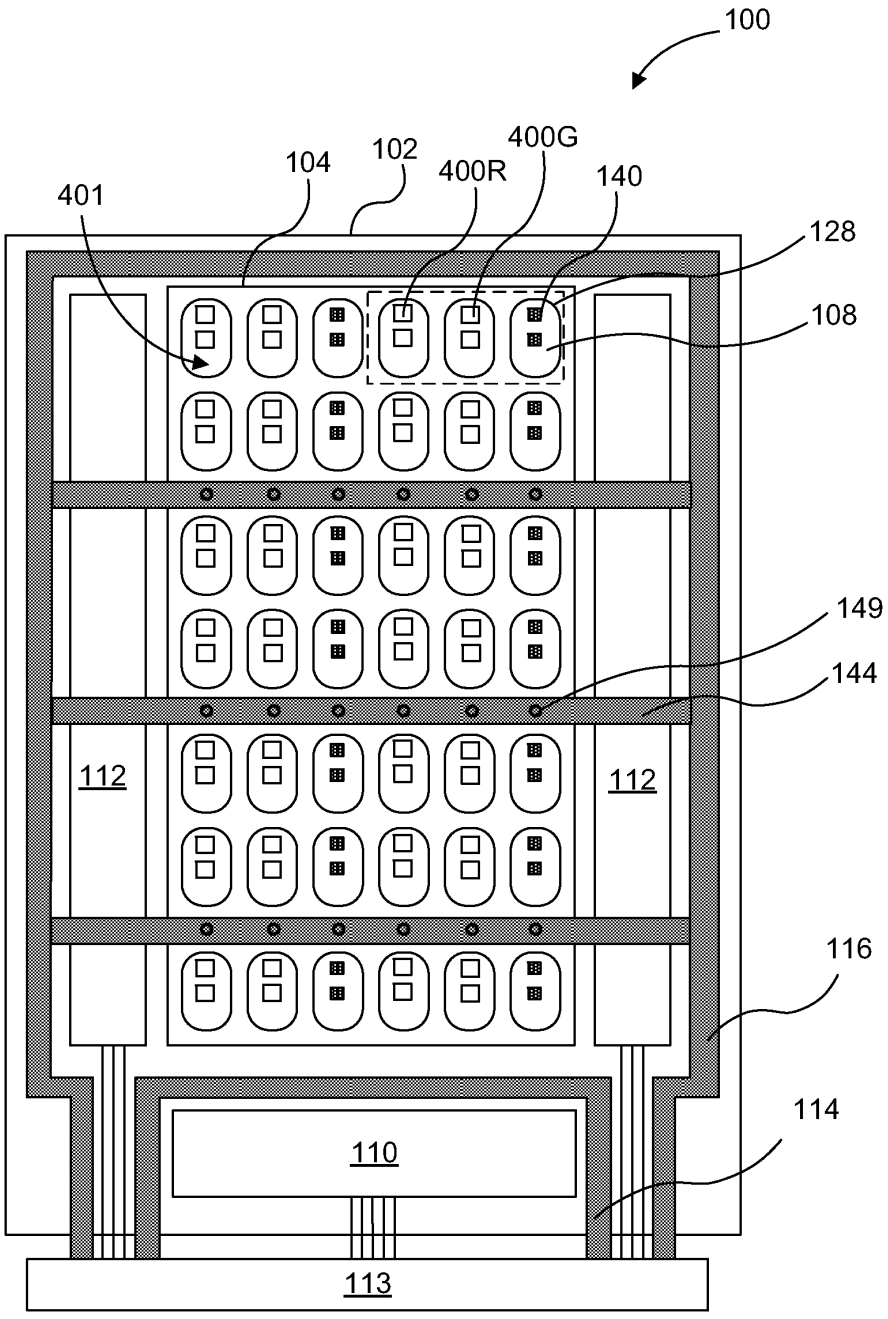

100
104
102
400G
400R
140
401
128
108
149
144
112
112
116
114
110
113

FIG. 5D

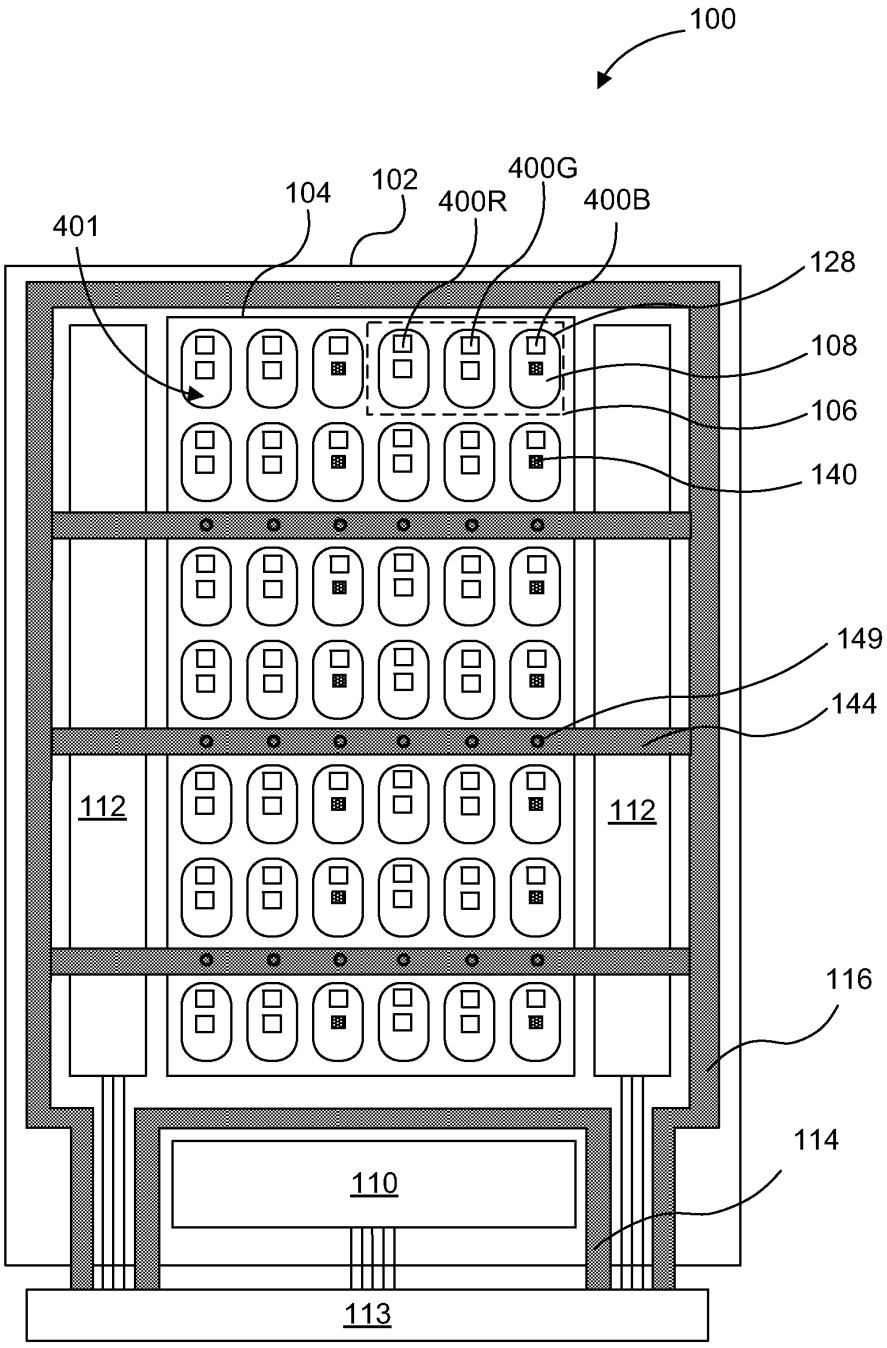

100
104
102
400G
400R
400B
401
128
108
106
140
149
144
112
112
116
114
110
113

FIG. 5E

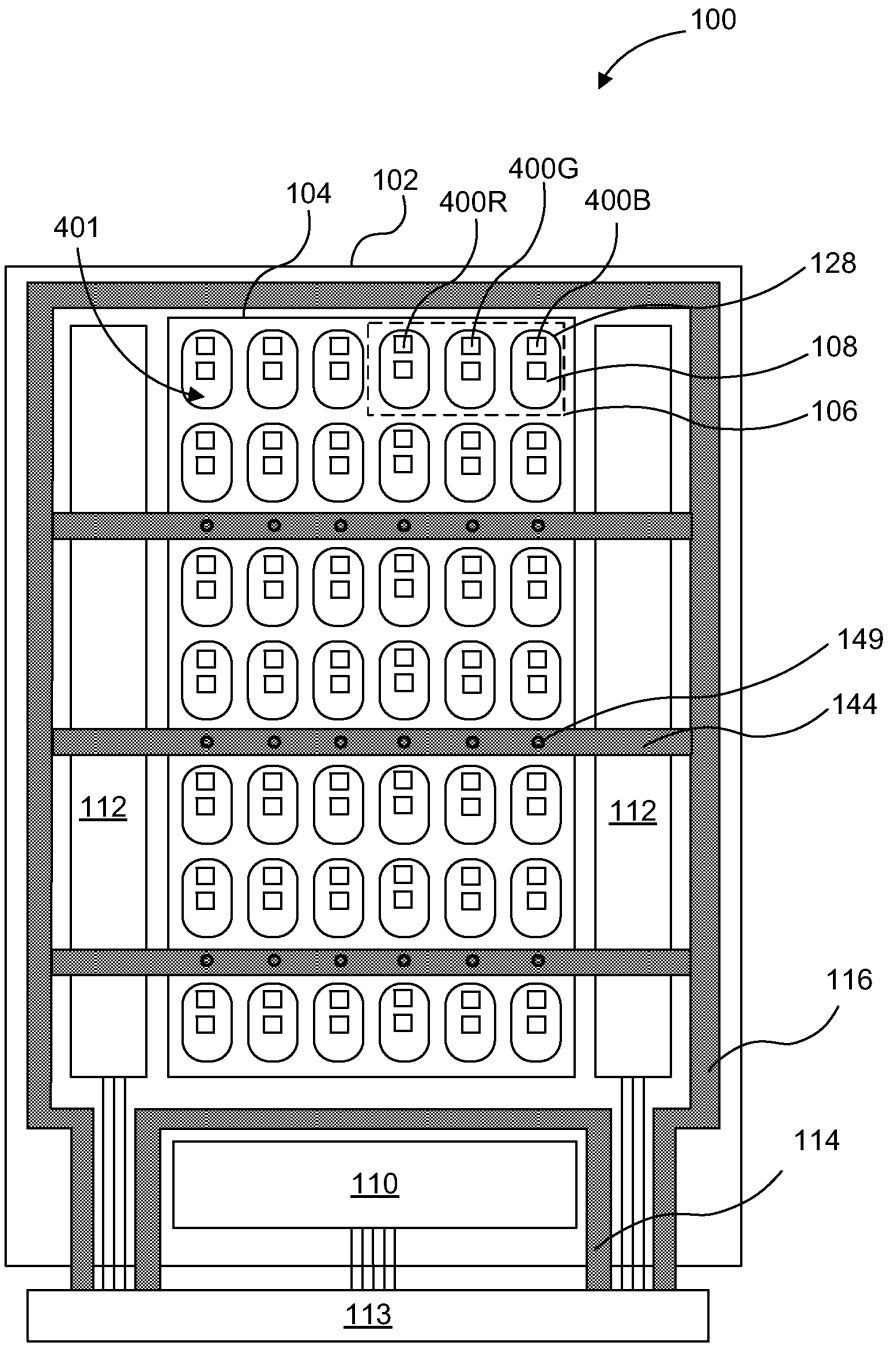

100
104
102
400G
400R
400B
401
128
108
106
149
144
112
112
116
114
110
113

FIG. 5F

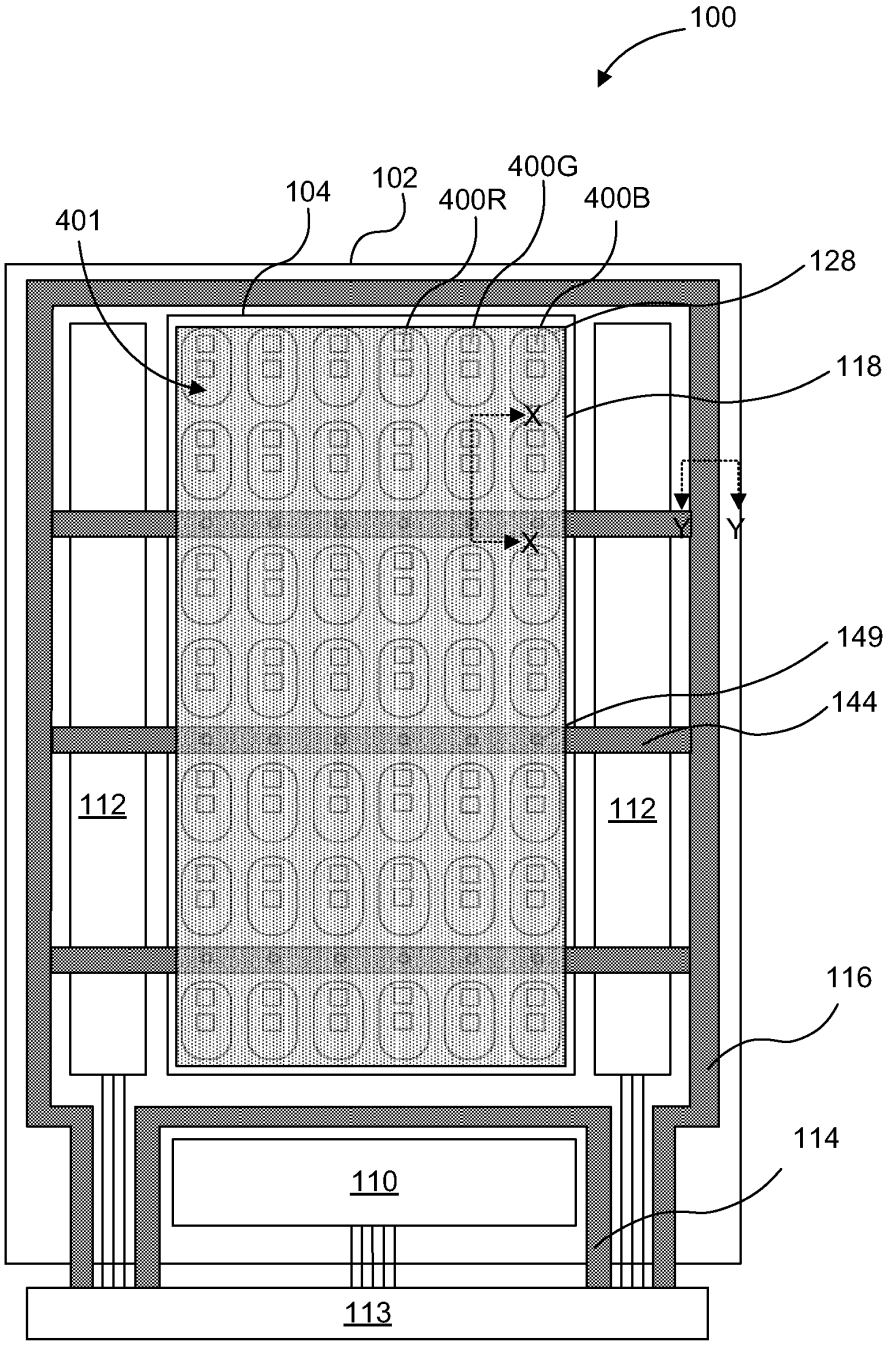

100
401
104
102
400R
400G
400B
128
118
X
X
Y
Y
149
144
112
112
116
114
110
113

FIG. 6A

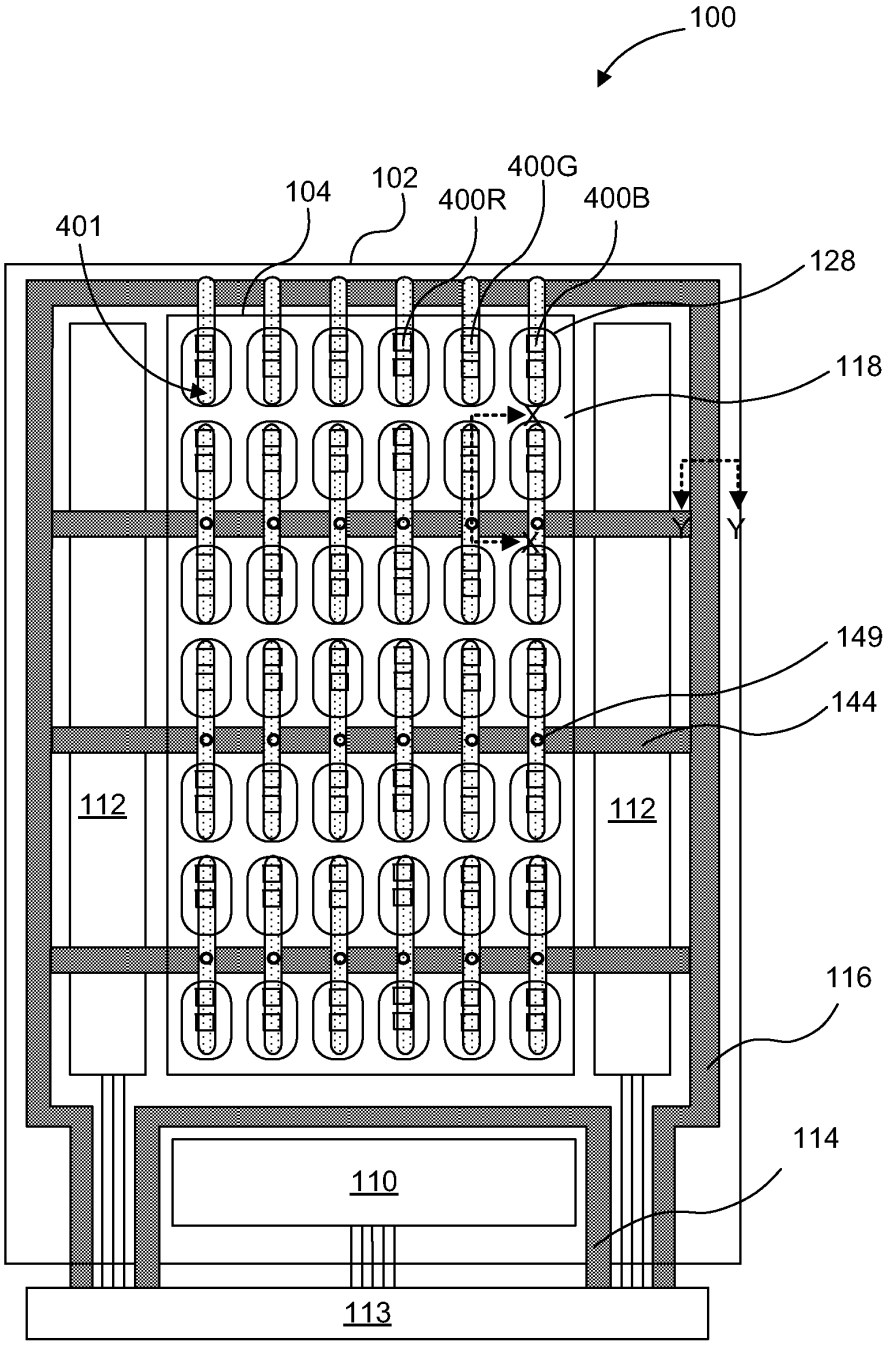

100
104
102
400G
400R
400B
401
128
118
X
X
Y
Y
149
144
112
112
116
114
110
113

FIG. 6B

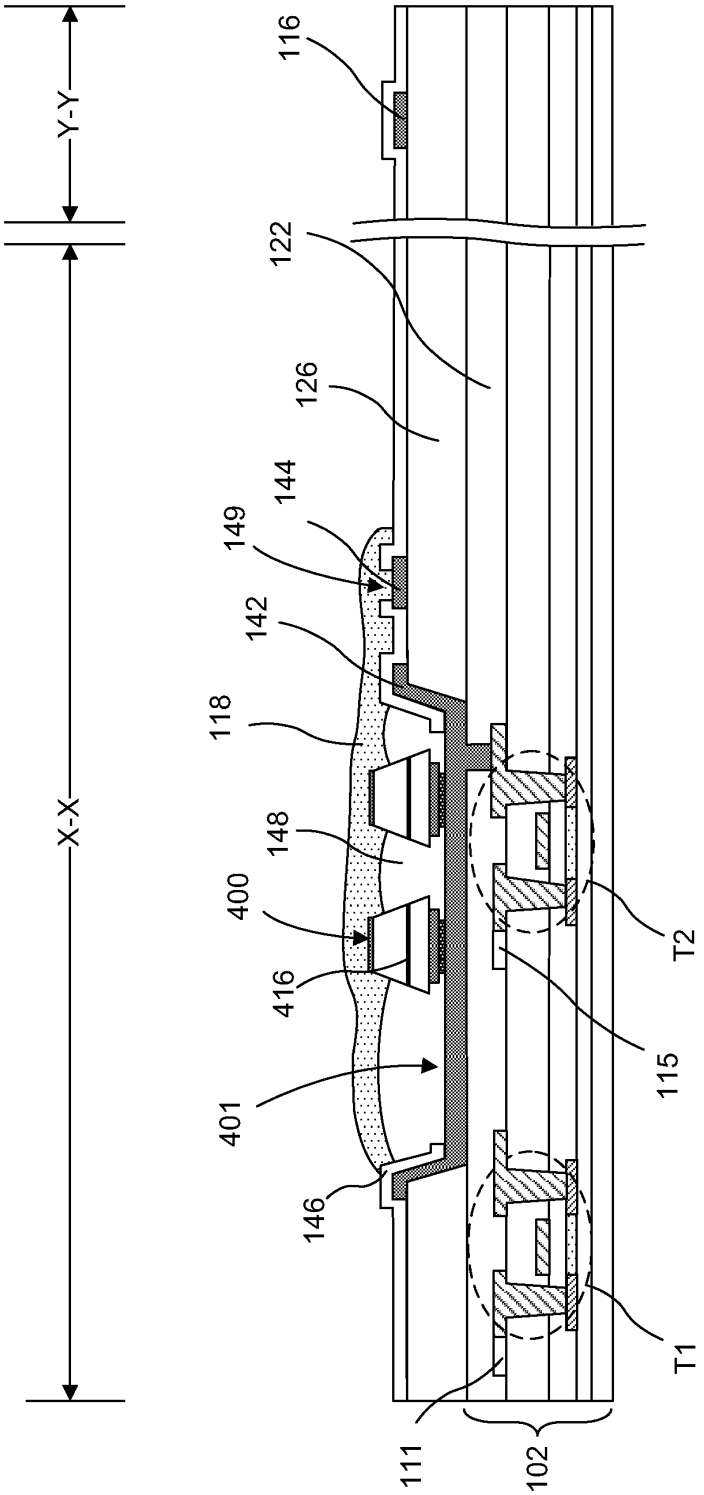

Y-Y
X-X
116
122
126
144
149
142
118
148
400
416
401
146
111
102
T1
T2
115

FIG. 6C

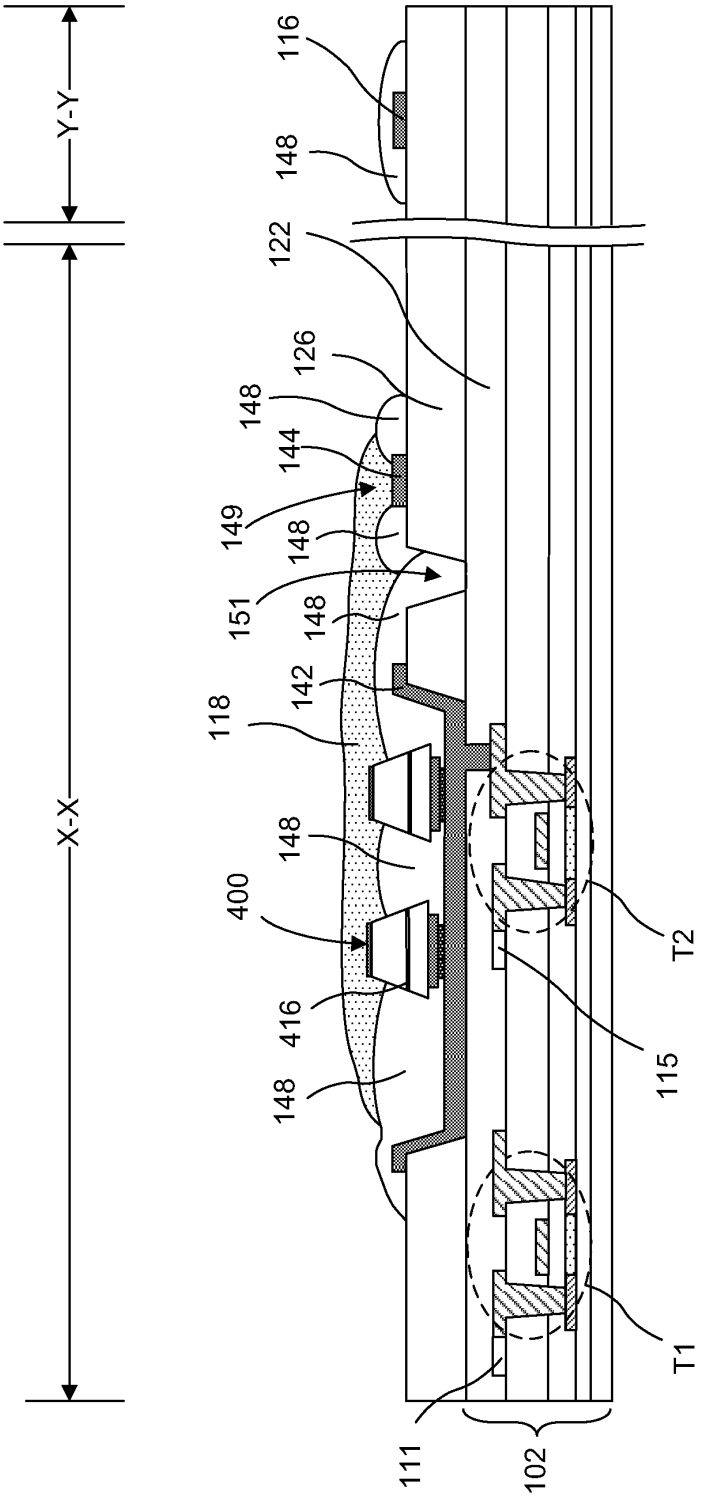

Y-Y
X-X
116
148
122
126
148
144
149
148
151
148
142
118
148
400
416
148
115
T2
T1
111
102

FIG. 6D

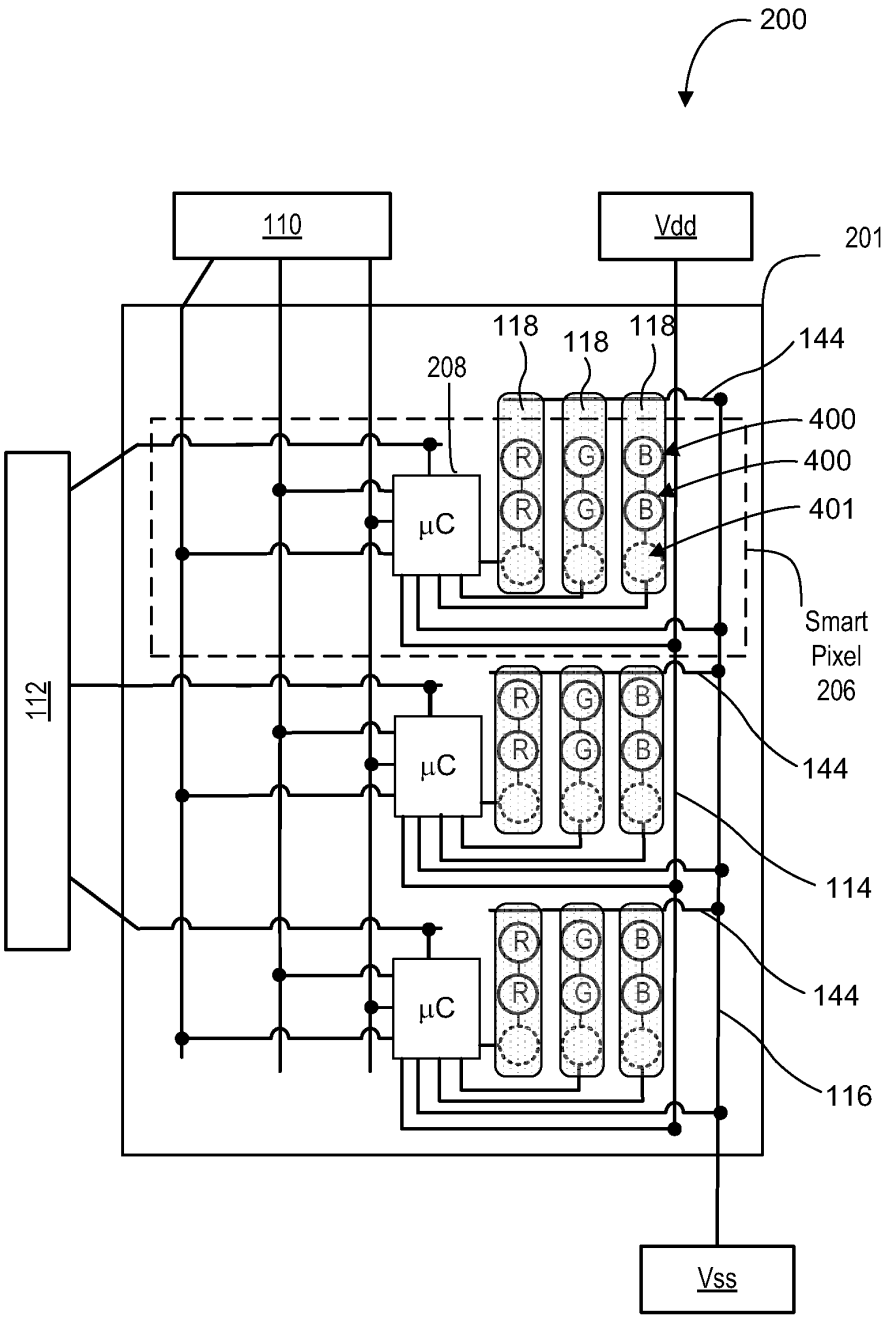

200
110
Vdd
201
118
118
118
144
208
400
400
401
R
G
B
μC
Smart
Pixel
206
112
144
114
144
116
Vss

FIG. 7

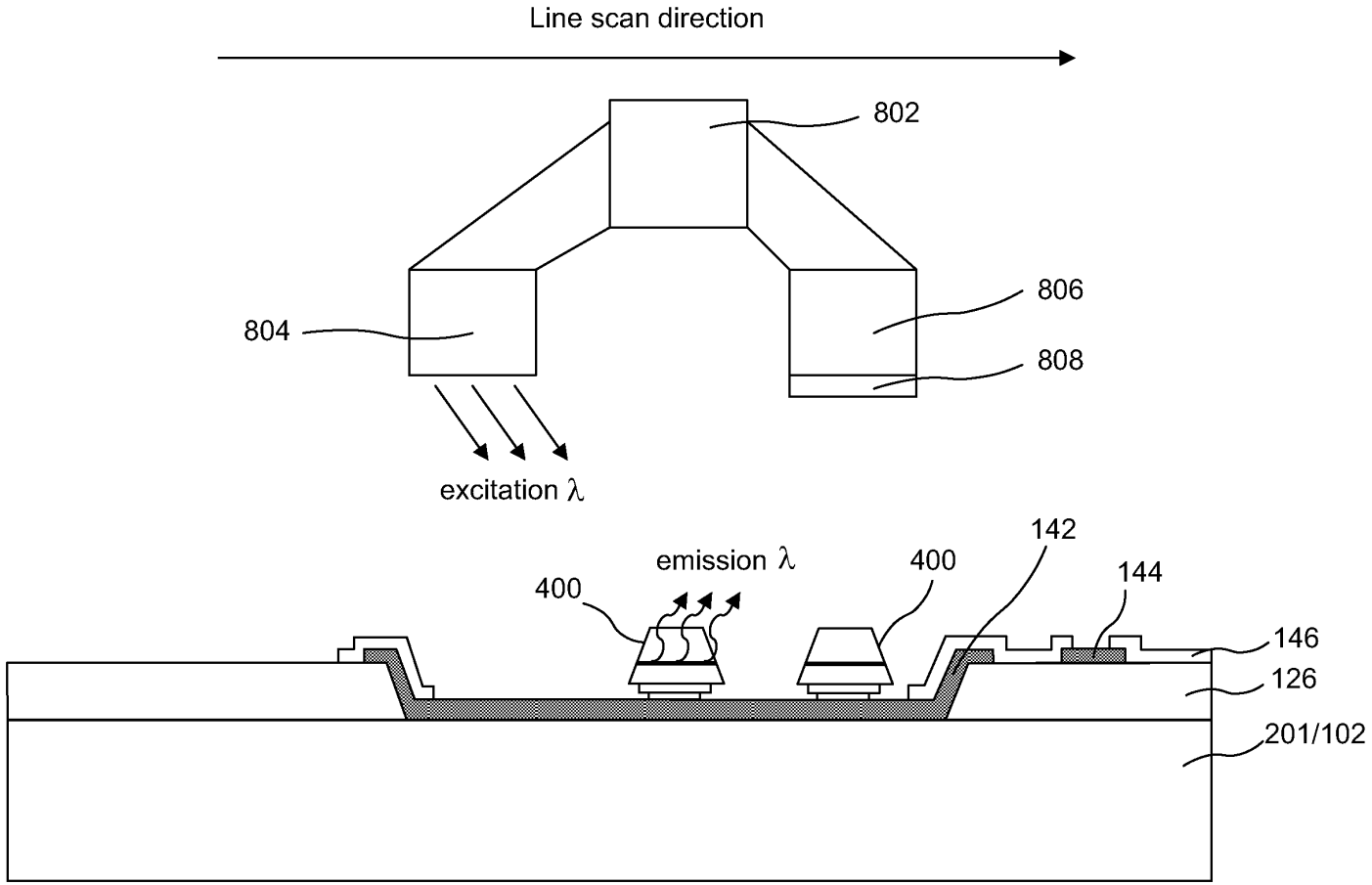


FIG. 8A

IPR2024-01134 - BOE
Exhibit 1009 - Page 310

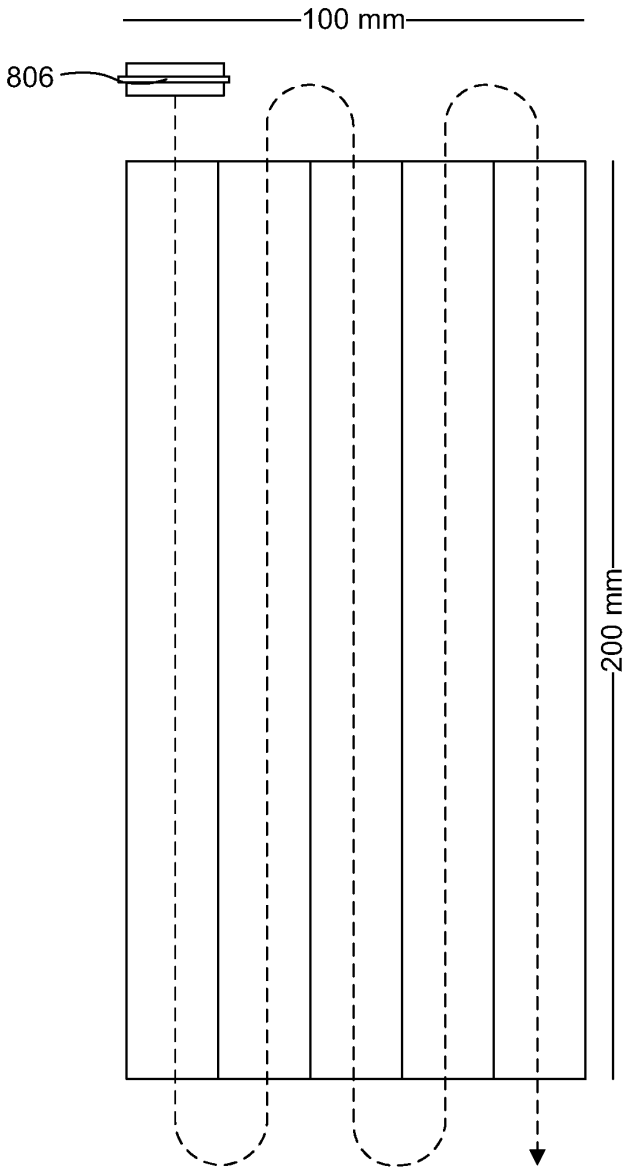


FIG. 8B

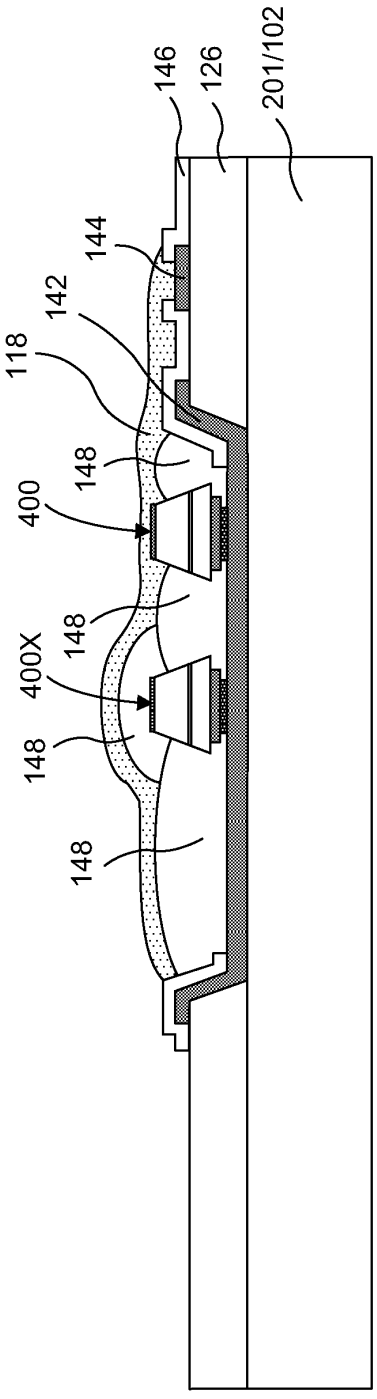

146
126
201/102
144
142
118
148
400
148
400X
148
148

FIG. 9

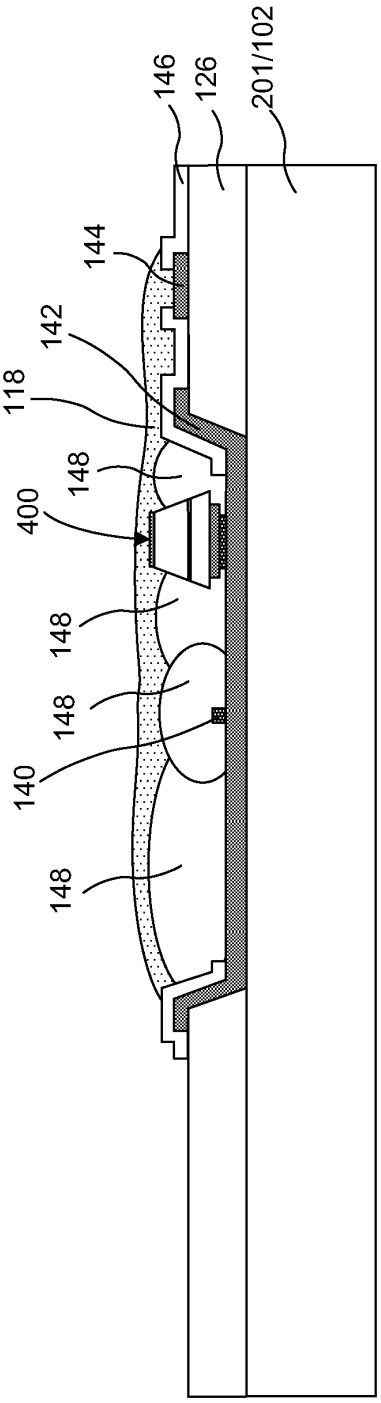

146
126
201/102
144
142
118
148
400
148
148
140
148

FIG. 10

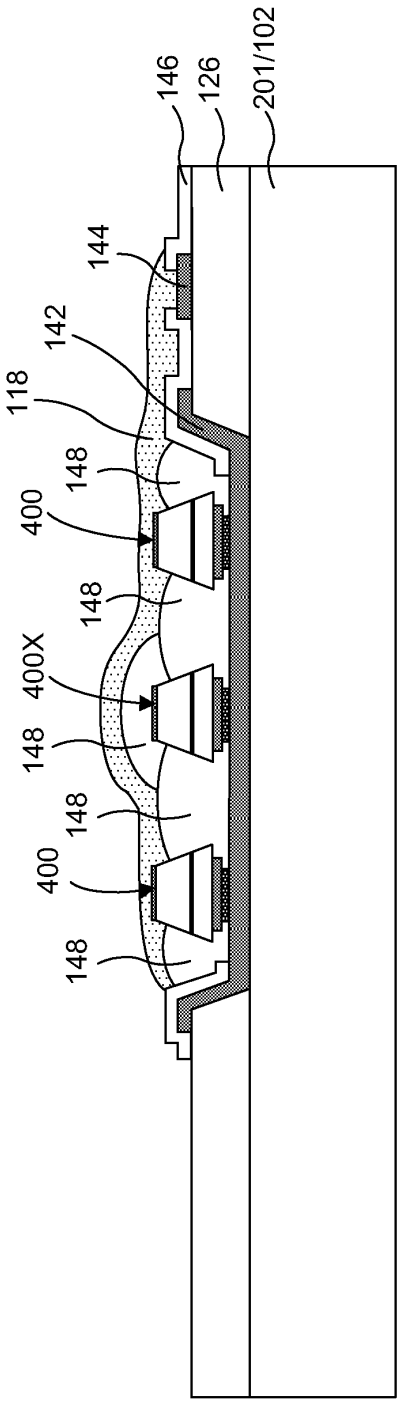

146
126
201/102
144
142
118
148
400
148
400X
148
148
400
148

FIG. 11

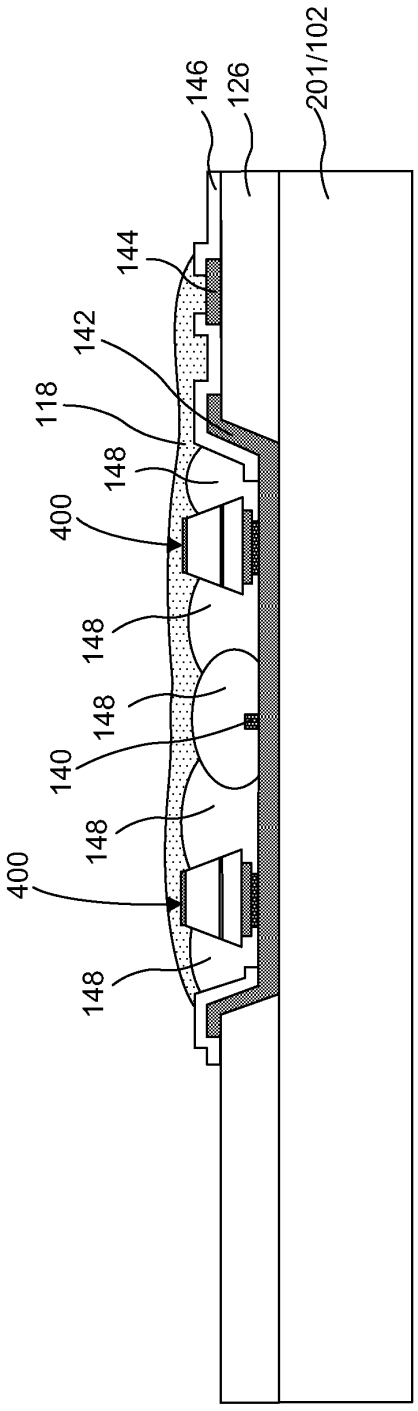

146
126
201/102
144
142
118
148
400
148
148
140
148
400
148

FIG. 12

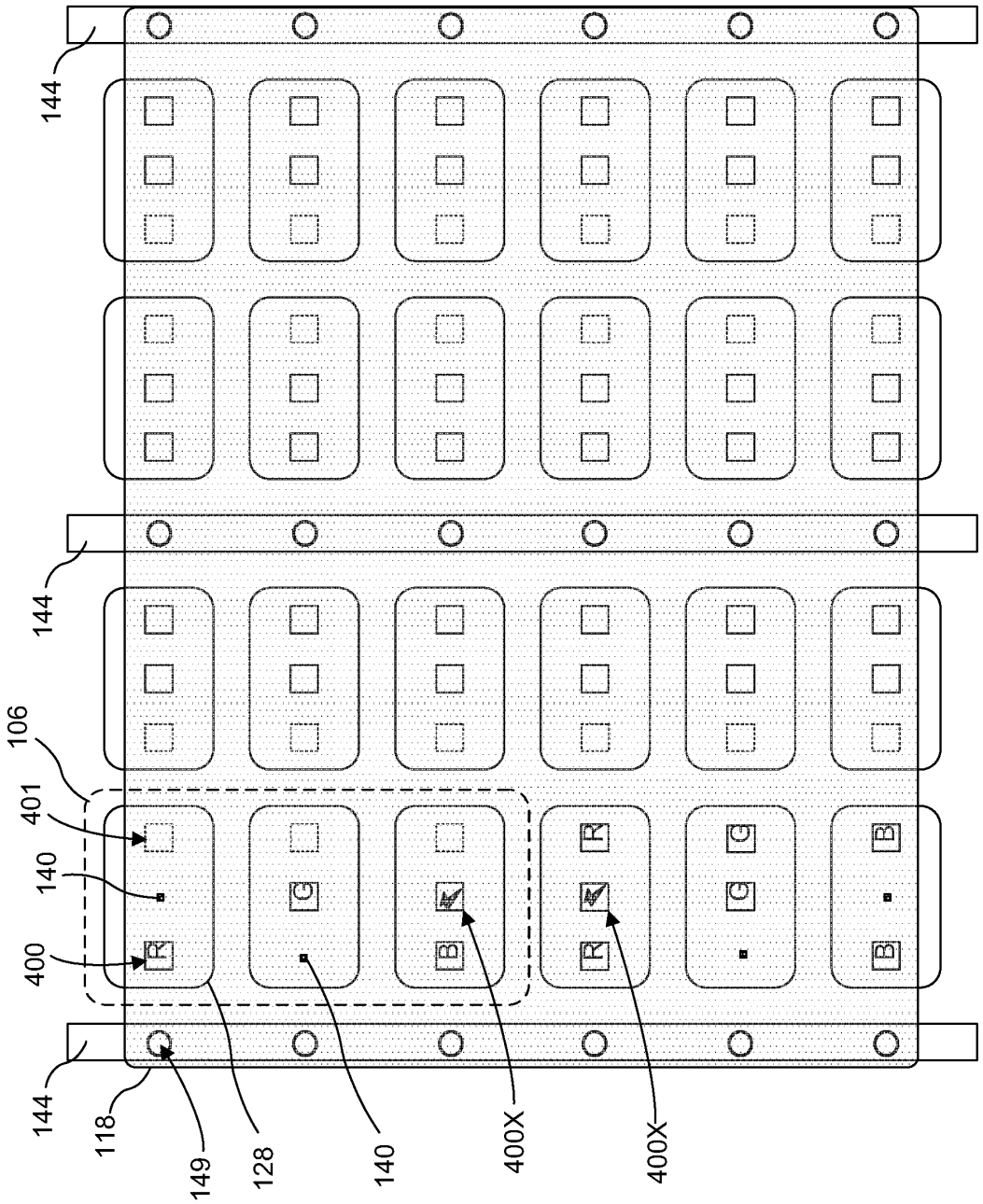

144
144
106
401
140
400
144
118
149
128
140
400X
400X
R
G
B
R
G
B
R
G
B

FIG. 13

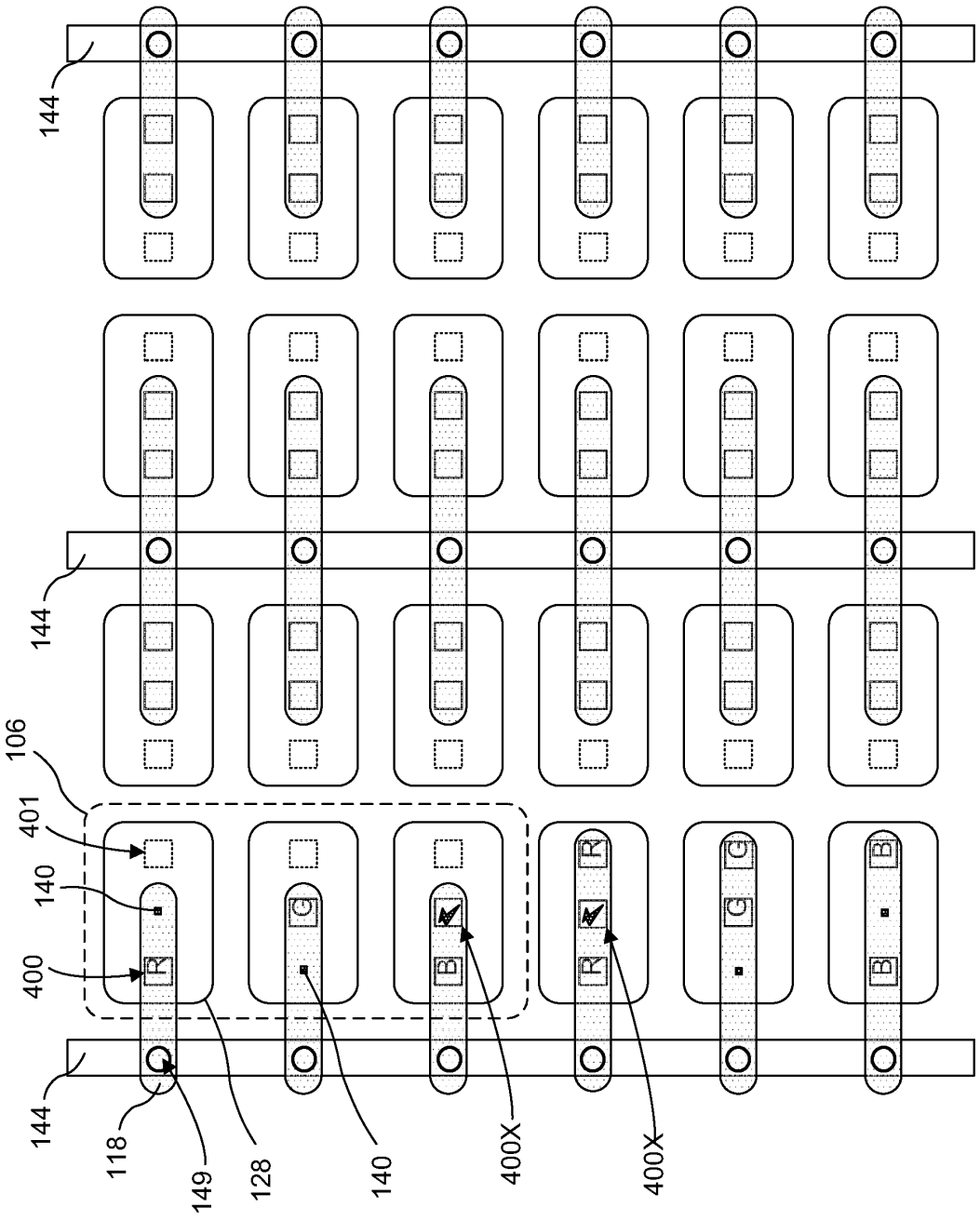


FIG. 14

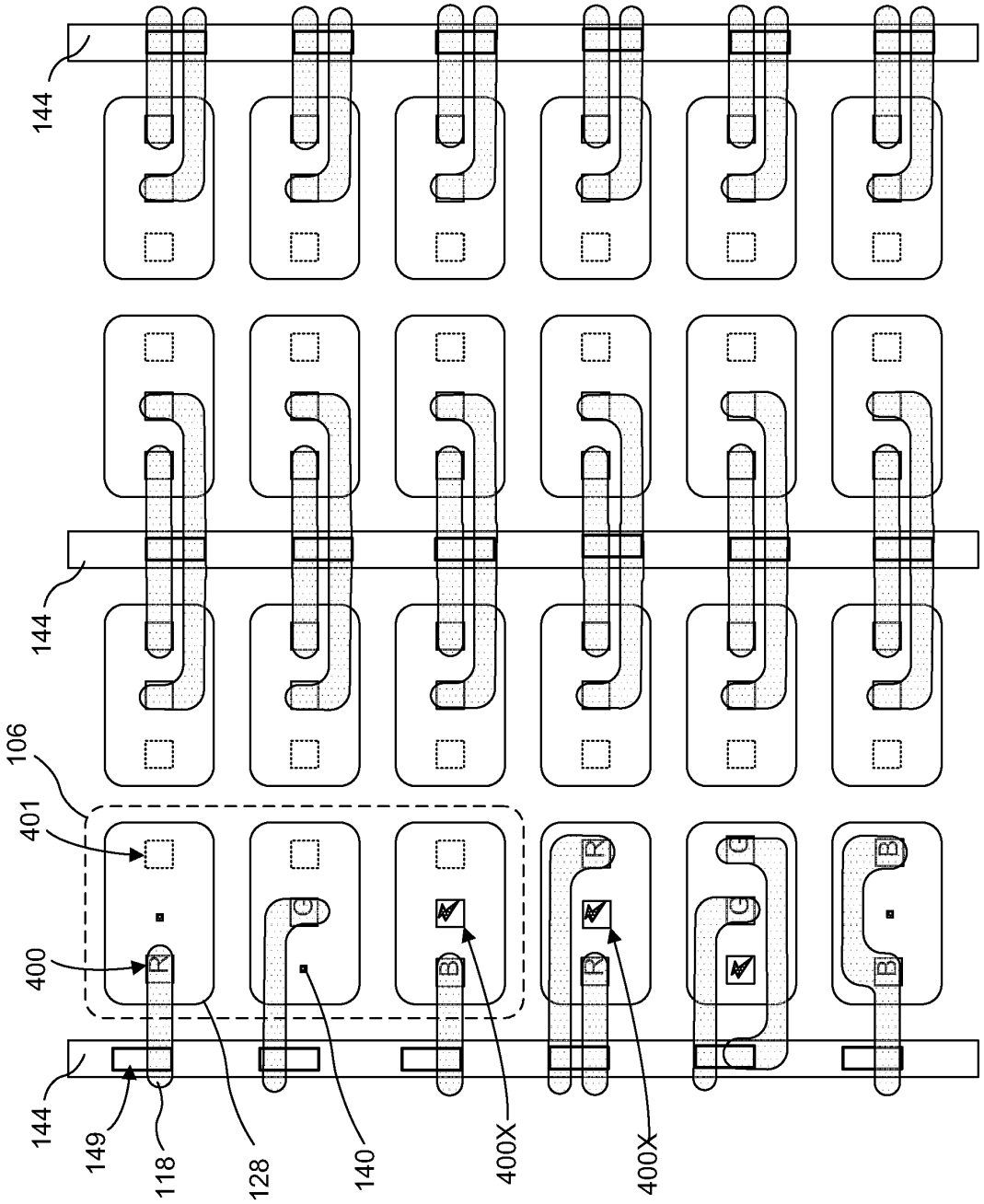


FIG. 15

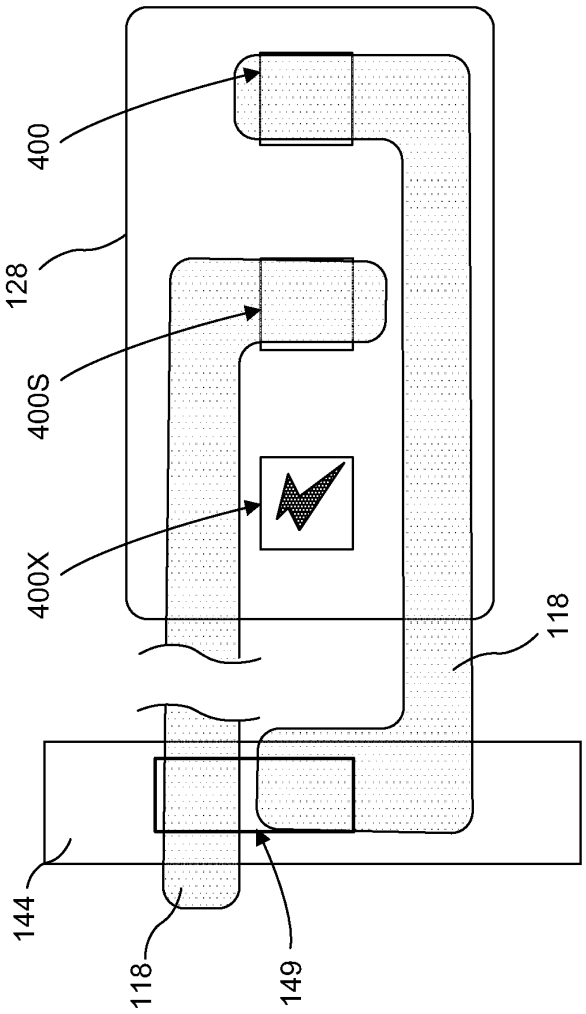


FIG. 16

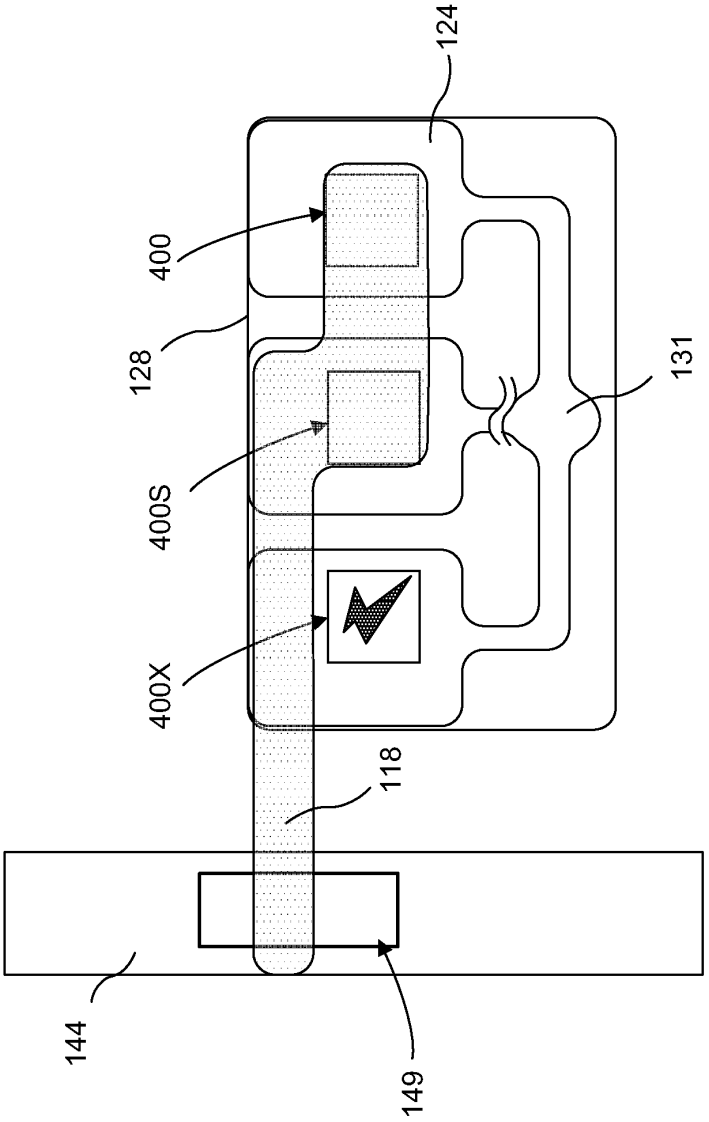


FIG. 17

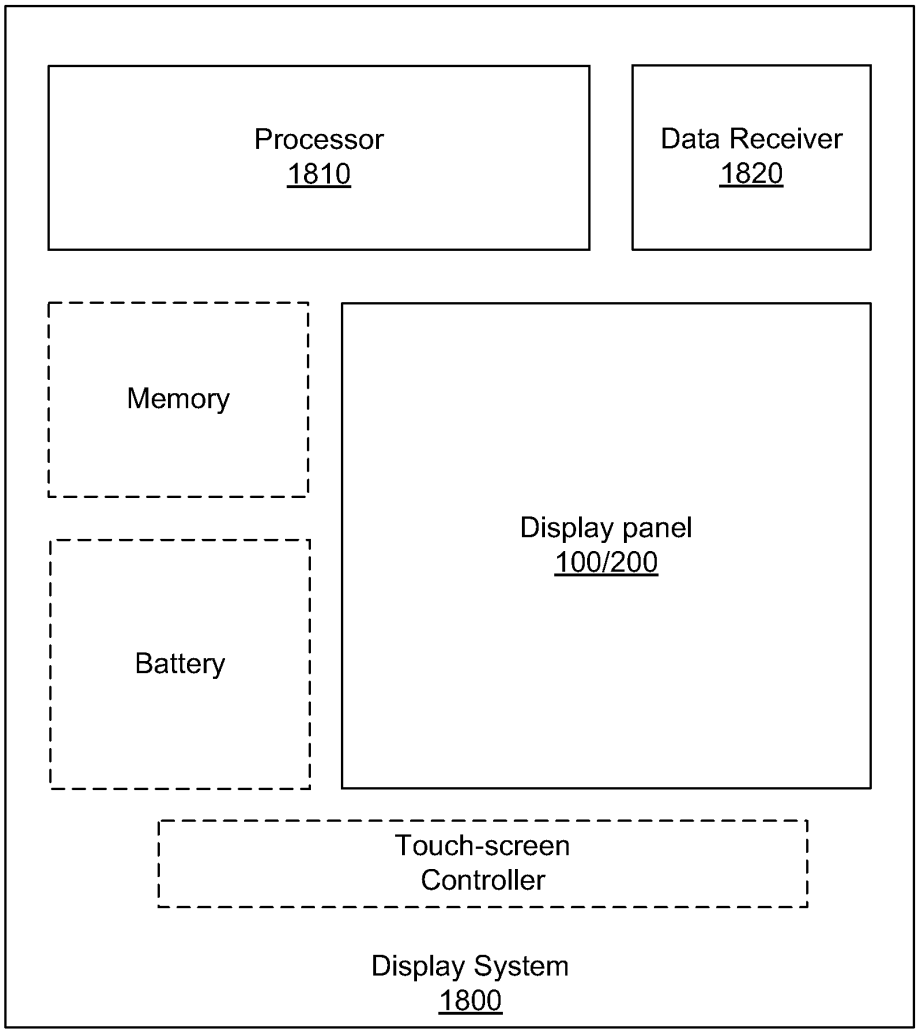

Processor
1810
Data Receiver
1820
Memory
Display panel
100/200
Battery
Touch-screen
Controller
Display System
1800

FIG. 18

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)		
☒ Declaration Submitted With Initial Filing OR ☐ Declaration Submitted After Initial Filing (surcharge (37 CFR 1.16(f)) required)	Attorney Docket Number	9299P027
	First Named Inventor	Andreas Bibl
	COMPLETE IF KNOWN	
	Application Number	
	Filing Date	
	Art Unit	
	Examiner Name	

LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME

(Title of the Invention)

As a below named inventor, I hereby declare that:

This declaration is directed to:

☒ The attached application,

OR

☐ United States Application Number or PCT International application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the above-identified application, including the claim(s).

I am aware of the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in 37 C.F.R. 1.56, including for a continuation-in-part application, information material to patentability that became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001), and may jeopardize the validity of the application or any patent issuing thereon. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

Authorization To Permit Access To Application by Participating Office

☒ If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified patent application is filed access to the above-identified patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified patent application is filed to have access to the above-identified patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the above-identified patent application with respect to: 1) the above-identified patent application-as-filed; 2) any foreign application to which the above-identified patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the above-identified patent application; and 3) any U.S. application-as-filed from which benefit is sought in the above-identified patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

Based on Forms PTO/AIA/08 and PTO/AIA/10 (6-12) as modified by Blakely, Sokoloff, Taylor & Zafman LLP on 09/17/2012.

DECLARATION— Utility or Design Patent Application

Direct all correspondence to: ☒	The address associated with Customer Number:	08791	OR ☐	Correspondence address below

Name

Address
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway

City	State	Zip
Sunnyvale	California	94085-4040

Country	Telephone	Email
U.S.A.	(408) 720-8300	MAIL@BSTZ.com

WARNING:

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Legal Name of Sole or First Inventor:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)
Andreas Bibl

Inventor's Signature	Date (Optional)

Residence: City	State	Country
Los Altos	CA	US

Mailing Address
588 Harrington Ave.

City	State	Zip	Country
Los Altos	CA	94024	US

Based on Forms PTO/AIA/08 and PTO/AIA/10 (6-12) as modified by Blakely, Sokoloff, Taylor & Zafman LLP on 09/17/2012.

Legal Name of Additional Joint Inventor, if any:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)
Kapil V. Sakariya

Inventor's Signature	Date (Optional)
	3/15/2013

Residence: City	State	Country
Sunnyvale	CA	US

Mailing Address
720 Sequoia Drive

City	State	Zip	Country
Sunnyvale	CA	94086	US

Legal Name of Additional Joint Inventor, if any:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)
Charles R. Griggs

Inventor's Signature	Date (Optional)
	3/15/2013

Residence: City	State	Country
San Jose	CA	US

Mailing Address
2365 Cherrystone Dr.

City	State	Zip	Country
San Jose	CA	95128	US

Legal Name of Additional Joint Inventor, if any:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)
James Michael Perkins

Inventor's Signature	Date (Optional)
	3/15/2013

Residence: City	State	Country
Mountain View	CA	US

Mailing Address
707 Continental Cir., Apt. 612

City	State	Zip	Country
Mountain View	CA	94040	US

Based on Forms PTO/AIA/08 and PTO/AIA/10 (6-12) as modified by Blakely, Sokoloff, Taylor & Zafman LLP on 09/17/2012.

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Filer:	Jacob T. Aikin
Attorney Docket Number:	9299P027
Filed as Large Entity	

Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	390	390
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Request for Prioritized Examination	1817	1	4800	4800
Pages:				
Claims:				
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300
Processing Fee, Except for Provis. Apps	1808	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**6490**

Electronic Acknowledgement Receipt	
EFS ID:	15268491
Application Number:	13842879
International Application Number:	
Confirmation Number:	7403
Title of Invention:	LIGHT EMITTING DIODE DISPLAY WITH REDUNDANCY SCHEME
First Named Inventor/Applicant Name:	Andreas Bibl
Customer Number:	8791
Filer:	Jacob T. Aikin/Betty Scaletta
Filer Authorized By:	Jacob T. Aikin
Attorney Docket Number:	9299P027
Receipt Date:	15-MAR-2013
Filing Date:	
Time Stamp:	20:26:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$6490
RAM confirmation Number	26747
Deposit Account	022666
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	TrackOne Request	9299P027_TrackOneReq_03-15-13.pdf	188013 40c323afa67e44d434596bca9f1090fa6e98f45d	no	2
Warnings:					
Information:					
2	Application Data Sheet	9299P027_ADS_03-15-13.pdf	1433123 4df49f9fb84d110992888d8887ef5629ba0e4dc1	no	7
Warnings:					
Information:					
3		9299P027_Application_Final_03-15-13.pdf	199299 91476b303270cb1c98b4c348f81ea0d5252930d1	yes	39

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	35
Claims	36	38
Abstract	39	39

Warnings:					
Information:					
4	Drawings-only black and white line drawings	9299P027_Drawings_Final_03-15-13.pdf	3054128 30ae8e294c50128ac515a666f8159f651dae2429	no	30
Warnings:					
Information:					
5	Power of Attorney	9299P027_POA-Trans_03-15-13.pdf	67667 f7a105ab00d8cc8ab2d7cd0a747c531c1443145d	no	2
Warnings:					
Information:					
6	Oath or Declaration filed	9299P027_DEC-executed.pdf	212303 50c06e7591ad0a19aa8e2dd7b821c3d7ffcfabcc	no	3
Warnings:					

Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	40593 7bcc5db641004e75b46580c3992e5caca1e8cf34	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	5195126	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	Not yet assigned
Filing Date	Herewith
First Named Inventor	Andreas Bibl
Title	Light Emitting Diode Display with Redundancy Scheme
Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	9299P027

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jacob Aikin/	Date	March 15, 2013
Name	Jacob T. Aikin	Telephone	(408) 720-8300
Registration Number	62,787		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

☐ *Total of _____ forms are submitted.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent): **08791**

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name Registration	Number	Name Registration	Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with the Customer Number:

OR

☐ Firm or Individual Name	BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP				
Address	1279 Oakmead Parkway				
City	Sunnyvale	State	California	Zip	94085
Country	USA				
Telephone	(408) 720-8300	Email	mail@BSTZ.com		

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient *Proprietary* Interest (*e.g.,* a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	11/30/2012
Name	Sam Hedgpeth	Telephone	408-703-4233
Title and Company	Chief Financial Officer, LuxVue Technology Corporation		

NOTE: Signature - This form must be signed by the applicant or applicant's representative in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

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