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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
456-010567-US(PAR)

Total Pages in this Submission
4

09/17/01 JC996 U.S. PTO

09/954608 U.S. PTO 09/17/01 J1033

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD FOR SUB-PIXEL VALUE INTERPOLATION

and invented by:

1) **Marta KARCZEWICZ** 2) **Antti HALLAPURO**

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 99 pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

Nokia Exhibit 2004, p. 1
Amazon.com v. Nokia
IPR2024-01141

UTILITY PATENT APPLICATION TRANSMITTAL
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Total Pages in this Submission
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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☐ Formal Number of Sheets _____
   b. ☒ Informal Number of Sheets 26
4. ☐ Oath or Declaration
   a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☐ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
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Nokia Exhibit 2004, p. 2
Amazon.com v. Nokia
IPR2024-01141

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UTILITY PATENT APPLICATION TRANSMITTAL (Large Entity) *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Docket No. 456-010567-US(PAR)
	Total Pages in this Submission 4

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

17. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

Nokia Exhibit 2004, p. 3
Amazon.com v. Nokia
IPR2024-01141

UTILITY PATENT APPLICATION TRANSMITTAL
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Docket No.
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Total Pages in this Submission
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Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	47	- 20 =	27	x $18.00	$486.00
Indep. Claims	11	- 3 =	8	x $80.00	$640.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$710.00
OTHER FEE *(specify purpose)*					$0.00
				TOTAL FILING FEE	$1,836.00

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Signature

Dated: **September 17, 2001**

Geza C. Ziegler, Jr. Reg. No.: 44,004
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Nokia Exhibit 2004, p. 4
Amazon.com v. Nokia
IPR2024-01141

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **KARCZEWICZ et al.**			Docket No. **456-010567-US(PAR)**
Serial No.	Filing Date **Herewith**	Examiner	Group Art Unit

Invention:

METHOD FOR SUB-PIXEL VALUE INTERPOLATION

I hereby certify that this **New Application Transmittal, patent application and accompanying papers**
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Nokia Exhibit 2004, p. 5
Amazon.com v. Nokia
IPR2024-01141

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Express Mail No.: EL627509093US
In re Application of: KARCZEWICZ et al.
FILING DATE: Herewith ART UNIT:
TITLE: METHOD FOR SUB-PIXEL VALUE INTERPOLATION
ATTORNEY DOCKET NO.: 456-010567-US(PAR)

Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:
Please amend the above-identified, enclosed patent application as follows:

IN THE CLAIMS

PLEASE CANCEL CLAIMS 26 AND 41 WITH OUT PREJUDICE.

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Nokia Exhibit 2004, p. 6
Amazon.com v. Nokia
IPR2024-01141

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METHOD FOR SUB-PIXEL VALUE INTERPOLATION

The present invention relates to a method for sub-pixel value interpolation in the encoding and decoding of data. It relates particularly, but not exclusively, to encoding and decoding of digital video.

Background of the invention

Digital video sequences, like ordinary motion pictures recorded on film, comprise a sequence of still images, the illusion of motion being created by displaying the images one after the other at a relatively fast frame rate, typically 15 to 30 frames per second. Because of the relatively fast frame rate, images in consecutive frames tend to be quite similar and thus contain a considerable amount of redundant information. For example, a typical scene may comprise some stationary elements, such as background scenery, and some moving areas, which may take many different forms, for example the face of a newsreader, moving traffic and so on. Alternatively, the camera recording the scene may itself be moving, in which case all elements of the image have the same kind of motion. In many cases, this means that the overall change between one video frame and the next is rather small. Of course, this depends on the nature of the movement. For example, the faster the movement, the greater the change from one frame to the next. Similarly, if a scene contains a number of moving elements, the change from one frame to the next is likely to be greater than in a scene where only one element is moving.

It should be appreciated that each frame of a raw, that is uncompressed, digital video sequence comprises a very large amount of image information. Each frame of an uncompressed digital video sequence is formed from an array of image pixels. For example, in a commonly used digital video format, known as the Quarter Common Interchange Format (QCIF), a frame

Nokia Exhibit 2004, p. 7
Amazon.com v. Nokia
IPR2024-01141

comprises an array of 176 x 144 pixels, in which case each frame has 25,344 pixels. In turn, each pixel is represented by a certain number of bits, which carry information about the luminance and/or colour content of the region of the image corresponding to the pixel. Commonly, a so-called YUV colour model is used to represent the luminance and chrominance content of the image. The luminance, or Y, component represents the intensity (brightness) of the image, while the colour content of the image is represented by two chrominance components, labelled U and V.

Colour models based on a luminance/chrominance representation of image content provide certain advantages compared with colour models that are based on a representation involving primary colours (that is Red, Green and Blue, RGB). The human visual system is more sensitive to intensity variations than it is to colour variations; YUV colour models exploit this property by using a lower spatial resolution for the chrominance components (U, V) than for the luminance component (Y). In this way the amount of information needed to code the colour information in an image can be reduced with an acceptable reduction in image quality.

The lower spatial resolution of the chrominance components is usually attained by sub-sampling. Typically, a block of 16x16 image pixels is represented by one block of 16x16 pixels comprising luminance information and the corresponding chrominance components are each represented by one block of 8x8 pixels representing an area of the image equivalent to that of the 16x16 pixels of the luminance component. The chrominance components are thus spatially sub-sampled by a factor of 2 in the *x* and *y* directions. The resulting assembly of one 16x16 pixel luminance block and two 8x8 pixel chrominance blocks is commonly referred to as a YUV macroblock, or macroblock, for short.

Nokia Exhibit 2004, p. 8
Amazon.com v. Nokia
IPR2024-01141

A QCIF image comprises 11x9 macroblocks. If the luminance blocks and chrominance blocks are represented with 8 bit resolution (that is by numbers in the range 0 to 255), the total number of bits required per macroblock is (16x16x8)+2x(8x8x8) = 3072 bits. The number of bits needed to represent a video frame in QCIF format is thus 99x3072 = 304,128 bits. This means that the amount of data required to transmit/record/display a video sequence in QCIF format, represented using a YUV colour model, at a rate of 30 frames per second, is more than 9 Mbps (million bits per second). This is an extremely high data rate and is impractical for use in video recording, transmission and display applications because of the very large storage capacity, transmission channel capacity and hardware performance required.

If video data is to be transmitted in real-time over a fixed line network such as an ISDN (Integrated Services Digital Network) or a conventional PSTN (Public Service Telephone Network), the available data transmission bandwidth is typically of the order of 64kbits/s. In mobile videotelephony, where transmission takes place at least in part over a radio communications link, the available bandwidth can be as low as 20kbits/s. This means that a significant reduction in the amount of information used to represent video data must be achieved in order to enable transmission of digital video sequences over low bandwidth communication networks. For this reason video compression techniques have been developed which reduce the amount of information transmitted while retaining an acceptable image quality.

Video compression methods are based on reducing the redundant and perceptually irrelevant parts of video sequences. The redundancy in video sequences can be categorised into spatial, temporal and spectral redundancy. 'Spatial redundancy' is the term used to describe the correlation between neighbouring pixels within a frame. The term 'temporal

Nokia Exhibit 2004, p. 9
Amazon.com v. Nokia
IPR2024-01141

redundancy' expresses the fact that the objects appearing in one frame of a sequence are likely to appear in subsequent frames, while 'spectral redundancy' refers to the correlation between different colour components of the same image.

Sufficiently efficient compression cannot usually be achieved by simply reducing the various forms of redundancy in a given sequence of images. Thus, most current video encoders also reduce the quality of those parts of the video sequence which are subjectively the least important. In addition, the redundancy of the compressed video bit-stream is itself reduced by means of efficient loss-less encoding. Typically, this is achieved using a technique known as 'variable length coding' (VLC).

Modern video compression standards, such as ITU-T recommendations H.261, H.263(+)(++), H.26L and the Motion Picture Experts Group recommendation MPEG-4 make use of 'motion compensated temporal prediction'. This is a form of temporal redundancy reduction in which the content of some (often many) frames in a video sequence is 'predicted' from other frames in the sequence by tracing the motion of objects or regions of an image between frames.

Compressed images which do not make use of temporal redundancy reduction are usually called INTRA-coded or I-frames, whereas temporally predicted images are called INTER-coded or P-frames. In the case of INTER frames, the predicted (motion-compensated) image is rarely precise enough to represent the image content with sufficient quality, and therefore a spatially compressed prediction error (PE) frame is also associated with each INTER frame. Many video compression schemes can also make use of bi-directionally predicted frames, which are commonly referred to as B-pictures or B-frames. B-pictures are inserted between reference or so-called 'anchor' picture pairs (I or P frames) and are predicted from either one of

Nokia Exhibit 2004, p. 10
Amazon.com v. Nokia
IPR2024-01141

both of the anchor pictures. B-pictures are not themselves used as anchor pictures, that is no other frames are predicted from them, and therefore, they can be discarded from the video sequence without causing deterioration in the quality of future pictures.

The different types of frame that occur in a typical compressed video sequence are illustrated in Figure 3 of the accompanying drawings. As can be seen from the figure, the sequence starts with an INTRA or I frame 30. In Figure 3, arrows 33 denote the 'forward' prediction process by which P-frames (labelled 34) are formed. The bi-directional prediction process by which B-frames (36) are formed is denoted by arrows 31a and 31b, respectively.

A schematic diagram of an example video coding system using motion compensated prediction is shown in Figures 1 and 2. Figure 1 illustrates an encoder 10 employing motion compensation and Figure 2 illustrates a corresponding decoder 20. The encoder 10 shown in Figure 1 comprises a Motion Field Estimation block 11, a Motion Field Coding block 12, a Motion Compensated Prediction block 13, a Prediction Error Coding block 14, a Prediction Error Decoding block 15, a Multiplexing block 16, a Frame Memory 17, and an adder 19. The decoder 20 comprises a Motion Compensated Prediction block 21, a Prediction Error Decoding block 22, a Demultiplexing block 23 and a Frame Memory 24.

The operating principle of video coders using motion compensation is to minimise the amount of information in a prediction error frame $E_n(x,y)$, which is the difference between a current frame $I_n(x,y)$ being coded and a prediction frame $P_n(x,y)$. The prediction error frame is thus:

$$E_n(x,y) = I_n(x,y) - P_n(x,y). \quad (1)$$

Nokia Exhibit 2004, p. 11
Amazon.com v. Nokia
IPR2024-01141

The prediction frame $P_n(x,y)$ is built using pixel values of a reference frame $R_n(x,y)$, which is generally one of the previously coded and transmitted frames, for example the frame immediately preceding the current frame and is available from the Frame Memory 17 of the encoder 10. More specifically, the prediction frame $P_n(x,y)$ is constructed by finding so-called 'prediction pixels' in the reference frame $R_n(x,y)$ which correspond substantially with pixels in the current frame. Motion information, describing the relationship (e.g. relative location, rotation, scale etc.) between pixels in the current frame and their corresponding prediction pixels in the reference frame is derived and the prediction frame is constructed by moving the prediction pixels according to the motion information. In this way, the prediction frame is constructed as an approximate representation of the current frame, using pixel values in the reference frame. The prediction error frame referred to above therefore represents the difference between the approximate representation of the current frame provided by the prediction frame and the current frame itself. The basic advantage provided by video encoders that use motion compensated prediction arises from the fact that a comparatively compact description of the current frame can be obtained by representing it in terms of the motion information required to form its prediction together with the associated prediction error information in the prediction error frame.

However, due to the very large number of pixels in a frame, it is generally not efficient to transmit separate motion information for each pixel to the decoder. Instead, in most video coding schemes, the current frame is divided into larger image segments S_k and motion information relating to the segments is transmitted to the decoder. For example, motion information is typically provided for each macroblock of a frame and the same motion information is then used for all pixels within the macroblock. In some video coding standards, such as H.26L, a macroblock can be divided into smaller blocks, each smaller block being provided with its own motion information.

Nokia Exhibit 2004, p. 12
Amazon.com v. Nokia
IPR2024-01141

The motion information usually takes the form of motion vectors $[\Delta x(x,y), \Delta y(x,y)]$. The pair of numbers $\Delta x(x,y)$ and $\Delta y(x,y)$ represents the horizontal and vertical displacements of a pixel at location (x,y) in the current frame $I_n(x,y)$ with respect to a pixel in the reference frame $R_n(x,y)$. The motion vectors $[\Delta x(x,y), \Delta y(x,y)]$ are calculated in the Motion Field Estimation block 11 and the set of motion vectors of the current frame $[\Delta x(\cdot), \Delta y(\cdot)]$ is referred to as the motion vector field.

Typically, the location of a macroblock in a current video frame is specified by the (x,y) co-ordinate of its upper left-hand corner. Thus, in a video coding scheme in which motion information is associated with each macroblock of a frame, each motion vector describes the horizontal and vertical displacement $\Delta x(x,y)$ and $\Delta y(x,y)$ of a pixel representing the upper left-hand corner of a macroblock in the current frame $I_n(x,y)$ with respect to a pixel in the upper left-hand corner of a substantially corresponding block of prediction pixels in the reference frame $R_n(x,y)$ (as shown in Figure 4b).

Motion estimation is a computationally intensive task. Given a reference frame $R_n(x,y)$ and, for example, a square macroblock comprising N x N pixels in a current frame (as shown in Figure 4a), the objective of motion estimation is to find an N x N pixel block in the reference frame that matches the characteristics of the macroblock in the current picture according to some criterion. This criterion can be, for example, a sum of absolute differences (SAD) between the pixels of the macroblock in the current frame and the block of pixels in the reference frame with which it is compared. This process is known generally as 'block matching'. It should be noted that, in general, the geometry of the block to be matched and that in the reference frame do not have to be the same, as real-world objects can undergo scale changes, as well as rotation and warping. However,

Nokia Exhibit 2004, p. 13
Amazon.com v. Nokia
IPR2024-01141

current international video coding standards, only a translational motion model is used (see below) and thus fixed rectangular geometry is sufficient.

Ideally, in order to achieve the best chance of finding a match, the whole of the reference frame should be searched. However, this is impractical as it imposes too high a computational burden on the video encoder. Instead, the search region is restricted to region $[-p, p]$ around the original location of the macroblock in the current frame, as shown in Figure 4c.

In order to reduce the amount of motion information to be transmitted from the encoder 10 to the decoder 20, the motion vector field is coded in the Motion Field Coding block 12 of the encoder 10, by representing it with a motion model. In this process, the motion vectors of image segments are re-expressed using certain predetermined functions or, in other words, the motion vector field is represented with a model. Almost all currently used motion vector field models are additive motion models, complying with the following general formula:

$$\Delta x(x,y) = \sum_{i=0}^{N-1} a_i f_i(x,y) \tag{2}$$

$$\Delta y(x,y) = \sum_{i=0}^{M-1} b_i g_i(x,y) \tag{3}$$

where coefficients a_i and b_i are called motion coefficients. The motion coefficients are transmitted to the decoder 20 (information stream 2 in Figures 1 and 2). Functions f_i and g_i are called motion field basis functions, and are known both to the encoder and decoder. An approximate motion vector field $(\tilde{\Delta}x(x,y), \tilde{\Delta}y(x,y))$ can be constructed using the coefficients and the basis functions. As the basis functions are known to (that is stored in) both the encoder 10 and the decoder 20, only the motion

Nokia Exhibit 2004, p. 14
Amazon.com v. Nokia
IPR2024-01141

coefficients need to be transmitted to the encoder, thus reducing the amount of information required to represent the motion information of the frame.

The simplest motion model is the translational motion model which requires only two coefficients to describe the motion vectors of each segment. The values of motion vectors are given by:

$$\Delta x(x,y) = a_0$$
$$\Delta y(x,y) = b_0 \qquad (4)$$

This model is widely used in various international standards (ISO MPEG-1, MPEG-2, MPEG-4, ITU-T Recommendations H.261 and H.263) to describe the motion of 16x16 and 8x8 pixel blocks. Systems which use a translational motion model typically perform motion estimation at full pixel resolution or some integer fraction of full pixel resolution, for example at half or one quarter pixel resolution.

The prediction frame $P_n(x,y)$ is constructed in the Motion Compensated Prediction block 13 in the encoder 10, and is given by:

$$P_n(x,y) = R_n\left[x + \tilde{\Delta}x(x,y), y + \tilde{\Delta}y(x,y)\right] \qquad (5)$$

In the Prediction Error Coding block 14, the prediction error frame $E_n(x,y)$ is typically compressed by representing it as a finite series (transform) of some 2-dimensional functions. For example, a 2-dimensional Discrete Cosine Transform (DCT) can be used. The transform coefficients are quantised and entropy (for example Huffman) coded before they are transmitted to the decoder (information stream 1 in Figures 1 and 2). Because of the error introduced by quantisation, this operation usually produces some degradation (loss of information) in the prediction error frame $E_n(x,y)$. To

Nokia Exhibit 2004, p. 15
Amazon.com v. Nokia
IPR2024-01141

compensate for this degradation, the encoder 10 also comprises a Prediction Error Decoding block 15, where a decoded prediction error frame $\tilde{E}_n(x,y)$ is constructed using the transform coefficients. This locally decoded prediction error frame is added to the prediction frame $P_n(x,y)$ in the adder 19 and the resulting decoded current frame $\tilde{I}_n(x,y)$ is stored in the Frame Memory 17 for further use as the next reference frame $R_{n+1}(x,y)$.

The information stream 2 carrying information about the motion vectors is combined with information about the prediction error in multiplexer 16 and an information stream 3 containing typically at least those two types of information is sent to the decoder 20.

The operation of a corresponding video decoder 20 will now be described.

The Frame Memory 24 of the decoder 20 stores a previously reconstructed reference frame $R_n(x,y)$. The prediction frame $P_n(x,y)$ is constructed in the Motion Compensated Prediction block 21 of the decoder 20 according to equation 5, using received motion coefficient information and pixel values of the previously reconstructed reference frame $R_n(x,y)$. The transmitted transform coefficients of the prediction error frame $E_n(x,y)$ are used in the Prediction Error Decoding block 22 to construct the decoded prediction error frame $\tilde{E}_n(x,y)$. The pixels of the decoded current frame $\tilde{I}_n(x,y)$ are then reconstructed by adding the prediction frame $P_n(x,y)$ and the decoded prediction error frame $\tilde{E}_n(x,y)$:

$$\tilde{I}_n(x,y) = P_n(x,y) + \tilde{E}_n(x,y) = R_n\left[x + \tilde{\Delta}x(x,y), y + \tilde{\Delta}y(x,y)\right] + \tilde{E}_n(x,y). \qquad (6)$$

This decoded current frame may be stored in the Frame Memory 24 as the next reference frame $R_{n+1}(x,y)$.

Nokia Exhibit 2004, p. 16
Amazon.com v. Nokia
IPR2024-01141

In the description of motion compensated encoding and decoding of digital video presented above, the motion vector $[\Delta x(x,y), \Delta y(x,y)]$ describing the motion of a macroblock in the current frame with respect to the reference frame $R_n(x,y)$ can point to any of the pixels in the reference frame. This means that motion between frames of a digital video sequence can only be represented at a resolution which is determined by the image pixels in the frame (so-called full pixel resolution). Real motion, however, has arbitrary precision, and thus the system described above can only provide approximate modelling of the motion between successive frames of a digital video sequence. Typically, modelling of motion between video frames with full pixel resolution is not sufficiently accurate to allow efficient minimisation of the prediction error (PE) information associated with each macroblock/frame. Therefore, to enable more accurate modelling of real motion and to help reduce the amount of PE information that must be transmitted from encoder to decoder, many video coding standards, such as H.263(+)(++) and H.26L, allow motion vectors to point 'in between' image pixels. In other words, the motion vectors can have 'sub-pixel' resolution. Allowing motion vectors to have sub-pixel resolution adds to the complexity of the encoding and decoding operations that must be performed, so it is still advantageous to limit the degree of spatial resolution a motion vector may have. Thus, video coding standards, such as those previously mentioned, typically only allow motion vectors to have full-, half- or quarter-pixel resolution.

Motion estimation with sub-pixel resolution is usually performed as a two-stage process, as illustrated in Figure 5, for a video coding scheme which allows motion vectors to have full- or half-pixel resolution. In the first step, a motion vector having full-pixel resolution is determined using any appropriate motion estimation scheme, such as the block-matching process

Nokia Exhibit 2004, p. 17
Amazon.com v. Nokia
IPR2024-01141

described in the foregoing. The resulting motion vector, having full-pixel resolution is shown in Figure 5.

In the second stage, the motion vector determined in the first stage is refined to obtain the desired half-pixel resolution. In the example illustrated in Figure 5, this is done by forming eight new search blocks of 16 x 16 pixels, the location of the top-left corner of each block being marked with an X in Figure 5. These locations are denoted as $[\Delta x + m/2, \Delta y + n/2]$, where m and n can take the values –1, 0 and +1, but cannot be zero at the same time. As only the pixel values of original image pixels are known, the values (for example luminance and/or chrominance values) of the sub-pixels residing at half-pixel locations must be estimated for each of the eight new search blocks, using some form of interpolation scheme.

Having interpolated the values of the sub-pixels at half-pixel resolution, each of the eight search blocks is compared with the macroblock whose motion vector is being sought. As in the block matching process performed in order to determine the motion vector with full pixel resolution, the macroblock is compared with each of the eight search blocks according to some criterion, for example a SAD. As a result of the comparisons, a minimum SAD value will generally be obtained. Depending on the nature of the motion in the video sequence, this minimum value may correspond to the location specified by the original motion vector (having full-pixel resolution), or it may correspond to a location having a half-pixel resolution. Thus, it is possible to determine whether a motion vector should point to a full-pixel or sub-pixel location and if sub-pixel resolution is appropriate, to determine the correct sub-pixel resolution motion vector. It should also be appreciated that the scheme just described can be extended to other sub-pixel resolutions (for example, one-quarter-pixel resolution) in an entirely analogous fashion.

Nokia Exhibit 2004, p. 18
Amazon.com v. Nokia
IPR2024-01141

In practice, the estimation of a sub-pixel value in the reference frame is performed by interpolating the value of the sub-pixel from surrounding pixel values. In general, interpolation of a sub-pixel value *F(x,y)* situated at a non-integer location $(x, y) = (n+\Delta x, m+\Delta y)$, can be formulated as a two-dimensional operation, represented mathematically as:

$$F(x,y) = \sum_{k=-K}^{K=1} \sum_{l=-L}^{L=1} f(k+K, l+L) F(n+k, m+l) \quad (7)$$

where *f(k,l)* are filter coefficients and *n* and *m* are obtained by truncating *x* and *y*, respectively, to integer values. Typically, the filter coefficients are dependent on the *x* and *y* values and the interpolation filters are usually so-called 'separable filters', in which case sub-pixel value *F(x,y)* can be calculated as follows:

$$F(x,y) = \sum_{k=-K}^{K=1} f(k+K) \sum_{l=-K}^{K=1} f(l+K) F(n+k, m+l) \quad (8)$$

The motion vectors are calculated in the encoder. Once the corresponding motion coefficients are transmitted to the decoder, it is a straightforward matter to interpolate the required sub-pixels using an interpolation method identical to that used in the encoder. In this way, a frame following a reference frame in the Frame Memory 24, can be reconstructed from the reference frame and the motion vectors.

The simplest way of applying sub-pixel value interpolation in a video coder is to interpolate each sub-pixel value every time it is needed. However, this is not an efficient solution in a video encoder, because it is likely that the same sub-pixel value will be required several times and thus calculations to interpolate the same sub-pixel value will be performed multiple times. This

Nokia Exhibit 2004, p. 19
Amazon.com v. Nokia
IPR2024-01141

results in an unnecessary increase of computational complexity / burden in the encoder.

An alternative approach, which limits the complexity of the encoder, is to pre-calculate and store all sub-pixel values in a memory associated with the encoder. This solution is called interpolation 'before-hand' interpolation hereafter in this document. While limiting complexity, before-hand interpolation has the disadvantage of increasing memory usage by a large margin. For example, if the motion vector accuracy is one quarter pixel in both horizontal and vertical dimensions, storing pre-calculated sub-pixel values for a complete image results in a memory usage that is 16 times that required to store the original, non-interpolated image. In addition, it involves the calculation of some sub-pixels which might not actually be required in calculating motion vectors in the encoder. Before-hand interpolation is also particularly inefficient in a video decoder, as the majority of pre-calculated sub-pixel values will never be required by the decoder. Thus, it is advantageous not to use pre-calculation in the decoder.

So-called 'on-demand' interpolation can be used to reduce memory requirements in the encoder. For example, if the desired pixel precision is quarter pixel resolution, only sub-pixels at one half unit resolution are interpolated before-hand for the whole frame and stored in the memory. Values of one-quarter pixel resolution sub-pixels are only calculated during the motion estimation / compensation process as and when it is required. In this case memory usage is only 4 times that required to store the original, non-interpolated image.

It should be noted that when before-hand interpolation is used, the interpolation process constitutes only a small fraction of the total encoder computational complexity / burden, since every pixel is interpolated just once. Therefore, in the encoder, the complexity of the interpolation process itself is not very critical when before-hand sub-pixel value interpolation is

Nokia Exhibit 2004, p. 20
Amazon.com v. Nokia
IPR2024-01141

used. On the other hand, on-demand interpolation poses a much higher computational burden on the encoder, since sub-pixels may be interpolated many times. Hence the complexity of interpolation process, which may be considered in terms of the number of computational operations or operational cycles that must be performed in order to interpolate the sub-pixel values, becomes an important consideration.

In the decoder, the same sub-pixel values are used a few times at most and some are not needed at all. Therefore, in the decoder it is advantageous not to use before-hand interpolation at all, that is, it is advantageous not to pre-calculate any sub-pixel values.

Two interpolation schemes have been developed as part of the work ongoing in the ITU-Telecommunications Standardization Sector, Study Group 16, Video Coding Experts Group (VCEG), Questions 6 and 15. These approaches were proposed for incorporation into ITU-T recommendation H.26L and have been implemented in test models (TML) for the purposes of evaluation and further development. The test model corresponding to Question 15 is referred to as Test Model 5 (TML5), while that resulting from Question 6 is known as Test Model 6 (TML6). The interpolation schemes proposed in both TML5 and TML6 will now be described.

Throughout the description of the sub-pixel value interpolation scheme used in test model TML5, reference will be made to Figure 12a, which defines a notation for describing pixel and sub-pixel locations specific to TML5. A separate notation, defined in Figure 13a, will be used in the discussion of the sub-pixel value interpolation scheme used in TML6. A still further notation, illustrated in Figure 14a, will be used later in the text in connection with the sub-pixel value interpolation method according to the invention. It should be appreciated that the three different notations used in the text are

Nokia Exhibit 2004, p. 21
Amazon.com v. Nokia
IPR2024-01141

intended to assist in the understanding of each interpolation method and to help distinguish differences between them. However, in all three figures, the letter A is used to denote original image pixels (full pixel resolution). More specifically, the letter A represents the location of pixels in the image data representing a frame of a video sequence, the pixel values of pixels A being either received as current frame $I_n(x,y)$ from a video source, or reconstructed and stored as a reference frame $R_n(x,y)$ in the Frame Memory 17, 24 of the encoder 10 or the decoder 20. All other letters represent sub-pixel locations, the values of the sub-pixels situated at the sub-pixel locations being obtained by interpolation.

Certain other terms will also be used in a consistent manner throughout the text to identify particular pixel and sub-pixel locations. These are as follows:

The term 'unit horizontal location' is used to describe the location of any sub-pixel that is constructed in a column of the original image data. Sub-pixels c and e in Figures 12a and 13a, as well as sub-pixels b and e in Figure 14a have unit horizontal locations.

The term 'unit vertical location' is used to describe any sub-pixel that is constructed in a row of the original image data. Sub-pixels b and d in Figures 12a and 13a as well as sub-pixels b and d in Figure 14a have unit vertical locations.

By definition, pixels A have unit horizontal and unit vertical locations.

The term 'half horizontal location' is used to describe the location of any sub-pixel that is constructed in a column that lies at half pixel resolution. Sub-pixels b, c, and e shown in Figures 12a and 13a fall into this category, as do sub-pixels b, c and f in Figure 14a. In a similar manner, the term 'half vertical location' is used to describe the location of any sub-pixel that lies

Nokia Exhibit 2004, p. 22
Amazon.com v. Nokia
IPR2024-01141

constructed in a row that lies at half-pixel resolution, such as sub-pixels c and d in Figures 12a and 13a, as well as sub-pixels b, c and g in Figure 14a.

Furthermore, the term 'quarter horizontal location' refers to any sub-pixel that is constructed in a column which lies at quarter-pixel resolution, such as sub-pixels d and e in Figure 12a, sub-pixels d and g in Figure 13a and sub-pixels d, g and h in Figure 14a. Analogously, the term 'quarter vertical location' refers to sub-pixels that are constructed in a row which lies at quarter-pixel resolution. In Figure 12a, sub-pixels e and f fall into this category, as do sub-pixels e, f and g in Figure 13a and sub-pixels e, f and h in Figure 14a.

The definition of each of the terms described above is shown by 'envelopes' drawn on the corresponding figures.

It should further be noted that it is often convenient to denote a particular pixel with a two-dimensional reference. In this case, the appropriate two-dimensional reference can be obtained by examining the intersection of the envelopes in Figures 12a, 13a and 14a. Applying this principle, pixel d in Figure 12a, for example, has a half horizontal and half vertical location and sub-pixel e has a unit horizontal and quarter vertical location. In addition, and for ease of reference, sub-pixels that reside at half unit horizontal and unit vertical locations, unit horizontal and half unit vertical locations as well as half unit horizontal and half unit vertical locations, will be referred to as ½ resolution sub-pixels. Sub-pixels which reside at any quarter unit horizontal and / or quarter unit vertical location will be referred to as ¼ resolution sub-pixels.

It should also be noted that in the descriptions of the two test models and in the detailed description of the invention itself, it will be assumed that pixels

Nokia Exhibit 2004, p. 23
Amazon.com v. Nokia
IPR2024-01141

have a minimum value of 0 and a maximum value of 2^n-1 where n is the number of bits reserved for a pixel value. The number of bits is typically 8. After a sub-pixel has been interpolated, if the value of that interpolated sub-pixel exceeds the value of 2^n-1, it is restricted to the range of $[0, 2^n-1]$, i.e. values lower than the minimum allowed value will become the minimum value (*0*) and values larger than the maximum will the become maximum value (2^n-1). This operation is called clipping.

The sub-pixel value interpolation scheme according to TML5 will now be described in detail with reference to Figures 12a, 12b and 12c.

1. The value for the sub-pixel at half unit horizontal and unit vertical location, that is ½ resolution sub-pixel b in Figure 12a, is calculated using a 6-tap filter. The filter interpolates a value for ½ resolution sub-pixel b based upon the values of the 6 pixels (A_1 to A_6) situated in a row at unit horizontal locations and unit vertical locations symmetrically about b, as shown in Figure 12b, according to the formula $b = (A_1 - 5A_2 + 20A_3 + 20A_4 - 5A_5 + A_6 + 16) / 32$. The operator / denotes division with truncation. The result is clipped to lie in the range $[0, 2^n-1]$.

2. Values for the ½ resolution sub-pixels labelled c are calculated using the same six tap filter as used in step 1 and the six nearest pixels or sub-pixels (A or b) in the vertical direction. Referring now to Figure 12c, the filter interpolates a value for the ½ resolution sub-pixel c located at unit horizontal and half vertical location based upon the values of the 6 pixels (A_1 to A_6) situated in a column at unit horizontal locations and unit vertical locations symmetrically about c, according to the formula $c = (A_1 - 5A_2 + 20A_3 + 20A_4 - 5A_5 + A_6 + 16) / 32$. Similarly, a value for the ½ resolution sub-pixel c at half horizontal and half vertical location is calculated according to $c = (b_1 - 5b_2 + 20b_3 + 20b_4 - 5b_5 + b_6 + 16) / 32$. Again, the operator / denotes division with truncation. The values

Nokia Exhibit 2004, p. 24
Amazon.com v. Nokia
IPR2024-01141

calculated for the c sub-pixels are further clipped to lie in the range [0, 2^n-1].

At this point in the interpolation process the values of all ½ resolution sub-pixels have been calculated and the process proceeds to the calculation of ¼ resolution sub-pixel values.

3. Values for the ¼ resolution sub-pixels labelled d are calculated using linear interpolation and the values of the nearest pixels and / or ½ resolution sub-pixels in the horizontal direction. More specifically, values for ¼ resolution sub-pixels d located at quarter horizontal and unit vertical locations, are calculated by taking the average of the immediately neighbouring pixel at unit horizontal and unit vertical location (pixel A) and the immediately neighbouring ½ resolution sub-pixel at half horizontal and unit vertical location (sub-pixel b), i.e. according to d = (A + b) / 2. Values for ¼ resolution sub-pixels d located at quarter horizontal and half vertical locations, are calculated by taking the average of the immediately neighbouring ½ resolution sub-pixels c which lie at unit horizontal and half vertical location and half horizontal and half vertical locations respectively, i.e. according to d = $(c_1 + c_2)/2$. Again operator / indicates division with truncation.

4. Values for the ¼ resolution sub-pixels labelled e are calculated using linear interpolation and the values of the nearest pixels and / or ½ resolution sub-pixels in the vertical direction. In particular, ¼ resolution sub-pixels e at unit horizontal and quarter vertical locations are calculated by taking the average of the immediately neighbouring pixel at unit horizontal and unit vertical location (pixel A) and the immediately neighbouring sub-pixel at unit horizontal and half vertical location (sub-pixel c) according to e = (A + c) / 2. ¼ resolution sub-pixels e_3 at half horizontal and quarter vertical locations are calculated by taking the

Nokia Exhibit 2004, p. 25
Amazon.com v. Nokia
IPR2024-01141

average of the immediately neighbouring sub-pixel at half horizontal and unit vertical location (sub-pixel b) and the immediately neighbouring sub-pixel at half horizontal and half vertical location (sub-pixel c), according to e = (b + c) / 2. Furthermore, ¼ resolution sub-pixels e at quarter horizontal and quarter vertical locations are calculated by taking the average of the immediately neighbouring sub-pixels at quarter horizontal and unit vertical location and the corresponding sub-pixel at quarter horizontal and half vertical location (sub-pixels d), according to $e = (d_1 + d_2) / 2$. Once more, operator / indicates division with truncation.

5. The value for ¼ resolution sub-pixel f is interpolated by averaging the values of the 4 closest pixels values at unit horizontal and vertical locations, according to $f = (A_1 + A_2 + A_3 + A_4 + 2) / 4$, where pixels A_1, A_2, A_3 and A_4 are the four nearest original pixels.

A disadvantage of TML5 is that the decoder is computationally complex. This results from the fact that TML5 uses an approach in which interpolation of ¼ resolution sub-pixel values depends upon the interpolation of ½ resolution sub-pixel values. This means that in order to interpolate the values of the ¼ resolution sub-pixels, the values of the ½ resolution sub-pixels from which they are determined must be calculated first. Furthermore, since the values of some of the ¼ resolution sub-pixels depend upon the interpolated values obtained for other ¼ resolution sub-pixels, truncation of the ¼ resolution sub-pixel values has a deleterious effect on the precision of some of the ¼ resolution sub-pixel values. Specifically, the ¼ resolution sub-pixel values are less precise than they would be if calculated from values that had not been truncated and clipped. Another disadvantage of TML5 is that it is necessary to store the values of the ½ resolution sub-pixels in order to interpolate the ¼ resolution sub-pixel values. Therefore, excess memory is required to store a result which is not ultimately required.

Nokia Exhibit 2004, p. 26
Amazon.com v. Nokia
IPR2024-01141

The sub-pixel value interpolation scheme according to TML6, referred to herein as direct interpolation, will now be described. In the encoder the interpolation method according to TML6 works like the previously described TML5 interpolation method, except that maximum precision is retained throughout. This is achieved by using intermediate values which are neither rounded nor clipped. A step-by-step description of interpolation method according to TML6 as applied in the encoder is given below with reference to Figures 13a, 13b and 13c.

1. The value for the sub-pixel at half unit horizontal and unit vertical location, that is ½ resolution sub-pixel b in Figure 13a, is obtained by first calculating an intermediate value *b* using a six tap filter. The filter calculates *b* based upon the values of the 6 pixels (A_1 to A_6) situated in a row at unit horizontal locations and unit vertical locations symmetrically about b, as shown in Figure 13b, according to the formula $b = (A_1 - 5A_2 + 20A_3 + 20A_4 - 5A_5 + A_6)$. The final value of b is then calculated as $b = (b + 16) / 32$ and is clipped to lie in the range $[0, 2^n-1]$. As before, the operator / denotes division with truncation.

2. Values for the ½ resolution sub-pixels labelled c are obtained by first calculating intermediate values *c*. Referring to Figure 13c, an intermediate value *c* for the ½ resolution sub-pixel c located at unit horizontal and half vertical location is calculated based upon the values of the 6 pixels (A_1 to A_6) situated in a column at unit horizontal locations and unit vertical locations symmetrically about c, according to the formula $c = (A_1 - 5A_2 + 20A_3 + 20A_4 - 5A_5 + A_6)$. The final value for the ½ resolution sub-pixel c located at unit horizontal and half vertical location is then calculated according to $c = (c + 16) / 32$. Similarly, an intermediate value *c* for the ½ resolution sub-pixel c at half horizontal and half vertical location is calculated according to $c = (b_1 - 5b_2 + 20b_3 + 20b_4 - 5b_5 + b_6)$. A final value for this ½ resolution sub-pixel is then

Nokia Exhibit 2004, p. 27
Amazon.com v. Nokia
IPR2024-01141

calculated according to (c + 512) / 1024. Again, the operator / denotes division with truncation and the values calculated for ½ resolution sub-pixels c are further clipped to lie in the range [0, 2^n-1].

3. Values for the ¼ resolution sub-pixels labelled d are calculated as follows. Values for ¼ resolution sub-pixels d located at quarter horizontal and unit vertical locations, are calculated from the value of the immediately neighbouring pixel at unit horizontal and unit vertical location (pixel A) and the intermediate value b calculated in step (1) for the immediately neighbouring ½ resolution sub-pixel at half horizontal and unit vertical location (½ resolution sub-pixel b), according to d = (32A + b + 32) / 64. Values for ¼ resolution sub-pixels d located at quarter horizontal and half vertical locations, are interpolated using the intermediate values c calculated for the immediately neighbouring ½ resolution sub-pixels c which lie at unit horizontal and half vertical location and half horizontal and half vertical locations respectively, according to d = ($32c_1 + c_2 + 1024$) / 2048. Again operator / indicates division with truncation and the finally obtained ¼ resolution sub-pixel values d are clipped to lie in the range [0, 2^n-1].

4. Values for the ¼ resolution sub-pixels labelled e are calculated as follows. Values for ¼ resolution sub-pixels e located at unit horizontal and quarter vertical locations are calculated from the value of the immediately neighbouring pixel at unit horizontal and unit vertical location (pixel A) and the intermediate value c calculated in step (2) for the immediately neighbouring ½ resolution sub-pixel at unit horizontal and half vertical location, according to e = (32A + c + 32) / 64. Values for ¼ resolution sub-pixels e located at half horizontal and

Nokia Exhibit 2004, p. 28
Amazon.com v. Nokia
IPR2024-01141

quarter vertical locations are calculated from the intermediate value *b* calculated in step (1) for the immediately neighbouring ½ resolution sub-pixel at half horizontal and unit vertical location and the intermediate value *c* calculated in step (2) for the immediately neighbouring ½ resolution sub-pixel at half horizontal and half vertical location, according to e = (32*b* + *c* + 1024) / 2048. Once more, operator / indicates division with truncation and the finally obtained ¼ resolution sub-pixel values e are clipped to lie in the range [0, 2^n-1].

5. Values for ¼ resolution sub-pixels labelled g are computed using the value of the nearest original pixel A and the intermediate values of the three nearest neighbouring ½ resolution sub-pixels, according to g = (1024A + 32*b* + 32c_1 + c_2 + 2048) / 4096. As before, operator / indicates division with truncation and the finally obtained for ¼ resolution sub-pixel values g are clipped to lie in the range [0, 2^n-1].

6. The value for ¼ resolution sub-pixel f is interpolated by averaging the values of the 4 closest pixels at unit horizontal and vertical locations, according to f = (A_1 + A_2 + A_3 + A_4 + 2) / 4, where the locations of pixels A_1, A_2, A_3 and A_4 are the four nearest original pixels.

In the decoder, sub-pixel values can be obtained directly by applying 6-tap filters in horizontal and vertical directions. In the case of ¼ sub-pixel resolution, referring to Figure 13a, the filter coefficients applied to pixels and sub-pixels at unit vertical location are [0, 0, 64, 0, 0, 0] for a set of six pixels A, [1, -5, 52, 20, -5, 1] for a set of six sub-pixels d, [2, -10, 40, 40, -10, 2] for a set of six sub-pixels b, and [1, -5, 20, 52, -5, 1] for a set of six sub-pixels d. These filter coefficients are applied to respective sets of pixels or sub-pixels in the same row as the sub-pixel values being interpolated.

Nokia Exhibit 2004, p. 29
Amazon.com v. Nokia
IPR2024-01141

After applying the filters in the horizontal and vertical directions, interpolated value *c* is normalized according to $c = (c + 2048) / 4096$ and clipped to lie in the range $[0, 2^n-1]$. When a motion vector points to an integer pixel position in either the horizontal or vertical direction, many zero coefficients are used. In a practical implementation of TML6, different branches are used in the software which are optimised for the different sub-pixel cases so that there are no multiplications by zero coefficients.

It should be noted that in TML6, ¼ resolution sub-pixel values are obtained directly using the intermediate values referred to above and are not derived from rounded and clipped values for ½ resolution sub-pixels. Therefore, in obtaining the ¼ resolution sub-pixel values, it is not necessary to calculate final values for any of the ½ resolution sub-pixels. Specifically, it is not necessary to carry out the truncation and clipping operations associated with the calculation of final values for the ½ resolution sub-pixels. Neither is it necessary to have stored final values for ½ resolution sub-pixels for use in the calculation of the ¼ resolution sub-pixel values. Therefore TML6 is computationally less complex than TML5, as fewer truncating and clipping operations are required. However, a disadvantage of TML6 is that high precision arithmetic is required both in the encoder and in the decoder. High precision interpolation requires more silicon area in ASICs and requires more computations in some CPUs. Furthermore, implementation of direct interpolation as specified in TML6 in an on-demand fashion has a high memory requirement. This is an important factor, particularly in embedded devices.

In view of the previously presented discussion, it should be appreciated that due to the different requirements of the video encoder and decoder with regard to sub-pixel interpolation, there exists a significant problem in developing a method of sub-pixel value interpolation capable of providing satisfactory performance in both the encoder and decoder. Furthermore,

Nokia Exhibit 2004, p. 30
Amazon.com v. Nokia
IPR2024-01141

neither of the current test models (TML5, TML6) described in the foregoing can provide a solution that is optimum for application in both encoder and decoder.

Summary of the Invention

According to a first aspect of the invention there is provided method of interpolation in video coding in which an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, is interpolated to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$, where x is a positive integer having a maximum value N, the method comprising:

a) when values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations are required, interpolating such values directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) when values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations are required, interpolating such values directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) when a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location is required, interpolating such a value by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N

Nokia Exhibit 2004, p. 31
Amazon.com v. Nokia
IPR2024-01141

such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

Preferably a first and a second weight are used in the weighted average referred to in (c), the relative magnitudes of the weights being inversely proportional to the (straight-line diagonal) proximity of the first and the second sub-pixel or pixel to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

In a situation where the first and the second sub-pixel or pixel are symmetrically located with respect to (equidistant from) the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location, the first and second weights may have equal values.

The first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations in step b) may be used when a sub-pixel at $1/2^{N-1}$ unit horizontal and $1/2^N$ unit vertical location is required.

The second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations in step b) may be used when a sub-pixel at $1/2^N$ unit horizontal and $1/2^{N-1}$ unit vertical location is required.

In one embodiment, when values for sub-pixels at $1/2^N$ unit horizontal and unit vertical locations, and $1/2^N$ horizontal and $1/2^{N-1}$ vertical locations are required, such values are interpolated by taking the average of the values of a first pixel or sub-pixel located at a vertical location corresponding to that of the sub-pixel being calculated and unit horizontal location and a second pixel or sub-pixel located at a vertical location corresponding to that of the sub-pixel being calculated and $1/2^{N-1}$ unit horizontal location.

Nokia Exhibit 2004, p. 32
Amazon.com v. Nokia
IPR2024-01141

When values for sub-pixels at unit horizontal and $1/2^N$ unit vertical locations, and $1/2^{N-1}$ unit horizontal and $1/2^N$ unit vertical locations are required, they may be interpolated by taking the average of the values of a first pixel or sub-pixel located at a horizontal location corresponding to that of the sub-pixel being calculated and unit vertical location and a second pixel or sub-pixel located at a horizontal location corresponding to that of the sub-pixel being calculated and $1/2^{N-1}$ unit vertical location.

Values for sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations may be interpolated by taking the average of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

Values for sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations may be interpolated by taking the average of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location.

Values for half of the sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations may be interpolated by taking the average of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and values for the other half of the sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are interpolated by taking the average of a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

Values for sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are alternately interpolated for one such sub-pixel by taking the average of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit

Nokia Exhibit 2004, p. 33
Amazon.com v. Nokia
IPR2024-01141

vertical location and values and for a neighbouring such sub-pixel by taking the average of a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

The sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations may be alternately interpolated in a horizontal direction.

The sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations may be alternately interpolated in a horizontal direction.

When values for some sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are required, such values may be interpolated by taking the average of a plurality of nearest neighbouring pixels.

At least one of step a) and step b) interpolating sub-pixel values directly using weighted sums may involve the calculation of an intermediate value for the sub-pixel values having a dynamic range greater than the specified dynamic range.

The intermediate value for a sub-pixel having $1/2^{N-1}$ sub-pixel resolution may be used the calculation of a sub-pixel value having $1/2^N$ sub-pixel resolution.

According to a second aspect of the invention, there is provided a method of interpolation in video coding in which an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, is interpolated to generate values for sub-pixels at fractional horizontal and vertical locations, the method comprising:

Nokia Exhibit 2004, p. 34
Amazon.com v. Nokia
IPR2024-01141

a) when values for sub-pixels at half unit horizontal and unit vertical locations, and unit horizontal and half unit vertical locations are required, interpolating such values directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) when values for sub-pixels at half unit horizontal and half unit vertical locations are required, interpolating such values directly using a weighted sum of values for sub-pixels residing at half unit horizontal and unit vertical locations calculated according to step (a); and

c) when values for sub-pixels at quarter unit horizontal and quarter unit vertical locations are required, interpolating such values by taking the average of at least one pair of a first pair of values of a sub-pixel located at a half unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and half unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a half unit horizontal and half unit vertical location.

According to a third aspect of the invention, there is provided a method of interpolation in video coding in which an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, is interpolated to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$ where x is a positive integer having a maximum value N, the method comprising:

a) when values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations are required, interpolating such values directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) when a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required, interpolating such a value directly using a

Nokia Exhibit 2004, p. 35
Amazon.com v. Nokia
IPR2024-01141

choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

The sub-pixels used in the first weighted sum may be sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and the first weighted sum may be used to interpolate a value for a sub-pixel at $1/2^{N-1}$ unit horizontal and $1/2^{N}$ unit vertical location.

The sub-pixels used in the second weighted sum may be sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations and the second weighted sum may be used to interpolate a value for a sub-pixel at $1/2^{N}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

When values for sub-pixels at $1/2^{N}$ unit horizontal and $1/2^{N}$ unit vertical locations are required, they may be interpolated by taking the average of at least one pair of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

In the foregoing, N may be equal an integer selected from a list consisting of the values 2, 3, and 4.

Sub-pixels at quarter unit horizontal location are to be interpreted as being sub-pixels having as their left-hand nearest neighbour a pixel at unit horizontal location and as their right-hand nearest neighbour a sub-pixel at half unit horizontal location as well as sub-pixels having as their left-hand nearest neighbour a sub-pixel at half unit horizontal location and as their

Nokia Exhibit 2004, p. 36
Amazon.com v. Nokia
IPR2024-01141

right-hand nearest neighbour a pixel at unit horizontal location. Correspondingly, sub-pixels at quarter unit vertical location are to be interpreted as being sub-pixels having as their upper nearest neighbour a pixel at unit vertical location and as their lower nearest neighbour a sub-pixel at half unit vertical location as well as sub-pixels having as their upper nearest neighbour a sub-pixel at half unit vertical location and as their lower nearest neighbour a pixel at unit vertical location.

The term dynamic range, refers to the range of values which the sub-pixel values and the weighted sums can take.

Preferably changing the dynamic range, whether by extending it or reducing it, means changing the number of bits which are used to represent the dynamic range.

In an embodiment of the invention, the method is applied to an image that is sub-divided into a number of image blocks. Preferably each image block comprises four corners, each corner being defined by a pixel located at a unit horizontal and unit vertical location. Preferably the method is applied to each image block as the block becomes available for sub-pixel value interpolation. Alternatively, sub-pixel value interpolation according to the method of the invention is performed once all image blocks of an image have become available for sub-pixel value interpolation.

Preferably the method is used in video encoding. Preferably the method is used in video decoding.

In one embodiment of the invention, when used in encoding, the method is carried out as before-hand interpolation, in which values for all sub-pixels at half unit locations and values for all sub-pixels at quarter unit locations are calculated and stored before being subsequently used in the determination

Nokia Exhibit 2004, p. 37
Amazon.com v. Nokia
IPR2024-01141

of a prediction frame during motion predictive coding. In alternative embodiments, the method is carried out as a combination of before-hand and on-demand interpolation. In this case, a certain proportion or category of sub-pixel values is calculated and stored before being used in the determination of a prediction frame and certain other sub-pixel values are calculated only when required during motion predictive coding.

Preferably, when the method is used in decoding, sub-pixels are only interpolated when their need is indicated by a motion vector.

According to a fourth aspect of the invention, there is provided a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$, where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) interpolate a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-m}$ unit vertical

Nokia Exhibit 2004, p. 38
Amazon.com v. Nokia
IPR2024-01141

location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^{N}$ unit horizontal and $1/2^{N}$ vertical location.

The video coder may comprise a video encoder. It may comprise a video decoder. There may be a codec comprising both the video encoder and the video decoder.

According to a fifth aspect of the invention, there is provided a communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^{x}$, where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) interpolate a value for a sub-pixel situated at a $1/2^{N}$ unit horizontal and $1/2^{N}$ unit vertical location by taking a weighted average of the value of a first

Nokia Exhibit 2004, p. 39
Amazon.com v. Nokia
IPR2024-01141

sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^{N}$ unit horizontal and $1/2^{N}$ vertical location.

The communications terminal may comprise a video encoder. It may comprise a video decoder. Preferably, it comprises a video codec comprising a video encoder and a video decoder.

Preferably the communications terminal comprising a user interface, a processor and at least one of a transmitting block and a receiving block, and a video coder according to at least one of the third and fourth aspects of the invention. Preferably the processor controls the operation of the transmitting block and/or the receiving block and the video coder.

According to a sixth aspect of the invention, there is provided a telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the communications terminal comprising a video coder for coding for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^{x}$, where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using

Nokia Exhibit 2004, p. 40
Amazon.com v. Nokia
IPR2024-01141

weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) interpolate a value for a sub-pixel situated at a $1/2^{N}$ unit horizontal and $1/2^{N}$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^{N}$ unit horizontal and $1/2^{N}$ vertical location.

Preferably the telecommunications system is a mobile telecommunications system comprising a mobile communications terminal and a wireless network, the connection between the mobile communications terminal and the wireless network being formed by a radio link. Preferably the network enables the communications terminal to communicate with other communications terminals connected to the network over communications links between the other communications terminals and the network.

According to a seventh aspect of the invention, there is provided a telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the network comprising a video coder for coding for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at

Nokia Exhibit 2004, p. 41
Amazon.com v. Nokia
IPR2024-01141

unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$, where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) interpolate a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

According to an eighth aspect of the invention there is provided a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and

Nokia Exhibit 2004, p. 42
Amazon.com v. Nokia
IPR2024-01141

vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

The interpolator may be further adapted to form the first weighted sum using the values of sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and to use the first weighted sum to interpolate a value for a sub-pixel at $1/2^{N-1}$ unit horizontal and $1/2^{N}$ unit vertical location.

The interpolator may be further adapted to form the second weighted sum using the values of sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations and to use the second weighted sum to interpolate a value for a sub-pixel at $1/2^{N}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

The interpolator may be further adapted to interpolate values for sub-pixels at $1/2^{N}$ unit horizontal and $1/2^{N}$ unit vertical locations by taking the average of at least one pair of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

Nokia Exhibit 2004, p. 43
Amazon.com v. Nokia
IPR2024-01141

According to a ninth aspect of the invention there is provided a communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

According to a tenth aspect of the invention there is provided a telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

Nokia Exhibit 2004, p. 44
Amazon.com v. Nokia
IPR2024-01141

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

According to an eleventh aspect of the invention there is provided a telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the network comprising a video coder for coding for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for

Nokia Exhibit 2004, p. 45
Amazon.com v. Nokia
IPR2024-01141

sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

Brief Description of the Figures

An embodiment of the invention will now be described by way of example only with reference to the accompanying drawings in which:

Figure 1 shows a video encoder according to the prior art;

Figure 2 shows a video decoder according to the prior art;

Figure 3 shows the types of frames used in video encoding;

Figures 4a, 4b, and 4c show steps in block-matching;

Figure 5 illustrates the process of motion estimation to sub-pixel resolution;

Figure 6 shows a terminal device comprising video encoding and decoding equipment in which the method of the invention may be implemented;

Figure 7 shows a video encoder according an embodiment of the present invention;

Figure 8 shows a video decoder according to an embodiment of the present invention;

Figures 9 and 10 have not been used and any such figures should be disregarded;

Figure 11 shows a schematic diagram of a mobile telecommunications network according to an embodiment of the present invention;

Figure 12a shows a notation for describing pixel and sub-pixel locations specific to TML5;

Figure 12b shows interpolation of a half resolution sub-pixels;

Figure 12c shows interpolation of a half resolution sub-pixels;

Figure 13a shows a notation for describing pixel and sub-pixel locations specific to TML6;

Figure 13b shows interpolation of a half resolution sub-pixels;

Figure 13c shows interpolation of a half resolution sub-pixels;

Nokia Exhibit 2004, p. 46
Amazon.com v. Nokia
IPR2024-01141

Figure 14 shows a notation for describing pixel and sub-pixel locations specific to the invention;

Figure 14b shows interpolation of a half resolution sub-pixels according to the invention;

Figure 14c shows interpolation of a half resolution sub-pixels according to the invention;

Figure 15 shows possible choices of diagonal interpolation for sub-pixels;

Figure 16 shows the half resolution sub-pixel values required to calculate other half resolution sub-pixel values;

Figure 17a shows the half resolution sub-pixel values that must be calculated in order to interpolate values for quarter resolution sub-pixels in an image block using the interpolation method of TML5;

Figure 17b shows the half resolution sub-pixel values that must be calculated in order to interpolate values for quarter resolution sub-pixels in an image block using the interpolation method according to the invention;

Figures 18a shows the numbers of half resolution sub-pixels that must be calculated in order to obtain values for quarter resolution sub-pixels within an image block using the sub-pixel value interpolation method according to TML5;

Figure 18b shows the numbers of half resolution sub-pixels that must be calculated in order to obtain values for quarter resolution sub-pixels within an image block using the sub-pixel value interpolation method according to the invention;

Figure 19 shows a numbering scheme for each of the 15 sub-pixel positions;

Figure 20 shows nomenclature used to describe pixels, half resolution sub-pixels, quarter resolution sub-pixels and eighth resolution sub-pixels

Figure 21a shows the diagonal direction to be used in the interpolation of each eighth resolution sub-pixel in an embodiment of the invention;

Nokia Exhibit 2004, p. 47
Amazon.com v. Nokia
IPR2024-01141

Figure 21b shows the diagonal direction to be used in the interpolation of each eighth resolution sub-pixel in another embodiment of the invention; and

Figure 22 shows nomenclature used to describe eighth resolution sub-pixels within an image.

Detailed Description

Figures 1 to 5, 12a, 12b, 12c, 13a, 13b, and 13c have been described in the foregoing.

Figure 6 presents a terminal device comprising video encoding and decoding equipment which may be adapted to operate in accordance with the present invention. More precisely, the figure illustrates a multimedia terminal 60 implemented according to ITU-T recommendation H.324. The terminal can be regarded as a multimedia transceiver device. It includes elements that capture, encode and multiplex multimedia data streams for transmission via a communications network, as well as elements that receive, de-multiplex, decode and display received multimedia content. ITU-T recommendation H.324 defines the overall operation of the terminal and refers to other recommendations that govern the operation of its various constituent parts. This kind of multimedia terminal can be used in real-time applications such as conversational videotelephony, or non real-time applications such as the retrieval/streaming of video clips, for example from a multimedia content server in the Internet.

In the context of the present invention, it should be appreciated that the H.324 terminal shown in Figure 6 is only one of a number of alternative multimedia terminal implementations suited to application of the inventive method. It should also be noted that a number of alternatives exist relating to the location and implementation of the terminal equipment. As illustrated

Nokia Exhibit 2004, p. 48
Amazon.com v. Nokia
IPR2024-01141

in Figure 6, the multimedia terminal may be located in communications equipment connected to a fixed line telephone network such as an analogue PSTN (Public Switched Telephone Network). In this case the multimedia terminal is equipped with a modem 71, compliant with ITU-T recommendations V.8, V.34 and optionally V.8bis. Alternatively, the multimedia terminal may be connected to an external modem. The modem enables conversion of the multiplexed digital data and control signals produced by the multimedia terminal into an analogue form suitable for transmission over the PSTN. It further enables the multimedia terminal to receive data and control signals in analogue form from the PSTN and to convert them into a digital data stream that can be demulitplexed and processed in an appropriate manner by the terminal.

An H.324 multimedia terminal may also be implemented in such a way that it can be connected directly to a digital fixed line network, such as an ISDN (Integrated Services Digital Network). In this case the modem 71 is replaced with an ISDN user-network interface. In Figure 6, this ISDN user-network interface is represented by alternative block 72.

H.324 multimedia terminals may also be adapted for use in mobile communication applications. If used with a wireless communication link, the modem 71 can be replaced with any appropriate wireless interface, as represented by alternative block 73 in Figure 6. For example, an H.324/M multimedia terminal can include a radio transceiver enabling connection to the current 2nd generation GSM mobile telephone network, or the proposed 3rd generation UMTS (Universal Mobile Telephone System).

It should be noted that in multimedia terminals designed for two-way communication, that is for transmission and reception of video data, it is advantageous to provide both a video encoder and video decoder implemented according to the present invention. Such an encoder and

Nokia Exhibit 2004, p. 49
Amazon.com v. Nokia
IPR2024-01141

decoder pair is often implemented as a single combined functional unit, referred to as a 'codec'.

Because a video encoder according to the invention performs motion compensated video encoding to sub-pixel resolution using a specific interpolation scheme and a particular combination of before-hand and on-demand sub-pixel value interpolation, it is generally necessary for a video decoder of a receiving terminal to be implemented in a manner compatible with the encoder of the transmitting terminal which formed the compressed video data stream. Failure to ensure this compatibility may have an adverse effect on the quality of the motion compensation and the accuracy of reconstructed video frames.

A typical H.324 multimedia terminal will now be described in further detail with reference to Figure 6.

The multimedia terminal 60 includes a variety of elements referred to as 'terminal equipment'. This includes video, audio and telematic devices, denoted generically by reference numbers 61, 62 and 63, respectively. The video equipment 61 may include, for example, a video camera for capturing video images, a monitor for displaying received video content and optional video processing equipment. The audio equipment 62 typically includes a microphone, for example for capturing spoken messages, and a loudspeaker for reproducing received audio content. The audio equipment may also include additional audio processing units. The telematic equipment 63, may include a data terminal, keyboard, electronic whiteboard or a still image transceiver, such as a fax unit.

The video equipment 61 is coupled to a video codec 65. The video codec 65 comprises a video encoder and a corresponding video decoder both implemented according to the invention. Such an encoder and decoder

Nokia Exhibit 2004, p. 50
Amazon.com v. Nokia
IPR2024-01141

will be described in the following. The video codec 65 is responsible for encoding captured video data in an appropriate form for further transmission over a communications link and decoding compressed video content received from the communications network. In the example illustrated in Figure 6, the video codec is implemented according to ITU-T recommendation H.263, with appropriate modifications to implement the sub-pixel value interpolation method according to the invention in both the encoder and the decoder of the video codec.

Similarly, the terminal's audio equipment is coupled to an audio codec, denoted in Figure 6 by reference number 66. Like the video codec, the audio codec comprises an encoder/decoder pair. It converts audio data captured by the terminal's audio equipment into a form suitable for transmission over the communications link and transforms encoded audio data received from the network back into a form suitable for reproduction, for example on the terminal's loudspeaker. The output of the audio codec is passed to a delay block 67. This compensates for the delays introduced by the video coding process and thus ensures synchronisation of audio and video content.

The system control block 64 of the multimedia terminal controls end-to-network signalling using an appropriate control protocol (signalling block 68) to establish a common mode of operation between a transmitting and a receiving terminal. The signalling block 68 exchanges information about the encoding and decoding capabilities of the transmitting and receiving terminals and can be used to enable the various coding modes of the video encoder. The system control block 64 also controls the use of data encryption. Information regarding the type of encryption to be used in data transmission is passed from encryption block 69 to the multiplexer/de-multiplexer (MUX/DMUX unit) 70.

Nokia Exhibit 2004, p. 51
Amazon.com v. Nokia
IPR2024-01141

During data transmission from the multimedia terminal, the MUX/DMUX unit 70 combines encoded and synchronised video and audio streams with data input from the telematic equipment 63 and possible control data, to form a single bit-stream. Information concerning the type of data encryption (if any) to be applied to the bit-stream, provided by encryption block 69, is used to select an encryption mode. Correspondingly, when a multiplexed and possibly encrypted multimedia bit-stream is being received, MUX/DMUX unit 70 is responsible for decrypting the bit-stream, dividing it into its constituent multimedia components and passing those components to the appropriate codec(s) and/or terminal equipment for decoding and reproduction.

It should be noted that the functional elements of the multimedia terminal, video encoder, decoder and video codec according to the invention can be implemented as software or dedicated hardware, or a combination of the two. The video encoding and decoding methods according to the invention are particularly suited for implementation in the form of a computer program comprising machine-readable instructions for performing the functional steps of the invention. As such, the encoder and decoder according to the invention may be implemented as software code stored on a storage medium and executed in a computer, such as a personal desktop computer, in order to provide that computer with video encoding and/or decoding functionality.

If the multimedia terminal 60 is a mobile terminal, that is if it is equipped with a radio transceiver 73, it will be understood by those skilled in the art that it may also comprise additional elements. In one embodiment it comprises a user interface having a display and a keyboard, which enables operation of the multimedia terminal 60 by a user, together with necessary functional blocks including a central processing unit, such as a microprocessor, which controls the blocks responsible for different functions of the multimedia

Nokia Exhibit 2004, p. 52
Amazon.com v. Nokia
IPR2024-01141

terminal, a random access memory RAM, a read only memory ROM, and a digital camera. The microprocessor's operating instructions, that is program code corresponding to the basic functions of the multimedia terminal 60, is stored in the read-only memory ROM and can be executed as required by the microprocessor, for example under control of the user. In accordance with the program code, the microprocessor uses the radio transceiver 73 to form a connection with a mobile communication network, enabling the multimedia terminal 60 to transmit information to and receive information from the mobile communication network over a radio path.

The microprocessor monitors the state of the user interface and controls the digital camera. In response to a user command, the microprocessor instructs the camera to record digital images into the RAM. Once an image is captured, or alternatively during the capturing process, the microprocessor segments the image into image segments (for example macroblocks) and uses the encoder to perform motion compensated encoding for the segments in order to generate a compressed image sequence as explained in the foregoing description. A user may command the multimedia terminal 60 to display the captured images on its display or to send the compressed image sequence using the radio transceiver 73 to another multimedia terminal, a video telephone connected to a fixed line network (PSTN) or some other telecommunications device. In a preferred embodiment, transmission of image data is started as soon as the first segment is encoded so that the recipient can start a corresponding decoding process with a minimum delay.

Figure 11 is a schematic diagram of a mobile telecommunications network according to an embodiment of the invention. Multimedia terminals MS are in communication with base stations BTS by means of a radio link. The base stations BTS are further connected, through a so-called Abis interface,

Nokia Exhibit 2004, p. 53
Amazon.com v. Nokia
IPR2024-01141

to a base station controller BSC, which controls and manages several base stations.

The entity formed by a number of base stations BTS (typically, by a few tens of base stations) and a single base station controller BSC, controlling the base stations, is called a base station subsystem BSS. Particularly, the base station controller BSC manages radio communication channels and handovers. The base station controller BSC is also connected, through a so-called A interface, to a mobile services switching centre MSC, which co-ordinates the formation of connections to and from mobile stations. A further connection is made, through the mobile service switching centre MSC, to outside the mobile communications network. Outside the mobile communications network there may further reside other network(s) connected to the mobile communications network by gateway(s) GTW, for example the Internet or a Public Switched Telephone Network (PSTN). In such an external network, or within the telecommunications network, there may be located video decoding or encoding stations, such as computers PC. In an embodiment of the invention, the mobile telecommunications network comprises a video server VSRVR to provide video data to a MS subscribing to such a service. The video data is compressed using the motion compensated video compression method as described in the foregoing. The video server may function as a gateway to an online video source or it may comprise previously recorded video clips. Typical videotelephony applications may involve, for example, two mobile stations or one mobile station MS and a videotelephone connected to the PSTN, a PC connected to the Internet or a H.261 compatible terminal connected either to the Internet or to the PSTN.

Figure 7 shows a video encoder 700 according to an embodiment the invention. Figure 8 shows a video decoder 800 according to an embodiment the invention.

Nokia Exhibit 2004, p. 54
Amazon.com v. Nokia
IPR2024-01141

The encoder 700 comprises an input 701 for receiving a video signal from a camera or other video source (not shown). It further comprises a DCT transformer 705, a quantiser 706, an inverse quantiser 709, an inverse DCT transformer 710, combiners 712 and 716, a before-hand sub-pixel interpolation block 730, a frame store 740 and an on-demand sub-pixel interpolation block 750, implemented in combination with motion estimation block 760. The encoder also comprises a motion field coding block 770 and a motion compensated prediction block 780. Switches 702 and 714 are operated co-operatively by a control manager 720 to switch the encoder between an INTRA-mode of video encoding and an INTER-mode of video encoding. The encoder 700 also comprises a multiplexer unit (MUX/DMUX) 790 to form a single bit-stream from the various types of information produced by the encoder 700 for further transmission to a remote receiving terminal, or for example for storage on a mass storage medium such as a computer hard drive (not shown).

It should be noted that the presence and implementations of before-hand sub-pixel interpolation block 730 and on-demand sub-pixel value interpolation block 750 in the encoder architecture depend on the way in which the sub-pixel interpolation method according to the invention is applied. In embodiments of the invention in which before-hand sub-pixel value interpolation is not performed, encoder 700 does not comprise before-hand sub-pixel value interpolation block 730. In other embodiments of the invention, only before-hand sub-pixel interpolation is performed and thus the encoder does not include on-demand sub-pixel value interpolation block 750. In embodiments in which both before-hand and on-demand sub-pixel value interpolation are performed, both blocks 730 and 750 are present in the encoder 700.

Nokia Exhibit 2004, p. 55
Amazon.com v. Nokia
IPR2024-01141

Operation of the encoder 700 according to the invention will now be described in detail. In the description, it will be assumed that each frame of uncompressed video, received from the video source at the input 701, is received and processed on a macroblock-by-macroblock basis, preferably in raster-scan order. It will further be assumed that when the encoding of a new video sequence starts, the first frame of the sequence is encoded in INTRA-mode. Subsequently, the encoder is programmed to code each frame in INTER-format, unless one of the following conditions is met: 1) it is judged that the current frame being coded is so dissimilar from the reference frame used in its prediction that excessive prediction error information is produced; 2) a predefined INTRA frame repetition interval has expired; or 3) feedback is received from a receiving terminal indicating a request for a frame to be coded in INTRA format.

The occurrence of condition 1) is detected by monitoring the output of the combiner 716. The combiner 716 forms a difference between the current macroblock of the frame being coded and its prediction, produced in the motion compensated prediction block 780. If a measure of this difference (for example a sum of absolute differences of pixel values) exceeds a predetermined threshold, the combiner 716 informs the control manager 720 via a control line 717 and the control manager 720 operates the switches 702 and 714 so as to switch the encoder 700 into INTRA coding mode. Occurrence of condition 2) is monitored by means of a timer or frame counter implemented in the control manager 720, in such a way that if the timer expires, or the frame counter reaches a predetermined number of frames, the control manager 720 operates the switches 702 and 714 to switch the encoder into INTRA coding mode. Condition 3) is triggered if the control manager 720 receives a feedback signal from, for example, a receiving terminal, via control line 718 indicating that an INTRA frame refresh is required by the receiving terminal. Such a condition might arise, for example, if a previously transmitted frame were badly corrupted by

Nokia Exhibit 2004, p. 56
Amazon.com v. Nokia
IPR2024-01141

interference during its transmission, rendering it impossible to decode at the receiver. In this situation, the receiver would issue a request for the next frame to be encoded in INTRA format, thus re-initialising the coding sequence.

It will further be assumed that the encoder and decoder are implemented in such a way as to allow the determination of motion vectors with a spatial resolution of up to quarter-pixel resolution. As will be seen in the following, finer levels of resolution are also possible.

Operation of the encoder 700 in INTRA coding mode will now be described. In INTRA-mode, the control manager 720 operates the switch 702 to accept video input from input line 719. The video signal input is received macroblock by macroblock from input 701 via the input line 719 and each macroblock of original image pixels is transformed into DCT coefficients by the DCT transformer 705. The DCT coefficients are then passed to the quantiser 706, where they are quantised using a quantisation parameter QP. Selection of the quantisation parameter QP is controlled by the control manager 720 via control line 722. Each DCT transformed and quantised macroblock that makes up the INTRA coded image information 723 of the frame is passed from the quantiser 706 to the MUX/DMUX 790. The MUX/DMUX 790 combines the INTRA coded image information with possible control information (for example header data, quantisation parameter information, error correction data etc.) to form a single bit-stream of coded image information 725. Variable length coding (VLC) is used to reduce redundancy of the compressed video bit-stream, as is known to those skilled in the art.

A locally decoded picture is formed in the encoder 700 by passing the data output by the quantiser 706 through inverse quantiser 709 and applying an inverse DCT transform 710 to the inverse-quantised data. The resulting

Nokia Exhibit 2004, p. 57
Amazon.com v. Nokia
IPR2024-01141

data is then input to the combiner 712. In INTRA mode, switch 714 is set so that the input to the combiner 712 via the switch 714 is set to zero. In this way, the operation performed by the combiner 712 is equivalent to passing the decoded image data formed by the inverse quantiser 709 and the inverse DCT transform 710 unaltered.

In embodiments of the invention in which before-hand sub-pixel value interpolation is performed, the output from combiner 712 is applied to before-hand sub-pixel interpolation block 730. The input to the before-hand sub-pixel value interpolation block 730 takes the form of decoded image blocks. In the before-hand sub-pixel value interpolation block 730, each decoded macroblock is subjected to sub-pixel interpolation in such a way that a predetermined sub-set of sub-pixel resolution sub-pixel values is calculated according to the interpolation method of the invention and is stored together with the decoded pixel values in frame store 740.

In embodiments in which before-hand sub-pixel interpolation is not performed, before-hand sub-pixel interpolation block is not present in the encoder architecture and the output from combiner 712, comprising decoded image blocks, is applied directly to frame store 740.

As subsequent macroblocks of the current frame are received and undergo the previously described coding and decoding steps in blocks 705, 706, 709, 710, 712, a decoded version of the INTRA frameis built up in the frame store 740. When the last macroblock of the current frame has been INTRA coded and subsequently decoded, the frame store 740 contains a completely decoded frame, available for use as a prediction reference frame in coding a subsequently received video frame in INTER format. In embodiments of the invention in which before-hand sub-pixel value interpolation is performed, the reference frame held in frame store 740 is at least partially interpolated to sub-pixel resolution.

Nokia Exhibit 2004, p. 58
Amazon.com v. Nokia
IPR2024-01141

Operation of the encoder 700 in INTER coding mode will now be described. In INTER coding mode, the control manager 720 operates switch 702 to receive its input from line 721, which comprises the output of the combiner 716. The combiner 716 forms prediction error information representing the difference between the current macroblock of the frame being coded and its prediction, produced in the motion compensated prediction block 780. The prediction error information is DCT transformed in block 705 and quantised in block 706 to form a macroblock of DCT transformed and quantised prediction error information. Each macroblock of DCT transformed and quantised prediction error information is passed from the quantiser 706 to the MUX/DMUX unit 790. The MUX/DMUX unit 790 combines the prediction error information 723 with motion coefficients 724 (described in the following) and control information (for example header data, quantisation parameter information, error correction data etc.) to form a single bit-stream of coded image information, 725.

Locally decoded prediction error information for the each macroblock of the INTER coded frame is then formed in the encoder 700 by passing the encoded prediction error information 723 output by the quantiser 706 through the inverse quantiser 709 and applying an inverse DCT transform in block 710. The resulting locally decoded macroblock of prediction error information is then input to combiner 712. In INTER-mode, switch 714 is set so that the combiner 712 also receives motion predicted macroblocks for the current INTER frame, produced in the motion compensated prediction block 780. The combiner 712 combines these two pieces of information to produce reconstructed image blocks for the current INTER frame.

As described above when considering INTRA coded frames, in embodiments of the invention in which before-hand sub-pixel value interpolation is performed, the output from combiner 712 is applied to the

Nokia Exhibit 2004, p. 59
Amazon.com v. Nokia
IPR2024-01141

before-hand sub-pixel interpolation block 730. Thus, the input to the before-hand sub-pixel value interpolation block 730 in INTER coding mode also takes the form of decoded image blocks. In the before-hand sub-pixel value interpolation block 730, each decoded macroblock is subjected to sub-pixel interpolation in such a way that a predetermined sub-set of sub-pixel values is calculated according to the interpolation method of the invention and is stored together with the decoded pixel values in frame store 740. In embodiments in which before-hand sub-pixel interpolation is not performed, before-hand sub-pixel interpolation block is not present in the encoder architecture and the output from combiner 712, comprising decoded image blocks, is applied directly to frame store 740.

As subsequent macroblocks of the video signal are received from the video source and undergo the previously described coding and decoding steps in blocks 705, 706, 709, 710, 712, a decoded version of the INTER frame is built up in the frame store 740. When the last macroblock of the frame has been INTER coded and subsequently decoded, the frame store 740 contains a completely decoded frame, available for use as a prediction reference frame in encoding a subsequently received video frame in INTER format. In embodiments of the invention in which before-hand sub-pixel value interpolation is performed, the reference frame held in frame store 740 is at least partially interpolated to sub-pixel resolution.

Formation of a prediction for a macroblock of the current frame will now be described.

Any frame encoded in INTER format requires a reference frame for motion compensated prediction. This means, inter alia, that when encoding a video sequence, the first frame to be encoded, whether it is the first frame in the sequence, or some other frame, must be encoded in INTRA format. This, in turn, means that when the video encoder 700 is switched into INTER coding

Nokia Exhibit 2004, p. 60
Amazon.com v. Nokia
IPR2024-01141

mode by control manager 720, a complete reference frame, formed by locally decoding a previously encoded frame, is already available in the frame store 740 of the encoder. In general, the reference frame is formed by locally decoding either an INTRA coded frame or an INTER coded frame.

The first step in forming a prediction for a macroblock of the current frame is performed by motion estimation block 760. The motion estimation block 760 receives the current macroblock of the frame being coded via line 727 and performs a block matching operation in order to identify a region in the reference frame which corresponds substantially with the current macroblock. According to the invention, the block-matching process is performed to sub-pixel resolution in a manner that depends on the implementation of the encoder 700 and the degree of before-hand sub-pixel interpolation performed. However, the basic principle behind the block-matching process is similar in all cases. Specifically, motion estimation block 760 performs block-matching by calculating difference values (e.g. sums of absolute differences) representing the difference in pixel values between the macroblock of the current frame under examination and candidate best-matching regions of pixels / sub-pixels in the reference frame. A difference value is produced for all possible offsets (e.g. quarter- or one eighth sub-pixel precision x, y displacements) between the macroblock of the current frame and candidate test region within a predefined search region of the reference frame and motion estimation block 760 determines the smallest calculated difference value. The offset between the macroblock in the current frame and the candidate test region of pixel values / sub-pixel values in the reference frame that yields the smallest difference value defines the motion vector for the macroblock in question. In certain embodiments of the invention, an initial estimate for the motion vector having unit pixel precision is first determined and then refined to a finer level of sub-pixel precision, as described in the foregoing.

Nokia Exhibit 2004, p. 61
Amazon.com v. Nokia
IPR2024-01141

In embodiments of the encoder in which before-hand sub-pixel value interpolation is not performed, all sub-pixel values required in the block matching process are calculated in on-demand sub-pixel value interpolation block 750. Motion estimation block 760 controls on-demand sub-pixel value interpolation block 750 to calculate each sub-pixel value needed in the block-matching process in an on-demand fashion, as and when it is required. In this case, motion estimation block 760 may be implemented so as to perform block-matching as a one-step process, in which case a motion vector with the desired sub-pixel resolution is sought directly, or it may be implemented so as to perform block-matching as a two step process. If the two-step process is adopted, the first step may comprise a search for e.g. a full or half-pixel resolution motion vector and the second step is performed in order to refine the the motion vector to the desired sub-pixel resolution. As block matching is an exhaustive process, in which blocks of n x m pixels in the current frame are compared one-by-one with blocks of n x m pixels or sub-pixels in the interpolated reference frame, it should be appreciated that a sub-pixel calculated in an on-demand fashion by the on-demand pixel interpolation block 750 may need to be calculated multiple times as successive difference values are determined. In a video encoder, this approach is not the most efficient possible in terms of computational complexity / burden.

In embodiments of the encoder which use only before-hand sub-pixel value interpolation, block-matching may be performed as a one step process, as all sub-pixel values of the reference frame required to determine a motion vector with the desired sub-pixel resolution are calculated before-hand in block 730 and stored in frame store 740. Thus, they are directly available for use in the block-matching process and can be retrieved as required from frame store 740 by motion estimation block 760. However, even in the case where all sub-pixel values are available from frame store 740, it is still more computationally efficient to perform block-matching as a two-step process,

Nokia Exhibit 2004, p. 62
Amazon.com v. Nokia
IPR2024-01141

as fewer difference calculations are required. It should be appreciated that while full before-hand sub-pixel value interpolation reduces computational complexity in the encoder, it is not the most efficient approach in terms of memory consumption.

In embodiments of the encoder in which both before-hand and on-demand sub-pixel value interpolation are used, motion estimation block 760 is implemented in such a way that it can retrieve sub-pixel values previously calculated in before-hand sub-pixel value interpolation block 730 and stored in frame store 740 and further control on-demand sub-pixel value interpolation block 750 to calculate any additional sub-pixel values that may be required. The block-matching process may be performed as a one-step or a two-step process. If a two-step implementation is used, before-hand calculated sub-pixel values retrieved from frame store 740 may be used in the first step of the process and the second step may be implemented so as to use sub-pixel values calculated by on-demand sub-pixel value interpolation block 750. In this case, certain sub-pixel values used in the second step of the block matching process may need to be calculated multiple times as successive comparisons are made, but the number of such duplicate calculations is significantly less than if before-hand sub-pixel value calculation is not used. Furthermore, memory consumption is reduced with respect to embodiments in which only before-hand sub-pixel value interpolation is used.

Once the motion estimation block 760 has produced a motion vector for the macroblock of the current frame under examination, it outputs the motion vector to the motion field coding block 770. Motion field coding block 770 then approximates the motion vector received from motion estimation block 760 using a motion model. The motion model generally comprises a set of basis functions. More specifically, the motion field coding block 770 represents the motion vector as a set of coefficient values (known as motion

Nokia Exhibit 2004, p. 63
Amazon.com v. Nokia
IPR2024-01141

coefficients) which, when multiplied by the basis functions, form an approximation of the motion vector. The motion coefficients 724 are passed from motion field coding block 770 to motion compensated prediction block 780. Motion compensated prediction block 780 also receives the pixel / sub-pixel values of the best-matching candidate test region of the reference frame identified by motion estimation block 760. In Figure 7, these values are shown to be passed via line 729 from on-demand sub-pixel interpolation block 750. In alternative embodiments of the invention, the pixel values in question are provided from the motion estimation block 760 itself.

Using the approximate representation of the motion vector generated by motion field coding block 770 and the pixel / sub-pixel values of the best-matching candidate test region, motion compensated prediction block 780 produces a macroblock of predicted pixel values. The macroblock of predicted pixel values represents a prediction for the pixel values of the current macroblock generated from the interpolated reference frame. The macroblock of predicted pixel values is passed to the combiner 716 where it is subtracted from the new current frame in order to produce prediction error information 723 for the macroblock, as described in the foregoing.

The motion coefficients 724 formed by motion field coding block are also passed to the MUX/DMUX unit 790, where they are combined with prediction error information 723 for the macroblock in question and possible control information from control manager 720 to form an encoded video stream 725 for transmission to a receiving terminal.

Operation of a video decoder 800 according to the invention will now be described. Referring to Figure 8, the decoder 800 comprises a demultiplexing unit (MUX/DMUX) 810, which receives the encoded video stream 725 from the encoder 700 and demultiplexes it, an inverse quantiser 820, an inverse DCT transformer 830, a motion compensated prediction

Nokia Exhibit 2004, p. 64
Amazon.com v. Nokia
IPR2024-01141

block 840, a frame store 850, a combiner 860, a control manager 870, an output 880, before-hand sub-pixel value interpolation block 845 and on-demand sub-pixel interpolation block 890 associated with the motion compensated prediction block 840. In practice the control manager 870 of the decoder 800 and the control manager 720 of the encoder 700 may be the same processor. This may be the case if the encoder 700 and decoder 800 are part of the same video codec.

Figure 8 shows an embodiment in which a combination of before-hand and on-demand sub-pixel value interpolation is used in the decoder. In other embodiments, only before-hand sub-pixel value interpolation is used, in which case decoder 800 does not include on-demand sub-pixel value interpolation block 890. In a preferred embodiment of the invention, no before-hand sub-pixel value interpolation is used in the decoder and therefore before-hand sub-pixel value interpolation block 845 is omitted from the decoder architecture. If both before-hand and on-demand sub-pixel value interpolation are performed, the decoder comprises both blocks 845 and 890.

The control manager 870 controls the operation of the decoder 800 in response to whether an INTRA or an INTER frame is being decoded. An INTRA / INTER trigger control signal, which causes the decoder to switch between decoding modes is derived, for example, from picture type information provided in the header portion of each compressed video frame received from the encoder. The INTRA / INTER trigger control signal is passed to control manager 870 via control line 815, together with other video codec control signals demultiplexed from the encoded video stream 725 by the MUX/DMUX unit 810.

When an INTRA frame is decoded, the encoded video stream 725 is demultiplexed into INTRA coded macroblocks and control information. No

Nokia Exhibit 2004, p. 65
Amazon.com v. Nokia
IPR2024-01141

motion vectors are included in the encoded video stream 725 for an INTRA coded frame. The decoding process is performed macroblock-by-macroblock. When the encoded information 723 for a macroblock is extracted from video stream 725 by MUX/DMUX unit 810, it is passed to inverse quantiser 820. The control manager controls inverse quantiser 820 to apply a suitable level of inverse quantisation to the macroblock of encoded information, according to control information provided in video stream 725. The inverse quantised macroblock is then inversely transformed in the inverse DCT transformer 830 to form a decoded block of image information. Control manager 870 controls combiner 860 to prevent any reference information being used in the decoding of the INTRA coded macroblock. The decoded block of image information is passed to the video output 880 of the decoder.

In embodiments of the decoder which employ before-hand sub-pixel value interpolation, the decoded block of image information (i.e. pixel values) produced as a result of the inverse quantisation and inverse transform operations performed in blocks 820 and 830 is passed to before-hand sub-pixel value interpolation block 845. Here, sub-pixel value interpolation is performed according to the method of the invention, the degree of before-hand sub-pixel value interpolation applied being determined by the details of the decoder implementation. In embodiments of the invention in which on-demand sub-pixel value interpolation is not performed, before-hand sub-pixel value interpolation block 845 interpolates all sub-pixelvalues. In embodiments that use a combination of before-hand and on-demand sub-pixel value interpolation, before-hand sub-pixel value interpolation block 845 interpolates a certain sub-set of sub-pixel values. This may comprise, for example, all sub-pixels at half-pixel locations, or a combination of sub-pixels at half-pixel and one quarter-pixel locations. In any case, after before-hand sub-pixel value interpolation, the interpolated sub-pixel values are stored in frame store 850, together with the original decoded pixel values. As

Nokia Exhibit 2004, p. 66
Amazon.com v. Nokia
IPR2024-01141

subsequent macroblocks are decoded, before-hand interpolated and stored, a decoded frame, at least partially interpolated to sub-pixel resolution is progressively assembled in the frame store 850 and becomes available for use as a reference frame for motion compensated prediction.

In embodiments of the decoder which do not employ before-hand sub-pixel value interpolation, the decoded block of image information (i.e. pixel values) produced as a result of the inverse quantisation and inverse transform operations performed on the macroblock in blocks 820 and 830 is passed directly to frame store 850. As subsequent macroblocks are decoded and stored, a decoded frame, having unit pixel resolution is progressively assembled in the frame store 850 and becomes available for use as a reference frame for motion compensated prediction.

When an INTER frame is decoded, the encoded video stream 725 is demultiplexed into encoded prediction error information 723 for each macroblock of the frame, associated motion coefficients 724 and control information. Again, the decoding process is performed macroblock-by-macroblock. When the encoded prediction error information 723 for a macroblock is extracted from the video stream 725 by MUX/DMUX unit 810, it is passed to inverse quantiser 820. Control manager 870 controls inverse quantiser 820 to apply a suitable level of inverse quantisation to the macroblock of encoded prediction error information, according to control information received in video stream 725. The inverse quantised macroblock of prediction error information is then inversely transformed in the inverse DCT transformer 830 to yield decoded prediction error information for the macroblock.

The motion coefficients 724 associated with the macroblock in question are extracted from the video stream 725 by MUX/DMUX unit 810 and passed to motion compensated prediction block 840, which reconstructs a motion

Nokia Exhibit 2004, p. 67
Amazon.com v. Nokia
IPR2024-01141

vector for the macroblock using the same motion model as that used to encode the INTER-coded macroblock in encoder 700. The reconstructed motion vector approximates the motion vector originally determined by motion estimation block 760 of the encoder. The motion compensated prediction block 840 of the decoder uses the reconstructed motion vector to identify the location of a block of pixel / sub-pixel values in a prediction reference frame stored in frame store 850. The reference frame may be, for example, a previously decoded INTRA frame, or a previously decoded INTER frame. In either case, the block of pixel / sub-pixel values indicated by the reconstructed motion vector, represents the prediction of the macroblock in question.

The reconstructed motion vector may point to any pixel or sub-pixel. If the motion vector indicates that the prediction for the current macroblock is formed from pixel values (i.e. the values of pixels at unit pixel locations), these can simply be retrieved from frame store 850, as the values in question are obtained directly during the decoding of each frame. If the motion vector indicates that the prediction for the current macroblock is formed from sub-pixel values, these must either be retrieved from frame store 850, or calculated in on-demand sub-pixel interpolation block 890. Whether sub-pixel values must be calculated, or can simply be retrieved from the frame store, depends on the degree of before-hand sub-pixel value interpolation used in the decoder.

In embodiments of the decoder that do not employ before-hand sub-pixel value interpolation, the required sub-pixel values are all calculated in on-demand sub-pixel value interpolation block 890. On the other hand, in embodiments in which all sub-pixel values are interpolated before-hand, motion compensated prediction block 840 can retrieve the required sub-pixel values directly from the frame store 850. In embodiments that use a combination before-hand and on-demand sub-pixel value interpolation, the

Nokia Exhibit 2004, p. 68
Amazon.com v. Nokia
IPR2024-01141

action required in order to obtain the required sub-pixel values depends on which sub-pixel values are interpolated before-hand. Taking as an example an embodiment in which all sub-pixel values at half-pixel locations are calculated before-hand, it is evident that if a reconstructed motion vector for a macroblock points to a pixel at unit location or a sub-pixel at half-pixel location, all the pixel or sub-pixel values required to form the prediction for the macroblock are present in the frame store 850 and can be retrieved from there by motion compensated prediction block 840. If, however, the motion vector indicates a sub-pixel at a quarter-pixel location, the sub-pixels required to form the prediction for the macroblock are not present in frame store 850 and are therefore calculated in on-demand sub-pixel value interpolation block 890. In this case, on-demand sub-pixel value interpolation block 890 retrieves any pixel or sub-pixel required to perform the interpolation from frame store 850 and applies the interpolation method described below. Sub-pixel values calculated in on-demand sub-pixel value interpolation block 890 are passed to motion compensated prediction block 840.

Once a prediction for a macroblock has been obtained, the prediction (that is, a macroblock of predicted pixel values) is passed from motion compensated prediction block 840 to combiner 860 where it combined with the decoded prediction error information for the macroblock to form a reconstructed image block which, in turn, is passed to the video output 880 of the decoder.

It should be appreciated that in practical implementations of encoder 700 and decoder 800, the extent to which frames are before-hand sub-pixel interpolated, and thus the amount of on-demand sub-pixel value interpolation that is performed, can be chosen according to, or dictated by, the hardware implementation of the video encoder 700, or the environment in which it is intended to be used. For example, if the memory available to

Nokia Exhibit 2004, p. 69
Amazon.com v. Nokia
IPR2024-01141

the video encoder is limited, or memory must be reserved for other functions, it is appropriate to limit the amount of before-hand sub-pixel value interpolation that is performed. In other cases, where the microprocessor performing the video encoding operation has limited processing capacity, e.g. the number of operations per second that can be executed is comparatively low, it is more appropriate to restrict the amount of on-demand sub-pixel value interpolation that is performed. In a mobile communications environment, for example, when video encoding and decoding functionality is incorporated in a mobile telephone or similar wireless terminal for communication with a mobile telephone network, both memory and processing power may be limited. In this case a combination of before-hand and on-demand sub-pixel value interpolation may be the best choice to obtain an efficient implementation in the video encoder. In video decoder 800, use of before-hand sub-pixel value is generally not preferred, as it typically results in the calculation of many sub-pixel values that are not actually used in the decoding process. However, it should be appreciated that although different amounts of before-hand and on-demand interpolation can be used in the encoder and decoder in order to optimise the operation of each, both encoder and decoder can be implemented so as to use the same division between before-hand and on-demand sub-pixel value interpolation.

Although the foregoing description does not describe the construction of bi-directionally predicted frames (B-frames) in the encoder 700 and the decoder 800, it should be understood that in embodiments of the invention, such a capability may be provided. Provision of such capability is considered within the ability of one skilled in the art.

An encoder 700 or a decoder 800 according to the invention can be realised using hardware or software, or using a suitable combination of both. An encoder or decoder implemented in software may be, for example, a

Nokia Exhibit 2004, p. 70
Amazon.com v. Nokia
IPR2024-01141

separate program or a software building block that can be used by various programs. In the above description and in the drawings, the functional blocks are represented as separate units, but the functionality of these blocks can be implemented, for example, in one software program unit.

The encoder 700 and decoder 800 can further be combined in order to form a video codec having both encoding and decoding functionality. In addition to being implemented in a multimedia terminal, such a codec may also be implemented in a network. A codec according to the invention may be a computer program or a computer program element, or it may be implemented at least partly using hardware.

The sub-pixel interpolation method used in the encoder 700 and decoder 800 according to the invention now be described in detail. The method will first be introduced at a general conceptual level and then two preferred embodiments will be described. In the first preferred embodiment, sub-pixel value interpolation is performed to ¼ pixel resolution and in the second the method is extended to ⅛ pixel resolution.

It should be noted that interpolation must produce identical values in the encoder and the decoder, but its implementation should be optimized for both entities separately. For example, in an encoder according to the first embodiment of the invention in which sub-pixel value interpolation is preformed to ¼ pixel resolution, it is most efficient to calculate ½ resolution pixels before-hand and to calculate values for ¼ resolution sub-pixels in an on-demand fashion, only when they are needed during motion estimation. This has the effect of limiting memory usage while keeping the computational complexity / burden at an acceptable level. In the decoder, on the other hand, it is advantageous not to pre-calculate any of the sub-pixels. Therefore, it should be appreciated that a preferred embodiment of the decoder does not include before-hand sub-pixel value interpolation.

Nokia Exhibit 2004, p. 71
Amazon.com v. Nokia
IPR2024-01141

block 845 and all sub-pixel value interpolation is performed in on-demand sub-pixel value interpolation block 890.

In the description of the interpolation method provided below, references are made to the pixel positions depicted in Figure 14a. In this figure pixels labelled A represent original pixels (that is, pixels residing at unit horizontal and vertical locations). Pixels labelled with other letters represent sub-pixels that are to be interpolated. The description that follows will adhere to the previously introduced conventions regarding the description of pixel and sub-pixel locations.

2005460 - 05-12-01

Next, the steps required to interpolate all sub-pixel positions are described:

Values for the ½ resolution sub-pixels labelled b are obtained by first calculating an intermediate value *b* using a Kth order filter, according to:

$$b = \sum_{i=1}^{K} \mathbf{x}_i \, \mathbf{A}_i \qquad (9)$$

where $\mathbf{x}_i$ is a vector of filter coefficients, $\mathbf{A}_i$ is a corresponding vector of original pixel values A situated at unit horizontal and unit vertical locations, and K is an integer which defines the order of the filter. Thus, equation 9 can be re-expressed as:

$$b = x_1 A_1 + x_2 A_2 + x_3 A_3 + ... + x_{K-1} A_{K-1} + x_K A_K \qquad (10)$$

The values of the filter coefficients x_i and the order of the filter K may vary from embodiment to embodiment. Equally, different coefficient values may be used in the calculation of different sub-pixels within an embodiment. In other embodiments, the values of filter coefficients x_i and the order of the filter may depend on which of the ½ resolution b sub-pixels is being

Nokia Exhibit 2004, p. 72
Amazon.com v. Nokia
IPR2024-01141

interpolated. Pixels A_i are disposed symmetrically with respect to the ½ resolution sub-pixel b being interpolated and are the closest neighbours of that sub-pixel. In the case of the ½ resolution sub-pixel b situated at half horizontal and unit vertical location, pixels A_i are disposed horizontally with respect to b (as shown in Figure 14b). If the ½ resolution sub-pixel b situated at unit horizontal and half vertical location is being interpolated, pixels A_i are disposed vertically with respect to b (as shown in Figure 14c).

A final value for ½ resolution sub-pixel b is calculated by dividing intermediate value *b* by a constant $scale_1$, truncating it to obtain an integer number and clipping the result to lie in the range $[0, 2^n-1]$. In alternative embodiments of the invention rounding may be performed instead of truncation. Preferably, constant $scale_1$ is chosen to be equal to the sum of filter coefficients x_i.

A value for the ½ resolution sub-pixel labelled c is also obtained by first calculating an intermediate value *c* using an Mth order filter, according to:

$$c = \sum_{i=1}^{M} \mathbf{y}_i \boldsymbol{b}_i \qquad (11)$$

where $\mathbf{y}_i$ is a vector of filter coefficients, $\boldsymbol{b}_i$ is a corresponding vector of intermediate values b_i in the horizontal or vertical direction. i.e.:

$$c = y_1 b_1 + y_2 b_2 + y_3 b_3 + ... + y_{M-1} b_{M-1} + y_M b_M \qquad (12)$$

The values of the filter coefficients y_i and the order of the filter M may vary from embodiment to embodiment. Equally, different coefficient values may be used in the calculation of different sub-pixels within an embodiment. Preferably, the *b* values are intermediate values for ½ resolution sub-pixels b which are disposed symmetrically with respect to ½ resolution sub-pixel c and are the closest neighbours of sub-pixel c. In an embodiment of the

Nokia Exhibit 2004, p. 73
Amazon.com v. Nokia
IPR2024-01141

invention, the ½ resolution sub-pixels b are disposed horizontally with respect to sub-pixel c, in an alternative embodiment they are disposed vertically with respect to sub-pixel c.

A final value of ½ resolution sub-pixel c is computed by dividing intermediate value *c* by a constant $scale_2$, truncating it to obtain an integer number and clipping the result to lie in the range $[0, 2^n-1]$. In alternative embodiments of the invention rounding may be performed instead of truncation. Preferably, constant $scale_2$ is equal to $scale_1 * scale_1$.

It should be noted that the use of intermediate values *b* in the horizontal direction leads to the same result as using intermediate values *b* in the vertical direction.

There are two alternatives for interpolating values for the ¼ resolution sub-pixels labelled h. Both involve linear interpolation along a diagonal line linking ½ resolution sub-pixels neighbouring the ¼ resolution sub-pixel h being interpolated. In a first embodiment, a value for sub-pixel h is calculated by averaging the values of the two ½ resolution sub-pixels b closest to sub-pixel h. In a second embodiment, a value for sub-pixel h is calculated by averaging the values of the closest pixel A and the closest ½ resolution sub-pixel c. It should be appreciated that this provides the possibility of using different combinations of diagonal interpolations to determine the values for sub-pixels h within the confines of different groups of 4 image pixels A. However, it should also be realised that the same combination should be used in both the encoder and the decoder in order to produce identical interpolation results. Figure 15 depicts 4 possible choices of diagonal interpolation for sub-pixels h in adjacent groups of 4 pixels within an image. Simulations in the TML environment have verified that both embodiments result in similar compression efficiency. The second embodiment has higher complexity, since calculation of sub-pixel c requires

Nokia Exhibit 2004, p. 74
Amazon.com v. Nokia
IPR2024-01141

calculation of several intermediate values. Therefore the first embodiment is preferred.

Values for ¼ resolution sub-pixels labelled d and g are calculated from the values of their nearest horizontal neighbours using linear interpolation. In other words, a value for ¼ resolution sub-pixel d is obtained by averaging values of its nearest horizontal neighbours, original image pixel A and ½ resolution sub-pixel b. Similarly, a value for ¼ resolution sub-pixel g is obtained by taking the average of its two nearest horizontal neighbours, ½ resolution sub-pixels b and c.

Values for ¼ resolution sub-pixels labelled e, f and i are calculated from the values of their nearest neighbours in the vertical direction using linear interpolation. More specifically, a value for ¼ resolution sub-pixel e is obtained by averaging the values of its two nearest vertical neighbours, original image pixel A and ½ resolution sub-pixel b. Similarly, a value for ¼ resolution sub-pixel f is obtained by taking the average of its two nearest vertical neighbours, ½ resolution sub-pixels b and c. In an embodiment of the invention, a value for ¼ resolution sub-pixel i is obtained in manner identical to that just described in connection with ¼ resolution sub-pixel f. However, in an alternative embodiment of the invention, and in common with the H.26 test models TML5 and TML6 previously described, ¼ resolution sub-pixel i is determined using the values of the four closest original image pixels, according to $(A_1+A_2+A_3+A_4+2) / 4$.

It should also be noted that in all cases where an average involving pixel and / or sub-pixel values is determined, the average may be formed in any appropriate manner. For example, the value for ¼ resolution sub-pixel d can be defined as d = (A + b) / 2 or as d = (A + b + 1) / 2. The addition of 1 to the sum of values for pixel A and ½ resolution sub-pixel b has the effect of causing any rounding or truncation operation subsequently applied to round

Nokia Exhibit 2004, p. 75
Amazon.com v. Nokia
IPR2024-01141

or truncate the value for d to the next highest integer value. This is true for any sum of integer values and may be applied to any of the averaging operations performed according to the method of the invention in order to control rounding or truncation effects.

It should be noted that the sub-pixel value interpolation method according to the invention provides advantages over each of TML5 and TML6.

In contrast to TML5, in which the values of some of the ¼ resolution sub-pixels depend on previously interpolated values obtained for other ¼ resolution sub-pixels, in the method according to the invention, all ¼ resolution sub-pixels are calculated from original image pixels or ½ resolution sub-pixel positions using linear interpolation. Thus, the reduction in precision of those ¼ resolution sub-pixel values which occurs in TML5 due to the intermediate truncation and clipping of the other ¼ resolution sub-pixels from which they are calculated, does not take place in the method according to the invention. In particular, referring to Figure 14a, ¼ resolution sub-pixels h (and sub-pixel i in one embodiment of the invention) are interpolated diagonally in order to reduce dependency on other ¼-pixels. Furthermore, in the method according to the invention, the number of calculations (and therefore the number of processor cycles) required to obtain a value for those ¼ resolution sub-pixels in the decoder is reduced compared with TML5. Additionally, the calculation of any ¼ resolution sub-pixel value requires a number of calculations which is substantially similar to the number of calculations required to determine any other ¼ resolution sub-pixel value. More specifically, in a situation where the required ½ resolution sub-pixel values are already available, e.g. they have been calculated before-hand, the number of calculations required to interpolate a ¼ resolution sub-pixel value from the pre-calculated ½ resolution sub-pixel values is the same as the number of calculations required to calculate any

Nokia Exhibit 2004, p. 76
Amazon.com v. Nokia
IPR2024-01141

other ¼ resolution sub-pixel value from the available ½ resolution sub-pixel values.

In comparison with TML6, the method according to the invention does not require high precision arithmetic to be used in the calculation of all sub-pixels. Specifically, as all of the ¼ resolution sub-pixel values are calculated from original image pixels or ½ resolution sub-pixel values using linear interpolation, lower precision arithmetic can be used in their interpolation. Consequently, in hardware implementations of the inventive method, for example in an ASIC (Application Specific Integrated Circuit), the use of lower precision arithmetic reduces the number of components (e.g. gates) that must be devoted to the calculation of ¼ resolution sub-pixel values. This, in turn, reduces the overall area of silicon that must be dedicated to the interpolation function. As the majority of sub-pixels are, in fact, ¼ resolution sub-pixels (12 out of the 15 sub-pixels illustrated in Figure 14a), the advantage provided by the invention in this respect is particularly significant. In software implementations, where sub-pixel interpolation is performed using the standard instruction set of a general purpose CPU (Central Processor Unit) or using a DSP (Digital Signal Processor), a reduction in the precision of the arithmetic required generally leads to an increase in the speed at which the calculations can be performed. This is particularly advantageous in 'low cost' implementations, in which it is desirable to use a general purpose CPU rather than any form of ASIC.

The method according to the invention provides still further advantages compared with TML5. As mentioned previously, in the decoder only 1 out of the 15 sub-pixel positions is required at any given time, namely that which is indicated by received motion vector information. Therefore, it is advantageous if the value of a sub-pixel in any sub-pixel location can be calculated with the minimum number of steps that result in a correctly interpolated value. The method according to the invention provides this

Nokia Exhibit 2004, p. 77
Amazon.com v. Nokia
IPR2024-01141

capability. As mentioned in the detailed description provided above, ½ resolution sub-pixel c can be interpolated by filtering in either the vertical or the horizontal direction, the same value being obtained for c regardless of whether horizontal or vertical filtering is used. The decoder can therefore take advantage of this property when calculating values for ¼ resolution sub-pixels f and g in such a way as to minimise the number of operations required in order to obtain the required values. For example, if the decoder requires a value for ¼ resolution sub-pixel f, ½ resolution sub-pixel c should interpolated in the vertical direction. If a value is required for ¼ resolution sub-pixel g, it is advantageous to interpolate a value for c in the horizontal direction. Thus, in general, it can be said that the method according to the invention provides flexibility in the way in which values are derived for certain ¼ resolution sub-pixels. No such flexibility is provided in TML5.

Two specific embodiments will now be described in detail. The first represents a preferred embodiment for calculating sub-pixels with up to ¼ pixel resolution, while in the second, the method according to the invention is extended to the calculation of values for sub-pixels having up to ⅛ pixel resolution. For both embodiments a comparison is provided between the computational complexity / burden resulting from use of the method according to the invention and that which would result from use of the interpolation methods according to TML5 and TML6 in equivalent circumstances.

The preferred embodiment for interpolating sub-pixels at ¼ pixel resolution will be described with reference to Figures 14a, 14b and 14c. In the following, it will be assumed that all image pixels and final interpolated values for sub-pixels are represented with 8-bits.

Calculation of ½ resolution sub-pixels at i) half unit horizontal and unit vertical locations and ii) unit horizontal and half unit vertical locations.

Nokia Exhibit 2004, p. 78
Amazon.com v. Nokia
IPR2024-01141

1. A value for the sub-pixel at half unit horizontal and unit vertical location, that is ½ resolution sub-pixel b in Figure 14a, is obtained by first calculating intermediate value $b = (A_1 - 5A_2 + 20A_3 + 20A_4 - 5A_5 + A_6)$ using the values of the six pixels (A_1 to A_6) which are situated at unit horizontal and unit vertical locations in either the row or the column of pixels containing b and which are disposed symmetrically about b, as shown in Figures 14b and 14c. A final value for ½ resolution sub-pixel b is calculated as $(b + 16) / 32$ where the operator / denotes division with truncation. The result is clipped to lie in the range [0, 255].

Calculation of ½ resolution sub-pixels at half unit horizontal and half unit vertical locations.

2. A value for the sub-pixel at half unit horizontal and half unit vertical location, that is ½ resolution sub-pixel c in Figure 14a, is calculated as $c = (b_1 - 5b_2 + 20b_3 + 20b_4 - 5b_5 + b_6 + 512) / 1024$ using the intermediate values *b* for the six closest ½ resolution sub-pixels which are situated in either the row or the column of sub-pixels containing c and which are disposed symmetrically about c. Again, operator / denotes division with truncation and the result is clipped to lie in the range [0, 255]. As previously explained, using intermediate values *b* for ½ resolution sub-pixels b in the horizontal direction leads to the same result as using intermediate values *b* for ½ resolution sub-pixels b in the vertical direction. Thus, in an encoder according to the invention, the direction for interpolating ½ resolution sub-pixels b can be chosen according to a preferred mode of implementation. In a decoder according to the invention, the direction for interpolating sub-pixels b is chosen according to which, if any, ¼ resolution sub-pixels will be interpolated using the result obtained for ½ resolution sub-pixel c.

Calculation of ¼ resolution sub-pixels at i) quarter unit horizontal and unit vertical locations; ii) quarter unit horizontal and half unit vertical locations; iii)

Nokia Exhibit 2004, p. 79
Amazon.com v. Nokia
IPR2024-01141

unit horizontal and quarter unit vertical locations; and iv) half unit horizontal and quarter unit vertical locations.

3. Values for ¼ resolution sub-pixels d, situated at quarter unit horizontal and unit vertical locations are calculated according to d = (A + b) / 2 using the nearest original image pixel A and the closest ½ resolution sub-pixel b in the horizontal direction. Similarly, values for ¼ resolution sub-pixels g, situated at quarter unit horizontal and half unit vertical locations are calculated according to g = (b + c) / 2 using the two nearest ½ resolution sub-pixels in the horizontal direction. In a similar manner, values for ¼ resolution sub-pixels e, situated at unit horizontal and quarter unit vertical locations, are calculated according e = (A + b) / 2 using the nearest original image pixel A and the closest ½ resolution sub-pixel b in the vertical direction. Values for ¼ resolution sub-pixels f, situated at half unit horizontal and quarter unit vertical locations, are determined from f = (b + c) / 2 using the two nearest ½ resolution sub-pixel in the vertical direction. In all cases, operator / denotes division with truncation.

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Calculation of ¼ resolution sub-pixels at quarter unit horizontal and quarter unit vertical locations.

4. Values for ¼ resolution sub-pixels h, situated at quarter unit horizontal and quarter unit vertical locations are calculated according to $h = (b_1 + b_2) / 2$, using the two nearest ½ resolution sub-pixels b in the diagonal direction. Again, operator / denotes division with truncation.

5. A value for the ¼ resolution sub-pixel labeled i is computed from $i = (A_1 + A_2 + A_3 + A_4 + 2) / 4$ using the four nearest original pixels A. Once more, operator / denotes division with truncation.

An analysis of the computational complexity of the first preferred embodiment of the invention will now be presented.

Nokia Exhibit 2004, p. 80
Amazon.com v. Nokia
IPR2024-01141

In the encoder, it is likely that the same sub-pixel values will be calculated multiple times. Therefore, and as previously explained, the complexity of the encoder can be reduced by pre-calculating all sub-pixel values and storing them in memory. However, this solution increases memory usage by a large margin. In the preferred embodiment of the invention, in which motion vector accuracy is ¼ pixel resolution in both the horizontal and vertical dimensions, storing pre-calculated sub-pixel values for the whole image requires 16 times the memory required to store the original, non-interpolated image. To reduce memory usage, all ½ resolution sub-pixels can be interpolated before-hand and ¼ resolution sub-pixels can be calculated on-demand, that is, only when they are needed. According to the method of the invention, on-demand interpolation of values for ¼ resolution sub-pixels only requires linear interpolation from ½ resolution sub-pixels. Four times the original picture memory is required to store the pre-calculated ½ resolution sub-pixels since only 8 bits are necessary to represent them.

However, if the same strategy of pre-calculating all ½ resolution sub-pixels using before-hand interpolation is used in conjunction with the direct interpolation scheme of TML6, the memory requirements increase to 9 times the memory required to store the original non-interpolated image. This results from the fact that a larger number of bits is required to store the high precision intermediate values associated with each ½ resolution sub-pixel in TML6. In addition, the complexity of sub-pixel interpolation during motion estimation is higher in TML6, since scaling and clipping has to be performed for every ½ and ¼ sub-pixel location.

In the following, the complexity of the sub-pixel value interpolation method according to the invention, when applied in a video decoder, is compared with that of the interpolation schemes used in TML5 and TML6. Throughout

Nokia Exhibit 2004, p. 81
Amazon.com v. Nokia
IPR2024-01141

the analysis which follows, it is assumed that in each method the interpolation of any sub-pixel value is performed using only the minimum number of steps required to obtain a correctly interpolated value. It is further assumed that each method is implemented in a block based manner, that is, intermediate values common for all the sub-pixels to be interpolated in a particular N x M block are calculated only once. An illustrative example is provided in Figure 16. Referring to Figure 16, it can be seen that in order to calculate a 4 x 4 block of ½ resolution sub-pixels c, a 9 x 4 block of ½ resolution sub-pixels b is first calculated.

Compared with the sub-pixel value interpolation method used in TML5, the method according to the invention has a lower computational complexity for the following reasons:

1. Unlike the sub-pixel value interpolation scheme used in TML5, according to the method of the invention, a value for ½ resolution sub-pixel c can be obtained by filtering in either the vertical or the horizontal direction. Thus, in order to reduce the number of operations, ½ resolution sub-pixel c can be interpolated in the vertical direction if a value for ¼ resolution sub-pixel f is required and in the horizontal direction if a value for ¼ resolution sub-pixel pixel g is required. As an example, Figure 17 shows all the ½ resolution sub-pixel values that must be calculated in order to interpolate values for ¼ resolution sub-pixels g in an image block defined by 4 x 4 original image pixels using the interpolation method of TML5 (Figure 17a) and using the method according to the invention (Figure 17b). In this example, the sub-pixel value interpolation method according to TML5 requires a total of 88 ½ resolution sub-pixels to be interpolated, while the method according to the invention requires the calculation of 72 ½ resolution sub-pixels. As can be seen from Figure 17b, according to the invention, ½ resolution

Nokia Exhibit 2004, p. 82
Amazon.com v. Nokia
IPR2024-01141

sub-pixels c are interpolated in the horizontal direction in order to reduce the number of calculations required.

2. According to the method of the invention, ¼ resolution sub-pixel h is calculated by linear interpolation from its two closest neighbouring ½ resolution sub-pixels in the diagonal direction. The respective numbers of ½ resolution sub-pixels that must be calculated in order to obtain values for ¼ resolution sub-pixels h within a 4 x 4 block of original image pixels using the sub-pixel value interpolation method according to TML5 and the method according to the invention are shown in Figures 18(a) and 18(b), respectively. Using the method according to TML5 it is necessary to interpolate a total of 56 ½ resolution sub-pixels, while according to the method of the invention it is necessary to interpolate 40 ½ resolution sub-pixels.

Table 1 summarizes the decoder complexities of the three sub-pixel value interpolation methods considered here, that according to TML5, the direct interpolation method used in TML6 and the method according to the invention. Complexity is measured in terms of the number of 6-tap filtering and linear interpolation operations performed. It is assumed that Interpolation of ¼ resolution sub-pixel i is calculated according to $i = (A_1 + A_2 + A_3 + A_4 + 2) / 4$ which is bilinear interpolation and effectively comprises two linear interpolation operations. The operations needed to interpolate sub-pixel values with one 4 x 4 block of original image pixels are listed for each of the 15 sub-pixel positions which, for convenience of reference, are numbered according to the scheme shown in Figure 19. Referring to Figure 19, location 1 is the location of an original image pixel A and locations 2 to16 are sub-pixel locations. Location 16 is the location of ¼ resolution sub-pixel i. In order to compute the average number of operations it has been assumed that the probability of a motion vector pointing to each sub-pixel position is the same. The average complexity is therefore the averaged of the

Nokia Exhibit 2004, p. 83
Amazon.com v. Nokia
IPR2024-01141

15 sums calculated for each sub-pixel location and the single full-pixel location.

	TML5		TML6		Inventive Method	
Location	linear.	6-tap	linear.	6-tap	linear.	6-tap
1	0	0	0	0	0	0
3,9	0	16	0	16	0	16
2,4,5,13	16	16	0	16	16	16
11	0	52	0	52	0	52
7,15	16	52	0	52	16	52
10,12	16	68	0	52	16	52
6,8,14	48	68	0	52	16	32
16	32	0	32	0	32	0
Average	**19**	**37**	**2**	**32**	**13**	**28.25**

Table 1: Complexity of ¼ resolution sub-pixel interpolation in TML5, TML6 and the method according to the invention.

It can be seen from Table 1 that the method according to the invention requires fewer 6-tap filter operations than the sub-pixel value interpolation method according to TML6 and only a few additional linear interpolation operations. Since 6-tap filter operations are much more complex than linear interpolation operations the complexity of the two methods is similar. The sub-pixel value interpolation method according to TML5 has a considerably higher complexity.

The preferred embodiment for interpolating sub-pixels with up to ⅛ pixel resolution will now be described with reference to Figures 20, 21 and 22.

Figure 20 presents the nomenclature used to describe pixels, ½ resolution sub-pixels, ¼ resolution sub-pixels and ⅛ resolution sub-pixels in this extended application of the method according to the invention.

1. Values for the ½ resolution and ¼ resolution sub-pixels labelled b^1, b^2 and b^3 in Figure 20 are obtained by first calculating intermediate values

Nokia Exhibit 2004, p. 84
Amazon.com v. Nokia
IPR2024-01141

$b^1 = (-3A_1 + 12A_2 - 37A_3 + 229A_4 + 71A_5 - 21A_6 + 6A_7 - A_8)$; $b^2 = (-3A_1 + 12A_2 - 39A_3 + 158A_4 + 158A_5 - 39A_6 + 12A_7 - 3A_8)$; and $b^3 = (-A_1 + 6A_2 - 21A_3 + 71A_4 + 229A_5 - 37A_6 + 13A_7 - 3A_8)$ using the values of the eight nearest image pixels (A_1 to A_8) situated at unit horizontal and unit vertical locations in either the row or the column containing b^1, b^2 and b^3 and disposed symmetrically about ½ resolution sub-pixel b^2. The asymmetries in the filter coefficients used to obtain intermediate values b^1 and b^3 account for the fact that pixels A_1 to A_8 are not symmetrically located with respect to ¼ resolution sub-pixels b^1 and b^3. Final values for sub-pixels b^i, i=1, 2, 3 are calculated according to $b^i = (b^i + 128) / 256$ where the operator / denotes division with truncation. The result is clipped to lie in the range [0, 255].

2. Values for the ½ resolution and ¼ resolution sub-pixels labelled c^{ij}, i, j = 1, 2, 3, are calculated according to $c^{1j} = (-3b_1^j + 12b_2^j - 37b_3^j + 229b_4^j + 71b_5^j - 21b_6^j + 6b_7^j - b_8^j + 32768) / 65536$, $c^{2j} = (-3b_1^j + 12b_2^j - 39b_3^j + 158b_4^j + 158b_5^j - 39b_6^j + 12b_7^j - 3b_8^j + 32768) / 65536$ and $c^{3j} = (-b_1^j + 6b_2^j - 21b_3^j + 71b_4^j + 229b_5^j - 37b_6^j + 13b_7^j - 3b_8^j + 32768) / 65536$ using the intermediate values b^1, b^2 and b^3 calculated for the eight closest sub-pixels (b_1^j to b_8^j) in the vertical direction, sub-pixels b^j being situated in the column comprising the ½ resolution and ¼ resolution sub-pixels c^{ij} being interpolated and disposed symmetrically about the ½ resolution sub-pixel c^{2j}. The asymmetries in the filter coefficients used to obtain values for sub-pixels c^{1j} and c^{3j} account for the fact that sub-pixels b_1^j to b_8^j are not symmetrically located with respect to ¼ resolution sub-pixels c^{1j} and c^{3j}. Once more, operator / denotes division with truncation. Before the interpolated values for sub-pixels c^{ij} are stored in the frame memory they are clipped to lie in the range [0, 255]. In an alternative embodiment of the invention, ½ resolution and ¼ resolution sub-pixels c^{ij}

Nokia Exhibit 2004, p. 85
Amazon.com v. Nokia
IPR2024-01141

are calculated using in an analogous manner using intermediate values b^1, b^2 and b^3 in the horizontal direction.

3. Values for ⅛ resolution sub-pixels labelled d are calculated using linear interpolation from the values of their closest neighbouring image pixel, ½ resolution or ¼ resolution sub-pixels in the horizontal or vertical direction. For example, upper leftmost ⅛ resolution sub-pixel d is calculated according to $d = (A + b^1 + 1) / 2$. As before, operator / indicates division with truncation.

4. Values for ⅛ resolution sub-pixels labelled e and f are calculated using linear interpolation from the values of image pixels, ½ resolution or ¼ resolution sub-pixels in the diagonal direction. For example, referring to Figure 20, upper leftmost pixel ⅛ resolution sub-pixel e is calculated according to $e = (b^1 + b^1 + 1) / 2$. The diagonal direction to be used in the interpolation of each ⅛ resolution sub-pixel in a first preferred embodiment of the invention, hereinafter referred to as 'preferred method 1', is indicated in Figure 21(a). Values for ⅛ resolution sub-pixels labelled g are calculated according to $g = (A + 3c^{22} + 3) / 4$. As always, operator / denotes division with truncation. In an alternative embodiment of the invention, hereinafter referred to as 'preferred method 2', computational complexity is further reduced by interpolating ⅛ resolution sub-pixels f using linear interpolation from ½ resolution sub-pixels b^2, that is, according to the relationship $f = (3b^2 + b^2 + 2) / 4$. The b^2 sub-pixel which is closer to f is multiplied by 3. The diagonal interpolation scheme used in this alternative embodiment of the invention is depicted in Figure 21(b). In further alternative embodiments, different diagonal interpolation schemes can be envisaged.

Nokia Exhibit 2004, p. 86
Amazon.com v. Nokia
IPR2024-01141

It should be noted that in all cases where an average involving pixel and / or sub-pixel values is used in the determination of ⅛ resolution sub-pixels, the average may be formed in any appropriate manner. The addition of 1 to the sum of values used in calculating such an average has the effect of causing any rounding or truncation operation subsequently applied to round or truncate the average in question to the next highest integer value. In alternative embodiments of the invention, the addition of 1 is not used.

As in the case of sub-pixel value interpolation to ¼ pixel resolution previously described, memory requirements in the encoder can be reduced by pre-calculating only a part of the sub-pixel values to be interpolated. In the case of sub-pixel value interpolation to ⅛ pixel resolution, it is advantageous to calculate all ½ resolution and ¼ resolution sub-pixels before-hand and to compute values for ⅛ resolution sub-pixels in an on-demand fashion, only when they are required. When this approach is taken, both the interpolation method according to TML5 and that according to the invention require 16 times the original picture memory to store the ½ resolution and ¼ resolution sub-pixel values. However, if the direct interpolation method according to TML6 is used in the same way, intermediate values for the ½ resolution and ¼ pixel resolution sub-pixels must be stored. These intermediate values are represented with 32-bit precision and this results in a memory requirement 64 times that for the original, non-interpolated image.

In the following, the complexity of the sub-pixel value interpolation method according to the invention, when applied in a video decoder to calculate values for sub-pixels at up to ⅛ pixel resolution, is compared with that of the interpolation schemes used in TML5 and TML6. As in the equivalent analysis for ¼ pixel resolution sub-pixel value interpolation described above, it is assumed that in each method the interpolation of any sub-pixel value is performed using only the minimum number of steps required to obtain a

Nokia Exhibit 2004, p. 87
Amazon.com v. Nokia
IPR2024-01141

correctly interpolated value. It is also assumed that each method is implemented in a block based manner, such that intermediate values common for all the sub-pixels to be interpolated in a particular N x M block are calculated only once.

Table 2 summarizes complexities of the three interpolation methods. Complexity is measured in terms of the number of 8-tap filter and linear interpolation operations performed in each method. The table presents the number of operations required to interpolate each of the 63 ⅛ resolution sub-pixels within one 4 x 4 block of original image pixels, each sub-pixel location being identified with a corresponding number, as illustrated in Figure 22. In Figure 22, location 1 is the location of an original image pixel and locations 2 to 64 are sub-pixel locations. When computing the average number of operations, it has been assumed that the probability of a motion vector pointing to each sub-pixel position is the same. The average complexity is thus the average of the 63 sums calculated for each sub-pixel location and the single full-pixel location.

	TML5		TML6		Preferred Method 1		Preferred Method 2	
Location	linear.	8-tap	linear.	8-tap	linera.	8-tap	linear.	8-tap
1	0	0	0	0	0	0	0	0
3,5,7,17,33,49	0	16	0	16	0	16	0	16
19,21,23,35,37,39, 51,53,55	0	60	0	60	0	60	0	60
2,8,9,57	16	16	0	16	16	16	16	16
4,6,25,41	16	32	0	16	16	32	16	32
10,16,58,64	32	76	0	60	16	32	16	32
11,13,15,59,61,63	16	60	0	60	16	60	16	60
18,24,34,40,50,56	16	76	0	60	16	60	16	60
12,14,60,62	32	120	0	60	16	32	16	32
26,32,42,48	32	108	0	60	16	32	16	32

Nokia Exhibit 2004, p. 88
Amazon.com v. Nokia
IPR2024-01141

20,22,36,38,52,54	16	120	0	60	16	76	16	76
27,29,31,43,45,47	16	76	0	60	16	76	16	76
28,30,44,46	32	152	0	60	16	60	16	60
Average	**64**	**290.25**	**0**	**197.75**	**48**	**214.75**	**48**	**192.75**

Table 2: Complexity of ⅛ resolution sub-pixel interpolation in TML5, TML6 and the method according to the invention. (Results shown separately for Preferred Method 1 and Preferred Method 2).

As can be seen from Table 2, the number of 8-tap filtering operations performed according to preferred methods 1 and 2 are, respectively, 26% and 34% lower than the number of 8-tap filtering operation performed in the sub-pixel value interpolation method of TML5. The number of linear operations is 25% lower, in both preferred method 1 and preferred method 2, compared with TML5, but this improvement is of lesser importance compared to the reduction in 8-tap filtering operations. It can further be seen that the direct interpolation method used in TML6 has a complexity comparable that of both preferred methods 1 and 2 when used to interpolate values for ⅛ resolution sub-pixels.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention. While a number of preferred embodiments of the invention have been described in detail, it should be apparent that many modifications and variations thereto are possible, all of which fall within the true spirit and scope of the invention.

Nokia Exhibit 2004, p. 89
Amazon.com v. Nokia
IPR2024-01141

CLAIMS

1. A method of interpolation in video coding in which an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, is interpolated to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$, where x is a positive integer having a maximum value N, the method comprising:

a) when values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations are required, interpolating such values directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) when values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations are required, interpolating such values directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) when a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location is required, interpolating such a value by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

2. A method according to claim 1 wherein a first and a second weight are used in the weighted average referred to in (c), the relative magnitudes of the weights being inversely proportional to the (straight-line diagonal)

Nokia Exhibit 2004, p. 90
Amazon.com v. Nokia
IPR2024-01141

proximity of the first and the second sub-pixel or pixel to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

3. A method according to claim 2, wherein in a situation where the first and the second sub-pixel or pixel are symmetrically located with respect to (equidistant from) the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location, the first and second weights have equal values.

4. A method according to claim 1 in which the first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations in step b) is used when a sub-pixel at $1/2^{N-1}$ unit horizontal and $1/2^N$ unit vertical location is required.

5. A method according to claim 1 in which the second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations in step b) is used when a sub-pixel at $1/2^N$ unit horizontal and $1/2^{N-1}$ unit vertical location is required.

6. A method according to claim 1 in which, when values for sub-pixels at $1/2^N$ unit horizontal and unit vertical locations, and $1/2^N$ horizontal and $1/2^{N-1}$ vertical locations are required, interpolating such values by taking the average of the values of a first pixel or sub-pixel located at a vertical location corresponding to that of the sub-pixel being calculated and unit horizontal location and a second pixel or sub-pixel located at a vertical location corresponding to that of the sub-pixel being calculated and $1/2^{N-1}$ unit horizontal location.

7. A method according to claim 1 in which, when values for sub-pixels at unit horizontal and $1/2^N$ unit vertical locations, and $1/2^{N-1}$ unit horizontal and $1/2^N$ unit vertical locations are required, interpolating such values by taking the average of the values of a first pixel or sub-pixel located at a horizontal location corresponding to that of the sub-pixel being calculated and unit

Nokia Exhibit 2004, p. 91
Amazon.com v. Nokia
IPR2024-01141

vertical location and a second pixel or sub-pixel located at a horizontal location corresponding to that of the sub-pixel being calculated and $1/2^{N-1}$ unit vertical location.

8. A method according to claim 1 in which values for sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are interpolated by taking the average of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

9. A method according to claim 1 in which values for sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are interpolated by taking the average of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location.

10. A method according to claim 1 in which values for half of the sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are interpolated by taking the average of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and values for the other half of the sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are interpolated by taking the average of a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

11. A method according to claim 10 in which values for sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are alternately interpolated for one such sub-pixel by taking the average of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and values and for a neighbouring such sub-pixel by taking the average of a second

Nokia Exhibit 2004, p. 92
Amazon.com v. Nokia
IPR2024-01141

pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

12. A method according to claim 11 in which the sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are alternately interpolated in a horizontal direction.

13. A method according to claim 11 in which the sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are alternately interpolated in a horizontal direction.

14. A method according to claim 1 in which when values for some sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations are required, such values are interpolated by taking the average of a plurality of nearest neighbouring pixels.

15. A method according to claim 1 in which N equals an integer selected from a list consisting of the values 2, 3, and 4.

16. A method according to claim 1 in which in at least one of step a) and step b) interpolating sub-pixel values directly using weighted sums involves the calculation of an intermediate value for the sub-pixel values having a dynamic range greater than the specified dynamic range.

17. A method according to claim 14 in which the intermediate value for a sub-pixel having $1/2^{N-1}$ sub-pixel resolution is used the calculation of a sub-pixel value having $1/2^N$ sub-pixel resolution.

18. A method of interpolation in video coding in which an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal

Nokia Exhibit 2004, p. 93
Amazon.com v. Nokia
IPR2024-01141

locations and the pixels in the columns residing at unit vertical locations, is interpolated to generate values for sub-pixels at fractional horizontal and vertical locations, the method comprising:

a) when values for sub-pixels at half unit horizontal and unit vertical locations, and unit horizontal and half unit vertical locations are required, interpolating such values directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) when values for sub-pixels at half unit horizontal and half unit vertical locations are required, interpolating such values directly using a weighted sum of values for sub-pixels residing at half unit horizontal and unit vertical locations calculated according to step (a); and

c) when values for sub-pixels at quarter unit horizontal and quarter unit vertical locations are required, interpolating such values by taking the average of at least one pair of a first pair of values of a sub-pixel located at a half unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and half unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a half unit horizontal and half unit vertical location.

19. A method of interpolation in video coding in which an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, is interpolated to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$ where x is a positive integer having a maximum value N, the method comprising:

a) when values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations are required, interpolating such values directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) when a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required, interpolating such a value directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

20. A method according to claim 1 in which the sub-pixels used in the first weighted sum are sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and the first weighted sum is used to interpolate a value for a sub-pixel at $1/2^{N-1}$ unit horizontal and $1/2^{N}$ unit vertical location.

21. A method according to claim 1 in which the sub-pixels used in the second weighted sum are sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations and the second weighted sum is used to interpolate a value for a sub-pixel at $1/2^{N}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

22. A method according to claim 1 in which when values for sub-pixels at $1/2^{N}$ unit horizontal and $1/2^{N}$ unit vertical locations are required, they are interpolated by taking the average of at least one pair of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

23. A video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical

Nokia Exhibit 2004, p. 95
Amazon.com v. Nokia
IPR2024-01141

locations being defined according to 1/2x, where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) interpolate a value for a sub-pixel situated at a $1/2^{N}$ unit horizontal and $1/2^{N}$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^{N}$ unit horizontal and $1/2^{N}$ vertical location.

24. A video coder according to claim 23, comprising a video encoder.

25. A video encoder according to claim 23, comprising a video decoder.

26. A codec comprising the video encoder of claim 24 and the video decoder of claim 25.

27. A communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit

Nokia Exhibit 2004, p. 96
Amazon.com v. Nokia
IPR2024-01141

vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$, where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) interpolate a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

28. A communications terminal according to claim 27 comprising a video encoder.

29. A communications terminal according to claim 27 comprising a video decoder.

30. A communications terminal according to claim 27 having a video codec comprising a video encoder and a video decoder.

Nokia Exhibit 2004, p. 97
Amazon.com v. Nokia
IPR2024-01141

31. A telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the communications terminal comprising a video coder for coding for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$, where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) interpolate a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

Nokia Exhibit 2004, p. 98
Amazon.com v. Nokia
IPR2024-01141

32. A telecommunications system according to claim 31 which is a mobile telecommunications system comprising a mobile communications terminal and a wireless network, the connection between the mobile communications terminal and the wireless network being formed by a radio link.

33. A telecommunications system according to claim 31 in which the network enables the communications terminal to communicate with other communications terminals connected to the network over communications links between the other communications terminals and the network.

34. A telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the network comprising a video coder for coding for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$, where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

Nokia Exhibit 2004, p. 99
Amazon.com v. Nokia
IPR2024-01141

c) interpolate a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

35. A video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

36. A video coder according to claim 35 in which the interpolator is further adapted to form the first weighted sum using the values of sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and to use the first weighted sum to interpolate a value for a sub-pixel at $1/2^{N-1}$ unit horizontal and $1/2^N$ unit vertical location.

Nokia Exhibit 2004, p. 100
Amazon.com v. Nokia
IPR2024-01141

37. A video coder according to claim 35 in which the interpolator is further adapted to form the second weighted sum using the values of sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations and to use the second weighted sum to interpolate a value for a sub-pixel at $1/2^{N}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

38. A method according to claim 35 in which the interpolator is further adapted to interpolate values for sub-pixels at $1/2^{N}$ unit horizontal and $1/2^{N}$ unit vertical locations by taking the average of at least one pair of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

39. A video coder according to claim 35, comprising a video encoder.

40. A video encoder according to claim 35, comprising a video decoder.

41. A codec comprising the video encoder of claim 39 and the video decoder of claim 40.

42. A communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

Nokia Exhibit 2004, p. 101
Amazon.com v. Nokia
IPR2024-01141

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

43. A communications terminal according to claim 42 comprising a video encoder.

44. A communications terminal according to claim 42 comprising a video decoder.

45. A communications terminal according to claim 42 having a video codec comprising a video encoder and a video decoder.

46. A telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

Nokia Exhibit 2004, p. 102
Amazon.com v. Nokia
IPR2024-01141

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

47. A telecommunications system according to claim 46 which is a mobile telecommunications system comprising a mobile communications terminal and a wireless network, the connection between the mobile communications terminal and the wireless network being formed by a radio link.

48. A telecommunications system according to claim 46 in which the network enables the communications terminal to communicate with other communications terminals connected to the network over communications links between the other communications terminals and the network.

49. A telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the network comprising a video coder for coding for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

Nokia Exhibit 2004, p. 103
Amazon.com v. Nokia
IPR2024-01141

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location is required directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

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Nokia Exhibit 2004, p. 104
Amazon.com v. Nokia
IPR2024-01141

ABSTRACT

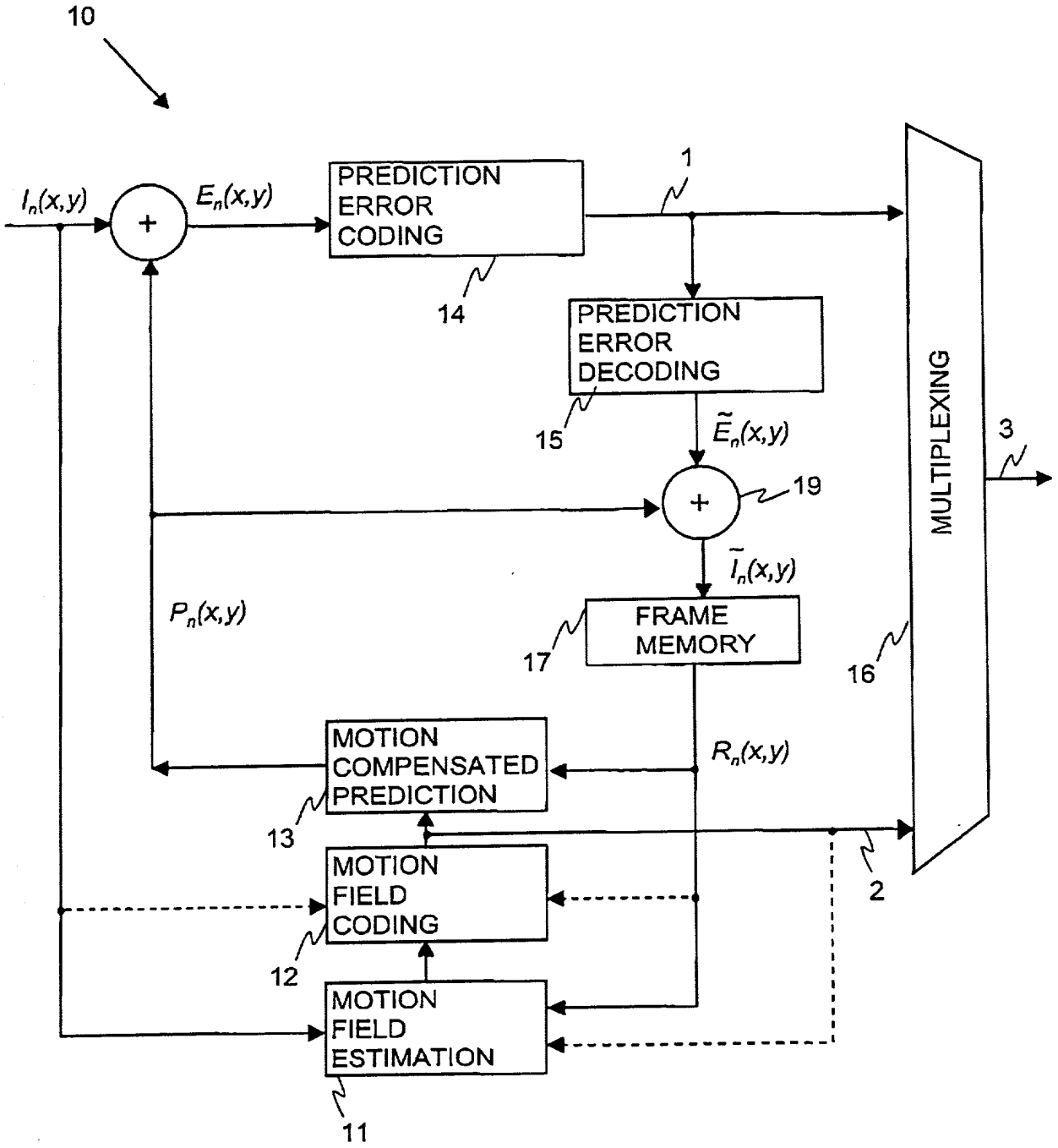
A method of interpolation in video coding in which an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, is interpolated to generate values for sub-pixels at fractional horizontal and vertical locations, the method comprising:

a) when values for sub-pixels at half unit horizontal and unit vertical locations, and unit horizontal and half unit vertical locations are required, interpolating such values directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) when values for sub-pixels at half unit horizontal and half unit vertical locations are required, interpolating such values directly using a weighted sum of values for sub-pixels residing at half unit horizontal and unit vertical locations calculated according to step (a); and

c) when values for sub-pixels at quarter unit horizontal and quarter unit vertical locations are required, interpolating such values by taking the average of at least one pair of a first pair of values of a sub-pixel located at a half unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and half unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a half unit horizontal and half unit vertical location.

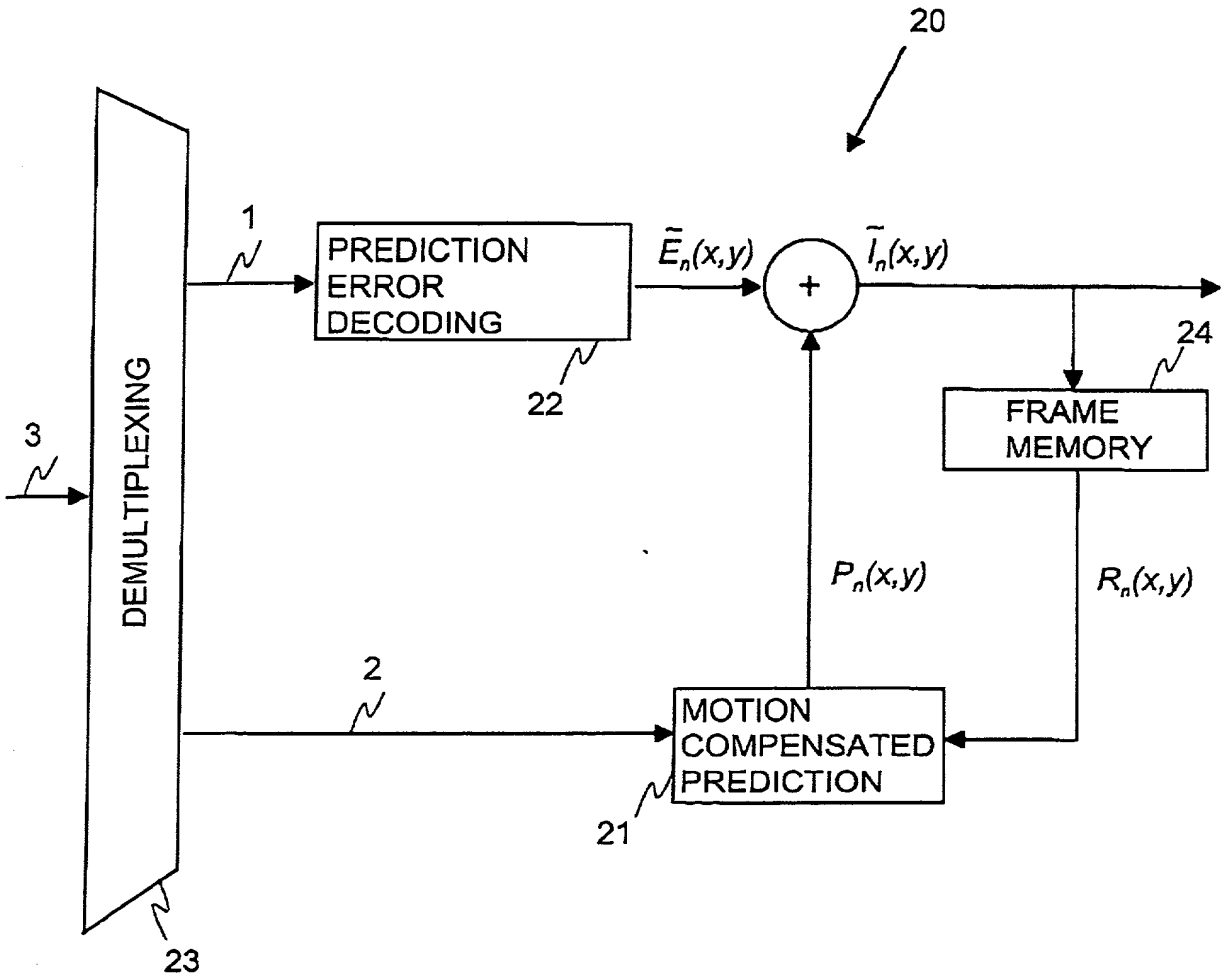
Nokia Exhibit 2004, p. 105
Amazon.com v. Nokia
IPR2024-01141



PRIOR ART

Fig. 1

Nokia Exhibit 2004, p. 106
Amazon.com v. Nokia
IPR2024-01141



PRIOR ART

Fig. 2

Nokia Exhibit 2004, p. 107
Amazon.com v. Nokia
IPR2024-01141

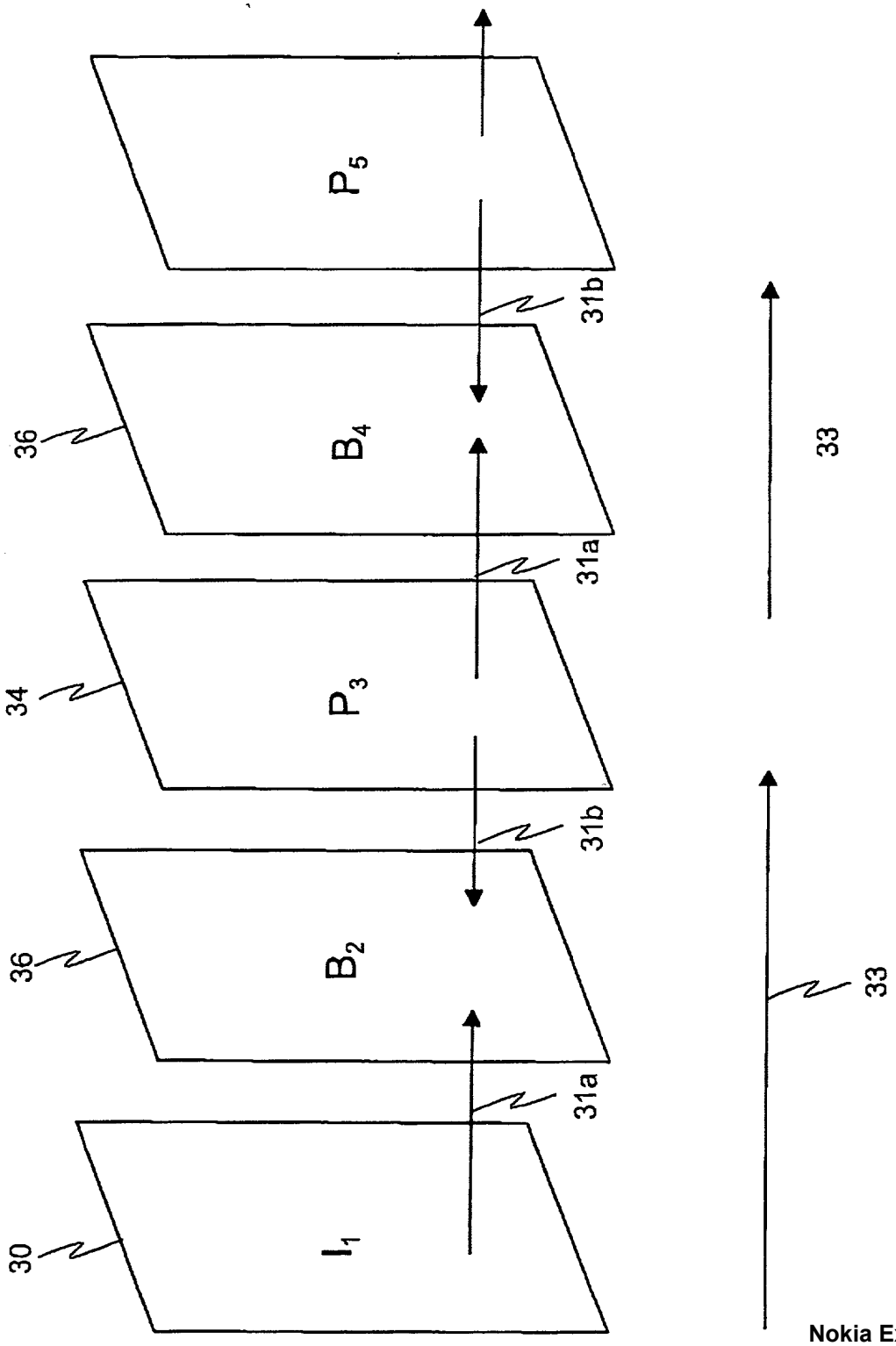
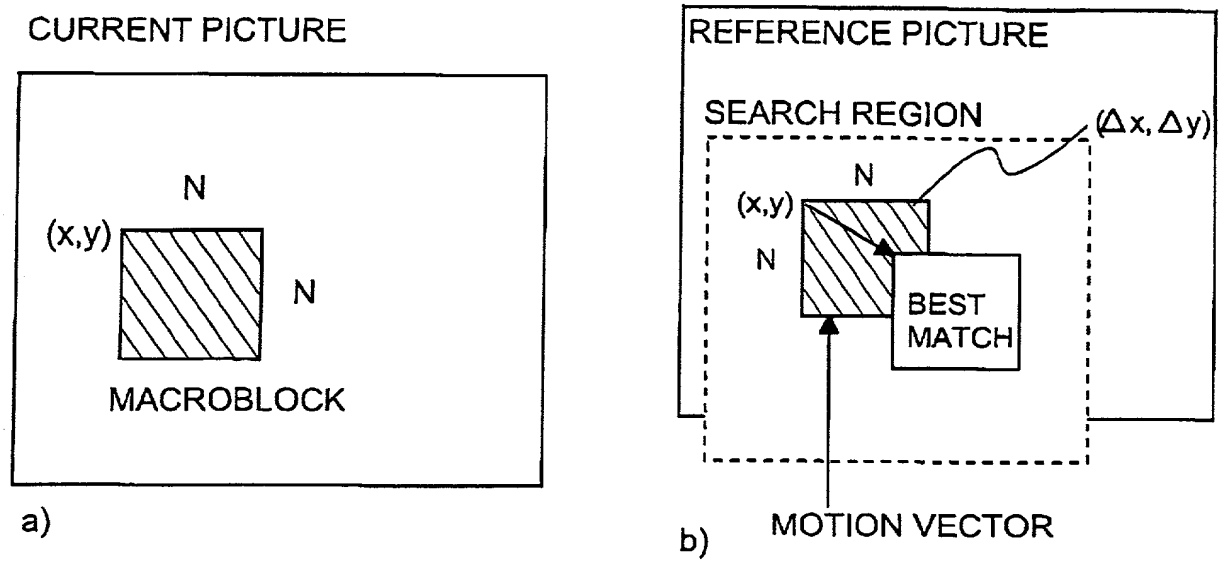


Fig. 3

Nokia Exhibit 2004, p. 108
Amazon.com v. Nokia
IPR2024-01141



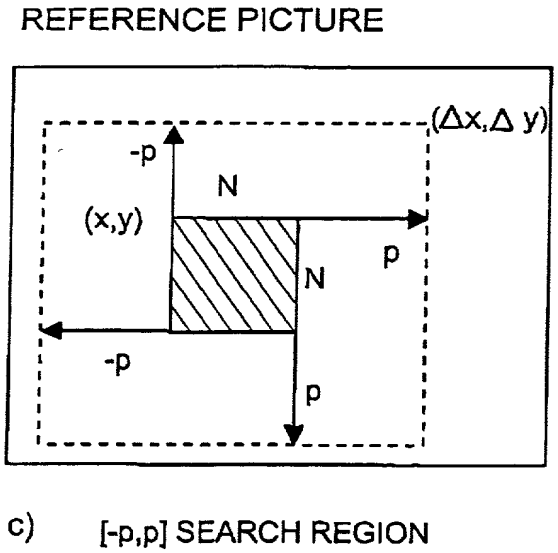


Fig. 4

Nokia Exhibit 2004, p. 109
Amazon.com v. Nokia
IPR2024-01141

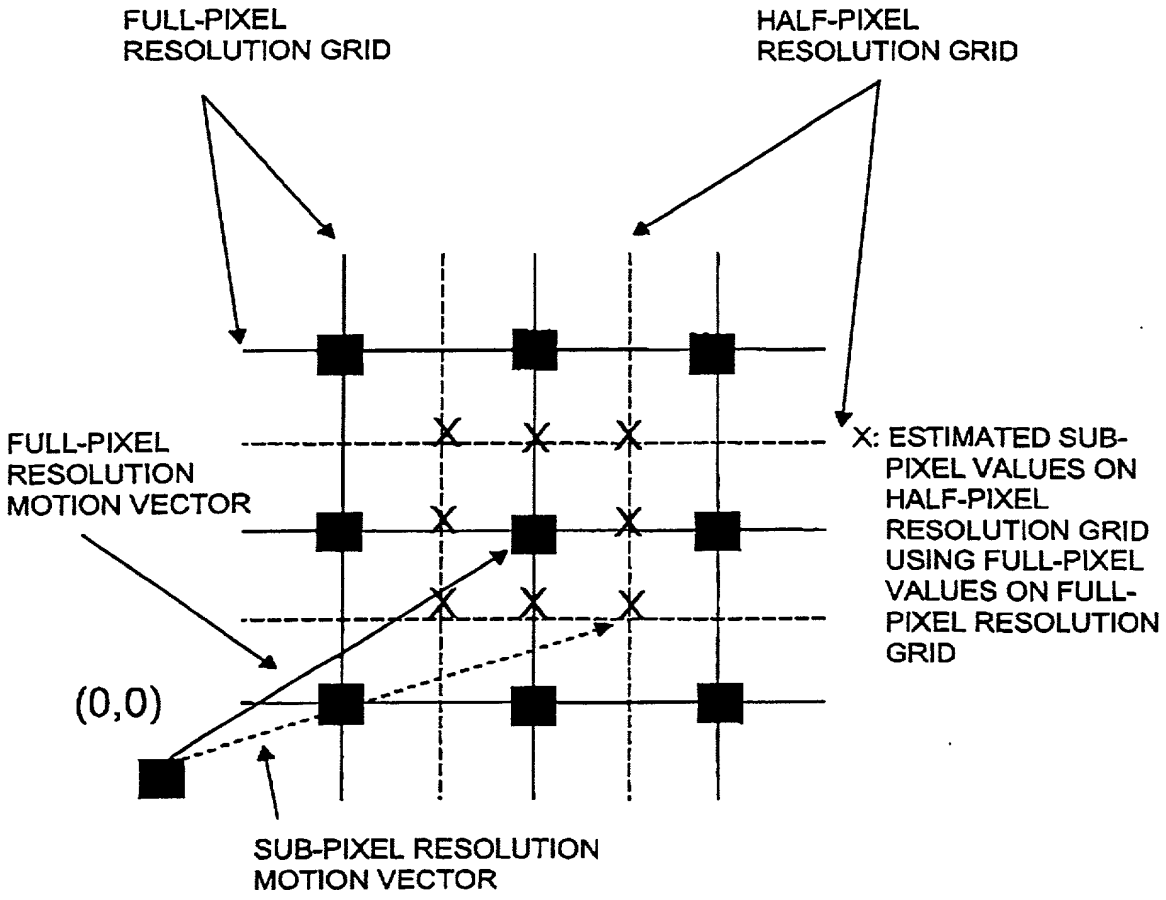


Fig. 5

Nokia Exhibit 2004, p. 110
Amazon.com v. Nokia
IPR2024-01141

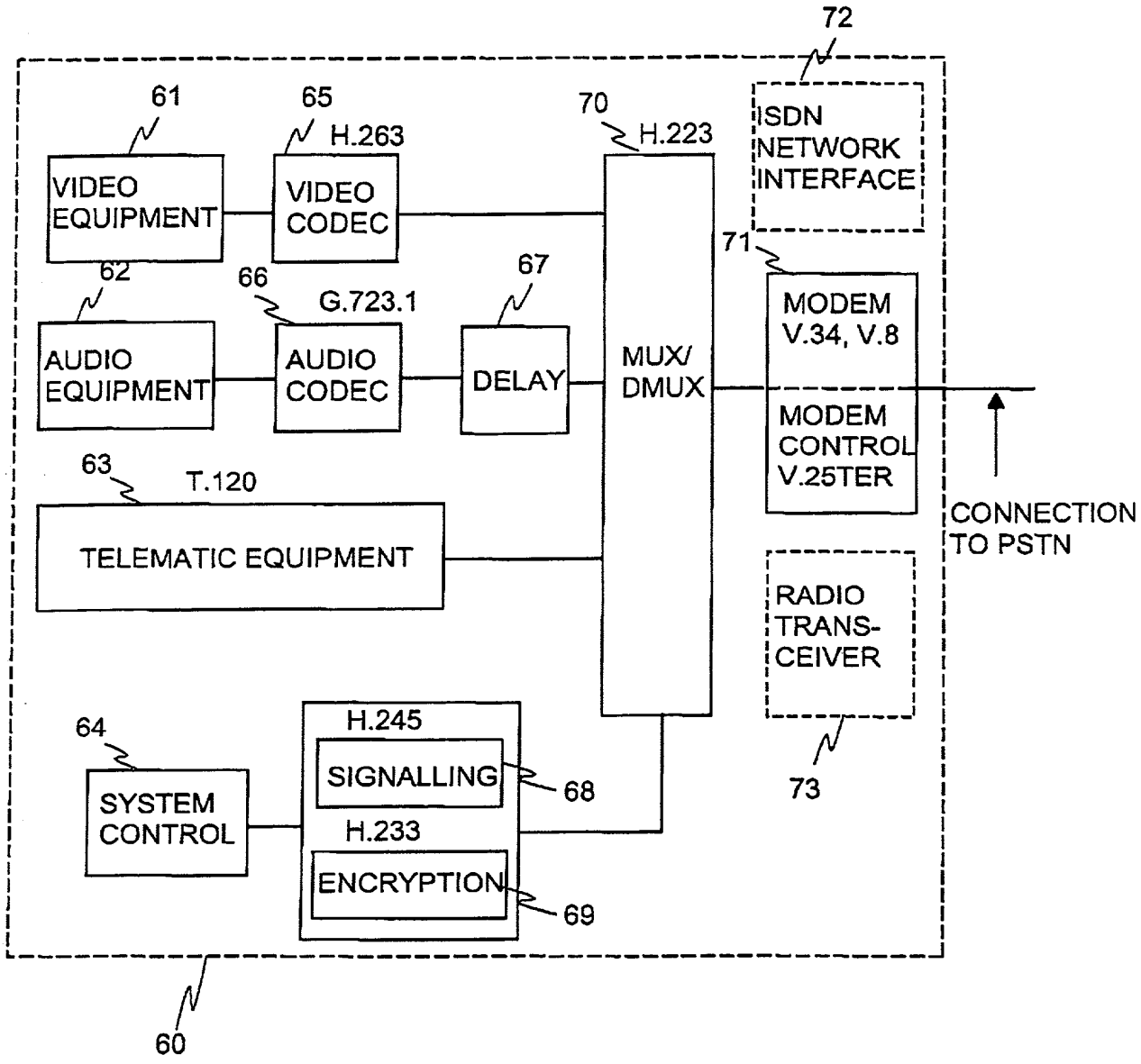


Fig. 6

Nokia Exhibit 2004, p. 111
Amazon.com v. Nokia
IPR2024-01141

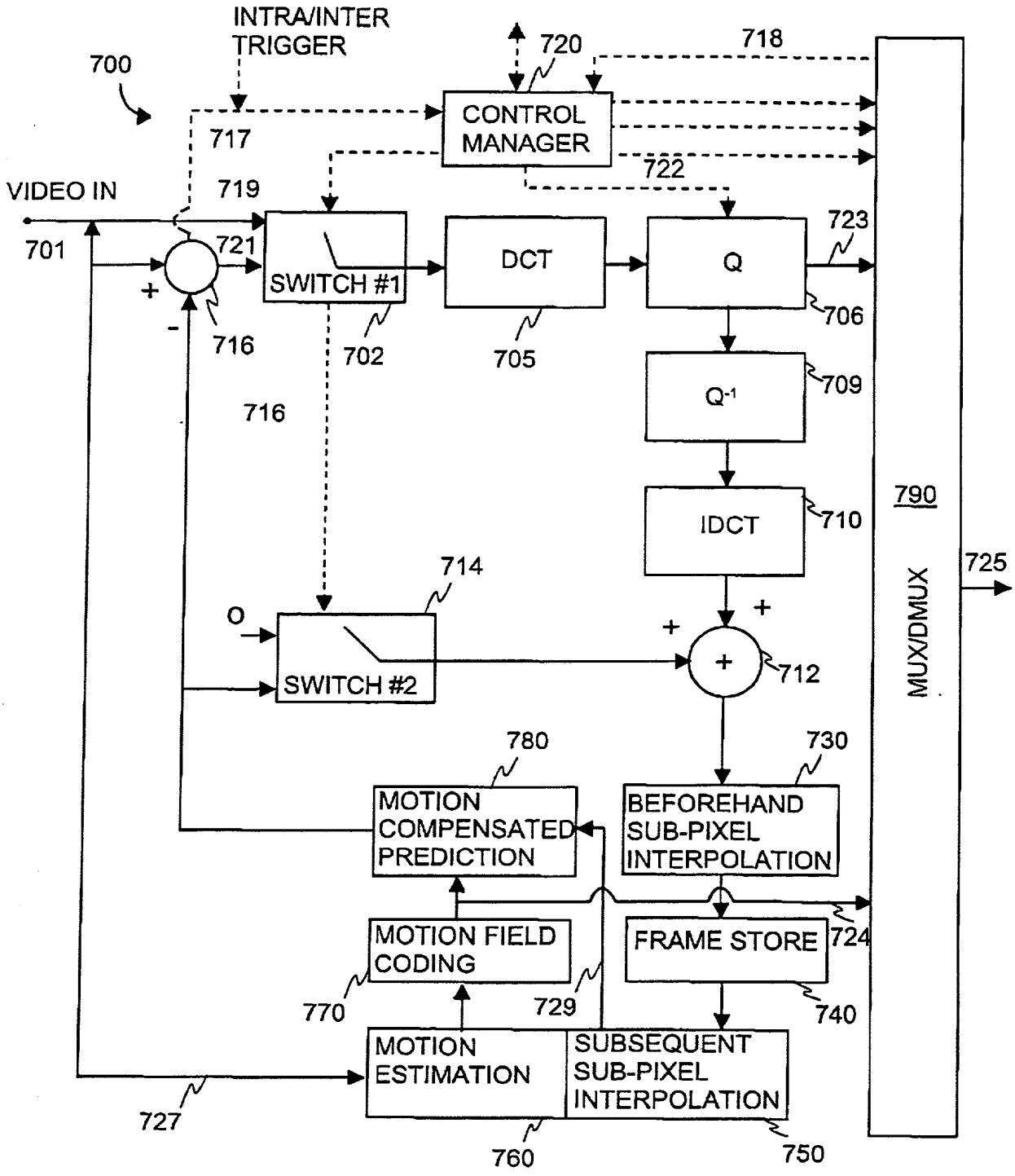


Fig. 7

Nokia Exhibit 2004, p. 112
Amazon.com v. Nokia
IPR2024-01141

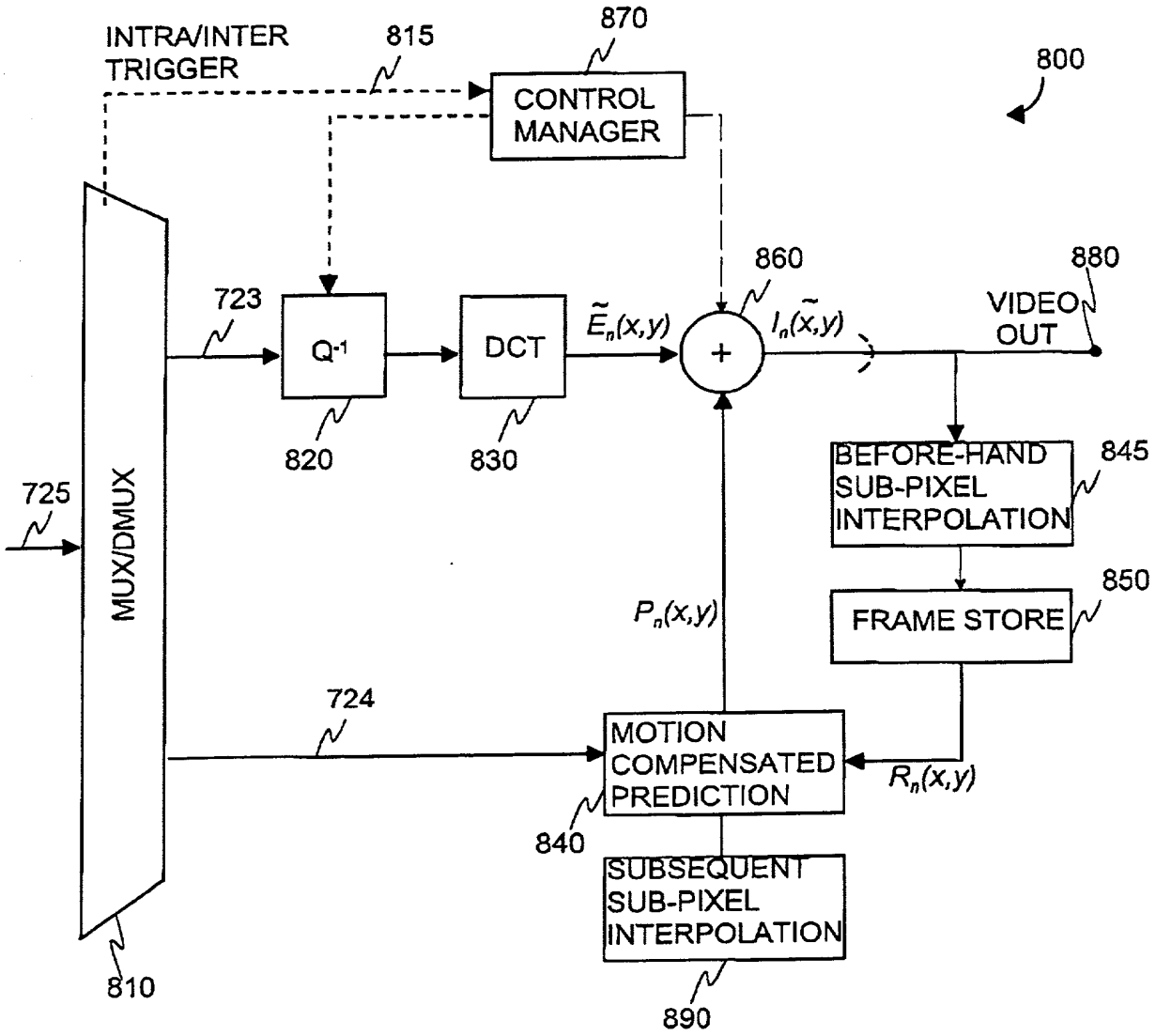


Fig. 8

Nokia Exhibit 2004, p. 113
Amazon.com v. Nokia
IPR2024-01141

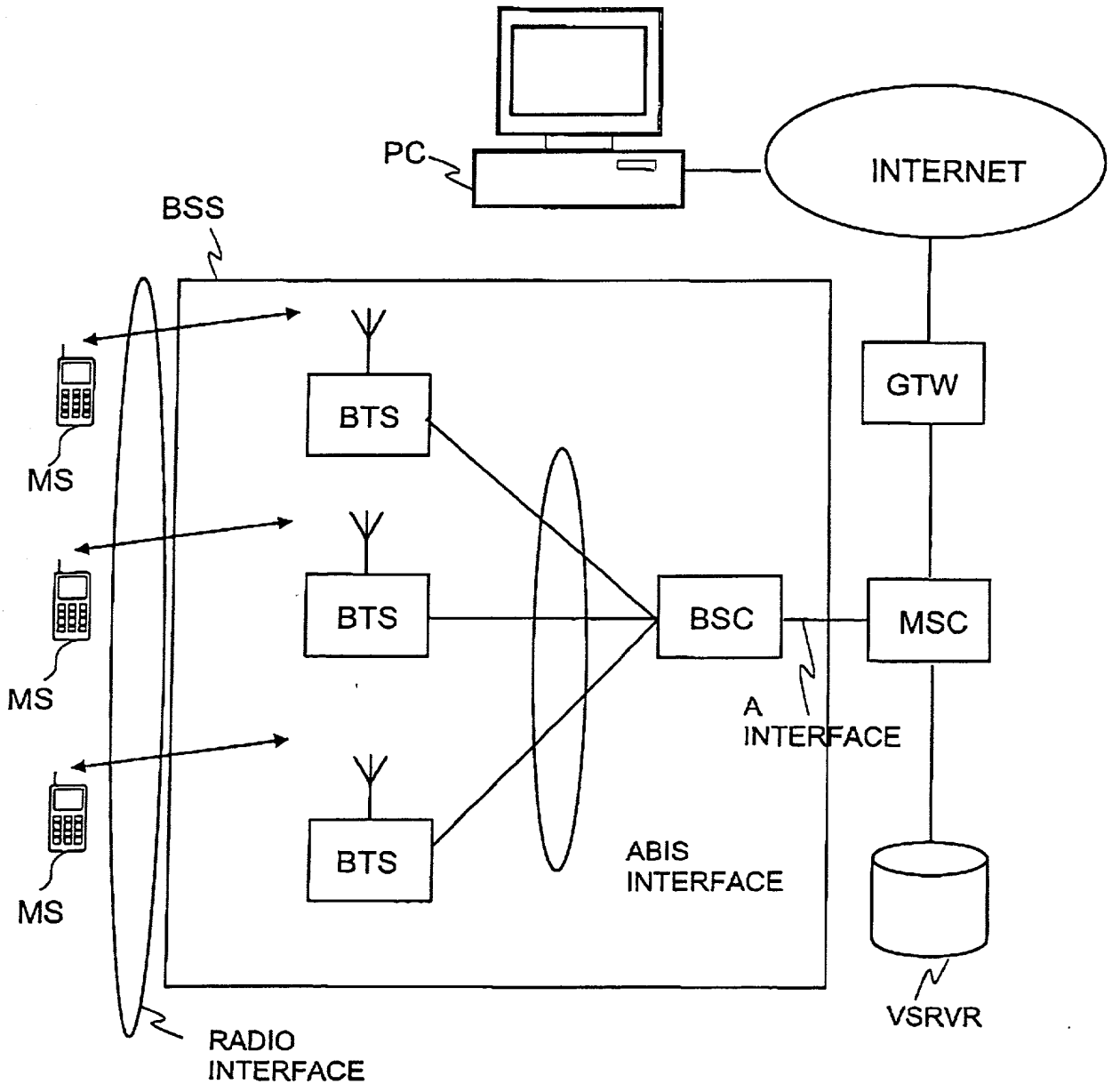


Fig. 11

Nokia Exhibit 2004, p. 114
Amazon.com v. Nokia
IPR2024-01141

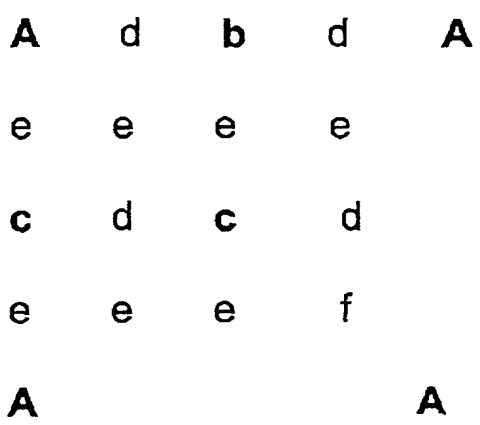


Fig. 12(a)

EP 2 575 308 A1

Nokia Exhibit 2004, p. 115
Amazon.com v. Nokia
IPR2024-01141

WO 2004/059960 PCT/IB2003/005950

A_1	A_2	A_3	A_4	A_5	A_6
		d b d	A		
		e e e	e		
		c d c	d		
		e e e	f		
		A	A		

Figure12(b)

Nokia Exhibit 2004, p. 116
Amazon.com v. Nokia
IPR2024-01141

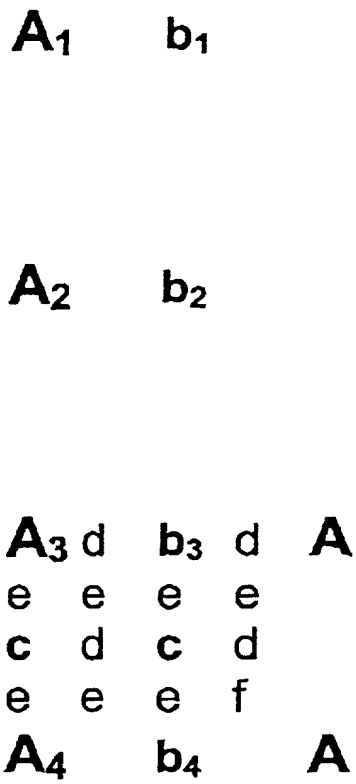


Figure 12(c)

Nokia Exhibit 2004, p. 117
Amazon.com v. Nokia
IPR2024-01141

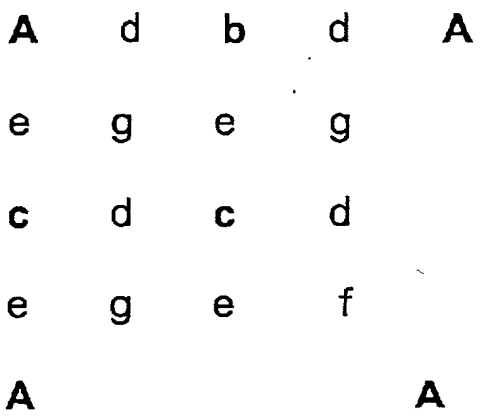


Fig. 13(a)

FOR TESTING PURPOSES

Nokia Exhibit 2004, p. 118
Amazon.com v. Nokia
IPR2024-01141

FIG. 13(b) 80644.5.50

A_1	A_2	A_3	A_4	A_5	A_6
		d b d	d		
		e g e	g		
		c d c	d		
		e g e	f		
		A	A		

Figure13(b)

Nokia Exhibit 2004, p. 119
Amazon.com v. Nokia
IPR2024-01141

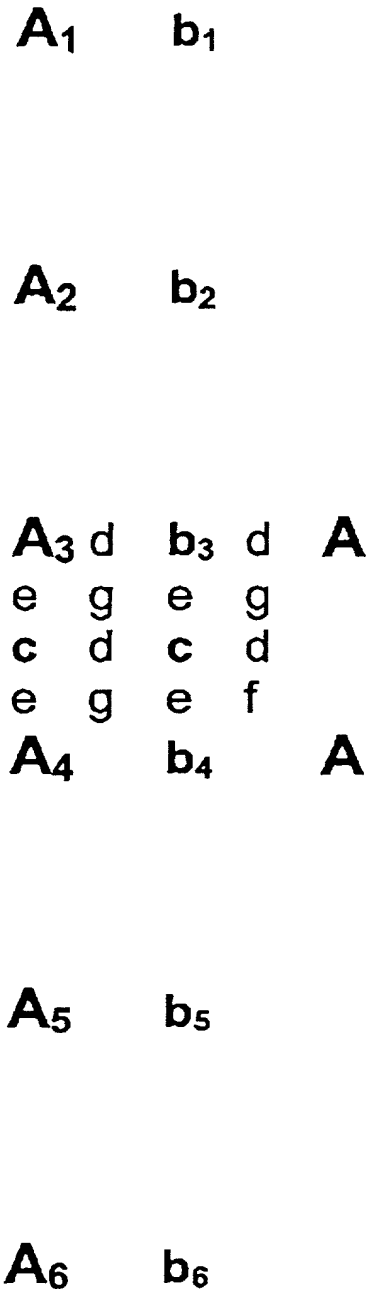


Figure 13(c)

Nokia Exhibit 2004, p. 120
Amazon.com v. Nokia
IPR2024-01141

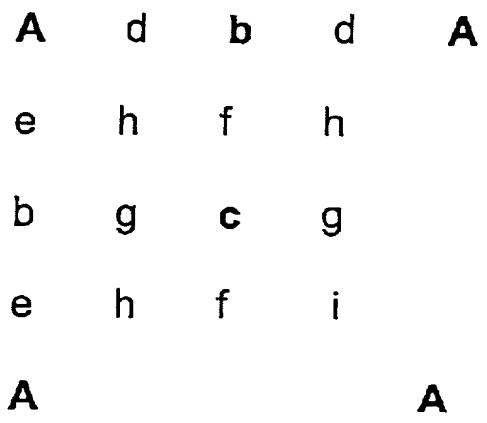


Fig. 14(a)

Nokia Exhibit 2004, p. 121
Amazon.com v. Nokia
IPR2024-01141

EP 1 750 803 B1

Figure14(b)

Nokia Exhibit 2004, p. 122
Amazon.com v. Nokia
IPR2024-01141

A_1

A_2

A_3

d	**b**	d	**A**
e	h	f	h	
b	g	**c**	g	
e	h	f	i	

A_4 **A**

A_5

A_6

Figure 14(c)

Nokia Exhibit 2004, p. 123
Amazon.com v. Nokia
IPR2024-01141

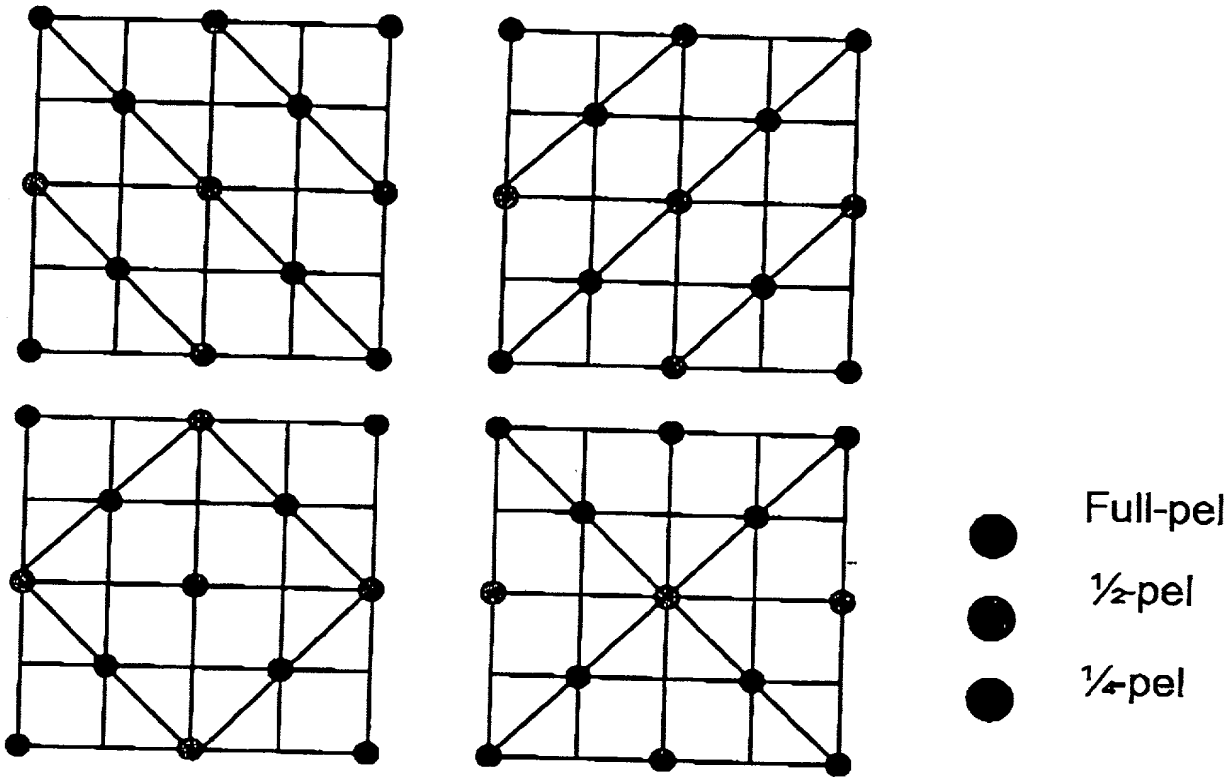


Fig. 15

EP 0 954 180 A1

Nokia Exhibit 2004, p. 124
Amazon.com v. Nokia
IPR2024-01141

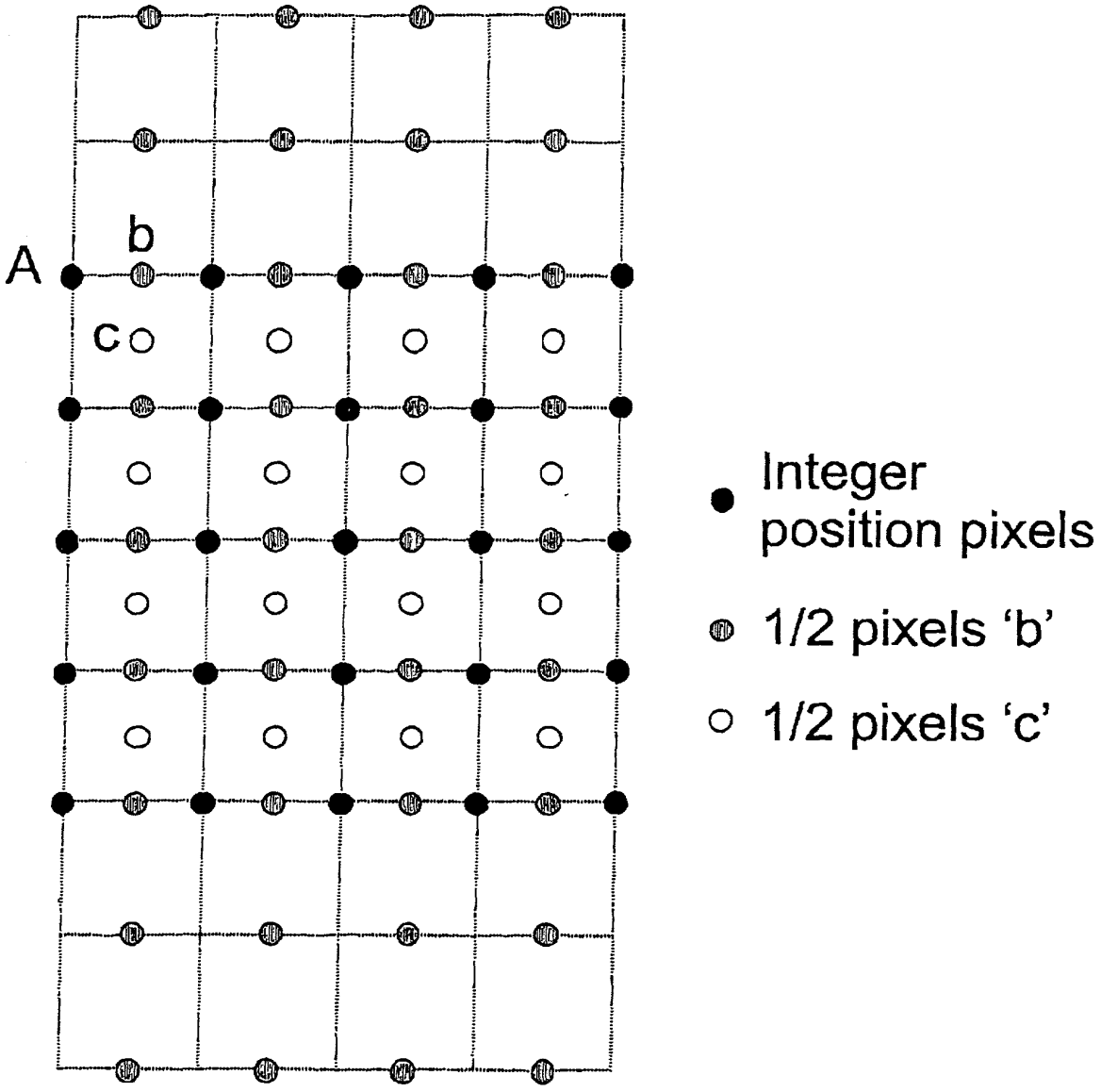


Fig. 16

Nokia Exhibit 2004, p. 125
Amazon.com v. Nokia
IPR2024-01141

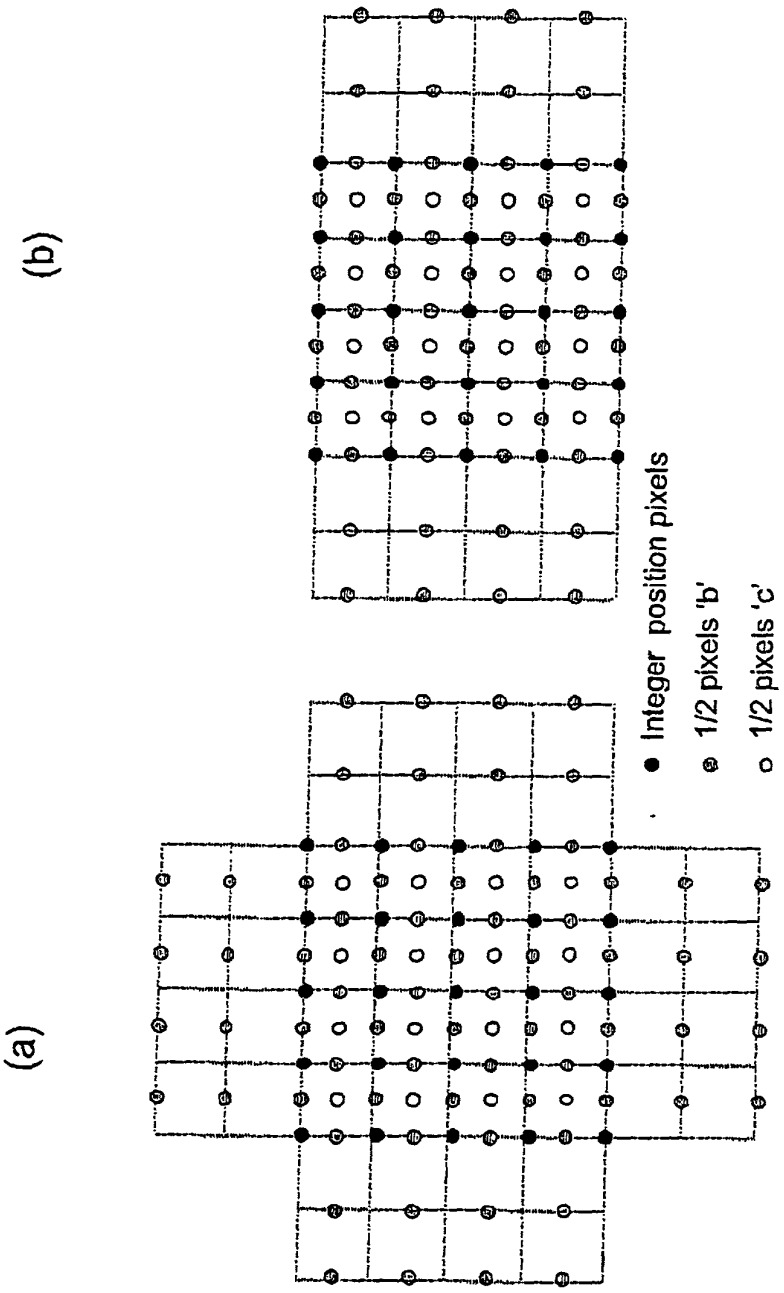
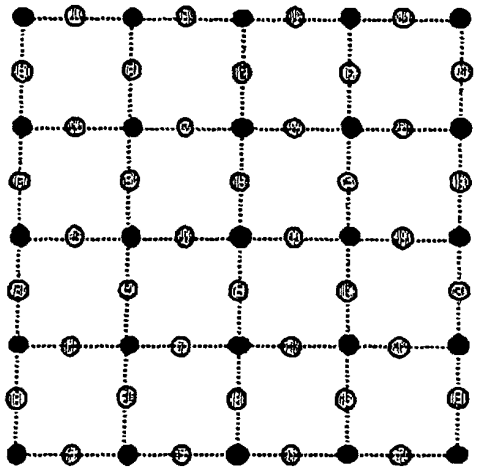
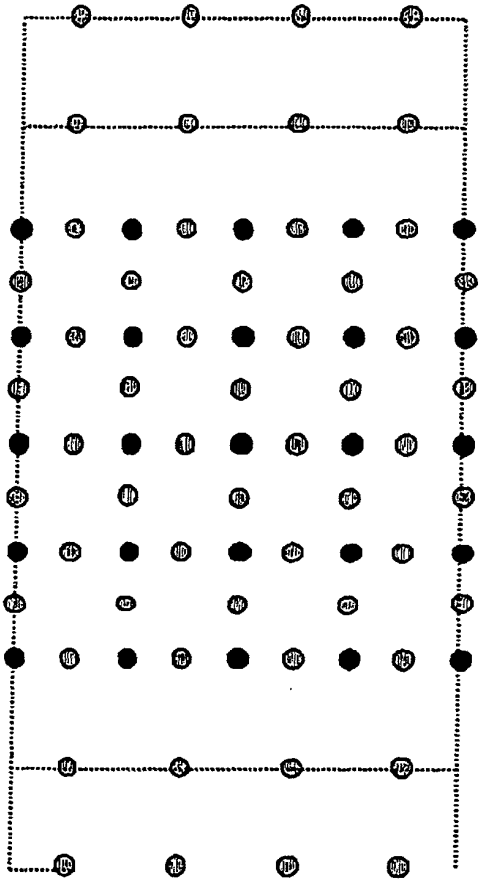


Fig. 17

Nokia Exhibit 2004, p. 126
Amazon.com v. Nokia
IPR2024-01141



(b)



(a)

● Integer position pixels 1/2 pixels 'b'

Fig. 18

WO 97/30548 PCT/SE97/00250

Nokia Exhibit 2004, p. 127
Amazon.com v. Nokia
IPR2024-01141



Fig. 19

09954508 "09/701

Nokia Exhibit 2004, p. 128
Amazon.com v. Nokia
IPR2024-01141

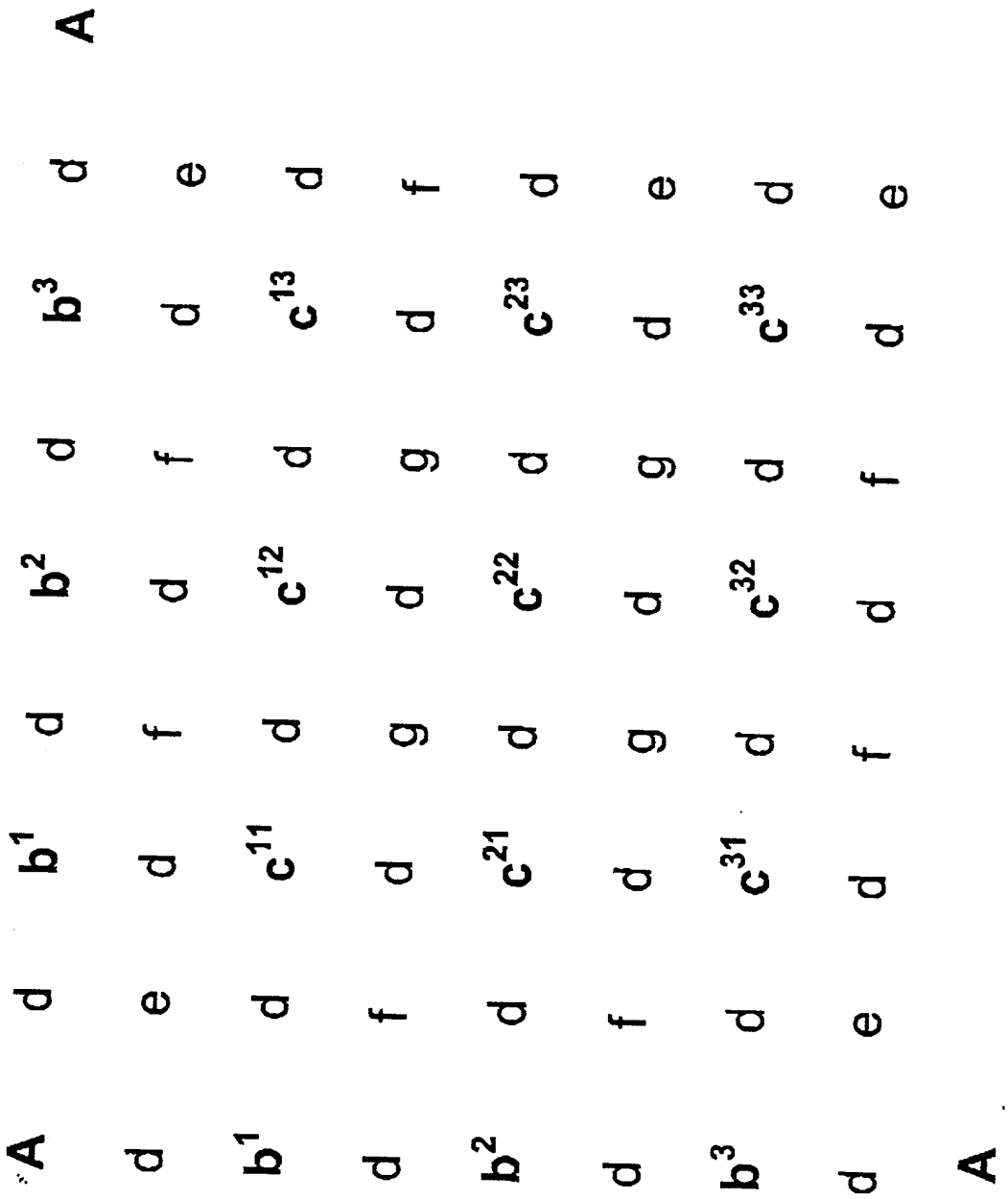


Figure 20

Nokia Exhibit 2004, p. 129
Amazon.com v. Nokia
IPR2024-01141

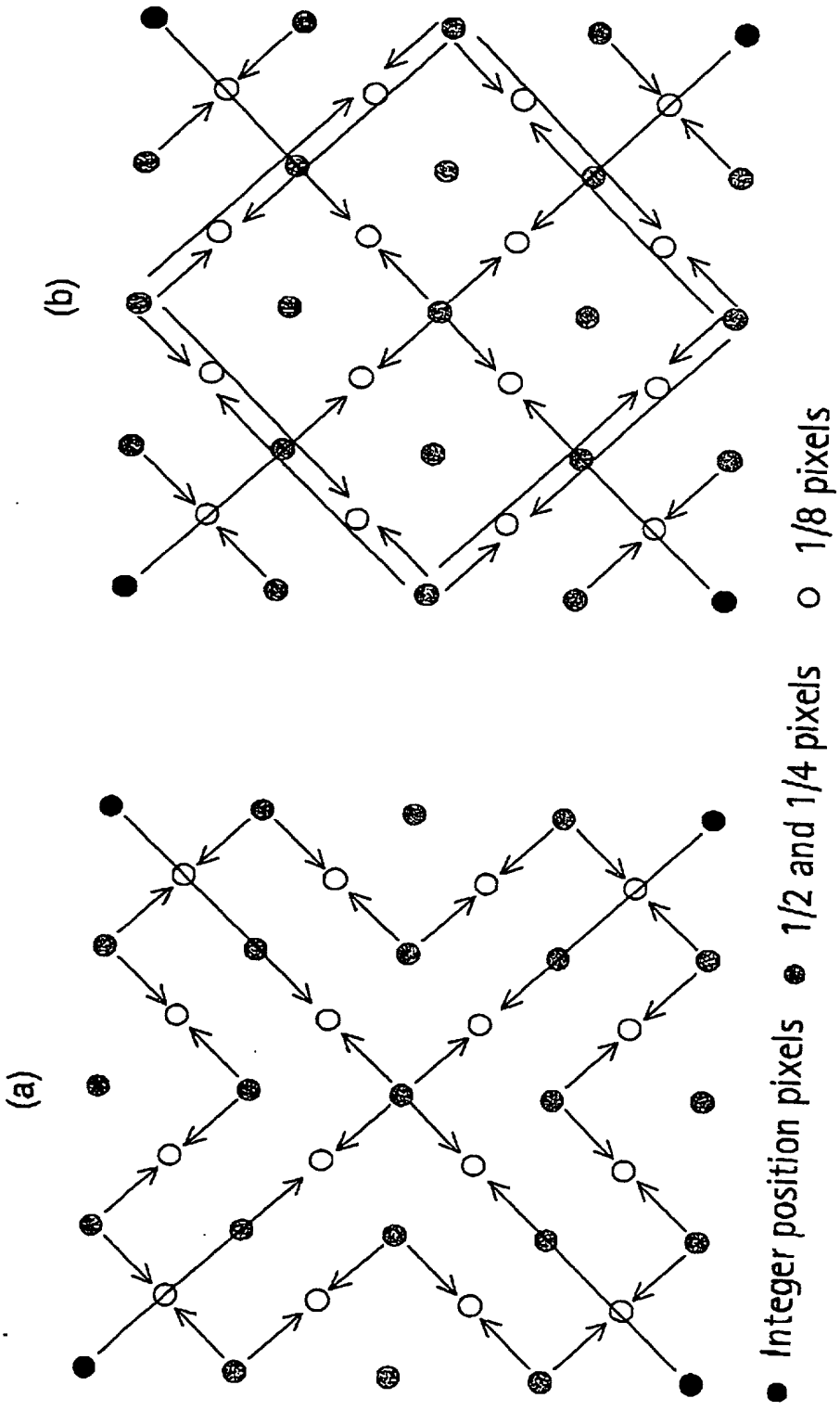


Fig. 21

EP 1 750 460 A1 20070207

Nokia Exhibit 2004, p. 130
Amazon.com v. Nokia
IPR2024-01141

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

Fig. 22

Nokia Exhibit 2004, p. 131
Amazon.com v. Nokia
IPR2024-01141

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

09/20/2001 MBIZUNES 00000016 09954608

01 FC:101	710.00 OP
02 FC:103	486.00 OP
03 FC:102	640.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1999-459-082/19144

Nokia Exhibit 2004, p. 132
Amazon.com v. Nokia
IPR2024-01141

Application or Docket Number

456 - 010567-US (PAR)

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2000

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	47	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	47 minus 20=	* 27
INDEPENDENT CLAIMS	11 minus 3 =	* 8
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	355.00	OR	BASIC FEE	710.00
X$ 9=		OR	X$18=	486
X40=		OR	X80=	640
+135=		OR	+270=	—
TOTAL		OR	TOTAL	1836

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 2.

Nokia Exhibit 2004, p. 133
Amazon.com v. Nokia
IPR2024-01141

CLAIMS ONLY

SERIAL NO.	FILING DATE
09954608	
APPLICANT(S)	

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	1					
2		1				
3		1				
4		1				
5		1				
6		1				
7		1				
8		1				
9		1				
10		1				
11		1				
12		1				
13		1				
14		1				
15		1				
16		1				
17		1				
18	1					
19	1					
20		1				
21		1				
22		1				
23	1					
24		1				
25		1				
~~26~~	~~1~~	~~1~~				
27	1					
28		1				
29		1				
30		1				
31	1					
32		1				
33		1				
34	1					
35	1					
36		1				
37		1				
38		1				
39		1				
40		1				
~~41~~	~~1~~	~~1~~				
42	1					
43		1				
44		1				
45		1				
46	1					
47		1				
48		1				
49	1					
50	1					
TOTAL IND.	13	⇩		⇩		⇩
TOTAL DEP.	36					
TOTAL CLAIMS	49					

	*		*		*	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
51	1					
52						
53						
54						
55						
56						
57						
58						
59						
60						
61						
62						
63						
64						
65						
66						
67						
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86						
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89						
90						
91						
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97						
98						
99						
100						
TOTAL IND.		⇩		⇩		⇩
TOTAL DEP.						
TOTAL CLAIMS						

* MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS

FORM PTO-2022 (1-98)

U.S.DEPARTMENT OF COMMERCE
Patent and Trademark Office

Nokia Exhibit 2004, p. 134
Amazon.com v. Nokia
IPR2024-01141

*U.S. Government Printing Office: 1998 - 433-214/70303

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/954,608	09/17/2001	Marta Karczewicz	456-010567-US(PAR)

CONFIRMATION NO. 8282

2512
PERMAN & GREEN
425 POST ROAD
FAIRFIELD, CT 06430

FORMALITIES LETTER

OC000000006974327

Date Mailed: 10/25/2001

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 130.**

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 3 - OFFICE COPY

Nokia Exhibit 2004, p. 135
Amazon.com v. Nokia
IPR2024-01141

O I P E JC
JAN 0 8 2002
PATENT & TRADEMARK OFFICE

#CB 039 $

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(s): Karczewicz et al.

SERIAL NO.: 09/954,608 ART UNIT:

FILING DATE: 9/17/01 EXAMINER:

TITLE: METHOD FOR SUB-PIXEL VALUE INTERPOLATION

ATTORNEY DOCKET NO.: 442-010567-US (PAR)

Commissioner of Patents
Washington, D.C. 20231

01/15/2002 SMINASS1 00000033 161350 09954608
01 FC:102 8.00 CH 160.00 OP

SUPPLEMENTAL PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified patent application as follows:

IN THE CLAIMS:

Please replace the following claim(s) as rewritten below:

---

23. (Amended) A video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined

Nokia Exhibit 2004, p. 136
Amazon.com v. Nokia
IPR2024-01141

according to $1/2^x$ where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for subpixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

B1

c) interpolate a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

B2

35. (Amended) A video coder for coding an image comprising pixels arranged in rows and columns and represented by values

Nokia Exhibit 2004, p. 137
Amazon.com v. Nokia
IPR2024-01141

having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixels being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

---

38. (Amended) A video coder according to claim 35 in which the interpolator is further adapted to interpolate values for sub-pixels at $1/2^{N}$ unit horizontal and $1/2^{N}$ unit vertical locations by taking the average of at least one pair of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical

Nokia Exhibit 2004, p. 138
Amazon.com v. Nokia
IPR2024-01141

location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

42. (Amended) A communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

46. (Amended) A telecommunications system comprising a communications terminal and a network, the telecommunications

Nokia Exhibit 2004, p. 139
Amazon.com v. Nokia
IPR2024-01141

network and the communications terminal being connected by a communications link over which coded video can be transmitted, the communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

---

49. (Amended) A telecommunications system comprising a communications terminal and a network, the telecommunication network and the communications terminal being connected by a communications link over which coded video can be transmitted, the network comprising a video coder for coding an image

Nokia Exhibit 2004, p. 140
Amazon.com v. Nokia
IPR2024-01141

comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

Please add the following claim(s):

50. (New) A codec for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the codec comprising a video encoder

Nokia Exhibit 2004, p. 141
Amazon.com v. Nokia
IPR2024-01141

and a video decoder, each of the video encoder and the video decoder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to $1/2^x$, where x is a positive integer having a maximum value N, the interpolator of the video encoder and the interpolator of the video decoder each being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

c) interpolate a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels

Nokia Exhibit 2004, p. 142
Amazon.com v. Nokia
IPR2024-01141

or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

51. (New) A codec for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the codec comprising a video encoder and a video decoder, each of the video encoder and the video decoder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator of the video encoder and the interpolator of the video decoder each being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

Nokia Exhibit 2004, p. 143
Amazon.com v. Nokia
IPR2024-01141

REMARKS

1. Claims 23, 35, 38, 42 and 49 are amended. Claims 50 and 51 are new. The claim amendments are to correct grammatical errors in the claims and are not related to patentability. A marked-up version of the amended claims is attached hereto.

2. A check in the amount of $160.00 is enclosed on account of the additional claims fee.

The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,

Geza Ziegler

11-30-01

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Date: 12/3/01

Signature: Carolina Rodriguez
Person Making Deposit

Nokia Exhibit 2004, p. 144
Amazon.com v. Nokia
IPR2024-01141

Marked Up Claim(s)

23. (Amended) A video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined according to [1/2x] $1/2^x$ where x is a positive integer having a maximum value N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate values for subpixels at $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical locations directly using a choice of a first weighted sum of values for sub-pixels residing at $1/2^{N-1}$ unit horizontal and unit vertical locations and a second weighted sum of values for sub-pixels residing at unit horizontal and $1/2^{N-1}$ unit vertical locations, the first and second weighted sums of values being calculated according to step (a); and

Nokia Exhibit 2004, p. 145
Amazon.com v. Nokia
IPR2024-01141

c) interpolate a value for a sub-pixel situated at a $1/2^N$ unit horizontal and $1/2^N$ unit vertical location by taking a weighted average of the value of a first sub-pixel or pixel situated at a $1/2^{N-m}$ unit horizontal and $1/2^{N-n}$ unit vertical location and the value of a second sub-pixel or pixel located at a $1/2^{N-p}$ unit horizontal and $1/2^{N-q}$ unit vertical location, variables m, n, p and q taking integer values in the range 1 to N such that the first and second sub-pixels or pixels are located diagonally with respect to the sub-pixel at $1/2^N$ unit horizontal and $1/2^N$ vertical location.

35. (Amended) A video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location [is required] directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding

Nokia Exhibit 2004, p. 146
Amazon.com v. Nokia
IPR2024-01141

to that of the sub-pixels being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

38. (Amended) A [method] video coder according to claim 35 in which the interpolator is further adapted to interpolate values for sub-pixels at $1/2^N$ unit horizontal and $1/2^N$ unit vertical locations by taking the average of at least one pair of a first pair of values of a sub-pixel located at a $1/2^{N-1}$ unit horizontal and unit vertical location, and a sub-pixel located at a unit horizontal and $1/2^{N-1}$ unit vertical location and a second pair of values of a pixel located at a unit horizontal and unit vertical location, and a sub-pixel located at a $1/2^{N-1}$ unit horizontal and $1/2^{N-1}$ unit vertical location.

42. (Amended) A communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of

Nokia Exhibit 2004, p. 147
Amazon.com v. Nokia
IPR2024-01141

pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location [is required] directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

46. (Amended) A telecommunications system comprising a communications terminal and a network, the telecommunications network and the communications terminal being connected by a communications link over which coded video can be transmitted, the communications terminal comprising a video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

Nokia Exhibit 2004, p. 148
Amazon.com v. Nokia
IPR2024-01141

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location [is required] directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

49. (Amended) A telecommunications system comprising a communications terminal and a network, the telecommunication network and the communications terminal being connected by a communications link over which coded video can be transmitted, the network comprising a video coder for coding [for coding] an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the resolution of the sub-pixels being determined by a positive integer N, the interpolator being adapted to:

a) interpolate values for sub-pixels at $1/2^{N-1}$ unit horizontal and unit vertical locations, and unit horizontal and $1/2^{N-1}$ unit vertical locations directly using weighted sums of pixels residing at unit horizontal and unit vertical locations;

b) interpolate a value for a sub-pixel at a sub-pixel horizontal and sub-pixel vertical location [is required]

Nokia Exhibit 2004, p. 149
Amazon.com v. Nokia
IPR2024-01141

directly using a choice of a first weighted sum of values for sub-pixels located at a vertical location corresponding to that of the sub-pixel being calculated and a second weighted sum of values for sub-pixels located at a horizontal location corresponding to that of the sub-pixel being calculated.

Nokia Exhibit 2004, p. 150
Amazon.com v. Nokia
IPR2024-01141

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):KARCZEWICZ et al.
SERIAL NO.: 09/954,608 EXAMINER:
FILING DATE:9/17/01 ART UNIT:
TITLE:METHOD FOR SUB-PIXEL VALUE INTERPOLATION
ATTORNEY DOCKET NO.: 456-010567-US(PAR)

The Commissioner of Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

The following information is being disclosed to the Patent and Trademark Office as information that may be material to the examination of the above-identified patent application.

This Information Disclosure Statement is being filed before receipt of a first Office Action on the above-identified patent application. Thus, a certification under 37 CFR 1.97 (e) or fee under 37 CFR 1.17 (p) is not required for the information herein to be considered.

Applicants' attorney encloses copies of United States Patent Nos. US 5,488,419, US 5,844,616, US 5,452,377, US 4,937,666, PCT International Publication No. WO 99/04574, FPM 21.3, "An Interpolator for HD-MAC Decoder", Chao et al., "Directional Interpolation for Magnetic Resonance Angiography Data", Mehran Moshfeghi, IEEE Transactions on Medical Imaging, Vol. 12, No. 2, June 1993. Document Q15-

Nokia Exhibit 2004, p. 151
Amazon.com v. Nokia
IPR2024-01141

"H.26L Test Model Long Term Number 5 (TML-5) draft0", ITU, Study Group 16, Document VCEG-L20, "Complexity Reduced Motion Compensated Prediction with 1/8-pel Displacement Vector Resolution", ITU, Study Group 16, English translation of Japanese publication No. Hei 6-14739, and Japanese Patent document No. JP 62-039920 (English abstract is attached); all of which were provided by the applicants and may be considered relevant to the invention claimed in the above-identified application.

Copies of the references are enclosed together with PTO-Form 1449.

The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,

12/28/01

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Amazon.com v. Nokia
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Nokia Exhibit 2004, p. 153
Amazon.com v. Nokia
IPR2024-01141

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INTERNATIONALE ANMELDUNG VERÖFFENTLICHT NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT)

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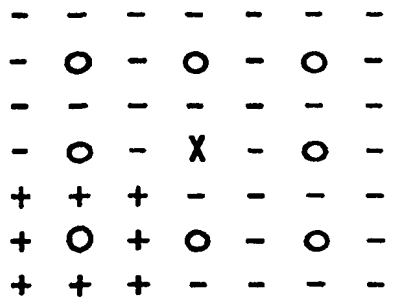
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Mit internationalem Recherchenbericht.
Vor Ablauf der für Änderungen der Ansprüche zugelassenen Frist; Veröffentlichung wird wiederholt falls Änderungen eintreffen.

(54) Title: INTERPOLATION FILTERING METHOD FOR ACCURATE SUB-PIXEL MOTION ASSESSMENT

(54) Bezeichnung: INTERPOLATIONSFILTERUNGSVERFAHREN FÜR SUB–PELGENAUIGKEIT–BEWEGUNGSSCHÄTZUNG

(57) Abstract

In order to generate an improved image signal in motion assessment, an exact pixel determination of a moving vector is initially carried out, followed by a two–step interpolation filtering at exact subpixel resolution. The interpolation coefficients are chosen with the purpose of reducing aliasing. A larger number of adjacent pixels are used in comparison with conventional interpolation methods. The quality of the prediction signal for moving images can be thus improved, thereby enhancing coding efficiency.



(57) Zusammenfassung

Zur Erzeugung eines verbesserten Bildsignals bei der Bewegungsschätzung erfolgt zuerst eine pelgenaue Bestimmung eines Bewegungsvektors und anschließend eine zweistufige Interpolationsfilterung auf Sub–Pelgenauigkeit. Die Interpolationskoeffizienten werden hinsichtlich einer Aliasing–Reduzierung gewählt. Zur Interpolation werden mehr Nachbarbildpunkte herangezogen als bei üblichen Interpolationsverfahren. Die Qualität eines Prädiktionssignals für Bewegungsbilder läßt sich verbessern und damit die Codierungseffizienz steigern.

Nokia Exhibit 2004, p. 154
Amazon.com v. Nokia
IPR2024-01141

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Nokia Exhibit 2004, p. 155
Amazon.com v. Nokia
IPR2024-01141

INTERPOLATIONSFILTERUNGSVERFAHREN FÜR SUB-PELGENAUIGKEIT-BEWEGUNGSSCHÄTZUNG

Stand der Technik

Die Erfindung geht aus von einem Verfahren zur Erzeugung eines verbesserten Bildsignals bei der Bewegungsschätzung von Bildsequenzen, insbesondere eines Prädiktionssignals für Bewegtbilder mit bewegungskompensierender Prädiktion, wobei für Bildblöcke Bewegungsvektoren gebildet werden, die für jeden Bildblock eines aktuellen Bildes die Position des zur Prädiktion benutzten Bildblockes gegenüber einem zeitlich davorliegenden Referenzbild angeben.

Aus der EP 0 558 922 B2 ist ein Verfahren zur Verbesserung der Bewegungsschätzung in Bildsequenzen in Halbpelgenauigkeit nach dem Full-Search-Verfahren bekannt. Dort wird in einem ersten Verfahrensschritt der Suchbereich und in einem zweiten Verfahrensschritt der Match-Block gefiltert unter Zuhilfenahme eines zusätzlichen digitalen Filters, daß eine Rasterverschiebung des Bildpunktrasters um ¼ pel ermöglicht. Mit dieser Maßnahme ist eine Verfälschung des Bewegungsvektorfeldes auszuschließen.

Nokia Exhibit 2004, p. 156
Amazon.com v. Nokia
IPR2024-01141

Beim „MPEG-4 Video Verification Model Version 7.0", Bristol, April 1997, MPEG 97/N1642 in ISO/IEC JTC1/SC 29/WG11 ist ein Encoder und Decoder zur objektbasierten Codierung von Bewegtbildfolgen spezifiziert. Dabei werden nicht mehr rechteckige Bilder fester Größe codiert und zum Empfänger übertragen, sondern sogenannte VIDEO OBJECTS (VO), welche beliebige Form und Größe aufweisen dürfen. Die Abbildung eines solchen VO in der Kamerabildebene zu einem bestimmten Zeitpunkt wird als VIDEO OBJECTS PLANE (VOP) bezeichnet. Somit ist die Beziehung zwischen VO und VOP äquivalent zu der Beziehung zwischen Bildfolge und Bild im Falle der Übertragung rechteckiger Bilder fester Größe.

Die bewegungskompensierende Prädiktion im Verifikationsmodell wird mit Hilfe sogenannter blockweiser Bewegungsvektoren durchgeführt, die für jeden Block der Größe 8 x 8 bzw. 16 x 16 Bildpunkte des aktuellen Bildes die Position des zur Prädiktion benutzten Blockes in einem bereits übertragenen Referenzbild angeben. Die Auflösung der Bewegungsvektoren ist dabei auf einen halben Bildpunkt beschränkt, wobei Bildpunkte zwischen dem Abtastraster (half pixel position) durch eine bilineare Interpolationsfilterung aus den Bildpunkten auf dem Abtastraster (integer pixel position) erzeugt werden (Figur 1).+ gibt hierbei die Ganzzahl-Pixel-Position und O die Halb-Pixel-Position an. Die interpolierten Werte a, b, c und d in Halb-Pixel-Position ergeben sich durch folgende Beziehungen:
$a = A$, $b = (A + B)//2$, $c = (A + C)//2$,
$d = (A + B + C + D)//4$, wobei // eine gerundete Ganzzahl-Division kennzeichnet.

Vorteile der Erfindung

Mit den Maßnahmen der Erfindung läßt sich die Qualität des Prädiktionssignals und somit die Kodierungseffizienz

Nokia Exhibit 2004, p. 157
Amazon.com v. Nokia
IPR2024-01141

verbessern. Dabei wird zur Erzeugung von Bildpunkten zwischen dem Bildpunkt-Abtastraster eine größere örtliche Nachbarschaft berücksichtigt, als bei der bilinearen Interpolation. Die erfindungsgemäße aliasing-reduzierende Interpolationsfilterung führt zu einer erhöhten Auflösung des Bewegungsvektors und damit zu einem Prädiktionsgewinn und einer erhöhten Codierungseffizienz. Bei der Erfindung können die FIR-Filterkoeffizienten den zu codierenden Signalen angepaßt und für jedes Video-Object getrennt übertragen werden, was eine weitere Effizienzerhöhung für die Codierung ermöglicht sowie die Flexibilität des Verfahrens erhöht.

Im Gegensatz zur Lösung gemäß der EP 0 558 922 B1 müssen keine zusätzlichen Polyphasenfilterstrukturen für Zwischenpositionen mit ¼ pel-Bildpunktauflösung in horizontaler und vertikaler Richtung entworfen werden.

Mit den Maßnahmen der Erfindung ist es möglich, daß bei gleichbleibender Datenrate die Bildfolgefrequenz eines MPEG-1-Coders von 25 Hz auf 50 Hz verdoppelt werden kann. Bei einem MPEG2-Coder kann die Datenrate bei gleichbleibender Bildqualität um bis zu 30% reduziert werden.

Zeichnungen

Anhand von Zeichnungen werden nun Ausführungbeispiele der Erfindung näher erläutert. Es zeigen:

Figur 2 ein Interpolationsschema für Bildpunkte zwischen dem Bildpunkt-Abtastraster,
Figur 3 die Struktur eines FIR-Filters zur Interpolation,
Figur 4 eine weitere Interpolation mit noch höherer Auflösung.

Nokia Exhibit 2004, p. 158
Amazon.com v. Nokia
IPR2024-01141

Beschreibung von Ausführungsbeispielen

Beim Verfahren nach der Erfindung werden für Bildblöcke Bewegungsvektoren gebildet, die für jeden Bildblock eines aktuellen Bildes die Position des zur Prädiktion benutzten Bildblockes gegenüber einem zeitlich davorliegenden Referenzbild angeben.

Die Bestimmung der Bewegungsvektoren für die Prädiktion erfolgt in drei aufeinanderfolgenden Schritten:
In einem ersten Suchschritt wird ein Bewegungsvektor mit Pelgenauigkeit nach einem herkömmlichen Verfahren, z.B. nach der Full-Search-Block-Matching-Methode, für jeden Bildblock bestimmt. Hierbei wird das Minimum des Fehlerkriteriums für mögliche Bewegungspositionen ermittelt und jener Vektor, der die Bewegung des Bildblockes am besten beschreibt, ausgewählt (EP 0 368 151 B1).

In einem zweiten Suchschritt, der wiederum auf einer solchen Minimumsuche für das Fehlerkriterium basiert, wird ausgehend von dem im ersten Schritt ermittelten Bewegungsvektor mit Pelgenauigkeit durch eine aliasing-reduzierende Interpolationsfilterung mittels eines digitalen symmetrischen FIR (finite impulse response)-Filters ein verbesserter Bewegungsvektor auf Subpelgenauigkeit ermittelt. Die Auflösung wird hierbei höher gewählt als im ersten Suchschritt, vorzugsweise wird eine Auflösung von einem halben Bildpunkt bezogen auf das Bildpunktraster gewählt. Figur 2 zeigt das Interpolationsmuster für die Bildpunkte b, c und d zwischen dem Bildpunktraster, die sich aus den Nachbarbildpunkten A, B, C, D, E, F, G, H auf dem Bildpunktraster ergeben. + gibt die Ganzzahl-Pixelposition an, o die Halbpixelposition. Es gilt:

Nokia Exhibit 2004, p. 159
Amazon.com v. Nokia
IPR2024-01141

$b = (CO1x(A_{-1} + A_{+1}) + CO2x\ (A_{-2} + A_{+2}) + CO3x\ (A_{-3} + A_{+3}) + CO4x\ (A_{-4} + A_{+4}))/256$

$c_i = (CO1x(A_i + E_i) + CO2x(B_i + F_i) + CO3x\ (C_i + G_i) + GO4x(D_i + H_i))/256$

$d = (CO1x(c_{-1} + c_{+1}) + CO2x(c_{-2} + c_{+2}) + CO3x\ (c_{-3} + c_{+3}) + CO4x(c_{-4} + c_{+4}))/256$

Die Struktur des verwendeten FIR-Interpolationsfilters ist aus Figur 3 ersichtlich. Es weist nach jeder Bildpunktposition δp einen Abzweig zu einem Koeffizientenbewerter 1, 2, 3 usw. auf und eine Summationseinrichtung 10 am Ausgang. Wie aus obigen Beziehungen ersichtlich ist, wird zur Erzeugung von Bildpunkten zwischen dem Abtastraster eine größere örtliche Nachbarschaft berücksichtigt, als bei der bilinearen Interpolation nach dem Stand der Technik. Die Interpolationsfilterkoeffizienten CO2, CO3, CO4 werden dabei so bestimmt, daß die Interpolationsfehlerleistung minimal wird. Die Koeffizienten können direkt mit dem bekannten Schätzverfahren des kleinsten, mittleren quadratischen Fehlers bestimmt werden. Aus der Minimierung der Interpolationsfehlerleistung erhält man ein lineares Gleichungssystem, dessen Koeffizienten aus dem Orthogonalitätsprinzip abgeleitet werden können. Ein derart optimierter Satz von FIR-Filterkoeffizienten ist durch die Koeffizienten CO1 = 161/256, CO2 = -43/256, CO3 = 23/256, CO4 = -8/256 gegeben.

Im dritten Suchschritt wird ausgehend von dem auf ½ Pelgenauigkeit bestimmten Bewegungsvektor durch eine weitere Interpolationsfilterung eine lokale Suche unter Zugrundelegung der acht Nachbarbildpunkte mit einer Auflösung, die noch weiter erhöht ist, vorzugsweise auf ¼ Bildpunkt, durchgeführt. Es wird wie zuvor der Bewegungsvektor ausgewählt, der die geringste Prädiktionsfehlerleistung liefert.

Nokia Exhibit 2004, p. 160
Amazon.com v. Nokia
IPR2024-01141

Das Interpolationsmuster hierzu zeigt Figur 4. Die ganzzahligen Bildpunkt-Positionen sind mit X gekennzeichnet, die Halb-Pixel-Bildpunktpositionen mit o und die Viertel-Pixel-Bildpunktpositionen mit -. O markiert die beste Kompensation mit 1/2-Bildpunkt und + die Viertelbildpunkt-Suchposition.

Interpoliert wird bezüglich des Bildpunktrasters mit der Auflösung von einem halben Bildpunkt aus dem zweiten Suchschritt mit den FIR-Filterkoeffizienten CO1' = 1/2, CO2' = O, CO3' = O, CO4' = O.

Die gleiche zuvor vorgestellte Interpolationstechnik wird für die bewegungskompensierende Prädiktion verwendet.

Falls die Verarbeitung innerhalb eines Coders mit einem reduzierten Bildformat durchgeführt wird (SIF-Format innerhalb eines MPEG1-Coders oder Q-CIF in einem H.263-Coder), zur Anzeige aber das ursprüngliche Eingangsformat verwendet wird, z.B. CCIR 601[1] bei MPEG-1 oder CIF bei H.263, muß als Nachverarbeitung eine örtliche Interpolationsfilterung durchgeführt werden. Auch für diesen Zweck kann die beschriebene aliasing-kompensierende-Interpolationsfilterung verwendet werden.

Um die aliasing-kompensierende Interpolation mit 1/4 Pel Auflösung zu aktivieren, können in einen Bildübertragungs-Bitstrom Aktivierungsbits eingefügt werden.

Für die Prädiktion von Video-Objekten können die Filterkoeffizienten CO1 bis CO4 und CO1' bis CO4' für jedes der Video-Objekte VO getrennt aufbereitet werden und in den Bildübertragungs-Bitstrom zu Beginn der Übertragung des jeweiligen Video-Objekts eingefügt werden.

Nokia Exhibit 2004, p. 161
Amazon.com v. Nokia
IPR2024-01141

Zur Codierung eines Bewegungsvektors kann der Wertebereich der zu codierenden Bewegungsvektor-Differenzen an die erhöhte Auflösung angepaßt werden.

Nokia Exhibit 2004, p. 162
Amazon.com v. Nokia
IPR2024-01141

Ansprüche

1. Verfahren zur Erzeugung eines verbesserten Bildsignals bei der Bewegungsschätzung von Bildsequenzen, insbesondere eines Prädiktionssignals für Bewegtbilder mit bewegungskompensierender Prädiktion, wobei für Bildblöcke Bewegungsvektoren gebildet werden, die für jeden Bildblock eines aktuellen Bildes die Position des zur Prädiktion benutzten Bildblockes gegenüber einem zeitlich davorliegenden Referenzbild angeben, mit folgenden Schritten:
- In einem ersten Suchschritt wird ein Bewegungsvektor auf Pelgenauigkeit bestimmt,
- in einem zweiten Suchschritt wird ausgehend von dem Bewegungsvektor mit Pelgenauigkeit durch eine aliasing-reduzierende Interpolationsfilterung mittels eines digitalen Filters ein verbesserter Bewegungsvektor auf Subpelgenauigkeit ermittelt, wobei die Auflösung höher gewählt ist, als es der Auflösung des Bildpunktrasters im ersten Suchschritt entspricht und wobei zur Interpolation mehr Nachbarbildpunkte herangezogen werden als bei einer bilinearen Interpolation,
- in einem dritten Suchschritt wird ausgehend von dem auf Subpelgenauigkeit bestimmten Bewegungsvektor durch eine weitere Interpolationsfilterung mittels des digitalen Filters ein weiter verbesserter Bewegungsvektor ermittelt,

Nokia Exhibit 2004, p. 163
Amazon.com v. Nokia
IPR2024-01141

wobei die Auflösung gegenüber dem zweiten Suchschritt nochmals erhöht wird und die Interpolation basierend auf dem Bildpunktraster mit der Auflösung im zweiten Suchschritt vorgenommen wird.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß zur Interpolationsfilterung beim zweiten Suchschritt ein FIR-Filter verwendet wird mit den Filterkoeffizienten CO1 = 161/256, CO2 = -43/256, CO3 = 23/256, CO4 = -8/256.

3. Verfahren nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß zur Interpolationsfilterung beim dritten Suchschritt ein FIR-Filter verwendet wird, mit den FIR-Filterkoeffizienten CO1' = 1/2, CO2' = 0, CO3' = 0, CO4' = 0.

4. Verfahren nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß für die Prädiktion von Video-Objekten (VO) die Filterkoeffizienten des digitalen Filters/FIR-Filters für jedes Video-Objekt getrennt aufbereitet werden und in einen Übertragungsbitstrom zu Beginn der Übertragung des jeweiligen Objektes eingefügt werden.

5. Verfahren nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß zur Codierung eines Bewegungsvektors, insbesondere für eine Übertragung der Wertebereich der zu codierende Bewegungsvektor-Differenzen an eine erhöhte Auflösung angepaßt wird.

Nokia Exhibit 2004, p. 164
Amazon.com v. Nokia
IPR2024-01141

1/2

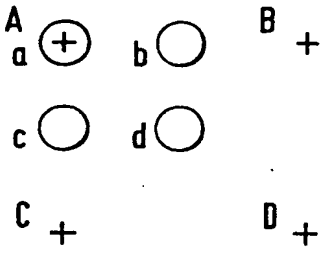


Fig.1

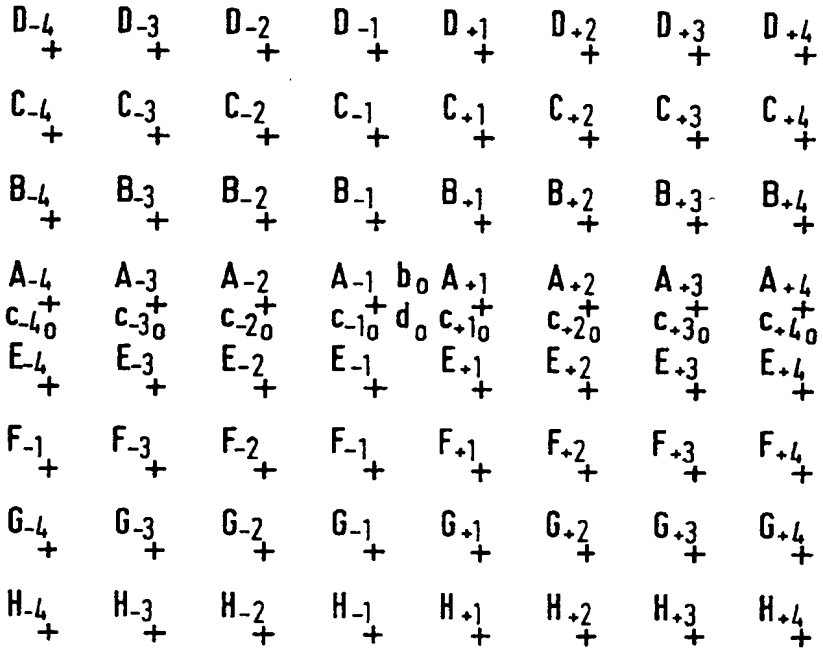


Fig.2

Nokia Exhibit 2004, p. 165
Amazon.com v. Nokia
IPR2024-01141

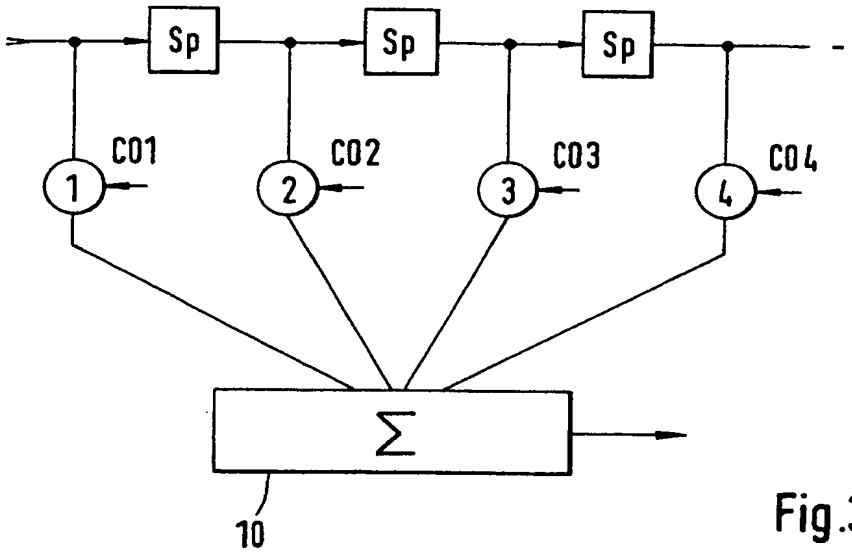


Fig.3

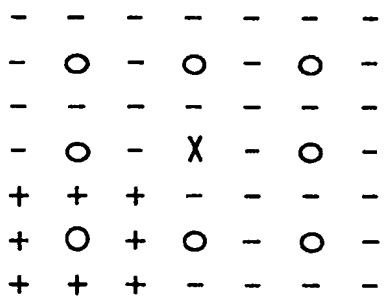


Fig.4

Nokia Exhibit 2004, p. 166
Amazon.com v. Nokia
IPR2024-01141

INTERNATIONAL SEARCH REPORT

Interr. ..onal Application No
PCT/DE 98/01938

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N7/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	ZIEGLER M: "HIERARCHICAL MOTION ESTIMATION USING THE PHASE CORRELATION METHOD IN 140 MBIT/S HDTV-CODING" SIGNAL PROCESSING OF HDTV, 2, TURIN, AUG. 30 - SEPT. 1, 1989, no. WORKSHOP 3, 30 August 1989, pages 131-137, XP000215234 CHIARIGLIONE L see paragraph 4.3 ---	1-5
Y	WERNER O: "DRIFT ANALYSIS AND DRIFT REDUCTION FOR MULTIRESOLUTION HYBRID VIDEO CODING" SIGNAL PROCESSING. IMAGE COMMUNICATION, vol. 8, no. 5, 1 July 1996, pages 387-409, XP000590242 see page 398, left-hand column, line 17 - right-hand column, line 8 ---	1-5

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
9 December 1998	16/12/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	BERBAIN, F

1

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Nokia Exhibit 2004, p. 167
page 1 of 2Amazon.com v. Nokia
IPR2024-01141

INTERNATIONAL SEARCH REPORT

Inter... Application No
PCT/DE 98/01938

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 558 922 A (BUNDESREP DEUTSCHLAND) 8 September 1993 cited in the application see claim 1 ---	1-5
A	SIU-LEONG IU: "COMPARISION OF MOTION COMPENSATION USING DIFFERENT DEGREES OF SUB- PIXEL ACCURACY FOR INTERFIELD/INTERFRAME HYBRID CODING OF HDTV IMAGE SEQUENCES" MULTIDIMENSIONAL SIGNAL PROCESSING, SAN FRANCISCO, MAR. 23 - 26, 1992, vol. 3, no. CONF. 17, 23 March 1992, pages 465-468, XP000378969 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS see abstract; figure 1 ---	1-5
A	"MUNICH MEETING OF MPEG-4 WORKING GROUP. REPORT ISO/IEC JTC1/SC29/WG11 MPEG4/N1172" INTERNATIONAL ORGANISATION FOR STANDARDISATION - ORGANISATION INTERNATIONALE DE NORMALISATION, January 1996, pages 3-49, XP002047798 see paragraph 3.3.2.4 ---	1-5
A	EP 0 348 207 A (MATSUSHITA ELECTRIC IND CO LTD) 27 December 1989 see abstract -----	1-5

1

Nokia Exhibit 2004, p. 168
page 2 of Amazon.com v. Nokia
IPR2024-01141

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern. ...nal Application No
PCT/DE 98/01938

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0558922 A	08-09-1993	DE 4206622 A	09-09-1993
EP 0348207 A	27-12-1989	JP 2005689 A	10-01-1990
		JP 7028408 B	29-03-1995
		JP 2118888 A	07-05-1990
		DE 68926475 D	20-06-1996
		DE 68926475 T	23-01-1997
		US 5111511 A	05-05-1992

Nokia Exhibit 2004, p. 169
Amazon.com v. Nokia
IPR2024-01141

INTERNATIONALER RECHERCHENBERICHT

Interr. ..nales Aktenzeichen
PCT/DE 98/01938

A. KLASSIFIZIERUNG DES ANMELDUNGSGEGENSTANDES
IPK 6 H04N7/36

Nach der Internationalen Patentklassifikation (IPK) oder nach der nationalen Klassifikation und der IPK

B. RECHERCHIERTE GEBIETE

Recherchierter Mindestprüfstoff (Klassifikationssystem und Klassifikationssymbole)
IPK 6 H04N

Recherchierte aber nicht zum Mindestprüfstoff gehörende Veröffentlichungen, soweit diese unter die recherchierten Gebiete fallen

Während der internationalen Recherche konsultierte elektronische Datenbank (Name der Datenbank und evtl. verwendete Suchbegriffe)

C. ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie*	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
Y	ZIEGLER M: "HIERARCHICAL MOTION ESTIMATION USING THE PHASE CORRELATION METHOD IN 140 MBIT/S HDTV-CODING" SIGNAL PROCESSING OF HDTV, 2, TURIN, AUG. 30 - SEPT. 1, 1989, Nr. WORKSHOP 3, 30. August 1989, Seiten 131-137, XP000215234 CHIARIGLIONE L siehe Absatz 4.3 ---	1-5
Y	WERNER O: "DRIFT ANALYSIS AND DRIFT REDUCTION FOR MULTIRESOLUTION HYBRID VIDEO CODING" SIGNAL PROCESSING. IMAGE COMMUNICATION, Bd. 8, Nr. 5, 1. Juli 1996, Seiten 387-409, XP000590242 siehe Seite 398, linke Spalte, Zeile 17 - rechte Spalte, Zeile 8 ---	1-5
	-/--	

[X] Weitere Veröffentlichungen sind der Fortsetzung von Feld C zu entnehmen

[X] Siehe Anhang Patentfamilie

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"&" Veröffentlichung, die Mitglied derselben Patentfamilie ist

Datum des Abschlusses der internationalen Recherche	Absendedatum des internationalen Recherchenberichts
9. Dezember 1998	16/12/1998

Name und Postanschrift der Internationalen Recherchenbehörde	Bevollmächtigter Bediensteter
Europäisches Patentamt, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	BERBAIN, F

1

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Nokia Exhibit 2004, p. 170
Amazon.com v. Nokia
IPR2024-01141

C.(Fortsetzung) ALS WESENTLICH ANGESEHENE UNTERLAGEN

Kategorie*	Bezeichnung der Veröffentlichung, soweit erforderlich unter Angabe der in Betracht kommenden Teile	Betr. Anspruch Nr.
A	EP 0 558 922 A (BUNDESREP DEUTSCHLAND) 8. September 1993 in der Anmeldung erwähnt siehe Anspruch 1 ---	1-5
A	SIU-LEONG IU: "COMPARISION OF MOTION COMPENSATION USING DIFFERENT DEGREES OF SUB- PIXEL ACCURACY FOR INTERFIELD/INTERFRAME HYBRID CODING OF HDTV IMAGE SEQUENCES" MULTIDIMENSIONAL SIGNAL PROCESSING, SAN FRANCISCO, MAR. 23 - 26, 1992, Bd. 3, Nr. CONF. 17, 23. März 1992, Seiten 465-468, XP000378969 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS siehe Zusammenfassung; Abbildung 1 ---	1-5
A	"MUNICH MEETING OF MPEG-4 WORKING GROUP. REPORT ISO/IEC JTC1/SC29/WG11 MPEG4/N1172" INTERNATIONAL ORGANISATION FOR STANDARDISATION - ORGANISATION INTERNATIONALE DE NORMALISATION, Januar 1996, Seiten 3-49, XP002047798 siehe Absatz 3.3.2.4 ---	1-5
A	EP 0 348 207 A (MATSUSHITA ELECTRIC IND CO LTD) 27. Dezember 1989 siehe Zusammenfassung -----	1-5

Nokia Exhibit 2004, p. 171
Amazon.com v. Nokia
IPR2024-01141

INTERNATIONALER RECHERCHENBERICHT

Angaben zu Veröffentlichungen, die zur selben Patentfamilie gehören

Internationales Aktenzeichen
PCT/DE 98/01938

Im Recherchenbericht angeführtes Patentdokument	Datum der Veröffentlichung	Mitglied(er) der Patentfamilie	Datum der Veröffentlichung
EP 0558922 A	08-09-1993	DE 4206622 A	09-09-1993
EP 0348207 A	27-12-1989	JP 2005689 A	10-01-1990
		JP 7028408 B	29-03-1995
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		US 5111511 A	05-05-1992

Nokia Exhibit 2004, p. 172
Amazon.com v. Nokia
IPR2024-01141

(11) Japanese Examined Publication: Hei 6-14739
(24) Date of Publication: 23/2/94
(21) Application No: Sho 60-180106
(22) Date of Application: 15/8/85
(73) Applicant: NEC Corporation

(54) Title: A movement compensation inter-frame prediction coding and decoding method for image signals and its devices

(57) Claims:
1. A movement compensation inter-frame prediction coding and decoding method for image signals comprising:
at a transmission side,
providing space interpolation of sampled input image signals so that the number of samples may be increased;
detecting blocks of a previous frame of said input image signals subjected to space interpolation, having the highest similarity to blocks of a present frame of said input image signals;
finding minority movement vectors showing drifts between said blocks of said present frame and said detected blocks of said previous frame;
finding prediction error signals and local decoded signals from said input image signals and prediction signals;
providing space interpolation of said local decoded signals;
providing variable delay of said local decoded signals subjected to space interpolation in accordance with said minority movement vectors to form said prediction signals; and
providing compression coding of said prediction error signals and said minority movement vectors before transmitted,
at a reception side,
providing extension decoding of said prediction error signals and said minority movement vectors, subjected to compression coding;
regenerating regenerative image signals from said prediction error signals subjected to extension decoding and reception-side prediction signals;
providing space interpolation of said regenerated image signals; and
providing variable delay of said regenerated image signals subjected to space interpolation in accordance with said minority movement vectors subjected to extension decoding to form said reception-side prediction signals.
2. A movement compensation inter-frame prediction coding

Nokia Exhibit 2004, p. 173
Amazon.com v. Nokia
IPR2024-01141

device for image signals comprising:
means for providing space interpolation of sampled input signals so that the number of samples may be increased;
means for detecting blocks of a previous frame of said input image signals subjected to space interpolation, having the highest similarity to blocks of a present frame of said input image signals, and finding minority movement vectors showing drifts between said blocks of said present frame and said detected blocks of said previous frame;
means for finding prediction error signals and local decoded signals from said input image signals and prediction signals;
means for providing space interpolation of said local decoded signals;
means for providing variable delay of said local decoded signals subjected to space interpolation in accordance with said minority movement vectors to form said prediction signals; and
means for providing compression coding of said prediction error signals and said minority movement vectors.
3. A movement compensation inter-frame prediction decoding device for image signals comprising:
means for detecting minority movement vectors in blocks for image signals, inputting signals consisting of prediction error signals, obtained by movement compensation inter-frame prediction coding in accordance with said minority movement vectors, and said minority movement vectors, both of which are subjected to compression coding, and providing extension decoding of said prediction error signals and said minority movement vectors, subjected to compression coding;
means for regenerating regenerative image signals from said prediction error signals subjected to extension decoding and reception-side prediction signals;
means for providing space interpolation of said regenerated image signals;
means for providing variable delay of said regenerated image signals subjected to space interpolation in accordance with said minority movement vectors subjected to extension decoding; and
means for providing space trimming of said regenerated image signals subjected to variable delay to form said reception-side prediction signals.

BACKGROUND OF THE INVENTION
[FIELD OF THE INVENTION]

The present invention relates to a movement compensation inter-frame prediction coding and decoding

Nokia Exhibit 2004, p. 174
Amazon.com v. Nokia
IPR2024-01141

method for image signals and its devices (referred to as "a prediction coding method" and "a prediction decoding method", and "a prediction coding device" and "a prediction decoding device", respectively), in particular, to a block matching type prediction coding and decoding method for efficiently coding and decoding image signals and its devices.

[PRIOR ART]

One of procedures in a prediction coding and decoding method for image signals is movement compensation inter-frame prediction coding and decoding. The method involve the use of signals of a previous frame drifted by movement vectors, instead of the direct use of signals of the previous frame, as prediction signals.

Fig.6 shows the movement of image signals in the movement compensation inter-frame prediction coding and decoding method. For example, as shown in Fig.6, a value for a prediction signal to a signal A on coordinates (X_0, Y_0) at a time $t=t_0$ is determined by a signal C on coordinates (X_0-V_X, Y_0-V_Y) in a front frame at a time $t=t_0-\tau$, if a movement vector is $\delta=(V_X, V_Y)$. The movement vector δ is the amount of displacement in one frame for an image near the signal A and its size and direction are generally different depending on the position of the signal A. In the method, if only the movement vector can be found precisely, the value for the signal C approximates the value for the signal A and so a prediction error signal gets to a small value, close to zero, producing higher coding efficiency. A block matching method or the like is proposed for how to find the movement vector. The block matching method is explained as follows:

An image is first divided into a number of blocks. Then, a number of drifted blocks is picked out of the previous frame and one block of the highest similarity is detected from them. Drifts between the blocks of the present frame and the blocks of the previous frame at this time are movement vectors. One example of the movement compensation inter-frame prediction coding using block matching is detailed in a paper "A movement compensation prediction system for inter-frame prediction coding" by *Ninomiya*, published in "1981 electronic communications institution magazine B" Vol.J64-B, No1, P24-P31.

[Problems of Prior Art]

In the above-described conventional movement compensation inter-frame prediction coding and decoding for image signals of lower space resolution, there is the disadvantage of producing more information content per

Nokia Exhibit 2004, p. 175
Amazon.com v. Nokia
IPR2024-01141

Page 175 of 350

picture element, than in the movement compensation inter-frame prediction coding and decoding for image signals of higher space resolution. The reason is as follows:

In case of the movement compensation inter-frame prediction coding and decoding when a true movement vector is located between picture elements, the quantitized movement vector is detected at the position of one of two picture elements during detecting the movement vector, because the true movement vector is not found. Therefore, the lower space resolution the image signals, the larger space between the picture elements, resulting in the movement vector to be detected more roughly, a larger value for the prediction error signal and more information content per picture element.

[Objects of the Present Invention]

An object of the invention is to provide a block matching type movement compensation inter-frame prediction coding and decoding method for image signals of lower pace resolution, wherein less information content per picture element is produced with less deterioration of imaging quality, than in the conventional block matching type movement compensation inter-frame prediction coding and decoding method, and to provide its devices.

[Configuration of the Invention]

1. A prediction coding and decoding method according this invention comprises:

at a transmission side,

providing space interpolation of sampled input image signals so that the number of samples may be increased;

detecting blocks of a previous frame of said input image signals subjected to space interpolation, having the highest similarity to blocks of a present frame of said input image signals;

finding minority movement vectors showing drifts between said blocks of said present frame and said detected blocks of said previous frame;

finding prediction error signals and local decoded signals from said input image signals and prediction signals;

providing space interpolation of said local decoded signals;

providing variable delay of said local decoded signals subjected to space interpolation in accordance with said minority movement vectors to form said prediction signals; and

providing compression coding of said prediction error signals and said minority movement vectors before transmitted,

Nokia Exhibit 2004, p. 176
Amazon.com v. Nokia
IPR2024-01141

at a reception side,
providing extension decoding of said prediction error signals and said minority movement vectors, subjected to compression coding;
regenerating regenerative image signals from said prediction error signals subjected to extension decoding and reception-side prediction signals;
providing space interpolation of said regenerated image signals; and
providing variable delay of said regenerated image signals subjected to space interpolation in accordance with said minority movement vectors subjected to extension decoding to form said reception-side prediction signals.

2. A prediction coding device according to this invention comprises:
means for providing space interpolation of sampled input signals so that the number of samples may be increased;
means for detecting blocks of a previous frame of said input image signals subjected to space interpolation, having the highest similarity to blocks of a present frame of said input image signals, and finding minority movement vectors showing drifts between said blocks of said present frame and said detected blocks of said previous frame;
means for finding prediction error signals and local decoded signals from said input image signals and prediction signals;
means for providing space interpolation of said local decoded signals;
means for providing variable delay of said local decoded signals subjected to space interpolation in accordance with said minority movement vectors to form said prediction signals; and
means for providing compression coding of said prediction error signals and said minority movement vectors.

3. A prediction decoding device according to this invention comprises:
means for detecting minority movement vectors in blocks for image signals, inputting signals consisting of prediction error signals, obtained by movement compensation inter-frame prediction coding in accordance with said minority movement vectors, and said minority movement vectors, both of which are subjected to compression coding, and providing extension decoding of said prediction error signals and said minority movement vectors, subjected to compression coding;
means for regenerating regenerative image signals from said prediction error signals subjected to extension decoding and reception-side prediction signals;

Nokia Exhibit 2004, p. 177
Amazon.com v. Nokia
IPR2024-01141

means for providing space interpolation of said regenerated image signals;
means for providing variable delay of said regenerated image signals subjected to space interpolation in accordance with said minority movement vectors subjected to extension decoding; and
means for providing space trimming of said regenerated image signals subjected to variable delay to form said reception-side prediction signals.

[Principle of the Invention]

Conventional movement compensation inter-frame prediction coding and decoding applied to image signals of lower space resolution makes values for prediction error signals, whose movement vectors are detected roughly, larger to produce more information content per picture element. In this invention, conventional block matching type movement compensation inter-frame prediction coding and decoding is changed in two following points:

(i) During detecting the movement vectors, the image signals of lower space resolution are subjected to space interpolation so that their fine movement can be detected which could not be detected before space interpolation.

(ii) After subjected to space interpolation, local decoding signals are subjected to minority picture element delay in accordance with minority movement vectors and then to space trimming again, whereby they are restored to their old resolution, not subjected under space interpolation, to form prediction signals.

At a position of a previous frame shown by the movement vectors detected in the above-described (i), no sampling point exists before space interpolation, and so the movement vectors are called minority movement vectors in this invention.

Since the prediction signals compensated for the fine movement can be formed in the procedures shown in the above-described (ii), accurate prediction is ensured, compared to that in the conventional block matching type movement compensation inter-frame prediction coding and decoding method for the image signals of lower space resolution.

[EMBODIMENTS]

The present invention is described with reference to the drawings.

Each of Fig.1 through Fig.4 is a block diagram showing a prediction coding device according to each of first through fourth embodiments of the invention, Fig.5 is a block diagram showing a prediction decoding device according to one embodiment of the invention and Fig.6 is

an explanatory drawing showing the movement of image signals between movement compensation frames in a prediction coding and decoding method.

In Fig.1, a first embodiment for the prediction coding device according to the invention is first described. Image signals applied to an input terminal 100 is supplied to a subtracting circuit 13, a block matching type minority movement vector detecting circuit 10 and a frame memory 11 capable of storing one frame. The image signals supplied to the frame memory 11 is sent to a space interpolating circuit 12, where they are subjected to space interpolation, and used in detecting minority movement vectors after about one frame time delay. In the block matching type minority movement vector detecting circuit 10, the image signals supplied from the input terminal 100 and image signals of a previous frame supplied from the space interpolating circuit 12 after space interpolation are used in detecting the movement of images. The minority movement vectors detected by the block matching type minority movement vector detecting circuit 10 are supplied to a variable delay circuit 19 and a compression coding circuit 21. In the subtracting circuit 13, a difference between the image signals supplied from the input terminal 100 and prediction signals supplied from a space trimming circuit 20 after space trimming is found. The difference, namely, prediction error signals, is supplied to a quantizing circuit 14 for quantization. The quantization includes linear quantization and non-linear quantization, one of which is selected. In the linear quantization, the low-order bits of the prediction error signals are trimmed and the number of the bits are thus reduced, providing less information content to be transmitted. In the non-linear quantization, the number of bits of the prediction error signals is reduced with quantizing operation in accordance with the characteristics of the non-linear quantization. The quantized prediction error signals are supplied to an inversely quantizing circuit 15 and the compression coding circuit 21. The prediction error signals supplied to the inversely quantizing circuit 15 are inversely quantized herein and then supplied to an adding circuit 16. The inverse quantization includes linear inverse quantization and non-linear inverse quantization, one of which is selected. In the linear inverse quantization, zeroes in number equivalent to the number of bits trimmed in the quantizing circuit 14 are added to the low-order positions of the prediction error signals to be restored to the number of their old bits, not subjected under quantization. In the non-linear inverse quantization, similar operation

Nokia Exhibit 2004, p. 179
Amazon.com v. Nokia
IPR2024-01141

of restoring the prediction error signals to the number of their old bits, not subjected under quantization, is carried out in accordance with the characteristics of the non-linear inverse quantization. In the adding circuit 16, the sum of the prediction error signals supplied from the inversely quantizing circuit 15 after inverse quantization and prediction signals supplied from the space trimming circuit 20 is found. The sum, namely, local decoding signals, is supplied to a frame memory 17, from which it is then output to a space interpolating circuit 18. In the space interpolating circuit 18, the local decoding signals are subjected to space interpolation and then supplied to the variable delay circuit 19. In the variable delay circuit 19, the prediction signals compensated for movement by using minority movement vectors supplied from the block matching type minority movement vector detecting circuit 10 are generated and then supplied to the space trimming circuit 20. In the space trimming circuit 20, the prediction signals are subjected to space trimming and then supplied to the subtracting circuit 13 and the adding circuit 16. In the compression coding circuit 21, the prediction error signals supplied from the quantizing circuit 14 after quantization and the minority movement vectors supplied from the block matching type minority movement vector detecting circuit 10 are subjected to compression coding and then output to a transmission passage 1000.

A second embodiment shown in Fig.2 is described, wherein the prediction coding device excludes the quantizing circuit 14 and the inversely quantizing circuit 15, shown in Fig.1. In the second embodiment, a difference between the image signals supplied from the input terminal 100 and the prediction signals supplied from the space trimming circuit 20 after space trimming, namely the prediction error signals, is applied to the compression coding circuit 21 and the adding circuit 16 as it is. In this case, high quality coded images with no quantization error are obtained.

A third embodiment shown in Fig.3 is described, wherein the prediction coding device has a function equal to that of the prediction coding device which excludes the quantizing circuit 14 and the inversely quantizing circuit 15, shown in Fig.1, and a structure different from that in the second embodiment. In the third embodiment, image signals supplied from an input terminal 300 are applied to a subtracting circuit 33 and also applied to a frame memory 34. The image signals applied to the frame memory 34 are passed through a space interpolating circuit 35, a variable

delay circuit 36 and a space trimming circuit 37, subjected to movement vector delay and then applied to the subtracting circuit 33. In the subtracting circuit 33, a difference between the image signals subjected to the movement vector delay and image signals subjected to completely no delay is operated, and the difference signals are given to a compression coding circuit 38.

In the first embodiment shown in Fig.1, orthogonal transformation such as Discrete Cosine Transform (DCT), instead of quantization, can be performed, which is properly selected for purposes.

In a fourth embodiment, another prediction coding device may be considered, which uses input image signals and local decoding signals subjected to space interpolation during detecting movement vectors. In the fourth embodiment shown in Fig.4, a block matching type minority movement vector detecting circuit 40 detects movement vectors by comparing the image signals supplied from an input terminal 400 with local decoding signals obtained from a space interpolating circuit 46 after space interpolation, and applies them to a variable delay circuit 47. In this case, only one frame memory is required, resulting in a simple structure.

One embodiment of the prediction decoding device according to the invention is described with reference to Fig.5. Signals supplied from a transmission passage 5000 after compression coding are supplied to an extension decoding circuit 50. In the extension decoding circuit 50, prediction error signals subjected to compression decoding and minority movement vectors are subjected to extension decoding and then supplied to an inversely quantizing circuit 51 and a variable delay circuit 55, respectively. In the inversely quantizing circuit 51, the prediction error signals quantized are inversely quantized and then supplied to an adding circuit 52. In the adding circuit 52, image signals are subjected to prediction decoding from the prediction error signals supplied from the inversely quantizing circuit 51 after inverse quantization and the prediction signals supplied from a space trimming circuit 56. The image signals subjected to prediction decoding are supplied to an output terminal 500 and a frame memory 53. The image signals supplied to the frame memory 53 is sent to a space interpolating circuit 54 where they are subjected to space interpolation, and then supplied to a variable delay circuit 55 to generate prediction signals. In the variable delay circuit 55, the prediction signals are generated in accordance with minority movement vectors supplied from the extension decoding circuit 50, and then

supplied to a space trimming circuit 56. In the space trimming circuit 56, the prediction signals are subjected to space trimming and then supplied to an adding circuit 52.

[Effects of the Invention]

According to the invention as above-described,

(i) during the detection of the movement vectors, the image signals of lower space resolutions are subjected to space interpolation so that their fine movement, which could not be detected before space interpolation, can be detected.

(ii) After subjected to space interpolation, local decoding signals are subjected to minority picture element delay in accordance with minority movement vectors and then to space trimming again, whereby they are restored to their old resolution, not subjected under space interpolation, to form prediction signals.

This causes fine detection and accurate prediction of the movement vectors, compared to those in the conventional block matching type movement compensation inter-frame prediction coding and decoding method for the image signals of lower space resolution, advantageously producing smaller values for the prediction error signals and less information content per picture element.

BRIEF DESCRIPTION OF THE DRAWINGS

Each of Fig.1 through Fig.4 is a block diagram showing a prediction coding device according to each of first through fourth embodiments of the invention, Fig.5 is a block diagram showing a prediction decoding device according to one embodiment of the invention and Fig.6 is an explanatory drawing showing the movement of image signals between movement compensation frames in a prediction coding and decoding method.

In the drawings,

10, 30, 40: block matching type minority movement vector circuit,
11, 17, 31, 34, 45, 53: frame memory,
12, 18, 32, 35, 46, 54: space interpolating circuit,
13, 33, 41: subtracting circuit,
14, 42: quantizing circuit,
15, 43, 51: inversely quantizing circuit,
16, 44, 52: adding circuit,
19, 36, 47, 55: variable delay circuit,
20, 37, 48, 56: space trimming circuit,
21, 38, 49: compression coding circuit,
50: extension decoding circuit,
100, 300, 400: input terminal,

Nokia Exhibit 2004, p. 182
Amazon.com v. Nokia
IPR2024-01141

Page 182 of 350

500: output terminal,
1000, 3000, 4000, 5000: transmission passage

Nokia Exhibit 2004, p. 183
Amazon.com v. Nokia
IPR2024-01141

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(54) METHOD AND APPARATUS FOR FORECAST CODING AND DECODING OF DYNAMIC COMPENSATION INTER-FRAME OF PICTURE SIGNAL

(57) Abstract:

PURPOSE: To reduce information per picture element while suppressing deterioration of picture quality by applying spatial interpolation to a local decoding signal, applying variable delay to the local decoding signal subjected to spatial interpolation according to a minority dynamic vector to form a forecast signal.

CONSTITUTION: In detecting a dynamic vector, minute movement not detected before spatial interpolation is detected by applying spatial interpolation to a picture signal with deteriorated spatial resolution. After a local decoding signal is subjected to spatial interpolation, a few picture elements are retarded according to the minority dynamic vector. Then spatial interleaving is applied to restore the resolution to the resolution before spatial interpolation and the result is used as a forecast signal. Thus, in comparison with the application of the conventional block matching dynamic compensation inter-frame forecast coding and decoding method, the dynamic vector is detected in detail and more suitable forecast is applied, then the value of the forecast error signal is decreased and the information quantity per picture element is reduced.

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Nokia Exhibit 2004, p. 184
Amazon.com v. Nokia
IPR2024-01141

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審査請求　未請求　発明の数 3　（全7頁）

⑤4発明の名称　画像信号の動き補償フレーム間予測符号化・復号化方法とその装置

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明　細　書

1. 発明の名称

画像信号の動き補償フレーム間予測符号化・復号化方法とその装置

2. 特許請求の範囲

(1)送信側に於いては、標本化された入力画像信号の標本点数が多くなるように空間補間し、前記入力画像信号の現フレームのブロックと類似度が最も高い空間補間された前記入力画像信号の前フレームのブロックを検出し、前記現フレームのブロックと検出された前記前フレームのブロックとの位置のずれを示す小数動きベクトルを求め、前記入力画像信号と予測信号より予測誤差信号と局部復号信号を求め、前記局部復号信号を空間補間し、空間補間された前記局部復号信号を前記小数動きベクトルに従って可変遅延して前記予測信号を作成し、前記予測誤差信号と前記小数動きベクトルとを圧縮符号化して伝送し、受信側に於いては、圧縮符号化された前記予測誤差信号と前記小数動きベクトルとを伸張復号化し、伸張復号化された前記予測誤差信号と受信側予測信号より再生画像信号を再生し、前記再生画像信号を空間補間し、空間補間された前記再生画像信号を伸張復号化された前記小数動きベクトルに従って可変遅延して前記受信側予測信号とすることを特徴とする画像信号の動き補償フレーム間予測符号化・復号化方法。

(2)標本化された入力画像信号の標本点数が多くなるように空間補間する手段と、前記入力画像信号の現フレームのブロックと類似度が最も高い空間補間された前記入力画像信号の前フレームのブロックを検出し、前記現フレームのブロックと検出された前記前フレームのブロックの位置のずれを示す小数動きベクトルを求める手段と、前記入力画像信号と予測信号より予測誤差信号と局部復号信号を求める手段と、前記局部復号信号を空間補間する手段と、空間補間された前記局部復号信号を前記小数動きベクトルに従って可変遅延して前

Nokia Exhibit 2004, p. 185
Amazon.com v. Nokia
IPR2024-01141

Page 185 of 350

記予測信号を作成する手段と、前記予測誤差信号と前記小数動きベクトルとを圧縮符号化する手段とを具備することを特徴とする画像信号の動き補償フレーム間予測符号化装置。

(3)画像信号に対してブロック毎に小数動きベクトルを検出し、前記小数動きベクトルに従って動き補償フレーム間予測符号化することにより得られる予測誤差信号と前記小数動きベクトルとを圧縮符号化した信号を入力し、圧縮符号化された前記予測誤差信号と前記小数動きベクトルとを伸張復号化する手段と、伸張復号化された前記予測誤差信号と受信側予測信号より再生画像信号を再生する手段と、前記再生画像信号を空間補間する手段と、空間補間された前記再生画像信号を伸張復号化された前記小数動きベクトルに従って可変遅延する手段と、可変遅延された前記再生画像信号を空間間引きして前記受信側予測信号とする手段とを具備することを特徴とする画像信号の動き補償フレーム間予測復号化装置。

3. 発明の詳細な説明

＜産業上の利用分野＞

本発明は画像信号の動き補償フレーム間予測符号化・復号化方法とその装置（以下予測符号化方法、予測復号化方法、予測符号化装置および予測復号化装置と称す）に関し、特に画像信号の効率的な符号化および復号化を行うブロックマッチング型の予測符号化・復号化方法とその装置に関する。

＜従来技術＞

画像信号の予測符号化・復号化方法に動き補償フレーム間の予測符号化・復号化がある。この方法では、予測信号として前フレーム信号を直接用いず動きベクトルだけずれた前フレームの信号を用いる。

第6図は動き補償フレーム間の予測符号化・復号化方法の画像信号の動きを示す説明図である。たとえば第6図に示すように、時間 $t = t_0$ における座標（X_0, Y_0）の信号Aに対する予測信号の値は動きベクトルが $\vec{V} = (V_X, V_Y)$ であるなら、

時間 $t = t_0 - \tau$ の前フレームに於ける座標が（$X_0 - V_X$, $Y_0 - V_Y$）の信号Cによって定める。ここで動きベクトル $\vec{V}$ は信号Aの近傍の画像に於ける1フレーム間の変位量でありその大きさおよび向きは一般に信号Aの位置により異なる。この方法では動きベクトルさえ精度良く求まれば信号Cは信号Aと非常に近い値となるので予測誤差信号は0に近い小さな値となり符号化効率は高くなる。動きベクトルの求め方としてはブロックマッチング法等が提案されている。以下ブロックマッチング法について説明する。まず画面を多数のブロックに分割する。そして各々のブロックについて、前フレーム中に多数の位置のずれたブロックを取りその中で最も類似度の高いブロックを検出する。この時の現フレームのブロックと前フレームのブロックのずれを動きベクトルとする。ブロックマッチングを用いた動き補償フレーム間予測符号化については、その一例が1981年電子通信学会論文誌B VOL. J64-B No.1 P24-P31に掲載されている二宮らによる論文

＜フレーム間予測符号化に於ける動き補正予測方式＞に詳しく書かれている。

＜従来技術の問題点＞

以上述べたような従来の、空間解像度の低下した画像信号に対して動き補償フレーム間予測符号化・復号化を行う例においては、それより空間解像度の高い画像信号に対して動き補償フレーム間予測符号化・復号化を行うときに比べて画素当たりの情報量が増加するという欠点がある。その理由は以下のとおりである。動き補償フレーム間予測符号化・復号化の場合、画素と画素の間の位置に真の動きベクトルがくるときには、動きベクトル検出をする際、真の動きベクトルが求まらず2画素のうちのいずれかの画素の位置に量子化された動きベクトルが検出される。そのため画像信号の空間解像度が低下するほど、画素と画素の間隔は大きくなり動きベクトルが粗く検出され、予測誤差信号の値が大きくなり画素当たりの情報量が増加するというわけである。

＜発明の目的＞

Nokia Exhibit 2004, p. 186
Amazon.com v. Nokia
IPR2024-01141

Page 186 of 350

本発明の目的は、空間解像度の低下した画像信号に対して、従来のブロックマッチング型の動き補償フレーム間予測符号化・復号化方法に比べて画質の劣化を抑えつつ画素当たりの情報量を削減するブロックマッチング型の動き補償フレーム間予測符号化・復号化方法およびその装置を提供することにある。

＜発明の構成＞

(1)本発明の予測符号化・復号化方法は、送信側においては、標本化された入力画像信号の標本点数が多くなるように空間補間し、前記入力画像信号の現フレームのブロックと類似度が最も高い空間補間された前記入力画像信号の前フレームのブロックを検出し、前記現フレームのブロックと検出された前記前フレームのブロックとの位置のずれを示す小数動きベクトルを求め、前記入力画像信号と予測信号より予測誤差信号と局部復号信号を求め、前記局部復号信号を空間補間し、空間補間された前記局部復号信号を前記小数動きベクトルに従って可変遅延して前記予測信号を作成し、前

記予測誤差信号と前記小数動きベクトルとを圧縮符号化して伝送し、受信側においては、圧縮符号化された前記予測誤差信号と前記小数動きベクトルとを伸張復号化し、伸張復号化された前記予測誤差信号と受信側予測信号より再生画像信号を再生し、前記再生画像信号を空間補間し、空間補間された前記再生画像信号を伸張復号化された前記小数動きベクトルに従って可変遅延して前記受信側予測信号としている。

(2)また本発明の予測符号化装置は、標本化された入力画像信号の標本点数が多くなるように空間補間する手段と、前記入力画像信号の現フレームのブロックと類似度が最も高い空間補間された前記入力画像信号の前フレームのブロックを検出し、前記現フレームのブロックと検出された前記前フレームのブロックの位置のずれを示す小数動きベクトルを求める手段と、前記入力画像信号と予測信号より予測誤差信号と局部復号信号を求める手段と、前記局部復号信号を空間補間する手段と、空間補間された前記局部復号信号を前記小数動き

ベクトルに従って可変遅延して前記予測信号を作成する手段と、前記予測誤差信号と前記小数動きベクトルとを圧縮符号化する手段とを具備している。

(3)さらにまた本発明の予測復号化装置は、画像信号に対してブロック毎に小数動きベクトルを検出し、前記小数動きベクトルに従って動き補償フレーム間予測符号化することにより得られる予測誤差信号と前記小数動きベクトルとを圧縮符号化した信号を入力し、圧縮符号化された前記予測誤差信号と前記小数動きベクトルとを伸張復号化する手段と、伸張復号化された前記予測誤差信号と受信側予測信号より再生画像信号を再生する手段と、前記再生画像信号を空間補間する手段と、空間補間された前記再生画像信号を伸張復号化された前記小数動きベクトルに従って可変遅延する手段と、可変遅延された前記再生画像信号を空間間引きして前記受信側予測信号とする手段とを具備している。

＜本発明の原理＞

空間解像度の低下した画像信号に対して、従来の動き補償フレーム間予測符号化・復号化を行うと、動きベクトルが粗く検出され予測誤差信号の値が大きくなり、画素当たりの情報量が増加する。そこで本発明に於いては、次の2点について従来のブロックマッチング型の動き補償フレーム間予測符号化・復号化を変更する。

(I)動きベクトルを検出する際、空間解像度の低下した画像信号を空間補間することによって空間補間する前には検出できなかった細かい動きを検出する。

(II)局部復号信号を空間補間したのち小数動きベクトルに従って小数画素遅延する。そして再び空間間引きを行い空間補間する前の解像度に戻しこれを予測信号とする。

上述の(I)のようにして検出された動きベクトルによって示される前フレームの位置には、空間補間する前には標本点が存在しないため、この動きベクトルを小数動きベクトルと本発明に於いては称する。

Nokia Exhibit 2004, p. 187
Amazon.com v. Nokia
IPR2024-01141

Page 187 of 350

また上述の(II)のようにすると細かい動きを補償した予測信号を作成することが可能であるため、空間解像度の低下した画像信号に対して従来のブロックマッチング型の動き補償フレーム間予測符号化・復号化を行う場合に比べて、予測を適確に行なうことが可能である。

＜実施例＞

次に、本発明について図面を参照して説明する。

第1図ないし第4図は本発明の予測符号化装置のそれぞれ第1ないし第4の実施例のブロック図、第5図は本発明の予測復号化装置の一実施例のブロック図、第6図は動き補償フレーム間の予測符号化・復号化方法の画像信号の動きを示す説明図である。

始めに第1図により、本発明の予測符号化装置の第1の実施例について説明する。入力端子100に加えられた画像信号は減算回路13とブロックマッチング型小数動きベクトル検出回路10と1フレームを記憶できるフレームメモリ11に供給される。フレームメモリ11に供給された画像信

－11－

子化操作が行なわれ予測誤差信号のビット数が低減される。この量子化された予測誤差信号は逆量子化回路15と圧縮符号化回路21に供給される。逆量子化回路15に供給された予測誤差信号はここで逆量子化され加算回路16に供給される。逆量子化に於いても線形逆量子化および非線形逆量子化等がありいずれかが選択される。線形逆量子化に於いては、予測誤差信号の下位に量子化回路14で削減したビット数だけ0を加え量子化する前のビット数に戻すという操作が行われる。また非線形逆量子化に於いても、非線形逆量子化特性に従って量子化する前のビット数に戻すという操作が行われる。加算回路16に於いては、逆量子化回路15から供給される逆量子化された予測誤差信号と空間間引き回路20から供給される予測信号との和が求められる。この和すなわち局部復号信号はフレームメモリ17に供給されたのち空間補間回路18に出力される。空間補間回路18に於いては、局部復号化信号が空間補間され可変遅延回路19に

－13－

号は空間補間回路12に送られここで空間補間され、およそ1フレーム時間遅延したのちに小数動きベクトル検出に用いられる。ブロックマッチング型小数動きベクトル検出回路10に於いては、入力端子100から供給される画像信号と空間補間回路12から供給される空間補間された前フレームの画像信号とを用いて画像の動きを検出する。ブロックマッチング型小数動きベクトル検出回路10に於いて検出された小数動きベクトルは可変遅延回路19と圧縮符号化回路21に供給される。減算回路13に於いては、入力端子100から供給される画像信号と空間間引き回路20から供給される空間間引きされた予測信号との差が求められる。この差すなわち予測誤差信号は量子化回路14に供給され量子化される。量子化には、線形量子化および非線形量子化等があり、いずれかが選択される。線形量子化に於いては予測誤差信号の下位ビットを削減しビット数を低減することによって伝送すべき情報量を削減する。また非線形量子化に於いては、非線形量子化特性に従って量

－12－

於いては、ブロックマッチング型小数動きベクトル検出回路10から供給される小数動きベクトルを用いて動き補償された予測信号を発生し空間間引き回路20に供給する。空間間引き回路20に於いては、予測信号が空間間引きされ、減算回路13と加算回路16に供給される。圧縮符号化回路21に於いては、量子化回路14から供給される量子化された予測誤差信号とブロックマッチング型小数動きベクトル検出回路10から供給される小数動きベクトルとが圧縮符号化され伝送路1000に出力される。

次に第2図に示す第2の実施例は、第1図における量子化回路14および逆量子化回路15のない予測符号化装置である。この第2の実施例では、入力端子100から供給される画像信号と空間間引き回路20から供給される空間間引きされた予測信号との差、すなわち予測誤差信号は、そのまま圧縮符号化回路21および加算回路16に加えられる。この場合には、量子化誤差のない高品質の符号化画像が得られる。

－14－

Nokia Exhibit 2004, p. 188
Amazon.com v. Nokia
IPR2024-01141

Page 188 of 350

また第3図に示す第3の実施例は、第1図における量子化回路14および逆量子化回路15のない予測符号化装置と等価な機能を持ち、第2の実施例とは異なる構成の予測符号化装置である。この第3の実施例では、入力端子300から供給される画像信号は減算回路33へ加えられるとともに、フレームメモリ34にも加えられる。フレームメモリ34に加えられた画像信号は、空間補間回路35、可変遅延回路36、空間間引き回路37を経て、動きベクトルだけ遅延され、減算回路33に加えられる。減算回路33では、この動きベクトルだけ遅延された画像信号と、全く遅延を受けない画像信号との差がとられ、この差信号が圧縮符号化回路38に与えられる。

さらに、第1図に示す第1の実施例で量子化の代りにDCT（Discrete Cosine Transform、ディスクリートコサイン変換）などの直交変換を行うことも可能であり、これらは目的に応じて適宜選択される。

他に、第4の実施例として動きベクトルを検出

－16－

する際に、入力画像信号と空間補間された局部復号信号を使う予測符号化装置も考えられる。第4図に示す第4の実施例では、ブロックマッチング型小数動きベクトル検出回路40は、入力端子400から供給された画像信号と空間補間回路46から得られる空間補間された局部復号信号を比較することにより動きベクトルを検出し、可変遅延回路47に加える。この場合には、フレームメモリが一つで済むため装置構成が簡単となる。

次に、本発明の予測復号化装置の一実施例について、第5図により説明する。伝送路5000より供給される圧縮符号化された信号は伸張復号化回路50に供給される。伸張復号化回路50に於いては、圧縮復号化された予測誤差信号と小数動きベクトルが伸張復号化され、それぞれ逆量子化回路51と可変遅延回路55に供給される。逆量子化回路51に於いては、量子化された予測誤差信号が逆量子化され加算回路52に供給される。加算回路52に於いては、逆量子化回路51から供給される逆量子化された予測誤差信号と空間間引

－17－

き回路56から供給される予測信号とから画像信号が予測復号化される。予測復号化された画像信号は出力端子500とフレームメモリ53に供給される。フレームメモリ53に供給された画像信号は空間補間回路54に送られ、ここで空間補間され予測信号を発生するために可変遅延回路55に供給される。可変遅延回路55に於いては、伸張復号化回路50から供給される小数動きベクトルに従って予測信号を発生し空間間引き回路56に供給する。空間間引き回路56に於いては、予測信号が空間間引きされ加算回路52に供給される。

＜発明の効果＞

以上説明したように本発明は、

(i)動きベクトルを検出する際、空間解像度の低下した画像信号を空間補間することによって空間補間する前には検出できなかった細かい動きを検出する

(ii)局部復号信号を空間補間したのち小数動きベクトルに従って小数画素遅延する。そして再び空間

－18－

間引きを行い空間補間する前の解像度に戻しこれを予測信号とする

ことにより、空間解像度の低下した画像信号に対し、従来のブロックマッチング型の動き補償フレーム間予測符号化・復号化方法を適用する場合に比べて、動きベクトルが細かく検出され予測をより的確に行うことができ、そのため予測誤差信号の値が小さくなり、画素当たりの情報量が低減できる効果がある。

4. 図面の簡単な説明

第1図ないし第4図は本発明の予測符号化装置のそれぞれ第1ないし第4の実施例のブロック図、第5図は本発明の予測復号化装置の一実施例のブロック図、第6図は動き補償フレーム間の予測符号化・復号化方法の画像信号の動きを示す説明図である。

10，30，40……ブロックマッチング型小数動きベクトル検出回路、11，17，31，34，45，53……フレームメモリ、12，

－19－

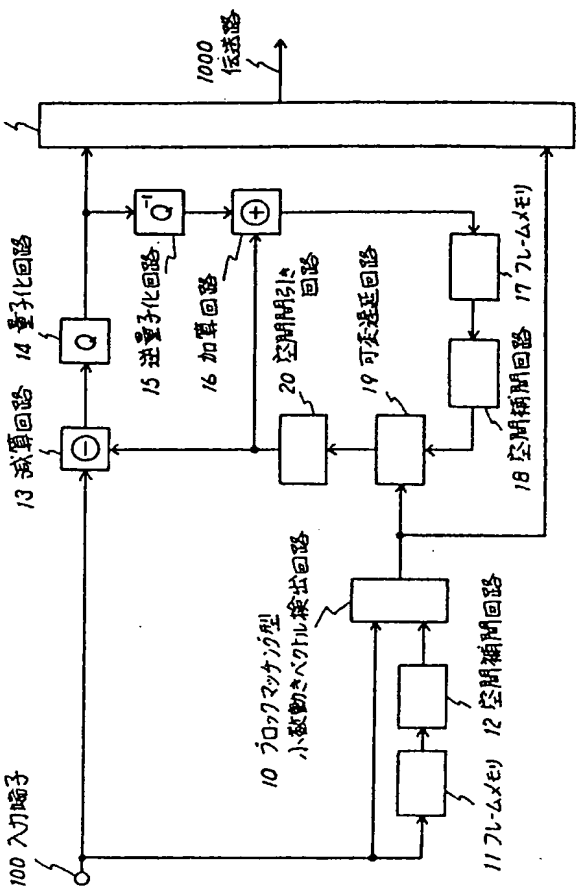
Nokia Exhibit 2004, p. 189
Amazon.com v. Nokia
IPR2024-01141

Page 189 of 350

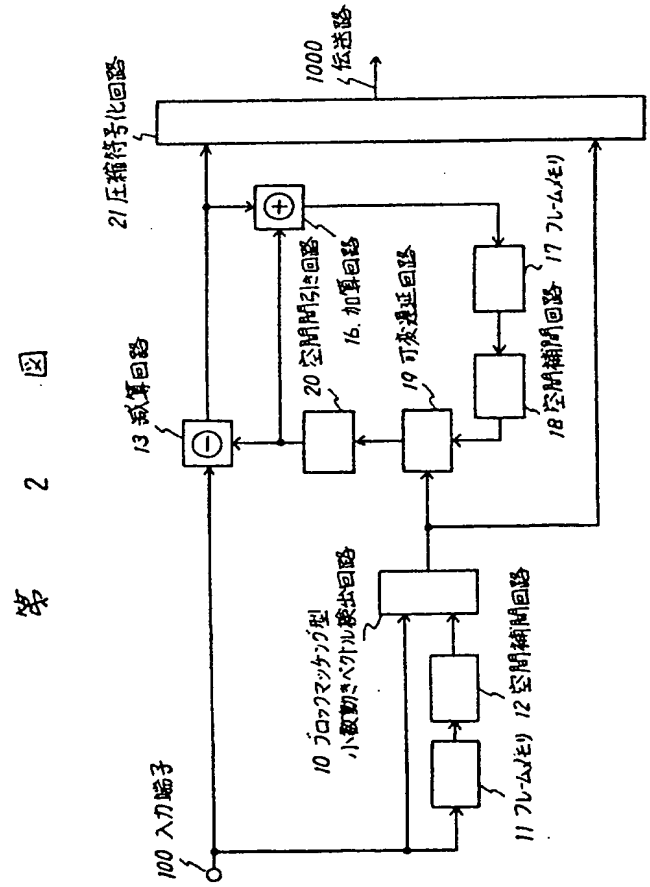
18，32，35，46，54……空間補間回路、13，33，41……減算回路、14，42……量子化回路、15，43，51……逆量子化回路、16，44，52……加算回路、19，36，47，55……可変遅延回路、20，37，48，56……空間間引き回路、21，38，49……圧縮符号化回路、50……伸長復号化回路、100，300，400……入力端子、500……出力端子、1000，3000，4000，5000……伝送路。

代理人　弁理士　内原　晋

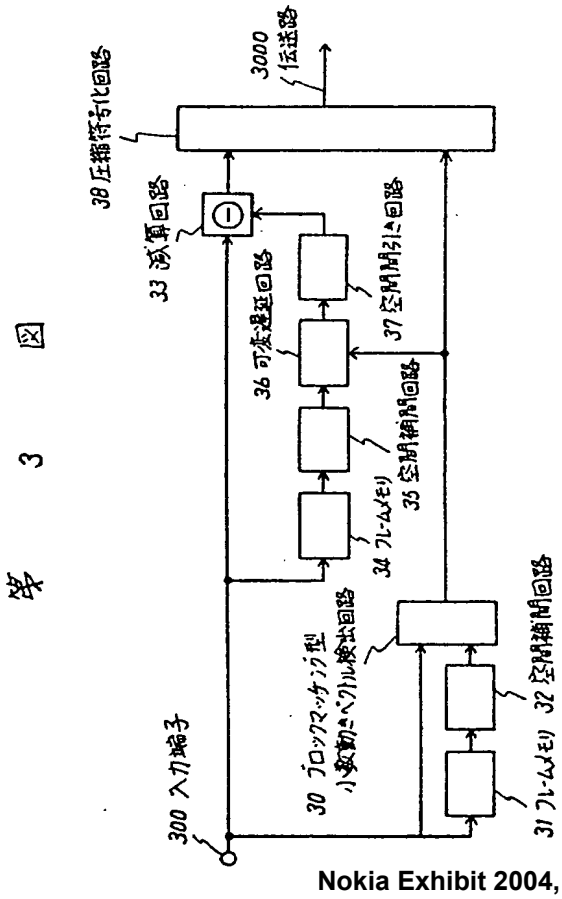
第1図



第2図



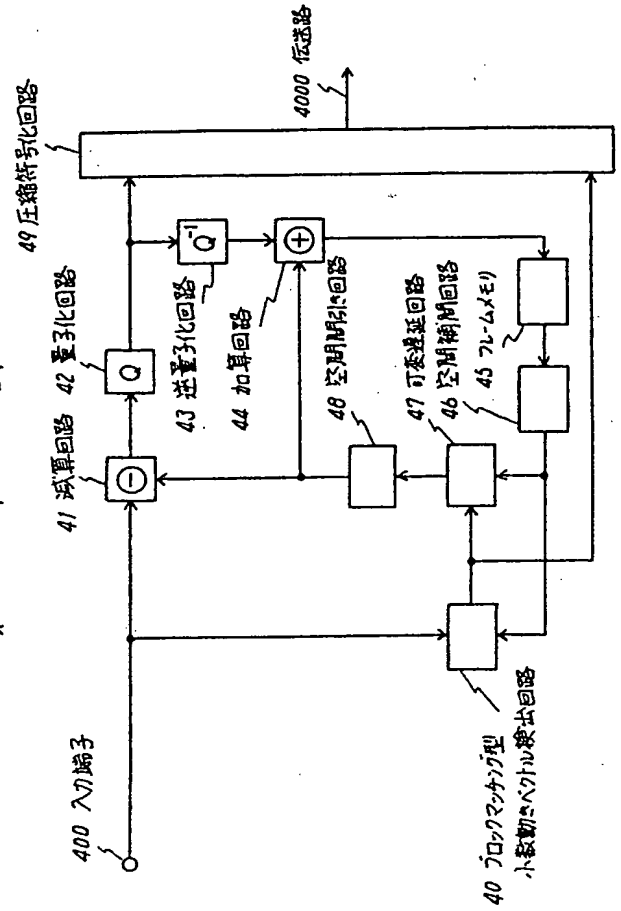
第3図



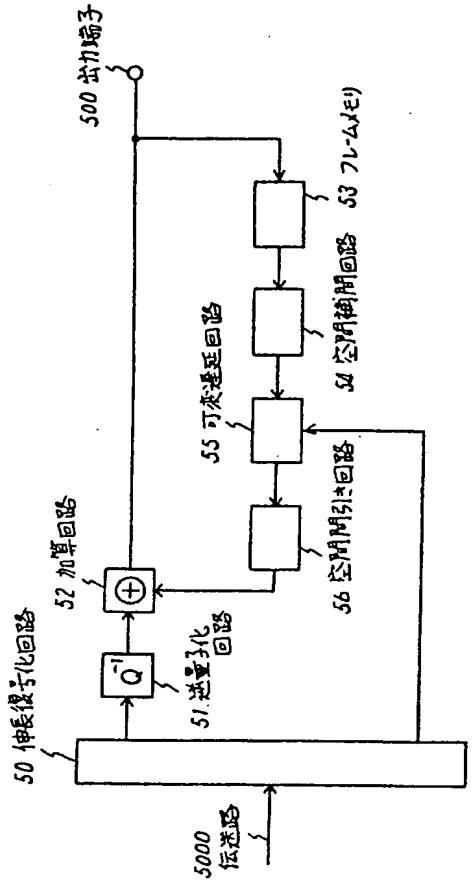
Nokia Exhibit 2004, p. 190
Amazon.com v. Nokia
IPR2024-01141

Page 190 of 350

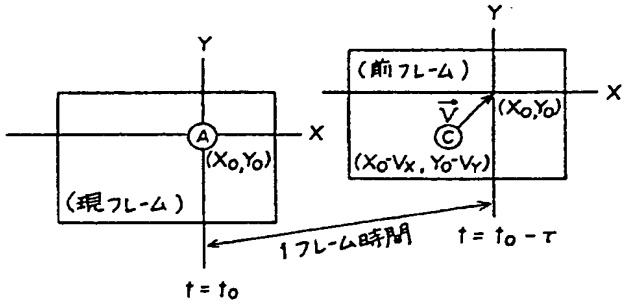
第4図



第5図



第6図



Nokia Exhibit 2004, p. 191
Amazon.com v. Nokia
IPR2024-01141

Page 191 of 350

OIPE JC
JAN 08 2002
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(s): Karczewicz et al.

SERIAL NO.: 09/954,608 ART UNIT:

FILING DATE: 9/17/01 EXAMINER:

TITLE: METHOD FOR SUB-PIXEL VALUE INTERPOLATION

ATTORNEY DOCKET NO.: 442-010567-US (PAR)

Commissioner of Patents
Washington, D.C. 20231

01/15/2002 SMINASS1 00000033 161350 09954608
01 FC:102 8.00 CH 160.00 OP

SUPPLEMENTAL PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified patent application as follows:

IN THE CLAIMS:

Please replace the following claim(s) as rewritten below:

---

23. (Amended) A video coder for coding an image comprising pixels arranged in rows and columns and represented by values having a specified dynamic range, the pixels in the rows residing at unit horizontal locations and the pixels in the columns residing at unit vertical locations, the video coder comprising an interpolator adapted to generate values for sub-pixels at fractional horizontal and vertical locations, the fractional horizontal and vertical locations being defined

09/08/2004 PZEWDIE1 00000001 09954608
01 FC:1202 35.00 DA

Nokia Exhibit 2004, p. 192
Amazon.com v. Nokia
IPR2024-01141

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 09/954608

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	47 minus 20= *	27
INDEPENDENT CLAIMS	11 minus 3 =	8
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	379.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	486. BD
X42=		OR	X80=	640.
+140=		OR	+280=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 49	Minus	** 47	= 2
Independent	* 13	Minus	*** 11	= 2
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	36. BD.
X42=		OR	X84=	168.
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 2.

Nokia Exhibit 2004, p. 193
Amazon.com v. Nokia
IPR2024-01141

JAN 16 2002
PAT & TRADEMARK OFFICE

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/954,608	09/17/2001	Marta Karczewicz	~~456-~~010567-US(PAR)

442

CONFIRMATION NO. 8282

2512
PERMAN & GREEN
425 POST ROAD
FAIRFIELD, CT 06430

FORMALITIES LETTER

OC000000006974327

Date Mailed: 10/25/2001

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(l) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.
- **The balance due by applicant is $ 130.**

Adjustment date: 10/24/2002 EEKUMSY1
07/16/2002 MTEKLEMI 00000010 161350 09954608
01 FC:103 36.00 CR

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202
PART 2 - COPY TO BE RETURNED WITH RESPONSE

1/22/2002 NMOHAMM1 00000094 09954608
1 FC:105 130.00 CP
07/16/2002 MTEKLEMI 00000010 161350 09954608
01 FC:103 36.00 CR

Nokia Exhibit 2004, p. 194
Amazon.com v. Nokia
IPR2024-01141

M-E Sector 4

Response To Notice To File Missing Parts Of Application Filing Date Granted (PTO-1533)(Large Entity)	Docket No. 442-010567-US(PAR)

In Re Application Of: **KARCZEWICZ et al.**

OIPE JC156 JAN 16 2002 PATENT & TRADEMARK OFFICE

COPY OF PAPERS ORIGINALLY FILED

Serial No.	Filing Date	Examiner	Group Art Unit
09/954,608	9/17/01		

Invention:

METHOD FOR SUB-PIXEL VALUE INTERPOLATION

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Box Missing Parts

This is a response to the Notice to File Missing Parts of Application - Filing Date Granted (PTO-1533) mailed on 10/25/2001 (*Date*).

Enclosed herewith for filing are the following:

- ☒ A copy of the Notice to File Missing Parts of Application - Filing Date Granted (PTO-1533). **(REQUIRED)**
- ☒ An oath or declaration in compliance with 37 CFR 1.63, including residence information and identifying the application by the above Application Number and Filing Date.
- ☐ A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date.
- ☐ An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date.
- ☐ A verified English translation of the non-English language application papers as originally filed. It is requested that this translation be used as the copy for examination purposes in the United States Patent and Trademark Office.
- ☐ Other (list):

Nokia Exhibit 2004, p. 195
Amazon.com v. Nokia
IPR2024-01141

Response To Notice To File Missing Parts Of Application Filing Date Granted (PTO-1533)(Large Entity)	Docket No. 442-010567-US(PAR)

In Re Application Of: **KARCZEWICZ et al.**

OIPE JC168 JAN 16 2002 PATENT & TRADEMARK OFFICE

Serial No.	Filing Date	Examiner	Group Art Unit
09/954,608	9/17/01		

Invention:

METHOD FOR SUB-PIXEL VALUE INTERPOLATION

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Box Missing Parts

COPY OF PAPERS ORIGINALLY FILED

☒ Completion of application fees as calculated below:

☐ Utility application filing fee	
☐ Design application filing fee	
☐ Total number of independent claims = _____	
☐ Total number of claims = _____	
☐ Multiple dependent claims	
☒ Surcharge for late payment of filing fee and/or late filing of original declaration or oath	**$130.00**
☐ Petition and fee for filing by other than all the inventors or a person not the inventor	
☐ Fee for processing an application filed with a non-English language specification	
☐ Fee for processing and retention of application	
Total completion of application fees	**$130.00**

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a response to the above-identified Notice to File Missing Parts of Application. The requested extension is as follows (check time period desired). If an additional time extension is required, please consider this a petition therefor.

☐ One month ☐ Two months ☐ Three months ☐ Four months ☐ Five months

from: _____ *Date* until: _____ *Date*

Total time extension fee

Total fees due **$130.00**

Nokia Exhibit 2004, p. 196
Amazon.com v. Nokia
IPR2024-01141

Response To Notice To File Missing Parts Of Application Filing Date Granted (PTO-1533) (Large Entity)	Docket No. 442-010567-US(PAR)

In Re Application Of: **KARCZEWICZ et al.**

OIPE SC1600
JAN 16 2002
PATENT & TRADEMARK OFFICE

Serial No.	Filing Date	Examiner	Group Art Unit
09/954,608	9/17/01		

Invention:

METHOD FOR SUB-PIXEL VALUE INTERPOLATION

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TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Box Missing Parts

The fee of **$130.00** is to be paid as follows:

- ☒ A check in the amount of the fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account No. **16-1350**
  A duplicate copy of this sheet is enclosed.
- ☒ If an additional extension of time is required, please consider this a petition therefor and charge any additional fees which may be required to Deposit Account No. **16-1350**
  A duplicate copy of this sheet is enclosed.

Signature

Dated: 15 Nov 01

Clarence A. Green, Reg. No. 24,622
Perman & Green, LLP
203-259-1800

I certify that this document and fee is being deposited on November 15, 2001 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Deborah J. Clark

Signature of Person Mailing Correspondence

DEBORAH J. CLARK

Typed or Printed Name of Person Mailing Correspondence

Customer No. 2512

cc:

Nokia Exhibit 2004, p. 197
Amazon.com v. Nokia
IPR2024-01141

(3)

OIPE JC100 JAN 16 2002 PATENT & TRADEMARK OFFICE

Attorney's Docket No. _____ **PATENT**

COMBINED DECLARATION AND POWER OF ATTORNEY

ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION OR C-I-P)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type: (check one applicable item below)

- ☒ original
- ☐ design
- ☐ supplemental

NOTE: If the declaration is for an International Application being filed as a divisional, continuation or continuation-in-part application, do not check next item; check appropriate one of last three items.

- ☐ national stage of PCT

NOTE: if one of the following 3 items apply, then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION OR C-I-P.

- ☐ divisional
- ☐ continuation
- ☐ continuation-in-part (C-I-P)

INVENTORSHIP IDENTIFICATION

WARNING: If the inventors are each not the inventors of all the claims, an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

Method for sub-pixel value interpolation

SPECIFICATION IDENTIFICATION

the specification of which: (complete (a), (b) or (c))

(a) ☐ is attached hereto.
(b) ☒ was filed on 17 Sep. 2001 as ☒ Serial No. 09/954,608
or ☐ Express Mail No., as Serial No. not yet known _____
and was amended on _____(if applicable)

Nokia Exhibit 2004, p. 198
Amazon.com v. Nokia
IPR2024-01141

NOTE: Amendments filed after the original papers are deposited with the PTO which contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

(c) ☐ was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____(*if any*).

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information

☒ which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56

(also check the following items, if desired)

☒ and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent, and

☐ In compliance with this duty there is attached an information disclosure statement in accordance with 37 CFR 1.98.

PRIORITY CLAIM (35 U.S.C. § 119)

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT International application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT International application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

(d) ☒ no such applications have been filed.

(e) ☐ such applications have been filed as follows.

NOTE: Where item (c) is entered above and the International Application which designated the U.S. itself claimed priority check item (e), enter the details below and make the priority claim.

Nokia Exhibit 2004, p. 199
Amazon.com v. Nokia
IPR2024-01141

A. PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119

COUNTRY (OR INDICATE IF PCT)	APPLICATION NUMBER	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ **YES** **NO**☐
			☐ **YES** **NO**☐
			☐ **YES** **NO**☐
			☐ **YES** **NO**☐
			☐ **YES** **NO**☐

ALL FOREIGN APPLICATION(S), IF ANY FILED MORE THAN 12 MONTHS (6) MONTHS FOR DESIGN PRIOR TO THIS U.S. APPLICATION

_____

_____

_____

NOTE: If the application filed more than 12 months from the filing date of this application is a PCT filing forming the basis for this application entering the United States as (1) the national stage, or (2) a continuation, divisional, or continuation-in-part, then also complete ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR C-I-P APPLICATION for benefit of the prior U.S. or PCT application(s) under 35 U.S.C. § 120.

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(List name and registration number)*

Clarence A. Green (24,622)
Mark F. Harrington (31,686)
Janik Marcovici (42,841)

(check the following item, if applicable)

☐ Attached as part of this declaration and power of attorney is the authorization of the above named attorney(s) to accept and follow instructions from my representative(s).

Nokia Exhibit 2004, p. 200
Amazon.com v. Nokia
IPR2024-01141

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

NOTE: Carefully indicate the family (or last) name as it should appear on the filing receipt and all other documents.

Full name of sole or first inventor

Marta	____	Karczewicz
(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature Kar
Date 10/10/2001 Country of Citizenship Poland
Residence Irving, Texas, U.S.A.
Post Office Address 1224 Hidden Ridge, #3097 Irving, TX 75038, U.S.A.

Full name of second joint inventor, if any

Antti	____	Hallapuro
(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature _____
Date _____ Country of Citizenship Finland
Residence Tampere, Finland
Post Office Address Insinöörinkatu 60 B 115, FIN-33720 Tampere, Finland

Nokia Exhibit 2004, p. 201
Amazon.com v. Nokia
IPR2024-01141

Full name of third joint inventor, if any

_____ _____ _____
(GIVEN NAME) (MIDDLE INITIAL OR NAME) FAMILY (OR LAST NAME)

Inventor's signature _____
Date _____ Country of Citizenship _____
Residence _____
Post Office Address _____

CHECK PROPER BOX(ES) FOR ANY OF THE FOLLOWING ADDED PAGE(S) WHICH FORM A PART OF THIS DECLARATION

☐ Signature for fourth and subsequent joint inventors. *Number of pages added* _____

...

☐ Signature by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. *Number of pages added* _____

...

☐ Signature for inventor who refuses to sign or cannot be reached by person authorised under 37 CFR 1.47. *Number of pages added* _____

...

☐ Added page for signature by one joint inventor on behalf of deceased inventor(s) where legal representative cannot be appointed in time (37 CFR 1.47).

...

☐ Added pages to combined declaration and power of attorney for divisional, continuation, or continuation-in-part (C-I-P) application. *Number of pages added* _____

...

☐ Authorization of attorney(s) to accept and follow instructions from representative.

...

(If no further pages form a part of this Declaration, then end this Declaration with this page and check the following item:)

☒ This declaration ends with this page.

Nokia Exhibit 2004, p. 202
Amazon.com v. Nokia
IPR2024-01141

SEND CORRESPONDENCE TO

Perman & Green
425 Post Road
Fairfield, CT 06430-6232

DIRECT TELEPHONE CALLS TO:
(Name and telephone number)
Mark F. Harrington

(203) 259-1800

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

NOTE: Carefully indicate the family (or last) name as it should appear on the filing receipt and all other documents.

Full name of sole or first inventor

Marta	_____	Karczewicz
(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature _____
Date _____ Country of Citizenship Poland
Residence Irving, Texas, U.S.A.
Post Office Address 1224 Hidden Ridge, #3097 Irving, TX 75038, U.S.A.

Full name of second joint inventor, if any

Antti	Olli	Hallapuro
(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature Antti Hallapuro
Date 15.10.2001 Country of Citizenship Finland
Residence Tampere, Finland
Post Office Address Insinöörinkatu 60 B 115, FIN-33720 Tampere, Finland

Nokia Exhibit 2004, p. 203
Amazon.com v. Nokia
IPR2024-01141

Full name of third joint inventor, if any

(GIVEN NAME) (MIDDLE INITIAL OR NAME) FAMILY (OR LAST NAME)

Inventor's signature _____
Date _____ Country of Citizenship _____
Residence _____
Post Office Address _____

CHECK PROPER BOX(ES) FOR ANY OF THE FOLLOWING ADDED PAGE(S) WHICH FORM A PART OF THIS DECLARATION

☐ Signature for fourth and subsequent joint inventors. *Number of pages added* ____

• • •

☐ Signature by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. *Number of pages added* _____

• • •

☐ Signature for inventor who refuses to sign or cannot be reached by person authorised under 37 CFR 1.47. *Number of pages added* _____

• • •

☐ Added page for signature by one joint inventor on behalf of deceased inventor(s) where legal representative cannot be appointed in time (37 CFR 1.47).

• • •

☐ Added pages to combined declaration and power of attorney for divisional, continuation, or continuation-in-part (C-I-P) application. *Number of pages added* _____

• • •

☐ Authorization of attorney(s) to accept and follow instructions from representative.

• • •

(If no further pages form a part of this Declaration, then end this Declaration with this page and check the following item:)

☒ This declaration ends with this page.

Nokia Exhibit 2004, p. 204
Amazon.com v. Nokia
IPR2024-01141

#71 Req for Refund
10-24-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(s) Karczewicz et al.

SERIAL NO.: 09/954,608 ART UNIT:2631

FILING DATE: 9/17/2001 EXAMINER:

TITLE: METHOD FOR SUB-PIXEL VALUE INTERPOLATION

ATTORNEY
DOCKET NO.: 442-010567-US (PAR)

Refund Section, Accounting Division, Office of Finance
Box 16
Commissioner of Patents
Washington, D.C. 20231

PETITION FOR REFUND TO DEPOSIT ACCOUNT

Sir:

Pursuant to 37 C.F. R. §1.26, Applicant, requests that the amount of $36.00 be refunded to Deposit Account # 16-1350. Applicant disputes the charge listed below:

7/16/02 - 09/954,608 - 442-010567-US (PAR) - 103 - $36.00

A copy of the Deposit Account statement is attached hereto.

The charge should not have been made. This application originally had 49 claims and 2 were cancelled in a Preliminary Amendment when this application was filed. Therefore, there were only 47 claims filed and 47 were paid for. Thus, there is no basis for the charge.

Accordingly the amount of $36.00 should be refunded to Deposit Account # 16-1350.

Respectfully submitted,

Geza C. Ziegler, Jr.
Reg. No. 44,004
PERMAN & GREEN, LLP
425 Post Road
Fairfield, CT 06824
(203) 259-1800
Customer No.: 2512

8/22/02
Date

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Amazon.com v. Nokia
IPR2024-01141

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope addressed to Refund Section, Accounting Division, Office of Finance, Box 16, Commissioner of Patents, Washington, D.C. 20231.

Date: 8/23/02 Signature: Denise Spaulding
Person Making Deposit

Nokia Exhibit 2004, p. 206
Amazon.com v. Nokia
IPR2024-01141

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
20231

MONTHLY STATEMENT OF DEPOSIT ACCOUNT

To replenish your Deposit Account, detach return top portion with your check. Make payable to Commissioner of Patents & Tra

Please check the accuracy of your charges & let Doris know of any errors

Account No.	161350
Date	7-31-02
Page	1

PERMAN & GREEN
WILLIAM G. HOFFMAN
425 POST ROAD

FAIRFIELD CT 06430

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P.O. Box 70541
Chicago, Ill. 60673

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7	1	02	2	09742935	680-009796US	102	JM	168.00	2218.66
7	1	02	4	09742784	473-010024-U	117	MS	920.00	1298.66
7	1	02	5	09879481	680-009258-U	103	JVG	54.00	1244.66
7	1	02	6	09672465	544-009698-U	103	MS	54.00	1190.66
7	1	02	161	09698772	680-009518-U	141	PW	40.00	1150.66
7	3	02	315	29138137	774D010226-U	561	GZ	30.00	correct 1120.66
7	5	02	4	09074093	200-007950-U	120	correct	-320.00	1440.66
7	5	02	5	09074093	200-007950-U	116	correct	-390.00	1830.66
7	10	02	11	P106144		122	patent	130.00	1700.66
7	10	02	12	P106143		122	copies	130.00	1570.66
7	10	02	13	PCT/US01/27447	486P009HA wrong DS	704	DS	-260.00	1830.66
7	10	02	13	P106142		122		130.00	1700.66
7	10	02	221	09888685	740-010330-U	561	MT	30.00	1670.66
7	16	02	1	09081235	200-007995-U	102	GZ	84.00	wrong 1586.66
7	16	02	22	09954608	442010567US	103	GZ	36.00	wrong 1550.66
7	17	02	1	Debbie 09152555	300-008212-U	103	GZ	36.00	correct 1514.66
7	17	02	2	09152555	300-008212-U	103	GZ	72.00	correct 1442.66
7	19	02	249	PCT/US02/22478	390P009911WO	801	JM	5.00	1437.66
7	19	02	251	PCT/US02/22478	390P009911WO	899	JM	440.00	997.66
7	19	02	252	PCT/US02/22478	390P009911WO	566	JM	15.00	982.66
7	24	02	2	09579618	611-008319-U	102	MS	168.00	814.66
7	24	02	175	09221741		704		-6.00	820.66
7	25	02	1	09249475	297-008492-U	102	DW	252.00	568.66
7	26	02	3	09615167	502-009523-U	115	MS	-110.00	678.66
7	29	02	99	10202642	324-009895-U	103	MS	288.00	390.66
7	29	02	100	10202642	324-009895-U	104	MS	280.00	110.66
7	30	02	20	PCT/US02/19590	819P010360WO	801	GZ	45.00	65.66
7	30	02	22	PCT/US02/19590	819P010360WO	566	GZ	15.00	50.66
7	31	02	142	SERVICE CHARGE	Debbie	608		25.00	25.66

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OPENING BALANCE	TOTAL CHARGES	TOTAL CREDITS	CLOSING BALANCE
2386.66	3447.00	1086.00	25.66

*** O.D. INDICATES OVERDRAWN ***

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OIPE JC61 JAN 13 2003 PATENT & TRADEMARK OFFICE

RECEIVED JAN 16 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(s): KARCZEWICZ et al.

SERIAL NO.: 09/954,608 ART UNIT: 2631

FILING DATE: 9/17/01 EXAMINER:

TITLE: METHOD FOR SUB-PIXEL VALUE INTERPOLATION

ATTORNEY
DOCKET NO.: 442-010567-US(PAR)

RECEIVED JAN 14 2003 Technology Center 2600

Commissioner of Patents
Washington, D.C. 20231

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
(37 C.F.R. §1.97(b)(3))

Sir:

This information disclosure statement is being filed before the mailing of a first Office Action on the merits.

The following information is being disclosed to the Patent and Trademark Office as information that may be material to the examination of the above-identified patent application.

The above-identified patent application has a corresponding PCT International Application No. PCT/FI02/00729 filed on September 11, 2002. Applicants' attorney encloses a copy of a PCT International Search Report issued on the corresponding PCT International

Nokia Exhibit 2004, p. 208
Amazon.com v. Nokia
IPR2024-01141

Application No. PCT/FI02/00729. The Search Report cited United States Patent Nos.: US 5,521,642 A; US 6,219,464 B1; US 5,570,436 A; US 5,568,597 A; US 5,901,248 A; US 6,252,576 B1, US Patent Publication No. 2002/064229 A1, European Patent Publication No. EP 0576290 A2, and United Kingdom Patent Application No. GB 2205707 A.

Copies of the PCT International Search Report and the cited references are enclosed together with PTO-Form 1449.

The filing of this Statement is not to be construed as a representation that a search has been made regarding the claimed invention (37 C.F.R. §1.97(g)) or that no other possible material information exists. In addition, the filing of this Information Disclosure Statement is not to be construed to be an admission that the information cited in the Statement is, or is considered to be, material to patentability (37 C.F.R. §1.97(h)).

The Commissioner is hereby authorized to charge payment for any additional fees associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,

Geza C. Ziegler, Jr. — Date: 1/8/03

Reg. No.: 44,004
PERMAN & GREEN, LLP
425 Post Road, Fairfield, CT 06824
(203) 259-1800
Customer No.: 2512

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Amazon.com v. Nokia
IPR2024-01141

CERTIFICATE OF MAILING

I hereby certify that this Supplemental Information Disclosure Statement, PCT International Search Report, PTO-Form 1449 and cited references are being deposited with the United States Postal Service on the date indicated below as first class mail in an envelope address to the Commissioner of Patents, Washington, D.C. 20231.

Date: 1/8/03 Signature: Deborah J Clark

Person Making Deposit

Nokia Exhibit 2004, p. 210
Amazon.com v. Nokia
IPR2024-01141

INFORMATION DISCLOSURE CITATION FORM FOR PATENT APPLICATION (FORM PTO-1449) (Substitute)	Docket No.: 442-010567-US(PAR) Serial No.: 09/954,608 Applicant(s): KARCZEWICZ et al. Filing Date: 9/17/01 Group: 2631

OIPE JC61 JAN 13 2003 PATENT & TRADEMARK

U.S. PATENTS

Initials	Patent Number	Issue Date	Name	Class	Sub-class	Filing date
	5,521,642	5/28/96	Park	348	409	10/7/93
	6,219,464 B1	4/17/01	Greggain et al.	382	298	8/24/99
	5,570,436	10/29/96	Fukushima et al.	382	300	12/8/94
	5,568,597	10/22/96	Nakayama et al.	395	132	5/20/94
	6,252,576 B1	6/26/01	Nottingham	345	127	8/6/98
	5,901,248	5/4/99	Fandrianto et al.	382	236	8/6/96

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U.S. PATENT PUBLICATIONS

Initials	Publication No.	Pub. Date	Name	Class	Sub-class	Filing Date
	2002/0064229	5/30/02	Nakaya	375	240.17	11/28/01

FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? Yes/No/n/a
	0576290 A2	12/29/93	Europe	Sony Corporation	n/a
	2205707	12/14/88	United Kingdom	Sony Corporation	n/a

OTHER DOCUMENTS (Title, Author, Date, Pages, Etc., if known)

Examiner's Signature:	Date Considered:

Initial if reference was considered, whether or not citation is in conformance with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).

Customer No.: 2512

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Amazon.com v. Nokia
IPR2024-01141

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 576 290 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **93304968.6**

(51) Int. Cl.[5] : **H04N 7/137**

(22) Date of filing : **24.06.93**

(30) Priority : **25.06.92 JP 191576/92**
26.10.92 JP 287179/92

(43) Date of publication of application :
29.12.93 Bulletin 93/52

(84) Designated Contracting States :
DE FR GB IT NL

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Inventor : **Yonemitsu, Jun, c/o Patents Division**
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Inventor : **Suzuki, Teruhiko, c/o Patents Division**
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Shinagawa-ku, Tokyo 141 (JP)

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(54) Picture signal coding and decoding.

(57) Picture signal coding and decoding methods and apparatus are disclosed which eliminate such a situation that, when a coded picture signal of a high definition television system is thinned out to one half in each of the vertical and horizontal directions and displayed on a television receiver of a lower definition system, the displayed picture does not exhibit smooth motion due to the loss of an interlace structure. In an encoder, picture element data are processed by DCT processing to obtain 8 x 8 coefficient data, and the coefficient data are transmitted. In a decoder, of the 8 x 8 coefficient data, only 4 x 4 coefficient data at the left upper corner are sampled out and processed by IDCT processing to obtain original picture element data. In the IDCT processing, those of the 4 x 4 coefficient data which belong to the fourth row are replaced by those of the coefficient data of the eighth row of the 8 x 8 coefficient data.

FIG. 14

d(0,0)	d(0,1)	d(0,2)	d(0,3)
d(1,0)	d(1,1)	d(1,2)	d(1,3)
d(2,0)	d(2,1)	d(2,2)	d(2,3)
d(7,0)	d(7,1)	d(7,2)	d(7,3)

EP 0 576 290 A2

Nokia Exhibit 2004, p. 212
Amazon.com v. Nokia
IPR2024-01141

This invention relates to picture signal coding and decoding methods and picture signal coding and decoding apparatus which may, for example, be used to compress and record a high quality picture signal, such as a signal of high definition television (high definition television (HDTV) signal), onto a recording medium such as an optical disk, a magneto-optical disk or a magnetic tape and subsequently to reproduce, decompress and display the thus recorded signal.

Various picture signal coding apparatus and decoding apparatus are already known, and general constructions of exemplary ones of conventional picture signal coding and decoding apparatus are shown in Figure 21. Referring to Figure 21, a pre-processing circuit 1 of the coding apparatus shown receives an input picture signal such as, for example, a high definition television signal and separates the input picture signal into a brightness signal component (Y) and a colour difference signal component (C). The brightness signal component is converted from an analog signal into a digital signal by an analog to signal (A/D) converter 2 and is written into a frame memory 4 once while the colour difference signal component is converted from an analog signal into a digital signal by another analog to digital (A/D) converter 3 and is written into another frame memory 5 once. A format change circuit 6 changes the formats of the brightness data and the colour difference data stored in the frame memories 4 and 5 to change the data from data in units of a frame to data in units of a block. The data in units of a block obtained by the format changing are supplied to and encoded by an encoder 7, and then supplied as a bit stream to and recorded onto a recording medium 8 in the form of an optical disk, a magneto-optical disk or a magnetic tape.

Subsequently, data reproduced from the recording medium 8 is supplied as a bit stream to and decoded by a decoder 9 of the decoding apparatus. A format change circuit 10 changes the format of the decoded data from the decoder 9 to change the data from data in units of a block to data in units of a frame. The brightness data and the colour difference data outputted from the format change circuit 10 are supplied to and stored into a pair of frame memories 11 and 12, respectively. Then, the brightness data and the colour difference data are read out from the frame memories 11 and 12 and converted from digital data into analog data by a pair of digital to analog (D/A) converters 13 and 14, respectively. They are then supplied as a brightness signal and a colour difference signal to and composed by a post-processing circuit 15 and outputted to another circuit (not shown).

The encoder 7 compresses picture data inputted thereto and supplies the thus compressed picture data to the recording medium 8, and the decoder 9 decompresses such compressed picture data and outputs the thus decompressed picture data to the format change circuit 10. By compressing data in this manner, the amount of data to be stored onto the recording medium 8 can be reduced. Line correlation or inter-frame correlation of a picture signal is utilized for such compression.

Where line correlation is utilized, a picture signal can be compressed, for example, by discrete cosine transform (DCT) or by some other processing.

Where inter-frame correlation is utilized, a picture signal can be coded into a further compressed condition. For example, when frame pictures PC1, PC2 and PC3 are generated at times t1, t2 and t3, respectively, in Figure 22, the difference between picture signals of the frame pictures PC1 and PC2 is calculated to produce a picture PC12, and the difference between picture signals PC2 and PC3 is calculated to produce another picture PC23. Since pictures of frames near to each other in time do not present a very great difference, if the difference between them is calculated, the difference signal has a small value. Therefore, if the difference signal is coded, then the amount of codes needed can be reduced.

However, transmission of only such difference signals does not allow regeneration of the original picture. Therefore, the picture of each frame is formed as one of three types of pictures including an I-picture, a P-picture and a B-picture to compress the picture signal.

In particular, for example, referring to Figure 23(A), a picture signal of 17 frames F1 to F17 is regarded as a group of pictures and as one unit for processing. Then, the picture signal of the first frame F1 is coded as an I-picture; the second frame F2 is processed as a B-picture; and the third frame F3 is processed as a P-picture. Then, the fourth to 17th frames are processed alternately as B-pictures and P-pictures.

For the picture signal of an I-picture, the picture signal for one full frame is coded and transmitted as it is. For the picture signal of a P-picture, basically the difference from the picture signal of an I-picture or a P-picture preceding in time is coded and transmitted as seen from Figure 23(A). Further, for the picture signal of a B-picture, basically the difference from an average value between a frame preceding in time and another frame following in time is calculated as seen from Figure 23(B), and the difference is coded and transmitted.

Figure 24 illustrates the principle of the method of coding a moving picture signal in this manner. As seen from Figure 24, since the first frame F1 is processed as an I-picture, it is coded as it is and transmitted as transmission data F1X into a transmission line (intra-picture coding). On the other hand, since the second frame F2 is processed as a B-picture, the difference of the second frame F2 from an average value between the frame F1 preceding in time and the frame F3 following in time is calculated, and the difference is coded and transmitted as transmission data

Nokia Exhibit 2004, p. 213
Amazon.com v. Nokia
IPR2024-01141

F2X.

More particularly, the processing for a B-picture includes four kinds of processing. The first kind of processing involves coding of data of the original frame F2 as it is and transmission of the coded data as transmission data F2X (SP1) (intra-picture coding) and is processing similar to that for an I-picture. In the second kind of processing, the difference from the frame F3 following in time is calculated, and the difference (SP2) is coded and transmitted (backward predictive coding). In the third kind of processing, the difference (SP3) from the frame F1 preceding in time is coded and transmitted (forward predictive coding). Finally in the fourth kind of processing, the difference (SP4) from an average value between the frame F1 preceding in time and the frame F3 following in time is calculated, and the difference is coded and transmitted as transmission data F2X.

That one of the four methods which minimizes the amount of transmission data is adopted.

It is to be noted that, when difference data is transmitted, a motion vector x1 from the picture (predictive picture) of the frame which makes an object for calculation of the difference (a motion vector between the frames F1 and F2) (in the case of forward prediction) or x2 (a motion vector between the frames F3 and F2) (in the case of backward prediction) or both of such motion vectors x1 and x2 are transmitted together with the difference data.

Further, for the frame F3 of a P-picture, using the frame F1 preceding in time as a predictive picture, a difference signal (SP3) of the frame F3 from the frame F1 and a motion vector x3 are calculated, and they are transmitted as transmission data F3X (forward predictive coding). Or else, data of the original frame F3 is transmitted as it is as transmission data F3X (SP1) (intra-picture coding). That one of the methods which minimizes the amount of transmission data is selected similarly as in the case of a B-picture.

Picture data of a frame which is constituted from V lines, each constituted from H dots, is divided, for example, for each 16 lines into N slices 1 to N, each including M macro blocks as seen from Figure 25. Each macro block includes block data Y[1] to Y[4] each including brightness data for 8 x 8 picture elements (pixels), block data Cb[5] and Cr[6] which are colour difference data corresponding to all of (16 x 16) picture element data of the block data Y[1] to Y[4].

In particular, in a macro block, with regard to a brightness signal, picture element data of 16 x 16 picture elements (Y[1] to Y[4]) which successively appear in the horizontal and vertical scanning directions make a unit, but with regard to the two colour difference signals corresponding to the brightness signal, colour difference data for 16 x 16 picture elements are allocated to each (8 x 8 picture elements) of the blocks Cr[6] and Cb[5] after reduction of the amount of data and time base multiplexing make a unit for processing. Picture data are arranged in each slice such that picture data appear successively in units of a macro block, and in each macro block, picture data appear successively in units of a block (8 x 8 dots) in the order of raster scanning.

It is to be noted that the data Y[1] to Y[4], Cb[5] and Cr[6] are transmitted in this order. In other words, the numbers applied to the symbols represent the order in transmission.

By compressing (thinning out) picture data of a high resolution, for example, picture data for high definition television, to 1/2 in each of the vertical and horizontal directions, picture data of a low resolution can be obtained. If the aspect ratio of the picture data thus obtained is changed from 16:9 to 4:3, then the picture data can be displayed on a television receiver of the NTSC system.

When it is tried to compress a picture of a high resolution to 1/4 (= 1/2 x 1/2) and display it in this manner, a decoder of, for example, such a construction as shown in Figure 26 is employed as the decoder 9 of Figure 21. It is to be noted that data of an input picture to the decoder 9 have been compressed by discrete cosine transform (DCT) by the encoder 7.

Referring to Figure 26, picture data (DCT coefficients) obtained by DCT processing in units of 8 x 8 picture elements by the encoder 7 are supplied to a sampling circuit 21 of the decoder 9, from which, for example, such data for 8 x 8 picture elements as shown in Figure 27 are sampled out. Referring to Figure 27, the 8 x 8 data are constituted from DCT coefficients, and the data correspond to higher frequency components of the picture in the vertical direction towards the bottom of Figure 27 while the data correspond to higher frequency components of the picture in the horizontal direction towards the right end of Figure 27.

Referring back to Figure 26, another sampling circuit 22 at the next stage samples out 4 x 4 DCT coefficients corresponding to lower frequency components shown in Figure 28 from the 8 x 8 DCT coefficients shown in Figure 27. The thus sampled out DCT coefficients are 4 x 4 coefficients at the left upper corner of Figure 27. The 4 x 4 DCT coefficients sampled out by the sampling circuit 22 are inputted to an inverse discrete cosine transform circuit (IDCT) 23, by which they are transformed by inverse discrete cosine transform. Consequently, picture data (4 x 4 picture element data) whose resolutions in the vertical and horizontal directions are reduced to 1/2 are obtained.

In the conventional apparatus described above, when picture data of a lower resolution are to be produced from picture data of a high resolution, only coefficients corresponding to low frequency components are sampled out. Consequently, an interlace structure included in high frequency components is lost. Therefore, the conventional apparatus has the

Nokia Exhibit 2004, p. 214
Amazon.com v. Nokia
IPR2024-01141

disadvantage that the picture of the low resolution does not present smooth motion.

Further, when predictive coding is applied to such a system as described above wherein coded data for 4 x 4 picture elements are sampled out on the decoder side from coded data processed by DCT processing in units of 8 x 8 picture elements on the encoder side to obtain a picture of a lower resolution by decoding, since a predictive picture produced on the decoder side does not coincide completely with another predictive picture produced by a local decoder on the encoder side, if the predictive picture produced on the decoder side is used for decoding, then a mismatch error will be accumulated. Such a mismatch error causes loss of an interlace structure in a picture of a low resolution and causes deterioration of the picture quality of a reproduced picture.

The invention addresses the problem of providing picture signal coding and decoding methods and picture signal coding and decoding apparatus which can regenerate a picture of a low resolution which maintains an interlace structure and exhibits smooth motion.

In order to attain the object described above, according to an aspect of the present invention, there is provided a picture signal decoding method of the type wherein, from coefficient data of a first block formed by orthogonal transformation of picture element data, those of the coefficient data of a second block having a smaller range than the first block are sampled out, and inverse orthogonal transformation is performed for the coefficient data of the second block, wherein the inverse orthogonal transformation is performed for data obtained by replacing at least one of the coefficient data in the second block by a corresponding one or ones of the coefficient data in the first block but outside the second block.

According to another aspect of the present invention, there is provided a picture signal coding apparatus, which comprises orthogonal transformation means for transforming picture element data of a frame formed from two fields and having an interlace structure by orthogonal transformation to form m x n coefficient data, quantization means for quantizing the coefficient data and outputting quantization data obtained by the quantization, and variable length coding means for coding the quantization data into variable length codes and successively transmitting the quantization data in the order of those coefficient data of a first quantization data group which correspond to j x k ones of the m x n coefficient data, j being smaller than m, k being smaller than n, those coefficient data of a second quantization data group which correspond to those of the m x n coefficient data which belong to the m-N+1th to mth rows in the first to kth columns, N being 1, 2, 3, ..., j-1, and those coefficient data of a third quantization data group which correspond to those of the m x n coefficient data which do not belong to any of the first and second quantization data groups.

According to a further aspect of the present invention, there is provided a picture signal decoding apparatus wherein transmission picture element data of a frame formed from two fields and having an interlace structure are transformed by orthogonal transformation to form m x n coefficient data, and then the coefficient data are quantized and coded into variable length codes to decode the transmission data, which comprises variable length decoding means for decoding the transmission data by variable length decoding to obtain decoded data and outputting the decoded data, dequantization means for dequantizing the decoded data to obtain coefficient data and outputting the coefficient data, sampling out means for sampling out, from the coefficient data, j x k coefficient data obtained by replacing successive ones of the coefficient data of the jth row by sums of the successive coefficient data of the jth row and corresponding ones of the coefficient data of the mth row in the corresponding columns, j being smaller than m, k being smaller than n, and inverse orthogonal transformation means for transforming the j x k coefficient data sampled out by the sampling out means by inverse orthogonal transformation.

According to a still further aspect of the present invention, there is provided a picture signal coding method, which comprises the steps of transforming picture element data of a frame formed from two fields and having an interlace structure by orthogonal transformation to form m x n coefficient data, quantizing the coefficient data and outputting quantization data obtained by the quantization, and coding the quantization data into variable length codes in the order of those coefficient data of a first quantization data group which correspond to j x k ones of the m x n coefficient data, j being smaller than m, k being smaller than n, those coefficient data of a second quantization data group which correspond to those of the m x n coefficient data which belong to the m-N+1th to mth rows in the first to kth columns, N being 1, 2, 3, ..., j-1, and those coefficient data of a third quantization data group which correspond to those of the m x n coefficient data which do not belong to any of the first and second quantization data groups.

In the picture signal coding and decoding methods and apparatus, picture data are processed by DCT processing into m x n coefficient data. Of the m x n coefficient data, j x k coefficient data are transmitted. Of the j x k coefficient data, the coefficient data of the jth row are added to the coefficient data of the mth row and then transmitted. Or else, the coefficient data of the jth row are replaced by the coefficient data of the mth row and then transmitted.

Consequently, those of the coefficient data which correspond to a low frequency region are transmitted. Then, predetermined ones of the transmission

Nokia Exhibit 2004, p. 215
Amazon.com v. Nokia
IPR2024-01141

data are processed so that they include coefficient data of a higher frequency region. Accordingly, such a situation that smooth motion of the picture is disturbed by the loss of an interlace structure is eliminated or reduced.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a picture signal coding apparatus;

Figures 2(A) and 2(B) are diagrammatic views illustrating operation of a predictive mode change-over circuit of the picture signal coding apparatus of Figure 1;

Figures 3(A) and 3(B) are diagrammatic views illustrating operation of a DCT mode change-over circuit of the picture signal coding apparatus of Figure 1;

Figure 4 is a table illustrating operation of an address control circuit shown in Figure 7;

Figure 5 is table showing the order in which data illustrated in Figure 4 are scanned by zigzag scanning;

Figure 6 is a block diagram of a picture signal decoding apparatus;

Figure 7 is a block diagram showing a selection circuit of the picture signal decoding apparatus of Figure 6;

Figures 8 to 11 are diagrammatic views illustrating different manners of motion compensation operation of a motion compensation circuit of the picture signal decoding apparatus of Figure 6 in a frame predictive mode (1), a field predictive mode, another frame predictive mode (2) and a further frame predictive mode (3), respectively;

Figure 12 is a table showing data sampled out from a left upper corner area of the table of Figure 4;

Figure 13 is a table illustrating data when data in the fourth row and data in the eighth row in Figure 4 are added to obtain data in the fourth row in Figure 12;

Figure 14 is a table illustrating data when the data in the fourth row in Figure 4 are replaced by the data in the eighth row;

Figure 15 is a table illustrating data when data in the third row and the data in the fourth row in Figure 4 are replaced by data in the seventh row and the data in the eighth row, respectively;

Figure 16 is a table illustrating the order of zigzag scanning when data obtained by the processing illustrated in Figure 15 are to be transmitted;

Figure 17 is a syntax diagram illustrating transmission of data when the zigzag scanning illustrated in Figure 16 is performed;

Figure 18 is a block diagram of another picture signal coding apparatus;

Figure 19 is a block diagram of another picture signal decoding apparatus;

Figure 20 is a block diagram showing a selection circuit of the picture signal coding apparatus of Figure 19;

Figure 21 is a block diagram showing a conventional picture signal coding apparatus and a conventional picture signal decoding apparatus;

Figure 22 is a diagrammatic view illustrating compression of data;

Figures 23(A) and 23(B) are diagrammatic views showing different picture types when picture data are compressed;

Figure 24 is a diagrammatic view illustrating the principle in coding a moving picture signal;

Figure 25 is a diagrammatic view showing a transmission format;

Figure 26 is a block diagram of a decoder of the picture signal decoding apparatus shown in Figure 9;

Figure 27 is a table illustrating data sampled out by a sampling circuit of the decoder shown in Figure 26; and

Figure 28 is a table illustrating data sampled out by another sampling circuit of the decoder shown in Figure 26.

A picture signal coding apparatus and a picture signal decoding apparatus according to one embodiment of the present invention have basically similar constructions to the conventional picture signal coding and decoding apparatus, respectively, described hereinabove with reference to Figure 21, but are different in that the encoder 7 and the decoder 9 have different constructions to those of the conventional picture signal coding and decoding apparatus. Therefore, detailed description will be given below only of the encoder and the decoder of the picture signal coding and decoding apparatus while overlapping description of common components of the picture signal coding and decoding apparatus to those of the conventional picture signal coding and decoding apparatus is omitted herein to avoid redundancy.

Referring first to Figure 1, there is shown a form of encoder. Picture data to be coded are inputted in units of a macro block to a motion vector detection circuit 50. The motion vector detection circuit 50 processes picture data of each frame as an I-picture, a P-picture or a B-picture in accordance with a preset predetermined sequence. As which ones of I-, P- and B-pictures pictures of frames sequentially inputted to the motion vector detection circuit 50 are to be processed is determined in advance. For example, as shown in Figure 23, the pictures of a group of pictures constituted from frames F1 to F17 are processed as I-, B-, P-, B-, P-, ..., B- and P-pictures, respectively.

Picture data of a frame to be processed as an I-picture such as, for example, the frame F1, are transferred from the motion vector detection circuit 50 to and stored in a forward original picture section 51a of

Nokia Exhibit 2004, p. 216
Amazon.com v. Nokia
IPR2024-01141

a frame memory 51; picture data of a frame to be processed as a B-picture such as, for example, the frame F2, are transferred to and stored into a reference original picture section 51b; and picture data of a frame to be processed as a P-picture such as, for example, the frame F3, are transferred to and stored into a backward original picture section 51c.

Further, when a picture of a frame to be processed as a B-picture (frame F4) or a P-picture (frame F5) is inputted at a next timing, the picture data of the first P-picture (frame F3) stored in the backward original picture section 51c until then are transferred to the forward original picture section 51a while the picture data of the next B-picture (frame F4) are stored (overwritten) into the reference original picture section 51b and the picture data of the next P-picture (frame F5) are stored (overwritten) into the backward original picture section 51c. Such a sequence of operations as described above is repeated successively.

A signal of a picture stored in the frame memory 51 is read out from the frame memory 51 and then processed by frame predictive mode processing or field predictive mode processing by a predictive mode change-over circuit 52. Further, under the control of a predictive discrimination circuit 54, calculation for intra-picture prediction, forward prediction, backward prediction or bidirectional prediction is performed by a calculation section or prediction circuit 53. Which one of the types of processing should be performed is determined based on a predictive error signal, that is, a difference between a reference original picture for an object of processing and a predictive picture for the reference original picture. Therefore, the motion vector detection circuit 50 generates an absolute value sum or a square sum of predictive error signals which is used for such discrimination.

Here, a frame predictive mode and a field predictive mode of the predictive mode change-over circuit 52 will be described.

When the frame predictive mode is set, the predictive mode change-over circuit 52 outputs four brightness blocks Y[1] to Y[4] supplied from the motion vector detection circuit 50 as they are to the calculation section 53 at the succeeding stage. In particular, in this instance, data of lines of odd-numbered fields and data of lines of even-numbered lines are present in a mixed condition in each brightness block. In the frame predictive mode, prediction is performed in units of four brightness blocks (macro blocks), and one motion vector corresponds to four brightness blocks.

On the other hand, in the field predictive mode, the predictive mode change-over circuit 52 processes a signal, which is inputted thereto from the motion vector detection circuit 50 and has such a construction as illustrated in Figure 2(A), so that, for example, the brightness blocks Y[1] and Y[2] of the four brightness blocks are constituted from dots of lines of odd-numbered fields while the other two brightness blocks Y[3] and Y[4] are constituted from data of lines of even-numbered fields as seen from Figure 2(B). The predictive mode change-over circuit 52 outputs the resulted data to the calculation section 53. In this instance, one motion vector (a motion vector of the odd-numbered fields) corresponds to the two brightness blocks Y[1] and Y[2], and another one motion vector (a motion vector of the even-numbered fields) corresponds to the other two brightness blocks Y[3] and Y[4].

The motion vector detection circuit 50 outputs an absolute value sum of predictive errors in the frame predictive mode and another absolute value sum of predictive errors in the field predictive mode to the predictive mode change-over circuit 52. The predictive mode change-over circuit 52 compares the absolute value sums of predictive errors in the frame predictive mode and the field predictive mode, performs processing of the absolute value sums corresponding to that one of the predictive modes in which the absolute value sum presents a lower value, and outputs the resulted data to the calculation section 53.

Alternatively, such processing as described above may be performed by the motion vector detection circuit 50. In particular, the motion vector detection circuit 50 can output a signal corresponding to a determined mode to the predictive mode change-over circuit 52, and the predictive mode change-over circuit 52 outputs the signal as it is to the calculation section 53 at the succeeding stage.

It is to be noted that, in the frame predictive mode, a colour difference signal is supplied to the calculation section 53 in a condition wherein data of lines of odd-numbered fields and data of lines of even-numbered fields are present in a mixed condition as seen from Figure 2(A). On the other hand, in the field predictive mode, upper halves (4 lines) of the colour difference blocks Cb[5] and Cr[6] are colour difference signals of odd-numbered fields corresponding to the brightness blocks Y[1] and Y[2] while the lower halves (four lines) are colour difference signals of even-numbered fields corresponding to the brightness blocks Y[3] and Y[4] as seen from Figure 2(B).

The motion vector detection circuit 50 produces an absolute value sum of predictive errors, which is to be used to determine which one of intra-picture prediction, forward prediction, backward prediction and bidirectional prediction should be performed by the predictive discrimination circuit 54, in the following manner.

In particular, the motion vector detection circuit 50 calculates, as an absolute value sum of predictive errors for intra-picture prediction, a difference between an absolute value $|\Sigma Aij|$ of a sum ΣAij of signals Aij of a macro block of a reference original picture and a sum $\Sigma|Aij|$ of absolute values $|Aij|$ of the signals Aij of the macro block. Furthermore, the motion vector detection

Nokia Exhibit 2004, p. 217
Amazon.com v. Nokia
IPR2024-01141

circuit 50 calculates, as an absolute value sum of predictive errors for forward prediction, a sum $\Sigma|Aij - Bij|$ of absolute values $|Aij - Bij|$ of differences Aij - Bij between signals Aij of a macro block of a reference original picture and signals Bij of another macro block of a predictive picture. Further, the motion vector detection circuit 50 calculates absolute value sums for backward prediction and bidirectional prediction in a similar manner as for forward prediction (changing the predictive picture to another predictive picture different from that in forward prediction).

The absolute value sums thus calculated are supplied to the predictive discrimination circuit 54. The predictive discrimination circuit 54 selects, as an absolute value sum of predictive errors for inter-frame prediction, that one of the absolute value sums of predictive errors for inter-frame predictions (forward prediction, backward prediction and bidirectional prediction) which has a smallest value. Further, the predictive discrimination circuit 54 compares the absolute value sum of predictive errors for the inter prediction and the absolute value sum of predictive errors for intra-picture prediction, selects that one of the absolute value sums which has a lower value, and sets a mode corresponding to the selected absolute value sum as a predictive mode. In particular, if the absolute value sum of predictive errors for intra-picture prediction is lower, the intra-picture predictive mode is set. Conversely, if the absolute value sum of predictive errors for inter-frame prediction is lower, a mode corresponding to that one of the absolute value sums in the forward predictive mode, the backward predictive mode and the bidirectional predictive mode which has a lowest value is set.

In this manner, the motion vector detection circuit 50 supplies a signal for a macro block of a reference original picture corresponding to one of the frame predictive mode and the field predictive mode selected by the predictive mode change-over circuit 52 to the calculation section 53 by way of the predictive mode change-over circuit 52, and detects a motion vector between a predictive picture corresponding to one of the four predictive modes selected by the predictive discrimination circuit 54 and a reference original picture and outputs the detected motion vector to a variable length coding circuit 58 and a motion compensation circuit 64. As described above, the motion vector is selected so that the corresponding absolute value sum of predictive errors may be in the minimum.

The predictive discrimination circuit 54 sets an intra-frame (intra-picture) predictive mode (in which no motion compensation is performed) as the predictive mode and changes over a switch 53d of the calculation section 53 to a contact a side when the motion vector detection circuit 50 is reading out picture data of an I-picture from the forward original picture section 51a. Consequently, the picture data of an I-picture are inputted to a DCT mode change-over circuit 55.

The DCT mode change-over circuit 55 puts data of four brightness blocks into a condition in which lines of odd-numbered fields and lines of even-numbered fields are present in a mixed condition (frame DCT mode) or another condition in which lines of odd-numbered fields and lines of even-numbered fields are present in a separate condition (field DCT mode) as shown in Figure 3(A) or 3(B), and outputs the resulted data to a DCT circuit 56.

In particular, the DCT mode change-over circuit 55 compares a coding efficiency when data of odd-numbered fields and even-numbered fields are present in a mixed condition and are processed by DCT processing and another coding efficiency when such data are present separately and are processed by DCT processing, and selects a mode in which the coding efficiency is higher.

For example, the DCT mode change-over circuit 55 changes input signals to signals of a construction wherein lines of odd-numbered fields and even-numbered fields are present in a mixed condition as seen in Figure 3(A), calculates differences between the signals of lines of the odd-numbered fields and the signals of lines of the even-numbered fields which are adjacent to each other in the vertical direction, and calculates a sum of absolute values (or a square sum) of the differences. Or, the DCT mode change-over circuit 55 changes input signals to signals of another construction wherein lines of odd-numbered fields and lines of even-numbered fields are separate from each other as shown in Figure 3(B), calculates differences between the signals of lines of the odd-numbered fields which are adjacent to each other in the vertical direction and the signals of lines of the even-numbered fields which are adjacent to each other in the vertical direction, and calculates two sums of absolute values (or square sums) of the differences. Further, the DCT mode change-over circuit 55 compares the two sums (absolute value sums) with each other and sets a DCT mode corresponding to that of the sums which has a lower value. In particular, if the former is lower, then the frame DCT mode is set, but if the latter is lower, then the field DCT mode is set.

When the predictive mode change-over circuit 52 sets the frame predictive mode (Figure 2(A)) and the DCT mode change-over circuit 55 sets the frame DCT mode (Figure 3(A)) and when the predictive mode change-over circuit 52 sets the field predictive mode (Figure 2(B)) and the DCT mode change-over circuit 55 sets the field DCT mode (Figure 3(B)), the DCT mode change-over circuit 55 need not change the array of data.

In contrast, when the predictive mode change-over circuit 52 sets the field predictive mode (Figure 2(B)) and the DCT mode change-over circuit 55 sets the frame DCT mode (Figure 3(A)) and when the pre-

Nokia Exhibit 2004, p. 218
Amazon.com v. Nokia
IPR2024-01141

dictive mode change-over circuit 52 sets the frame predictive mode (Figure 2(A)) and the DCT mode change-over circuit 55 sets the field DCT mode (Figure 3(B)), the DCT mode change-over circuit 55 performs re-arrangement of data. In order to allow the processing to be realized, a predictive flag is supplied from the predictive mode change-over circuit 52 to the DCT mode change-over circuit 55.

The DCT mode change-over circuit 55 outputs data of a construction corresponding to a selected DCT mode to the DCT circuit 56 and outputs a DCT flag indicative of the selected DCT mode to the variable length coding circuit 58 and a conversion circuit 65.

As apparent from comparison between the predictive mode (Figures 2(A) and 2(B)) of the predictive mode change-over circuit 52 and the DCT mode (Figures 3(A) and 3(B)) of the DCT mode change-over circuit 55, data structures of a brightness block in the different modes are substantially the same as each other.

When the predictive mode change-over circuit 52 selects the frame predictive mode (in which odd-numbered lines and even-numbered lines are present in a mixed condition), the possibility that the DCT mode change-over circuit 55 may select the frame DCT mode (in which odd-numbered lines and even-numbered lines are present in a mixed condition) is high, but when the predictive mode change-over circuit 52 selects the field predictive mode (in which data of odd-numbered fields and data of even-numbered fields are separate from each other), the possibility that the DCT mode change-over circuit 55 may select the field DCT mode (in which data of odd-numbered fields and data of even-number fields are separate from each other) is high.

However, this is not always the case, and the predictive mode change-over circuit 52 decides a mode so that the absolute value sum of predictive errors may be minimized while the DCT mode change-over circuit 55 decides a mode so that a highest coding efficiency may be achieved.

Picture data of an I-picture outputted from the DCT mode change-over circuit 55 are inputted to the DCT circuit 56, processed by DCT (discrete cosine transform) processing and converted into DCT coefficients. The DCT coefficients are inputted to a quantization circuit 57, by which they are quantized with a quantization step corresponding to the amount of data (buffer accumulated amount) accumulated in a transmission buffer memory 59. The thus quantized data are inputted to the variable length coding circuit 58.

The variable length coding circuit 58 converts picture data (in the present case, data of an I-picture) supplied thereto from the quantization circuit 57 into a variable length code such as, for example, a Huffman code in accordance with a quantization step (scale) supplied thereto from the quantization circuit 57, and outputs the thus obtained variable length code to a transmission buffer memory 59.

The quantized DCT coefficients are outputted, from the characteristic of the DCT, such that coefficients of a low frequency region (high in power) are outputted to a left upper corner are (for example, those of 8 x 8 DCT coefficients shown at a left upper corner in Figure 4). Generally, a coefficient is coded into a variable length code in a combination of a run length of Os (zero run) and a coefficient (level). The system by which a coefficient is coded in a combination of a zero run and a level is called run length coding. When a code is coded by run length coding, a long zero run can be produced by performing transmission of coefficients in such an order called zigzag scanning as illustrated in Figure 5 (in Figure 5, the numerals indicate numbers in the order of transmission), and consequently, data can be compressed.

The variable length coding circuit 58 receives a quantization step (scale) from the quantization circuit 57, a predictive mode (set from among the intra-picture predictive mode, the forward predictive mode, the rearward predictive mode and the bidirectional predictive mode) (block type) from the predictive discrimination circuit 54, a motion vector from the motion vector detection circuit 50, a predictive flag (a flag indicating which one of the frame predictive mode and the field predictive mode is set) from the predictive mode change-over circuit 52 and a DCT flag (a flag indicating which one of the frame DCT mode or the field DCT mode is set) outputted from the DCT mode change-over circuit 55. Also the data thus received are converted into variable length codes together with zigzag scanned quantization data.

The transmission buffer memory 59 stores data transmitted thereto once and then outputs the data as a bit stream at a predetermined timing. Further, the transmission buffer memory 59 feeds back a quantized control signal in units of a macro block to the quantization circuit 57 in response to an amount of data remaining therein to control the quantization scale. Consequently, the transmission buffer memory 59 adjusts the amount of data generated as a bit stream to keep the data in the inside thereof to an appropriate remaining amount (at which no overflow or underflow takes place).

For example, if the remaining amount of data of the transmission buffer memory 59 is increased to an allowable upper limit value, then the transmission buffer memory 59 increases the quantization scale of the quantization circuit 57 by means of a quantization control signal to reduce the amount of quantization data. Or on the contrary if the amount of remaining data of the transmission buffer memory 59 decreases to an allowable lower limit, the transmission buffer 59 decreases the quantization scale of the quantization circuit 57 by way of a quantization control signal to in-

Nokia Exhibit 2004, p. 219
Amazon.com v. Nokia
IPR2024-01141

crease the amount of quantization data.

A bit stream outputted from the transmission buffer memory 59 is multiplexed with a coded audio signal, a code synchronizing signal and so forth, and further, a code for error correction is added to the multiplexed signal, whereafter predetermined modulation is applied to the resulted signal. Then, the modulated signal is recorded as convex and concave bits onto a master disk by laser light. A stamper is formed making use of the master disk, and a large amount of copy disks (for example, optical disks) are formed from the stamper.

Meanwhile, data of an I-picture outputted from the quantization circuit 57 are inputted to a dequantization circuit 60, in which they are dequantized to a representative value in accordance with a quantization step supplied thereto from the quantization circuit 57. The output of the dequantization circuit 60 is inputted to and processed by inverse DCT processing by an IDCT (inverse DCT) circuit 61, and then inputted to a conversion circuit 65. The conversion circuit 65 returns the data inputted thereto from the IDCT circuit 61 into the condition of the frame predictive mode (Figure 2(A)) or into the condition of the field predictive mode (Figure 2(B)) in accordance with a DCT flag supplied thereto from the DCT mode change-over circuit 55 and a predictive flag outputted from the predictive mode change-over circuit 52 so that they may coincide with the condition of predictive picture data outputted from the motion compensation circuit 64, and outputs the resulted data to an arithmetic unit 62. The data outputted from the arithmetic unit 62 are inputted to a conversion circuit 66, by which they are returned into those of the condition in the frame predictive mode (the condition shown in Figure 2(A)) in response to a predictive flag. The resulted data is supplied to and stored into a forward predictive picture section 63a of the frame memory 63.

It is to be noted that the frame memory 63 can be substituted by a field memory, and in this instance, since data are stored individually for each field, data outputted from the arithmetic unit 62 are returned into those of the condition in the field predictive mode (the condition of Figure 2(B)) by the conversion circuit 66.

The motion vector detection circuit 50 first processes, when it is to process picture data of frames inputted sequentially thereto as, for example, I-, B-, P-, B-, P-, B-, ... pictures, the picture data of a frame inputted first as an I-picture and then processes, before another picture inputted subsequently is to be processed as a B-picture, picture data of a further picture inputted subsequently to the second picture as a P-picture. This is because a B-picture involves backward prediction and accordingly cannot be decoded unless a P-picture as a backward predictive picture is prepared beforehand.

Therefore, the motion vector detection circuit 50 starts, after processing of the I-picture, processing of picture data of a P-picture stored in the backward original picture section 51c. Then, similarly as in the case described above, an absolute value sum of interframe differences (predictive errors) in units of a macro block is supplied from the motion vector detection circuit 50 to the predictive mode change-over circuit 52 and the predictive discrimination circuit 54. The predictive mode change-over circuit 52 and the predictive discrimination circuit 54 set, in accordance with the absolute valve sum of predictive errors of the macro block of the P-picture, the frame or field predictive mode or the intra-picture predictive, forward predictive, backward predictive or bidirectional predictive mode (block type), respectively.

The calculation section 53 changes over the switch 53d to the contact a side as described above when the intra-frame predictive mode is set. Accordingly, the data are transmitted to the transmission line by way of the DCT mode change-over circuit 55, the DCT circuit 56, the quantization circuit 57, the variable length coding circuit 58 and the transmission buffer memory 59 similarly as the data of the I-picture. Further, the data are supplied to and stored into the backward predictive picture section 63b of the frame memory 63 by way of the dequantization circuit 60, the IDCT circuit 61, the conversion circuit 65, the arithmetic unit 62 and the conversion circuit 66.

In the forward predictive mode, the switch 53d is changed over to the contact b and picture data stored in the forward predictive picture section 63a of the frame memory 63 (in the present case, data of the I-picture) are read out and undergo motion compensation by the motion compensation circuit 64 in accordance with a motion vector outputted from the motion vector detection circuit 50. In particular, when setting of the forward predictive mode is instructed by the predictive discrimination circuit 54, the motion compensation circuit 64 displaces the read address of the forward predictive picture section 63a by an amount corresponding to the motion vector from a position corresponding to the position of the macro block being outputted at present from the motion vector detection circuit 50, reads out data from the displaced address and produces predictive picture data. Further, in this instance, the motion compensation circuit 64 arrays the predictive picture data into those of the condition shown in Figure 2(A) or 2(B) in response to a frame/field predictive flag supplied thereto from the predictive mode change-over circuit 52.

The predictive picture data outputted from the motion compensation circuit 64 are supplied to an arithmetic unit 53a. The arithmetic unit 53a subtracts the predictive picture data supplied thereto from the motion compensation circuit 64 and corresponding to a macro block of a reference original picture from data of the macro block supplied thereto from the predictive mode change-over circuit 52, and outputs the difference (predictive error) between them. The differ-

Nokia Exhibit 2004, p. 220
Amazon.com v. Nokia
IPR2024-01141

ence data is transmitted into the transmission line by way of the DCT mode change-over circuit 55, the DCT circuit 56, the quantization circuit 57, the variable length coding circuit 58 and the transmission buffer memory 59. Further, the difference data is locally decoded by the dequantization circuit 60, the IDCT circuit 61 and the conversion circuit 65 and then inputted to the arithmetic unit 62.

Data same as the predictive picture data supplied to the arithmetic unit 53a is also supplied to the arithmetic unit 62. The arithmetic unit 62 adds the predictive picture data outputted from the motion compensation circuit 62 to the difference data outputted from the conversion circuit 65. Consequently, picture data of an original (decoded) P-picture are obtained. However, since the data have undergone arraying processing as shown in Figure 2(A) or 2(B) by the predictive mode change-over circuit 52, processing for returning the array into that of the condition in the frame predictive mode (the condition shown in Figure 2(A)) (where the frame memory 63 is constituted otherwise from a field memory, the condition in the field predictive mode (the condition shown in Figure 2(B)) is performed in response to a predictive flag by the conversion circuit 66. The picture data of the P-picture are supplied to and stored into the backward predictive picture section 63b of the frame memory 63.

The motion vector detection circuit 50 executes processing of a B-picture after the data of the I-picture and the P-picture have been stored into the forward predictive picture section 63a and the backward predictive picture section 63b, respectively. In response to the magnitude of the absolute value sum of inter-frame differences in units of a macro block, the predictive mode change-over circuit 52 sets the frame or field predictive mode and the predictive discrimination circuit 54 sets the intra-frame/forward/backward/bidirectional predictive mode (block type) to one of the intra-frame predictive mode, the forward predictive mode, the backward predictive mode and the bidirectional predictive mode.

As described above, when in the intra-frame predictive mode or the forward predictive mode, the switch 53d is changed over to the contact a or b. In this instance, processing similar to that for the P-picture is performed, and resulted data are transmitted.

In contrast, when the backward predictive mode or the bidirectional predictive mode is set, the switch 53d is changed over to the contact c or d.

When in the forward predictive mode in which the switch 53d is changed over to the contact c, data of a picture stored in the backward predictive picture section 63b (in the present case, the picture data of a P-picture) are read out and undergo motion compensation by the motion compensation circuit 64 in accordance with a motion vector outputted from the motion vector detection circuit 50. In particular, when setting of the backward predictive mode is instructed from the predictive discrimination circuit 54, the motion compensation circuit 64 displaces the read address of the backward predictive picture section 63b by an amount corresponding to the motion vector from a position corresponding to the position of a macro block being outputted at preset from the motion vector detection circuit 50, reads out data from the thus displaced address, and produces predictive picture data. Further, the motion compensation circuit 64 arrays the data in such a manner as illustrated in Figure 2(A) or 2(B) in response to a predictive flag outputted from the predictive mode change-over circuit 52.

The predictive picture data outputted from the motion compensation circuit 64 are supplied to the arithmetic unit 53b. The arithmetic unit 53b subtracts the predictive picture data supplied thereto from the motion compensation circuit 64 from data of a macro block of a reference original picture supplied thereto from the predictive mode change-over circuit 52, and outputs the differences between them. The difference data are transmitted into the transmission line by way of the DCT mode change-over circuit 55, the DCT circuit 56, the quantization circuit 57, the variable length coding circuit 58 and the transmission buffer memory 59.

When the bidirectional predictive mode wherein the switch 53d is changed over to the contact d is set, data of a picture stored in the forward predictive picture section 63a (in the present case, the picture of an I-picture) and data of another picture stored in the backward predictive picture section 63b (in the present case, the picture of a P-picture) are read out and undergo motion compensation by the motion compensation circuit 64 in response to a motion vector outputted from the motion vector detection circuit 50. In particular, when setting of the bidirectional predictive mode is instructed from the predictive discrimination circuit 54, the motion compensation circuit 50 displaces the read addresses of the forward predictive picture section 63a and the backward predictive picture section 63b by amounts corresponding to motion vectors for a forward predictive picture and a backward predictive picture from positions corresponding to the positions of a macro block being outputted at present from the motion vector detection circuit 50, reads out data from the thus displaced addresses, and produces predictive picture data. Further, the data are arranged in response to a predictive flag from the predictive mode change-over circuit 52.

The predictive picture data outputted from the motion compensation circuit 64 are supplied to an arithmetic unit 53c. The arithmetic unit 53c subtracts an average value of the predictive picture data supplied thereto from the motion compensation circuit 64 from data of a macro block of a reference original picture supplied thereto from the motion vector detection circuit 50, and outputs the difference between them.

Nokia Exhibit 2004, p. 221
Amazon.com v. Nokia
IPR2024-01141

The difference data is transmitted into the transmission line by way of the DCT mode change-over circuit 55, the DCT circuit 56, the quantization circuit 57, the variable length coding circuit 58 and the transmission buffer memory 59.

Any picture data of a P-picture is not stored into the frame memory 63 because it is not used as a predictive picture for any other picture.

It is to be noted that the forward predictive picture section 63a and the backward predictive picture section 63b of the frame memory 63 perform bank changing over when necessary, and a predetermined reference original picture stored in one or the other of them can be switchably outputted as a forward predictive picture or a backward predictive picture.

While the foregoing description has been given mainly of brightness blocks, also colour difference blocks are processed and transmitted in units of a macro block shown in Figures 2(A) or 2(B) and 3(A) or 3(B). It is to be noted that a motion vector used when a colour difference block is processed is obtained by reducing a motion vector of a corresponding brightness block to one half in each of the vertical and horizontal directions.

Referring now to Figure 6, there is shown a decoder. An input bit stream is inputted to the decoder from an optical disk (recording medium 8 shown in Figure 21) or a like recording medium. The input bit stream is inputted by way of a reception buffer memory 70 to and decoded by a variable length decoding circuit (IVLC) 71. As a result of the decoding, quantized data (DCT coefficients), motion vectors, predictive modes, predictive flags, DCT flags, quantization scales and so forth are obtained. Data (DCT coefficients) outputted from the variable length decoding circuit 71 are inputted to and dequantized to representative values by a dequantization circuit 72. The dequantization step is controlled in response to a quantization scale outputted from the variable length decoding circuit 71.

Quantized regenerated values (DCT coefficients) as an output of the dequantization circuit 72 are outputted as 8 x 8 values for each block. An IDCT circuit 73 performs IDCT processing of the 8 x 8 coefficients. Consequently, a block of 8 x 8 picture element data is obtained. The output of the IDCT circuit 73 is inputted to a conversion circuit 77, in which it is returned in response to a DCT flag and a predictive flag supplied thereto from the variable length decoding circuit 71 into the array condition in which it coincides with the array of data outputted from the motion compensation circuit 74. The output of the conversion circuit 77 is supplied to an arithmetic unit 74.

When picture data supplied to the arithmetic unit 74 are data of an I-picture, the data are outputted from the arithmetic unit 74 and returned in response to predictive flag supplied thereto from the variable length decoding circuit 71 by a conversion circuit 78 into those of the condition in the frame predictive mode shown in Figure 2(A) (when a frame memory 75 is constituted from a field memory, the condition of the field predictive mode (the condition shown in Figure 2(B)), whereafter they are supplied to and stored into a forward predictive picture section 75a of the frame memory 75 in order to allow production of predictive picture data for picture data (data of a P-picture or a B-picture) to be inputted to the arithmetic unit 74 later. Further, the data are outputted as they are to, for example, the format conversion circuit 10 (Figure 21) at the succeeding stage.

When picture data supplied to the arithmetic unit 74 are data of a P-picture produced using picture data of a preceding frame as predictive picture data and the forward predictive mode is set, the picture data of the preceding frame (data of the I-picture) stored in the forward predictive picture section 75a of the frame memory 75 are read out and undergo motion compensation corresponding to a motion vector outputted from the variable length decoding circuit 71 and processing corresponding to the predictive mode (block type) by the motion compensation circuit 76. Further, data are arrayed as shown in Figure 2(A) or 2(B) in response to the predictive flag. Then, the arithmetic unit 74 adds picture data (difference data) supplied thereto from the conversion circuit 77 to the data from the motion compensation circuit 76 and outputs the resulted data therefrom. The data obtained by the addition, that is, the decoded data of the P-picture, are supplied to and stored into the backward predictive picture section 75b of the frame memory 75 in order to allow production of predictive picture data for picture data (data of a B-picture or a P-picture) to be inputted to the arithmetic unit 74 later.

Even when the data are data of a P-picture, the data in the intra-picture predictive mode are not processed by particular processing by the arithmetic unit 74 and are stored as they are into the backward predictive picture section 75b similarly to the data of the I-picture.

Since the P-picture is a picture to be displayed subsequently to a succeeding B-picture, it is not outputted at this point of time to the format conversion circuit 10 at the succeeding stage as yet (as described above, the P-picture inputted succeedingly to the B-picture is processed and transmitted prior to the B-picture).

When the picture data supplied from the conversion circuit 77 are data of a B-picture, the picture data of the I-picture stored in the forward predictive picture section 75a of the frame memory 75 (in the case of the forward predictive mode), the picture data of the P-picture stored in the backward predictive picture section 75b (in the case of the backward predictive mode) or the picture data of both of the I-picture and the P-picture are read out in response to a predictive mode supplied from the variable length decoding cir-

Nokia Exhibit 2004, p. 222
Amazon.com v. Nokia
IPR2024-01141

cuit 71, and motion compensation is performed for the thus read out picture data in accordance with a motion vector outputted from the variable length decoding circuit 71 by the motion compensation circuit 76. The picture data after the motion compensation are then processed by arraying processing of data in response to a predictive flag to produce a predictive picture. However, when no motion compensation is required (in the case of the intra-picture predictive mode), no predictive picture is produced.

The data obtained by motion compensation by the motion compensation circuit 76 in this manner are added to the output of the conversion circuit 77 by the arithmetic unit 74. The addition output is returned into the signals of the condition in the frame predictive mode in response to the predictive flag by another conversion circuit 78 and then outputted to the format conversion circuit 10.

However, since the addition output is data of a B-picture and is not utilized for production of a predictive picture for any other picture at all, it is not stored into the frame memory 75.

After the picture of a B-picture is outputted, picture data of the P-picture stored in the backward predictive picture section 75b are read out and outputted by way of the motion compensation circuit 76, the arithmetic unit 74 and the conversion circuit 78. In this instance, motion compensation, arraying processing or the like is not performed.

Further, while the foregoing description has been given of processing of a brightness signal, processing of a colour difference signal is performed in a similar manner. In this instance, however, a motion vector used is obtained by reducing a motion vector for a brightness signal to one half in each of the vertical and horizontal directions.

If the picture regenerated in such a manner as described above is converted from digital to analog values, then a decoded picture of a high definition television system of a high resolution can be obtained.

The decoder described above includes, in addition to the construction for obtaining a decoded picture of a high definition television system described above, another construction for obtaining a decoded picture of a resolution equal to one fourth the resolution of the standard television system. The second construction includes a dequantization circuit 81, which dequantizes data outputted from the variable length decoding circuit 71 to a representative value in accordance with a quantization scale also outputted from the variable length decoding circuit 71 and outputs the resulted data to a selection circuit 82. It is to be noted that the dequantization circuit 81 is provided in order to obtain a standard television video output together with a high definition television video output, and when it is required to output only one of the two outputs, the dequantization circuit 81 may be omitted. In this instance, the output of the dequantization circuit 72 is supplied to the selection circuit 82.

Referring now to Figure 7, the selection circuit 82 may be constituted from a calculation circuit 90, an address control circuit 91 and a memory 92. Data supplied from the dequantization circuit 81 (or 72) are written into the memory 92. Then, the data are read out from the memory 92 and outputted to an IDCT circuit 83. Writing into and reading out from the memory 92 is controlled by an address control circuit 91. While details of the writing and reading control will be hereinafter described, the selection circuit 82 selects predetermined 4 x 4 DCT coefficients from such 8 x 8 DCT coefficients as shown in Figure 4.

Referring back to Figure 6, the IDCT circuit 83 processes the inputted 4 x 4 coefficients by IDCT processing and outputs the resulted data to a conversion circuit 88. The conversion circuit 88 returns the array of the data, in response to a DCT flag and a predictive flag outputted from the variable length decoding circuit 71, into that of a condition wherein it coincides with the array of predictive picture data outputted from a motion compensation circuit 86. The conversion circuit 88 outputs the data after such array change to an arithmetic unit 84. The motion compensation circuit 86 performs motion compensation of picture data stored in a frame memory 85 in response to a motion vector and a predictive mode supplied thereto from the variable length decoding circuit 71, and then performs such array conversion of the picture data as illustrated in Figure 2(A) or 2(B) in response to a predictive code to produce predictive picture data.

The data outputted from the motion compensation circuit 86 are added to the output of the conversion circuit 88. The array condition of the resulted data is converted, in response to the predictive flag, into the condition in the frame predictive mode (the condition of the field predictive mode when the frame memory 85 is constituted from a field memory), and then the data are outputted as standard television picture data. It is to be noted that, since motion at the motion compensation circuit 86 is equal to about one half the motion at the motion compensation circuit 76, a motion vector outputted from the variable length decoding circuit 71 is converted to one half by scale conversion by a scaling circuit 87 and then supplied to the motion compensation circuit 86.

In particular, when the predictive mode in the encoder of Figure 1 is determined as the frame predictive mode by the predictive discrimination circuit 54 of the encoder, also the predictive mode in the decoder is set to the frame predictive mode. On the other hand, when the predictive mode in the encoder is determined as the field predictive mode, also the predictive mode in the decoder is set to the field predictive mode. In short, when the the motion compensation circuit 64 of the encoder forms a predictive picture in the frame p[illegible] motion com-

Nokia Exhibit 2004, p. 223
Amazon.com v. Nokia
IPR2024-01141

pensation circuit 86 of the decoder cooperates with the scaling circuit 87 to form a predictive picture in the frame predictive mode similarly. On the other hand, when the motion compensation circuit 64 forms a predictive picture in the field predictive mode, the motion compensation circuit 86 cooperates with the scaling circuit 87 to form a predictive picture in the field predictive mode similarly.

Subsequently, the relationship between motion compensation and the frame or field predictive mode will be described. In the case of the frame predictive mode (frame predictive mode (1)), in motion compensation of the encoder performed by the motion compensation circuit 64 (similar with motion compensation of the motion compensation circuit 76 of a high definition television decoder block), a single predictive frame is formed as a predictive picture from a first field (odd-numbered field) including such picture elements a, c, e, g, ... as shown in (a) of Figure 8 and a second field (even-numbered field) including such picture elements b, d, f, ... as shown in (a) of Figure 8. Meanwhile, in motion compensation for a standard television decoder block performed by the motion compensation circuit 86 of the decoder, a single predictive frame is formed as a predictive picture from a first field including such picture elements a', c', ... as shown in (b) of Figure 8 and a second field including such picture elements z', b', d', ... (the distance between z' and b' and the distance between b' and d' are equal to each other) as shown in (b) of Figure 8.

In order to convert data of a high resolution (high definition television) into data of a 1/4 resolution, picture elements should be thinned out to one half in both of the horizontal direction and the vertical direction. Now, considering only thinning out in the vertical direction, since a frame has an interlace structure based on two fields, if lines are thinned out to one half in the vertical direction, then data of one field (in the case shown in Figure 8, the first field) after all correspond to data of one frame of a 1/4 resolution (2 fields). In the case shown, the picture elements a, e, ... among the picture elements a, c, e, g, ... of the first field of a high resolution correspond to the picture elements a', c', ... of the first field of a low resolution, and the picture elements c, g, ... correspond to the picture elements b', d', ... of the second field of a low resolution.

Describing, for example, the picture element a, in the local decoder ((a) in Figure 8) of the encoder, if 0, 1, 2, 3 or 4 (1 of the motion vector indicates an offset corresponding to 0.5 picture elements in the vertical directions of a screen of a high resolution) is outputted as a motion vector for motion compensation for the picture element a (it is assumed that the motion vector indicates only motion in the vertical direction) from the motion vector detection circuit 50, then a, (a + b)/2, b, (b + c)/2 or c is outputted as a picture element of a predictive picture from the motion compensation circuit 64. In particular, an interpolation picture element is formed when the motion vector is equal to 1 or 3.

On the other hand, on the standard television decoder block side ((b) in Figure 8), when 0, 1, 2, 3 or 4 is outputted as a motion vector for motion compensation for the picture element a' from the variable length decoding circuit 71 (when the motion vector outputted from the scaling circuit 87 is 0, 0.5, 1, 1.5 or 2), a', (3a' + b')/4, (3b' + z')/4, (a' + 3b')/4 or b is outputted as a picture element of a predictive picture from the motion compensation circuit 86. In particular, when the motion vector is 1, 2 or 3 (when the motion vector outputted from the scaling circuit 87 is 0.5, 1 or 1.5), an interpolation picture element is formed. This similarly applies also where the motion vector is greater than 5).

As seen from Figure 8, picture element data of a low resolution (1/4 resolution) correspond to picture element data of a high resolution (full resolution) of the encoder such that the parities (fields) and the positions of them coincide with each other. In particular, when the motion vector is 1 or 3, picture element data of a high resolution are interpolated from the picture element data a and c of the first field and the picture element data b of the second field ((a + b)/2 or (b + c)/2). On the other hand, also picture element data of a low resolution are interpolated, when the motion vector is 1 or 3 (when the motion vector outputted from the scaling circuit 87 is 0.5 or 1.5), from the picture element data a' of the first field and the picture element data b' of the second field. Accordingly, they coincide with each other in parity (field) (both of them are interpolated from the first and second fields). Further, since the weighting values of the picture elements of them are adjusted, the positions of them in the vertical direction coincide with each other.

Further, when the motion vector is equal to 2 (when the motion vector outputted from the scaling circuit 87 is equal to 1), since the picture element data b of a high resolution is data of the second field, also a corresponding picture element of a low resolution is interpolated from the picture elements z' and b' of the second field ((3b' + z')/4). Consequently, the parities and the positions in the vertical direction of them coincide with each other.

Subsequently, motion compensation in the field predictive mode will be described with reference to Figure 9. In this instance, in the local decoder of the encoder, as seen from (a) of Figure 9, picture elements (a + c)/2 and (c + e)/2 of a first predictive field are formed as a predictive picture from a first field including picture elements a, c, e, g, ..., and picture elements (b + d)/2 and (d + f)/2 of a second predictive field are formed as another predictive picture from a second field including picture elements b, d, f, ...

Nokia Exhibit 2004, p. 224 ...
Amazon.com v. Nokia
IPR2024-01141

Meanwhile, in the standard television decoder block, as seen from (b) of Figure 9, picture elements (3a' + c')/4, (a' + c')/2 and (d' + 3c')/4 of a first predictive field are formed as a predictive picture from a first field including picture elements a', c', ... and picture elements (3b' + z')/4, (3b' + d')/4 and (b' + d')/2 of a second predictive field are formed as a predictive picture from a second field including picture elements z', b', d' ... (the distance between z' and b' and the distance between b' and d' are equal to each other).

In particular, in the case of motion compensation, for example, for the picture element a of the first field in accordance with a motion vector, in the encoder, when 0, 1, 2, 3 or 4 is given as a motion vector from the motion vector detection circuit 50, a, (a + c)/2, c, (c + e)/2 or e is outputted as a picture element of a predictive picture from the motion compensation circuit 64, respectively. When the motion vector is 1 or 3, the picture element is interpolated.

Meanwhile, on the standard television decoder block side, when 0, 1, 2, 3 or 4 is give as a motion vector from the variable length decoding circuit 71 (when the motion vector outputted from the scaling circuit 87 is 0, 0.5, 1, 1.5 or 2), a', (3a' + c')/4, (a' + c')/2, (a' + 3c')/4 or c' is outputted as a picture element of a predictive picture from the motion compensation circuit 86, respectively. When the motion vector is 1, 2 or 3 (when the motion vector outputted from the scaling circuit 87 is 0.5, 1 or 1.5), an interpolation picture element is formed by interpolation so that the position of the corresponding picture element may coincide with that in the encoder.

On the other hand, in motion compensation of the picture element of the second field, when 0, 1, 2, 3 or 4 is given as a motion vector to the encoder, b, (b + d)/2, d,(d + f)/2 or f is outputted as a picture element of a predictive picture from the motion compensation circuit 64, respectively. Meanwhile, on the standard television decoder block side, when 0, 1, 2, 3 or 4 is given as a motion vector (when the motion vector outputted from the scaling circuit 87 is O, 0.5, 1, 1.5 or 2), (3b' + z')/4, b', (3b' + d')/2, (b' + d')/2 or (b' + 3d')/4 is outputted as a picture element of a predictive picture from the motion compensation circuit 86, respectively.

An original picture element which corresponds to the picture element b of the second field of a full resolution is not present in the second field of a 1/4 resolution. If the picture element b' is made coincide with the picture element b, then since the positions of them in the vertical direction do not coincide with each other, also the motion compensated picture element is displaced from the original picture element. Therefore, the picture element (3b' + z')/4 is produced at the position at which it coincides with the picture element b.

In each field, since each interpolation data is produced from data in the field, also the parities coincide with each other.

A different manner of motion compensation in the frame predictive mode (frame predictive mode (2)) will be described subsequently with reference to Figure 10. The present manner of motion compensation is different from the manner of motion compensation in the frame predictive mode (1) of Figure 8 in processing on the standard television decoder block side. While a reference picture element when the motion vector is 1, 2 or 3 (when the motion vector outputted from the scaling circuit 87 is 0.5, 1 or 1.5) can be produced by interpolation of the picture element a', b' and/or z' similarly as in the case of Figure 8, a reference picture element when the motion vector is 4 (when the motion vector outputted from the scaling circuit 87 is 2) is produced by interpolation of the picture elements a' and c' of the first field since it is referred to from a field of a same parity as a reference picture element in the encoder, and the picture element of a predictive picture to be outputted from the motion compensation circuit is (a' + c')/2. In other words, in this instance, the picture element b' is used only for interpolation of some other picture element and is not itself outputted as a reference picture element.

Figure 11 is a further manner of motion compensation in the frame predictive mode (frame predictive mode (3)). In the present manner of motion compensation, in the case of a 1/4 resolution, when the motion vector is 1 or 3 (when the motion vector outputted from the scaling circuit 87 is 0.5 or 1.5), a reference picture element is either interpolated as (1/2) (a' + (3b' + z')/4) from the picture elements a' and (3b' + z')/4 or interpolated as (1/2)((a' + c')/2 + (3b' + z')/4) from the picture elements (a' + c')/2 and (3b' + z')/4. Except this, the present manner of motion compensation is the same as the manner of motion compensation of Figure 10.

When motion compensation is performed in response to the frame or field predictive mode (predictive flag) so that coincidence in parity and position may be established in this manner, since mismatch errors arising from incoincidence between a predictive picture of the encoder and another predictive picture of the low resolution decoder are reduced, such a situation is reduced that a picture does not exhibit smooth motion due to the loss of an interlace structure.

Subsequently, processing of the selection circuit 82 of Figure 7 will be described.

Such 8 x 8 coefficient data supplied from the dequantization circuit 82 as seen in Figure 4 are stored into the memory 92 of the selection circuit 83. When the predictive flag supplied from the variable length decoding circuit 71 represents the frame DCT mode, the address control circuit 91 reads out 4 x 4 data at the left upper corner and 1 x 4 data at the left lower corner of the table of Figure 4 and outputs the data

Nokia Exhibit 2004, p. 225
Amazon.com v. Nokia
IPR2024-01141

to the arithmetic circuit 90. The arithmetic circuit 90 adds the four data d(7, 0), d(7, 1), d(7, 2) and d(7, 3) of the eighth row to the four data d(3, 0), d(3, 1), d(3, 2) and d(3, 3) of the fourth row, respectively. As a result, the 4 x 4 coefficients sampled out first and shown in Figure 12 are changed to 4 x 4 coefficients shown in Figure 13. In particular, while the coefficients in the upper three rows in Figure 13 are the same as those in Figure 12, the data in the lowermost row are d(3, 0) + d(7, 0), d(3, 1) + d(7, 1), d(3, 2) + d(7, 2) and d(3, 3) + d(7, 3). The data are written into the memory 92.

Four data corresponding to high frequency components arising from motion between fields of a same frame of an interlace picture are arranged at the four left data in the eighth row shown in Figure 4. Since the four data are added to the corresponding data in the fourth row which correspond to a highest frequency in the low frequency region (4 x 4 data), if the 4 x 4 coefficients (Figure 13) are read out from the address control circuit 91 and supplied to the IDCT circuit 83 so as to be processed by IDCT processing, then the loss of an interlace structure which is caused by sampling out only 4 x 4 coefficient data at the left upper corner in the low frequency region from within 8 x 8 DCT coefficient data while removing the other coefficient data is reduced, and a picture, which otherwise exhibits unnatural motion due to the loss of an interlace structure, is regenerated exhibiting smooth motion.

While high frequency components arising from interlace are included in and around the lowermost row of 8 x 8 DCT coefficient data in the frame DCT mode, such components are not contained in the lowermost row of 8 x 8 DCT coefficients in the field DCT mode. Accordingly, although such processing as illustrated in Figure 13 is performed in the frame DCT mode, it is not performed in the field DCT mode. In this instance, the processing illustrated in Figure 12 is performed.

Figure 14 illustrates another manner of processing of the selection circuit 82 in the frame DCT mode. In the present manner of processing, a sum D3 of absolute values of eight data d(3, 0) to d(3, 7) in the fourth row of Figure 4 is calculated by the arithmetic unit 90. Similarly, a sum D7 of absolute values of eight data d(7, 0) to d(7, 7) in the eighth row is calculated by the arithmetic unit 90. Further, the arithmetic unit 90 compares the sums D3 and D7 with each other, and, if the sum D3 is greater than the sum D7, it selects the data d(3, 0) to d(3, 3) as the four data of the fourth row of the 4 x 4 coefficients, but on the contrary if the sum D7 is greater than the sum D3, it selects the data d(7, 0) to d(7, 3). Figure 14 illustrates the condition in this instance.

In particular, that the sum D3 is greater than the sum D7 means that the picture exhibits motion of a comparatively small amount between the two fields in the frame. Accordingly, in this instance, not the data d(7, 0) to d(7, 3) corresponding to high frequency components but the data d(3, 0) to d(3, 3) corresponding to low frequency components are selected. On the contrary, when the sum D7 is greater than the sum D3, since the picture exhibits motion of a comparatively great amount, the data d(7, 0) to d(7, 3) corresponding to higher frequency components are selected.

Figure 15 illustrates a further manner of processing. In the present manner of processing, when the sum D3 described above is greater than the sum D7, such coefficients as shown in Figure 12 are selected as the 4 x 4 coefficients, but when the sum D7 is greater than the sum D3, four left side data d(6, 0) to d(6, 3) in the seventh row in Figure 4 and four left side data d(7, 0) to d(7, 3) in the eighth row are selected, and the 2 x 4 data are replaced with four left side data d(2, 0) to d(2, 3) in the third row and four left side data d(3, 0) to d(3, 3) in the fourth row, respectively. In short, such 4 x 4 data as seen in Figure 15 are obtained. In the present manner of processing, higher frequency components are contained by a greater amount than in the manner of processing illustrated in Figure 14.

It is to be noted that, when the predictive flag supplied from the variable length decoding circuit 71 indicates the frame predictive mode and the selection circuit 82 determines that the sum D3 is greater than the sum D7, motion compensation may be performed in the frame predictive mode (1), but when the sum D7 is greater than the sum D3, motion compensation may be performed in the frame predictive mode (2). This is because, when the sum D3 is greater than the sum D7, since the picture exhibits motion of a small amount between the fields of the frame as described above, b' - (a' + c')/2, and consequently, even if (a' + c')/2 is not produced by interpolation, a sufficient predictive picture can be obtained.

Subsequently, a method of zigzag scanning when such processing as described above is to be executed will be described. In order to realize the three manners of processing described above, it is possible, similarly as in the prior art, for the variable length coding circuit 58 of the encoder to scan 8 x 8 coefficients in a zigzag pattern such that, for example, as shown in Figure 5, the scanning point first moves rightwardly from the number 1 at the left upper corner to the number 2 on the right side and then moves to the number 3 on the obliquely left lower side and then to the number 4 below the number 3, whereafter it advances to the number 5 on the obliquely right upper side. However, if zigzag scanning is performed in such a manner as, for example, in Figure 16, then data can be transmitted in a higher efficiency.

In the manner of zigzag scanning illustrated in Figure 16, zigzag scanning is first performed within

Nokia Exhibit 2004, p. 226
Amazon.com v. Nokia
IPR2024-01141

the range of 4 x 4 coefficients at the left upper corner in 8 x 8 coefficients. In particular, the coefficient at the number 1 at the left upper corner is first transmitted, and then the coefficient at the number 2 on the right side to the number 1 is transmitted. Thereafter, the scanning point moves to the number 3 on the obliquely left lower side to the number 2, and then to the number 4 below the number 3, whereafter it moves to the number 5 on the obliquely right upper side to the number 4. The 16 coefficients are transmitted in a similar manner. Subsequently, four left side coefficients of the numbers 17 to 20 in the eighth row are successively transmitted, and thereafter, four left side coefficients of the numbers 21 to 24 in the seventh row are successively transmitted beginning with the leftmost one. Then, after a total of 24 coefficients are transmitted in this manner, the scanning point advances to the coefficient at the number 25 at the leftmost position in the fifth row, and zigzag scanning is performed successively in the oblique direction except the coefficients which have been transmitted already.

The transmission by zigzag scanning is illustrated in a syntax diagram of Figure 17. Referring to Figure 17, a quantization scale is transmitted first, and then a DCT coefficient which is indicated at the number 1 in Figure 16 and represents a dc component is transmitted. Subsequently, DCT coefficients of low frequencies indicated at the numbers 2 to 4 in Figure 16 are transmitted successively. Then, after the 24 coefficients are transmitted, a signal EOB representative of the end of the block is sent out.

After the signal EOB is sent out, a dequantization scale is sent out again. The first quantization scale indicates a quantization step which is used until the first EOB signal is sent out, and the second quantization scale indicates another quantization step which is used for coefficients to be transmitted later. After the second quantization scale is sent out, the remaining coefficients of the numbers 25 to 64 in Figure 16 are successively transmitted in the order of the numbers. Then, after the 64th coefficient is transmitted, another EOB signal indicative of the end of the block is transmitted again. The EOB signals are generated by an EOB generator 58a built in the variable length coding circuit 58 of Figure 1.

If data are transmitted in such an order as described above, when the selection circuit 82 of the decoder shown in Figure 6 receives the first EOB signal, it may skip the coefficients which are transmitted thereto since then and then start its processing beginning with a coefficient transmitted immediately after the second EOB signal is thereafter transmitted thereto. On the other hand, in the high definition television signal system, the IDCT circuit 73 ignores the first EOB signal and detects the second EOB signal as an end signal of the block.

While, in the foregoing description, a manner of processing is selected by the decoder side, it is otherwise possible for the encoder side to given an instruction of processing. FIGS. 18 and 19 respectively show an encoder and a decoder constructed in a manner just described. In particular, in the encoder shown in Figure 18, a motion vector detection circuit 101 (the motion vector detection circuit 50 may serve also as the motion vector detection circuit 101) detects a motion vector of a block from picture data for one field stored in a frame memory 51. The reason why a motion vector is detected not from data for one frame but from data for one field is that it is intended to detect motion in interlace, that is, motion between an odd-numbered field and an even-numbered field. The motion vector (motion information) detected by the motion vector detection circuit 101 is supplied to a variable length coding circuit 58, from which it is transmitted as data of 1 bit or 2 bits and as a bit stream to the decoder side.

On the decoder side, as shown in Figure 19, a variable length decoding circuit 71 detects the motion information transmitted thereto from the encoder side and controls a selection circuit 82 in accordance with the motion information. In particular, the selection circuit 82 is constructed as shown, for example, in Figure 20. Referring to Figure 20, the motion information supplied thereto from the variable length decoding circuit 71 is discriminated by a discrimination circuit 111, and an address control circuit 91 is controlled in accordance with a result of the discrimination to control data to be read out from the memory 92.

Accordingly, in order to allow two of the manners of processing illustrated in FIGS. 13 to 15 to be executed, if a predetermined flag of one bit is transmitted from the encoder side, then two of the manners of processing illustrated in FIGS. 13 to 15 can be executed on the decoder side in response to the flag.

Furthermore, if, for example, 2 bits are prepared for such motion information as described above, then a total of four kinds of data can be sent out. Therefore, motion can be divided into fourth types including a great amount of motion, a medium amount of motion, a small amount of motion and a stopping condition, and when the amount of motion is great, the processing illustrated in Figure 15 may be executed; when the amount of motion is medium, the processing illustrated in Figure 14 may be executed; when the amount of motion is small, the processing illustrated in Figure 13 may be executed; and when the picture is in a stopping condition, the processing illustrated in Figure 12 may be executed.

While, in the foregoing description, coefficient data of the fourth row or coefficient data of the third and fourth rows of 4 x 4 coefficient data are replaced by coefficient data of the eighth row or coefficient data of the seventh and eighth rows, respectively, at least one coefficient data may be replaced. Or on the contrary, the number of rows to be replaced may be

Nokia Exhibit 2004, p. 227
Amazon.com v. Nokia
IPR2024-01141

increased to three.

Further, while data along a row or rows are replaced in the foregoing description, data along a column or columns may be replaced alternatively.

Furthermore, while picture data are processed by DCT processing in the foregoing description, the present invention can be applied to any other orthogonal transformation than the DCT.

Further, while, in the foregoing description, 8 x 8 quantized data outputted from the quantization circuit 57 are coded as they are into variable length codes and transmitted on the encoder side and, when a picture of the standard television system is to be obtained, 4 x 4 data are sampled out on the decoder side, when 4 x 4 quantized data on the low frequency side (at the left upper corner) are separated from the other quantized data and then the 4 x 4 quantized data and the other data are individually coded into variable length codes and transmitted on the encoder side, in order to obtain a picture of the standard television system, only the 4 x 4 quantized data on the low frequency side (at the left upper corner) may be decoded as they are, but in order to obtain a picture of a full resolution, both of the 4 x 4 quantized data and the other data may be decoded by variable length decoding into two kinds of quantized data, which are dequantized subsequently.

As apparent from the foregoing description, according to the present invention, when coefficient data of a particular range are sampled out from within a predetermined number of coefficient data and inverse orthogonal transformation is to be performed for the thus sampled out coefficient data, the coefficient data are processed so that they include those coefficient data which are not included in the particular range. Further, motion compensation is performed in response to a predictive flag so that a predictive picture and a parity of fields on the decoder side may coincide with those on the encoder side. Consequently, such a situation that smooth motion of the picture is disturbed by the loss of an interlace structure is eliminated or minimized.

Having now fully described the invention, it will be apparent to one of ordinary skill in the art that many changes and modifications can be made thereto without departing from the scope of the invention as set forth herein.

Claims

1. A picture signal decoding method comprising the steps of:

   sampling out from coefficient data of a first block formed by orthogonal transformation of picture element data, those of the coefficient data of a second block having a smaller range than the first block;

   replacing at least one of the coefficient data in the second block by a corresponding one or ones of the coefficient data in the first block but outside the second block; and

   performing inverse orthogonal transformation for the coefficient data of the second block.

2. A picture signal decoding method according to claim 1, wherein the first block includes m x n coefficient data while the second block includes j x k coefficient data, j being smaller than m, k being smaller than n, and the inverse orthogonal transformation being performed for data obtained by replacing successive ones of the coefficient data of the j-N+1th row to the jth row in the second block by corresponding ones of the coefficient data of the m-N+1th row to the mth row in the corresponding columns of the first block, respectively, N being 1, 2, 3, ..., j-1.

3. A picture signal decoding method according to any one of claims 1 and 2, wherein the orthogonal transformation is a discrete cosine transform, and the inverse orthogonal transformation is an inverse discrete cosine transform.

4. A picture signal decoding method according to any one of claims 1, 2 or 3, wherein the picture element data are picture element data of a frame formed from two fields and having an interlace structure, and where the coefficient data of the first block are produced based on a difference from a predictive picture for which motion compensation has been performed in a frame predictive mode or a field predictive mode, motion compensation being performed in response to a predictive mode of the first block to produce a predictive picture for the second block.

5. A picture signal decoding method according to claim 4, wherein, where the coefficient data of the first block are produced based on the difference from the predictive picture for which the motion compensation has been performed in the frame predictive mode, motion compensation for the second block is performed so that a field of picture elements of the predictive picture for the second block may coincide with a corresponding field of picture elements of a predictive picture for the first block.

6. A picture signal decoding method according to claim 5, wherein, when the picture elements of the predictive picture for the first block are produced by interpolation upon the motion compensation, also corresponding picture elements of the predictive picture for the second block are

Nokia Exhibit 2004, p. 228
Amazon.com v. Nokia
IPR2024-01141

produced by interpolation.

7. A picture element decoding method according to any one of claims 4 and 5, wherein, when picture elements corresponding to the picture elements of the predictive picture for the first block are present in the predictive picture for the second block upon the motion compensation, the picture elements are used for motion compensation.

8. A picture signal decoding method according to any one of claims 4 and 5, wherein, where the coefficient data of the first block are produced based on the difference from the predictive picture for which the motion compensation has been performed in the field predictive mode, motion compensation for the second block is performed so that the positions of the picture elements of the predictive picture for the second block may coincide with the positions of corresponding picture elements of a predictive picture for the first block.

9. A picture signal decoding method comprising the steps of:

sampling out from coefficient data of a first block formed by orthogonal transformation of picture element data, those of the coefficient data of a second block having a smaller range than the first block;

replacing at least one of the coefficient data in the second block by a sum or sums between the at least one coefficient data in the second block and a corresponding one or ones of the coefficient data in the first block but outside the second block; and

performing inverse orthogonal transformation for the coefficient data of the second block.

10. A picture signal decoding method according to claim 9, wherein the first block includes m x n coefficient data while the second block includes j x k coefficient data, j being smaller than m, k being smaller than n, and the inverse orthogonal transformation is performed for data obtained by replacing successive ones of the coefficient data in the jth row of the second block with a sum or sums between the coefficient data of the jth row in the second block and corresponding ones of the coefficient data in the mth row of the first block in the respective corresponding columns.

11. A picture signal decoding method according to claim 9, wherein m is equal to n and j is equal to k.

12. A picture signal decoding method according to claim 11, wherein m and n are equal to 8, and j and k are equal to 4.

13. A picture signal decoding method according to any one of claims 9 to 12, wherein the orthogonal transformation is a discrete cosine transform, and the inverse orthogonal transformation is an inverse discrete cosine transform.

14. A picture signal decoding method according to any one of claims 9 to 13, wherein the picture element data are picture element data of a frame formed from two fields and having an interlace structure, and where the coefficient data of the first block are produced based on a difference from a predictive picture for which motion compensation has been performed in a frame predictive mode or a field predictive mode, motion compensation being performed in response to a predictive mode of the first block to produce a predictive picture for the second block.

15. A picture signal decoding method according to claim 14, wherein, where the coefficient data of the first block are produced based on the difference from the predictive picture for which the motion compensation has been performed in the frame predictive mode, motion compensation for the second block is performed so that a field of picture elements of the predictive picture for the second block may coincide with a corresponding field of picture elements of a predictive picture for the first block.

16. A picture signal decoding method according to claim 15, wherein, when the picture elements of the predictive picture for the first block are produced by interpolation upon the motion compensation, also corresponding picture elements of the predictive picture for the second block are produced by interpolation.

17. A picture element decoding method according to any one of claims 14 and 15, wherein, when picture elements corresponding to the picture elements of the predictive picture for the first block are present in the predictive picture for the second block upon the motion compensation, the picture elements are used for motion compensation.

18. A picture signal decoding method according to any one of claims 14 and 15, wherein, where the coefficient data of the first block are produced based on the difference from the predictive picture for which the motion compensation has been performed in the field predictive mode, motion compensation for the second block is performed

Nokia Exhibit 2004, p. 229
Amazon.com v. Nokia
IPR2024-01141

so that the positions of the picture elements of the predictive picture for the second block may coincide with the positions of corresponding picture elements of a predictive picture for the first block.

19. A picture signal decoding method comprising the steps of:

sampling out from m x n coefficient data of a first block formed by orthogonal transformation of picture element data of a frame formed from two fields and having an interlace structure, a second block including j x k coefficient data, j being smaller than m and k being smaller than n;

discriminating motion between the two fields of the first block;

selecting, in response to a result of the discrimination, one of a first inverse orthogonal transformation mode in which the coefficient data of the second block are transformed as they are by inverse orthogonal transformation and a second inverse orthogonal transformation mode in which the inverse orthogonal transformation is performed for data obtained by replacing at least one of the coefficient data in the second block by a corresponding one or ones of the coefficient data in the first block but outside the second block; and

performing inverse orthogonal transformation for the coefficient data of the second block.

20. A picture signal decoding method according to claim 19, wherein m is equal to n and j is equal to k.

21. A picture signal decoding method according to claim 20, wherein m and n are equal to 8, and j and k are equal to 4.

22. A picture signal decoding method according to any one of claims 19 to 21, wherein the orthogonal transformation is a discrete cosine transform, and the inverse orthogonal transformation is an inverse discrete cosine transform.

23. A picture signal decoding method comprising the steps of:

sampling out from m x n coefficient data of a first block formed by orthogonal transformation of picture element data of a frame having an interlace structure formed from two fields, a second block including j x k coefficient data, j being smaller than m and k being smaller than n;

discriminating motion between the two fields of the first block;

selecting, in response to a result of the discrimination, one of a first inverse orthogonal transformation mode in which the coefficient data of the second block are transformed as they are by inverse orthogonal transformation and a second inverse transformation mode in which the inverse orthogonal transformation is performed for data obtained by replacing successive ones of the coefficient data of the j-N+1th row to the jth row in the second block by corresponding ones of the coefficient data of the m-N+1th row to the mth row in the corresponding columns of the first block, respectively, N being 1, 2, 3, ... j-1; and

performing inverse orthogonal transformation for the coefficient data of the second block.

24. A picture signal decoding method according to claim 23, wherein motion between the two fields is discriminated from a result of comparison between an absolute value sum J of the coefficient data of the jth line in the first block and another absolute value sum M of the coefficient data of the mth row in the first block.

25. A picture signal decoding method according to claim 24, wherein, where the m x n coefficient data of the first block are produced based on a difference from a predictive picture for which motion compensation has been performed in a frame predictive mode, when the absolute value sum J is equal to or greater than the absolute value sum M, a predictive picture for the second block is produced in a first frame predictive mode, but when the absolute value sum J is smaller than the absolute value sum M, a predictive picture for the second block is produced in a second frame predictive mode.

26. A picture signal decoding method according to claim 24, wherein, when the absolute value sum J is equal to or greater than the absolute value sum M, the first inverse orthogonal transformation mode is selected, but when the absolute value J is smaller than the absolute value sum M, the second inverse orthogonal transformation mode wherein N is equal to 1 is selected.

27. A picture signal decoding method according to claim 24, wherein, when the absolute value sum J is equal to or greater than the absolute value sum M, the first inverse orthogonal transformation mode is selected, but when the absolute value J is smaller than the absolute value sum M, the second inverse orthogonal transformation mode wherein N is equal to 2 is selected.

28. A picture signal decoding method according to any one of claims 24 to 27, wherein m is equal to n and j is equal to k

Nokia Exhibit 2004, p. 230
Amazon.com v. Nokia
IPR2024-01141

Page 230 of 350

29. A picture signal decoding method according to any one of claims 24 to 27, wherein the orthogonal transformation is a discrete cosine transform, and the inverse orthogonal transformation is an inverse discrete cosine transform.

30. A picture signal decoding method comprising the steps of:

sampling out from m x n coefficient data of a first block formed by orthogonal transformation of picture element data of a frame formed from two fields and having an interlace structure, a second block including j x k coefficient data, j being smaller than m, k being smaller than n;

selecting, in accordance with information transmitted together with the coefficient data, one of a first inverse orthogonal transformation mode in which the coefficient data of the second block are transformed as they are by inverse orthogonal transformation and a second inverse orthogonal transformation mode in which the inverse orthogonal transformation is performed for data obtained by replacing successive ones of the coefficient data of the j-N+1th to jth rows in the second block by corresponding ones of the coefficient data of the m-N+1th to mth rows in the corresponding columns, respectively, N being 1, 2, 3, ..., j-1; and

performing inverse orthogonal transformation for the coefficient data of the second block.

31. A picture signal decoding method according to claim 30, wherein the information includes first motion information which represents a stopping condition and second motion information which represents some motion, and when the first motion information is detected, the first inverse orthogonal transformation mode is selected, but when the second motion information is detected, the second inverse orthogonal transformation mode wherein N is equal to 1 is selected.

32. A picture signal decoding method according to claim 30, wherein the information includes first motion information which represents a stopping condition and second motion information which represents some motion, and when the first motion information is detected, the first inverse orthogonal transformation mode is selected, but when the second motion information is detected, the second inverse orthogonal transformation mode wherein N is equal to 2 is selected.

33. A picture signal decoding method according to claim 30, wherein the information includes first motion information which represents a stopping condition, second motion information which represents small motion, and third motion information which represents great motion, and when the first motion information is detected, the first inverse orthogonal transformation mode is selected; when the second motion information is detected, the second inverse orthogonal transformation mode wherein N is equal to 1 is selected; and when the third motion information is detected, the second inverse orthogonal transformation mode wherein N is equal to 2 is selected.

34. A picture signal decoding method according to claim 30, wherein m is equal to n and j is equal to k.

35. A picture signal decoding method according to claim 34, wherein m and n are equal to 8, and j and k are equal to 4.

36. A picture signal decoding method according to any one of claims 30 to 35, wherein the orthogonal transformation is a discrete cosine transform, and the inverse orthogonal transformation is an inverse discrete cosine transform.

37. A picture signal coding apparatus, comprising:

orthogonal transformation means for transforming picture element data of a frame formed from two fields and having an interlace structure by orthogonal transformation to form m x n coefficient data;

quantization means for quantizing the coefficient data and outputting quantization data obtained by the quantization; and

variable length coding means for coding the quantization data into variable length codes and successively transmitting the quantization data in the order of those coefficient data of a first quantization data group which correspond to j x k ones of the m x n coefficient data, j being smaller than m and k being smaller than n, those coefficient data of a second quantization data group which correspond to those of the m x n coefficient data which belong to the m-N+1th to mth rows in the first to kth columns, N being 1, 2, 3, ..., j-1, and those coefficient data of a third quantization data group which correspond to those of the m x n coefficient data which do not belong to any of the first and second quantization data groups.

38. A picture signal coding apparatus according to claim 37, wherein said variable length coding means includes means for adding end information to each of the second and third quantization data groups.

39. A picture signal coding apparatus according to

Nokia Exhibit 2004, p. 231
Amazon.com v. Nokia
IPR2024-01141

claim 37, wherein wherein m is equal to n and j is equal to k.

40. A picture signal coding apparatus according to claim 39, wherein m and n are equal to 8, and j and k are equal to 4.

41. A picture signal coding apparatus according to claim 37, wherein the orthogonal transformation is a discrete cosine transform.

42. A picture signal coding apparatus, comprising:

orthogonal transformation means for transforming picture element data of a frame formed from two fields and having an interlace structure by orthogonal transformation to form m x n coefficient data;

motion detection means for detecting motion between the two fields and outputting corresponding motion information;

quantization means for quantizing the coefficient data and outputting quantization data obtained by the quantization; and

variable length coding means for coding the motion information and the quantization data into variable length codes and outputting the variable length codes.

43. A picture signal coding apparatus according to claim 42, wherein the quantization data are converted into variable length codes and successively transmitted in the order of those coefficient data of a first quantization data group which correspond to j x k ones of the m x n coefficient data, j being smaller than m and k being smaller than n, those coefficient data of a second quantization data group which correspond to those of the m x n coefficient data which belong to the m-N+1th to mth rows in the first to kth columns, N being 1, 2, 3, ..., j-1, and those coefficient data of a third quantization data group which correspond to those of the m x n coefficient data which do not belong to any of the first and second quantization data groups.

44. A picture signal coding apparatus according to claim 42, wherein said variable length coding means includes means for adding end information to each of the second and third quantization data groups.

45. A picture signal coding apparatus according to claim 42, wherein wherein m is equal to n and j is equal to k.

46. A picture signal coding apparatus according to claim 45, wherein m and n are equal to 8, and j and k are equal to 4.

47. A picture signal decoding apparatus wherein transmission picture element data of a frame formed from two fields and having an interlace structure are transformed by orthogonal transformation to form m x n coefficient data, and then the coefficient data are quantized and coded into variable length codes to decode the transmission data, comprising:

variable length decoding means for decoding the transmission data by variable length decoding to obtain decoded data and outputting the decoded data;

dequantization means for dequantizing the decoded data to obtain coefficient data and outputting the coefficient data;

sampling out means for sampling out, from the coefficient data, j x k coefficient data obtained by replacing successive ones of the coefficient data of the jth row by sums of the successive coefficient data of the jth row and corresponding ones of the coefficient data of the mth row in the corresponding columns, j being smaller than m, k being smaller than n; and

inverse orthogonal transformation means for transforming the j x k coefficient data sampled out by said sampling out means by inverse orthogonal transformation.

48. A picture signal decoding apparatus according to claim 47, wherein m is equal to n and j is equal to k.

49. A picture signal decoding apparatus according to claim 47 or 48, wherein the orthogonal transformation is a discrete cosine transform, and the inverse orthogonal transformation is an inverse discrete cosine transform.

50. A picture signal decoding apparatus wherein transmission picture element data of a frame formed from two fields and having an interlace structure are transformed by orthogonal transformation to form m x n coefficient data which constitute a first block, and then the coefficient data are quantized and coded into variable length codes to decode the transmission data, comprising:

variable length decoding means for decoding the transmission data by variable length decoding to obtain decoded data and outputting the decoded data;

dequantization means for dequantizing the decoded data to obtain coefficient data and outputting the coefficient data;

motion discrimination means for discriminating motion between the two fields in the first block;

sampling out means responsive to a result

Nokia Exhibit 2004, p. 232
Amazon.com v. Nokia
IPR2024-01141

of the discrimination by said motion discrimination means for selectively sampling out first j x k ones of the coefficient data, j being smaller than m, k being smaller than n, or second j x k coefficient data obtained by replacing successive ones of the coefficient data of the j-N+1th to jth rows by those of the coefficient data of the m-N+1th to mth rows in the corresponding columns, N being 1, 2, 3, ..., j-1; and

inverse orthogonal transformation means for transforming the j x k coefficient data sampled out by said sampling out means by inverse orthogonal transformation.

51. A picture signal decoding apparatus according to claim 50, wherein said discrimination means includes means for calculating an absolute value sum J of the coefficient data of the jth line, means for calculating another absolute value sum M of the coefficient data of the mth row in columns corresponding to those of the coefficient data of the jth row, and means for comparing the absolute value sum J and the absolute value sum M with each other.

52. A picture signal decoding apparatus according to claim 51, wherein said sampling out means selects the first coefficient data when the absolute value sum J is equal to or greater than the absolute value sum M, but selects the second coefficient data wherein N is equal to 1 when the absolute value J is smaller than the absolute value sum M.

53. A picture signal decoding apparatus according to claim 51, wherein said sampling out means selects the first coefficient data when the absolute value sum J is equal to or greater than the absolute value sum M, but selects the second coefficient data wherein N is equal to 2 when the absolute value J is smaller than the absolute value sum M.

54. A picture signal decoding apparatus according to claim 50, wherein said motion discrimination means includes motion information detection means for detecting motion information included in the transmission data.

55. A picture signal decoding apparatus according to claim 54, wherein the information includes first motion information which represents a stopping condition and second motion information which represents some motion, and said sampling out means selects the first coefficient data when the first motion information is detected, but selects the second coefficient data wherein N is equal to 1 is selected when the second motion information is detected.

56. A picture signal decoding apparatus according to claim 54, wherein the information includes first motion information which represents a stopping condition and second motion information which represents some motion, and said sampling out means selects the first coefficient data when the first motion information is detected, but selects the second coefficient data wherein N is equal to 2 is selected when the second motion information is detected.

57. A picture signal decoding apparatus according to claim 54, wherein the information includes first motion information which represents a stopping condition, second motion information which represents small motion, and third motion information which represents great motion, and said sampling out means selects the first coefficient data when the first motion information is detected, but selects the second coefficient data wherein N is equal to 1 when the second motion information is detected, and otherwise selects the coefficient data wherein N is equal to 2 when the third motion information is detected.

58. A picture signal decoding apparatus according to claim 50, wherein m is equal to n and j is equal to k.

59. A picture signal decoding apparatus according to claim 58, wherein m and n are equal to 8, and j and k are equal to 4.

60. A picture signal decoding apparatus according to any one of claims 50 to 59, wherein the orthogonal transformation is discrete cosine transform, and the inverse orthogonal transformation is inverse discrete cosine transform.

61. A picture signal coding method, comprising the steps of:

transforming picture element data of a frame formed from two fields and having an interlace structure by orthogonal transformation to form m x n coefficient data;

quantizing the coefficient data and outputting quantization data obtained by the quantization; and

coding the quantization data into variable length codes in the order of those coefficient data of a first quantization data group which correspond to j x k ones of the m x n coefficient data, j being smaller than m, k being smaller than n, those coefficient data of a second quantization data group which correspond to those of the m x n coefficient data which belong to the m-N+1th to

Nokia Exhibit 2004, p. 233
Amazon.com v. Nokia
IPR2024-01141

mth rows in the first to kth columns, N being 1, 2, 3, ..., j-1, and those coefficient data of a third quantization data group which correspond to those of the m x n coefficient data which do not belong to any of the first and second quantization data groups.

62. A picture signal coding method according to claim 61, wherein the quantization data after conversion into variable length codes are transmitted after end information is added to each of the second and third quantization data groups.

63. A picture signal coding method according to claim 61, wherein m is equal to n and j is equal to k.

64. A picture signal coding method according to any one of claims 61 to 63, wherein the orthogonal transformation is a discrete cosine transform.

65. A picture signal coding method, comprising the steps of:

transforming picture element data of a frame formed from two fields and having an interlace structure by orthogonal transformation to form m x n coefficient data;

detecting motion between the two fields and outputting corresponding motion information;

quantizing the coefficient data and outputting quantization data obtained by the quantization; and

coding the motion information and the quantization data into variable length codes and transmitting the variable length codes.

66. A picture signal coding method according to claim 65, wherein the transmission of the quantization data after conversion into variable length codes is performed in the order of those coefficient data of a first quantization data group which correspond to j x k ones of the m x n coefficient data, j being smaller than m, k being smaller than n, those coefficient data of a second quantization data group which correspond to those of the m x n coefficient data which belong to the m-N+1th to mth rows in the first to kth columns, N being 1, 2, 3, ..., j-1, and those coefficient data of a third quantization data group which correspond to those of the m x n coefficient data which do not belong to any of the first and second quantization data groups.

67. A picture signal coding method according to claim 65, wherein the quantization data after conversion into variable length codes are transmitted after end information is added to each of the second and third quantization data groups.

68. A picture signal coding method according to claim 65, wherein m is equal to n and j is equal to k.

69. A picture signal coding method according to claim 68, wherein m and n are equal to 8, and j and k are equal to 4.

70. A picture signal coding method according to any one of claims 65 to 69, wherein the orthogonal transformation is a discrete cosine transform.

Nokia Exhibit 2004, p. 234
Amazon.com v. Nokia
IPR2024-01141

FIG. 1(A)

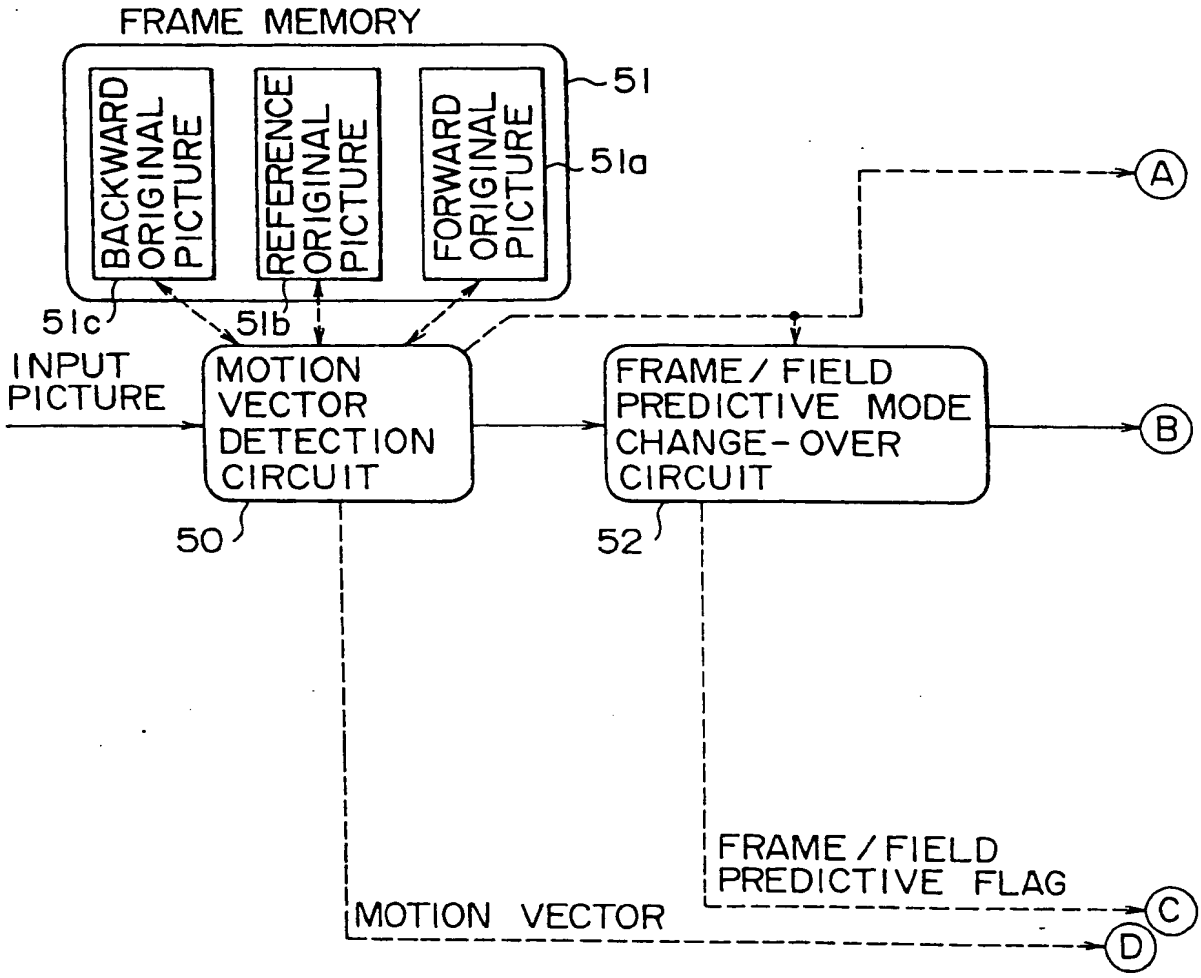
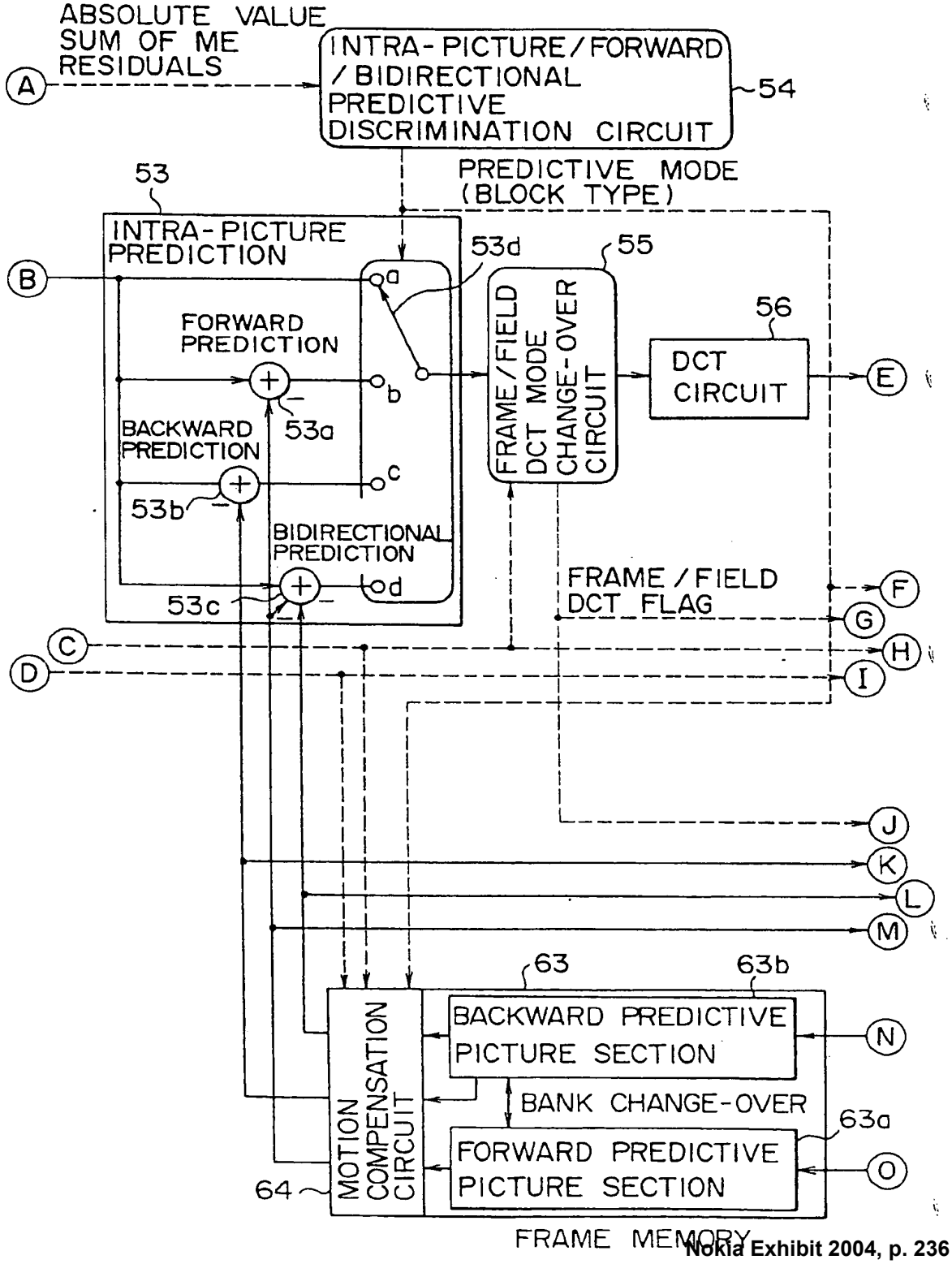


FIG. 1

FIG. 1(A)	FIG. 1(B)	FIG. 1(C)

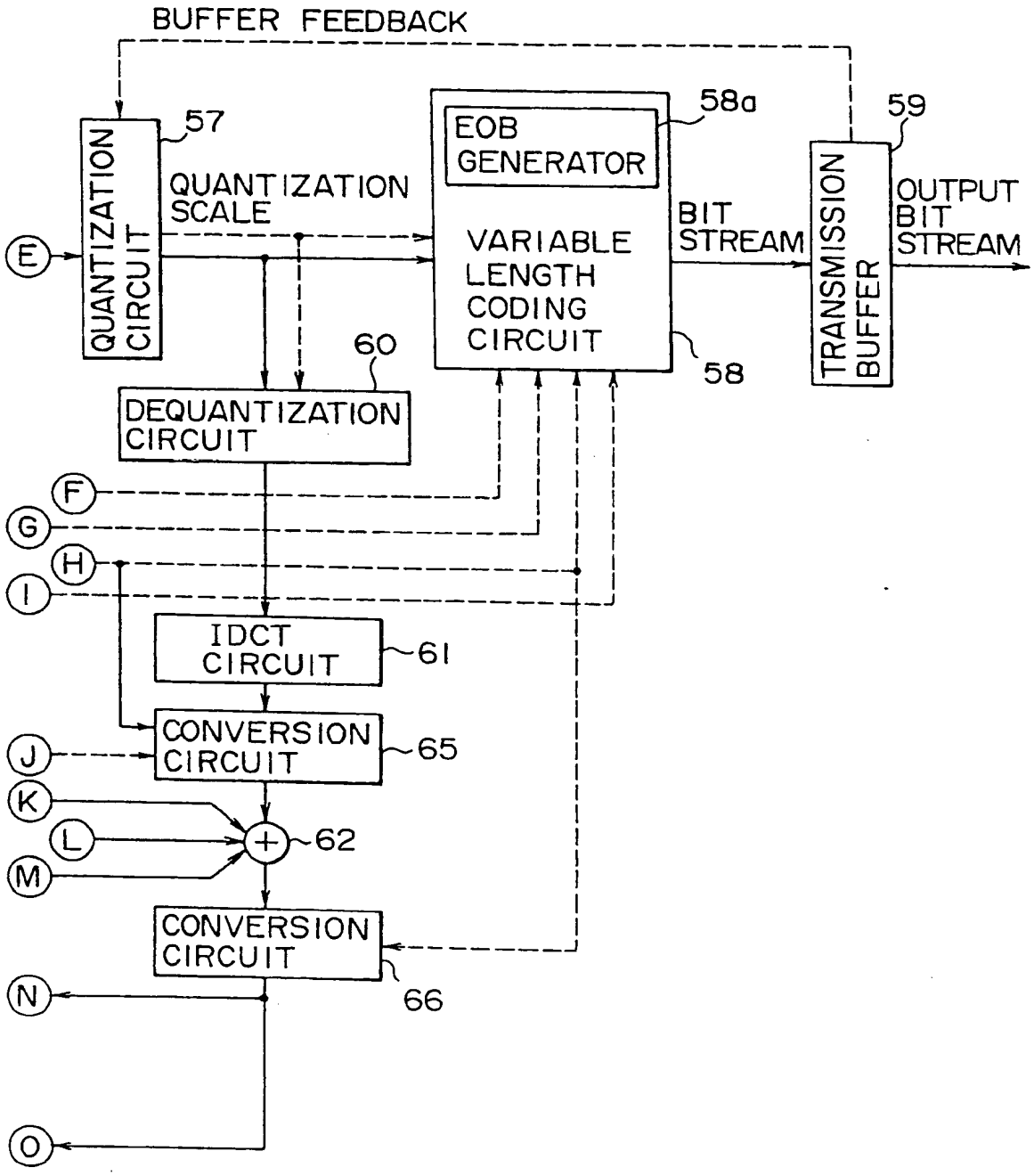
Nokia Exhibit 2004, p. 235
Amazon.com v. Nokia
IPR2024-01141

FIG. 1(B)



Nokia Exhibit 2004, p. 236
Amazon.com v. Nokia
IPR2024-01141

FIG. 1(C)



Nokia Exhibit 2004, p. 237
Amazon.com v. Nokia
IPR2024-01141

FIG. 2(A)

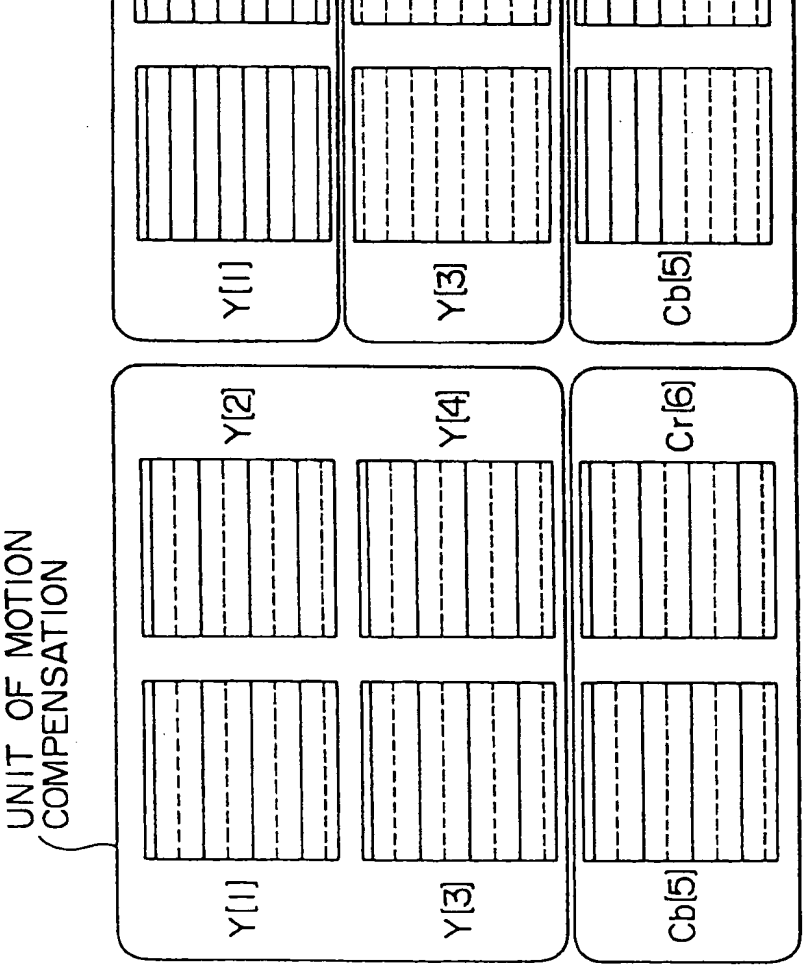
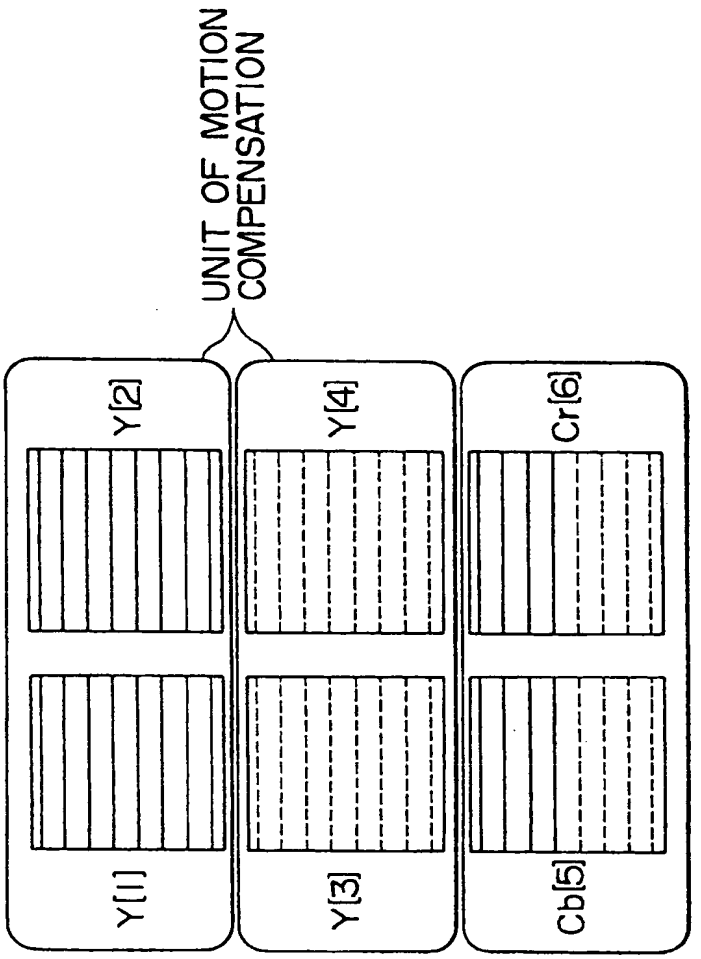


FIG. 2(B)



Nokia Exhibit 2004, p. 238
Amazon.com v. Nokia
IPR2024-01141

FIG. 3(A)

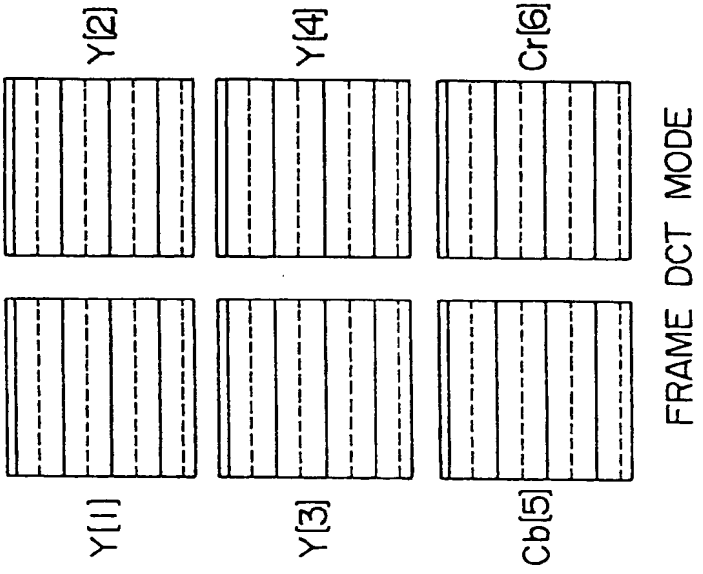
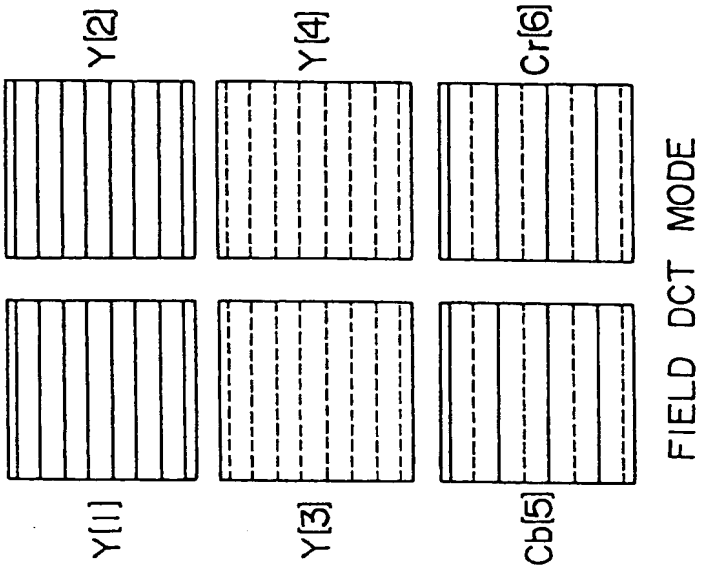


FIG. 3(B)



——— DATA OF FIRST FIELD

- - - - - DATA OF SECOND FIELD

Nokia Exhibit 2004, p. 239
Amazon.com v. Nokia
IPR2024-01141

FIG. 4

d(0,0)	d(0,1)	d(0,2)	d(0,3)	d(0,4)	d(0,5)	d(0,6)	d(0,7)
d(1,0)	d(1,1)	d(1,2)	d(1,3)	d(1,4)	d(1,5)	d(1,6)	d(1,7)
d(2,0)	d(2,1)	d(2,2)	d(2,3)	d(2,4)	d(2,5)	d(2,6)	d(2,7)
d(3,0)	d(3,1)	d(3,2)	d(3,3)	d(3,4)	d(3,5)	d(3,6)	d(3,7)
d(4,0)	d(4,1)	d(4,2)	d(4,3)	d(4,4)	d(4,5)	d(4,6)	d(4,7)
d(5,0)	d(5,1)	d(5,2)	d(5,3)	d(5,4)	d(5,5)	d(5,6)	d(5,7)
d(6,0)	d(6,1)	d(6,2)	d(6,3)	d(6,4)	d(6,5)	d(6,6)	d(6,7)
d(7,0)	d(7,1)	d(7,2)	d(7,3)	d(7,4)	d(7,5)	d(7,6)	d(7,7)

Nokia Exhibit 2004, p. 240
Amazon.com v. Nokia
IPR2024-01141

FIG. 5

1	2	6	7	15	16	28	29
3	5	8	14	17	27	30	43
4	9	13	18	26	31	42	44
10	12	19	25	32	41	45	54
11	20	24	33	40	46	53	55
21	23	34	39	47	52	56	61
22	35	38	48	51	57	60	62
36	37	49	50	58	59	63	64

ZIGZAG SCAN

Nokia Exhibit 2004, p. 241
Amazon.com v. Nokia
IPR2024-01141

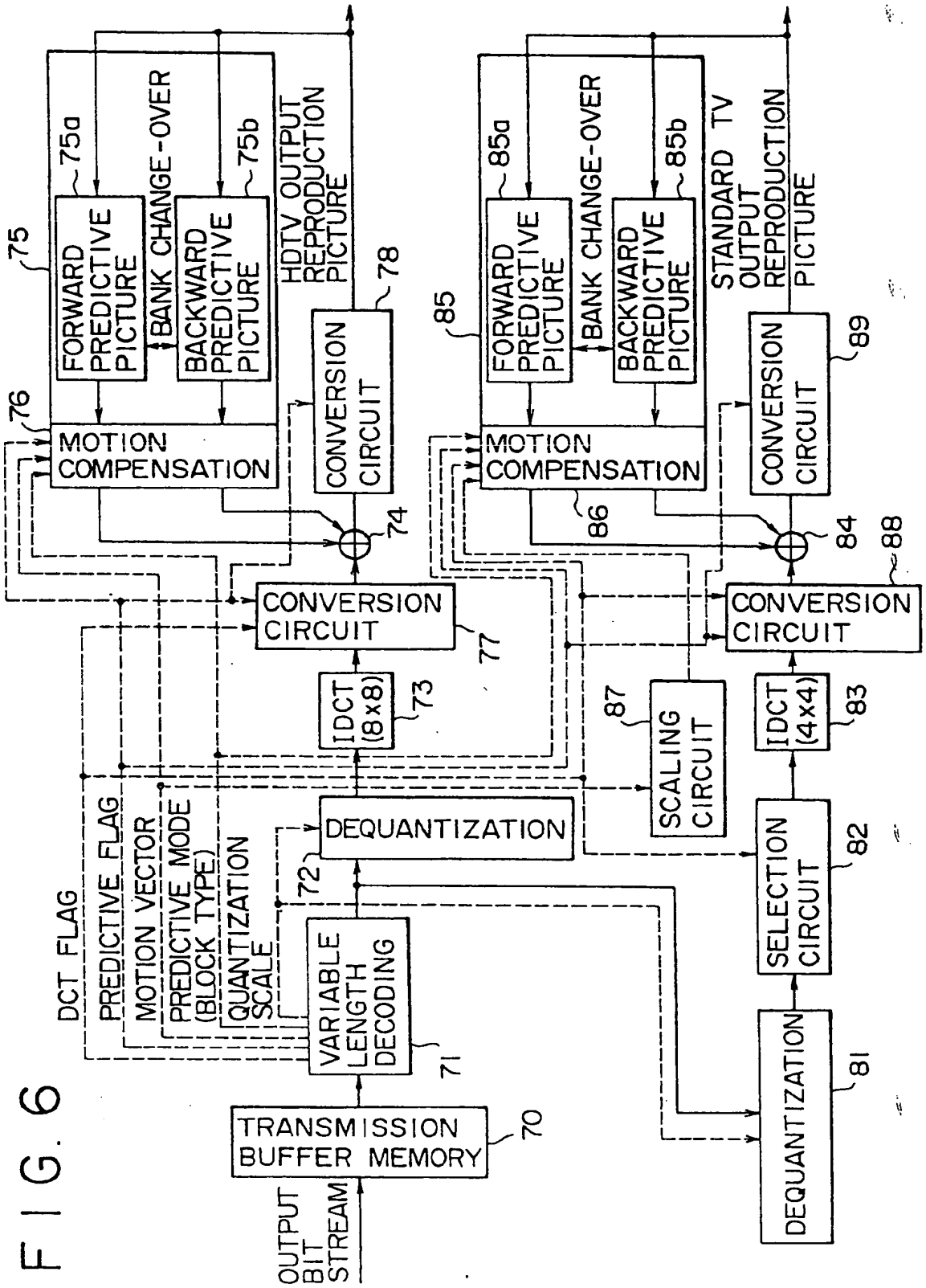
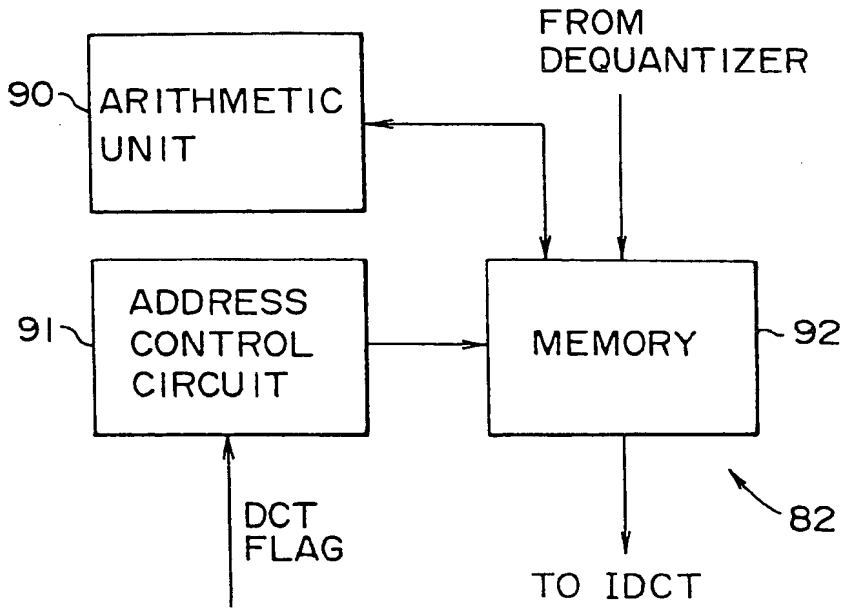


FIG. 6

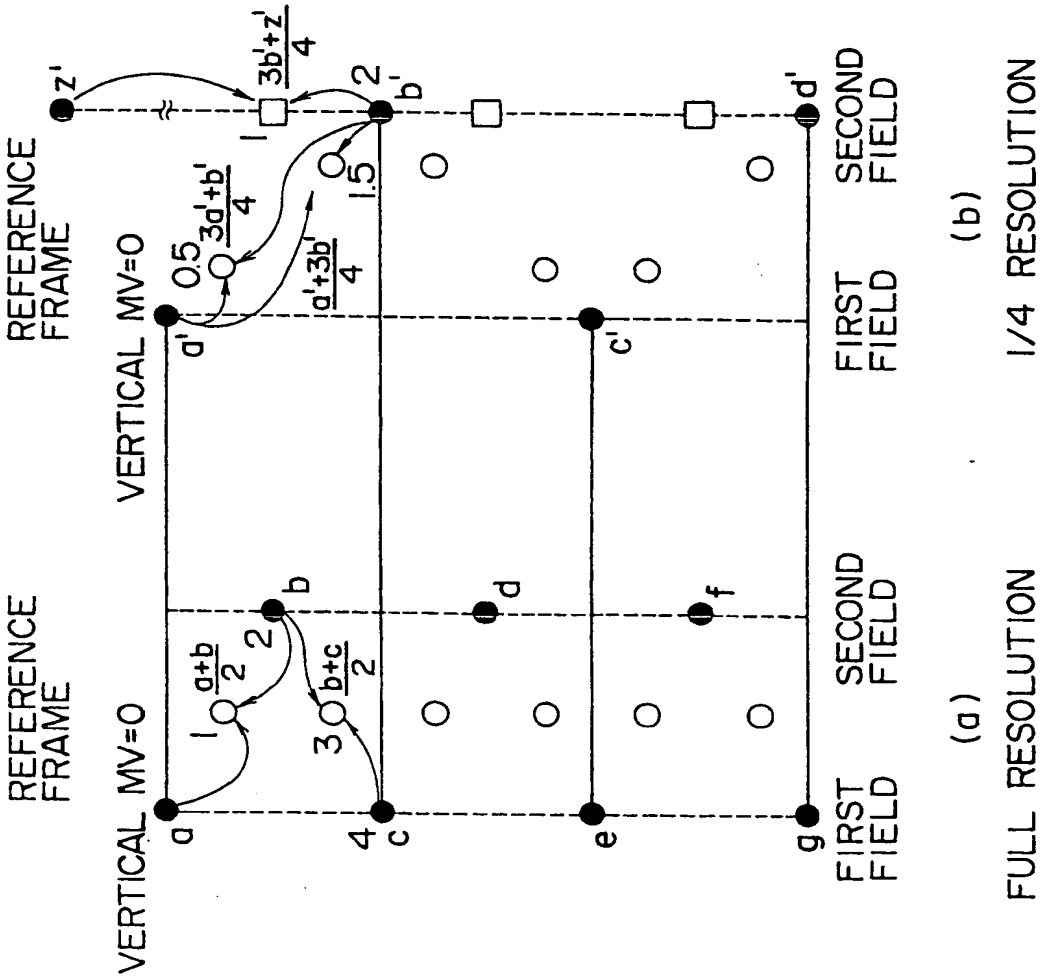
Nokia Exhibit 2004, p. 242
Amazon.com v. Nokia
IPR2024-01141

FIG. 7



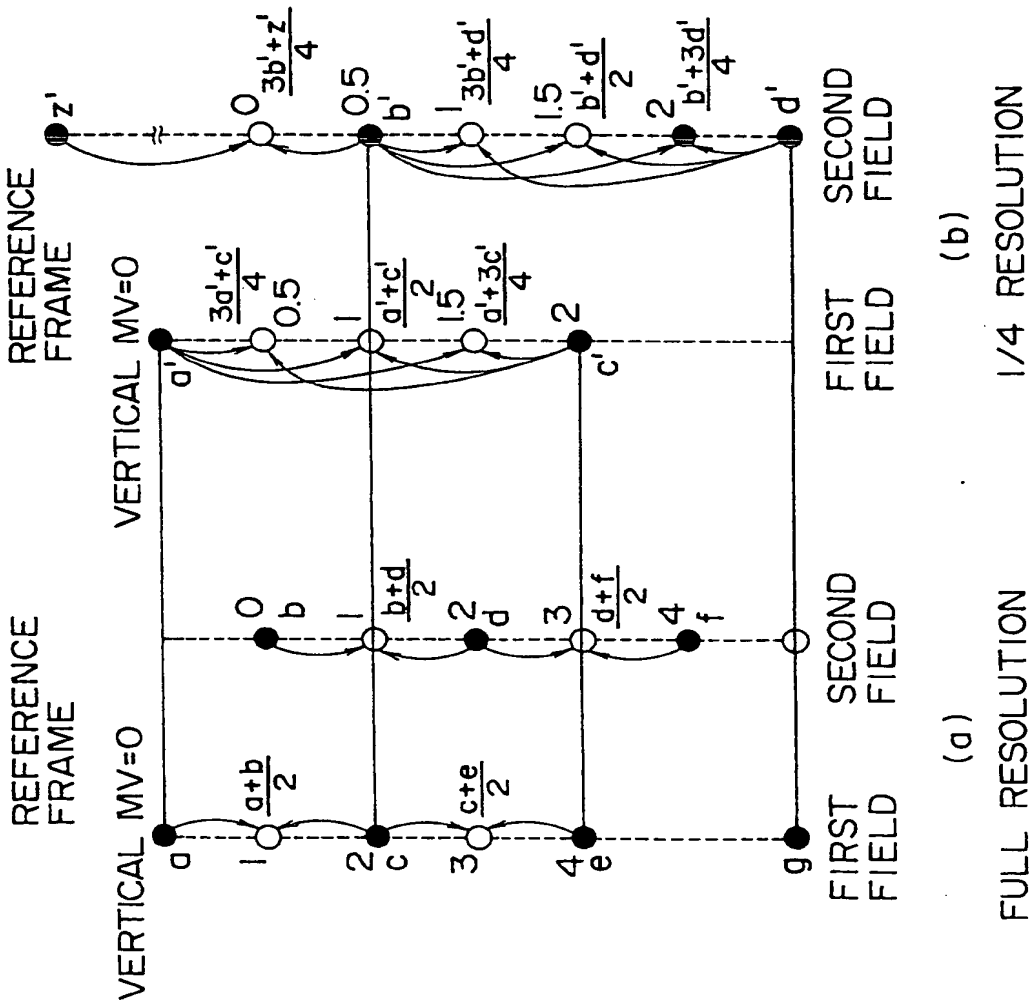
Nokia Exhibit 2004, p. 243
Amazon.com v. Nokia
IPR2024-01141

FIG. 8



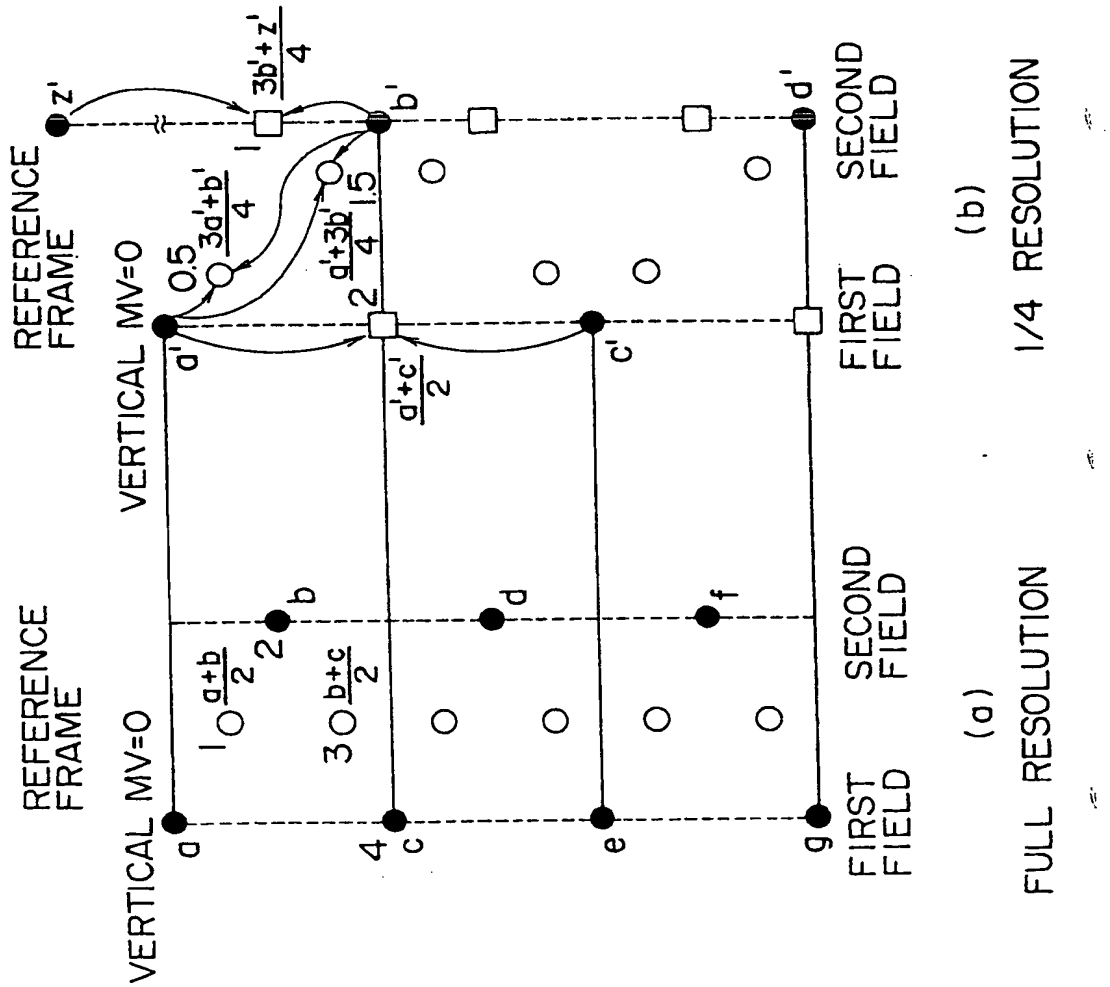
Nokia Exhibit 2004, p. 244
Amazon.com v. Nokia
IPR2024-01141

FIG. 9



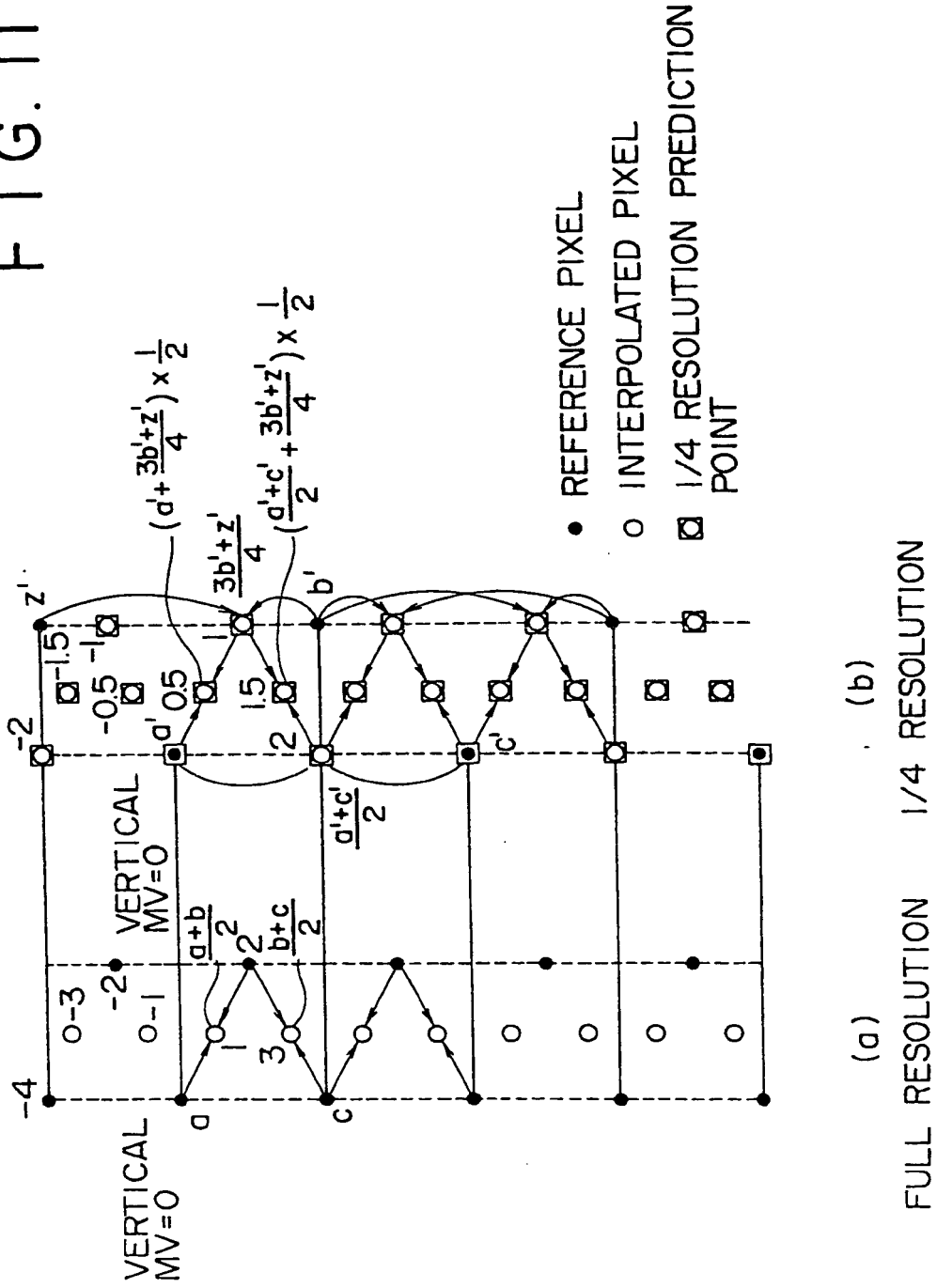
Nokia Exhibit 2004, p. 245
Amazon.com v. Nokia
IPR2024-01141

FIG. 10



Nokia Exhibit 2004, p. 246
Amazon.com v. Nokia
IPR2024-01141

FIG. 11



Nokia Exhibit 2004, p. 247
Amazon.com v. Nokia
IPR2024-01141

FIG. 12

d(0,0)	d(0,1)	d(0,2)	d(0,3)
d(1,0)	d(1,1)	d(1,2)	d(1,3)
d(2,0)	d(2,1)	d(2,2)	d(2,3)
d(3,0)	d(3,1)	d(3,2)	d(3,3)

FIG. 13

d(0,0)	d(0,1)	d(0,2)	d(0,3)
d(1,0)	d(1,1)	d(1,2)	d(1,3)
d(2,0)	d(2,1)	d(2,2)	d(2,3)
d(3,0) + d(7,0)	d(3,1) + d(7,1)	d(3,2) + d(7,2)	d(3,3) + d(7,3)

Nokia Exhibit 2004, p. 248
Amazon.com v. Nokia
IPR2024-01141

FIG. 14

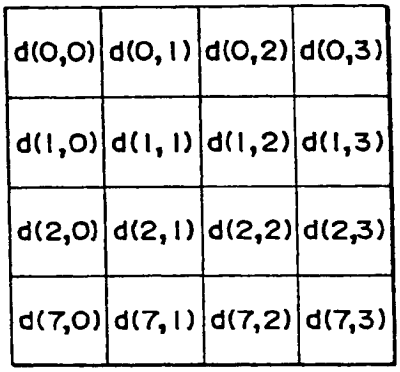
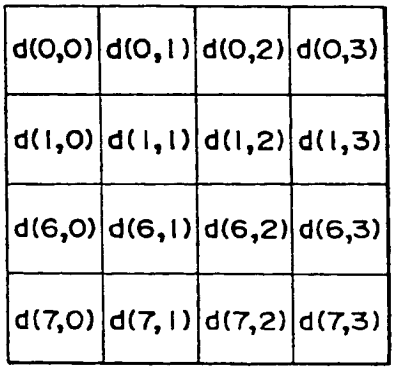


FIG. 15



Nokia Exhibit 2004, p. 249
Amazon.com v. Nokia
IPR2024-01141

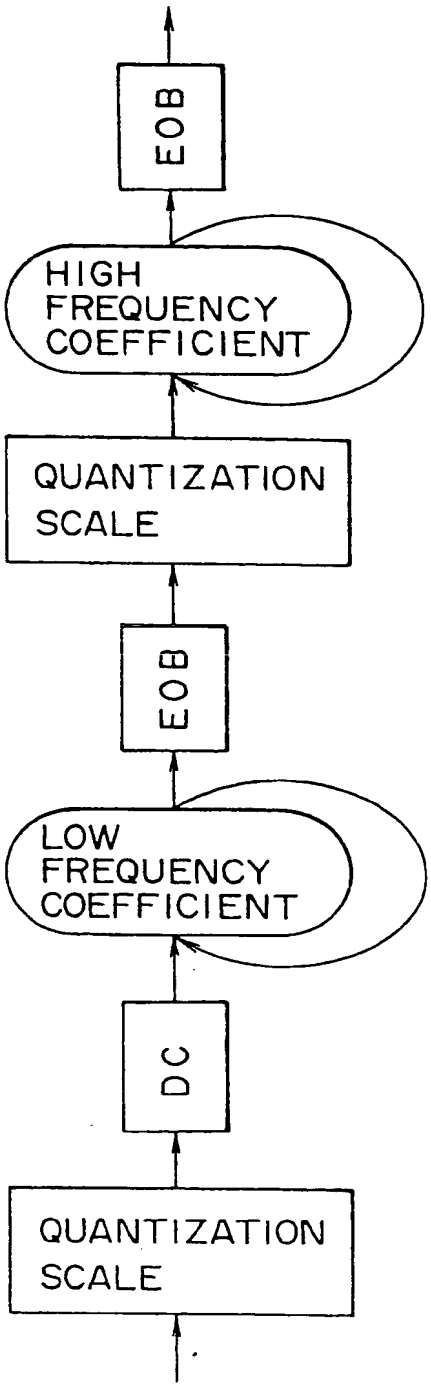
FIG. 16

1	2	6	7	26	27	35	36
3	5	8	13	28	34	37	46
4	9	12	14	33	38	45	47
10	11	15	16	39	44	48	54
25	29	32	40	43	49	53	55
30	31	41	42	50	52	56	61
21	22	23	24	51	57	60	62
17	18	19	20	58	59	63	64

ZIGZAG SCAN

Nokia Exhibit 2004, p. 250
Amazon.com v. Nokia
IPR2024-01141

FIG. 17



Nokia Exhibit 2004, p. 251
Amazon.com v. Nokia
IPR2024-01141

FIG. 18(A)

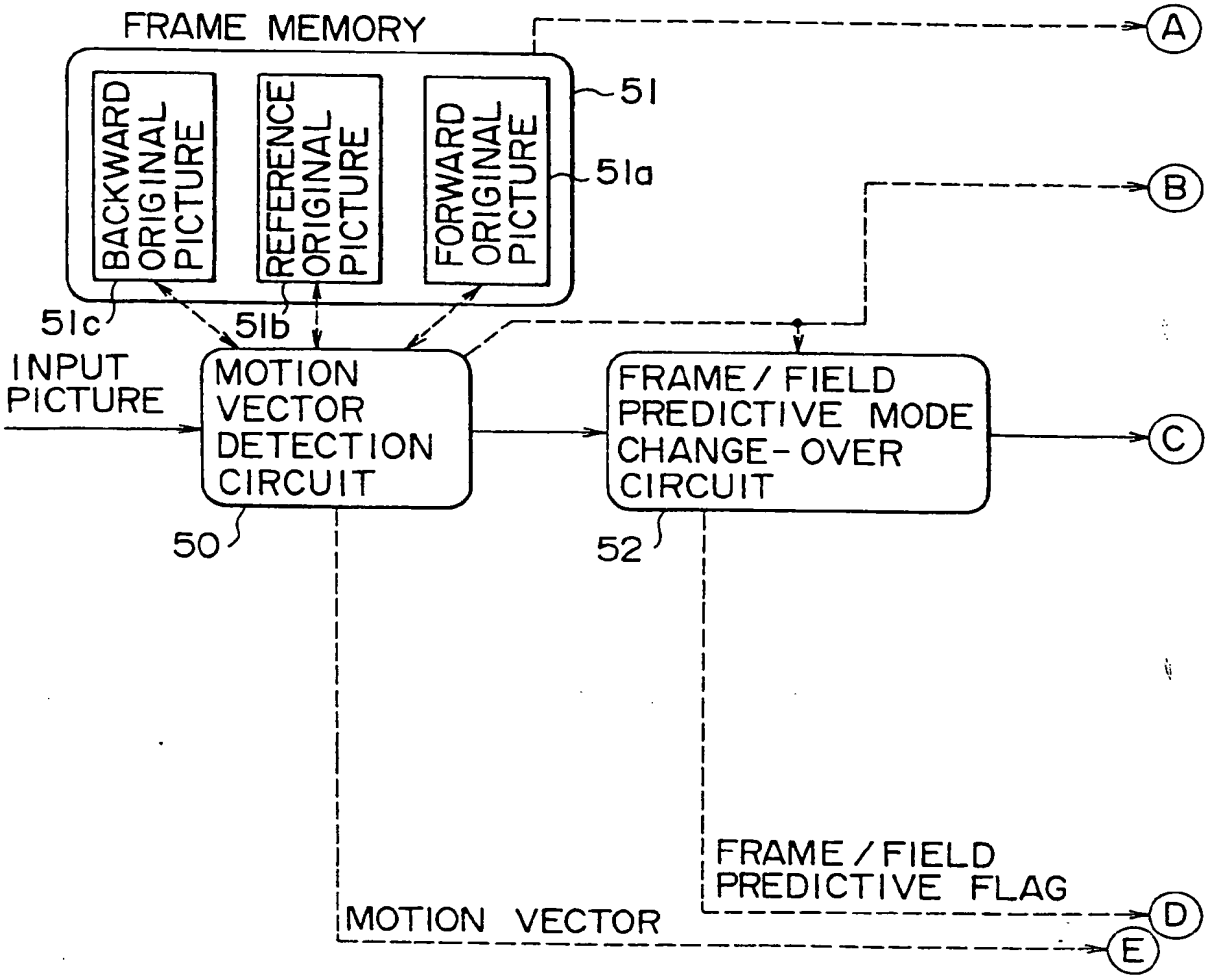
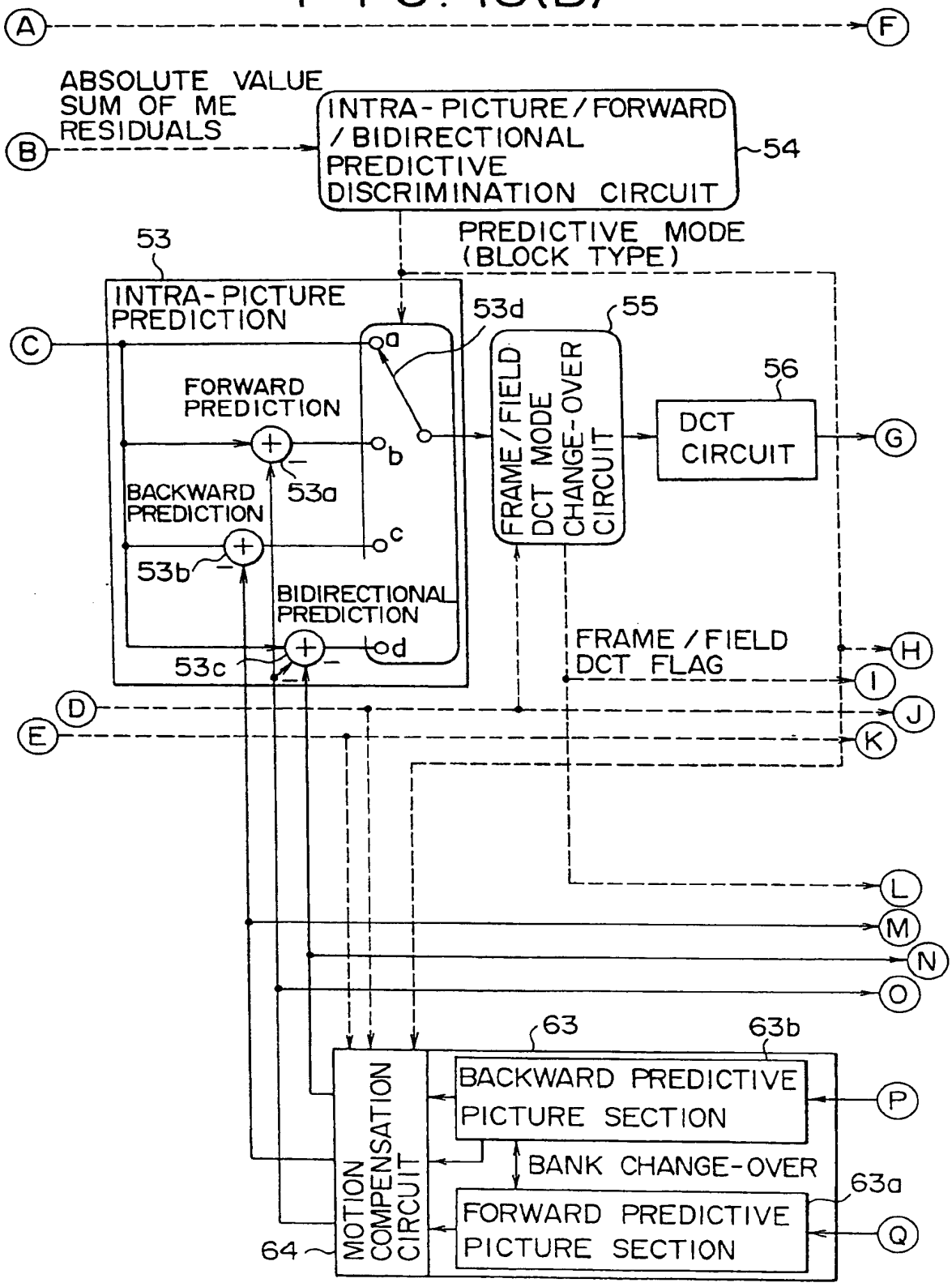


FIG. 18

FIG.18(A)	FIG.18(B)	FIG.18(C)

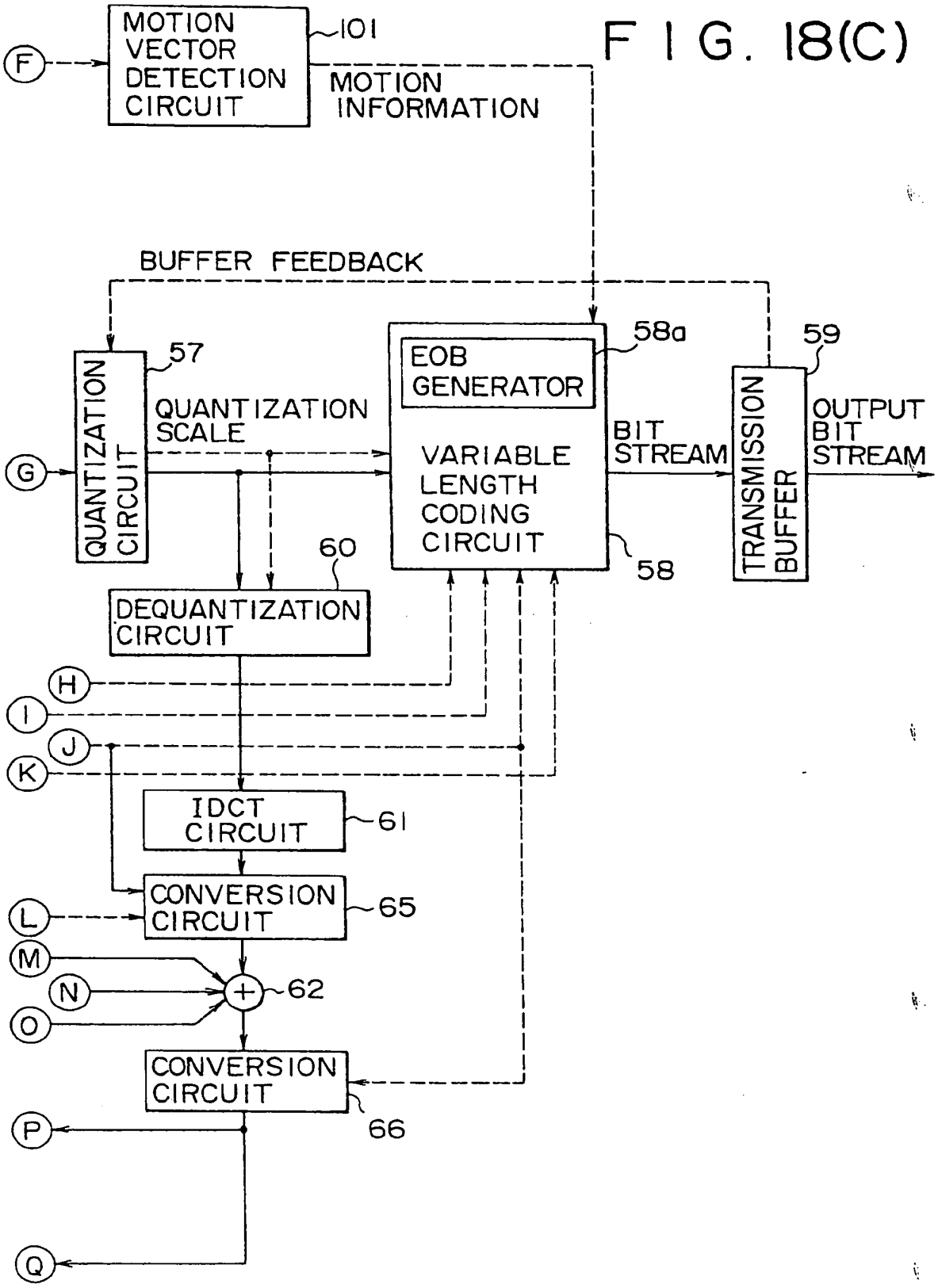
Nokia Exhibit 2004, p. 252
Amazon.com v. Nokia
IPR2024-01141

FIG. 18(B)



Nokia Exhibit 2004, p. 253
Amazon.com v. Nokia
IPR2024-01141

FIG. 18(C)



Nokia Exhibit 2004, p. 254
Amazon.com v. Nokia
IPR2024-01141

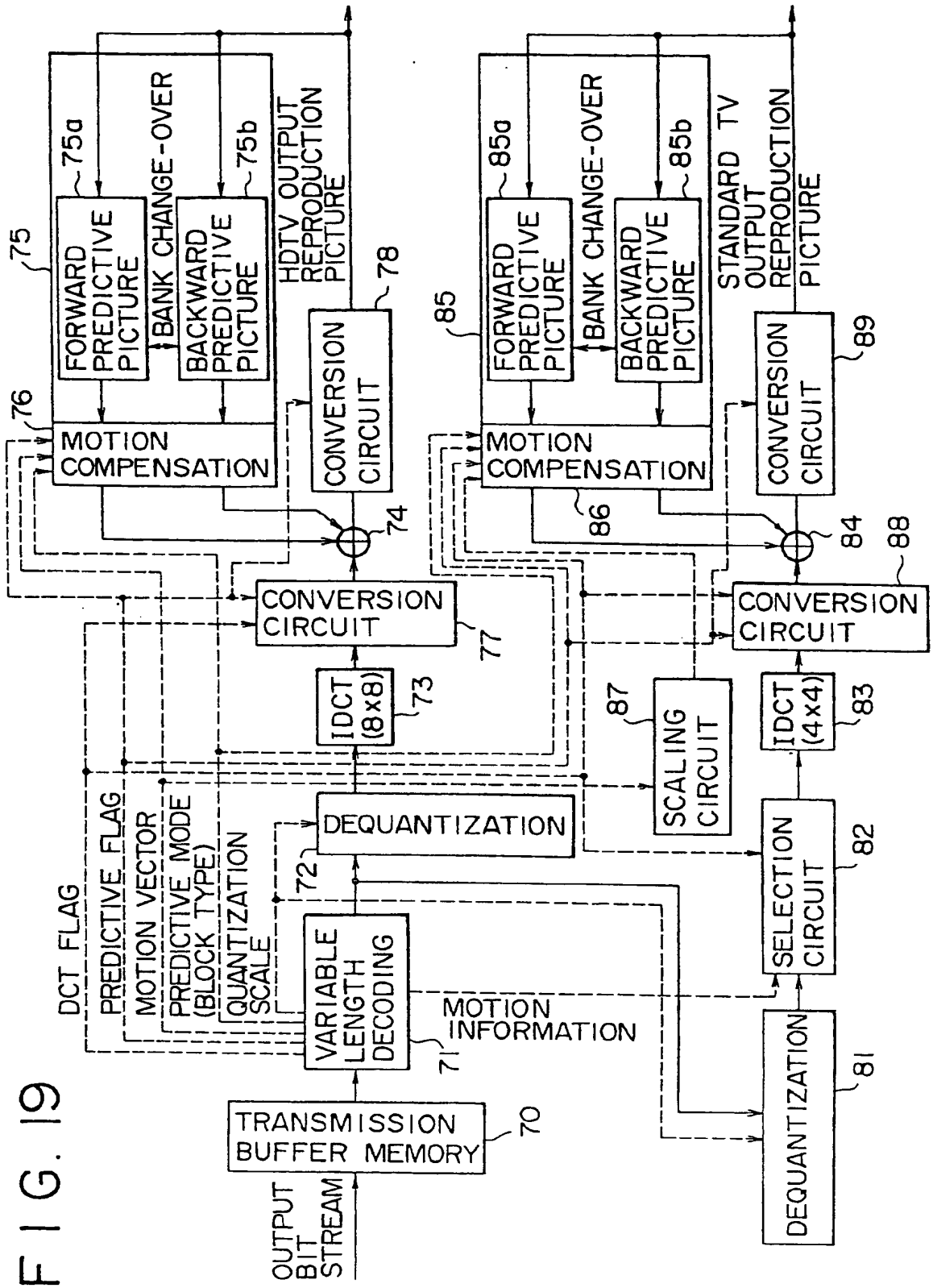
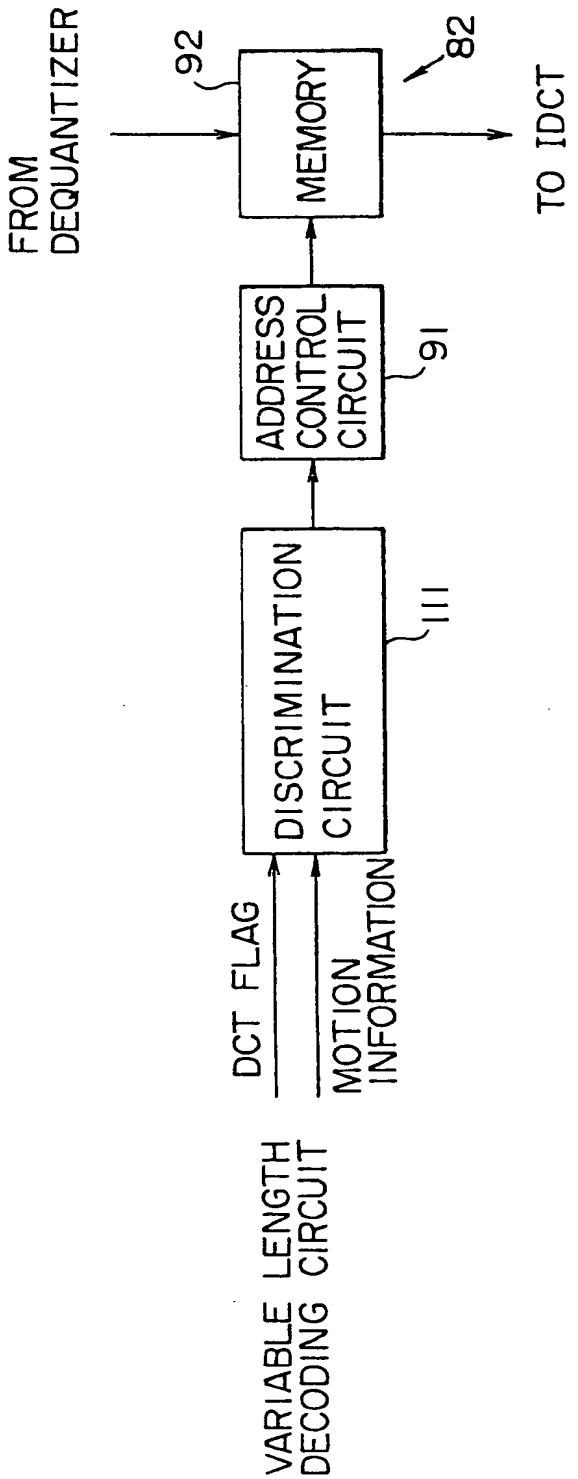


FIG. 19

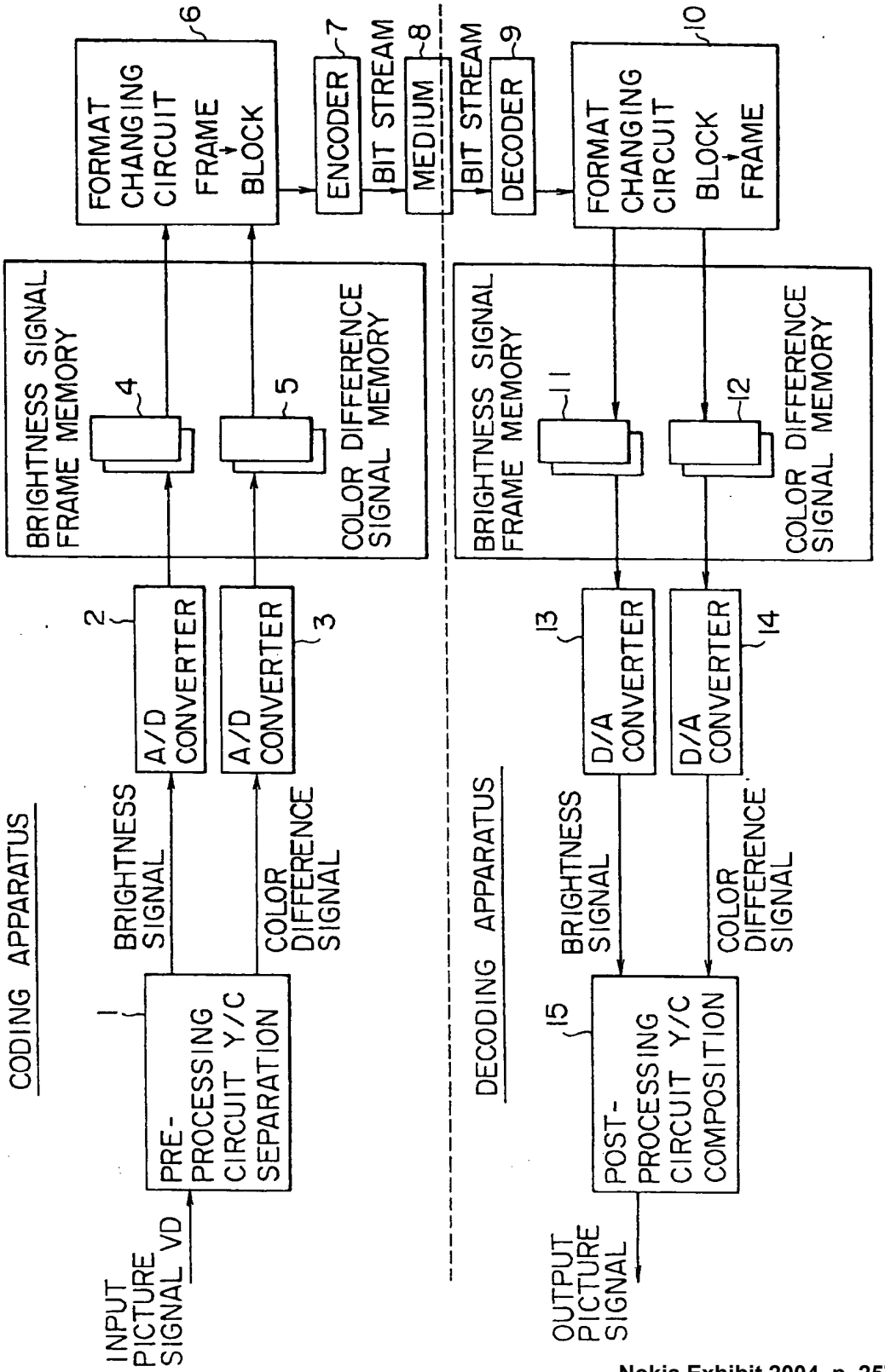
Nokia Exhibit 2004, p. 255
Amazon.com v. Nokia
IPR2024-01141

FIG. 20



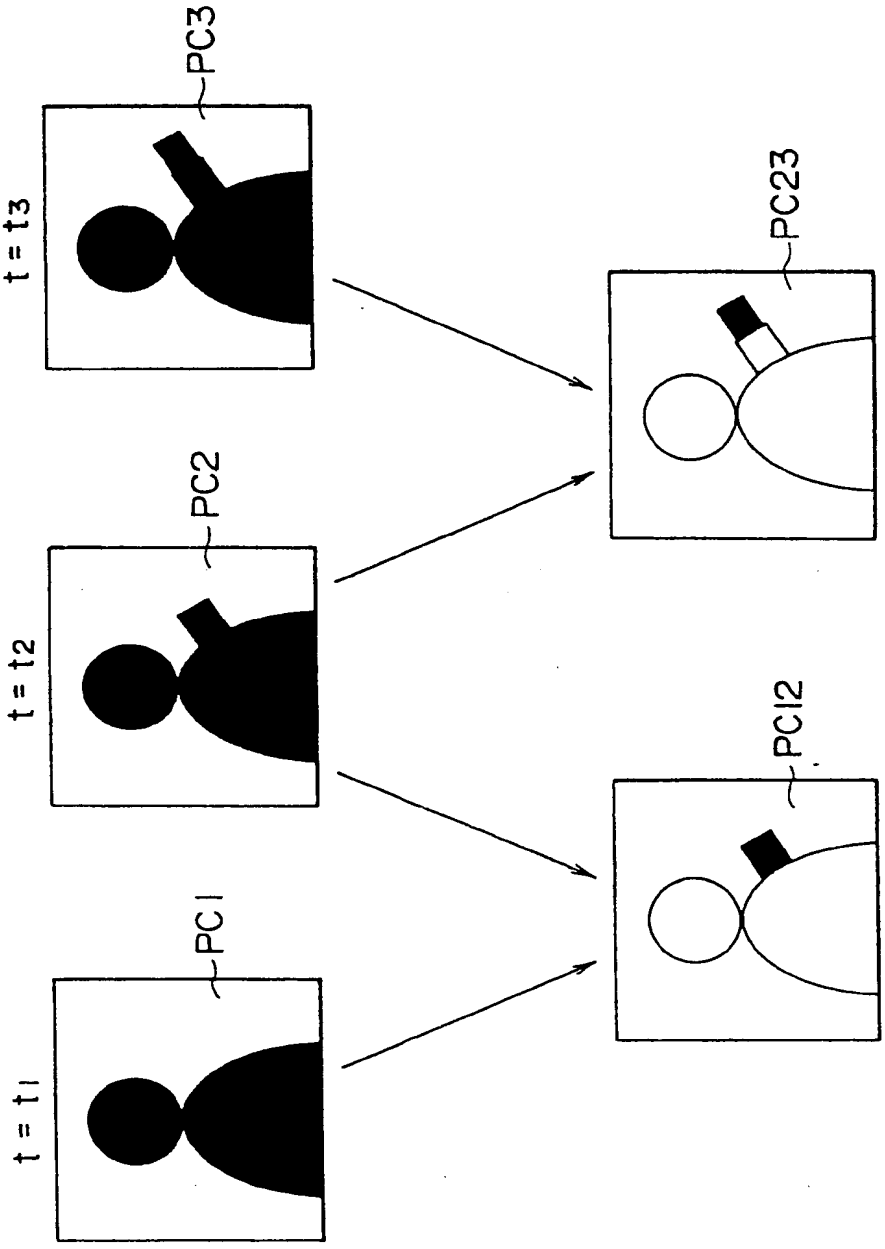
Nokia Exhibit 2004, p. 256
Amazon.com v. Nokia
IPR2024-01141

FIG. 21



Nokia Exhibit 2004, p. 257
Amazon.com v. Nokia
IPR2024-01141

FIG. 22



Nokia Exhibit 2004, p. 258
Amazon.com v. Nokia
IPR2024-01141

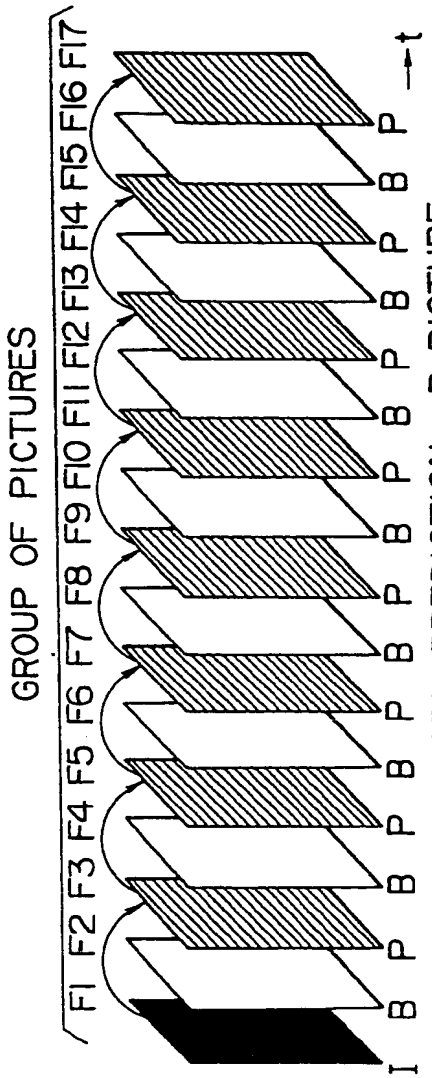


FIG. 23(A)

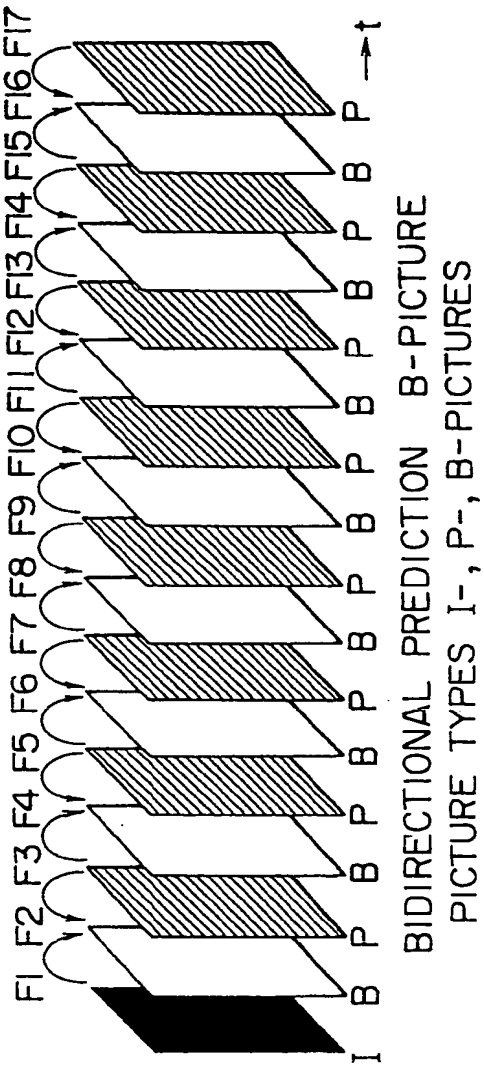


FIG. 23(B)

Nokia Exhibit 2004, p. 259
Amazon.com v. Nokia
IPR2024-01141

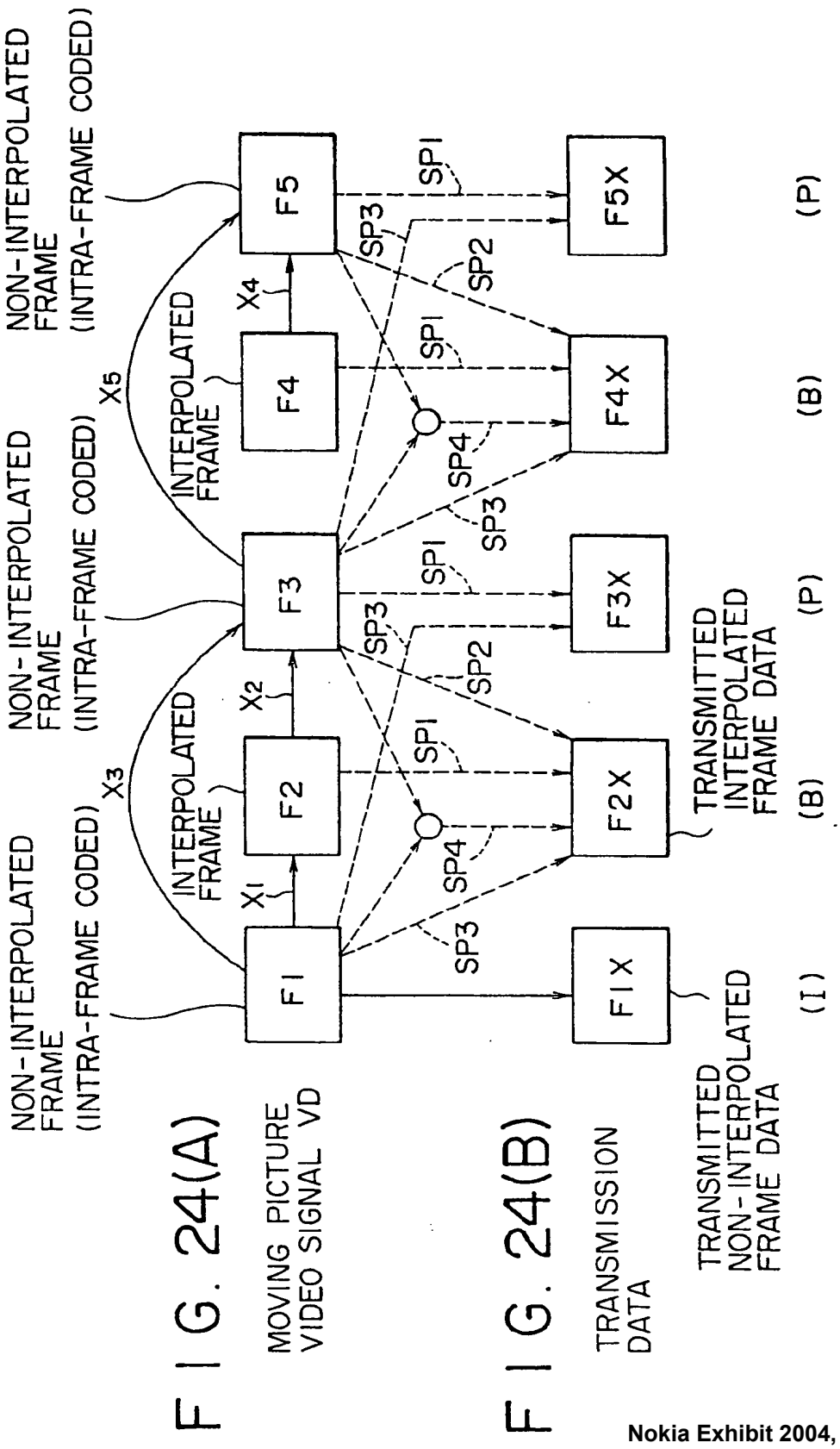
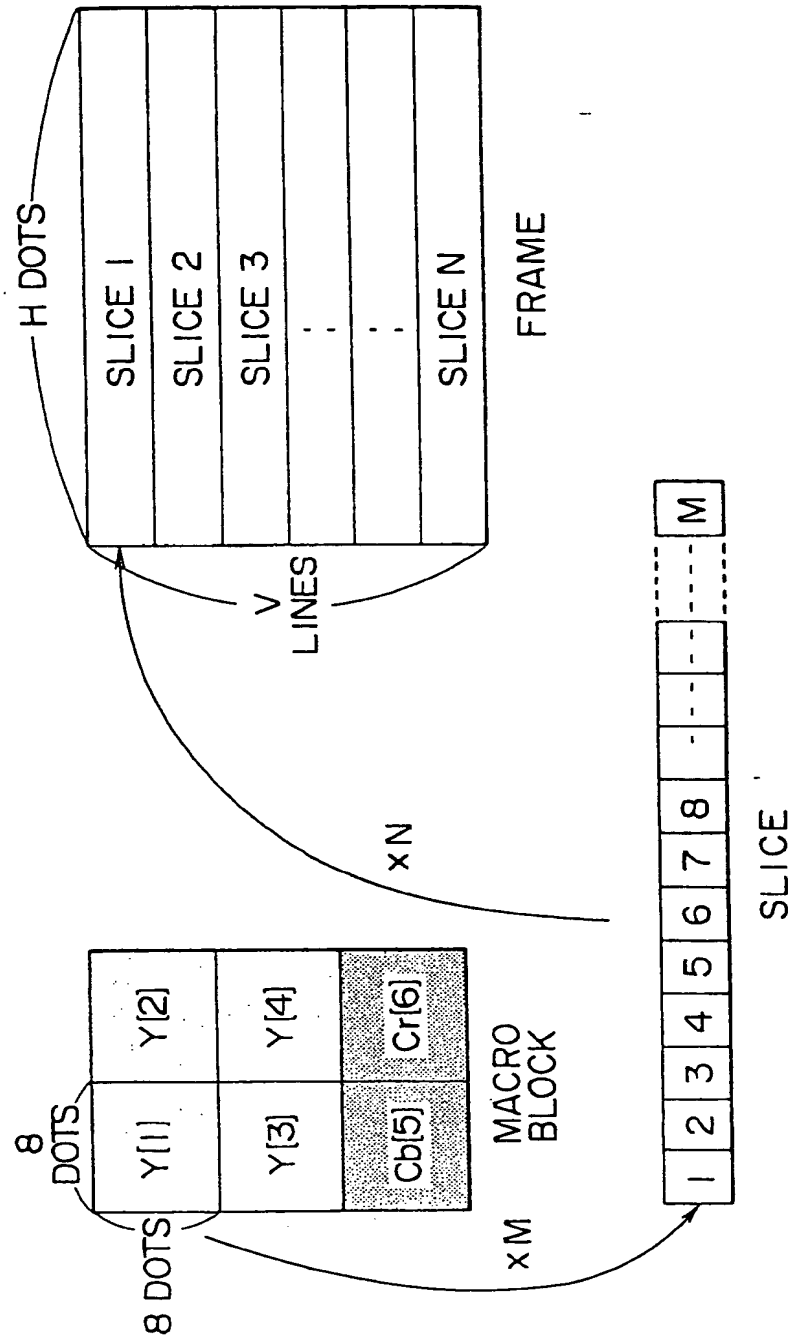


FIG. 24(A)

FIG. 24(B)

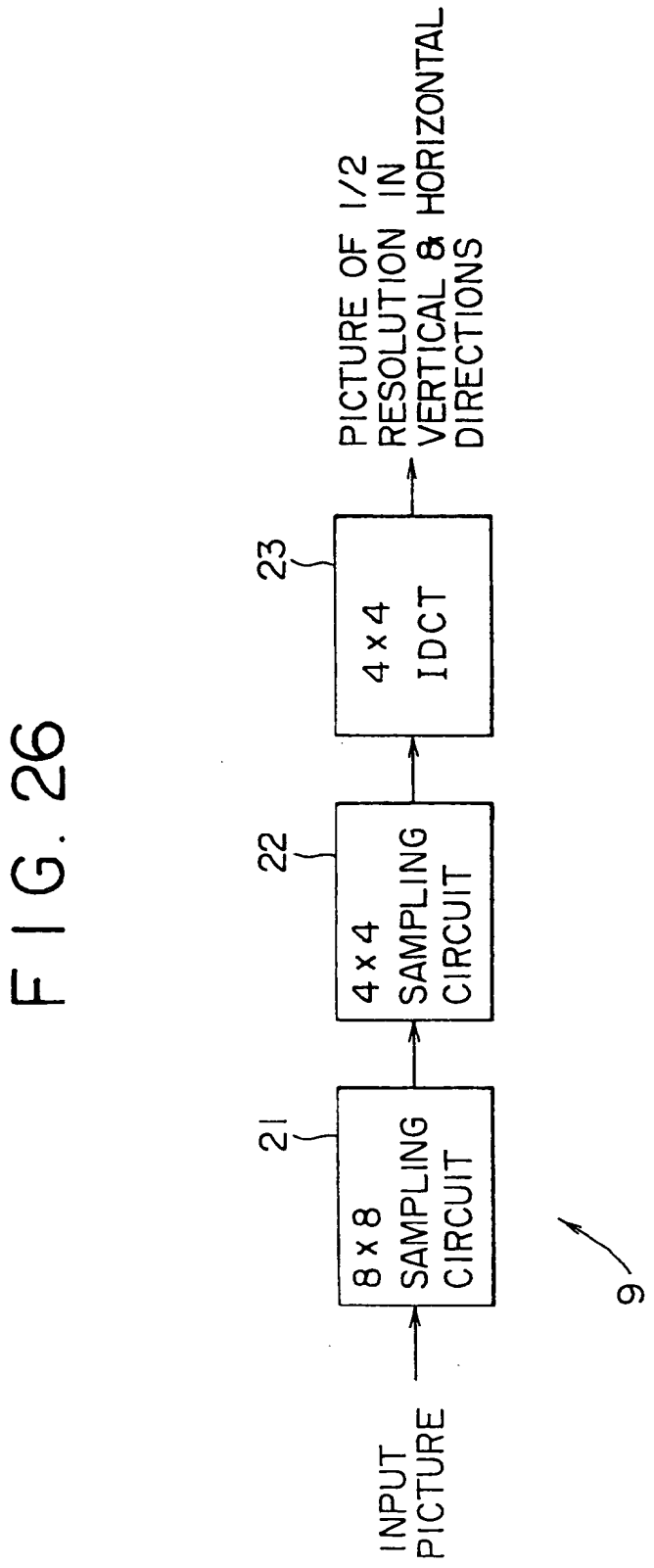
Nokia Exhibit 2004, p. 260
Amazon.com v. Nokia
IPR2024-01141

FIG. 25



Nokia Exhibit 2004, p. 261
Amazon.com v. Nokia
IPR2024-01141

FIG. 26



Nokia Exhibit 2004, p. 262
Amazon.com v. Nokia
IPR2024-01141

FIG. 27

d(0,0)	d(0,1)	d(0,2)	d(0,3)	d(0,4)	d(0,5)	d(0,6)	d(0,7)
d(1,0)	d(1,1)	d(1,2)	d(1,3)	d(1,4)	d(1,5)	d(1,6)	d(1,7)
d(2,0)	d(2,1)	d(2,2)	d(2,3)	d(2,4)	d(2,5)	d(2,6)	d(2,7)
d(3,0)	d(3,1)	d(3,2)	d(3,3)	d(3,4)	d(3,5)	d(3,6)	d(3,7)
d(4,0)	d(4,1)	d(4,2)	d(4,3)	d(4,4)	d(4,5)	d(4,6)	d(4,7)
d(5,0)	d(5,1)	d(5,2)	d(5,3)	d(5,4)	d(5,5)	d(5,6)	d(5,7)
d(6,0)	d(6,1)	d(6,2)	d(6,3)	d(6,4)	d(6,5)	d(6,6)	d(6,7)
d(7,0)	d(7,1)	d(7,2)	d(7,3)	d(7,4)	d(7,5)	d(7,6)	d(7,7)

FIG. 28

d(0,0)	d(0,1)	d(0,2)	d(0,3)
d(1,0)	d(1,1)	d(1,2)	d(1,3)
d(2,0)	d(2,1)	d(2,2)	d(2,3)
d(3,0)	d(3,1)	d(3,2)	d(3,3)

Nokia Exhibit 2004, p. 263
Amazon.com v. Nokia
IPR2024-01141

(12) UK Patent Application (19) GB (11) 2 205 707 (13) A

(43) Application published 14 Dec 1988

(21) Application No 8728446

(22) Date of filing 4 Dec 1987

(30) Priority data
(31) 8713454 (32) 9 Jun 1987 (33) GB

(71) Applicant
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(Incorporated in Japan)

6-7-35 Kitashinagawa, Shinagawa-ku, Tokyo 141, Japan

(72) Inventor
Clive Henrry Gillard

(74) Agent and/or Address for service:
D. Young & Co
10 Staple Inn, London, WC1V 7RD

(51) INT CL⁴
H04N 7/01 5/14 5/76

(52) Domestic classification (Edition J):
H4F D10 D12M D12X D1B1 D1D1 D1K1 D30K D30T1 D30T2 D30T3 D30X D54 EP

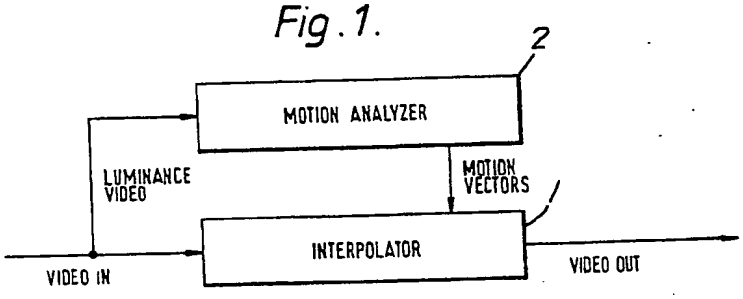
(56) Documents cited
GB A 2188510 GB A 2172171 GB A 2162018
GB A 2129651 EP A2 0210862 EP A1 0187641
WO A1 85/02080

(58) Field of search
H4F
Selected US specifications from IPC sub-class H04N

(54) Television standards converters

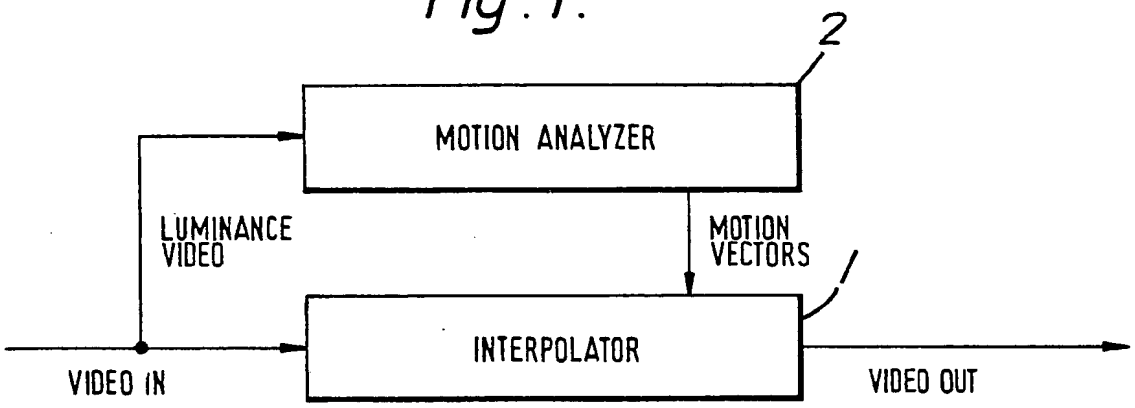
(57) A television standards converter comprises a motion analyzer 2 for analyzing the motion between consecutive fields of an input television signal of one television standard, and an interpolator 1 operative to align the fields pixel by pixel in dependence on the analyzed motion so as effectively to represent static pictures, and to effect conversion using said static pictures to derive the required output television signal of a different television standard. A slow motion processor using basically the same circuitry operates in a similar way.

Fig.1.



Nokia Exhibit 2004, p. 264
Amazon.com v. Nokia
IPR2024-01141

Fig. 1.



Nokia Exhibit 2004, p. 265
Amazon.com v. Nokia
IPR2024-01141

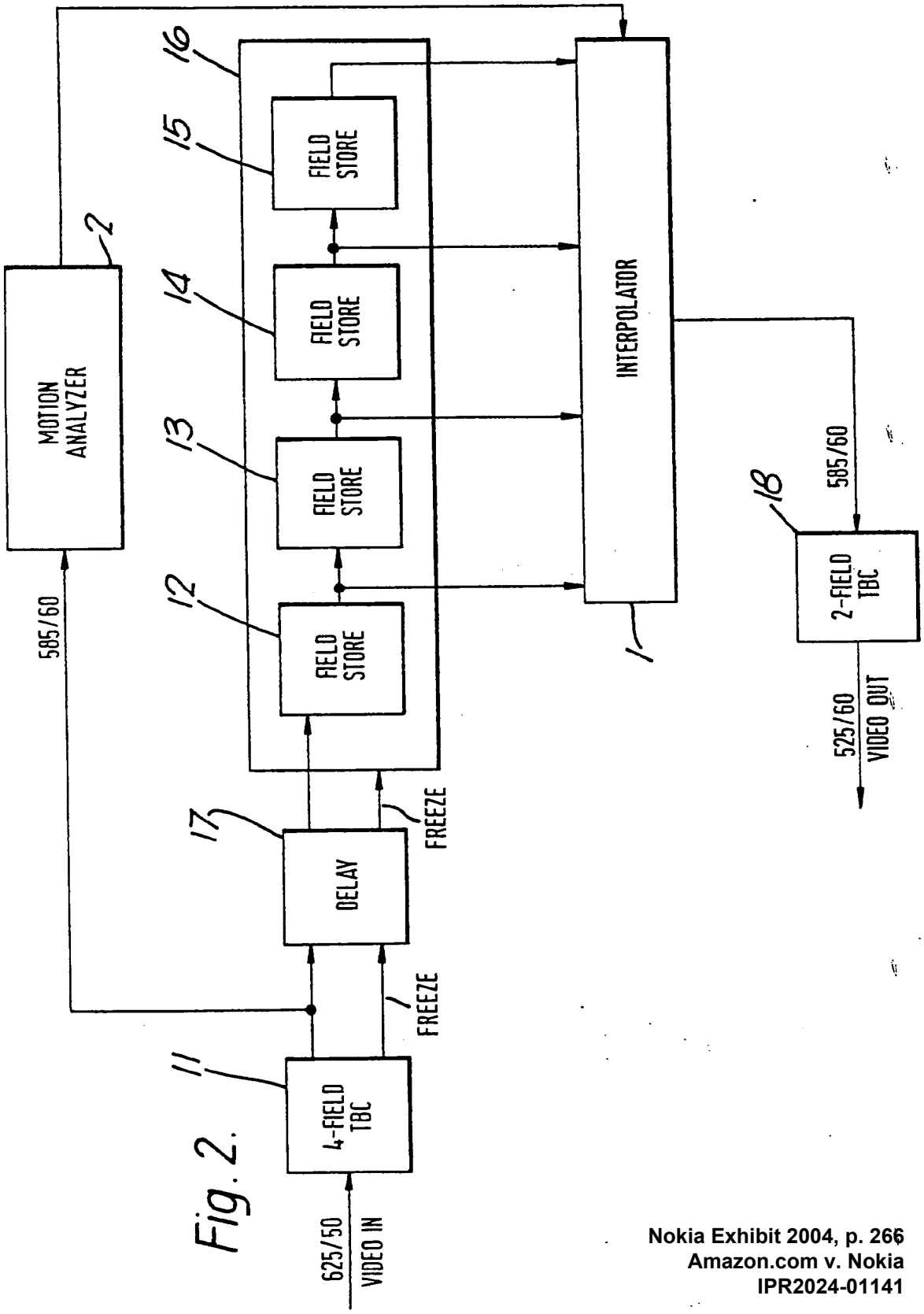


Fig. 2.

Nokia Exhibit 2004, p. 266
Amazon.com v. Nokia
IPR2024-01141

2205707

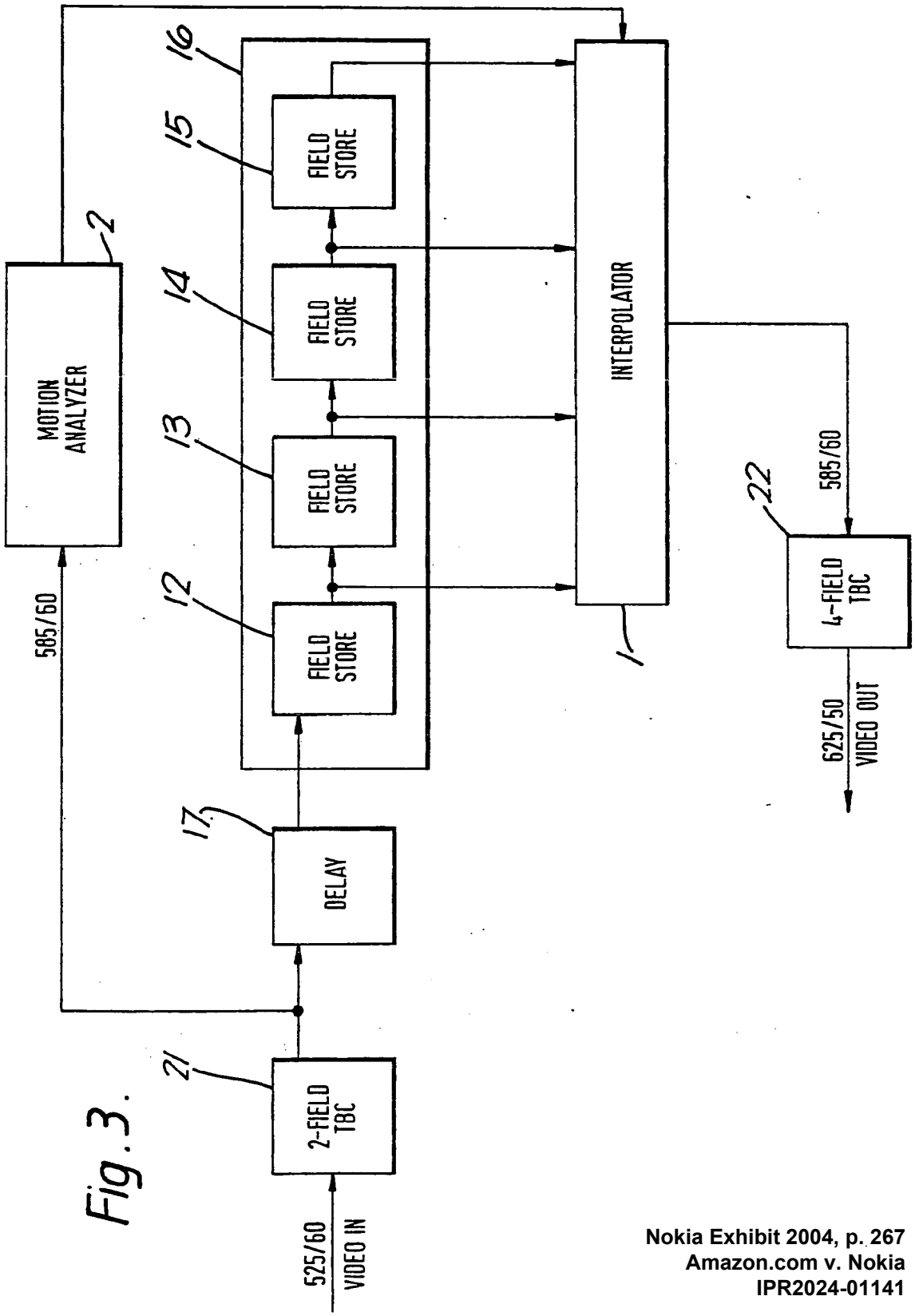
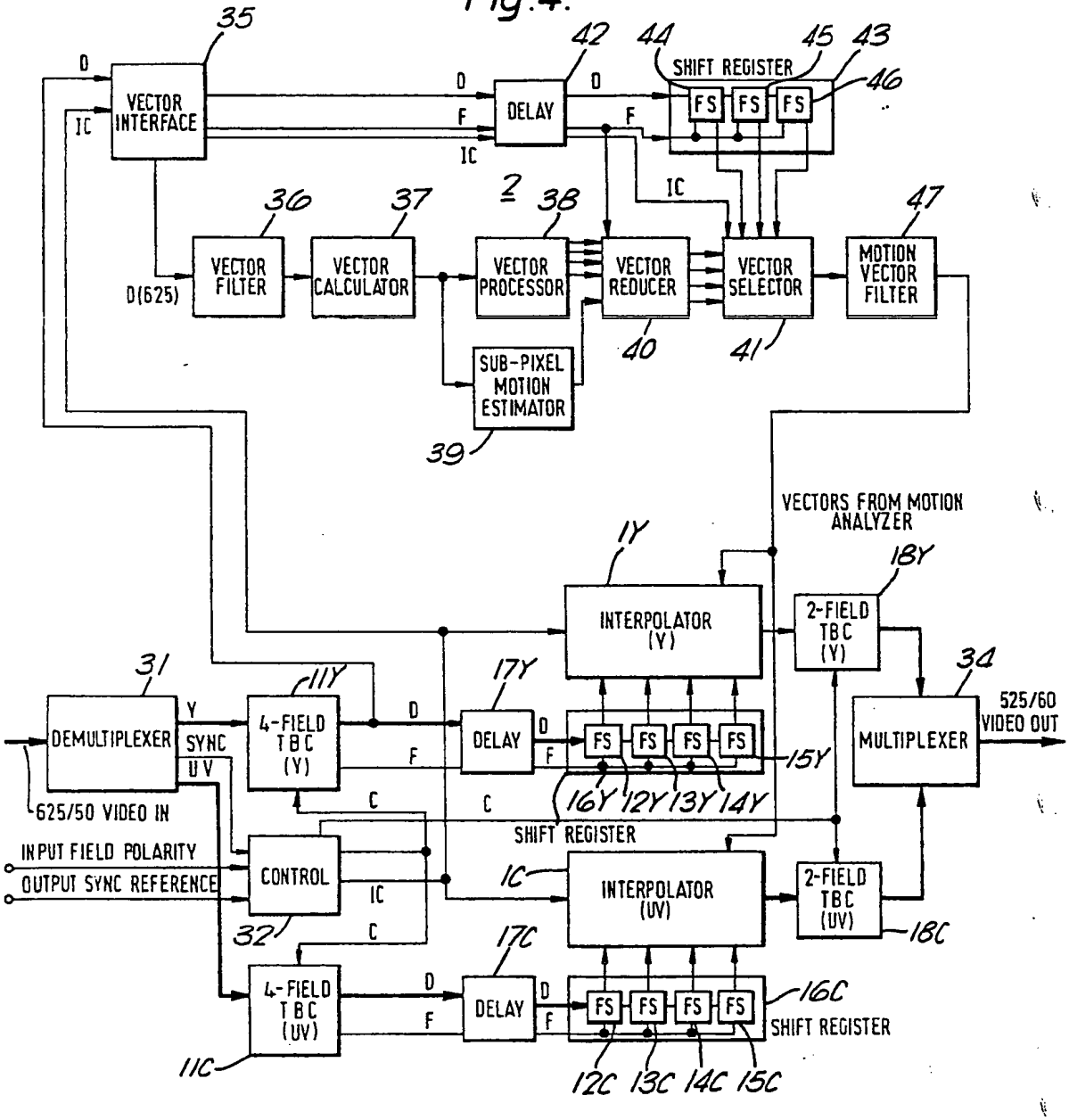


Fig. 3.

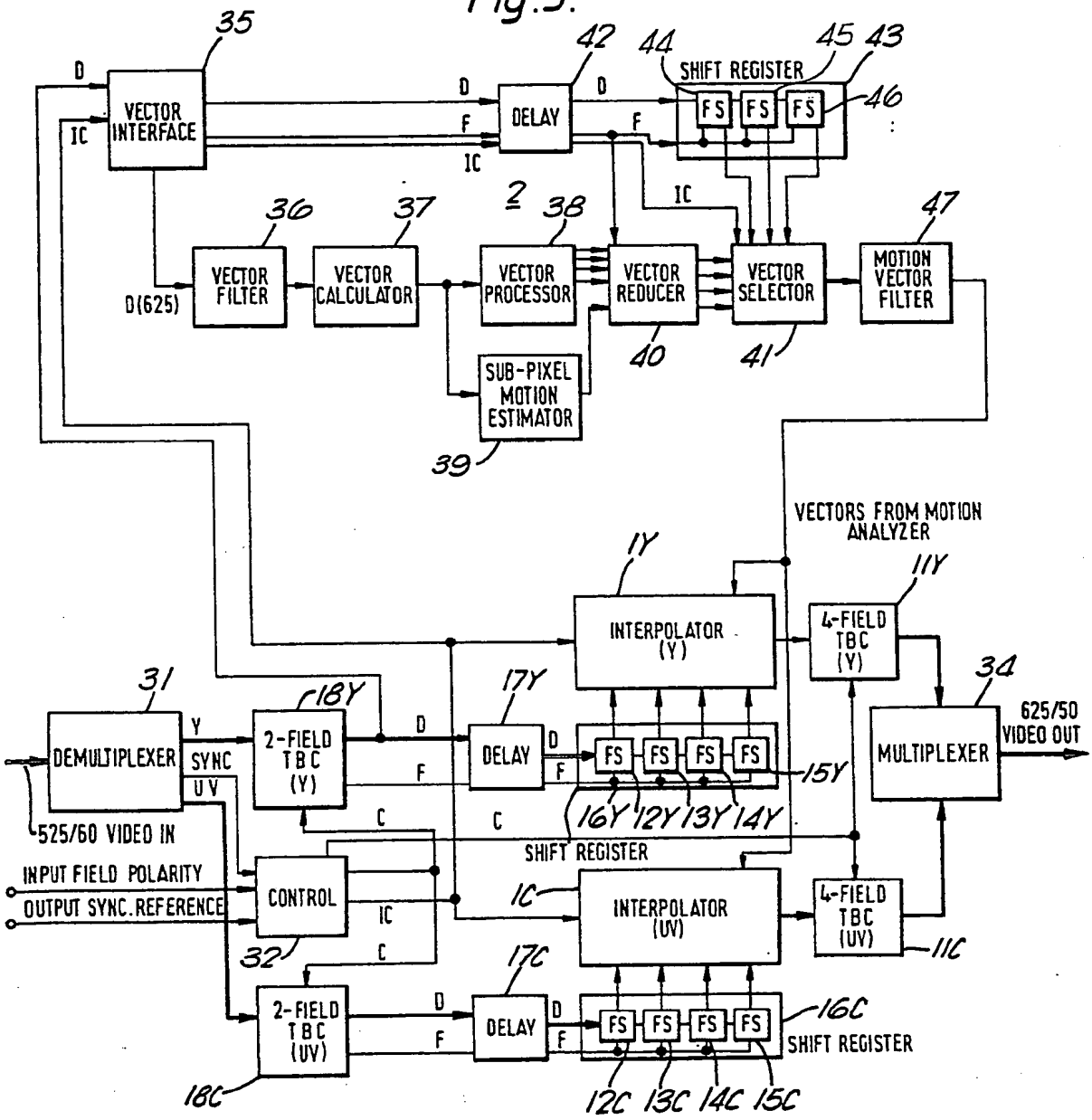
Nokia Exhibit 2004, p. 267
Amazon.com v. Nokia
IPR2024-01141

Fig.4.



Nokia Exhibit 2004, p. 268
Amazon.com v. Nokia
IPR2024-01141

Fig.5.



Nokia Exhibit 2004, p. 269
Amazon.com v. Nokia
IPR2024-01141

Fig.6.

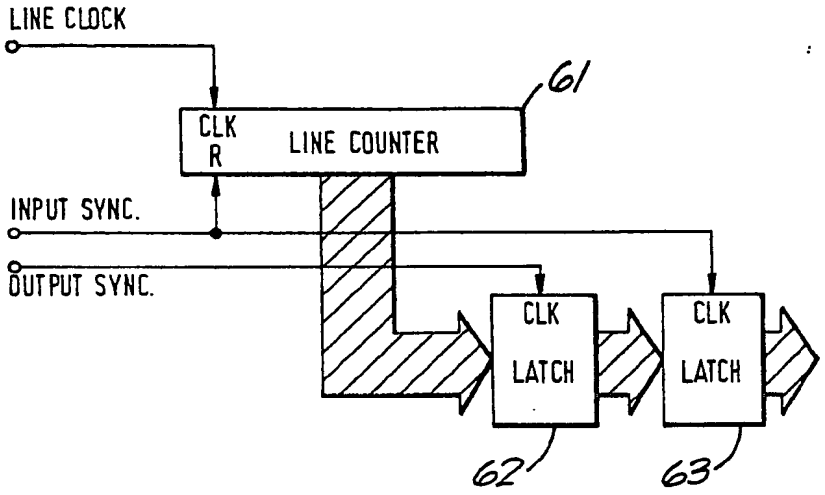


Fig.7A.

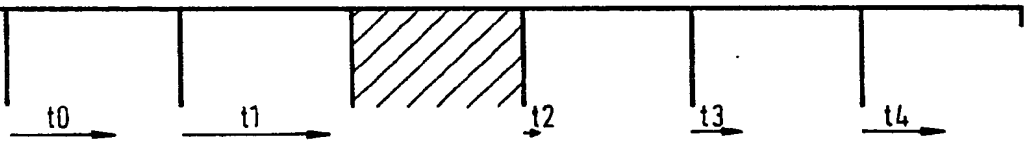


Fig.7B.



Fig.7C.



Fig.7D.

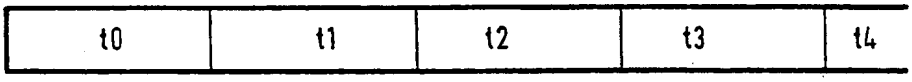
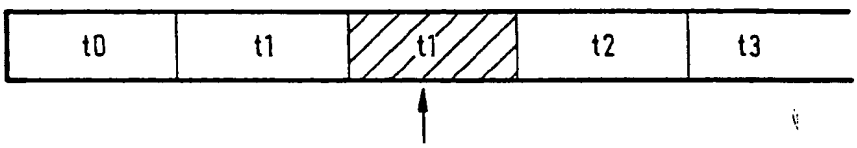


Fig.7E.



Nokia Exhibit 2004, p. 270
Amazon.com v. Nokia
IPR2024-01141

Fig. 8.

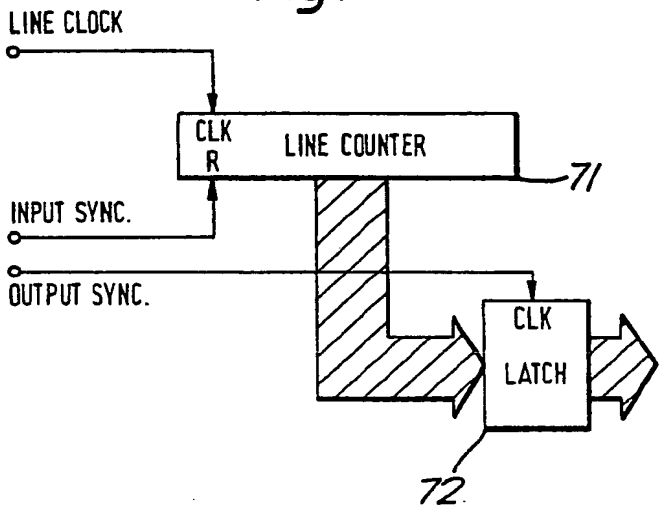


Fig. 9A.

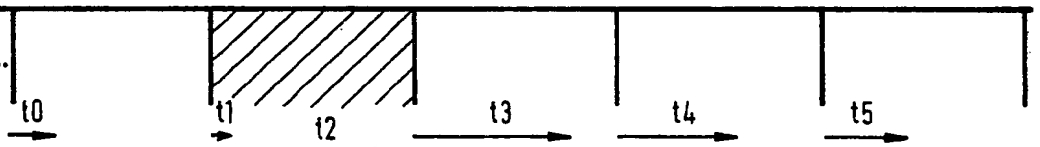


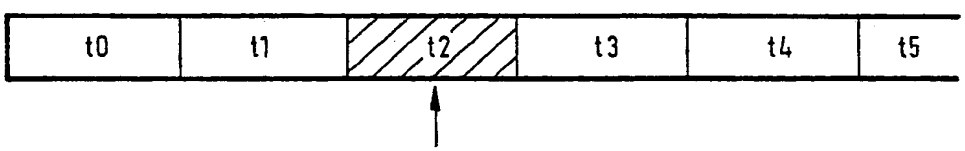
Fig. 9B.



Fig. 9C.

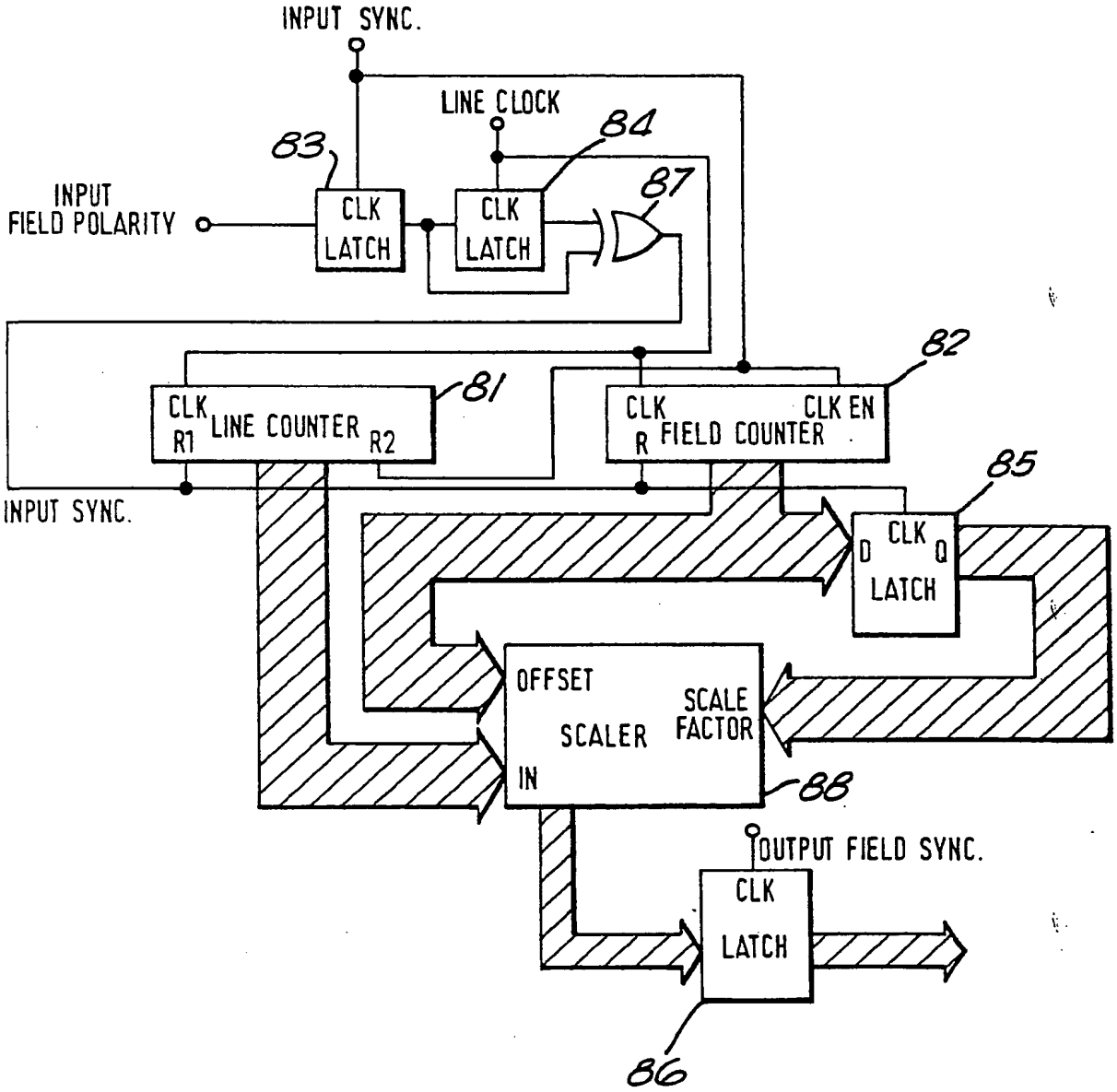


Fig. 9D.



Nokia Exhibit 2004, p. 271
Amazon.com v. Nokia
IPR2024-01141

Fig.10.



Nokia Exhibit 2004, p. 272
Amazon.com v. Nokia
IPR2024-01141

2205707

Fig.11A.

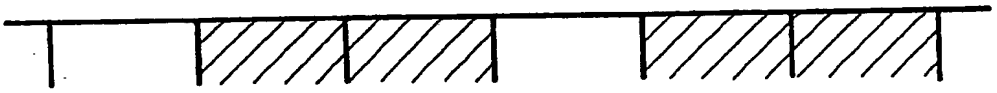


Fig.11B.



Fig.11C.

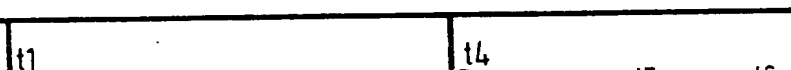


Fig.11D.

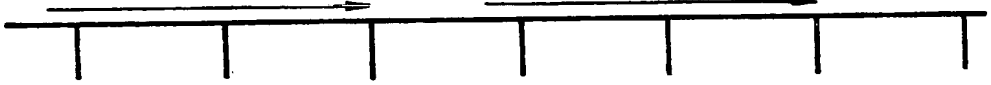


Fig.11E.

Fig.11F.

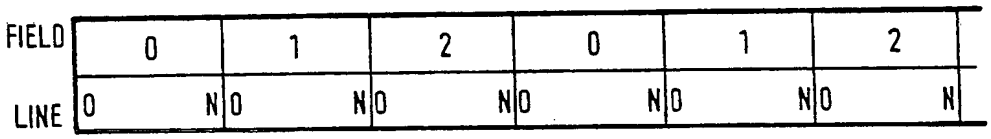


Fig.11G.

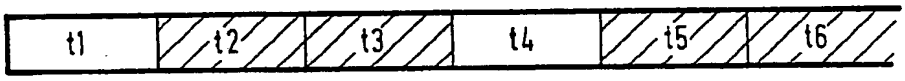
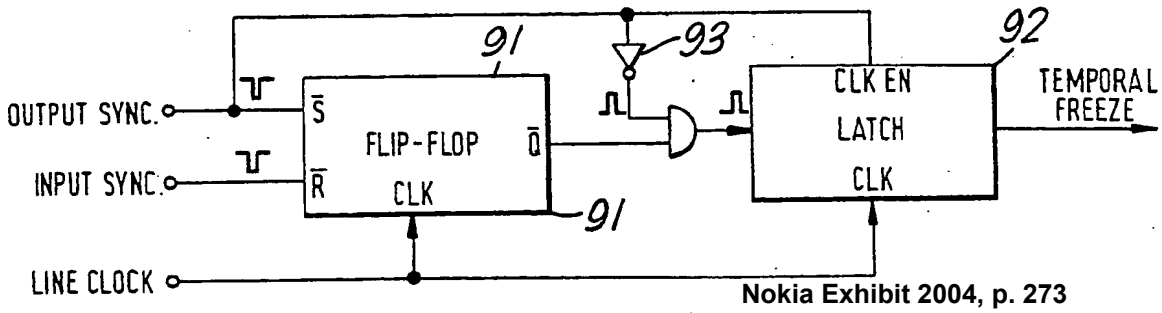


Fig.11H.



Fig.12.



Nokia Exhibit 2004, p. 273
Amazon.com v. Nokia
IPR2024-01141

TELEVISION STANDARDS CONVERTERS

This invention relates to television standards converters, and to slow motion processors.

International television programme exchange necessitates standards converters due to the different television standards used in different countries, for example, the 625-line 50-fields per second (625/50) PAL system used in the UK, and the 525-line 60-fields per second (525/60) NTSC system used in the USA.

Many different standards converters have been previously proposed. One of the best known is the ACE (Advanced Conversion Equipment) developed by the British Broadcasting Corporation. Basically ACE operates on an input digital television signal line-by-line to derive interpolated samples required to form an output digital television signal. Interpolation is done not only spatially using four successive horizontal scan lines of the input television signal, but also temporally using four successive fields of the input television signal. Thus, each line of the output television signal is derived by multiplying respective samples from sixteen lines of the input television signal by respective weighting coefficients.

Further details of ACE will be found in UK patent specification GB-A-2 059 712 and in 'Four-field digital standards converter for the eighties' by R N Robinson and G J Cooper at Pages 11 to 13 of 'Television' (the journal of the Royal Television Society) for January/February 1982.

Although ACE gives good results, there is the problem that the equipment is very bulky. To overcome this problem, we have previously proposed a television standards converter comprising three field stores and four 4-line stores for receiving an input digital television signal of one standard and deriving therefrom arrays of sixteen lines, each array consisting of four successive lines from each of four successive fields of the input television signal. A weighting coefficient store stores sets of sixteen weighting coefficients, respective sets corresponding to positions both spatial and temporal of respective lines of an output digital television signal of a different standard, relative to the sixteen lines of the input television signal. Two interpolation filters then derive line

Nokia Exhibit 2004, p. 274
Amazon.com v. Nokia
IPR2024-01141

by-line the output television signal by multiplying corresponding sample values from each of the sixteen lines of the input television signal by a respective weighting coefficient in a set of weighting coefficients and sum the resulting products to form an interpolated sample value, and four output field stores receive and store the derived lines of the output television signal. To store the additional lines which are derived when the output television signal has more lines than the input television signal, a 45-line store is interposed between one of the interpolation filters and the output field stores. Further details will be found in our UK patent specification GB-A-2 140 644.

The performance of such standards converters which employ vertical/temporal interpolation techniques represents a compromise between generating blurred pictures while maintaining good motion portrayal and maintaining vertical resolution but at the expense of 'judder'. The former is a result of post filtering in order to prevent disturbing alias effects; the latter is a result of the intrusion of the adjacent 2-dimensional repeat sample structures.

According to the present invention there is provided a television standards converter comprising:

means for analyzing the motion between consecutive fields of an input television signal of one television standard;

means then to align said fields so as effectively to represent static pictures; and

means to effect conversion using said static pictures to derive the required output television signal of a different television standard.

According to the present invention there is also provided a 625-line 50-fields per second to 525-line 60-fields per second television standards converter comprising:

a 4-field time base corrector for receiving an input 625-line 50-fields per second digital television signal;

a motion analyzer connected to the output of said time base corrector for analyzing motion in said input television signal;

a shift register also connected to the output of said time base corrector;

an interpolator for deriving samples of a required output 525-line 60-fields per second digital television signal in dependence on samples

Nokia Exhibit 2004, p. 275
Amazon.com v. Nokia
IPR2024-01141

derived from said shift register and picture motion data derived by said motion analyzer; and

a 2-field time base corrector for assembling said derived samples to form said output television signal.

According to the present invention there is also provided a 525-line 60-fields per second to 625-line 50-fields per second television standards converter comprising:

a 2-field time base converter for receiving an input 525-line 60-fields per second digital television signal;

a motion analyzer connected to the output of said time base corrector for analyzing motion in said input television signal;

a shift register also connected to the output of said time base corrector;

an interpolator for deriving samples of a required output 625-line 50-fields per second digital television signal in dependence on samples derived from said shift register and picture motion data derived by said motion analyzer; and

a 4-field time base corrector for assembling said derived samples to form said output television signal.

According to the present invention there is also provided a slow motion processor comprising:

an input circuit for receiving an input digital television signal;

a motion analyzer for analyzing motion in an input digital television signal;

a shift register for holding successive different fields of said input television signal;

an interpolator for deriving samples of a required slow motion output digital television signal in dependence on the degree of slow motion, samples derived from said shift register, and picture motion data derived by said motion analyzer; and

a 2-field time base corrector for assembling said derived samples to form said slow motion output television signal.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

Figure 1 shows in very simplified block diagrammatic form a television standards converter according to the present invention;

Nokia Exhibit 2004, p. 276
Amazon.com v. Nokia
IPR2024-01141

Figure 2 shows in simplified block diagrammatic form a first embodiment of television standards converter according to the present invention;

Figure 3 shows in simplified block diagrammatic form a second embodiment of television standards converter according to the present invention;

Figure 4 shows in more detailed block diagrammatic form the first embodiment of television standards converter according to the present invention;

Figure 5 shows in more detailed block diagrammatic form the second embodiment of television standards converter according to the present invention;

Figure 6 shows part of the embodiment of Figure 5 in more detailed block diagrammatic form;

Figure 7 shows time charts for explaining the operation of Figure 6;

Figure 8 shows part of the embodiment of Figure 4 in more detailed block diagrammatic form;

Figure 9 shows time charts for explaining the operation of Figure 8;

Figure 10 shows part of the embodiment of Figure 4 in more detailed block diagrammatic form;

Figure 11 shows time charts for explaining the operation of Figure 10; and

Figure 12 shows part of the embodiment of Figure 4 in more detailed block diagrammatic form.

The embodiments of standards converters to be described maintain vertical resolution and remove the 'judder' by compensating for motion between fields. In effect the motion between consecutive fields is analyzed. These fields can then be 'aligned' such that they represent static pictures upon which conversion can then take place. As a result, vertical resolution can be maintained.

The embodiments of standards converter to be described can be divided into two parts. The first part is analogous to a known standards converter performing vertical/temporal interpolation to convert between 525/60 and 625/50 television standards. Alone, this would generate an output in which vertical resolution would be

Nokia Exhibit 2004, p. 277
Amazon.com v. Nokia
IPR2024-01141

maintained but with the added effect of judder. To remove this judder four fields of the input digital television signal which are used in the conversion process are aligned under the control of motion vectors generated from a motion analyzer which forms the second part of the standards converter.

This is shown in very simplified diagrammatic block form in Figure 1. The video portion of an input digital television signal of one standard, which may for example have been derived by sampling an analogue television signal at 13.5 MHz, is supplied to an interpolator 1 from which the video portion of the required output television signal of a different standard is derived. A motion analyzer 2 receives the luminance video and derives motion vectors which provide data representing the motion between successive fields of the input television signal to control the operation of the interpolator 1. The interpolator 1 operates in a generally similar manner to the corresponding portion of a known standards converter, for example as referred to above. It also, however, contains the means to align the four fields used in the interpolation, under the control of the motion vectors.

The repositioning of the four fields is performed in two stages. The first stage involves varying the address of a variable delay element associated with each field to reposition the picture to the nearest line or sample. The second stage uses interpolation techniques both vertically and horizontally to reposition to within $\pm 1/16$ line or $\pm 1/8$ of a sample. Even with no movement, both the above techniques are used to enable conversion of line standards.

The vertical interpolator has four taps per field allowing effectively an 8-tap vertical filter to be applied to the static pictures. An 8-tap interpolator allows good vertical resolution to be maintained with minimal distortion. The effect of distortion in the horizontal interpolator is less of a problem, so a 2-tap horizontal filter is used, although a 4-tap horizontal filter, for example, may be used.

The temporal interpolator is used in normal operation to enable interpolation of perspective changes or when no sensible motion vector can be detected, in which case the interpolator 1 must revert to normal standards conversion operation where no picture re-positioning

Nokia Exhibit 2004, p. 278
Amazon.com v. Nokia
IPR2024-01141

occurs.

When converting from a high field rate to a lower rate, the incoming fields are interpolated such that an interpolated field can occasionally be dropped without any movement deterioration. All the interpolation is done at the input field rate and passed to a time base corrector which then spreads the fields generated over the required time period for the output standard.

The above operation is necessary when converting from 525/60 to 625/50. It is also evident however that 625 lines must be generated where only 525 lines exist in the input signal.

To overcome the line number conversion problem a second time base corrector is used at the input to produce a signal having 585 lines at the 60 Hz rate. A 585-line format can contain all the active picture information in the 625-line format. Following this first time base corrector there are occasional lines which have no video information. The interpolator stores are frozen during this time, so that an additional interpolated line can be generated from the same lines used to generate the previous output line. This process allows 625 lines to be interpolated from the original 525.

The reason for selecting the 585/60 format will now be explained in more detail. A 625-line picture contains 288 active lines in each field, and 720 samples in each horizontal line at the sampling rate of 13.5 MHz. The circuits, to be described below, of the embodiments of Figure 4 and 5 use techniques which allow the picture to be shifted horizontally by plus or minus twenty-four samples. This requires a minimum horizontal blanking of forty-eight samples. The total number of sample positions required in a field is therefore:

$$(720 + 48) \times 288$$
$$= 221184.$$

There are clearly considerable advantages in using a 13.5 MHz clock throughout the system, in which case the number of clock cycles within a 60 Hz period (more exactly a 59.94 Hz period) is:

225225.

Nokia Exhibit 2004, p. 279
Amazon.com v. Nokia
IPR2024-01141

If 576 lines of data are required in one frame, the number of horizontal samples would be 782.03125. Although this number is sufficient to contain the required (720 + 48) samples, the fractional sample would mean that the structure was non-orthogonal on a line to line basis. This would cause significant design difficulties in the rest of the standards converter, so the number of lines required was gradually increased, from 576, until a whole number of samples, in fact 770, existed in each line.

The only format that achieves the orthogonal structure is the 585/60 format, which in addition gives a useful vertical blanking of four lines in the first field, five lines in the second field and fifty samples of horizontal blanking.

In the 625/50 to 625/50 slow motion mode referred to below there is no requirement to store the active video of the 625 format within a 60 Hz period, so the interpolation and other processing is done in the normal 625/50 format.

When converting from a low field rate to a higher rate the input time base corrector is required to produce a video stream at the output rate. This is done by occasionally repeating an input field. When the repeated field occurs, all the interpolator stores must be frozen so that the interpolation is applied to the same input fields used to create the previous output field.

If this technique were not used, two sets of interpolator and movement detector would be required to make up the missing field.

The above operation is performed when converting from 625/50 to 525/60. To allow 625 lines to exist during a 60-fields per second period again requires the 585/60 intermediate format to be adopted. During this process some of the interpolated lines will not be required, as only 525 have to be produced from the original 625. A time base converter is therefore required on the output to produce the final 525/60 format.

The amount of interpolation required is determined by comparing input and output synchronization pulse phases.

As mentioned above, motion analysis is performed on the luminance of the input video. The method employed involves a number of stages to arrive at a single motion vector for each pixel. Movement can be detected in the range ± 24 pixels horizontally and ± 8 (field rate)

Nokia Exhibit 2004, p. 280
Amazon.com v. Nokia
IPR2024-01141

vertically.

In a first stage, motion in the picture at points on the screen spaced sixteen samples horizontally and eight lines vertically is determined using a block matching technique. The original motion vectors in a field are calculated every sixteenth sample and every eighth line. Each one of these points is at the centre of a search block. Conceptually each block is scanned ±24 samples horizontally, and +8 and -8 samples vertically over the next field each time generating the summation of the differences between the two fields over the area of the search block. The minimum overall difference then indicates in which direction the object at that point has moved.

In practice, the above technique is applied in separate steps which greatly reduces the amount and complexity of hardware required:

Step 1.

Test for minimum difference in just three positions, centre position, sixteen samples to the left, sixteen samples to the right.

Step 2. Starting from point indicated above.

Test for minimum difference in nine positions symmetrically distributed about the above starting point in steps of eight samples or lines.

Step 3. Starting from point indicated above.

Test for minimum difference in nine positions symmetrically distributed about the above starting point in steps of four samples or lines.

Step 4. Starting from point indicated above.

Test for minimum difference in nine positions symmetrically distributed about the above starting point in steps of two samples or lines.

Step 5. Starting from point indicated above.

Test for minimum difference in nine positions symmetrically distributed about the above starting point in steps of one sample or line.

Step 6.

After step 5, the motion of the object has been detected to the nearest pixel. A more accurate motion vector value can be achieved by adding a sixth step in which the difference produced at the final position indicated by step 5 is compared with the two differences

Nokia Exhibit 2004, p. 281
Amazon.com v. Nokia
IPR2024-01141

above and below to adjust the vertical vector value and with the two differences to the left and right to adjust the horizontal vector value.

The above technique relies on achieving correlation between the reference search block and a similar block of video data on the following field (the search positions). In step 5 it is possible the true movement was a half pixel more or less than detected, but it is necessary for the best correlation to occur at this point, even although exact correlation cannot be achieved. To ensure this occurs the picture can be filtered both vertically and horizontally by a gaussian filter which has +6 dB attenuation at 1/2 Nyquist frequency.

Similarly, for step 4, the picture can be filtered with a 6 dB attenuation at 1/4 Nyquist frequency, which allows a one pixel error in detection.

Step 3 uses a picture filtered with a 6 dB attenuation at 1/8 Nyquist frequency allowing a two pixel error.

Step 2 uses a picture frequency with a 6 dB attenuation at 1/16 Nyquist frequency allowing a four pixel error.

Finally, step 1 uses a picture filtered with 6 dB attenuation at 1/32 Nyquist frequency allowing an eight pixel error. In addition, because the pictures are so heavily filtered during steps 1, 2, 3 and 4, the samples can be reduced, for example halved in number, which still further greatly reduces the number of calculations and amount of hardware required.

The effective search block size is sixteen lines high and forty-eight samples long. A large search block is necessary to detect accurately the movement of large plain areas. The central part of plain areas are unimportant as the values of the pixels at these points do not change from one field to the next, but the edges of such objects are obviously important. If the detection of motion is limited to ± 24 samples horizontally and ± 8 lines vertically then a block of the above size would be the minimum size to ensure accurate motion detection.

In the embodiments, depending upon the conversion modes, the luminance video entering the motion analyzer 2 is in various forms of 585-lines/60-fields per second. This might comprise repeated lines for 525 input or repeated fields for 625 input. In addition, the

Nokia Exhibit 2004, p. 282
Amazon.com v. Nokia
IPR2024-01141

input contains both field polarities. The first process is to ensure a continuity of data and single field polarity for the motion estimation processing. This is done by interpolation on the input data by a vector interface to maintain continuity, and filtration horizontally to aid subsequent motion detection/correlation.

Separate outputs from this circuit are passed to motion estimation vector filters and motion detection field stores/vector selectors. The output of the vector interface is, as described above, spatially continuous, single field polarity data. The output to the field stores/vector selectors depends upon the input and output modes. In some modes it is continuous, and in others it contains repeated lines/fields. The vector filters and vector calculators perform the steps outlined above.

The processing of the various steps is performed by vector calculators and a vector processor. The vector calculators perform steps 1 to 5 and the vector processor performs step 6. In addition, the vector processor performs the second stage in the motion estimation, as follows:

For each 8 x 16 block a choice is made of four from seven motion vectors, the seven motion vectors being the one for that particular block and the six for the six nearest blocks respectively.

In addition, the vector processor also determines the four most common motion vectors throughout the whole input field, these being called modal motion vectors. The primary use of the modal motion vectors is in the border areas close to the edge of a field where it is not possible actually to calculate any local motion vectors. Also, if any one or more of the local motion vectors are equal, then these are substituted for by the modal motion vectors.

In the next stage of motion detection, for each pixel, the four motion vectors are tested by producing the difference between the extrapolated positions on field 0 to field 1. During standards conversion a field needs to be interpolated between two fields; say between field 0 and field 1. So the motion vectors generated between these two fields are considered to be most representative of the motion. Four motion vectors are used from these two fields. To decide which is the correct motion vector a pixel from field 0 is compared with a pixel from field 1 using the motion vector to decide

Nokia Exhibit 2004, p. 283
Amazon.com v. Nokia
IPR2024-01141

where the pixel to be generated had come from on field 0 and where it has gone to by field 1. Mathematically, if the position x, y, z must be generated, where; x = horizonal position, y = vertical position, z = temporal position between field 0 and field 1, the pixels used for comparison are as shown below. Field 0 is assumed to be at z=0 and field 1 at z=1.

Pixel from field 0

$$x^0 = x - V_h * z$$

$$y^0 = y - V_v * z$$

Pixel from field 1

$$x^1 = x + (1-z)V_h$$

$$y^1 = y + (1-z)V_v$$

V_h = horizontal component of vector

V_v = vertical component of vector

For each motion vector a modulus of the difference between the pixels indicated in field 0 and field 1 is found. The minimum difference is assumed, as a first estimate, to indicate the correct motion vector. If a number of motion vectors produce a very similar difference then these motion vectors are tested again using a comparison between fields -1 and 0.

Pixels from field -1

$$x^{-1} = x - (1+z)V_h$$

$$y^{-1} = y - (1+z)V_v$$

The minimum modulus of difference of the remaining motion vectors produced by this second test is then considered to represent most accurately the motion vector.

If a number of motion vectors again have similar differences then an option exists to assume no movement. If only the horizontal component varied and the vertical component did not, then only the horizontal component would be set to zero and the vertical component would be maintained at the detected value. If only the vertical

Nokia Exhibit 2004, p. 284
Amazon.com v. Nokia
IPR2024-01141

component varied, then the horizontal component would be maintained and only the vertical component set to zero. If the pixel difference chosen is too large then an option exists to set the whole motion vector to zero in both directions.

A final stage is applied once every pixel has been assigned a motion vector. Here the motion of each pixel is tracked from one field to the next and a recursive filter applied to the motion vector value. This removes the effects of noise and small movement estimation errors and also smooths the trajectory of the motion vectors.

There are two possible ways of tracking the motion of a pixel.

In the first, the motion vector for a pixel in field t is used to point to a pixel in field (t+1). The motion vector determined for this pixel in field (t+1) is then recursively filtered to form the final motion vector for the pixel in field (t+1).

In the second, the motion vector for a given pixel in field t is used to point to a pixel in field (t-1). The motion vector from this pixel is then recursively filtered with the motion vector for the given pixel to form the final motion vector for this given pixel in field t.

In either case the final output is a motion vector for each pixel which is passed from the motion analyzer to the interpolator to be employed in aligning the four fields used in the standards conversion process.

A first embodiment of standards converter for converting an input digital 625-line 50-fields per second television signal to an output digital 525-line 60-fields per second television signal will now be described with reference to Figure 2, which shows the standards converter in simplified block form.

The incoming video at 50-fields per second and a sample rate of 13.5 MHz is supplied to a 4-field store time base corrector (TBC) 11. The TBC 11 occasionally repeats fields, so that the output is at 60-fields per second. The control to the TBC 11 which causes the repetition of a field is derived from the input field synchronization pulses, and the required output synchronization pulses. The comparison of the synchronization pulses also provides a temporal offset figure which indicates the amount of temporal interpolation

Nokia Exhibit 2004, p. 285
Amazon.com v. Nokia
IPR2024-01141

required at the output of the TBC 11 such that smooth motion at 60-fields per second would be observed.

When converting from 50-fields per second to 60-fields in this way a line conversion of 625 to 525 is necessary. It is therefore necessary to maintain the original 625 lines of information at a 60-fields per second rate so that they are all available to form the interpolated lines.

The embodiment uses an intermediate standard which is capable of containing all the active vertical information of the 50-fields per second signal at the 60-fields per second rate. The intermediate standard also contains all the active line information arranged orthogonally line by line still using the original 13.5 MHz sample rate.

The intermediate standard used, and which is as explained above capable of meeting all these requirements, is a 585-line format at 60-fields per second. When sampled at 13.5 MHz each line of this format has exactly 770 samples. It is clear therefore that 585 lines is sufficient to contain the 576 active lines of the 625-line format at a 60-fields per second rate. As the active line width is only 720 samples there is still fifty samples of horizontal blanking.

The interpolator 1, be it linear or motion compensated, derives the 585-line format signal from the TBC 11 via four field stores 12, 13, 14 and 15 arranged as a temporal shift register 16. When the output of the TBC 11 is frozen, during a repeat field, the shift register 16 is also frozen so that four distinct consecutive fields of the input always exist in the shift register 16. The shift register 16 is then used to provide the temporal taps for the interpolator 1.

Data is sent directly from the output of the TBC 11 to the motion analyzer 2, so that motion vectors can be generated. In fact a frame delay 17 is necessary between the TBC 11 and the shift register 16 to allow for the time taken to process the motion vectors. The freezing of the shift register 16 must therefore also be delayed by one frame.

Each temporal tap produces four line taps at a position depending on the motion vectors, so that a 2-dimensional filter can be used to provide the necessary interpolation. The interpolated picture will contain 576 active lines, so that a correct picture will be obtained when every sixth line in one field is dropped. The 484 lines left

Nokia Exhibit 2004, p. 286
Amazon.com v. Nokia
IPR2024-01141

produce the active picture portion of the 525-line format. To enable lines to be dropped in this way, the output from the interpolator 1 is supplied to a 2-field TBC 18. The TBC 18 writes in all 576/2 lines, but only reads out the required 484/2 lines to provide the required output television signal.

This embodiment can readily be modified to form a slow motion processor with good motion portrayal. It is not however necessary to use the vertical interpolator to provide the line number conversion.

Whereas in 50-fields per second to 60-fields per second conversion a field was occasionally repeated, in slow motion the field is repeated the same number of times as the input field is repeated. As repeated fields are not written into the shift register 16, the shift register 16 again contains distinct consecutive fields. Indeed if a video tape recorder reproduces without any interpolation of its own, the original interlace structure is maintained allowing full resolution pictures to be produced. The temporal offset required is calculated by comparing the actual field rate pulses, be they 50-fields per second or 60-fields per second, with the rate at which a new field is received. To determine the temporal offset in this way, the system needs a signal to be available which indicates the true field polarity of the field being repeatedly replayed. The vertical interpolator will always produce the field polarity required at the output.

Conceptually the TBC 11 is not really required for slow motion operation, but its presence does provide a frame synchronization facility and also simplifies the system configuration.

A second embodiment of standards converter for converting an input digital 525-line 60-fields per second television signal to an output digital 625-line 50-fields per second television signal will now be described with reference to Figure 3, which shows the standards converter in simplified block form. In this case, interpolation requires that all the input data is available in a consecutive form. In this embodiment it would not therefore be possible to convert to 50-fields per second before the interpolator 1. The input data however contains only 484 active lines and the interpolator 1 must produce 576. A 2-field TBC 21 is therefore positioned at the front of the standards converter to provide the necessary time slots for 484

Nokia Exhibit 2004, p. 287
Amazon.com v. Nokia
IPR2024-01141

line to 576-line conversion.

The original continuous line structure is written into the TBC 21, but is read out in the 585-line standard with approximately every sixth line being blank. The interpolator 1 is then used to produce a continuous picture at the output line rate by freezing its line stores during the blank input line, and producing the required additional line at the output, so ensuring that a spatially correct picture is produced. The required temporal offset is detected and applied as in the first embodiment, although the interpolation is applied such that a field can occasionally be dropped leaving the motion smooth. The field is dropped such that 60-fields per second to 50-fields per second conversion is achieved. The dropping of a field is achieved by using a 4-field TBC 22 at the output.

The first embodiment of standards converter for converting an input digital 625-line 50-fields per second television signal to an output digital 525-line 60-fields per second television signal is shown in detailed block form in Figure 4. Where appropriate, the same reference numerals are used as in Figure 2, but with suffixes added in some cases.

The incoming video at 50-fields per second and a sample rate of 13.5 MHz, that is CCIR 601 data, is supplied to a demultiplexer 31 which separates it into luminance components Y, synchronizing signals SYNC and chrominance components UV. The luminance components Y are supplied to a 4-field luminance TBC 11Y and the chrominance components UV are supplied to a 4-field chrominance TBC 11C. The synchronizing signals SYNC are supplied to a control 32 together with an input field polarity signal from an external input, and an output synchronizing reference signal from another external input.

The luminance data (D) from the luminance TBC 11Y is supplied by way of a processing compensating delay 17Y to a luminance temporal shift register 16Y comprising four field stores (FS) 12Y, 13Y, 14Y and 15Y. The luminance TBC 11Y also supplies a temporal freeze signal (F) by way of the delay 17Y to the shift register 16Y. The chrominance TBC 11C supplies the chrominance data (D) by way of a processing compensating delay 17C to a chrominance temporal shift register 16C which comprises four field stores 12C, 13C, 14C and 15C. The chrominance TBC 11C also supplies a temporal freeze signal by way of

Nokia Exhibit 2004, p. 288
Amazon.com v. Nokia
IPR2024-01141

the delay 17C to the shift register 16C. Associated with the shift register 16Y is a luminance interpolator 1Y which receives inputs from each of the field stores 12Y, 13Y, 14Y and 15Y. The output of the luminance interpolator 1Y is supplied to a 2-field luminance TBC 18Y. Associated with the shift register 16C is a chrominance interpolator 1C which receives inputs from each of the field stores 12C, 13C, 14C and 15C. The output of the chrominance interpolator 1C is supplied to a 2-field chrominance TBC 18C. The outputs of the luminance TBC 18Y and of the chrominance TBC 18C are supplied to a multiplexer 34 which multiplexes the luminance components Y and the chrominance components UV to provide output CCIR 601 data in the form of a digital 525-line 60-fields per second television signal.

The control 32 supplies control signals (C) to the luminance TBC 11Y and to the chrominance TBC 11C. The control 32 also supplies control signals to the luminance TBC 18Y and the chrominance TBC 18C. It also supplies interpolation control signals (IC) to the luminance interpolator 1L and to the chrominance interpolator 1C.

The luminance data only, as supplied by the luminance TBC 11Y, is also supplied to the motion analyzer 2 shown in the upper part of Figure 4.

The motion analyzer 2 comprises a vector interface 35 to which the luminance data from the luminance TBC 11Y is supplied, together with the interpolation control signal from the control 32. The vector interface 35 supplies data interpolated to 625 lines to a vector filter 36 and to a vector calculator 37, which together perform the motion estimation described above. The output of the vector calculator 37 is supplied to a modal motion vector processor 38 and also to a sub-pixel motion estimator 39. The motion vector processor 38 supplies four outputs and the sub-pixel motion estimator 39 one output to a motion vector reducer 40 which supplies four outputs to a vector selector 41.

The vector interface 35 also supplies the data interpolated to even fields to a processing compensating delay 42 to which it also supplies the received interpolation control signal, and also a temporal freeze signal generated at the vector interface 35. The data from the delay 42 is supplied to a temporal shift register 43 which comprises three field stores 44, 45 and 46 which supply respective

Nokia Exhibit 2004, p. 289
Amazon.com v. Nokia
IPR2024-01141

data outputs to the vector selector 41. The delay 42 supplies the interpolation control signal to the vector selector 41 which supplies the selected motion vector to a recursive motion vector filter 47, the output of which is the motion vector data which is supplied to the luminance interpolator 1Y and to the chrominance interpolator 1C.

The way in which the motion analyzer 2 derives the motion vector data has been described in detail above, but the operation of the elements 35 to 43 and 47 will now be briefly described.

The vector interface 35 receives the luminance data from the luminance TBC 11Y, and the interpolation control signals from the control 32. It supplies 625-line data, normally contained within the 585/60 format, to the vector filter 36. It also supplies data to the delay 42. These data must contain a picture which is the same line standard as the required output, again normally contained within the 585/60 format. Each field of the interpolated data is also made to appear even.

The vector filter 36 produces the filtered picture data required for steps 1 to 5 above of the motion detection. The filtered picture data are supplied in sample reduced form to the vector calculator 37.

The vector calculator 37 operates on the filtered and sample-reduced data from the vector filter 36 using an algorithm described in the terms of steps 1 to 5 above of the motion detection. The process is essentially a two-dimensional binary search for motion down to pixel/line resolution. For each field, 1200 motion vectors are generated and are supplied to both the modal vector processor 38 and the sub-pixel motion estimator 39. It also supplies surrounding weighted absolute difference (WAD) values as calculated by step 5 above to the sub-pixel motion estimator 39. For details of WAD calculations, see 'Advances in Picture Coding', Musmann et al, Proceedings of the IEEE, April 1985. The specific WAD value which is the minimum in step 5 above of the motion detection provides a figure of merit (FOM).

The vector processor 38 calculates the four most common motion vectors that are detected in each field and supplies them to the vector reducer 40.

The sub-pixel motion estimator 39 receives the motion vectors from the vector calculator 37 together with the surrounding WAD

Nokia Exhibit 2004, p. 290
Amazon.com v. Nokia
IPR2024-01141

values. From these it estimates sub-pixel movement to be appended to the motion vector values. With each motion vector its corresponding final WAD value is also supplied to the vector reducer 40.

The vector reducer 40 receives the motion vectors from the vector processor 38 and from the sub-pixel motion estimator 39. For each motion vector from the sub-pixel motion estimator 39, the six motion vectors closest to it are grouped together. For each motion vector there are then eleven choices. The reduction process selects four motion vectors from the eleven for supply to the vector selector 41.

The vector reducer 40 supplies the vector selector 41 with four representative motion vectors for each sixteen pixel by eight line block of the picture. By comparing pixels over three fields, the vector selector 41 selects the single best motion vector for each pixel in the picture. The motion vector selected is supplied to the motion vector filter 47.

The delay 42 delays the data by one frame less twenty-one lines to compensate for other delays in the system.

The temporal shift register 43 holds and supplies the three fields of data used by the vector selector 41.

The motion vector filter 47 tracks a motion vector from one field to another so applying some filtering to the motion vectors by combining motion vectors in different fields, so reducing motion detection errors. The output of the motion vector filter 47 is supplied to the luminance and chrominance interpolators 1Y and 1C to control the alignment of the field data.

Exactly the same hardware can be used as a slow motion processor for either a 625/50 or a 525/60 television signal. In all cases the control 32 determines what action is required by recognizing the input/output standard from the input and output field synchronizing signals. In slow motion the input field polarity is used.

The second embodiment of standards converter for converting an input digital 525-line 60-fields per second television signal to an output digital 625-line 50-fields per second television signal is shown in detailed block form in Figure 5. Where appropriate, the same reference numerals are used as in Figure 3, but with suffixes added in some cases.

The second embodiment differs from the first embodiment shown in

Nokia Exhibit 2004, p. 291
Amazon.com v. Nokia
IPR2024-01141

Figure 4 in only minor respects. In particular, the luminance TBCs 11Y and 18Y are interchanged, and the chrominance TBCs 11C and 18C are also interchanged. Also, no temporal freeze signals are required. Other than in these respects, the form and operation of the second embodiment are the same as those of the first embodiment.

In both cases the control 32 has various functions as follows; controlling the reading and writing of the TBCs 11Y, 11C, 18Y and 18C; generating a temporal offset number, and in the case of the first embodiment the temporal freeze signal, and generating a vertical offset number together with vertical interpolation control signals. These functions will now be described in more detail.

Firstly, the 2-field luminance and chrominance TBCs 18Y and 18C always switch between field stores at the end of every 60 Hz field. However, the operation of the 4-field luminance and chrominance TBCs 11Y and 11C depend on the mode of operation, and their control is also associated with the generation of the temporal offset signal. In fact, the control of the luminance and chrominance TBCs 11Y and 11C is determined from the input and output field synchronizing signals.

The derivation of the temporal offset signal in the case of 525/60 to 625/50 operation will now be described with reference to Figures 6 and 7.

In Figure 6, the control 32 is shown as including a line counter 61, and first and second latches 62 and 63. A line clock signal is supplied to a clock terminal of the line counter 61, while the input field synchronizing signal is supplied to a reset terminal of the line counter 61 and to a clock terminal of the second latch 62. The output field synchronization signal is supplied to a clock terminal of the first latch 62. The output of the line counter 61 is supplied to the input of the first latch 62, the output of which is supplied to the input of the second latch 63, the output of which is the temporal offset signal supplied to the luminance and chrominance shift registers 11Y, 11C, 18Y and 18C.

The input and output field synchronizing signals are shown in Figures 7A and 7B respectively. Figure 7C shows the output of the line counter 61 which repetitively counts from 0 to 524. Figures 7D and 7E show the outputs of the first and second latches 62 and 63 respectively. By latching the counter 61, the required proportion of

Nokia Exhibit 2004, p. 292
Amazon.com v. Nokia
IPR2024-01141

the input field period is determined. The temporal shift value tn indicates the position between two input fields where the output field must be interpolated such that when the shaded field shown in Figure 7A is dropped, continuous motion still occurs. Thus, the field which uses the temporal offset shown shaded in Figure 7E is the one that is dropped. It will be seen by reference to Figures 7A and 7B, that the field which is dropped is the one which does not have a new temporal shift associated with it. The field (arrowed) which is to be dropped is indicated to the following circuitry by the temporal freeze signal.

The derivation of the temporal offset signal in the case of 625/50 to 525/60 operation will now be described with reference to Figures 8 and 9.

In Figure 8, the control 32 is shown as including a line counter 71 and a latch 72. A line clock signal is supplied to a clock terminal of the line counter 71, while the input field synchronizing signal is supplied to a reset terminal of the line counter 71. The output field synchronization signal is supplied to a clock terminal of the latch 72. The output of the line counter 71 is supplied to the input of the latch 72, the output of which is the temporal offset signal supplied to the luminance and chrominance shift registers 11Y, 11C, 18Y and 18C.

The input and output field synchronizing signals are shown in Figures 9A and 9B respectively. Figure 9C shows the output of the line counter 71 which repetitively counts from 0 to 624. Figure 9D shows the output of the latch 72. By latching the counter 71, the required proportion of the input field period is determined. Thus, the temporal shift value tn again indicates the position between two input fields where the output field must be interpolated, such that if the shaded field is repeated, continuous motion still occurs. The field which is repeated is the one which has two temporal shift values associated with it. The field (arrowed) which is to be repeated is indicated to the following circuitry by the temporal freeze signal.

The deviation of the temporal offset signal in the case of slow motion whether at 525/60 to 525/60 or 625/50 to 625/50 is the same, and will now be described with reference to Figures 10 and 11.

In Figure 10, the control 32 is shown as including a line counter 81, a field counter 82, first to fourth latches 83 to 86, an

Nokia Exhibit 2004, p. 293
Amazon.com v. Nokia
IPR2024-01141

exclusive-OR gate 87 and a scaler 88. The input field synchronizing signal is supplied to a clock terminal of the first latch 83, to a clock enable terminal of the field counter 82, and to a second reset terminal of the line counter 81. The input field polarity signal is supplied to the first latch 83 and thence to the second latch 84 and also to one input of the gate 87. The second latch 84 supplies an output to the second input of the gate 87, the output of which is supplied to a first reset terminal of the line counter 81, to a reset terminal of the field counter 82 and to a clock terminal of the third latch 85, which forms a speed detector latch. A line clock signal is supplied to a clock terminal of the second latch 84, and to respective clock terminals of the line counter 81 and the field counter 84. The output of the line counter 81 is supplied to an input terminal of the scaler 88, and the output of the field counter 82 is supplied to an input of the third latch 85 and also to an offset input terminal of the scaler 88. The output field synchronizing signal is supplied to a clock terminal of the fourth latch 86. The output of the third latch 85 is supplied to a scale factor terminal of the scaler 88, the output of which is supplied to the fourth latch 86, the output of which is the temporal offset signal.

The input field synchronizing signal and the input field polarity signal are shown in Figures 11A and 11B respectively. Figure 11C also indicates the input field synchronizing signals and Figure 11D the output field synchronizing signals. Figures 11E and 11F indicate the operations of the field counter 82 and the line counter 81, which are respectively counting fields and lines from 0 to N. Figure 11G indicates the output of the fourth latch 86 which is the temporal offset signal. Figure 11H indicates the temporal freeze signal (which is active when low), and, as indicated by the arrows, the shaded field that uses the temporal offset shown is a repeat of the previous field that used the temporal offset t1.

To generate the temporal freeze signal, the control 32 is shown in Figure 12 as including a synchronous RS flip-flop 91, a latch 92, an inverter 93 and an AND-gate 94. The output field synchronizing signal is supplied to one input of the flip-flop 91, to the input of the inverter 93 and to a clock enable terminal of the latch 92. The input field synchronizing signal is supplied to the other input of the

Nokia Exhibit 2004, p. 294
Amazon.com v. Nokia
IPR2024-01141

flip-flop 91, while a line clock signal is supplied to clock terminals of the flip-flop 91 and the latch 92. The output of the flip-flop 91 is supplied to one input of the gate 94, which receives at its other input the output of the inverter 93. The output of the gate 94 is supplied to the input of the latch 92, the output of which forms the temporal freeze signal. The operation of this circuit is such that if more than one output field synchronizing pulse follows an input field synchronizing pulse, a freeze occurs.

Finally, referring back to Figure 4, the generation of the vertical offset number by the control 32 will now be described. The same address generator which reads data from the luminance TBC 11Y into the luminance interpolator 1Y and the motion analyzer 2, also addresses an erasable programmable read-only memory (EPROM) which provides the vertical offset number together with vertical freeze signals when required.

(In the Figure 5 arrangement which is used for 525/60 to 625/50, the read addresses of the luminance TBC 18Y are used, but in all other modes the read addresses of the luminance TBC 11Y are used.)

The vertical offset number is generated assuming that both the input and the output fields are even, and it then indicates the position between two input lines where the output line must be interpolated such that a non-distorted picture would be produced if:
a line were occasionally dropped in 625/50 to 525/60 conversion,
or
a line were occasionally repeated in 525/60 to 625/50 conversion.

When a line is repeated by the luminance TBC 11Y (18Y), a vertical freeze signal is generated.

If the input fields are not both even, then the interpolators 1Y and 1C must make use of the input field polarity and output field polarity to ensure correct interpolation.

The contents of the EPROM are generated in a way similar to that described above in connection with Figure 12 for the temporal offset signal, using the known line position in both a 525 and a 625 picture.

Attention is drawn to seven other UK patent applications relating to subject matter similar to that of the present application, which we filed on the same day as the present application, and the disclosures in which are incorporated herein by reference.

Nokia Exhibit 2004, p. 295
Amazon.com v. Nokia
IPR2024-01141

CLAIMS

1. A television standards converter comprising:
means for analyzing the motion between consecutive fields of an input television signal of one television standard;
means then to align said fields so as effectively to represent static pictures; and
means to effect conversion using said static pictures to derive the required output television signal of a different television standard.

2. A television standards converter according to claim 1 wherein said means to effect conversion comprises an interpolator for effecting vertical/temporal interpolation, and said input television signal is supplied to said interpolator by way of a time base corrector which produces therefrom a 585-line 60-fields per second television signal.

3. A television standards converter according to claim 2 wherein said input television signal is a 625-line 50-fields per second signal, said time base corrector is a 4-field time base corrector, and the output of said time base corrector is supplied to said interpolator by way of a 4-field shift register.

4. A television standards converter according to claim 2 wherein said input television signal is a 525-line 60-fields per second signal, said time base corrector is a 2-field time base corrector, and the output of said time base corrector is supplied to said interpolator by way of a 4-field shift register.

5. A television standards converter according to any one of the preceding claims wherein said means to align said fields operates to vary the address of a variable delay element to reposition each pixel of the picture to the nearest line or sample, and then reposition each pixel of the picture both vertically and horizontally to a fraction of a line and a fraction of a sample respectively.

Nokia Exhibit 2004, p. 296
Amazon.com v. Nokia
IPR2024-01141

6. A television standards converter according to claim 5 wherein said vertical repositioning to a fraction of a line is done by a vertical interpolator with four taps per field, and said horizontal repositioning to a fraction of a sample is done by a horizontal filter having two or four taps.

7. A 625-line 50-fields per second to 525-line 60-fields per second television standards converter comprising:
a 4-field time base corrector for receiving an input 625-line 50-fields per second digital television signal;
a motion analyzer connected to the output of said time base corrector for analyzing motion in said input television signal;
a shift register also connected to the output of said time base corrector;
an interpolator for deriving samples of a required output 525-line 60-fields per second digital television signal in dependence on samples derived from said shift register and picture motion data derived by said motion analyzer; and
a 2-field time base corrector for assembling said derived samples to form said output television signal.

8. A television standards converter according to claim 7 wherein said 4-field time base corrector derives a 585-line 60-fields per second television signal from said input television signal for supply to said shift register.

9. A 525-line 60-fields per second to 625-line 50-fields per second television standards converter comprising:
a 2-field time base converter for receiving an input 525-line 60-fields per second digital television signal;
a motion analyzer connected to the output of said time base corrector for analyzing motion in said input television signal;
a shift register also connected to the output of said time base corrector;
an interpolator for deriving samples of a required output 625-line 50-fields per second digital television signal in dependence on samples derived from said shift register and picture motion data derived by

Nokia Exhibit 2004, p. 297
Amazon.com v. Nokia
IPR2024-01141

said motion analyzer; and
a 4-field time base corrector for assembling said derived samples to form said output television signal.

10. A television standards converter according to claim 9 wherein said 2-field time base corrector derives a 585-line 60-fields per second television signal from said input television signal for supply to said shift register.

11. A television standards converter according to claim 8 or claim 10 wherein said motion analyzer derives motion vectors in dependence on the motion between corresponding pixels in consecutive fields of said input television signal, and supplies said motion vectors to said interpolator so as effectively to align said pixels in said consecutive fields to represent static pictures.

12. A slow motion processor comprising:
an input circuit for receiving an input digital television signal;
a motion analyzer for analyzing motion in said input digital television signal;
a shift register for holding successive different fields of said input television signal;
an interpolator for deriving samples of a required slow motion output digital television signal in dependence on the degree of slow motion, samples derived from said shift register, and picture motion data derived by said motion analyzer; and
a 2-field time base corrector for assembling said derived samples to form said slow motion output television signal.

13. A slow motion processor according to claim 12 wherein said input circuit comprises a 4-field time base corrector.

14. A slow motion processor according to claim 13 wherein said 4-field time base corrector derives a 585-line 60-fields per second television signal from said input television signal for supply to said shift register.

Nokia Exhibit 2004, p. 298
Amazon.com v. Nokia
IPR2024-01141

15. A television standards converter substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

16. A television standards converter substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.

17. A television standards converter substantially as hereinbefore described with reference to Figure 4 of the accompanying drawings.

18. A television standards converter substantially as hereinbefore described with reference to Figure 5 of the accompanying drawings.

19. A slow motion processor substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

20. A slow motion processor substantially as hereinbefore described with reference to Figure 4 of the accompanying drawings.

Nokia Exhibit 2004, p. 299
Amazon.com v. Nokia
IPR2024-01141

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L Number	Hits	Search Text	DB	Time stamp
1	198	sub adj4 pixel adj4 interpolat$4	USPAT; US-PGPUB	2004/08/24 07:34
2	198	sub adj4 pixel adj4 interpolat$4	USPAT; US-PGPUB	2004/08/24 07:34
3	136	sub adj4 pixel adj4 interpolat$4	USPAT	2004/08/24 07:34
4	0	(sub adj4 pixel adj4 interpolat$4) same (weight$4 adj4 sum$3)	USPAT	2004/08/24 07:35
5	33	(sub adj4 pixel adj4 interpolat$4) and (weight$4 adj4 sum$3)	USPAT	2004/08/24 07:36
6	111	375/240.17.ccls.	USPAT	2004/08/24 07:38
7	1	((sub adj4 pixel adj4 interpolat$4) and (weight$4 adj4 sum$3)) and 375/240.17.ccls.	USPAT	2004/08/24 07:37
8	15	375/240.17.ccls. and (weigh$4 near4 sum$3)	USPAT	2004/08/24 07:39

Nokia Exhibit 2004, p. 300
Amazon.com v. Nokia
~~**IPR2024-01141**~~

L Number	Hits	Search Text	DB	Time stamp
1	210673	"1/2"$2 or (unit adj3 (horizontal or vertical))	USPAT	2004/08/25 07:38
2	17414	(unit adj3 (horizontal or vertical))	USPAT	2004/08/25 07:39
3	3869	(unit adj (horizontal or vertical))	USPAT	2004/08/25 07:39
4	3235	((unit adj (horizontal or vertical))) and sum$5	USPAT	2004/08/25 07:39
5	124	(((unit adj (horizontal or vertical))) and sum$5) and interpolat$3	USPAT	2004/08/25 07:39
6	67	((((unit adj (horizontal or vertical))) and sum$5) and interpolat$3) and pixel	USPAT	2004/08/25 07:40
7	40	(((((unit adj (horizontal or vertical))) and sum$5) and interpolat$3) and pixel) and (pixel$3 near4 interpolat$5)	USPAT	2004/08/25 07:46
8	594	(motion adj3 vector) and (pixel near4 interpolat$5)	USPAT	2004/08/25 07:47
9	120	((motion adj3 vector) and (pixel near4 interpolat$5)) and (sub near3 pixel)	USPAT	2004/08/25 07:47
10	586	((motion adj3 vector) and (pixel near4 interpolat$5)) and sum$6	USPAT	2004/08/25 07:47
11	117	(((motion adj3 vector) and (pixel near4 interpolat$5)) and (sub near3 pixel)) and sum$6	USPAT	2004/08/25 07:48
12	43	((((motion adj3 vector) and (pixel near4 interpolat$5)) and (sub near3 pixel)) and sum$6) and (weight$4 near4 sum$6)	USPAT	2004/08/25 07:48

L Number	Hits	Search Text	DB	Time stamp
31	192	half near4 (pixel or pel) and (quarter near4 (pixel or pel))	USPAT	2004/08/26 07:43
32	101	(half near4 (pixel or pel) and (quarter near4 (pixel or pel))) and interpolat$5	USPAT	2004/08/26 07:42
33	59	((half near4 (pixel or pel) and (quarter near4 (pixel or pel))) and interpolat$5) and weight$4	USPAT	2004/08/26 07:43
34	27	(half near4 (pixel or pel) and (quarter near4 (pixel or pel))) near10 interpolat$5	USPAT	2004/08/26 07:43
35	16	((half near4 (pixel or pel) and (quarter near4 (pixel or pel))) near10 interpolat$5) and weight$4	USPAT	2004/08/26 10:50
36	411	quarter near4 (pixel or pel)	USPAT	2004/08/26 10:50
37	42	(quarter near4 (pixel or pel)) near10 interpolat$4	USPAT	2004/08/26 10:50
38	17	((quarter near4 (pixel or pel)) near10 interpolat$4) and search	USPAT	2004/08/26 10:55
39	25	((quarter near4 (pixel or pel)) near10 interpolat$4) not (((quarter near4 (pixel or pel)) near10 interpolat$4) and search)	USPAT	2004/08/26 10:56

Nokia Exhibit 2004, p. 302
Amazon.com v. Nokia
IPR2024-01141

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HANEY, MATTHEW J

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TITLE OF INVENTION: METHOD FOR SUB-PIXEL VALUE INTERPOLATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$300	$1630	12/09/2004

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A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is n claiming SMALL ENTITY status, check box 5a on Part B - Fee Transmittal and pay the PUBLICATION FEE (if required) and 1 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) w your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when du

Nokia Exhibit 2004, p. 303
Amazon.com v. Nokia
IPR2024-01141

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed wh appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2512 7590 09/09/2004

PERMAN & GREEN
425 POST ROAD
FAIRFIELD, CT 06824

Note: A certificate of mailing can only be used for domestic mailings of Fee(s) Transmittal. This certificate cannot be used for any other accompany papers. Each additional paper, such as an assignment or formal drawing, m have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the Un States Postal Service with sufficient postage for first class mail in an envel addressed to the Mail Stop ISSUE FEE address above, or being facsim transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's na
(Signat
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,608	09/17/2001	Marta Karczewicz	442-010567-US(PAR)	8282

TITLE OF INVENTION: METHOD FOR SUB-PIXEL VALUE INTERPOLATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$300	$1630	12/09/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
HANEY, MATTHEW J	2613	375-240170

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Governm

4a. The following fee(s) are enclosed:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s):

❑ A check in the amount of the fee(s) is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other part interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to proc an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to comp this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 14 Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Nokia Exhibit 2004, p. 304
Amazon.com v. Nokia
IPR2024-01141

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,608	09/17/2001	Marta Karczewicz	442-010567-US(PAR)	8282

2512 7590 09/09/2004

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FAIRFIELD, CT 06824

EXAMINER	
HANEY, MATTHEW J	
ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 09/09/2004

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 489 day(s). If the issue fee is paid on the date that is three months after t mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a ha months) after the mailing date of this notice, the Patent Term Adjustment will be 489 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date th determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retriev (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Nokia Exhibit 2004, p. 305
Amazon.com v. Nokia
IPR2024-01141

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,608	09/17/2001	Marta Karczewicz	442-010567-US(PAR)	8282

2512 7590 09/09/2004

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FAIRFIELD, CT 06824

EXAMINER	
HANEY, MATTHEW J	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 09/09/2004

Notice of Fee Increase on October 1, 2004

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after October 1, 2004, then t amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" because an increase in fe effective on October 1, 2004 is anticipated. See Revision of Patent Fees for Fiscal Year 2005; Proposed Rule, 69 Fe Reg. 25861, 25863, 25864 (May 10, 2004).

The current fee schedule is accessible from WEB site (http://www.uspto.gov/main/howtofees.htm).

If the fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due" but not the correct amount in vie of the fee increase, a "Notice of Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processi delays associated with mailing of a "Notice of Pay Balance of Issue Fee," if the response to the Notice of Allowan is to be filed on or after October 1, 2004 (or mailed with a certificate of mailing on or after October 1, 2004), t issue fee paid should be the fee that is required at the time the fee is paid. See Manual of Patent Examining Procedu (MPEP), Section 1306 (Eighth Edition, Rev. 2, May 2004). If the issue fee was previously paid, and the response the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue f now due, then the difference between the issue fee amount at the time the response is filed and the previously-pa issue fee should be paid. See MPEP Section 1308.01.

Effective October 1, 2004, 37 CFR 1.18 is proposed to be amended by revising paragraphs (a) through (c) to read set forth below. As stated above, the final fee may be a different amount, and applicant should check the WEB s given above when paying the fee.

Section 1.18 Patent post allowance (including issue) fees.

(a) Issue fee for issuing each original or reissue patent,
except a design or plant patent:
By a small entity (Sec. 1.27(a)) $670.00
By other than a small entity $1,340.00
(b) Issue fee for issuing a design patent:
By a small entity (Sec. 1.27(a)) $245.00
By other than a small entity $490.00
(c) Issue fee for issuing a plant patent:
By a small entity (Sec. 1.27(a)) $325.00
By other than a small entity $650.00

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of t Office of Patent Publication at (703) 305-8283.

Nokia Exhibit 2004, p. 306
Amazon.com v. Nokia
IPR2024-01141

Notice of Allowability	Application No.	Applicant(s)	
	09/954,608	KARCZEWICZ ET AL.	
	Examiner	Art Unit	
	Matthew Haney	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are 1-51.

3. ☒ The drawings filed on 9/17/01 are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Nokia Exhibit 2004, p. 307
Amazon.com v. Nokia
IPR2024-01141

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-51 are allowed.

2. The following is an examiner's statement of reasons for allowance: The examiner was unable to find prior art that showed the limitations discussed in the claims. The examiner considered the art in his own search as well as the art by applicant.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Haney whose telephone number is 703-305-4915. The examiner can normally be reached on M-Th (7-4:30), Every Other Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Nokia Exhibit 2004, p. 308
Amazon.com v. Nokia
IPR2024-01141

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Haney
Examiner
Art Unit 2613

mjh

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Notice of References Cited	Application/Control No. 09/954,608	Applicant(s)/Patent Under Reexamination KARCZEWICZ ET AL.	
	Examiner Matthew Haney	Art Unit 2613	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,594,813	01-1997	Fandrianto et al.	382/236
	B	US-5,852,468 A	12-1998	Okada, Hidefumi	348/272
	C	US-6,381,279 B1	04-2002	Taubman, David S.	375/240.18
	D	US-5,754,240	05-1998	Wilson, William Brent	375/240.15
	E	US-5,485,279	01-1996	Yonemitsu et al.	375/240.14
	F	US-6,104,753	08-2000	Kim et al.	375/240.16
	G	US-6,714,593	03-2004	Benzler et al.	375/240.16
	H	US-4,816,913	03-1989	Harney et al.	375/240.08
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lappalainen, Ville, Performance analysis of Intel MMX technology for an H.263 video H.263 video encoder, 1998, ACM Press, Pages 309-314
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Nokia Exhibit 2004, p. 310
Amazon.com v. Nokia
IPR2024-01141

INFORMATION DISCLOSURE CITATION FORM FOR PATENT APPLICATION (FORM PTO-1449) (Substitute)	Docket No.: 442-010567-US(PAR) Serial No.: 09/954,608 Applicant(s): KARCZEWICZ et al. Filing Date: 9/17/01 Group: 2631

OIPE JC81 JAN 13 2003 PATENT & TRADEMARK OFFICE

U.S. PATENTS

Initials	Patent Number	Issue Date	Name	Class	Sub-class	Filing date
MJH	5,521,642	5/28/96	Park	348	409	10/7/93
MJH	6,219,464 B1	4/17/01	Greggain et al.	382	298	8/24/99
MJH	5,570,436	10/29/96	Fukushima et al.	382	300	12/8/94
MJH	5,568,597	10/22/96	Nakayama et al.	395	132	5/20/94
MJH	6,252,576 B1	6/26/01	Nottingham	345	127	8/6/98
MJH	5,901,248	5/4/99	Fandrianto et al.	382	236	8/6/96

RECEIVED
JAN 14 2003
Technology Center 2600

U.S. PATENT PUBLICATIONS

Initials	Publication No.	Pub. Date	Name	Class	Sub-class	Filing Date
MJH	2002/0064229	5/30/02	Nakaya	375	240.17	11/28/01

FOREIGN PATENT DOCUMENTS

Initials	Document Number	Date	Country	Name	Translation? Yes/No/n/a
MJH	0576290 A2	12/29/93	Europe	Sony Corporation	n/a
MJH	2205707	12/14/88	United Kingdom	Sony Corporation	n/a

OTHER DOCUMENTS (Title, Author, Date, Pages, Etc., if known)

Examiner's Signature: Matthew Henry Date Considered: 8/26/04

Initial if reference was considered, whether or not citation is in conformance with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).

Customer No.: 2512

Nokia Exhibit 2004, p. 311
Amazon.com v. Nokia
IPR2024-01141

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

BIBDATASHEET

CONFIRMATION NO. 8282

Bib Data Sheet

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/954,608	09/17/2001 RULE	375	2613	442-010567-US (PAR)

APPLICANTS

Marta Karczewicz, Irving, TX;

Antti Olli Hallapuro, Tampere, FINLAND;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 10/25/2001

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
☐ yes ☑ no	COUNTRY	DRAWING	CLAIMS	CLAIMS
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance	TX	26	49	13
Verified and Acknowledged Examiner's Signature MJH Initials				

ADDRESS
2512
PERMAN & GREEN
425 POST ROAD
FAIRFIELD , CT
06824

TITLE
Method for sub-pixel value interpolation

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees
RECEIVED 2134	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

Nokia Exhibit 2004, p. 312
Amazon.com v. Nokia
IPR2024-01141

Issue Classification	Application No.	Applicant(s)	
	09/954,608	KARCZEWICZ ET AL.	
	Examiner	Art Unit	
	Matthew Haney	2613	

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
375	240.17	~~375~~	~~240.17~~						
INTERNATIONAL CLASSIFICATION									
H 0 4 N	7/12								
	/								
	/								
	/								
	/								

Matthew Haney 8/26/04
(Assistant Examiner) (Date)

9/7/04
(Legal Instruments Examiner) (Date)

9/7/04
(Primary Examiner) (Date)

Total Claims Allowed: 51

O.G. Print Claim(s)

O.G. Print Fig.

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
	3		33		63		93		123		153		183
	4		34		64		94		124		154		184
	5		35		65		95		125		155		185
	6		36		66		96		126		156		186
	7		37		67		97		127		157		187
	8		38		68		98		128		158		188
	9		39		69		99		129		159		189
	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
	21		51		81		111		141		171		201
	22		52		82		112		142		172		202
	23		53		83		113		143		173		203
	24		54		84		114		144		174		204
	25		55		85		115		145		175		205
	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

Nokia Exhibit 2004, p. 313
Amazon.com v. Nokia
IPR2024-01041

Index of Claims

Application No.	Applicant(s)	
09/954,608	KARCZEWICZ ET AL.	
Examiner	**Art Unit**	
Matthew Haney	2613	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date									
Final	Original	8/26/04									
1	1	=									
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Claim		Date									
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Nokia Exhibit 2004, p. 314
Amazon.com v. Nokia
IPR2024-01141

Search Notes	Application No.	Applicant(s)	
	09/954,608	KARCZEWICZ ET AL.	
	Examiner	Art Unit	
	Matthew Haney	2613	

SEARCHED			
Class	Subclass	Date	Examiner
375	240.17	8/26/2004	MJH
382	236	8/26/2004	MJH
375	240.16	8/26/2004	MJH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
375	**240.17**	8/26/2004	**MJH**

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached Search History	8/26/2004	MJH
IEEE search performed : interpolation <and> quarter <and> search	8/26/2004	MJH
IEEE search performed : interpolation <and> half <and> search	8/26/2004	MJH
ACM Digital Library searched: interpolation and half and pixel and search	8/26/2004	MJH
ACM Digital Library searched: interpolation and quarter and pixel and search	8/26/2004	MJH

PA IDC

QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	09954608	Prepared by	DA	Tracking Number	20011686
Examiner-GAU	Kelley - 2613	Date	10-12-04	Week Date	9-13-04
		No. of queries	2	IFW	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE 1. Claim 26 depends on Claims 24 & 25

2. Claim 44 depends on Claims 39 and 40.

THANK YOU

initials DA

RESPONSE

Nokia Exhibit 2004, p. 316
Amazon.com v. Nokia
IPR2024-01141

initials

E-5 (Rev. 10/01/02)

OIPE JC
OCT 25 2004
U.S. PATENT & TRADEMARK OFFICE

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed wh appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2512 7590 09/09/2004

PERMAN & GREEN
425 POST ROAD
FAIRFIELD, CT 06824

10/26/2004 HDEMESS2 00000038 09954608

01 FC:1501 1370.00 OP
02 FC:1504 300.00 OP
03 FC:8001 30.00 OP

Note: A certificate of mailing can only be used for domestic mailings of Fee(s) Transmittal. This certificate cannot be used for any other accompany papers. Each additional paper, such as an assignment or formal drawing, m have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the Un States Postal Service with sufficient postage for first class mail in an envel addressed to the Mail Stop ISSUE FEE address above, or being facsim transmitted to the USPTO (703) 746-4000, on the date indicated below.

Meaghan Baye	(Depositor's na
Meaghan Baye	(Signat
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,608	09/17/2001	Marta Karczewicz	442-010567-US(PAR)	8282

TITLE OF INVENTION: METHOD FOR SUB-PIXEL VALUE INTERPOLATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	~~$1330~~ $1370	$300	~~$1630~~ $1670	12/09/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
HANEY, MATTHEW J	2613	375-240170

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Perman & Green, LLP
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Nokia Corporation
(B) RESIDENCE: (CITY and STATE OR COUNTRY): FIN-02150 Espoo Finland

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Governm

4a. The following fee(s) are enclosed:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies _____

4b. Payment of Fee(s):
☒ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment Deposit Account Number 16-1350 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other part interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 18 October 2004

Typed or printed name Geza C. Ziegler, Jr. Registration No. 44,004

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to proc an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to comp this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 14 Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Nokia Exhibit 2004 of 317
Amazon.com v. Nokia
IPR2024-01141

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,608	09/17/2001	Marta Karczewicz	442-010567-US(PAR)	8282

2512 7590 03/14/2005

PERMAN & GREEN
425 POST ROAD
FAIRFIELD, CT 06824

EXAMINER	
HANEY, MATTHEW J	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Notice of Allowability	Application No.	Applicant(s)	
	09/954,608	KARCZEWICZ ET AL.	
	Examiner	Art Unit	
	Matthew Haney	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-51*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Nokia Ex. 1004, p. 319
Amazon.com v. Nokia
IPR2024-01141

DETAILED ACTION

The application has been amended as follows:

Change Claim 26, Line 1 from "and" to --or--.

Change Claim 41, Line 1 from "and" to --or--.

Allowable Subject Matter

1. Claims 1-51 are allowed.

2. The following is an examiner's statement of reasons for allowance: The examiner was unable to find prior art that showed the limitations discussed in the claims. The examiner considered the art in his own search as well as the art by applicant.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Haney whose telephone number is 703-305-4915. The examiner can normally be reached on M-Th (7-4:30), Every Other Friday Off.

Nokia Exhibit 2004, p. 320
Amazon.com v. Nokia
IPR2024-01141

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Haney
Examiner
Art Unit 2613

mjh

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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HANEY

BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 8282

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/954,608	09/17/2001 RULE	375	2613	442-010567-US (PAR)

APPLICANTS

Marta Karczewicz, Irving, TX;

Antti Olli Hallapuro, Tampere, FINLAND;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 10/25/2001

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
☐ yes ☑ no	COUNTRY	DRAWING	CLAIMS	CLAIMS
35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance	TX	26	49	13
Verified and Acknowledged Examiner's Signature MJH Initials				

ADDRESS
2512
PERMAN & GREEN
425 POST ROAD
FAIRFIELD , CT
06824

TITLE
Method for sub-pixel value interpolation

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees
RECEIVED 2134	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

Nokia Exhibit 2004, p. 322
Amazon.com v. Nokia
IPR2024-01141

Figure 14a shows a notation for describing pixel and sub-pixel locations specific to the invention;

Figure 14b shows interpolation of a half resolution sub-pixels according to the invention;

Figure 14c shows interpolation of a half resolution sub-pixels according to the invention;

Figure 15 shows possible choices of diagonal interpolation for sub-pixels;

Figure 16 shows the half resolution sub-pixel values required to calculate other half resolution sub-pixel values;

Figure 17a shows the half resolution sub-pixel values that must be calculated in order to interpolate values for quarter resolution sub-pixels in an image block using the interpolation method of TML5;

Figure 17b shows the half resolution sub-pixel values that must be calculated in order to interpolate values for quarter resolution sub-pixels in an image block using the interpolation method according to the invention;

Figures 18a shows the numbers of half resolution sub-pixels that must be calculated in order to obtain values for quarter resolution sub-pixels within an image block using the sub-pixel value interpolation method according to TML5;

Figure 18b shows the numbers of half resolution sub-pixels that must be calculated in order to obtain values for quarter resolution sub-pixels within an image block using the sub-pixel value interpolation method according to the invention;

Figure 19 shows a numbering scheme for each of the 15 sub-pixel positions;

Figure 20 shows nomenclature used to describe pixels, half resolution sub-pixels, quarter resolution sub-pixels and eighth resolution sub-pixels

Figure 21a shows the diagonal direction to be used in the interpolation of each eighth resolution sub-pixel in an embodiment of the invention;

Nokia Exhibit 2004, p. 323
Amazon.com v. Nokia
IPR2024-01141

PA IRW

QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	09954608	Prepared by	AP	Tracking Number	20011686
Examiner-GAU	Kelley - 2613	Date	10-12-04	Week Date	9-13-05
		No. of queries	2	IFW	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION
a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS
a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
k. Other

MESSAGE 1. Claim 26 depends on Claims 24 & 25

2. Claim 44 depends on Claims 39 and 40.

THANK YOU

initials AP

RESPONSE The examiner ant with the NOA on 3-14-05 corrected the problem

initials DW

E-5 (Rev. 10/01/02)

Nokia Exhibit 2004, p. 324
Amazon.com v. Nokia
IPR2024-01141

Notice of Allowability	Application No. 09/954,608	Applicant(s) KARCZEWICZ ET AL.	
	Examiner Matthew Haney	Art Unit 2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
2. ☒ The allowed claim(s) is/are *1-51*.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
CENTER 2600

Nokia Exhibit 2004, p. 325
Amazon.com v. Nokia
IPR2024-01141

DETAILED ACTION

The application has been amended as follows:

Change Claim 26, Line 1 from "and" to --or--.

Change Claim 41, Line 1 from "and" to --or--.

Allowable Subject Matter

1. Claims 1-51 are allowed.

2. The following is an examiner's statement of reasons for allowance: The examiner was unable to find prior art that showed the limitations discussed in the claims. The examiner considered the art in his own search as well as the art by applicant.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Haney whose telephone number is 703-305-4915. The examiner can normally be reached on M-Th (7-4:30), Every Other Friday Off.

Nokia Exhibit 2004, p. 326
Amazon.com v. Nokia
IPR2024-01141

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Haney
Examiner
Art Unit 2613

mjh

CHRIS KELLEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,608	09/17/2001	Marta Karczewicz	442-010567-US(PAR)	8282

2512 7590 08/08/2005

PERMAN & GREEN
425 POST ROAD
FAIRFIELD, CT 06824

EXAMINER	
HANEY, MATTHEW J	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

NOTICE OF DRAWING INCONSISTENCY WITH SPECIFICATION

The drawings filed 9/17/01 have been received. However, an inconsistency exists between the drawings and the Brief Description of the Drawings in the specification.

Figures 9, 10 are listed in the Brief Description of the Drawings in the specification but not contained in the Drawings.

Figures _____ are contained in the Drawings but not listed in the Brief Description of the Drawings in the specification.

Applicant is required to correct the above-noted inconsistency within a time period of **ONE MONTH or THIRTY (30) DAYS, whichever is longer,** from the mailing date of this Notice, or within the time remaining in the time period set forth in the Notice of Allowability (Form PTOL-37) to file corrected drawings, whichever is longer. **NO EXTENSION OF THIS TIME PERIOD MAY BE GRANTED UNDER EITHER 37 CFR 1.136 (a) OR (b)**

Failure to correct the above noted inconsistency will result in **abandonment** of the application.

The file will be held in the Publishing Division to await the correction of the inconsistency.

Return Corrected Drawings/Specification to:
Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450

Alexandria, VA 22313-1450

Office of Patent Publication/Publishing Division
Customer Service: 703-308-6789
1-888-786-0101

FORM PTO-1631 (REV. 10-03)

Nokia Exhibit 2004, p. 329
Amazon.com v. Nokia
IPR2024-01141

Facsimile Message From

Law Offices
PERMAN & GREEN, LLP
425 Post Road
Fairfield, Connecticut 06824 USA
Facsimile Number: (203) 255-5170
Telephone Number: (203) 259-1800

RECEIVED
CENTRAL FAX CENTER
AUG 17 2005

TO: Mail Stop Issue Fee FAX NO: (571) 273-8300

DATE: August 17, 2005

FROM: Geza C. Ziegler, Jr.

RE: P&G Reference: 442-010567-US (PAR)

Number of Pages, including this sheet, being transmitted: 7

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Nokia Exhibit 2004, p. 330
Amazon.com v. Nokia
IPR2024-01141

PAGE 1/7 * RCVD AT 8/17/2005 3:52:31 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID: * DURATION (mm-ss):01-08

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(s):	Karczewicz et al.		
SERIAL NO.:	09/954,608	ART UNIT:	2613
FILING DATE:	03/25/2005	EXAMINER:	Haney, Matthew J.
TITLE:	METHOD FOR SUB-PIXEL VALUE INTERPOLATION		
ATTORNEY DOCKET NO.:	442-010567-US (PAR)		

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE OF DRAWING INCONSISTENCY WITH SPECIFICATION

I. INTRODUCTION

This is in response to the Notice mailed August 8, 2005 in regard to the above-identified patent application.

Please amend the Application as follows:

Nokia Exhibit 2004, p. 331
Amazon.com v. Nokia
IPR2024-01141

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III. IN THE SPECIFICATION

Please replace the section beginning on page 40, line 4, through page 42, line 5 as rewritten below:

Brief Description of the Figures

An embodiment of the invention will now be described by way of example only with reference to the accompanying drawings in which:

Figure 1 shows a video encoder according to the prior art;

Figure 2 shows a video decoder according to the prior art;

Figure 3 shows the types of frames used in video encoding;

Figures 4a, 4b, and 4c show steps in block-matching;

Figure 5 illustrates the process of motion estimation to sub-pixel resolution;

Figure 6 shows a terminal device comprising video encoding and decoding equipment in which the method of the invention may be implemented;

Figure 7 shows a video encoder according an embodiment of the present invention;

Figure 8 shows a video decoder according to an embodiment of the present invention;

~~Figures 9 and 10 have not been used and any such figures should be disregarded;~~

Figure 11 shows a schematic diagram of a mobile telecommunications network according to an embodiment of the present invention;

Figure 12a shows a notation for describing pixel and sub-pixel locations specific to TML5;

Figure 12b shows interpolation of a half resolution sub-pixels;

Figure 12c shows interpolation of a half resolution sub-pixels;

Nokia Exhibit 2004, p. 332
Amazon.com v. Nokia
IPR2024-01141

PAGE 4/7 * RCVD AT 8/17/2005 3:52:31 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID: * DURATION (mm-ss):01-08

Page 332 of 350

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Figure 13a shows a notation for describing pixel and sub-pixel locations specific to TML6;

Figure 13b shows interpolation of a half resolution sub-pixels;

Figure 13c shows interpolation of a half resolution sub-pixels;

Figure 14 shows a notation for describing pixel and sub-pixel locations specific to the invention;

Figure 14b shows interpolation of a half resolution sub-pixels according to the invention;

Figure 14c shows interpolation of a half resolution sub-pixels according to the invention;

Figure 15 shows possible choices of diagonal interpolation for sub-pixels;

Figure 16 shows the half resolution sub-pixel values required to calculate other half resolution sub-pixel values;

Figure 17a shows the half resolution sub-pixel values that must be calculated in order to interpolate values for quarter resolution sub-pixels in an image block using the interpolation method of TML5;

Figure 17b shows the half resolution sub-pixel values that must be calculated in order to interpolate values for quarter resolution sub-pixels in an image block using the interpolation method according to the invention;

Figures 18a shows the numbers of half resolution sub-pixels that must be calculated in order to obtain values for quarter resolution sub-pixels within an image block using the sub-pixel value interpolation method according to TML5;

Figure 18b shows the numbers of half resolution sub-pixels that must be calculated in order to obtain values for quarter resolution sub-pixels within an image block using the sub-pixel value interpolation method according to the invention;

Figure 19 shows a numbering scheme for each of the 15 sub-pixel positions;

Nokia Exhibit 2004, p. 333
Amazon.com v. Nokia
IPR2024-01141

PAGE 5/7 * RCVD AT 8/17/2005 3:52:31 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID: * DURATION (mm-ss):01-08

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Page 333 of 350

II. DRAWINGS

In the drawings, please cancel Figures 9 and 10.

Nokia Exhibit 2004, p. 334
Amazon.com v. Nokia
IPR2024-01141

PAGE 3/7 * RCVD AT 8/17/2005 3:52:31 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID: * DURATION (mm-ss):01-08

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Page 334 of 360

Figure 20 shows nomenclature used to describe pixels, half resolution sub-pixels, quarter resolution sub-pixels and eighth resolution sub-pixels

Figure 21a shows the diagonal direction to be used in the interpolation of each eighth resolution sub-pixel in an embodiment of the invention;

Figure 21b shows the diagonal direction to be used in the interpolation of each eighth resolution sub-pixel in another embodiment of the invention; and

Figure 22 shows nomenclature used to describe eighth resolution sub-pixels within an image.

Nokia Exhibit 2004, p. 335
Amazon.com v. Nokia
IPR2024-01141

PAGE 6/7 * RCVD AT 8/17/2005 3:52:31 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID: * DURATION (mm-ss):01-08

Page 335 of 350

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IV. REMARKS

The application drawings do not include figures 9 and 10. Applicant thus proposes to cancel the drawings.

The specification is amended to delete the reference to Figures 9 and 10.

The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,

Geza C. Ziegler, Jr.
Reg. No. 44,004

17 August 2005
Date

Perman & Green, LLP
425 Post Road
Fairfield, CT 06824
(203) 259-1800
Customer No.: 2512

CERTIFICATE OF FACSMILE

I hereby certify that this correspondence is being transmitted by fax to 571-273-8300, addressed to Mail Stop ISSUE FEE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: August 17, 2005 Signature: Meaghan Bay
Person Making Deposit

Nokia Exhibit 2004, p. 336
Amazon.com v. Nokia
IPR2024-01141

PAGE 7/7 * RCVD AT 8/17/2005 3:52:31 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID: * DURATION (mm-ss):01-08

Page 336 of 350

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,608	09/17/2001	Marta Karczewicz	442-010567-US(PAR)	8282

2512 7590 08/31/2005

PERMAN & GREEN
425 POST ROAD
FAIRFIELD, CT 06824

EXAMINER	
HANEY, MATTHEW J	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 08/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Response to Rule 312 Communication	Application No.	Applicant(s)	
	Examiner	Art Unit	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address---

1. [X] The amendment filed on 8-17-05 under 37 CFR 1.312 has been considered, and has been:

a) [X] entered.

b) [ ] entered as directed to matters of form not affecting the scope of the invention.

c) [ ] disapproved because the amendment was filed after the payment of the issue fee.

Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) [ ] disapproved. See explanation below.

e) [ ] entered in part. See explanation below.

Natasha Kane
Publishing Division

Nokia Exhibit 2004, p. 338
Amazon.com v. Nokia
IPR2024-01141

OIPE IAP93 APR 25 2006 PATENT & TRADEMARK OFFICE

09/954608

C of C

PATENT

Practitioner's Docket No. 982-010567-US (PAR)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number: 6,950,469 B2

Issued: September 27, 2005

Patentee: Karczewicz et al.

Title: METHOD FOR SUB-PIXEL VALUE INTERPOLATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

LETTER CALLING ATTENTION TO ERROR IN PATENT

It is respectfully requested that this letter, calling attention to the following error(s) in this patent, be made of record in the patent file:

First page, Col. 1, (Foreign Patent Documents), line 1, delete "0573290" and insert - - 0576290 - -.

Column 48, line 17, claim 23, delete "1/2X" and insert - - $1/2^{x}$ - -.

Column 50, line 61, claim 35, after "location" delete "is required".

Column 50, line 64. claim 35, delete "sub-pixel" and insert - - sub-pixels - -.

Column 51, line 45, claim 42, after "location" delete "is required".

Column 52, line 12, claim 46, after "location" delete "is required".

Column 52, line 29, claim 49, delete "telecommunications" and insert - - telecommunication - -.

Column 52, line 33, claim 49, delete "for coding" before "an image".

Column 52, line 48, claim 49, after "location" delete "is required".

Certificate
MAY 1 0 2006
of Correction

Nokia Exhibit 2004, p. 339
Amazon.com v. Nokia
IPR2024-01141

SIGNATURE OF PRACTITIONER

Reg. No. 44,004

Geza C. Ziegler, Jr.
(type or print name of practitioner)

Tel. No. (203) 259-1800

425 Post Road
Address

Customer No.: 2512

Fairfield, CT 06824

NOTE: Letters which merely call attention to errors in patents, with a request that the letter be made of record in the patented file, will not be acknowledged" MPEP § 1480.

(Letter Calling Attention to Error in Patent [14-4)

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:16-cv-1440	12/21/2016	Eastern District of Texas

PLAINTIFF	DEFENDANT
Nokia Technologies OY and Alcatel-Lucent USA Inc.	Apple Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,680,974	1/20/2004	Alcatel-Lucent USA Inc.
2	6,711,211	3/23/2004	Nokia Technologies Oy
3	6,856,701	2/15/2005	Nokia Technologies Oy
4	6,950,469	9/27/2005	Nokia Technologies Oy
5	6,968,005	11/22/2005	Nokia Technologies Oy

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,532,808	5/12/2009	Nokia Technologies Oy
2 8,036,273	10/11/2011	Nokia Technologies Oy
3 8,144,764	3/27/2012	Nokia Technologies Oy
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

Nokia Exhibit 2004, p. 341
Amazon.com v. Nokia
IPR2024-01141

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

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Nokia Technologies OY and Alcatel-Lucent USA Inc.	Apple Inc.

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2	6,711,211	3/23/2004	Nokia Technologies Oy
3	6,856,701	2/15/2005	Nokia Technologies Oy
4	6,950,469	9/27/2005	Nokia Technologies Oy
5	6,968,005	11/22/2005	Nokia Technologies Oy

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2 8,036,273	10/11/2011	Nokia Technologies Oy
3 8,144,764	3/27/2012	Nokia Technologies Oy
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Nokia Exhibit 2004, p. 342
Amazon.com v. Nokia
IPR2024-01141

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
5:19-CV-427-BO	9/25/2019	Eastern District of North Carolina

PLAINTIFF	DEFENDANT
Nokia Technologies Oy	Lenovo (Shanghai) Electronics Technology Co., Ltd. et al

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,856,701		
2	6,950,469		
3	6,968,005		
4	7,263,125		
5	7,280,599		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,532,808		
2 7,724,818		
3 8,036,273		
4 8,144,764		
5 9,800,891		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
PETER A. MOORE, JR.	Joanne Rudd, Deputy	9/26/2019

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Nokia Exhibit 2004, p. 343
Amazon.com v. Nokia
IPR2024-01141

AO 120 (Rev. 08/10)

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
5:19-CV-427-BO	9/25/2019	Eastern District of North Carolina

PLAINTIFF	DEFENDANT
Nokia Technologies Oy	Lenovo (Shanghai) Electronics Technology Co., Ltd. et al

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1	6,856,701		
2	6,950,469		
3	6,968,005		
4	7,263,125		
5	7,280,599		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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2	7,724,818		
3	8,036,273		
4	8,144,764		
5	9,800,891		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
PETER A. MOORE, JR.	Joanne Rudd, Deputy	9/26/2019

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Copy 3—Upon termination of action, mail this copy to Director
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Nokia Exhibit 2004, p. 344
Amazon.com v. Nokia
IPR2024-01141

Trials@uspto.gov
571.272.7822

Paper No. 21
Entered: April 27, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LENOVO (UNITED STATES) INC.,
Petitioner,

v.

NOKIA TECHNOLOGIES OY,
Patent Owner.

IPR2020-01685, IPR2021-00035, IPR2021-00036 (Patent 6,950,469 B2);
IPR2021-00037, IPR2021-00038, IPR2021-00039 (Patent 7,280,599 B2);
IPR2021-00040, IPR2021-00041, IPR2021-00042,
IPR2021-00043 (Patent 8,036,273 B2)[1]

Before BARBARA A. PARVIS, JENNIFER MEYER CHAGNON, and MONICA S. ULLAGADDI, *Administrative Patent Judges.*

CHAGNON, *Administrative Patent Judge.*

DECISION
Settlement Prior to Institution of Trial
37 C.F.R. § 42.74

[1] This Order applies to each of the listed proceedings. The parties are not authorized to use this style heading for any subsequent papers.

Nokia Exhibit 2004, p. 345
Amazon.com v. Nokia
IPR2024-01141

I. INTRODUCTION

With the Board's authorization, Petitioner and Patent Owner (collectively, "the Parties") filed a Joint Motion to terminate each of the above-identified proceedings. Paper 18[2] ("Mot."). Along with each Joint Motion, the Parties filed a copy of a confidential Settlement Agreement (Ex. 1020) and Patent Agreement Terms (Ex. 1021 ("Term Sheet")), as well as a Joint Request to Treat the Settlement Agreement as Business Confidential Information pursuant to 35 U.S.C. § 317(b) and 37 C.F.R. § 42.74(c) (Paper 20 ("Joint Request")).

II. DISUCSSION

In the Joint Motion, the Parties represent that they "have executed a settlement agreement that resolves all of their disputes concerning U.S. Patent Nos. 6,950,469, 7,280,599, and 8,036,273." Mot. 3. The Parties further represent that "a true and correct copy of the Litigation Settlement Agreement has been filed." *Id.* at 4; Ex. 1020. The Settlement Agreement references a Term Sheet, which also has been filed. Mot. 4; Ex. 1021. The Parties note that the Settlement Agreement "references another potential agreement, but the parties have not entered into that agreement as of this filing, and there are no other agreements between the parties." Mot. 4. The Parties, thus, confirm "that the documents filed as Exhibits 1020 [(i.e., the Settlement Agreement)] and 1021 [(i.e., the Term Sheet)] represent all

[2] For purposes of expediency, we cite to Papers and Exhibits filed in IPR2020-01685. Corresponding Papers and Exhibits were filed in each of the captioned proceedings, as shown in the Appendix.

agreements made in connection with, or in contemplation of, the termination of this proceeding. All such agreements have been filed with the Board as required by 35 U.S.C. § 317(b) and 37 C.F.R. § 42.74(b)." *Id.*

This proceeding is still in its preliminary stages. We have not entered a decision on whether to institute *inter partes* review in these proceedings. In view of the early stage of these proceedings and the settlement between the parties, we determine that good cause exists to terminate these proceedings with respect to the parties.

We also have reviewed the Settlement Agreement and Term Sheet, and we determine that the Settlement Agreement and Term Sheet contain business confidential information regarding the terms of the settlement, and that good cause exists to treat the Settlement Agreement and Term Sheet as business confidential information under 37 C.F.R. § 42.74(c).

This Order does not constitute a final written decision pursuant to 35 U.S.C. § 318(a).

According, it is

ORDERED that the parties' Joint Request to treat the Settlement Agreement and Term Sheet as business confidential information under 37 C.F.R. § 42.74(c) is *granted* in each of the captioned proceedings, and the Settlement Agreement and Term Sheet shall be kept separate from the files of respective U.S. Patent Nos. 6,950,469 B2, 7,280,599B2, and 8,036,273 B2, and made available only to Federal Government agencies on written request, or to any person on a showing of good cause, pursuant to 35 U.S.C. § 317(b) and 37 C.F.R. § 42.74(c); and

IPR2020-01685, IPR2021-00035, IPR2021-00036 (Patent 6,950,469 B2);
IPR2021-00037, IPR2021-00038, IPR2021-00039 (Patent 7,280,599 B2);
IPR2021-00040, IPR2021-00041, IPR2021-00042,
IPR2021-00043 (Patent 8,036,273 B2)

FURTHER ORDERED that the parties' Joint Motion to Terminate is *granted* in each of the captioned proceedings; the Petition in each of IPR2020-01685, IPR2021-00035, IPR2021-00036, IPR2021-00037, IPR2021-00038, IPR2021-00039, IPR2021-00040, IPR2021-00041, IPR2021-00042, and IPR2021-00043 is dismissed; and the captioned proceedings are *terminated.*

Nokia Exhibit 2004, p. 348
Amazon.com v. Nokia
IPR2024-01141

IPR2020-01685, IPR2021-00035, IPR2021-00036 (Patent 6,950,469 B2);
IPR2021-00037, IPR2021-00038, IPR2021-00039 (Patent 7,280,599 B2);
IPR2021-00040, IPR2021-00041, IPR2021-00042,
IPR2021-00043 (Patent 8,036,273 B2)

APPENDIX

Proceeding	Joint Motion	Joint Request	Settlement Agreement	Term Sheet
IPR2020-01685	Paper 18	Paper 20	Ex. 1020	Ex. 1021
IPR2021-00035	Paper 16	Paper 17	Ex. 1120	Ex. 1121
IPR2021-00036	Paper 15	Paper 17	Ex. 1220	Ex. 1221
IPR2021-00037	Paper 15	Paper 16	Ex. 1018	Ex. 1019
IPR2021-00038	Paper 15	Paper 16	Ex. 1119	Ex. 1120
IPR2021-00039	Paper 15	Paper 16	Ex. 1218	Ex. 1219
IPR2021-00040	Paper 15	Paper 16	Ex. 1018	Ex. 1019
IPR2021-00041	Paper 15	Paper 16	Ex. 1118	Ex. 1119
IPR2021-00042	Paper 17	Paper 18	Ex. 1218	Ex. 1219
IPR2021-00043	Paper 15	Paper 16	Ex. 1319	Ex. 1320

Nokia Exhibit 2004, p. 349
Amazon.com v. Nokia
IPR2024-01141

IPR2020-01685, IPR2021-00035, IPR2021-00036 (Patent 6,950,469 B2);
IPR2021-00037, IPR2021-00038, IPR2021-00039 (Patent 7,280,599 B2);
IPR2021-00040, IPR2021-00041, IPR2021-00042,
IPR2021-00043 (Patent 8,036,273 B2)

PETITIONER:

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Joseph Haag
Haixia Lin
Jonathan Knight
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Nokia Exhibit 2004, p. 350
Amazon.com v. Nokia
IPR2024-01141