

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REOLINK DIGITAL TECHNOLOGY CO., LTD.
Petitioner,

v.

KT IMAGING US, LLC
Patent Owner

U.S. Patent No. 8,314,481

**DECLARATION OF R. JACOB BAKER, PH.D., P.E.,
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,314,481**

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I, R. Jacob Baker Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 8,314,481 (“the ’481 patent”) (Ex. 1001).

2. My name is R. Jacob Baker and I am a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas. I have prepared this declaration as an expert witness on behalf of Petitioner Reolink Digital Technology Co., Ltd. (“Petitioner” or “Reolink Digital”). In this declaration, I will give my opinion as to whether claims 1–3 of the ’481 patent are unpatentable. I also provide herein the technical bases for these opinions, as appropriate.

3. For my efforts in connection with the preparation of this declaration, I have been compensated at my usual and customary rate for this type of consulting activity. My compensation is in no way contingent on the outcome of these or any other proceedings.

4. I have been asked to consider whether certain references disclose or suggest the features recited in claims 1–3 of the ’481 patent. My opinions are set forth below.

II. QUALIFICATIONS / PROFESSIONAL BACKGROUND

5. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching regarding semiconductors, semiconductor packaging, and semiconductor image sensors.

6. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is being submitted by Petitioner as Exhibit 1003. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

7. I have been teaching electrical engineering at UNLV since 2012. Prior to that position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991. I have been working as an engineer since 1985.

8. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993.

9. As described in my CV, I am a licensed Professional Engineer and have more than 35 years of industry and academic experience, including extensive experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. (“MTI”) in Boise, Idaho.

10. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle.

11. I have been recognized for my contributions as an educator in the field.

While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

12. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and coauthored, more than 100 papers and presentations in the areas of solid-state circuit design, fabrication, and packaging. I am the named inventor on 152 granted U.S. patents in integrated circuit designs. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities.

13. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-2024). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

III. MATERIALS REVIEWED

14. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding electrical engineering, circuit design, and electrical devices, such as semiconductor image sensor substrates and packages.

15. In forming my opinions expressed in this Declaration, I reviewed the following materials and information:

EXHIBIT	DESCRIPTION
Ex. 1001	U.S. Patent No. 8,314,481
Ex. 1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
Ex. 1004	File History of U.S. Patent No. 8,314,481
Ex. 1005	U.S. Patent Application Publication No. 2003/0071332 (“Hsu”)
Ex. 1006	U.S. Patent No. 6,262,479 (“Chou”)
Ex. 1007	U.S. Patent Application Publication No. 2006/0008939 (“Chen”)
Ex. 1008	U.S. Patent Application Publication No. 2005/0109926 (“Minamio”)
Ex. 1009	U.S. Patent No. 6,071,760 (“Nakada”)
Ex. 1010	U.S. Patent Application Publication No. 2005/0057883 (“Bolken”)

16. I also reviewed any other materials I refer to in this Declaration in support of my opinions.

17. My opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the state of the art, the prior art, and the claims and the specification of the ’481 patent at the time of the alleged invention. I have been asked to initially consider that the time of the alleged invention of the ’481 patent is around May 18, 2005. My opinions reflect how one of ordinary skill in the art (which I have described below) would have understood the ’481 patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

18. Based on my experience and expertise, it is my opinion that the prior art discloses and/or suggests all the features recited in challenged claims 1–3 of the '481 patent, as I discuss in detail below.

19. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, during the relevant timeframe (*e.g.*, the time of the alleged invention), which I have been asked to assume is around May 18, 2005.

IV. LEVEL OF ORDINARY SKILL IN THE ART

20. In determining the skills of a hypothetical person of ordinary skill in the art of the '481 patent at the time of the claimed invention (which I have been asked to assume is May 2005), I considered several things, including various prior art techniques for hermetically sealing semiconductor packages and arranging components of an image sensor package. I also considered the type of problems that such techniques gave rise to and the rapidity with which innovations were made. I also considered the sophistication of the technologies involved and the educational background and experience of those actively working in the field.

21. For the purposes of my analysis, I have been asked to assume that a person of ordinary skill in the field of art of the '481 patent would have had (1) a Master of Science degree in engineering, with approximately two years of experience with semiconductor or image sensor packaging; or (2) a Bachelor of Science degree in engineering with approximately four years of experience with

semiconductor or image sensor packaging. My opinions below have taken that into account and reflect that level of skill in determining the content of the prior art and what it would have suggested to a person of ordinary skill.

IV. BACKGROUND OF THE TECHNOLOGY

22. At the time of the alleged invention, solid-state image sensors, for example, charge coupled devices (CCDs) or complementary metal-oxide semiconductor (CMOS) chips, were well established technology and in high demand for use with electronic products, such as digital cameras. (Ex. 1010, ¶0004.) Conventionally, these image sensors were packaged for use by mounting them to a substrate and enclosing them within a housing assembly. (*Id.*) The housing assembly would typically include a transparent lid to allow light to be received by the sensor. (*Id.*)

23. For example, the '481 patent depicts an image sensor package that was known in the prior art, as illustrated below. (Ex. 1001, FIG. 1.) Substrate 10 and frame layer 18 form a housing assembly in which an image sensor chip 26 is placed and then enclosed by a transparent glass 34. (Ex. 1001, 1:14–33.) Bonding wires 28 connect the circuits of the image sensor chip to first electrodes that extend under the frame layer and connect to second electrodes 22 on the back of the substrate 16.

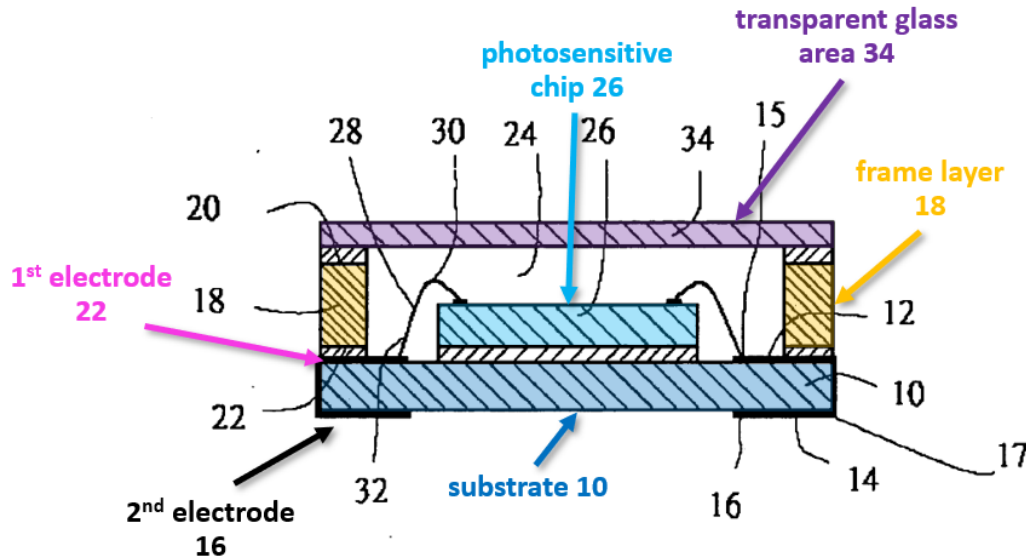


FIG.1(Prior Art)

(Ex. 1001, FIG. 1.)

24. The substrate and housing were often formed from a ceramic material, while the lid was usually glass or a similar transparent substance attached to the housing by an adhesive. (Ex. 1010, ¶0004.) The choice of materials would often come with tradeoffs, such as cost. Various methods were developed in attempts to simplify the construction of image sensor packages and reduce material costs. (*Id.*, ¶0005.)

25. Another consideration in packaging the image sensor was hermetic sealing capabilities of packaging, especially at edge locations where minute gaps may expose the image sensor to the outside environment. (*Id.*, ¶0006.) For instance, moisture may ultimately find its way into the interior of the package, resulting in damage to the image sensor circuitry. (*Id.*) Another consideration was that the use of a housing molded from low-cost materials, such as BT, epoxy resin, or other

plastic materials, may not have the high dimensional tolerances to sealing the substrate and transparent lid. (*Id.*, ¶¶0005–0006.) In light of these concerns, a person of ordinary skill in the art would have appreciated that it was important to design an image sensor package that is simple and inexpensive to manufacture, and that also provides reliable hermetic sealing capabilities to prevent moisture damage and other harmful environmental effects. (*Id.*, ¶¶0007.)

V. OVERVIEW OF THE '481 PATENT

26. The '481 patent is directed to a substrate structure for an image sensor package. (Ex. 1001, 1:8–12.) The '481 patent purports to improve the reliability of the package as compared to a prior art image sensor arrangement. (*Id.* at 1:13–55.) To accomplish this goal, the '481 describes placing an insulation material in gaps between electrodes in an image sensor package that may otherwise allow “particles and wet air from [the surrounding] atmosphere” to enter the image sensor package. (*See id.*) In other words, openings in the image sensor package are filled with insulation to seal the image sensor package from dust and moisture in the external environment. (*Id.*, 1:34–37, 1:41–44.)

27. The '481 patent illustrates a “prior art” image sensor package, where a lower surface of a frame layer 18 is adhered to an upper surface 22 of a substrate 10. (Ex. 1001, 1:14–33, FIG 1 (below).) A plurality of first electrodes 15 are formed on

the substrate 10 and a plurality of second electrodes 16 are formed on a second surface 14. (*Id.*)

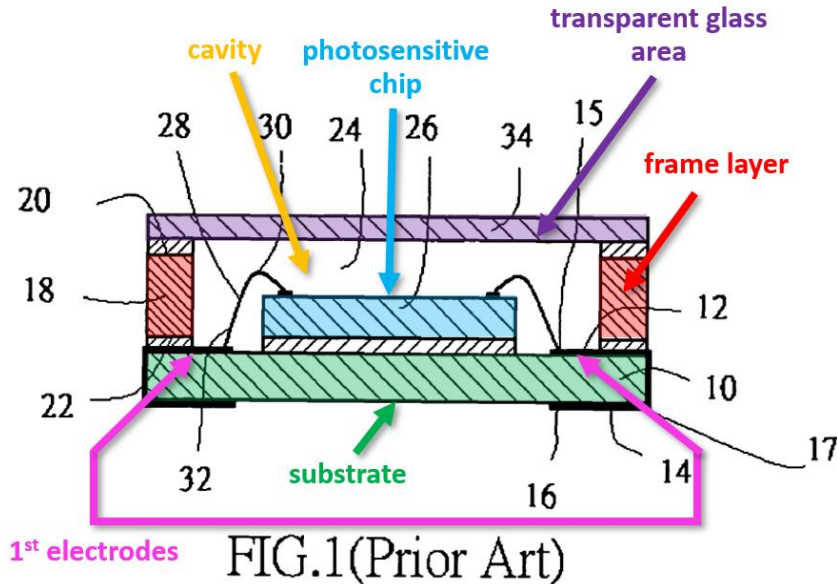
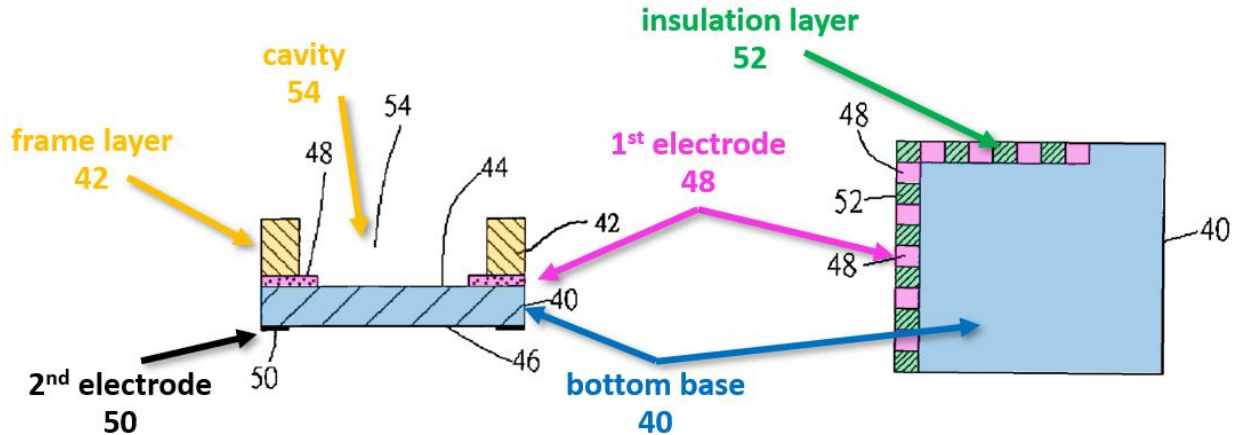


FIG.1(Prior Art)

(Ex. 1001, FIG. 1.)¹

28. According to the '481 patent, this prior art arrangement undesirably allows particles (dust) or wet air (moisture) to enter through gaps or passages between the first electrodes that lay on the substrate 10 and under the frame layer 18. (Ex. 1001, 1:34–37.) And this purportedly reduces the reliability of the image sensor. (*Id.*) To address this issue, the '481 patent proposes coating an insulation layer between the first electrodes. (Ex. 1001, 2:6–24.) As shown below, insulation layer 52 is placed between first electrodes 48. (*Id.*, FIGs. 2–3.)

¹ All color annotations throughout are added unless noted otherwise.



(Ex. 1001, FIG. 2, 3.)

29. As illustrated in Figs. 2 and 3 reproduced above, the substrate structure for an image sensor package includes a bottom base 40 and a frame layer 42. (*Id.* 2:6-8.) The bottom base 40 has an upper surface 44 with a plurality of first electrodes 48, and lower surface 46 with a plurality of second electrodes 50. (*Id.*, 2:9-11.) Each of the first electrodes 48 is electrically connected to the corresponding second electrode 50. (*Id.*, 2:11-13.)

30. The '481 patent states that “[a]n insulation layer 52 is coated between the first electrodes 48 and in direct surface contact with the upper surface 44 of the bottom base 40 so as to smooth the first electrodes 48 on the upper surface 44 of the bottom base 40 [and] the insulation layer 52 is interposed between the bottom base 40 and the frame layer 42.” (*Id.* at 2:13-19.) The '481 patent further states that “[t]he frame layer 42 is arranged on and in direct surface contact with the first electrodes 48 and the insulation layer 52 to form a cavity 54 together with the bottom base 40.” (*Id.* at 2:22-24.)

VI. CLAIM CONSTRUCTION

31. I understand that claim terms are typically given their ordinary and customary meanings, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention, which as I explained above I have been asked to assume is around May 18, 2005. In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, and the prosecution history of record. I have been asked to consider the claim terms under their plain meanings and thus considered the claims, specification and prosecution history for the '481 patent in doing so in support of my opinions concerning the '481 patent and the prior art discussed herein.

32. I understand that in the corresponding district court litigation between the same parties, a court ruled that the preamble of claim 1, *i.e.* “[a] substrate structure for an image sensor package,” was not limiting and therefore did not require construction. As I understand it, no other terms of the '481 patent were construed.

VII. OVERVIEW OF THE PRIOR ART

A. Hsu (Ex. 1005)

33. Similar to the '481 patent, Hsu is directed to a semiconductor packaging structure. In particular, Hsu describes a semiconductor packaging structure that is easy to fabricate, incurs a low production cost and has a good heat

dissipation. (Ex. 1005, ¶0002.) Hsu describes prior art substrate structures which appear to be nearly identical to the conventional image sensor package described by the '481 patent. (*Compare* Ex. 1001, ¶¶0004–0006, FIGs. 1 and 2 *with* Ex. 1005, ¶¶0003–0006, FIGs. 13 and 14.) Similar to the '481, Hsu recognizes the susceptibility of the prior art image sensor packages to moisture. (*See, e.g.*, Ex. 1005, ¶0007 (“Since the substrate is made of epoxy resin, the substrate is easy to absorb moisture, and the chip mounted on the substrate would be affected by the moisture, so that the stability of the chip is reduced.”).)

34. Hsu also acknowledges several other potential shortcomings of the prior art arrangements:

- The plurality of leads on the substrate is formed by an electroplating process, such that the reliability of forming the leads is hard to control. (Ex. 1005, ¶0008.)
- The efficiency of heat dissipation of the epoxy resin substrate is much lower than a substrate made of metal. (Ex. 1005, ¶0009.)
- Since the plurality of leads on the substrate extends from the top surface of the substrate and passes through a lateral side of the substrate to a bottom surface of the substrate, thus the signal conducting path is longer, which may delay the signal conduction. (Ex. 1005, ¶0010.)

35. To address these potential shortcomings, Hsu proposes five embodiments of a semiconductor packaging structure. (Ex. 1005, ¶¶0028–0041.) Hsu states that “[t]he primary objective of the invention is to provide a semiconductor packaging structure that is easy to fabricate, is able to reduce the production cost, has a high efficiency of heat dissipation and is able to mitigate a signal delay.” (Ex. 1005, ¶0012.)

36. A first embodiment of a semiconductor packaging structure illustrated in Figure 1 below comprises a lead frame (10) made of a metal material, a wall portion (20), a chip (30) and a transparent cover (40). (Ex. 1005, ¶0028.) The lead frame (10) has a die pad (11) for mounting the chip (30) and a plurality of leads (12) arranged around the die pad (11), wherein each lead (12) is separate from each other. (Ex. 1005, ¶0029.) This separation is necessary so that the individual circuits can be individually addressed. The multiple gaps (14) defined between two adjacent leads (12), and an interval between the die pad (11) and the plurality of leads (12), are all filled with an isolating resin (13) (as shown in FIG. 3). (Ex. 1005, ¶0029.) As a matter of basic circuit design, a person of ordinary skill would have understood that the resin is made of a dielectric material so as to not short circuit the separated electrode leads.

37. Further, Hsu states that “wall portion (20) is formed by molding compound and is installed at periphery of the lead frame (10), wherein the wall

portion (20) is also formed by an isolating material.” (Ex. 1005, ¶0030.) The wall portion (20) and the isolating resin (13) can be formed integrally on the lead frame (10) or the wall portion (20) is formed on the lead frame (10) after the isolating resin (13) is put in the gaps (14). (Ex. 1005, ¶0030.)

38. Then a chip (30) is mounted on the die pad (11) by a silver epoxy or other kinds of solders and is further electrically connected to the plurality of leads (12) via gold wires (31), as was common at the time. (Ex. 1005, ¶0031.) After the chip is mounted an enclosing means, for example the transparent cover (40), is applied on the packaging structure to enclose the chip (30) inside the wall portion (20) so that the transparent cover (40) is able to protect the chip (20) from the contaminant, such as dust or moisture. (Ex. 1005, ¶0032.)

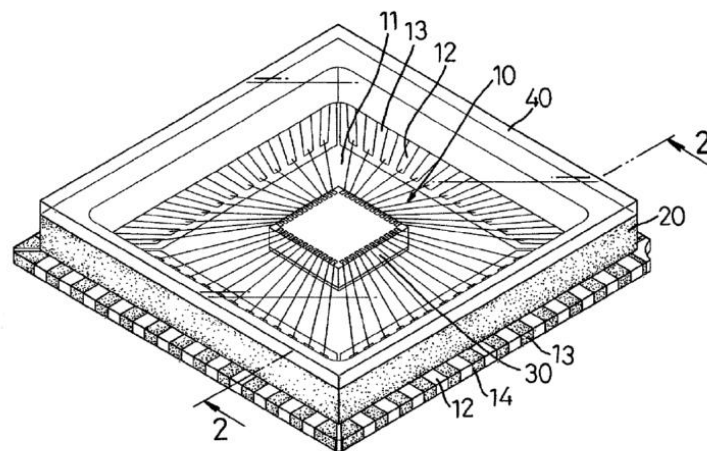
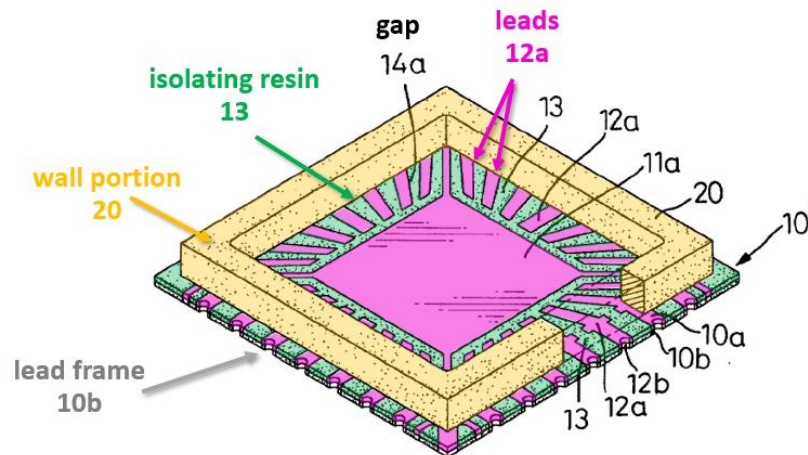


FIG.1

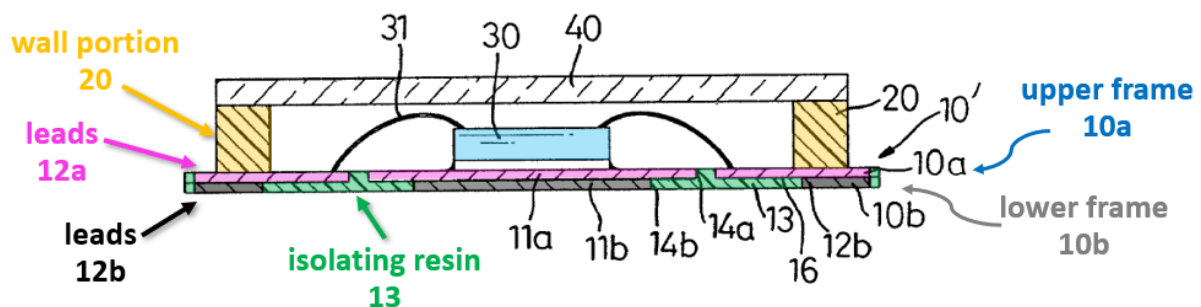
(Ex. 1005, FIG. 1.)

39. A fifth embodiment of a semiconductor packaging structure is illustrated below, where a wall portion 20 is arranged on an upper leads 12a and isolation resin 13. (Ex. 1005, ¶0036.)



(Ex. 1005, FIG. 8 (a perspective view of the fifth embodiment).)

40. In the fifth embodiment, a metal frame (10') is combined by an upper lead frame (10a) and a lower lead frame (10b) through a thermal-compress process.
(Ex. 1005, ¶0036.)



(Ex. 1005, FIG. 11.)

41. As illustrate above, with the upper and lower lead frames in this contiguous arrangement, leads (12b) of the lower lead frame (10b) correspond to the leads (12a) of the upper lead frame (10a), which electrically couples the respective upper and lower leads. (Ex. 1005, ¶0040.) Because the two die pads (11a)(11b) and sets of leads (12a)(12b) have the different configurations, once the two lead frames (10a)(10b) are compressed together, multiple interstice (16) are defined for receiving the isolating resin (13). The isolating resin (13) further fills the multiple interstice (16) and the gaps (14a)(14b) between the leads. (*Id.*) A cover 40 encloses the chip 30 and, thus much like the first embodiment, the chip is protected from dust and moisture.

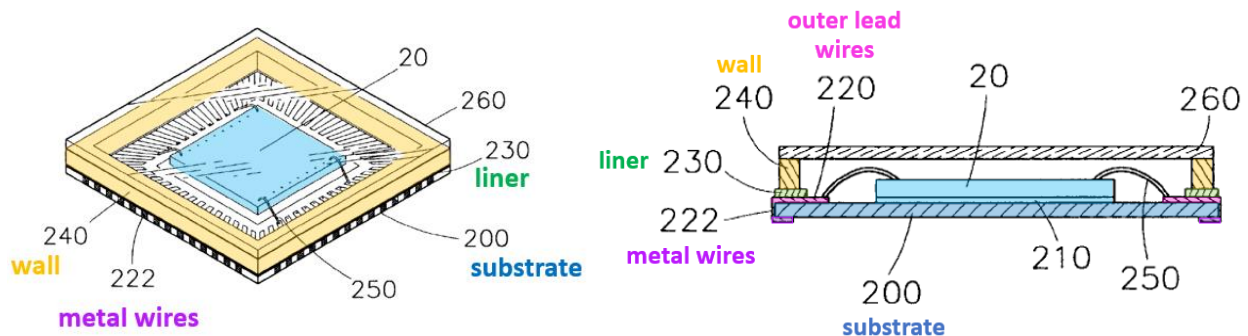
A. Chou (Ex. 1006)

42. Similar to the '481 patent, Chou is directed to a semiconductor packaging structure, and provides a semiconductor package structure with a simple structural mold and a lower cost. (Ex. 1006, 1:5–49.) Chou recognizes that because the outer lead wires formed on a substrate surface will create an irregular (undulated) surface, it was therefore desirable to make a flat seat for placing a framing wall. (Ex. 1006, 2:42–47.)

43. In other words, as shown in Figure 4, substrate 200 has a flat surface on which the outer leads wires 220 are formed. As illustrated in Figure 6, the outer lead wires are arranged around the dies pad. A few exemplary wire bonds are illustrated

connecting the chip to the outer lead wires. As can be appreciated from Figures 3–6 and Chou’s disclosure, these separated outer lead wires leave gaps between the lead wires 220 which with the lead wires form an undulating or corrugated surface. As would have been appreciated by a person of ordinary skill in the art, these gaps between the outer electrode leads 220 would do not provide a flat surface for the wall 240 and spaces where the wall 240 would not adhere to the substrate 200.

44. To form a flat seat and increase adhesion to the wall, Chou discloses an insulating liner coats the periphery of the substrate. (*Id.*) As shown in Figures 4 and 6, the liner 230 fills the space between the outer electrode leads 220 and provides a flat surface for forming the wall 240.



(Ex. 1006, FIGs. 4 and 6.)

C. Chen (Ex. 1007)

45. Similar the '481 patent, Chen is directed to an image sensor package, and in particular to an image sensor with increased reliability. (Ex. 1007, ¶0002.) Chen discloses an image sensor package known in the prior art where each first electrode 15 of the substrate 10 is arranged in straight line, and a green paint 35 is

coated between the each first electrode 15. (Ex. 1007, ¶0006.) As discussed above, a person of ordinary skill would have appreciated that the first electrodes are respectively connected to the semiconductor chip by individual wire bonds 28 and thus it is further understood that the green paint 35 is an electrically insulating material so as to not short circuit the first electrodes.

46. Chen further discloses that in the prior art image sensor package a frame layer 18 is mounted on substrate 10. (*Id.*) Chen recognizes that, despite the green paint between the first electrodes, there may nevertheless be a gap between the first electrodes 15 where moisture may enter the package and the reliability of the product may be reduced. (*Id.*)

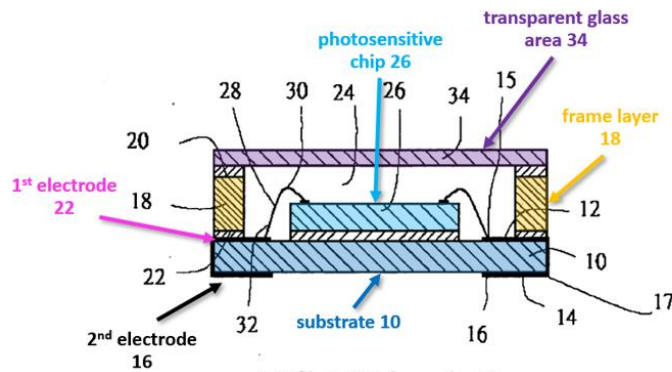


FIG.1(Prior Art)

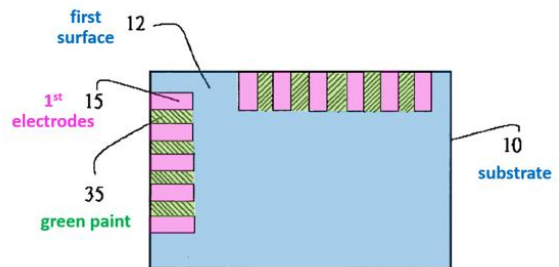
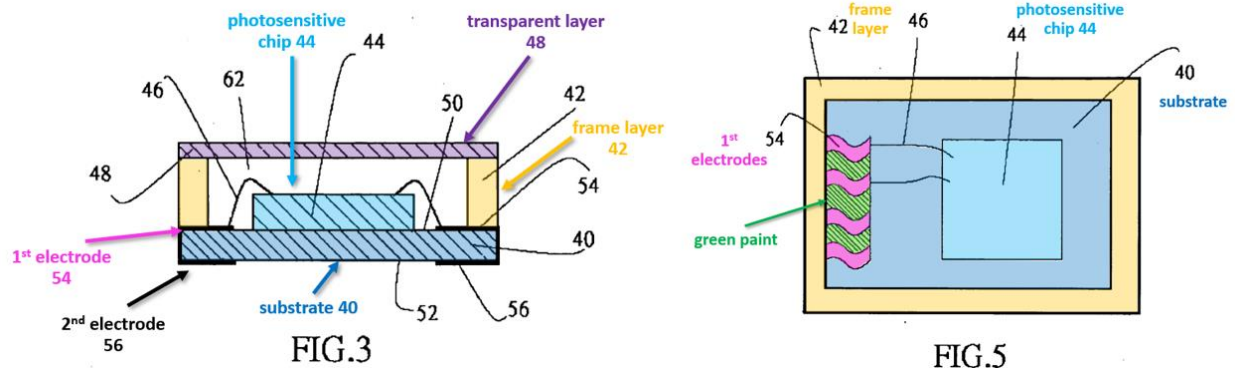


FIG.2(Prior Art)

(Ex. 1007, FIGs. 1 (cross-sectional view) and 2 (top-view).)

47. To address this issue, Chen proposes a curved first electrode arrangement with green paint coated between the first electrodes. (Ex. 1007, ¶0015.) This first electrode arrangement is illustrated in Figure 5 below. According to Chen,

this arrangement prevents moisture (wet air) from entering the image sensor. (Ex. 1007, ¶10020.)



(Ex. 1007, FIGs. 3 (cross-sectional view) and 5 (top view).)

VIII. THE PRIOR ART DISCLOSES AND/OR SUGGESTS THE RECITED FEATURES OF CLAIMS 1–3 OF THE '481 PATENT

A. Ground I – Claims 1–2 are anticipated by Hsu

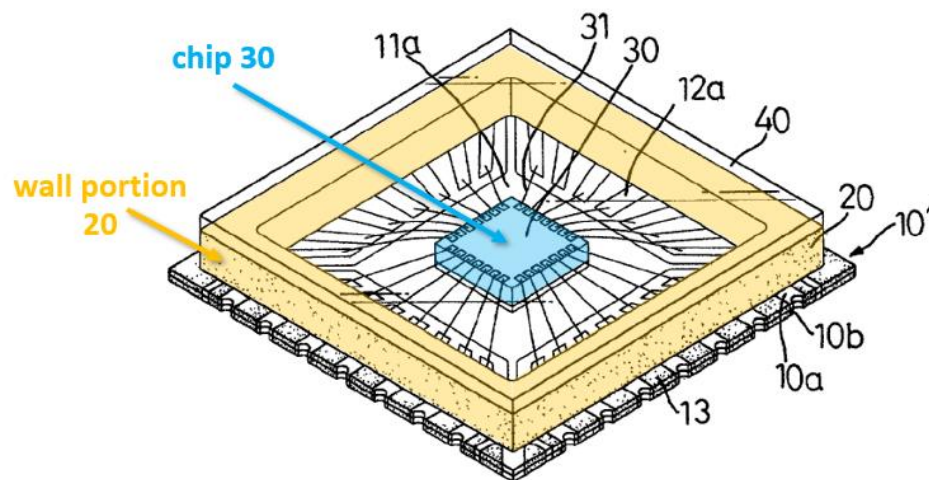
1. Claim 1

48. Hsu discloses each and every limitation of claim 1 of the '481 patent.

a. A substrate structure for an image sensor package, the substrate structure comprising:

49. As I noted above, I understand the district court ruled that the preamble is not limiting. Nevertheless, Hsu discloses a semiconductor substrate structure suitable for an optical sensing package 30. (See, e.g., Ex. 1005, ¶¶0002 (“The present invention relates to a **semiconductor packaging substrate**...”), 0028, 0033 (“Both the transparent cover 40 and the transparent resin are suitable for the **optical sensing semiconductor packaging structure**.”), 0037–0041, FIG. 7 (reproduced below).) Further, Hsu discloses that a conventional semiconductor packaging

structure for sensing optical signals may be a charge coupled device (CCD) (*i.e.*, a common type of image sensor). (Ex. 1005, ¶0004.) In light of this disclosure and the structural similarity to well-known components common to image sensor packages (*e.g.*, a semiconductor chip, a die pad, a wall portion (also referred to as a frame), electrical leads connected by gold wires to the chip, *etc.*), a person of ordinary skill in the art would have understood Hsu's substrate structure to be suitable for an image sensor. An illustration of the fifth embodiment is provided below.



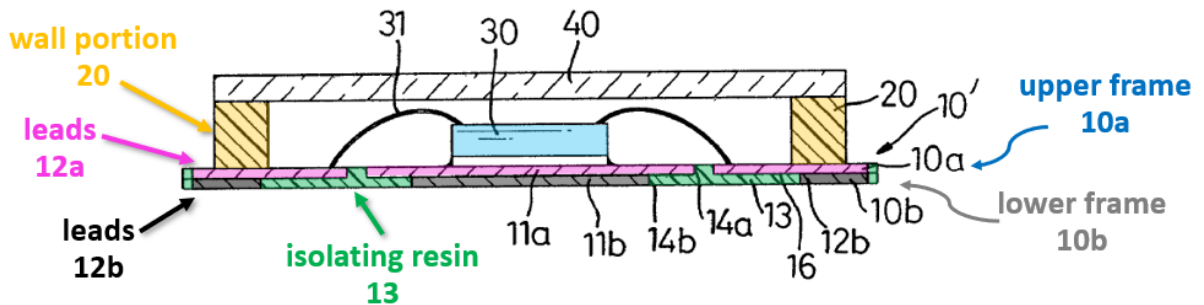
(Ex. 1005, FIG. 7 (perspective view).)

50. Although my analysis below focuses on the particular description of Hsu's fifth embodiment (FIGs. 7–12), it should be noted that Hsu's description of the fifth embodiment pertains to lead frame 10' as an alternative to lead frame 10 and thus does not repeat its description of other common components (such as wall portion 20). (Ex. 1005, ¶0037.) But as would have been appreciated by a person of

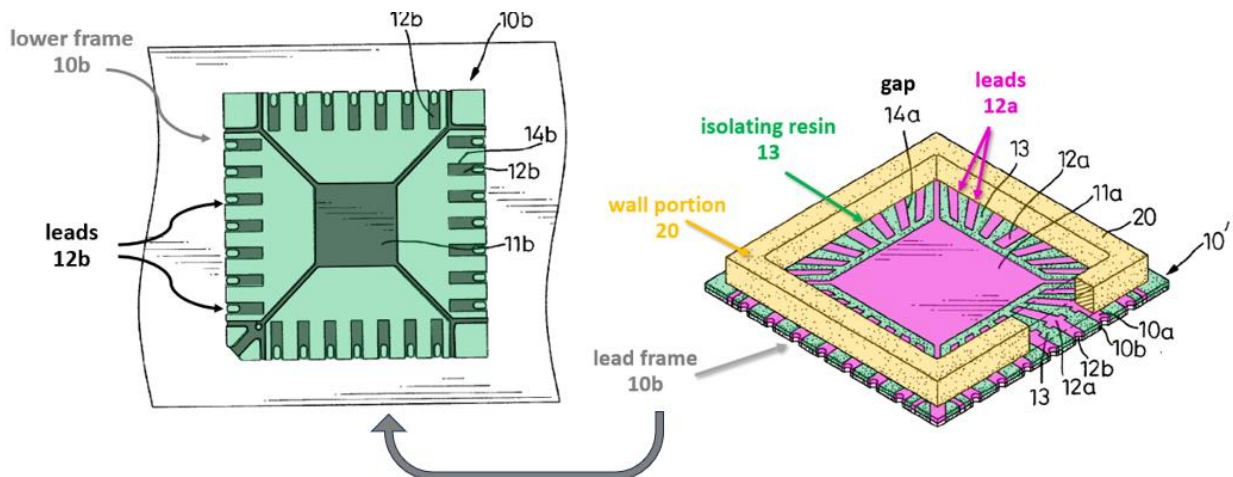
ordinary skill, Hsu description of common components would apply equally to all embodiments.

b. a bottom base having an upper surface formed with a plurality of first electrodes, and a lower surface formed with a plurality of second electrodes

51. Hsu discloses this limitation. For instance, Hsu discloses a lower frame 10b (*i.e.*, a bottom base) having an upper surface formed with a plurality of leads 12a (*i.e.*, first electrodes), and a lower surface formed with a plurality of leads 12b (*i.e.*, second electrodes). (Ex. 1005, ¶¶0037–0041, FIGs. 7–11.)



(Ex. 1005, FIG. 11 (cross-sectional view).)

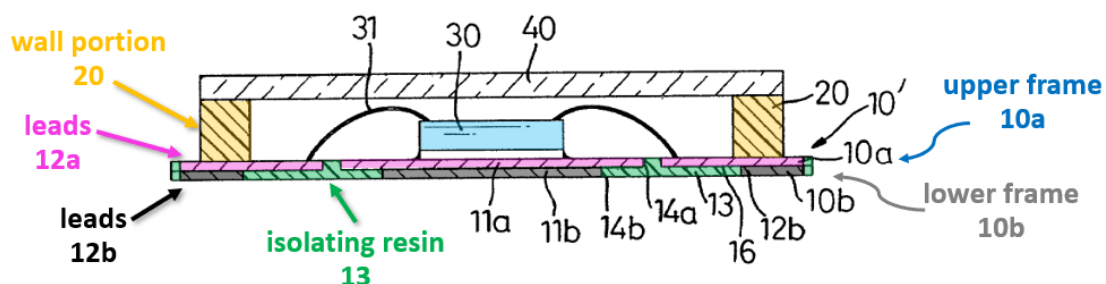


(Ex. 1005, FIGs. 8 (perspective view) and 10 (top view of the lower frame).)

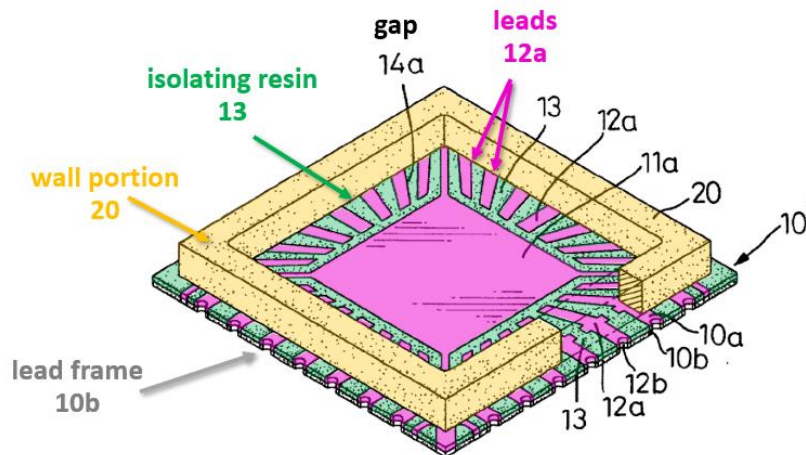
52. In particular, Hsu discloses lower frame 10b (*i.e.*, a bottom base) has an upper surface adjoining upper frame 10a as shown in Figures 8 and 11. In particular, “the upper lead frame 10a and the lower lead frame 10b are in alignment with each other and compressed together to form metal frame 10', and the leads 12b of the lower lead frame 10b are corresponded to the leads 12a of the upper lead frame 10a.” (Ex. 1005, ¶0040.) Hence, the upper surface of lower lead frame 10b is formed with a plurality of leads 12a (*i.e.*, first electrodes), and a lower surface of lower lead frame 10b is formed with a plurality of leads 12b (*i.e.*, second electrodes). (Ex. 1005, ¶¶0037–0041, FIGs. 7–11).

c. wherein an insulation layer is coated between first electrodes and in direct surface contact with the upper surface of the bottom base

53. Hsu discloses this limitation. For instance, Hsu discloses isolating resin layer 13 (*i.e.*, an insulation layer) is coated between leads 12a (*i.e.*, first electrodes) and arranged on (*i.e.*, in direct surface contact with) the upper surface of the bottom base, as shown in Figures 8 and 11 (below). (Ex. 1005, ¶¶0037–0041, FIGs. 7–11.)



(Ex. 1005, FIG. 11.)



(Ex. 1005, FIG. 8.)

54. Specifically, as I mentioned above in my summary of Hsu, a person of ordinary skill in the art would have understood that isolating resin 13 is an electrically insulating layer which electrically isolates individual pairs of leads 12a and 12b from the other pairs of leads. Suitable resin materials, such as epoxy resin or other plastic materials, would have been known to be an electrically insulating material.

55. Moreover, its described function (*i.e.*, “isolating”) and its arrangement in the gaps between the pairs of electrical leads 12a, 12b is indicative of an electrically isolating (*i.e.*, electrically insulating) material. A person of ordinary skill in the art would have also understood that if isolating resin 13 were conductive, it would create an electrical short (*i.e.*, electrical connection) between the leads and the substrate would not function as intended. (Ex. 1005, ¶0039 (“[E]ach of the plurality of leads 12b of the lower lead frame 10b only has an external portion

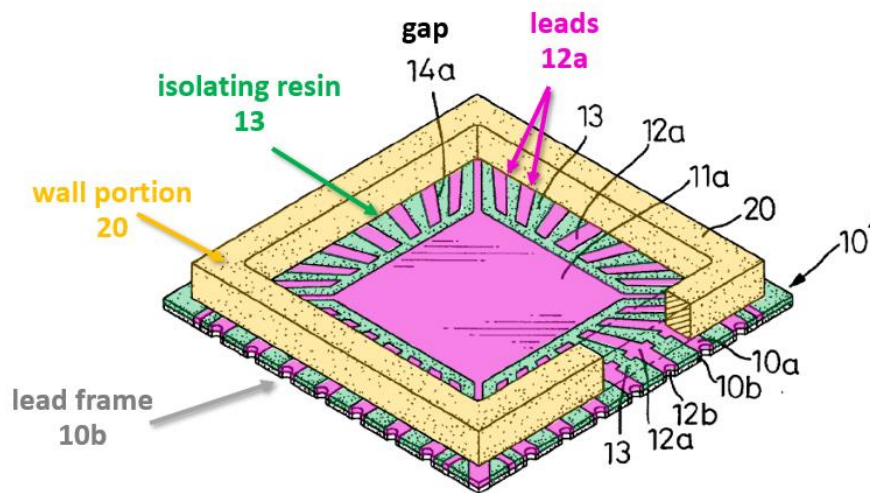
corresponding to one of the external portions of the leads 12a”); ¶0046 (“Since the chip is directly connected to the leads of the lead frame and the leads are electrically and directly mounted on a circuit board, thus the signal conduction path is very short and the conducting delay is avoid[ed].”).) Therefore, based on my experience, a person of ordinary skill in the art would conclude that isolating resin 13 is an insulating layer.

56. Hsu further discloses that “[a]n interval is defined between the die pad 11a, 11b and the plurality of leads 12a, 12b for filling with the isolating resin 13.” Also, “[m]ultiple gaps 14a, 14b are each defined by two adjacent leads 12a, 12b.” (Ex. 1005, ¶0039.) Thus, “multiple interstice 16 are defined for receiving the isolating resin 13.” (Ex. 1005, ¶0040.) Hsu states that “[t]he isolating resin 13 further fills the multiple interstice 16 and the gaps 14a, 14b by molding compound.” (Ex. 1005, ¶0040.) Hence, isolating resin 13 is coated between leads 12a in gaps 14a and in direct surface contact with the upper surface of the lower lead frame 10b, as shown in Figures 7–11.

d. frame layer arranged on and in direct surface contact with the first electrodes and the insulation layer to form a cavity together with the bottom base

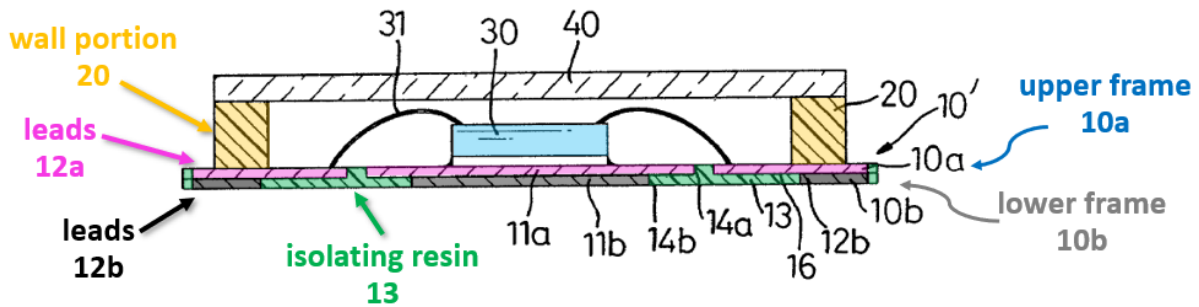
57. Hsu discloses this limitation. For instance, Hsu discloses wall portion 20 (*i.e.*, a frame layer) arranged on and (*i.e.*, in direct surface contact) with the leads 12a (*i.e.*, the first electrodes) and the isolating resin (*i.e.*, the insulation layer). (*See*,

e.g., Ex. 1005, ¶¶0057–0065; FIGs. 1–7B.) In particular, as illustrated below in Figure 8, wall portion 20 extends around the periphery of the lead frame (Ex. 1005, FIG. 8; *see also id.*, ¶0030 (“The wall portion 20 is formed by molding compound and is installed at [the] periphery of the lead frame 10.”).) Therefore, a person of ordinary skill in the art would have considered wall portion 20 be a “frame layer” as claimed.



(Ex. 1005, FIG. 8.)

58. As illustrated in Figure 8 (above) and also Figure 11 (below), Hsu wall portion 20 (*i.e.*, a frame layer) “can be formed integrally on” the lead frame and thus in direct surface contact with the leads 12a (*i.e.*, the first electrodes) and the isolating resin (*i.e.*, the insulation layer). (Ex. 1005, ¶0030.)

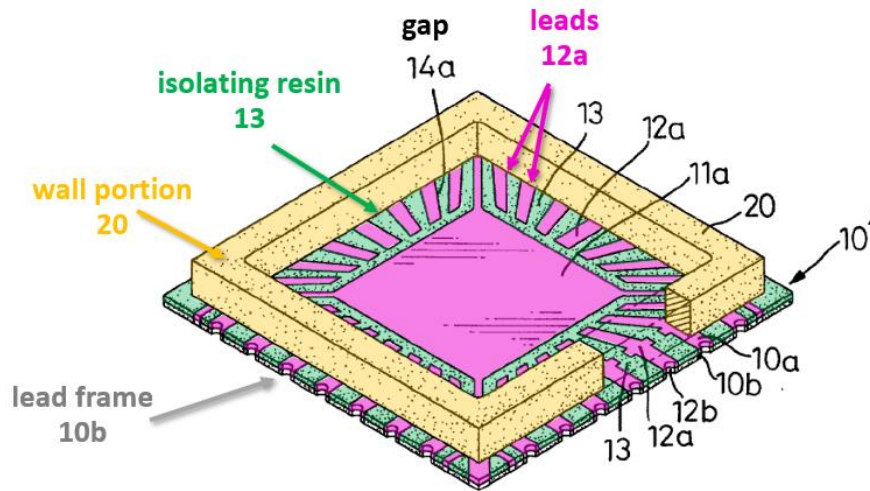


(Ex. 1005, FIG. 11.)

59. Further, Hsu discloses that the wall portion 20 (*i.e.*, frame layer), leads 12a (*i.e.*, first electrodes), and isolating resin 13 (*i.e.*, insulating layer) form a cavity to enclose the chip 30 together with the lead frame 10b (*i.e.*, bottom base), as illustrated above in Figure 11. (*See* Ex. 1005, ¶¶0032 FIGs 1, 3.)

e. wherein the insulation layer is interposed between the bottom base and the frame layer

60. Hsu discloses this limitation. For instance, Hsu discloses isolating resin 13 (*i.e.*, the insulation layer) is interposed between the lead frame 10b (*i.e.*, the bottom base) and wall portion 20 (*i.e.*, the frame layer). (*See, e.g.*, Ex. 1005, ¶¶0037–0041, FIGs. 7–11.) In particular, as illustrated in Figure 8 below, at the outer periphery, the wall portion 20 is arranged over top of the isolating resin 13 and isolating resin 13 is above lower frame 10b. At least in this sense, isolating resin 13 is arranged between the lead frame 10b and wall portion 20.



(Ex. 1005, FIG. 8.)

2. Claim 2 – The substrate structure according to claim 1, wherein the first electrodes are electrically connected to the second electrodes, respectively

61. Hsu discloses the limitation recited in claim 2. For instance, as noted above, Hsu discloses that “each of the plurality of leads 12b of the lower lead frame 10b only has an external portion corresponding to one of the external portions of the leads 12a.” (Ex. 1005, ¶0039.) Hsu further discloses that “the upper lead frames 10a and the lower lead frame 10b are in alignment with each other and compressed together to form the metal frame 10', and the leads 12 of the lower lead frame 10b are corresponded to the leads 12a of the upper lead frame 10a.” (Ex. 1005, ¶0040.) Hence, this direct contact between the leads forms a direct physical connection. A person of ordinary skill in the art would have therefore understood the upper leads 12a (*i.e.*, the first electrodes) are electrically connected to the lower leads 12b (*i.e.*, the second electrodes), respectively.

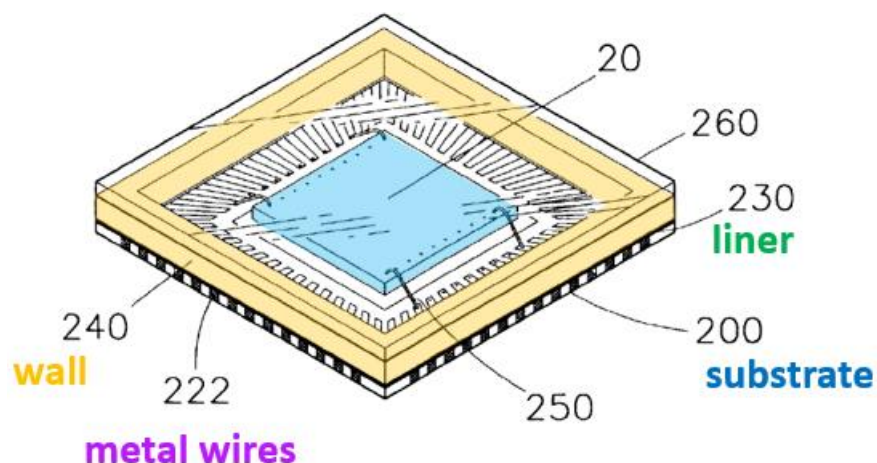
B. Ground II – Claims 1–2 are obvious over Chou and Hsu

1. Claim 1

62. Chou and Hsu discloses and/or suggests every limitation of claim 1 of the '481 patent and a person of ordinary skill would had a rationale to modify Chou in light of the teachings of Hsu.

a. A substrate structure for an image sensor package, the substrate structure comprising:

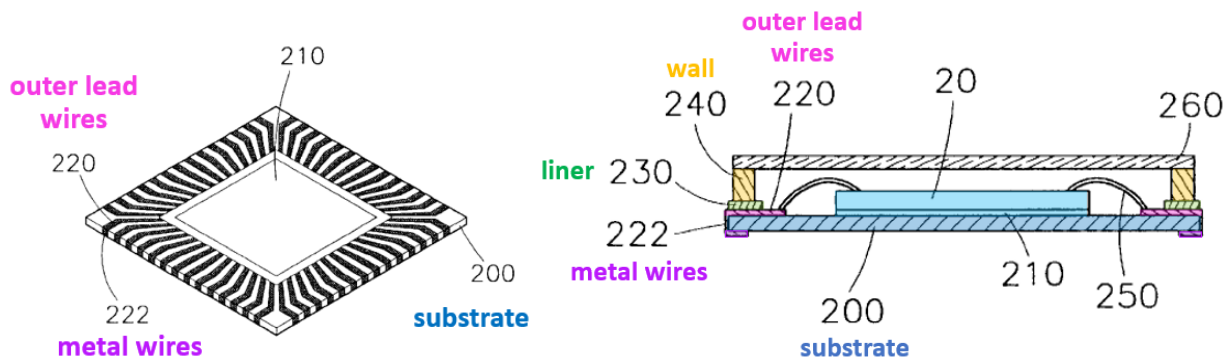
63. As noted above, I understand that the district court ruled that the preamble is not limiting. Nevertheless I have been asked to consider it and give it weight. Chou discloses substrate structure for an image sensor package. (*See, e.g.,* Ex. 1006, 2:21–29 (“[T]he semiconductor packaging structure serves to package [a] photoelectric element, for example a charge coupling device (CCD).”) As I noted above, a CCD was a well-known type of image sensor.



(Ex. 1006, FIG. 6 (perspective view).)

- b. a bottom base having an upper surface formed with a plurality of first electrodes, and a lower surface formed with a plurality of second electrodes**

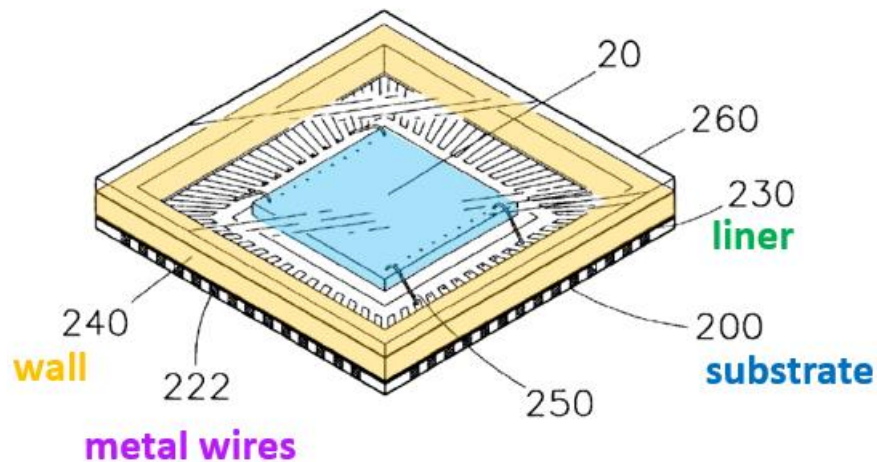
64. Chou discloses this limitation. For instance, Chou discloses substrate 200 (*i.e.*, a bottom base) having an upper surface formed with a plurality of outer lead wires 220 (*i.e.*, first electrodes), and a lower surface formed with a plurality of metal wires 222 (*i.e.*, second electrodes). (Ex. 1006, 2:30–37 (“With reference to FIG. 3, a perspective view of the substrate 200 and the related elements are illustrated. A chip seat 210 is installed on the substrate 200. A plurality of outer lead wires 220 and metal wires 222 are installed on the periphery of the chip seat 210. The metal wire 222 extends to pass through the lateral side of the substrate 200 to the bottom of the substrate 200.”), FIGs. 3–6.)



(Ex. 1006, FIGs. 3 (perspective view) and 4 (cross-sectional view).)

- c. wherein an insulation layer is coated between first electrodes and in direct surface contact with the upper surface of the bottom base**

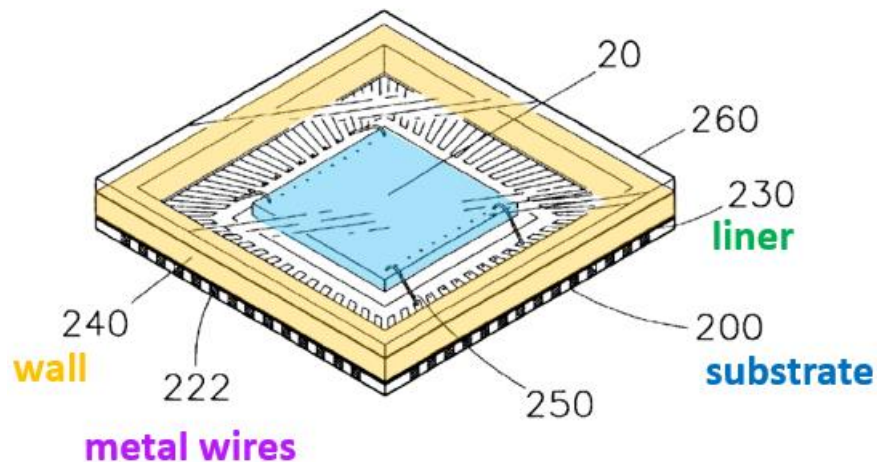
65. Chou discloses this limitation. For instance, Chou discloses liner 230 (*i.e.*, an insulation layer) is coated between outer lead wires 220 (*i.e.*, first electrodes) and arranged on (*i.e.*, in direct surface contact with) the upper surface of the substrate 200 (*i.e.*, the bottom base), as illustrated in Figure 6 (below). (Ex. 1005, ¶¶0037–0041, FIGs. 3–6.) In particular, Chou discloses the “[s]ince the outer lead wires 220 will form with an undulated surface ... a liner (for example, *insulating* plate) is firstly *coated on the periphery of the substrate 200* of the wall 240 for forming a flat seat to install the wall 240 and increase adhesion.” (Ex. 1006, 2:42–47; *see also id.*, 1:50–61.) Hence, a person of ordinary skill in the art would have understood that the insulating liner fills in the gaps between the outer lead wires to form a smooth surface.



(Ex. 1006, FIG. 6.)

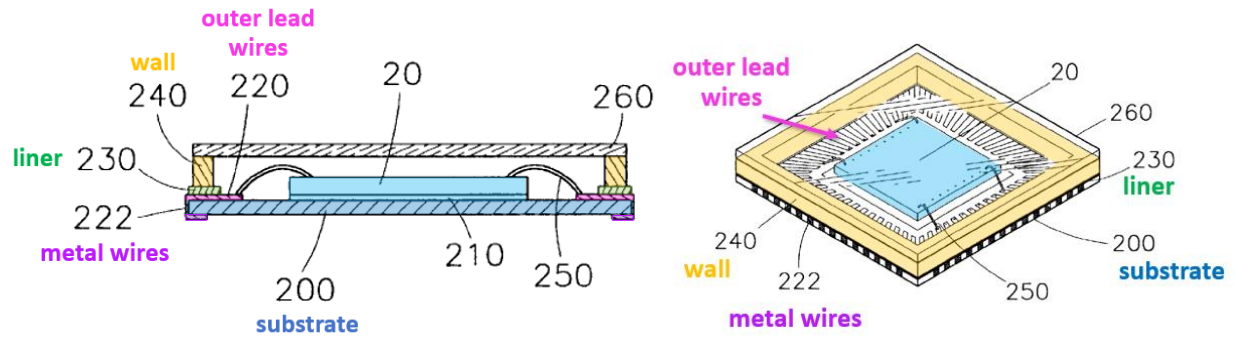
- d. a frame layer arranged on and in direct surface contact with the first electrodes and the insulation layer to form a cavity together with the bottom base

66. the combination of Chou and Hsu suggests this limitation. For instance, Chou discloses a wall 240 (*i.e.*, a frame layer) arranged on and (*i.e.*, in direct surface contact) with liner 230 (*i.e.*, the insulation layer). (See, *e.g.*, Ex. 1006, 2:41–42 (“The wall 240 is formed by molding compound and is installed at the periphery of the substrate 200.”); FIGs. 3–6.) In particular, Chou discloses “a liner (for example, *insulating plate*) ... *form[s] a flat seat to install the wall 240* and increase adhesion.” (Ex. 1006, 2:42–47; see also *id.*, 1:50–61.)



(Ex. 1006, FIG. 6.)

67. Further, as illustrated in Figures 4 and 6 (below), wall 240 (*i.e.*, frame layer), outer lead wires 220 (*i.e.*, first electrodes), and liner 230 (*i.e.*, insulating layer) form a cavity together with the substrate 200 (*i.e.*, bottom base) in which to place a semiconductor chip. (Ex. 1006, 2:22–52; FIGs 4, 6.) For example, Chou states that “[a] wall portion 240 is installed on the substrate [200] for *forming a groove to receive a photoelectric element.*” (Ex. 1006, 2:42–47; see also *id.*, 1:50–61.)



(Ex. 1006, FIGs. 4, 6.)

68. Although Chou does not expressly disclose that wall 240 is in direct surface contact with outer lead wires 220, such a feature straightforward matter of design choice and a known alternative to Chou's liner structure. As Chou illustrates, there was a known desire to have a flat surface to which to mount a frame layer. (See, e.g., Ex. 1006, 2:40–50 , 3:6–8.) Chou describes using a liner to coat the undulating surface of a substrate that is formed by individual lead wires and thereby form a flat surface for install the frame layer and increase adhesion. (See, e.g., Ex. 1006, 2:42–47.)

69. A person of ordinary skill in the art would have appreciated that a known way to form such a flat surface is to fill the gaps between the outer lead wires/electrodes with an insulating material to thereby form a flat surface around the perimeter of the substrate. Several examples of such an arrangement exist in the prior art, including the teachings of Hsu discussed above. (See my discussion above in the overview of the prior art and in in the detailed discussion of Ground I (explaining how Hsu discloses an isolating resin that fills the gaps between electrode

leads and thereby forms a flat surface for a wall portion that acts as a frame layer, for example as shown in the first and fifth embodiments). As can be appreciated by a person of ordinary skill completely filling the gaps between the electrodes forms a flat surface so that a flush mold can be formed constituting the wall/frame structure. Of course, Hsu is not alone in teaching such an arrangement. For example, Minamio discloses an image sensor having an insulating film 8a flush with internal electrodes 6a. (Ex. 1008, ¶¶0024–0028, FIGs. 1–3). And Nakada describes an image sensor with an insulating sealant 12 that fills the area between electrical leads 4, 5 properly to seal the perimeter of the image sensor substrate and forms a flat surface for a lid 11. (Ex. 1009, 2:3–4:12, FIGs. 1A–1C, 3.) In each case, the frame structure is in direct surface contact with both the underlying electrode and the insulation layer so as to seal the image sensor package.

70. Further, a person of ordinary skill in the art would have appreciated that although Chou illustrates in Figure 4 that the liner 230 extends above outer lead wires 220, such an arrangement is not necessary to form a flat surface for the wall 240, particular in light of these prior art teachings. All that is needed to form a flat surface is to fill the gaps between the electrodes completely. By contrast, it would not be necessary to fully cover the electrodes leads, for example, to still accomplish Chou's stated goal of forming a flat surface and increasing adhesion. Furthermore, filling only the gaps between outer lead wires would beneficially minimize the

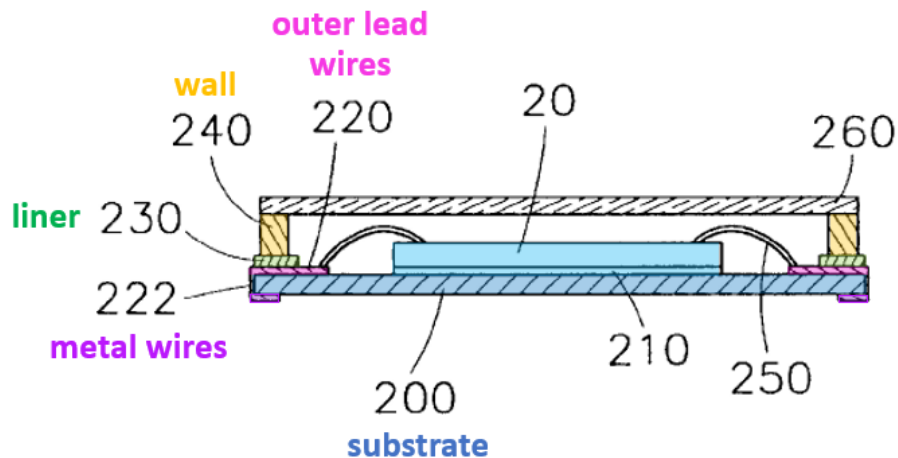
amount of material needed to form a smooth surface for the wall in in Chou's package, thereby reducing material costs while still achieving Chou's aims.

71. In light of the above, a person of ordinary skill in the art would have found that modifying Chou's package to include an insulating liner between the outer lead wires (*e.g.*, similar to the arrangement disclosed by Hsu and others and thereby ensure that the bottom surface of the wall 240 is in direct surface contact with the outer lead wires 220 and the insulating liner 230 would be consistent with the implementation of known components according to known methods, as discussed above. Such a modification to Chou would have been a predictable combination of known components according to known methods (*e.g.*, applying the teachings of Hsu regarding using filling the gaps between electrical leads to Chou's semiconductor package), and would have been produced a predictable combination of known components resulting in a flat surface for install a wall/frame. (*Id.*)

e. wherein the insulation layer is interposed between the bottom base and the frame layer

72. Chou discloses this limitation. For instance, Chou discloses liner 230 (*i.e.*, the insulation layer) is interposed between substrate 200 (*i.e.*, the bottom base) and wall 240 (*i.e.*, the frame layer). (*See, e.g.*, Ex. 1006, 1:50–61, 2:28–47, FIGs. 4, 6.) In particular, Chou discloses that “a liner (for example, insulating plate) is firstly coated on the periphery of the substrate 200 of the wall 240 for forming a flat seat

to install the wall 240 and increase adhesion.” (Ex. 1006, 2:42–47; *see also id.*, 1:50–61.) Moreover, as illustrated below, the liner 230 lies between wall 240 and base 200. Notably, the modification proposed above does not alter that arrangement because it only reduces the height of the liner which would still reside between the outer lead wires.

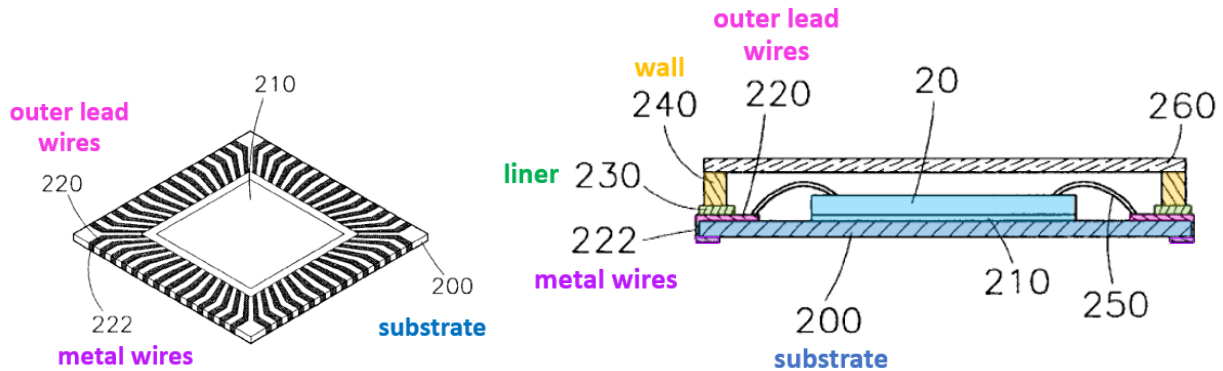


(Ex. 1005, FIG. 4.)

2. Claim 2 – The substrate structure according to claim 1, wherein the first electrodes are electrically connected to the second electrodes, respectively

73. Chou discloses this limitation. For instance, Chou discloses outer lead wires 220 (*i.e.*, the first electrodes) are electrically connected to metal wires 222 (*i.e.*, the second electrodes), respectively. In particular, Chou discloses that “[b]onding wires are connected on the element for electrically connecting the packaging element with outer devices.” (Ex. 1006, 1:57–59; *see also id.*, 1:32–34.) To this end, bonding wires 250 are physically connected to outer lead wires 220, which are in

turn, physically connected to metal wires 222, respectively, as illustrated in Figures 3 and 4 (below). A person of ordinary skill in the art would have understood that such a physical respective connection between conductive wires also results in a respective electrical connection.



(Ex. 1005, FIGs. 3, 4.)

C. Ground III – Claims 1–3 are anticipated by Chen

1. Claim 1

74. Chen discloses each and every limitation of claim 1 of the '481 patent as discussed below.

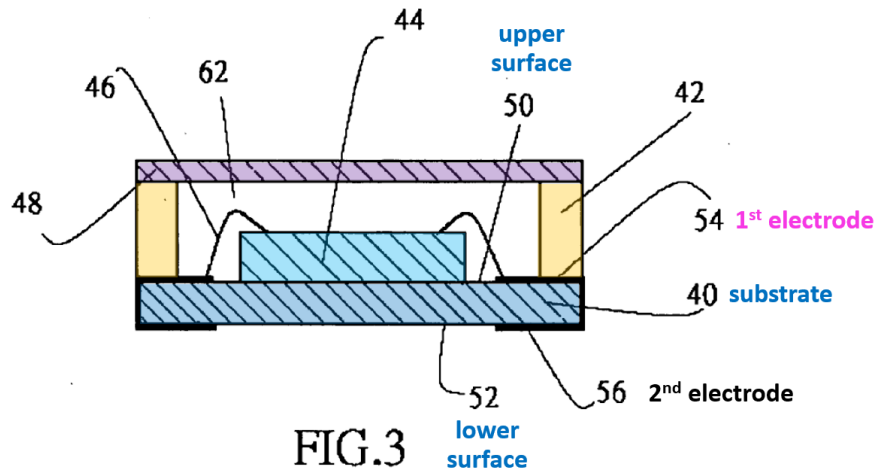
a. A substrate structure for an image sensor package, the substrate structure comprising:

75. As noted above, the district court ruled that the preamble is not limiting. Nevertheless, I have been asked to consider the preamble to be limiting. Chen discloses a substrate structure for an image sensor package. (See, e.g., Ex. 1007, ¶¶0007–0008, 0011–0013, 0014 (“Please refer to FIG. 3, FIG. 4, and FIG. 5, it is **an image sensor package** of the present invention includes a substrate 40, a frame layer



- b. a bottom base having an upper surface formed with a plurality of first electrodes, and a lower surface formed with a plurality of second electrodes**

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(Ex. 1007, FIG. 3.)

- c. wherein an insulation layer is coated between first electrodes and in direct surface contact with the upper surface of the bottom base

77. Chen discloses this limitation. For instance, Chen discloses green paint 58 (*i.e.*, an insulation layer) is coated between each first electrode 54 and arranged on (*i.e.*, in direct surface contact with) the upper surface 50 of the substrate 40 (*i.e.*, a bottom base), as shown in Figure 5 (below). (*See, e.g.*, Ex. 1007, ¶¶0007–0008, 0011–0014, 0015 (“A green-paint 58 is coated between the each first electrode 54 of the substrate 40.”), 0016–0020, FIG. 3–5.) This is illustrated below and is similar to the arrangement of the prior art image sensor package. *See* my discussion above in the overview of Chen.

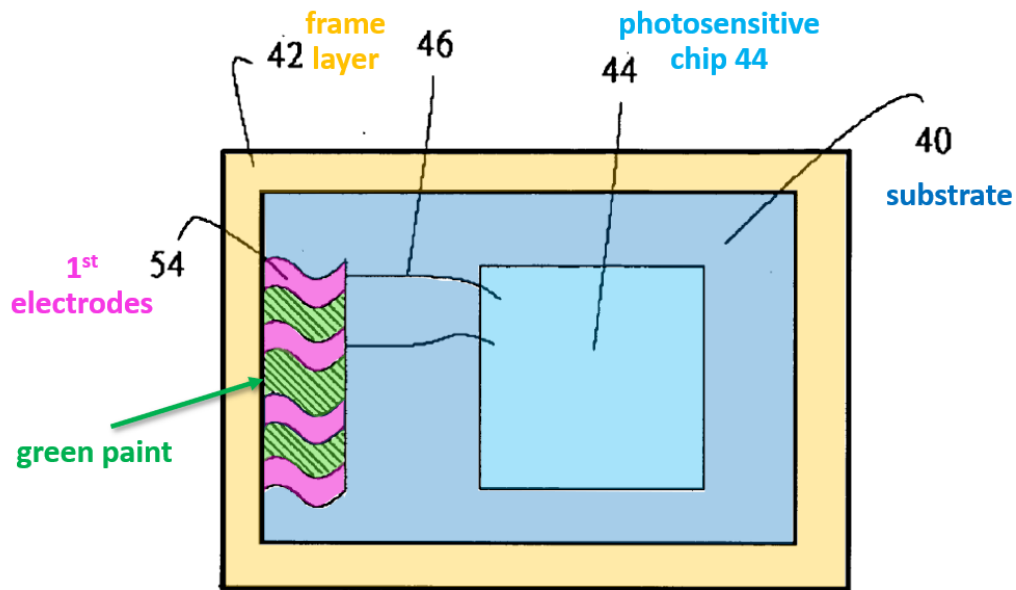


FIG. 5

(Ex. 1007, FIG. 5 (a top-view showing the image sensor package).)

78. Given the placement of the green paint between the first electrodes and the conventional understanding of image sensor packages to include individually addressable electrodes, a person of ordinary skill in the art would have understood that Chen's green paint 58 is an insulating layer which electrically insulates each first electrode 54. A paint is generally understood to be a non-conductive material. Moreover, a person of ordinary skill in the art would have understood that if green paint 58 were conductive, it would create an electrical short between the leads and the image sensor would not function as intended. For example, as discussed above, an image sensor is understood to be made up of an array of individual photosensitive elements that are individually addressable to output an electrical signal

corresponding to the sensed light. See my background discussion above. Consistent with this, Chen describes the conventional use of a plurality of wires to electrically connect the photosensitive chip and the respective first electrodes. (Ex. 1007, ¶0018 (“The plurality of wires 46 are electrically connected the photosensitive chip 44 to the first electrode 54 of the substrate 40.”).) In light of Chen’s intended application and the conventional understanding of a person of ordinary skill in the art, a skilled artisan reading Chen would have understood the green paint 58 to be an insulating layer so as to not short circuit the photosensitive chip.

d. a frame layer arranged on and in direct surface contact with the first electrodes and the insulation layer to form a cavity together with the bottom base

79. Chen discloses this limitation. For instance, in Figures 3 and 5, Chen illustrates a frame layer 42 arranged on and in direct surface contact with the first electrodes 54 and the green paint 58 (*i.e.*, the insulation layer) to form a cavity 62 together with the substrate 40 (*i.e.*, the bottom base). (*See, e.g.*, Ex. 1007, ¶¶0004–0020; FIGs. 1–5.)

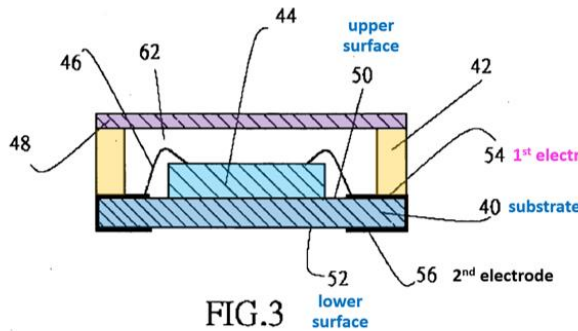


FIG.3

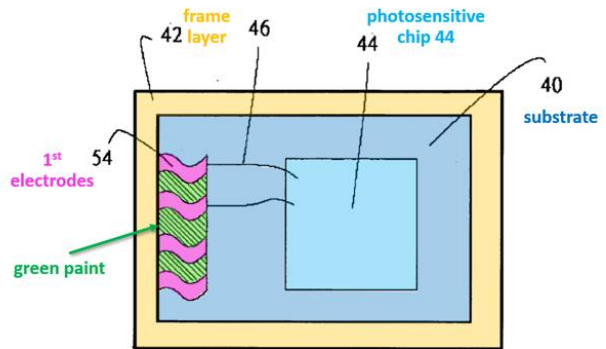


FIG.5

(Ex. 1007, FIGs. 3 (cross-sectional view) and 5 (top view).)

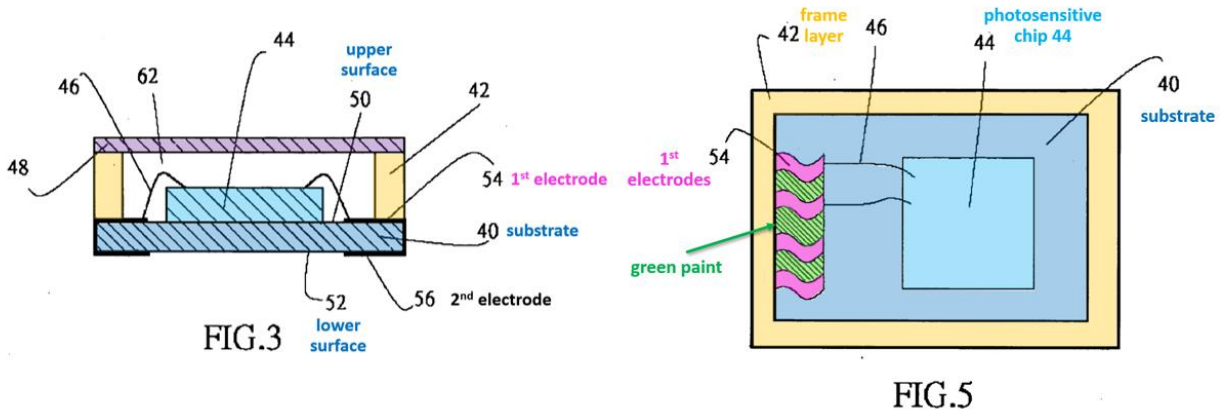
80. Further, as illustrated above in Figure 3, there is a limited volume of space between the frame layer 42 and the substrate 40 which is in part occupied by the first electrodes 54. The only remaining space unaccounted for is the gap between the electrodes. However, Figure 5 shows that that gap between the first electrodes is coated with the green paint 58, similar to the gap between the first electrodes of the prior art. (See Ex. 1007, FIG. 2.) Chen discloses, however, that green paint 58 between curved electrodes does not allow moisture (wet air) to enter the cavity containing the photosensitive chip, unlike the prior art image sensor package that wet air to enter the package. (Ex. 1007, ¶¶0006–0007, 0015, 0020.) Therefore, a person of ordinary skill in the art would have understood from Chen’s disclosure that the change in the shape of electrodes 54 would have allowed the green paint to fill the gap between electrodes and thereby seal hermetically seal the image sensor cavity 62. Understandably, if green paint 58 did not completely fill the volume between substrate 40, first electrodes 54, and the frame layer 42, moisture would be

allowed to enter cavity 62 and Chen's curved electrode arrangement would not be any more reliable than the prior art image sensor arrangement. (See Ex. 1007, ¶0007 ("An object of the invention is to provide an image sensor package [that] can prevent the wet-air from the atmosphere air [from] inter[ing] the internal [cavity] of the product [so as to] enhance[] the reliability of the product.")) Further, with the gap between the electrodes filled, the green paint (*i.e.*, the insulating layer) would be in direct surface contact with the frame layer 42 which extends across the top of the gap between the electrodes. (Ex. 1007, FIGs. 3–5; *see also id.* ¶0006 ("Referring to FIG. 2, it is a top view of the substrate of the FIG. 1. The each electrode 15 of the substrate 10 is arranged in straight line, and a green paint 35 is coated between the each first electrode 15. The frame layer 18 is mounted on the green paint 35."))

e. wherein the insulation layer is interposed between the bottom base and the frame layer

81. Chen discloses this limitation. For instance, for much of the same reasons discussed above with respect to the limitation 1(d), Chen discloses green paint 58 (*i.e.*, the insulation layer) is interposed between the substrate 40 (*i.e.*, the bottom base) and frame layer 42. (See, *e.g.*, Ex. 1007, ¶¶0008, 0014–0016, FIGs. 3–5.) In particular, as illustrated in Figure 3 (below), at the outer periphery of the package, the frame layer 42 is arranged over top of electrodes 54 and above substrate 40. Further, the green paint 58 is coated between the electrodes, as shown in Figures

4 and 5. Thus, the green paint is logically arranged between frame layer 42 and substrate 40. (Ex. 1004, 68–70 (amending the claims to recite this feature and relying on original Figures 2–4).)



(Ex. 1007, FIGs. 3 and 5.)

2. **Claim 2 – The substrate structure according to claim 1, wherein the first electrodes are electrically connected to the second electrodes, respectively**

82. Chen discloses this limitation. For instance, Chen discloses that “[t]he first electrodes 54 are corresponding to electrically connect to the second electrode 56.” (Ex. 1007, ¶0015.)

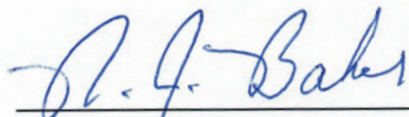
3. **Claim 3 – The substrate structure according to claim 1, wherein the insulation layer is composed of green paint**

83. Chen discloses this limitation. For instance, as noted above, Chen discloses that “[a] green-paint 58 is coated between the each first electrode 54 of the substrate 40.” (Ex. 1007, ¶0015.)

IX. CONCLUSION

84. My opinions are based upon the information that I have considered to date. I am unaware of any evidence of secondary considerations with respect to the '481 patent that would render any of the asserted claims non-obvious. I reserve the right, however, to supplement my opinions in the future to respond to any arguments raised by the owner of the '481 patent and to consider new information that becomes available to me.

85. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

By: 
R. Jacob Baker, Ph.D., P.E.

Date: July 2, 2024