THE ART OF ELECTRONICS

Second Edition

Paul Horowitz HARVARD UNIVERSITY

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TO CAROL, JACOB, MISHA, AND GINGER

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PREFACE

Electronics, perhaps more than any other field of technology, has enjoyed an explosive development in the last four decades. Thus it was with some trepidation that we attempted, in 1980, to bring out a definitive volume teaching the art of the subject. By "art" we meant the kind of mastery that comes from an intimate familiarity with real circuits, actual devices, and the like, rather than the more abstract approach often favored in textbooks on electronics. Of course, in a rapidly evolving field, such a nuts-and-bolts approach has its hazards – most notably a frighteningly quick obsolescence.

The pace of electronics technology did not disappoint us! Hardly was the ink dry on the first edition before we felt foolish reading our words about "the classic [2Kbyte] 2716 EPROM ... with a price tag of about $25." They're so classic you can't even get them anymore, having been replaced by EPROMs 64 times as large, and costing less than half the price! Thus a major element of this revision responds to improved devices and methods – completely rewritten chapters on microcomputers and microprocessors (using the IBM PC and the 68008) and substantially revised chapters on digital electronics (including PLDs, and the new HC and AC logic families), on op-amps and precision design (reflecting the availability of excellent FET-input op-amps), and on construction techniques (including CAD/CAM). Every table has been revised, some substantially; for example, in Table 4.1 (operational amplifiers) only 65% of the original 120 entries survived, with 135 new op-amps added.

We have used this opportunity to respond to readers' suggestions and to our own experiences using and teaching from the first edition. Thus we have rewritten the chapter on FETs (it was too complicated) and repositioned it before the chapter on op-amps (which are increasingly of FET construction). We have added a new chapter on low-power and micropower design (both analog and digital), a field both important and neglected. Most of the remaining chapters have been extensively revised. We have added many new tables, including A/D and D/A converters, digital logic components, and low-power devices, and throughout the book we have expanded the number of figures. The book now contains 78 tables (available separately as *The Horowitz and Hill Component Selection Tables*) and over 1000 figures.

Throughout the revision we have strived to retain the feeling of informality and easy access that made the first edition so successful and popular, both as reference and text. We are aware of the difficulty students often experience when approaching electronics for the first time: The field is densely interwoven, and there is no path of learning that takes you, by logical steps, from neophyte to broadly competent designer. Thus we have added extensive cross-referencing throughout the text; in addition, we have expanded the separate *Laboratory Manual* into a *Student Manual* (*Student Manual for The Art of Electronics*, by Thomas C. Hayes and Paul Horowitz),

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complete with additional worked examples of circuit designs, explanatory material, reading assignments, laboratory exercises, and solutions to selected problems. By offering a student supplement, we have been able to keep this volume concise and rich with detail, as requested by our many readers who use the volume primarily as a reference work.

We hope this new edition responds to all our readers' needs – both students and practicing engineers. We welcome suggestions and corrections, which should be addressed directly to Paul Horowitz, Physics Department, Harvard University, Cambridge, MA 02138.

In preparing this new edition, we are appreciative of the help we received from Mike Aronson and Brian Matthews (AOX, Inc.), John Greene (University of Cape Town), Jeremy Avigad and Tom Hayes (Harvard University), Peter Horowitz (EVI, Inc.), Don Stern, and Owen Walker. We thank Jim Mobley for his excellent copyediting, Sophia Prybylski and David Tranah of Cambridge University Press for their encouragement and professional dedication, and the never-sleeping typesetters at Rosenlaui Publishing Services, Inc. for their masterful composition in TEX.

Finally, in the spirit of modern jurisprudence, we remind you to read the legal notice here appended.

Paul Horowitz
Winfield Hill

March 1989

LEGAL NOTICE

In this book we have attempted to teach the techniques of electronic design, using circuit examples and data that we believe to be accurate. However, the examples, data, and other information are intended solely as teaching aids and should not be used in any particular application without independent testing and verification by the person making the application. Independent testing and verification are especially important in any application in which incorrect functioning could result in personal injury or damage to property.

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PREFACE TO FIRST EDITION

This volume is intended as an electronic circuit design textbook and reference book; it begins at a level suitable for those with no previous exposure to electronics and carries the reader through to a reasonable degree of proficiency in electronic circuit design. We have used a straightforward approach to the essential ideas of circuit design, coupled with an in-depth selection of topics. We have attempted to combine the pragmatic approach of the practicing physicist with the quantitative approach of the engineer, who wants a thoroughly evaluated circuit design.

This book evolved from a set of notes written to accompany a one-semester course in laboratory electronics at Harvard. That course has a varied enrollment – undergraduates picking up skills for their eventual work in science or industry, graduate students with a field of research clearly in mind, and advanced graduate students and postdoctoral researchers who suddenly find themselves hampered by their inability to "do electronics."

It soon became clear that existing textbooks were inadequate for such a course. Although there are excellent treatments of each electronics specialty, written for the planned sequence of a four-year engineering curriculum or for the practicing engineer, those books that attempt to address the whole field of electronics seem to suffer from excessive detail (the handbook syndrome), from oversimplification (the cookbook syndrome), or from poor balance of material. Much of the favorite pedagogy of beginning textbooks is quite unnecessary and, in fact, is not used by practicing engineers, while useful circuitry and methods of analysis in daily use by circuit designers lie hidden in application notes, engineering journals, and hard-to-get data books. In other words, there is a tendency among textbook writers to represent the theory, rather that the art, of electronics.

We collaborated in writing this book with the specific intention of combining the discipline of a circuit design engineer with the perspective of a practicing experimental physicist and teacher of electronics. Thus, the treatment in this book reflects our philosophy that electronics, as currently practiced, is basically a simple art, a combination of some basic laws, rules of thumb, and a large bag of tricks. For these reasons we have omitted entirely the usual discussions of solid-state physics, the *h*-parameter model of transistors, and complicated network theory, and reduced to a bare minimum the mention of load lines and the *s*-plane. The treatment is largely nonmathematical, with strong encouragement of circuit brainstorming and mental (or, at most, back-of-the-envelope) calculation of circuit values and performance.

In addition to the subjects usually treated in electronics books, we have included the following:

- an easy-to-use transistor model
- extensive discussion of useful subcircuits, such as current sources and current mirrors
- single-supply op-amp design
- easy-to-understand discussions of topics on which practical design information is often difficult to find: op-amp frequency

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compensation, low-noise circuits, phase-locked loops, and precision linear design
- simplified design of active filters, with tables and graphs
- a section on noise, shielding, and grounding
- a unique graphical method for streamlined low-noise amplifier analysis
- a chapter on voltage references and regulators, including constant current supplies
- a discussion of monostable multivibrators and their idiosyncrasies
- a collection of digital logic pathology, and what to do about it
- an extensive discussion of interfacing to logic, with emphasis on the new NMOS and PMOS LSI
- a detailed discussion of A/D and D/A conversion techniques
- a section on digital noise generation
- a discussion of minicomputers and interfacing to data buses, with an introduction to assembly language
- a chapter on microprocessors, with actual design examples and discussion – how to design them into instruments, and how to make them do what you want
- a chapter on construction techniques: prototyping, printed circuit boards, instrument design
- a simplified way to evaluate high-speed switching circuits
- a chapter on scientific measurement and data processing: what you can measure and how accurately, and what to do with the data
- bandwidth narrowing methods made clear: signal averaging, multichannel scaling, lock-in amplifiers, and pulse-height analysis
- amusing collections of "bad circuits," and collections of "circuit ideas"
- useful appendixes on how to draw schematic diagrams, IC generic types, *LC* filter design, resistor values, oscilloscopes, mathematics review, and others
- tables of diodes, transistors, FETs, op-amps, comparators, regulators, voltage references, microprocessors, and other devices, generally listing the characteristics of both the most popular and the best types

Throughout we have adopted a philosophy of naming names, often comparing the characteristics of competing devices for use in any circuit, and the advantages of alternative circuit configurations. Example circuits are drawn with real device types, not black boxes. The overall intent is to bring the reader to the point of understanding clearly the choices one makes in designing a circuit – how to choose circuit configurations, device types, and parts values. The use of largely nonmathematical circuit design techniques does not result in circuits that cut corners or compromise performance or reliability. On the contrary, such techniques enhance one's understanding of the real choices and compromises faced in engineering a circuit and represent the best approach to good circuit design.

This book can be used for a full-year electronic circuit design course at the college level, with only a minimum mathematical prerequisite, namely, some acquaintance with trigonometric and exponential functions, and preferably a bit of differential calculus. (A short review of complex numbers and derivatives is included as an appendix.) If the less essential sections are omitted, it can serve as the text for a one-semester course (as it does at Harvard).

A separately available laboratory manual, *Laboratory Manual for the Art of Electronics* (Horowitz and Robinson, 1981), contains twenty-three lab exercises, together with reading and problem assignments keyed to the text.

To assist the reader in navigation, we have designated with open boxes in the margin those sections within each chapter that we feel can be safely passed over in an abbreviated reading. For a one-semester course it would probably be wise

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to omit, in addition, the materials of Chapter 5 (first half), 7, 12, 13, 14, and possibly 15, as explained in the introductory paragraphs of those chapters.

We would like to thank our colleagues for their thoughtful comments and assistance in the preparation of the manuscript, particularly Mike Aronson, Howard Berg, Dennis Crouse, Carol Davis, David Griesinger, John Hagen, Tom Hayes, Peter Horowitz, Bob Kline, Costas Papaliolios, Jay Sage, and Bill Vetterling. We are indebted to Eric Hieber and Jim Mobley, and to Rhona Johnson and Ken Werner of Cambridge University Press, for their imaginative and highly professional work.

Paul Horowitz
Winfield Hill

April 1980

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FEEDBACK AND OPERATIONAL AMPLIFIERS

CHAPTER 4

INTRODUCTION

Feedback has become such a well-known concept that the word has entered the general vocabulary. In control systems, feedback consists in comparing the output of the system with the desired output and making a correction accordingly. The "system" can be almost anything: for instance, the process of driving a car down the road, in which the output (the position and velocity of the car) is sensed by the driver, who compares it with expectations and makes corrections to the input (steering wheel, throttle, brake). In amplifier circuits the output should be a multiple of the input, so in a feedback amplifier the input is compared with an attenuated version of the output.

4.01 Introduction to feedback

Negative feedback is the process of coupling the output back in such a way as to cancel some of the input. You might think that this would only have the effect of reducing the amplifier's gain and would be a pretty stupid thing to do. Harold S. Black, who attempted to patent negative feedback in 1928, was greeted with the same response. In his words, "Our patent application was treated in the same manner as one for a perpetual-motion machine." (See the fascinating article in *IEEE Spectrum*, December 1977.) True, it does lower the gain, but in exchange it also improves other characteristics, most notably freedom from distortion and nonlinearity, flatness of response (or conformity to some desired frequency response), and predictability. In fact, as more negative feedback is used, the resultant amplifier characteristics become less dependent on the characteristics of the open-loop (no-feedback) amplifier and finally depend only on the properties of the feedback network itself. Operational amplifiers are typically used in this *high-loop-gain* limit, with *open-loop* voltage gain (no feedback) of a million or so.

A feedback network can be frequency-dependent, to produce an equalization amplifier (with specific gain-versus-frequency characteristics, an example being the famous RIAA phono amplifier

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characteristic), or it can be amplitude-dependent, producing a nonlinear amplifier (a popular example is a logarithmic amplifier, built with feedback that exploits the logarithmic V_{BE} versus I_C of a diode or transistor). It can be arranged to produce a current source (near-infinite output impedance) or a voltage source (near-zero output impedance), and it can be connected to generate very high or very low input impedance. Speaking in general terms, the property that is sampled to produce feedback is the property that is improved. Thus, if you feed back a signal proportional to the output current, you will generate a good current source.

Feedback can also be *positive*; that's how you make an oscillator, for instance. As much fun as that may sound, it simply isn't as important as negative feedback. More often it's a nuisance, since a negative-feedback circuit may have large enough phase shifts at some high frequency to produce positive feedback and oscillations. It is surprisingly easy to have this happen, and the prevention of unwanted oscillations is the object of what is called *compensation*, a subject we will treat briefly at the end of the chapter.

Having made these general comments, we will now look at a few feedback examples with operational amplifiers.

4.02 Operational amplifiers

Most of our work with feedback will involve operational amplifiers, very high gain dc-coupled differential amplifiers with single-ended outputs. You can think of the classic long-tailed pair (Section 2.18) with its two inputs and single output as a prototype, although real op-amps have much higher gain (typically 10^5 to 10^6) and lower output impedance and allow the output to swing through most of the supply range (you usually use a split supply, most often ± 15V). Operational amplifiers are now available in literally hundreds of types, with the universal symbol shown in Figure 4.1, where the (+) and (−) inputs do as expected: The output goes positive when the noninverting input (+) goes more positive than the inverting input (−), and vice versa. The (+) and (−) symbols don't mean that you have to keep one positive with respect to the other, or anything like that; they just tell you the relative phase of the output (which is important to keep negative feedback negative). Using the words "noninverting" and "inverting," rather than "plus" and "minus," will help avoid confusion. Power-supply connections are frequently not displayed, and there is no ground terminal. Operational amplifiers have enormous voltage gain, and they are *never* (well, hardly ever) used without feedback. Think of an op-amp as fodder for feedback. The open-loop gain is so high that for any reasonable closed-loop gain, the characteristics depend only on the feedback network. Of course, at some level of scrutiny this generalization must fail. We will start with a naive view of op-amp behavior and fill in some of the finer points later, when we need to.

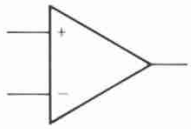


Figure 4.1

There are literally hundreds of different op-amps available, offering various performance trade-offs that we will explain later (look ahead to Table 4.1 if you want to be overwhelmed by what's available). A very good all-around performer is the popular LF411 ("411" for short), originally introduced by National Semiconductor. Like all op-amps, it is a wee beastie packaged in the so-called mini-DIP (dual in-line package), and it looks

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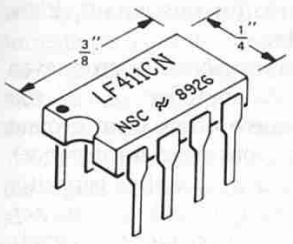


Figure 4.2. Mini-DIP integrated circuit.

as shown in Figure 4.2. It is inexpensive (about 60 cents) and easy to use; it comes in an improved grade (LF411A) and also in a mini-DIP containing two independent op-amps (LF412, called a "dual" op-amp). We will adopt the LF411 throughout this chapter as our "standard" op-amp, and we recommend it as a good starting point for your circuit designs.

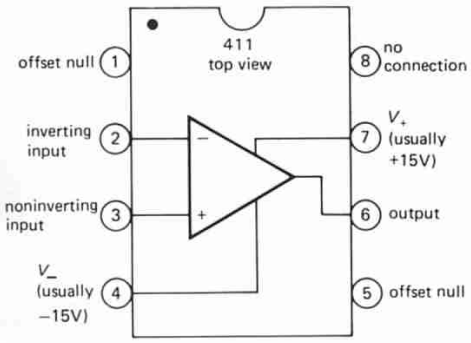


Figure 4.3

Inside the 411 is a piece of silicon containing 24 transistors (21 BJTs, 3 FETs), 11 resistors, and 1 capacitor. The pin connections are shown in Figure 4.3. The dot in the corner, or notch at the end of the package, identifies the end from which to begin counting the pin numbers. As with most electronic packages, you count pins counterclockwise, viewing from the top. The "offset null" terminals (also known as "balance" or "trim") have to do with correcting (externally) the small asymmetries that are unavoidable when making the op-amp. You will learn about this later in the chapter.

4.03 The golden rules

Here are the simple rules for working out op-amp behavior with external feedback. They're good enough for almost everything you'll ever do.

First, the op-amp voltage gain is so high that a fraction of a millivolt between the input terminals will swing the output over its full range, so we ignore that small voltage and state golden rule I:

I. The output attempts to do whatever is necessary to make the voltage difference between the inputs zero.

Second, op-amps draw very little input current (0.2nA for the LF411; picoamps for low-input-current types); we round this off, stating golden rule II:

II. The inputs draw no current.

One important note of explanation: Golden rule I doesn't mean that the op-amp actually changes the voltage at its *inputs*. It can't do that. (How could it, and be consistent with golden rule II?) What it does is "look" at its input terminals and swing its output terminal around so that the external feedback network brings the input differential to zero (if possible).

These two rules get you quite far. We will illustrate with some basic and important op-amp circuits, and these will prompt a few cautions listed in Section 4.08.

BASIC OP-AMP CIRCUITS

4.04 Inverting amplifier

Let's begin with the circuit shown in Figure 4.4. The analysis is simple, if you remember your golden rules:

I. Point B is at ground, so rule I implies that point A is also.

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2. This means that (a) the voltage across R_2 is V_{out} and (b) the voltage across R_1 is V_{in}.

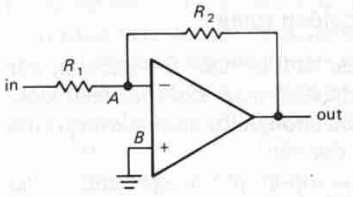


Figure 4.4. Inverting amplifier.

3. So, using rule II, we have

$$V_{out}/R_2 = -V_{in}/R_1$$

In other words,

$$\text{voltage gain} = V_{out}/V_{in} = -R_2/R_1$$

Later you will see that it's often better not to ground B directly, but through a resistor. However, don't worry about that now.

Our analysis seems almost too easy! In some ways it obscures what is actually happening. To understand how feedback works, just imagine some input level, say +1 volt. For concreteness, imagine that R_1 is 10k and R_2 is 100k. Now, suppose the output decides to be uncooperative, and sits at zero volts. What happens? R_1 and R_2 form a voltage divider, holding the inverting input at +0.91 volt. The op-amp sees an enormous input unbalance, forcing the output to go negative. This action continues until the output is at the required −10.0 volts, at which point both op-amp inputs are at the same voltage, namely ground. Similarly, any tendency for the output to go more negative than −10.0 volts will pull the inverting input below ground, forcing the output voltage to rise.

What is the input impedance? Simple. Point A is always at zero volts (it's called a *virtual ground*). So $Z_{in} = R_1$. At this point you don't yet know how to figure the output impedance; for this circuit, it's a fraction of an ohm.

Note that this analysis is true even for dc – it's a dc amplifier. So if you have a signal source offset from ground (collector of a previous stage, for instance), you may want to use a coupling capacitor (sometimes called a blocking capacitor, since it blocks dc but couples the signal). For reasons you will see later (having to do with departures of op-amp behavior from the ideal), it is usually a good idea to use a blocking capacitor if you're only interested in ac signals anyway.

This circuit is known as an *inverting amplifier*. Its one undesirable feature is the low input impedance, particularly for amplifiers with large (closed-loop) voltage gain, where R_1 tends to be rather small. That is remedied in the next circuit (Fig. 4.5).

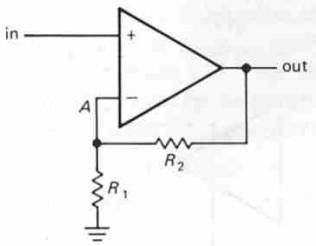


Figure 4.5. Noninverting amplifier.

4.05 Noninverting amplifier

Consider Figure 4.5. Again, the analysis is simplicity itself:

$$V_A = V_{in}$$

But V_A comes from a voltage divider:

$$V_A = V_{out}R_1/(R_1 + R_2)$$

Set $V_A = V_{in}$, and you get

$$\text{gain} = V_{out}/V_{in} = 1 + R_2/R_1$$

This is a *noninverting amplifier*. In the approximation we are using, the input impedance is infinite (with the 411 it would be $10^{12}\Omega$ or more; a bipolar op-amp

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will typically exceed $10^8\Omega$). The output impedance is still a fraction of an ohm. As with the inverting amplifier, a detailed look at the voltages at the inputs will persuade you that it works as advertised.

Once again we have a dc amplifier. If the signal source is ac-coupled, you must provide a return to ground for the (very small) input current, as in Figure 4.6. The component values shown give a voltage gain of 10 and a low-frequency 3dB point of 16Hz.

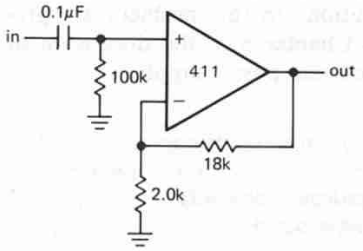


Figure 4.6

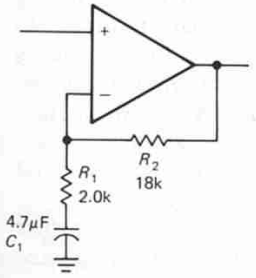


Figure 4.7

An ac amplifier

Again, if only ac signals are being amplified, it is often a good idea to "roll off" the gain to unity at dc, especially if the amplifier has large voltage gain, in order to reduce the effects of finite "input offset voltage." The circuit in Figure 4.7 has a low-frequency 3dB point of 17Hz, the frequency at which the impedance of the capacitor equals 2.0k. Note the large capacitor value required. For noninverting amplifiers with high gain, the capacitor in this ac amplifier configuration may be undesirably large. In that case it may be preferable to omit the capacitor and trim the offset voltage to zero, as we will discuss later (Section 4.12). An alternative is to raise R_1 and R_2, perhaps using a T network for the latter (Section 4.18).

In spite of its desirable high input impedance, the noninverting amplifier configuration is not necessarily to be preferred over the inverting amplifier configuration in all circumstances. As we will see later, the inverting amplifier puts less demand on the op-amp and therefore gives somewhat better performance. In addition, its virtual ground provides a handy way to combine several signals without interaction. Finally, if the circuit in question is driven from the (stiff) output of another op-amp, it makes no difference whether the input impedance is 10k (say) or infinity, because the previous stage has no trouble driving it in either case.

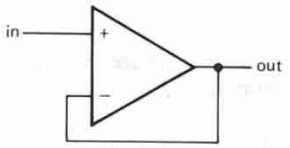


Figure 4.8. Follower.

4.06 Follower

Figure 4.8 shows the op-amp version of an emitter follower. It is simply a noninverting amplifier with R_1 infinite and R_2 zero (gain = 1). There are special op-amps, usable only as followers, with improved characteristics (mainly higher speed), e.g., the LM310 and the OPA633, or with simplified connections, e.g., the TL068 (which comes in a 3-pin transistor package).

An amplifier of unity gain is sometimes called a *buffer* because of its isolating

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properties (high input impedance, low output impedance).

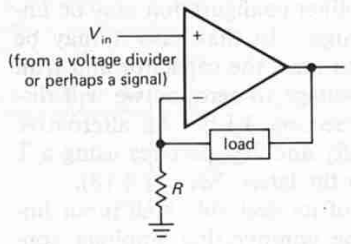


Figure 4.9

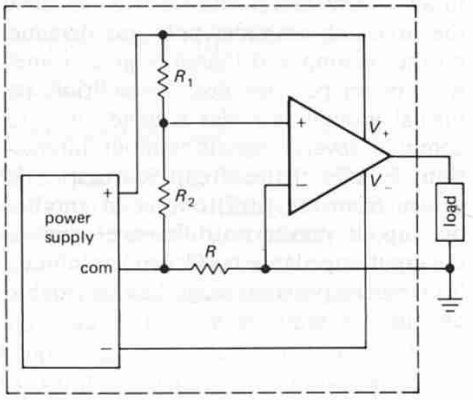


Figure 4.10. Current source with grounded load and floating power supply.

4.07 Current sources

The circuit in Figure 4.9 approximates an ideal current source, without the V_{BE} offset of a transistor current source. Negative feedback results in V_{in} at the inverting input, producing a current $I = V_{\text{in}}/R$ through the load. The major disadvantage of this circuit is the "floating" load (neither side grounded). You couldn't generate a usable sawtooth wave with respect to ground with this current source, for instance. One solution is to float the whole circuit (power supplies and all) so that you can ground one side of the load (Fig. 4.10). The circuit in the box is the previous current source, with its power supplies shown explicitly. R_1 and R_2 form a voltage divider to set the current. If this circuit seems confusing, it may help to remind yourself that "ground" is a relative concept. Any one point in a circuit could be called ground. This circuit is useful for generating currents into a load that is returned to ground, but it has the disadvantage that the control input is now floating, so you cannot program the output current with an input voltage referenced to ground. Some solutions to this problem are presented in Chapter 6 in the discussion of constant-current power supplies.

Current sources for loads returned to ground

With an op-amp and external transistor it is possible to make a simple high-quality current source for a load returned to ground; a little additional circuitry makes it possible to use a programming input referenced to ground (Fig. 4.11). In the first circuit, feedback forces a voltage $V_{CC} - V_{\text{in}}$ across R, giving an emitter current (and therefore an output current) $I_E = (V_{CC} - V_{\text{in}})/R$. There are no V_{BE} offsets, or their variations with temperature, I_C, V_{CE}, etc., to worry about. The current source is imperfect (ignoring op-amp errors: I_b, V_{os}) only insofar as the small base current may vary somewhat with V_{CE} (assuming the op-amp draws no input current), not too high a price to pay for the convenience of a grounded load; a Darlington for Q_1 would reduce this error considerably. This error comes about, of course, because the op-amp stabilizes the *emitter* current, whereas the load sees the *collector* current. A variation of this circuit, using a FET instead of a bipolar transistor, avoids this problem altogether, since FETs draw no gate current.

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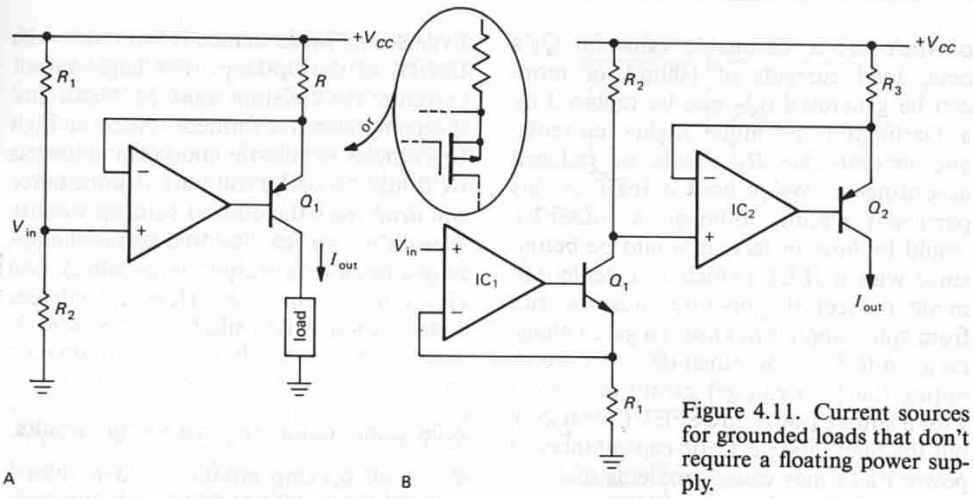


Figure 4.11. Current sources for grounded loads that don't require a floating power supply.

With this circuit the output current is proportional to the voltage drop below V_{CC} applied to the op-amp's noninverting input; in other words, the programming voltage is referenced to V_{CC}, which is fine if V_{in} is a fixed voltage generated by a voltage divider, but an awkward situation if an external input is to be used. This is remedied in the second circuit, in which a similar current source with *npn* transistor is used to convert an input voltage (referenced to ground) to a V_{CC}-referenced input to the final current source. Op-amps and transistors are inexpensive. Don't hesitate to use a few extra components to improve performance or convenience in circuit design.

One important note about the last circuit: The op-amp must be able to operate with its inputs near or at the positive supply voltage. An op-amp like the 307, 355, or OP-41 is good here. Alternatively, the op-amp could be powered from a separate V_+ voltage higher than V_{CC}.

EXERCISE 4.1

What is the output current in the last circuit for a given input voltage V_{in}?

Figure 4.12 shows an interesting variation on the op-amp/transistor current source. It has the advantage of zero base current error, which you get with FETs, without being restricted to output currents less than $I_{DS(ON)}$. In this circuit (actually a current *sink*), Q_2 begins to conduct when Q_1 is drawing about 0.6mA drain current. With Q_1's minimum I_{DSS}

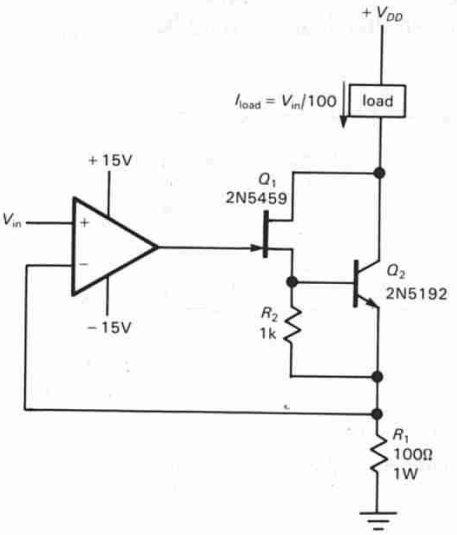


Figure 4.12. FET/bipolar current source suitable for high currents.

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of 4mA and a reasonable value for Q_2's beta, load currents of 100mA or more can be generated (Q_2 can be replaced by a Darlington for much higher currents, and in that case R_1 should be reduced accordingly). We've used a JFET in this particular circuit, although a MOSFET would be fine; in fact, it would be better, since with a JFET (which is a depletion-mode device) the op-amp must be run from split supplies to ensure a gate voltage range sufficient for pinch-off. It's worth noting that you can get plenty of current with a simple power MOSFET ("VMOS"); but the high interelectrode capacitances of power FETs may cause problems that you avoid with the hybrid circuit here.

Howland current source

Figure 4.13 shows a nice "textbook" current source. If the resistors are chosen so that $R_3/R_2 = R_4/R_1$, then it can be shown that $I_{\text{load}} = -V_{\text{in}}/R_2$.

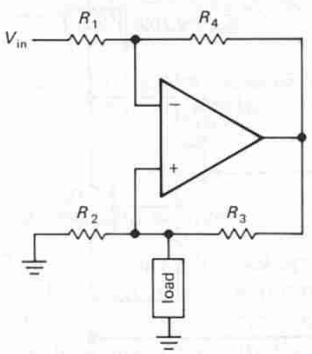


Figure 4.13. Howland current source.

EXERCISE 4.2
Show that the preceding result is correct.

This sounds great, but there's a hitch: The resistors must be matched exactly; otherwise it isn't a perfect current source. Even so, its performance is limited by the CMRR of the op-amp. For large output currents, the resistors must be small, and the compliance is limited. Also, at high frequencies (where the loop gain is low, as we'll learn shortly) the output impedance can drop from the desired value of infinity to as little as a few hundred ohms (the op-amp's open-loop output impedance). As clever as it looks, the Howland current source is not widely used.

4.08 Basic cautions for op-amp circuits

1. In all op-amp circuits, golden rules I and II (Section 4.03) will be obeyed only if the op-amp is in the active region, i.e., inputs and outputs not saturated at one of the supply voltages.

For instance, overdriving one of the amplifier configurations will cause output clipping at output swings near V_{CC} or V_{EE}. During clipping, the inputs will no longer be maintained at the same voltage. The op-amp output cannot swing beyond the supply voltages (typically it can swing only to within 2V of the supplies, though certain op-amps are designed to swing all the way to one supply or the other). Likewise, the output compliance of an op-amp current source is set by the same limitation. The current source with floating load, for instance, can put a maximum of $V_{CC} - V_{\text{in}}$ across the load in the "normal" direction (current in the same direction as applied voltage) and $V_{\text{in}} - V_{EE}$ in the reverse direction (the load could be rather strange, e.g., it might contain batteries, requiring the reverse sense of voltage to get a forward current; the same thing might happen with an inductive load driven by changing currents).

2. The feedback must be arranged so that it is negative. This means (among other things) that you must not mix up the inverting and noninverting inputs.

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3. There must always be feedback at dc in an op-amp circuit. Otherwise the op-amp is guaranteed to go into saturation.

For instance, we were able to put a capacitor from the feedback network to ground in the noninverting amplifier (to reduce gain at dc to 1, Fig. 4.7), but we could not similarly put a capacitor in series between the output and the inverting input.

4. Many op-amps have a relatively small maximum differential input voltage limit. The maximum voltage difference between the inverting and noninverting inputs might be limited to as little as 5 volts in either polarity. Breaking this rule will cause large input currents to flow, with degradation or destruction of the op-amp.

We will take up some more issues of this type in Section 4.11 and again in Section 7.06 in connection with precision circuit design.

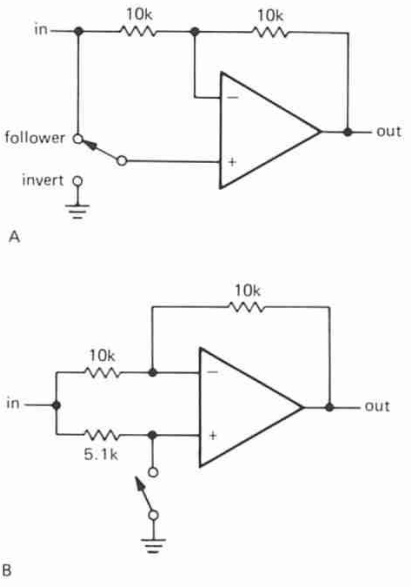


Figure 4.14

AN OP-AMP SMORGASBORD

In the following examples we will skip the detailed analysis, leaving that fun for you, the reader.

4.09 Linear circuits

Optional inverter

The circuits in Figure 4.14 let you invert, or amplify without inversion, by flipping a switch. The voltage gain is either +1 or −1, depending on the switch position.

EXERCISE 4.3

Show that the circuits in Figure 4.14 work as advertised.

Follower with bootstrap

As with transistor amplifiers, the bias path can compromise the high input impedance you would otherwise get with an op-amp,

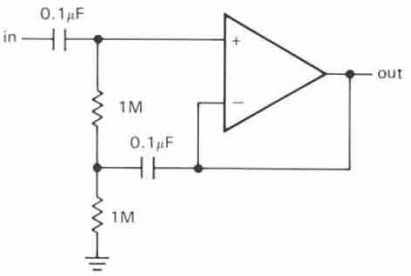


Figure 4.15

particularly with ac-coupled inputs, where a resistor to ground is mandatory. If that is a problem, the bootstrap circuit shown in Figure 4.15 is a possible solution. As in the transistor bootstrap circuit (Section 2.17), the 0.1μF capacitor makes the upper 1M resistor look like a high-impedance current source to input signals. The low-frequency rolloff for this circuit will begin at about 10Hz, dropping at 12dB per octave for frequencies somewhat below this. Note: You might be tempted to

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reduce the input coupling capacitor, since its load has been bootstrapped to high impedance. However, this can generate a peak in the frequency response, in the manner of an active filter (see Section 5.06).

Ideal current-to-voltage converter

Remember that the humble resistor is the simplest I-to-V converter. However, it has the disadvantage of presenting a nonzero impedance to the source of input current; this can be fatal if the device providing the input current has very little compliance or does not produce a constant current as the output voltage changes. A good example is a *photovoltaic cell*, a fancy name for a sun battery. Even the garden-variety signal diodes you use in circuits have a small photovoltaic effect (there are amusing stories of bizarre circuit behavior finally traced to this effect). Figure 4.16 shows the good way to convert current

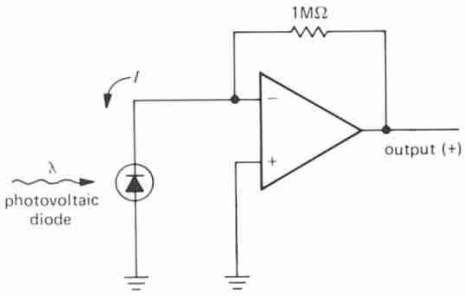


Figure 4.16

to voltage while holding the input strictly at ground. The inverting input is a virtual ground; this is fortunate, since a photovoltaic diode can generate only a few tenths of a volt. This particular circuit has an output of 1 volt per microamp of input current. (With BJT-input op-amps you sometimes see a resistor connected between the noninverting input and ground; its function will be explained shortly in connection with op-amp shortcomings.)

Of course, this *transresistance* configuration can be used equally well for devices that source their current via some positive excitation voltage, such as V_{CC}. Photomultiplier tubes and phototransistors (both devices that source current from a positive supply when exposed to light) are often used this way (Fig. 4.17).

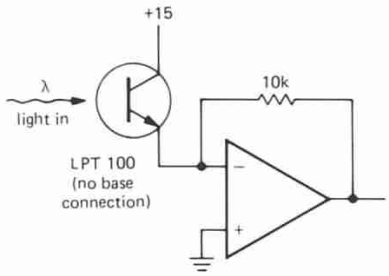


Figure 4.17

EXERCISE 4.4

Use a 411 and a 1mA (full scale) meter to construct a "perfect" current meter (i.e., one with zero input impedance) with 5mA full scale. Design the circuit so that the meter will never be driven more than ±150% full scale. Assume that the 411 output can swing to ±13 volts (±15V supplies) and that the meter has 500 ohms internal resistance.

Differential amplifier

The circuit in Figure 4.18 is a differential amplifier with gain R_2/R_1. As with the current source that used matched resistor ratios, this circuit requires precise resistor matching to achieve high common-mode rejection ratios. The best procedure is to stock up on a bunch of 100k 0.01% resistors next time you have a chance. All your differential amplifiers will have unity gain, but that's easily remedied with further (single-ended) stages of gain. We will treat differential amplifiers in more detail in Chapter 7.

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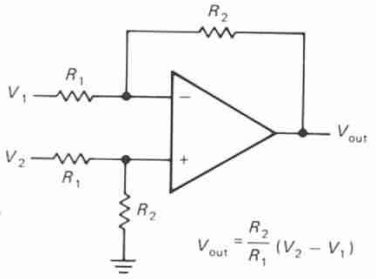


Figure 4.18. Classic differential amplifier.

Summing amplifier

The circuit shown in Figure 4.19 is just a variation of the inverting amplifier. Point X is a virtual ground, so the input current is $V_1/R + V_2/R + V_3/R$. That gives $V_{out} = -(V_1 + V_2 + V_3)$. Note that the inputs can be positive or negative. Also, the input resistors need not be equal; if they're unequal, you get a weighted sum. For instance, you could have four inputs, each of which is +1 volt or zero, representing binary values 1, 2, 4, and 8. By using input resistors of 10k, 5k, 2.5k, and 1.25k you will get an output in volts equal to the binary count input. This scheme can be easily expanded to several digits. It is the basis of digital-to-analog conversion, although a different input circuit (an $R-2R$ ladder) is usually used.

EXERCISE 4.5

Show how to make a two-digit digital-to-analog converter by appropriately scaling the input resistors in a summing amplifier. The digital input represents two digits, each consisting of four lines that represent the values 1, 2, 4, and 8 for the respective digits. An input line is either at +1 volt or at ground, i.e., the eight input lines represent 1, 2, 4, 8, 10, 20, 40, and 80. Because op-amp outputs generally cannot swing beyond ±13 volts, you will have to settle for an output in volts equal to one-tenth the value of the input number.

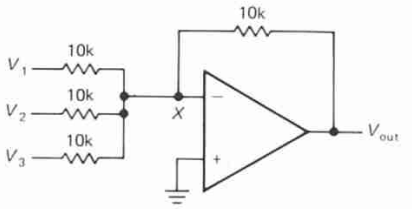
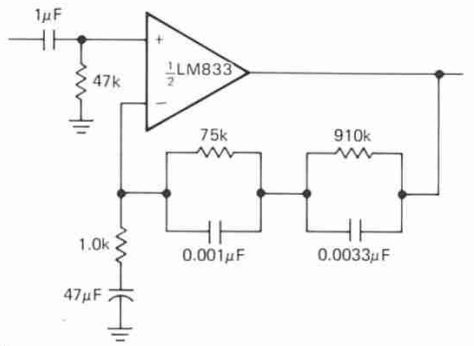
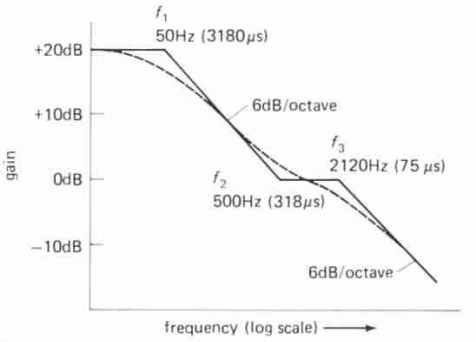


Figure 4.19



A



B

Figure 4.20. Op-amp RIAA phono playback amplifier.

RIAA preamp

The RIAA preamp is an example of an amplifier with a specifically tailored frequency response. Phonograph records are cut with approximately flat amplitude characteristics; magnetic pickups, on the other hand, respond to velocity, so a playback amplifier with rising bass response is required.

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The circuit shown in Figure 4.20 produces the required response. The RIAA playback amplifier frequency response (relative to 0dB at 1kHz) is shown in the graph, with the breakpoints given in terms of time constants. The 47μF capacitor to ground rolls off the gain to unity at dc, where it would otherwise be about 1000; as we have hinted earlier, the reason is to avoid amplification of dc input "offsets." The LM833 is a low-noise dual op-amp intended for audio applications (a "gold-plated" op-amp for this application is the ultra-low-noise LT1028, which is 13dB quieter, and 10dB more expensive, than the 833!).

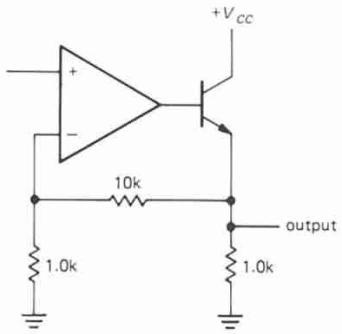


Figure 4.21

Power booster

For high output current, a power transistor follower can be hung on an op-amp output (Fig. 4.21). In this case a noninverting amplifier has been drawn; the follower can be added to any op-amp configuration. Notice that feedback is taken from the emitter; thus, feedback enforces the desired output voltage in spite of the V_{BE} drop. This circuit has the usual problem that the follower output can only *source* current. As with transistor circuits, the remedy is a push-pull booster (Fig. 4.22). You will see later that the limited speed with which the op-amp can move its output (slew rate) seriously limits the speed

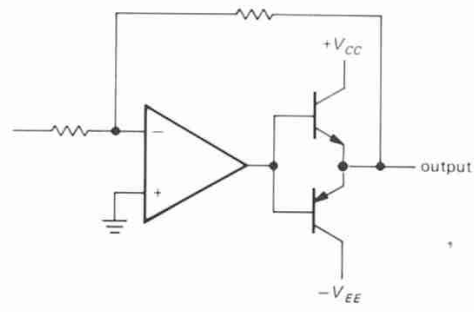


Figure 4.22

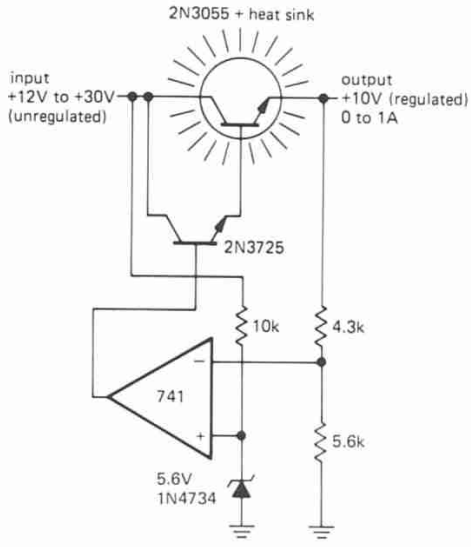


Figure 4.23

of this booster in the crossover region, creating distortion. For slow-speed applications you don't need to bias the push-pull pair into quiescent conduction, because feedback will take care of most of the crossover distortion. Commercial op-amp power boosters are available, e.g., the LT1010, OPA633, and 3553. These are unity-gain push-pull amplifiers capable of 200mA of output current and operation to 100MHz and above. You can include them inside the feedback loop without any worries (See Table 7.4).

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Power supply

An op-amp can provide the gain for a feedback voltage regulator (Fig. 4.23). The op-amp compares a sample of the output with the zener reference, changing the drive to the Darlington "pass transistor" as needed. This circuit supplies 10 volts regulated, at up to 1 amp load current. Some notes about this circuit:

1. The voltage divider that samples the output could be a potentiometer, for adjustable output voltage.

2. For reduced ripple at the zener, the 10k resistor should be replaced by a current source. Another approach is to bias the zener from the output; that way you take advantage of the regulator you have built. Caution: When using this trick, you must analyze the circuit carefully to be sure it will start up when power is first applied.

3. The circuit as drawn could be damaged by a temporary short circuit across the output, because the op-amp would attempt to drive the Darlington pair into heavy conduction. Regulated power supplies should always have circuitry to limit "fault" current (see Section 6.05 for more details).

4. Integrated circuit voltage regulators are available in tremendous variety, from the time-honored 723 to the convenient 3-terminal adjustable regulators with internal current limit and thermal shutdown (see Tables 6.8–6.10). These devices, complete with temperature-compensated internal zener reference and pass transistor, are so easy to use that you will almost never use a general-purpose op-amp as a regulator. The exception might be to generate a stable voltage within a circuit that already has a stable power-supply voltage available.

In Chapter 6 we will discuss voltage regulators and power supplies in detail, including special ICs intended for use as voltage regulators.

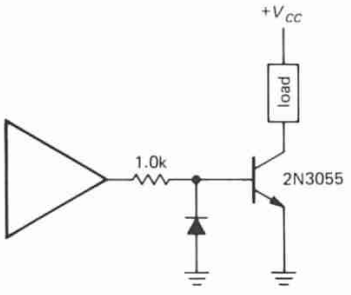


Figure 4.24

4.10 Nonlinear circuits

Power-switching driver

For loads that are either on or off, a switching transistor can be driven from an op-amp. Figure 4.24 shows how. Note the diode to prevent reverse base-emitter breakdown (op-amps easily swing more than −5V). The 2N3055 is everyone's power transistor for noncritical high-current applications. A Darlington (or power MOSFET) can be used if currents greater than about 1 amp need to be driven.

Active rectifier

Rectification of signals smaller than a diode drop cannot be done with a simple diode-resistor combination. As usual, op-amps come to the rescue, in this case by putting a diode in the feedback loop (Fig. 4.25). For V_{in} positive, the diode provides negative feedback; the output follows the input, coupled by the diode, but without a V_{BE} drop. For V_{in} negative, the op-amp goes into negative saturation and V_{out} is at ground. R could be chosen smaller for lower output impedance, with the tradeoff of higher op-amp output current. A better solution is to use an op-amp follower at the output, as shown, to produce very low output impedance regardless of the resistor value.

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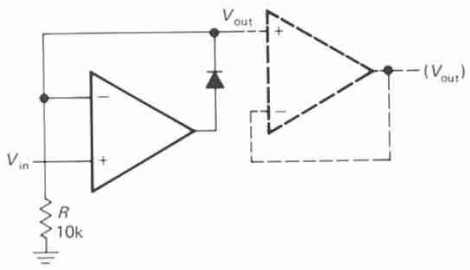


Figure 4.25. Simple active rectifier.

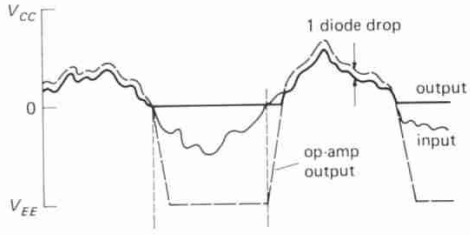


Figure 4.26. Effect of finite slew rate on the simple active rectifier.

There is a problem with this circuit that becomes serious with high-speed signals. Because an op-amp cannot swing its output infinitely fast, the recovery from negative saturation (as the input waveform passes through zero from below) takes some time, during which the output is incorrect. It looks something like the curve shown in Figure 4.26. The output (heavy line) is an accurate rectified version of the input (light line), except for a short time interval after the input rises through zero volts. During that interval the op-amp output is racing up from saturation near $-V_{EE}$, so the circuit's output is still at ground. A general-purpose op-amp like the 411 has a *slew rate* (maximum rate at which the output can change) of 15 volts per microsecond; recovery from negative saturation therefore takes about 1μs, which may introduce significant output error for fast signals. A circuit modification improves the situation considerably (Fig. 4.27).

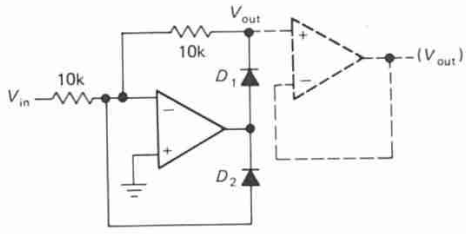


Figure 4.27. Improved active rectifier.

D_1 makes the circuit a unity-gain inverter for negative input signals. D_2 clamps the op-amp's output at one diode drop below ground for positive inputs, and since D_1 is then back-biased, V_{out} sits at ground. The improvement comes because the op-amp's output swings only two diode drops as the input signal passes through zero. Since the op-amp output has to slew only about 1.2 volts instead of V_{EE} volts, the "glitch" at zero crossings is reduced more than tenfold. This rectifier is inverting, incidentally. If you require a noninverted output, attach a unity-gain inverter to the output.

The performance of these circuits is improved if you choose an op-amp with a high slew rate. Slew rate also influences the performance of the other op-amp applications we've discussed, for instance the simple voltage amplifier circuits. At this point it is worth pausing for a while to see in what ways real op-amps depart from the ideal, since that influences circuit design, as we have hinted on several occasions. A good understanding of op-amp limitations and their influence on circuit design and performance will help you choose your op-amps wisely and design with them effectively.

A DETAILED LOOK AT OP-AMP BEHAVIOR

Figure 4.28 shows the schematic of the 741, a very popular op-amp. Its circuit is

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relatively straightforward, in terms of the kinds of transistor circuits we discussed in the last chapter. It has a differential input stage with current mirror load, followed by a common-emitter *npn* stage (again with active load) that provides most of the voltage gain. A *pnp* emitter follower drives the push-pull emitter follower output stage, which includes current-limiting circuitry. This circuit is typical of many op-amps now available. For many applications the properties of these amplifiers approach ideal op-amp performance characteristics. We will now take a look at the extent to which real op-amps depart from the ideal, what the consequences are for circuit design, and what to do about it.

4.11 Departure from ideal op-amp performance

The ideal op-amp has these characteristics:
1. Input impedance (differential or common mode) = infinity
2. Output impedance (open loop) = 0
3. Voltage gain = infinity
4. Common-mode voltage gain = 0
5. $V_{out} = 0$ when both inputs are at the same voltage (zero "offset voltage")
6. Output can change instantaneously (infinite slew rate)

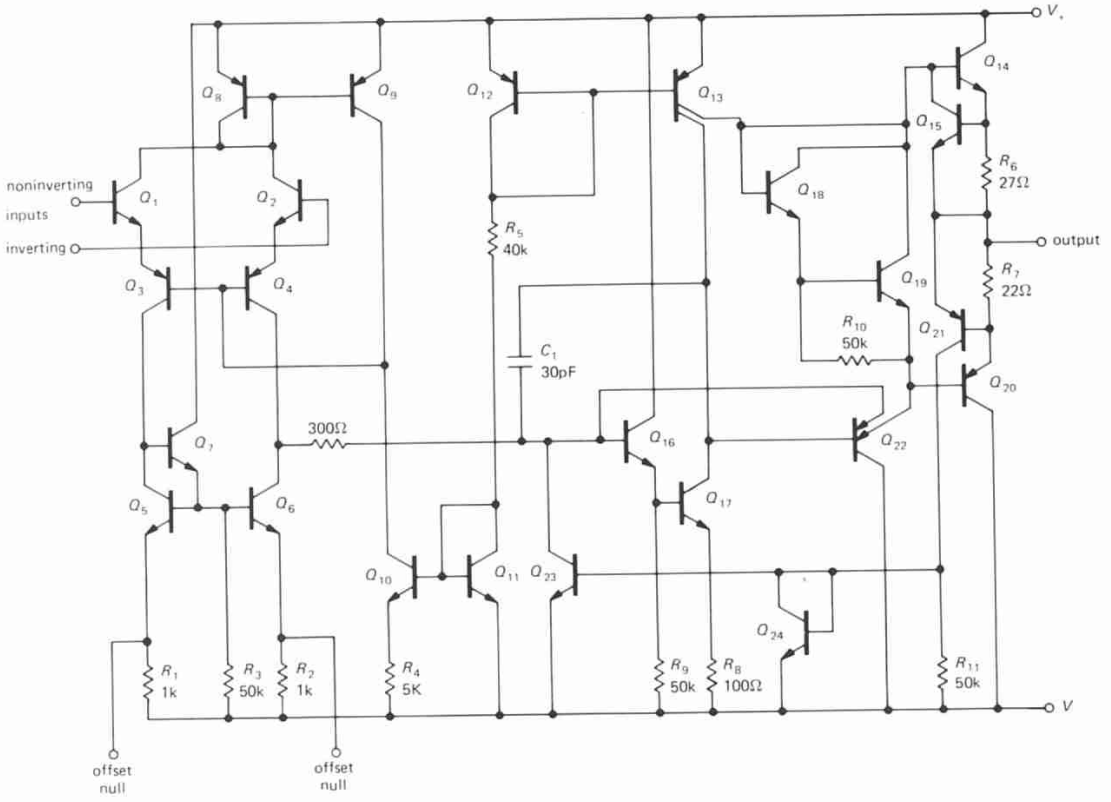


Figure 4.28. Schematic of the 741 op-amp. (Courtesy of Fairchild Camera and Instrument Corp.)

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All of these characteristics are independent of temperature and supply voltage changes.

Real op-amps depart from these characteristics in the following ways (see Table 4.1 for some typical values).

Input current

The input terminals sink (or source, depending on the op-amp type) a small current called the input bias current, I_B, which is defined as half the sum of the input currents with the inputs tied together (the two input currents are approximately equal and are simply the base or gate currents of the input transistors). For the JFET-input 411 the bias current is typically 50pA at room temperature (but as much as 2nA at 70°C), while a typical BJT-input op-amp like the OP-27 has a typical bias current of 15nA, varying little with temperature. As a rough guide, BJT-input op-amps have bias currents in the tens of nanoamps, while FET-input op-amps have input currents in the tens of picoamps (i.e., 1000 times lower). Generally speaking, you can ignore input current with FET op-amps, but not with bipolar-input op-amps.

The significance of input bias current is that it causes a voltage drop across the resistors of the feedback network, bias network, or source impedance. How small a resistor this restricts you to depends on the dc gain of your circuit and how much output variation you can tolerate. You will see how this works later.

Op-amps are available with input bias currents down to a nanoamp or less for (bipolar) transistor-input circuit types or down to a few picoamps ($10^{-6}\mu$A) for FET-input circuit types. The very lowest bias currents are typified by the superbeta Darlington LM11, with a maximum input current of 50pA, the AD549, with an input current of 0.06pA, and the MOSFET ICH8500, with an input current of 0.01pA. In general, transistor op-amps intended for high-speed operation have higher bias currents.

Input offset current

Input offset current is a fancy name for the difference in input currents between the two inputs. Unlike input bias current, the offset current, I_{os}, is a result of manufacturing variations, since an op-amp's symmetrical input circuit would otherwise result in identical bias currents at the two inputs. The significance is that even when it is driven by identical source impedances, the op-amp will see unequal voltage drops and hence a difference voltage between its inputs. You will see shortly how this influences design.

Typically, the offset current is one-half to one-tenth the bias current. For the 411, $I_{\text{offset}} = 25$pA, typical.

□ *Input impedance*

Input impedance refers to the differential input resistance (impedance looking into one input, with the other input grounded), which is usually much less than the common-mode resistance (a typical input stage looks like a long-tailed pair with current source). For the FET-input 411 it is about 10^{12} ohms, while for BJT-input op-amps like the 741 it is about 2MΩ. Because of the input bootstrapping effect of negative feedback (it attempts to keep both inputs at the same voltage, thus eliminating most of the differential input signal), Z_{in} in practice is raised to very high values and usually is not as important a parameter as input bias current.

□ *Common-mode input range*

The inputs to an op-amp must stay within a certain voltage range, typically less than the full supply range, for proper operation. If the inputs go beyond this range, the gain of the op-amp may change drastically, even reversing sign! For a 411 operating

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from ±15 volt supplies, the guaranteed common-mode input range is ±11 volts minimum. However, the manufacturer claims that the 411 will operate with common-mode inputs all the way to the positive supply, though performance may be degraded. Bringing either input down to the negative supply voltage causes the amplifier to go berserk, with symptoms like phase reversal and output saturation to the positive supply.

There are op-amps available with common-mode input ranges down to the negative supply, e.g., the LM358 (a good dual op-amp) or the LM10, CA3440, or OP-22, and up to the positive supply, e.g., the 301, OP-41, or the 355 series. In addition to the *operating* common-mode range, there are maximum allowable input voltages beyond which damage will result. For the 411 they are ±15 volts (but not to exceed the negative supply voltage, if it is less).

Differential input range

Some bipolar op-amps allow only a limited voltage between the inputs, sometimes as small as ±0.5 volt, although most are more forgiving, permitting differential inputs nearly as large as the supply voltages. Exceeding the specified maximum can degrade or destroy the op-amp.

□ *Output impedance; output swing versus load resistance*

Output impedance R_0 means the op-amp's intrinsic output impedance *without feedback*. For the 411 it is about 40 ohms, but with some low-power op-amps it can be as high as several thousand ohms (see Fig. 7.16). Feedback lowers the output impedance into insignificance (or raises it, for a current source); so what usually matters more is the maximum output current, with typical values of 20mA or so. This is frequently given as a graph of output voltage swing V_{om} as a function of load resistance, or sometimes just a few values for typical load resistances. Many op-amps have asymmetrical output drive capability, with the ability to sink more current than they can source (or vice versa). For the 411, output swings to within about 2 volts of V_{CC} and V_{EE} are possible into load resistances greater than about 1k. Load resistances significantly less than that will permit only a small swing. Some op-amps can produce output swings all the way down to the negative supply (e.g., the LM358), a particularly useful feature for circuits operated from a single positive supply, since output swings all the way to ground are then possible. Finally, op-amps with MOS transistor outputs (e.g., the CA3130, 3160, ALD1701, and ICL761x) can swing all the way to both rails. The remarkable bipolar LM10 shares this property, without the limited supply voltage range of the MOS op-amps (usually ±8V max).

□ *Voltage gain and phase shift*

Typically the voltage gain A_{vo} at dc is 100,000 to 1,000,000 (often specified in decibels), dropping to unity gain at a frequency (called f_T) of 1MHz to 10MHz. This is usually given as a graph of open-loop voltage gain as a function of frequency. For *internally compensated* op-amps this graph is simply a 6dB/octave rolloff beginning at some fairly low frequency (for the 411 it begins at about 10Hz), an intentional characteristic necessary for stability, as you will see in Section 4.32. This rolloff (the same as a simple RC low-pass filter) results in a constant 90° lagging phase shift from input to output (open-loop) at all frequencies above the beginning of the rolloff, increasing to 120° to 160° as the open-loop gain approaches unity. Since a 180° phase shift at a frequency where the voltage gain equals 1 will result in positive feedback (oscillations), the term "phase margin" is used to specify the difference between the phase shift at f_T and 180°.

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Input offset voltage

Op-amps don't have perfectly balanced input stages, owing to manufacturing variations. If you connect the two inputs together for zero input signal, the output will usually saturate at either V_{CC} or V_{EE} (you can't predict which). The difference in input voltages necessary to bring the output to zero is called the input offset voltage V_{os} (it's as if there were a battery of that voltage in series with one of the inputs). Usually op-amps make provision for trimming the input offset voltage to zero. For a 411 you use a 10k pot between pins 1 and 5, with the wiper connected to V_{EE}.

Of greater importance for precision applications is the drift of the input offset voltage with temperature and time, since any initial offset can be trimmed to zero. A 411 has a typical offset voltage of 0.8mV (2mV maximum), with temperature coefficient ("tempco") of 7μV/°C and unspecified coefficient of offset drift with time. The OP-77, a precision op-amp, is laser-trimmed for a typical offset of 10 *microvolts*, with temperature coefficient TCV_{os} of 0.2μV/°C and long-term drift of 0.2μV/month.

Slew rate

The op-amp "compensation" capacitance (discussed further in Section 4.32) and small internal drive currents act together to limit the rate at which the output can change, even when a large input unbalance occurs. This limiting speed is usually specified as *slew rate* or slewing rate (SR). For the 411 it is 15V/μs; low-power op-amps typically have slew rates less than 1V/μs, while a high-speed op-amp might slew at 100V/μs, and the LH0063C "damn fast buffer" slews at 6000V/μs. The slew rate limits the amplitude of an undistorted sine-wave output swing above some critical frequency (the frequency at which the full supply swing requires the maximum slew rate of the op-amp, Fig. 4.29), thus explaining the "output voltage swing as a function of frequency" graph. A sine wave of frequency f hertz and amplitude A volts requires a minimum slew rate of $2\pi Af$ volts per second.

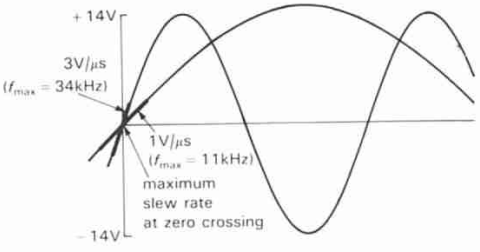


Figure 4.29. Slew-rate-induced distortion.

For externally compensated op-amps the slew rate depends on the compensation network used. In general, it will be lowest for "unity gain compensation," increasing to perhaps 30 times faster for ×100 gain compensation. This is discussed further in Section 4.32.

Temperature dependence

All these parameters have some temperature dependence. However, this usually doesn't make any difference, since small variations in gain, for example, are almost entirely compensated by feedback. Furthermore, the variations of these parameters with temperature are typically small compared with the variations from unit to unit.

The exceptions are input offset voltage and input offset current. This will matter, particularly if you've trimmed the offsets approximately to zero, and will appear as drifts in the output. When high precision is important, a low-drift "instrumentation" op-amp should be used, with external loads kept above 10k to minimize

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the horrendous effects on input-stage performance caused by temperature gradients. We will have much more to say about this subject in Chapter 7.

For completeness, we should mention here that op-amps are also limited in common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), input noise voltage and current (e_n, i_n), and output crossover distortion. These become significant limitations only in connection with precision circuits and low-noise amplifiers, and they will be treated in Chapter 7.

4.12 Effects of op-amp limitations on circuit behavior

Let's go back and look at the inverting amplifier with these limitations in mind. You will see how they affect performance, and you will learn how to design effectively in spite of them. With the understanding you will get from this example, you should be able to handle other op-amp circuits. Figure 4.30 shows the circuit again.

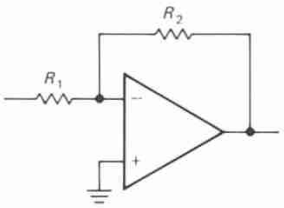


Figure 4.30

Open-loop gain

Because of finite open-loop gain, the voltage gain of the amplifier with feedback (closed-loop gain) will begin dropping at a frequency where the open-loop gain approaches R_2/R_1 (Fig. 4.31). For garden-variety op-amps like the 411, this means that you're dealing with a relatively low frequency amplifier; the open-loop gain is down to 100 at 50kHz, and f_T is 4MHz. Note that the closed-loop gain is always less than the open-loop gain; this means, for instance, that a $\times 100$ amplifier built with a 411 will show a noticeable falloff of gain for frequencies approaching 50kHz. Later in the chapter (Section 4.25), when we deal with transistor feedback circuits with finite open-loop gains, we will have a more accurate statement of this behavior.

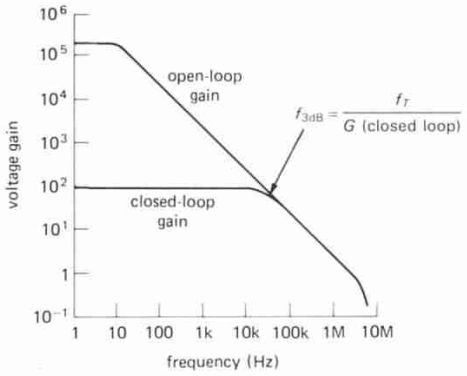


Figure 4.31. LF411 gain versus frequency ("Bode plot").

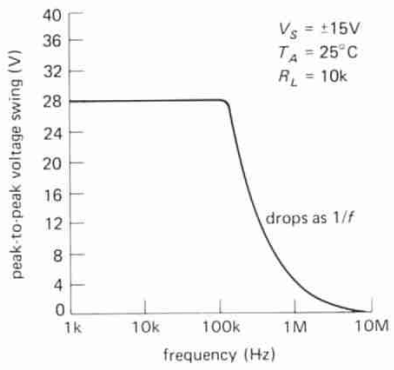


Figure 4.32. Output swing versus frequency (LF411).

Slew rate

Because of limited slew rate, the maximum undistorted sine-wave output swing drops above a certain frequency. Figure 4.32 shows the curve for a 411, with its 15V/μs

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slew rate. For slew rate S, the output amplitude is limited to $A(\text{pp}) \leq S/\pi f$ for a sine wave of frequency f, thus explaining the $1/f$ dropoff of the curve. The flat portion of the curve reflects the power-supply limits of output voltage swing.

As an aside, the slew-rate limitation of op-amps can be usefully exploited to filter sharp noise spikes from a desired signal, with a technique known as *nonlinear low-pass filtering*: By deliberately limiting the slew rate, the fast spikes can be dramatically reduced without any distortion of the underlying signal.

Output current

Because of limited output current capability, an op-amp's output swing is reduced for small load resistances. Figure 4.33 shows the graph for a 411. For precision applications it is a good idea to avoid large output currents in order to prevent on-chip thermal gradients produced by excessive power dissipation in the output stage.

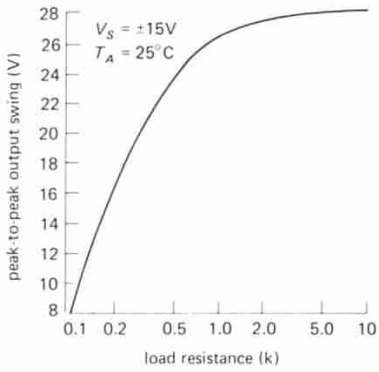


Figure 4.33. Output swing versus load (LF411).

Offset voltage

Because of input offset voltage, a zero input produces an output of $V_{\text{out}} = G_{dc}V_{os}$. For an inverting amplifier with voltage gain of 100 built with a 411, the output could be as large as ±0.2 volt when the input is grounded (V_{os} = 2mV max). Solutions: (a) If you don't need gain at dc, use a capacitor to drop the gain to unity at dc, as in Figure 4.7, as well as the RIAA amplifier circuit (Fig. 4.20). In this case you could do that by capacitively coupling the input signal. (b) Trim the voltage offset to zero using the manufacturer's recommended trimming network. (c) Use an op-amp with smaller V_{os}. (d) Trim the voltage offset to zero using an external trimming network as described in Section 7.06 (Fig. 7.5).

Input bias current

Even with a perfectly trimmed op-amp (i.e., $V_{os} = 0$), our inverting amplifier circuit will produce a non-zero output voltage when its input terminal is connected to ground. That is because the finite input bias current, I_B, produces a voltage drop across the resistors, which is then amplified by the circuit's voltage gain. In this circuit the inverting input sees a driving impedance of $R_1 \parallel R_2$, so the bias current produces a voltage $V_{\text{in}} = I_B(R_1 \parallel R_2)$, which is then amplified by the gain at dc, $-R_2/R_1$.

With FET-input op-amps the effect is usually negligible, but the substantial input current of bipolar op-amps can cause real problems. For example, consider an inverting amplifier with R_1 = 10k and R_2 = 1M; these are reasonable values for an inverting stage, where we might like to keep Z_{in} at least 10k. If we chose the low-noise bipolar LM833, the output (for grounded input) could be as large as 100×1000nA×9.9k, or 0.99 volt ($G_{dc}I_B R_{\text{unbalance}}$), which is unacceptable. By comparison, for our jellybean LF411 (JFET-input) op-amp the corresponding worst-case output (for grounded input) is 0.2mV; for most applications this is negligible, and in any case is dwarfed by the

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V_{os}-produced output error (200mV, worst-case untrimmed, for the LF411).

There are several solutions to the problem of bias-current errors. If you must use an op-amp with large bias current, it is a good idea to ensure that both inputs see the same dc driving resistance, as in Figure 4.34. In this case, 9.1k is chosen as the parallel resistance of 10k and 100k. In addition, it is best to keep the resistance of the feedback network small enough so that bias current doesn't produce large offsets; typical values for the resistance seen from the op-amp inputs are 1k to 100k or so. A third cure involves reducing the gain to unity at dc, as in the RIAA amplifier earlier.

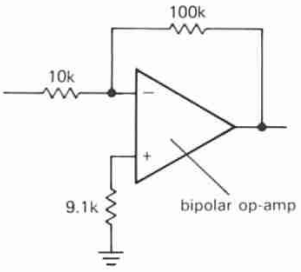


Figure 4.34. With bipolar op-amps, use a compensation resistor to reduce errors caused by input bias current.

In most cases, though, the simplest solution is to use op-amps with negligible input current. Op-amps with JFET or MOSFET input stages generally have input currents in the picoamp range (watch out for its rapid rise versus temperature, though, roughly doubling every 10°C), and many modern bipolar designs use superbeta transistors or bias-cancellation schemes to achieve bias currents nearly as low, *decreasing* slightly with temperature. With these op-amps, you can have the advantages of bipolar op-amps (precision, low noise) without the annoying problems caused by input current. For example, the precision low-noise bipolar OP-27 has I_B =10nA (typ), the inexpensive bipolar LM312 has I_B =1.5nA (typ), and its improved bipolar cousins (the LT1012 and LM11) have I_B = 30pA (typ). Among inexpensive FET op-amps, the JFET LF411 has I_B = 50pA (typ), and the MOSFET TLC270 series, priced under a dollar, have I_B = 1pA (typ).

Input offset current

As we just described, it is usually best to design circuits so that circuit impedances, combined with op-amp bias current, produce negligible errors. However, occasionally it may be necessary to use an op-amp with high bias current, or to deal with signals of extraordinarily high Thévenin impedances. In that case the best you can do is to balance the dc driving resistances seen by the op-amp at its input terminals. There will still be some error at the output ($G_{dc}I_{\text{offset}}R_{\text{source}}$), due to unavoidable asymmetry in the op-amp input currents. In general, I_{offset} is smaller than I_{bias} by a factor of 2 to 20 (with bipolar op-amps generally showing better matching than FET op-amps).

In the preceding paragraphs we have discussed the effects of op-amp limitations, taking the example of the simple inverting voltage amplifier circuit. Thus, for example, op-amp input current caused a *voltage* error at the output. In a different op-amp application you may get a different effect; for example, in an op-amp integrator circuit, finite input current produces an output *ramp* (rather than a constant) with zero applied input. As you become familiar with op-amp circuits you will be able to predict the effects of op-amp limitations in a given circuit and therefore choose which op-amp to use in a given application. In general, there is no "best" op-amp (even when price is no object): For example,

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TABLE 4.1. OPERATIONAL AMPLIFIERS

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Offset max (mV)	Drift typ (µV/°C)	Drift max (µV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
BIPOLAR, PRECISION																	
OP-07A	PM+	•	A	–	•	–	1	6	44	4	0.01	0.025	0.2	0.6	2	2	9.6
OP-07E	PM+	•	A	–	•	–	1	6	44	4	0.03	0.08	0.3	1.3	4	3.8	9.6
OP-21A	PM	•	A	A	•	–	1	5	36	0.3	0.04	0.1	0.5	1	100	4	21
OP-27E	PM+	•	A	A	•	–	1	8	44	5	0.01	0.025	0.2	0.6	40	35	3.0
OP-27G	PM+	•	A	A	•	–	1	8	44	6	0.03	0.1	0.4	1.8	80	75	3.2
OP-37E	PM+	•	A	–	•	–	5	8	44	5	0.01	0.025	0.2	0.6	40	35	3.0
OP-50E	PM	•	–	–	•	•	5	10	36	4	0.01	0.025	0.15	0.3	5	1	4.5
OP-77E	PM	•	A	A	•	–	1	6	44	2	0.01	0.025	0.1	0.3	2	1.5	9.6
OP-90E	PM	•	A	A	•	–	1	1.6	36	0.02	0.05	0.15	0.3	2	15	3	60
OP-97E	PM	•	–	–	•	–	1	4.5	40	0.6	0.01	0.025	0.2	0.6	0.1	0.1	14
MAX400M	MA	•	–	–	•	–	1	6	44	4	0.004	0.01	0.2	0.3	2	2	9.6
LM607A	NS	•	–	–	•	•	1	6	44	1.5	0.015	0.025	0.2	0.3	2	2	6.5
AD707C	AD	•	A	–	•	–	1	6	36	3	0.005	0.015	0.03	0.1	1	1	9.6
AD846B	AD	•	–	–	–	•	2	10	36	6.5	0.025	0.075	0.8	3.5	250	(k)	2
LT1001A	LT	•	A	–	•	–	1	6	44	3.3	0.01	0.025	0.2	0.6	4	4	9.6
LT1007A	LT	•	–	–	•	–	1	5	44	4	0.01	0.025	0.2	0.6	35	30	2.5
LT1012C	LT+	•	A	–	•	•	1	4	40	0.6	0.01	0.05	0.2	1.5	0.15	0.15	14
LT1028A	LT	•	–	–	•	•	1	8	44	9.5	0.01	0.04	0.2	0.8	90	50	0.9
LT1037A	LT	•	–	–	•	–	5	5	44	4.5	0.01	0.025	0.2	0.6	35	30	2.5
RC4077A	RA	•	–	–	•	–	1	6	44	1.7	0.004	0.01	0.1	0.3	2	1.5	9.6
HA5134A	HA	–	–	•	–	–	1	10	40	8	0.05	0.1	0.3	1.2	25	25	7
HA5135	HA	•	–	–	•	–	1	8	40	1.7	0.01	0.08	0.4	1.3	4	4	9
HA5147A	HA	•	–	–	•	–	10	8	44	4	0.01	0.025	0.2	0.6	40	35	3.0
BIPOLAR, LOW-BIAS (see also "bipolar, precision")																	
OP-08E	PM	•	–	–	–	•	U	10	40	0.5	0.07	0.15	0.5	2.5	2	0.2	20
LM10	NS+	•	–	–	•	–	1	1	45	0.4	0.3	2	2	-	20	0.7	47
LM11	NS+	•	–	–	•	•	1	5	40	0.6	0.1	0.3	1	3	50pA	10pA	150
OP-12E	PM+	•	–	–	–	–	1	10	40	0.5	0.07	0.15	0.5	2.5	2	0.2	20
LM308	NS+	•	A	–	–	•	U	10	36	0.8	2	7.5	6	30	7	1	35
LM312	NS+	•	–	–	•	•	1	10	40	0.8	2	7.5	6	30	7	1	35
LP324	NS	–	–	•	–	–	1	4	32	0.25	2	4	10	-	10	2	-
BIPOLAR, SINGLE-SUPPLY																	
324A	NS+	A	A	•	–	–	1	3	32	3	2	3	7	30	100	30	-
LP324	NS	–	–	•	–	–	1	4	32	0.25	2	4	10	-	10	2	-
LT1013C	LT	–	•	A	–	–	1	4	44	1	0.06	0.3	0.4	2.5	50	2	22
HA5141A	HA	•	A	A	–	–	1	2	40	0.07	0.5	2	3	-	75	10	20
BIPOLAR, SINGLE-SUPPLY PRECISION																	
LT1006A	LT	•	–	–	•	–	1	2.7	44	0.5	0.02	0.05	0.2	1.3	15	0.5	22
LT1013A	LT	–	•	A	–	–	1	4	44	1	0.04	0.15	0.4	2	35	1.3	22

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Type	Slew rate[e] typ (V/µs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	Swing to supplies?[g] In −	Swing to supplies?[g] Out +	Swing to supplies?[g] Out −	Comments
OP-07A	0.17	0.6	110	100	110	10	30[h]	−	−	−	−	
OP-07E	0.17	0.6	106	94	106	10	30[h]	−	−	−	−	
OP-21A	0.25	0.6	100	104	120	-	30	−	−	−	−	low power
OP-27E	2.8	8	114	100	120	20	0.5	−	−	−	−	low noise
OP-27G	2.8	8	100	94	117	20	0.5	−	−	−	−	cheap grade
OP-37E	17	63	114	100	120	20	0.5	−	−	−	−	low noise, decomp OP-27
OP-50E	3	25	126	126	140	70	10[h]	−	−	−	−	high current, low noise
OP-77E	0.3	0.6	120	110	134	12	30[h]	−	−	−	−	improved OP-07
OP-90E	0.01	0.02	100	104	117	6	36	−	•	−	•	micropower
OP-97E	0.2	0.9	114	114	110	10	0.5	−	−	−	−	low power OP-77
MAX400M	0.3	0.6	114	100	114	12	30	−	−	−	−	lowest non-chopper V_{os}
LM607A	0.7	1.8	124	100	134	10	0.5	−	−	−	−	
AD707C	0.3	0.9	130	120	138	12	44	−	−	−	−	improved OP-07; dual = 708
AD846B	450	310	110	110	-	50	18	−	−	−	−	current feedback; fast
LT1001A	0.25	0.8	114	110	113	30	30	−	−	−	−	
LT1007A	2.5	8	117	110	137	20	0.5	−	−	−	−	low noise, ~OP-27
LT1012C	0.2	0.8	110	110	106	12	1	−	−	−	−	improved 312; dual = 1024
LT1028A	15	75	114	117	137	20	1	−	−	−	−	ultra low noise
LT1037A	15	60	117	110	137	20	0.5	−	−	−	−	decomp 1007, ~OP-37
RC4077A	0.25	0.8	120	110	128	15	30	−	−	−	−	lowest non-chopper V_{os}
HA5134A	1	4	94	100	108	20	40	−	−	−	−	quad, low noise
HA5135	0.8	2.5	106	94	120	20	15[h]	−	−	−	−	
HA5147A	35	140	114	80	120	15	0.5	−	−	−	−	low noise, high speed, uncomp
OP-08E	0.12	0.8	104	104	98	5	0.5	−	−	−	−	precision 308
LM10	0.12	0.1	93	90	102	20	40	−	•	•	•	1V op-amp; precision; volt. ref.
LM11	0.3	0.5	110	100	100	2	0.5	−	−	−	−	precision; lowest bias bipolar
OP-12E	0.12	0.8	104	104	98	5	0.5	−	−	−	−	precision 312
LM308	0.15	0.3	80	80	88	5	0.5	−	−	−	−	original low-bias (superbeta)
LM312	0.15	0.3	80	96	88	5	0.5	−	−	−	−	compensated 308
LP324	0.05	0.1	80	90[t]	94	5	32	−	•	−	•	low power, single supply
324A	0.5	1	65	65	88	20	30	−	•	−	•	a classic; dual=358A
LP324	0.05	0.1	80	90[t]	94	5	32	−	•	−	•	low power, low bias
LT1013C	0.4	0.8	97	100	122	25	30	−	•	−	•	improved 358/324; quad = 1014
HA5141A	1.5	0.4	80	94	94	1	7	−	•	−	•	micropower
LT1006A	0.4	1	100	106	120	20	30	−	•	−	•	optional I_s = 90µA
LT1013A	0.4	0.8	100	103	124	25	30	−	•	−	•	improved 358/324; quad = 1014

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (μV/°C)	Voltage Drift max (μV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
BIPOLAR, HIGH-SPEED																	
OP-62E	PM	•	–	–	•	•	1	16	36	7	-	0.2	-	-	300	100	2.5
OP-63E	PM	•	–	–	•	•	1	16	36	7	-	0.75	-	-	300	100	7
OP-64E	PM	•	–	–	•	•	5	16	36	7	-	0.75	-	-	300	100	7
OP-65E	PM	•	–	–	•	–	1	9	14	25	-	2	-	-	3μA	1μA	-
CLC400	CL	•	–	–	•	–	1	-	7	15	2	5.5	20	40	25μA	(k)	12
AD509K	AD	•	–	–	•	•	3	10	40	6	4	8	-	40	200	25	19
SL541B	PL	•	–	–	•	–	10	-	24	21	-	5	15	-	25μA	10	-
VA705L	VT	•	A	A	•	–	1	8	12	10	1	2	20	-	900	25	-
VA706K	VT	•	A	A	•	–	1	8	12	10	4	10	20	-	1μA	120	-
VA707K	VT	•	A	A	•	–	12	8	12	10	3	6	20	-	1μA	120	-
LM837	NS	–	–	•	–	–	1	8	36	15	0.3	5	2	-	1μA	200	4.5
AD840K	AD	•	–	–	•	–	10	10	36	12	0.1	0.3	3	-	5μA	200	4
AD841K	AD	•	–	–	•	–	1	10	36	12	0.5	1	35	20	5μA	200	13
AD847J	AD	•	–	–	•	–	1	9	36	5.6	0.5	1	15	-	7μA	50[t]	15[t]
AD848J	AD	•	–	–	•	–	5	9	36	5.6	0.5	1	2	10	5μA	15[t]	4[t]
AD849J	AD	•	–	–	•	–	25	9	36	5.6	0.5	1	1	10	5μA	15[t]	4[t]
HA2539	HA	•	–	–	–	–	10	10	35	25	8	15	20	-	20μA	6μA	6
SL2541B	PL	•	–	–	•	–	1	14	30	25[t]	10	-	20	-	20μA	-	-
HA2541	HA	•	–	–	•	–	1	10	35	45	-	2	20	-	35μA	7μA	10
HA2542	HA	•	–	–	•	•	2	10	35	40	-	10	20	-	35μA	7μA	10
HA2544	HA	•	–	–	•	•	1	10	33	10	6	15	10	-	15μA	2μA	-
CA3450	RC	•	–	–	•	•	1	10	14	35	8	15	-	-	350	150	-
HA5101	HA	•	A	A	•	–	1	4	40	6	0.5	3	3	-	200	75	3.3
HA5111	HA	•	A	A	•	•	10	4	40	6	0.5	3	3	-	200	75	3.3
HA5147A	HA	•	–	–	•	–	10	8	44	4	0.01	0.025	0.2	0.6	40	35	3.0
HA5195	HA	•	–	–	–	–	5	20	35	25	3	6	20	-	15μA	4μA	6
LM6361	NS	•	–	–	•	–	1	5	36	6.5	5	20	10	-	5μA	2μA	15
LM6364	NS	•	–	–	•	–	5	5	36	6.5	2	9	6	-	5μA	2μA	8
LM6365	NS	•	–	–	•	–	25	5	36	6.8	1	6	3	-	5μA	2μA	5
BIPOLAR, OTHER																	
OP-20B	PM	•	A	A	•	–	1	4	36	0.08	0.06	0.25	0.75	1.5	25	1.5	58
LM833	NS	–	•	–	–	–	1	10	36	8	0.3	5	2	-	1μA	200	4.5
CA3193A	RC	•	–	–	•	–	1	7	36	3.5	0.14	0.2	1	3	20	5	24
XR4560	XR	–	•	–	–	–	1	8	36	2	0.5	6	-	-	500	200	8
HA5151	HA	•	A	A	–	–	1	2	40	0.25	2	3	3	-	150	30	15
NE5534	SN+	•	A	–	•	•	3	6	44	8	0.5	4	-	-	2μA	300	4
MC33078	MO	–	•	A	–	–	1	10	36	5	0.15	2	2	-	750	150	4.5
MC33171	MO	•	A	A	•	–	1	3	44	0.25	2	4.5	10	-	100	20	32
MC34071A	MO	•	A	A	•	–	1	3	44	2.5	0.5	1.5	10	-	500	50	32

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Type	Slew rate[e] typ (V/μs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
OP-62E	15	50	110	105	111	20	5	–	–	–	–	precision
OP-63E	50	50	110	105	100	20	5	–	–	–	–	
OP-64E	200	200	110	105	100	20	5	–	–	–	–	
OP-65E	200	150	85	90	100	50	5	–	–	–	–	
CLC400	700	280	40	40	-	50	-	–	–	–	–	transimpedance; decomp=401
AD509K	120	20	80	80	80	-	15	–	–	–	–	fast
SL541B	175	100	60	46	46	6.5	9	–	–	–	–	fast, video
VA705L	35	25	60	60	80	50	9	–	–	–	–	video, drives 50Ω; fast settle
VA706K	42	25	60	60	66	50	9	–	–	–	–	video, drives 50Ω; fast settle
VA707K	105	300	60	60	74	50	9	–	–	–	–	decomp, fast, 50Ω
LM837	10	25	80	120	90	40	30	–	–	–	–	low noise, low distortion
AD840K	400	400	100	94	104	50	6	–	–	–	–	decomp 841; 842 has G>2
AD841K	300	40	90	90	88	50	6	–	–	–	–	fast settle; decomp versions
AD847J	300	50	78	75	70	20	6	–	–	–	–	fast settle; decomp versions
AD848J	300	250	104[t]	104[t]	82	25	6	–	–	–	–	decomp 847
AD849J	300	725	110[t]	100[t]	90	25	6	–	–	–	–	uncomp 847
HA2539	600	600	60	85	80	10	6	–	–	–	–	low noise, sim to 2540
SL2541B	900	800	47	40[t]	45	10	10	–	–	–	–	has uncommitted unity gain buf
HA2541	280	40	70	60	80	10	6	–	–	–	–	fast settle, low distortion
HA2542	375	120	70	70	80	100	6	–	–	–	–	fast settle, decomp
HA2544	150	33	75	70	70	35	6	–	–	–	–	video
CA3450	420	190	50	60	96	75	5	–	–	–	–	video amp/line driver
HA5101	10	10	100[t]	80	136[t]	30	7	–	–	–	–	low noise
HA5111	50	100	100[t]	100[t]	136[t]	30	7	–	–	–	–	low noise, uncomp
HA5147A	35	140	114	80	120	15	0.7	–	–	–	–	low noise, precision, uncomp
HA5195	200	150	74	70	80	25	6	–	–	–	–	Elantec EL2195 = improved
LM6361	300	50	70	72	52	30	8	–	–	–	–	vertical PNP
LM6364	300	160	102[t]	70	66[t]	30	8	–	–	–	–	vertical PNP
LM6365	300	725	80	104[t]	75	30	8	–	–	–	–	vertical PNP
OP-20B	0.05	0.1	96	100	114	0.5	30	–	•	–	–	accurate low power
LM833	7	15	80	80	90	10	30	–	–	–	–	low noise, low distortion
CA3193A	0.25	1.2	110	100	110	7	5	–	–	–	–	
XR4560	4	10	70	76	86	100	30	–	–	–	–	intended for audio
HA5151	4.5	1.3	80	80	94	3	7	–	–	–	•	low power
NE5534	6	10	70	80	88	20	0.5	–	–	–	–	low noise, intended for audio
MC33078	7	16	80	80	90	20	36	–	–	–	–	low noise, low distortion
MC33171	2.1	1.8	80	80	94	4	44	–	•	–	–	
MC34071A	10	4.5	80	80	94	25	44	–	•	–	–	drives 0.01μF

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1 2 4	Trim Ext comp[c] Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (μV/°C)	Voltage Drift max (μV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
BIPOLAR, OBSOLESCENT													
OP-01E	PM	• – –	• – 1	10	44	3	1	2	3	10	50	5	-
OP-02E	PM	• A –	• – 1	10	44	2	0.3	0.5	2	8	30	2	21
OP-05E	PM+	• A –	• – 1	6	44	4	0.2	0.5	0.7	2	4	3.8	9.6
OP-11E	PM	– – •	– – 1	10	44	6	0.3	0.5	2	10	300	20	12
307	NS+	• – –	– – 1	10	44	2.5	2	7.5	6	30	250	50	16
LM318	NS+	• – –	• • 1	10	40	10	4	10	-	-	500	200	14
349	NS	– – •	– – 5	10	36	4.5	1	6	-	-	200	50	60
AD517L	AD	• – –	• – 1	10	36	3	-	0.025	-	0.5	1	0.25	20
AD518J	AD	• – –	• • 1	10	40	10	4	10	10	-	500	200	-
NE530	SN	• A –	• – 1	10	36	3	2	5	6	-	150	40	30
NE531	SN	• – –	• • U	12	44	10	2	6	-	-	2μA	200	-
NE538	SN	• A –	• – 5	10	36	2.8	2	5	6	-	150	40	18
μA725	FA+	• – –	• • U	6	44	3	0.5	1	2	5	100	20	-
μA739	FA	– • –	– • U	8	36	14	1	6	-	-	2μA	10μA	-
741C	FA+	• A A	• – 1	10	36	2.8	2	6	-	-	500	200	-
748C	FA+	• – –	• • U	10	36	3.3	2	6	-	-	500	200	-
μA749	FA	– • –	– • U	8	36	10	1	3	3	-	750	400	-
1435	TP	• – –	• • 10	24	32	30	2	5	5	25	20μA	-	-
1456	MO	• – –	• – 1	10	36	3	5	10	-	-	30	10	45
HA2505	HA	• – –	• • 1	20	40	6	4	8	20	-	250	50	-
HA2515	HA	• – –	• • 1	20	40	6	5	10	30	-	250	50	-
HA2525	HA	• – –	• • 3	20	40	6	5	10	30	-	250	50	-
HA2605	HA	• – –	• • 1	10	45	4	3	5	10	-	25	25	-
HA2625	HA	• – –	• • 5	10	45	4	3	5	10	-	25	25	-
CA3100	RC	• – –	• • 10	13	36	11	1	5	-	-	2μA	400	-
4558	RA+	– • –	– – 1	8	36	5.6	2	6	-	-	500	200	43
NE5535	SN	A • –	• – 1	10	36	2.8	2	5	6	-	150	40	17
5539	SI+	• – –	– • 7	6	24	15	2.5	5	5	10	20μA	-	4
JFET, PRECISION													
OP-41E	PM	• – –	• – 1	10	36	1	0.2	0.25	2.5	5	0.005	0.001	32
OP-43E	PM	• – –	• – 1	10	36	1	0.2	0.25	2.5	5	0.005	0.001	32
OPA101B	BB	• – –	• – 1	10	40	8	0.05	0.25	3	5	0.01	4pA	8
OPA111B	BB	• A –	• – 1	10	36	3.5	0.05	0.25	0.5	1	1pA	0.7pA	7
AD547L	AD	• A –	• – 1	5	36	1.5	-	0.25	-	1	0.025	2pA[t]	30
AD548C	AD	• A –	• – 1	9	36	0.2	0.1	0.25	-	2	0.01	0.005	30
OPA627B	BB	• – –	• – 1	9	36	8	0.04	0.1	0.5	0.8	0.02	0.02	5.2
AD711C	AD	• A A	• – 1	9	36	2.8	0.1	0.25	2	3	0.025	0.01	18
AD845K	AD	• – –	• – 1	9.5	36	12	0.1	0.25	1.5	5	1	0.1	25
LT1055A	LT	• – –	• – 1	10	40	4	0.05	0.15	1.2	4	0.05	0.01	14
HA5170	HA	• – –	• – 1	9	44	2.5	0.1	0.3	2	5	0.1	0.06	10

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Type	Slew rate[e] typ (V/µs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
OP-01E	18	2.5	80	80	94	6	30					fast, precision
OP-02E	0.5	1.3	90	90	100	6	30					precision, low current
OP-05E	0.17	0.6	110	94	106	10	30[h]					
OP-11E	1	2	110	90	100	6	30					precision quad
307	0.5	1	70	70	84	10	30	•				a classic; uncomp=301
LM318	70	15	70	65	86	10	0.5					was popular
349	2	4	70	77	88	15	36					decomp 348 (quad 741)
AD517L	0.1	0.25	110	96	120	10	30					
AD518J	70	12	70	65	88	15	-					
NE530	35	3	70	76	94	10	30	•				fast; dual=5530
NE531	35	1	70	76	86	-	15	•				
NE538	60	5	70	76	94	10	30	•				fast; dual=5538
µA725	0.005	0.08	110	100	108	15	5					original precision op-amp
µA739	1	6	70	85[t]	76	1.5	5			•		low noise, intended for audio
741C	0.5	1.2	70	76	86	20	30					old classic; dual=1458, quad=348
748C	0.5	1.2	70	76	94	15	30					uncomp 741
µA749	2	6	70	74	86	1.5	5			•		sim to 739
1435	300	1GHz	80	75[t]	80	10	2					fast settle
1456	2.5	1	70	74	97	5	40					
HA2505	30	12	74	74	84	10	15	•				
HA2515	60	12	74	74	78	10	15	•				
HA2525	120	20	74	74	78	10	15	•				
HA2605	7	12	74	74	98	10	12					
HA2625	35	100	74	74	98	10	12					
CA3100	25	30	76	60	58	15	12					
4558	1	2.5	70	74	86	15	30					fast 1458
NE5535	15	1	70	76	94	10	30	•				fast
5539	600	1200	70	66	46	40	10			•		small output swing
OP-41E	1.3	0.5	100	92	120	15	20	•				low bias, low dist; OP-43 faster
OP-43E	6	2.4	100	92	120	15	20	•				low bias, low dist; OP-41 stabler
OPA101B	7	20	80	86	96	45	20					low noise; decomp = OPA102
OPA111B	2	2	100	100	120	10	36					low noise, low bias
AD547L	3	1	80	80	108	20	20					dual = AD642, 647
AD548C	1.8	1	86	86	110	20	20					improved LF441; dual = AD648
OPA627B	55	16	106	106	110	30	-					fast
AD711C	20	4	86	86	106	20	20					improved LF411/2
AD845K	100	16	94	95	108	30	36					fast
LT1055A	13	5	86	90	104	30	40					LT1056 is 20% faster
HA5170	8	8	90	74	110	10	30	•				low noise

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (μV/°C)	Voltage Drift max (μV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
JFET, HIGH-SPEED																	
OP-42E	PM	•	–	–	•	–	1	15	40	6.5	0.3	0.75	4	10	0.2	0.04	13
OP-44E	PM	•	–	–	•	–	3	16	40	6	0.03	0.75	4	10	0.2	40pA	13
357B	NS+	•	–	–	•	–	5	10	36	7	3	5	5	-	100pA	0.02	12
AD380K	AD	•	–	–	•	•	U	12	40	15	-	1	-	10	0.1	5pA[t]	15
LF401A	NS	•	–	–	•	•	1	15	36	12	-	0.2	-	-	0.2	0.1	23
OPA404B	BB	–	–	•	–	–	1	10	36	10	0.26	0.75	3	-	0.004	4pA	15
LF457B	NS	•	–	–	•	–	5	10	36	10	0.18	0.4	3	4	50pA	20pA	10
OPA602C	BB	•	–	–	•	–	1	10	36	4	0.1	0.25	1	2	1pA	1pA	13
OPA605K	BB	•	–	–	•	•	50	10	40	9	0.25	0.5	-	5	0.035	2pA[t]	20
OPA606L	BB	•	–	–	•	–	1	10	36	9.5	0.1	0.5	3	5	0.01	5pA	13
AD744C	AD	•	A	–	•	•	2	9	36	4	0.1	0.25	2	3	0.05	0.02	18
AD843B	AD	•	–	–	•	–	1	9	36	12	0.5	1	15	-	1	0.1	13
AD845K	AD	•	–	–	•	–	1	9.5	36	10.2	0.1	0.25	1.5	3	0.4	0.05	25
LT1022A	LT	•	–	–	•	–	1	20	40	7	0.08	0.25	1.3	5	0.05	0.01	14
HA5160	HA	•	–	–	–	•	U	14	40	10	1	3	20	-	0.05	0.01	35
MC34080A	MO	•	A	A	•	–	2	6	44	3.4	0.3	0.5	10	-	0.2	0.1	30
MC34081A	MO	•	A	A	•	–	1	6	44	3.4	0.3	0.5	10	-	0.2	0.1	30
JFET, OTHER																	
TL031C	TI	•	A	A	•	–	1	10	36	0.28	0.5	1.5	6	-	0.2	0.1	41
TL051C	TI	•	A	A	•	–	1	10	36	3.2	0.6	1.5	8	-	0.2	0.1	18
TL061C	TI+	•	A	A	•	–	1	4	36	0.25	3	15	10	-	0.4	0.2	42
TL071C	TI+	•	A	A	•	–	1	7	36	2.5	3	10	10	-	0.2	0.05	18
TL081B	TI+	•	A	A	•	–	1	7	36	2.8	2	3	10	-	0.2	0.01	18
OPA121	BB	•	–	–	•	–	1	10	36	4	0.5	2	3	10	0.005	4pA	8
OPA128L	BB	•	–	–	•	–	1	10	36	1.5	0.14	0.5	-	5	75fA	30fA[t]	27
LF351	NS+	•	A	A	•	–	1	10	36	3.4	5	10	10	-	0.2	0.1	25
355B	NS+	•	–	–	•	–	1	10	36	4	3	5	5	-	100pA	0.02	20
356B	NS+	•	–	–	•	–	1	10	36	7	3	5	5	-	100pA	0.02	12
LF411	NS+	•	A	–	•	–	1	10	36	3.4	0.8	2	7	20	0.2	0.1	25
LF*nnn*	NS	–	•	–	–	–	1	6	36	25	1	-	-	-	100pA	50pA	3.5
LF441	NS	•	A	A	•	–	1	10	36	0.25	1	5	10	20	0.1	0.05	35
LF455B	NS	•	–	–	•	–	1	10	36	4	0.18	0.4	3	4	50pA	20pA	12
LF456B	NS	•	–	–	•	–	1	10	36	8	0.18	0.4	3	4	50pA	20pA	10
AD549L	AD	•	–	–	•	–	1	10	36	0.7	0.3	0.5	5	10	60fA	20fA[t]	35
AD611K	AD	•	–	–	•	–	1	10	36	2.5	0.25	0.5	5	10	0.05	0.025	18
LT1057A	LT	–	•	A	–	–	1	20	40	3.8	0.15	0.45	1.8	7	0.05	0.04	13
HA5180	HA	•	–	–	•	–	1	10	40	1	0.1	0.5	5	-	0.001	200fA	70
MC34001A	MO	•	A	A	•	–	1	8	36	2.5	1	2	10	-	0.1	0.05	25
MC34181	MO	•	A	A	•	–	1	3	36	0.2	0.5	2	10	-	0.1	0.05	38

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Type	Slew rate[e] typ (V/µs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
OP-42E	58	10	88	86	114	25	40	−	−	−	−	low Z_{out}
OP-44E	120	16	88	90	114	15	40	−	−	−	−	
357B	50	20	85	85	94	20	30	•	−	−	−	decomp 356
AD380K	330	300	60	60	92	60	20	−	−	−	−	hybrid, fast, 50Ω
LF401A	30	16	90	80	100	50	32	−	−	−	−	accurate
OPA404B	35	6.4	92	86	92	10	36	−	−	−	−	accurate quad
LF457B	50	20	86	86	106	100[l]	40	•	−	−	−	low noise; drives 0.01µF
OPA602C	35	6.5	92	86	92	20	36	−	−	−	−	low bias, fast settle
OPA605K	94	20	80	74	104[t]	30	20	−	−	−	−	uncomp
OPA606L	35	13	85	90	100	10	36	−	−	−	−	improved LF356
AD744C	75	13	86	92	108	20	36	−	−	−	−	very low dist (3ppm); fast settle
AD843B	250	35	100	95	88	50	-	−	−	−	−	fast settle
AD845K	100	16	94	98	106	25	20	−	−	−	−	fast settle
LT1022A	26	8.5	86	88	104	10	40	−	−	−	−	
HA5160	120	100	74	108	98	22	40	−	−	−	−	low bias
MC34080A	50	16	75	75	94	20	44	−	−	−	−	V_{in} > V-+4V; decomp 34081
MC34081A	25	8	75	75	94	20	44	−	−	−	−	V_{in} > V-+4V
TL031C	3	1	75	75	74	8	30	•	−	−	−	low power; improved TL061
TL051C	24	3	75	75	94	30	30	•	−	−	−	low dist; improved TL071/081
TL061C	3.5	1	70	70	70	5	30	−	−	−	−	low power
TL071C	13	3	70	70	88	10	30	−	−	−	−	lower noise
TL081B	13	3	80	80	94	10	30	−	−	−	−	
OPA121	2	2	86	86	110	10	36	−	−	−	−	low noise
OPA128L	3	1	90	90	110	10	36	−	−	−	−	very low bias
LF351	13	4	70	70	88	10	30	•	−	−	−	353=dual, 347=quad
355B	5	2.5	85	85	94	20	30	•	−	−	−	popular
356B	12	5	85	85	94	20	30	•	−	−	−	faster 355
LF411	15	4	70	70	88	20	30	•	−	−	−	jellybean
LF*nnn*	20	10	80	80	100	15	2	•	−	−	−	lowest noise JFET
LF441	1	1	70	70	88	4	30	•	−	−	−	low current jellybean
LF455B	5	3	86	86	106	100[l]	40	•	−	−	−	low noise; drives 0.01µF
LF456B	12.5	5	86	86	106	100[l]	40	•	−	−	−	low noise; drives 0.01µF
AD549L	3	1	90	90	110	10	36	−	−	−	−	electrometer; guard pin
AD611K	13	2	80	80	94	20	20	−	−	−	−	low dist, gen purp JFET
LT1057A	13	5	86	88	104	10	40	−	−	−	−	accurate dual/quad JFET
HA5180	7	2	90	90	106	15	40	−	−	−	−	very low bias over temp; noisy
MC34001A	13	4	80	80	94	20	30	•	−	−	−	
MC34181	10	4	70	70	88	8	36	−	−	−	−	low power, fast, low dist.

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (µV/°C)	Voltage Drift max (µV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
JFET, OBSOLESCENT																	
OP-15E	PM+	•	A	–	•	–	1	10	44	4	0.2	0.5	2	5	0.05	0.01	15
OP-16E	PM+	•	–	–	•	–	1	10	44	7	0.2	0.5	2	5	0.05	0.01	15
AD515L	AD	•	–	–	•	–	1	10	36	1.5	0.4	1	-	25	80fA	80fA	50
AD542L	AD	•	–	–	•	–	1	10	36	1.5	-	0.5	-	5	0.025	2pA[t]	30
AD544L	AD	•	–	–	•	–	1	10	36	2.5	-	0.5	-	5	0.05	0.5pA[t]	18
AD545L	AD	•	–	–	•	–	1	10	36	1.5	-	0.5	-	5	0.001	-	35
ICH8500A	IL	•	–	–	•	–	1	16	36	2.5	-	50	-	-	10fA	10fA	40
MOSFET																	
OP-80E	PM	•	–	–	•	–	1	4.5	16	0.2	0.4	1	-	-	60fA	10fA[t]	70
TLC27L2A	TI	A	•	A	–	–	1	3	18	0.04	-	5	0.7	-	1pA[t]	1pA[t]	70
TLC27M2A	TI	A	•	A	–	–	1	3	18	0.6	-	5	2	-	1pA[t]	1pA[t]	38
TLC272A	TI	A	•	A	–	–	1	3	18	4	-	5	5	-	1pA[t]	1pA[t]	25
TLC279C	TI	–	–	•	–	–	1	3	18	8	0.4	1.2	2	-	0.7pA[t]	0.1pA[t]	25
LMC660A	NS	–	–	•	–	–	1	5	16	2.2	1	2	1.3	5	20pA	20pA	22
TLC1078C	TI	–	•	A	–	–	1	1.4	16	0.05	0.18	0.6	1	-	0.7pA[t]	0.1pA[t]	68
ALD1701	AL	•	–	–	–	–	1	2	12	0.25	-	4.5	7	-	0.03	0.025	-
ALD1702	AL	•	–	–	–	–	1	2	12	2	-	4.5	7	-	0.03	0.025	100
CA3140A	RC	•	A	–	•	–	1	4	44	6	2	5	6	-	0.04	0.02	40
CA3160A	RC	•	A	–	•	•	1	5	16	15	2	5	10	-	0.03	0.02	72
CA3410A	RC	–	–	•	–	–	1	4	36	10	3	8	10	-	0.03	0.01	40
CA3420A	RC	•	–	–	•	•	1	2	22	1	2	5	4	-	0.005	0.004	62
CA5160A	RC	•	A	–	•	•	1	5	15	0.4	1.5	4	-	-	0.01	0.005	-
CA5420A	RC	•	–	–	•	•	1	2	20	0.5	1	5	-	-	0.001	0.5pA	-
CA5422	RC	•	–	–	•	–	1	2	20	0.7	1.8	10	20	-	0.005	0.004	-
ICL7612B	IL+	•	–	–	–	–	1	3	18	2.5	-	5	5	-	0.05	0.03	100
ICL7641B	IL+	A	A	•	–	–	1	1	18	2.5	-	5	5	-	0.05	0.03	100
CHOPPER STABILIZED																	
MAX420E	MA	•	–	–	–	–	1	6	33	2	0.001	0.005	0.02	0.05	0.03	0.06	1.1[j]
MAX422E	MA	•	–	–	–	–	1	6	33	0.5	0.001	0.005	0.02	0.05	0.03	0.06	1.1[j]
LMC668A	NS	•	–	–	–	–	1	5	16	3.5	0.001	0.005	0.05	-	0.06	-	2[j]
TSC900A	TS	•	–	–	–	–	1	4.5	16	0.2	-	0.005	0.02	0.05	0.05	0.5pA[t]	4[j]
TSC901	TS	•	A	A	–	–	1	5	32	0.6	0.007	0.015	0.05	0.15	0.05	0.1	5[j]
TSC911A	TS	•	A	A	–	–	1	4	16	0.6	0.005	0.015	0.05	0.15	0.07	0.02	11[j]
TSC915	TS	•	–	–	–	–	1	7	32	1.5		0.01	0.01	0.1	0.1	0.1	0.8[j]
TSC918	TS	•	–	–	–	–	1	4.5	16	0.8	-	0.05	0.4	0.8	0.1	0.5pA[t]	4[j]
LTC1050	LT	•	–	–	–	–	1	4.8	16	1.5	0.5µV	0.005	0.01	0.05	0.03	0.06	1.6[j]
LTC1052	LT	•	–	–	–	–	1	4.8	16	2	0.5µV	0.005	0.01	0.05	0.03	0.03	1.5[j]
ICL7650	IL+	•	–	–	–	–	1	4.5	16	3.5	0.002	0.005	0.1	-	0.01	5pA[t]	2[j]
ICL7650S	IL	•	–	–	–	–	1	4.5	16	3	0.7µV	0.005	0.02	0.1	0.01	0.02	2[j]
ICL7652	IL+	•	–	–	–	–	1	5	16	3.5	0.002	0.005	0.1	-	0.03	25pA[t]	0.7[j]
ICL7652S	IL	•	–	–	–	–	1	5	16	2.5	0.7µV	0.005	0.01	0.06	0.03	0.04	0.7[j]
TSC76HV52	TS	•	–	–	–	–	1	7	32	1.5	-	0.01	-	0.3	0.1	0.1	0.8[j]

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Type	Slew rate[e] typ (V/µs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
OP-15E	17	6	86	86	100	15	40	−	−	−	−	precision fast 355
OP-16E	25	8	86	86	100	20	40	−	−	−	−	precision fast 356 (OP-17=decomp)
AD515L	1	0.4	70	74	94	10	20	−	−	−	−	very low bias, precision
AD542L	3	1	80	80	110	10	20	−	−	−	−	precision
AD544L	13	2	80	80	94	15	20	−	−	−	−	precision, low noise
AD545L	1	0.7	76	74[t]	92	10	20	−	−	−	−	precision
ICH8500A	0.5	0.5	60	80[t]	100[t]	10	0.5	−	−	−	−	ultra low bias
OP-80E	0.4	0.3	60	60	100	10	16	−	•	−	•	electrometer; I_b<20pA @ 125°C
TLC27L2A	0.04	0.1	70	70	90	10	18	−	•	−	•	CMOS jellybeans
TLC27M2A	0.6	0.7	70	70	86	10	18	−	•	−	•	CMOS jellybeans
TLC272A	4.5	2.3	70	65	80	10	18	−	•	−	•	CMOS jellybeans
TLC279C	4.5	2.3	65	65	80	10	18	−	•	−	•	best V_{os} of 272-series
LMC660A	1.7	1.5	72	80	112	15	16	−	•	•	•	quad CMOS jellybean
TLC1078C	0.05	0.11	75	75	114	15	16	−	•	−	•	low offset
ALD1701	0.7	0.7	65	65	90	0.5	12	•	•	•	•	rail-to-rail; specs @ +5V supply
ALD1702	2.1	1.5	65	65	94	2	12	•	•	•	•	rail-to-rail; specs @ +5V supply
CA3140A	7	3.7	70	76	86	+10,-1	8	−	•	−	•	
CA3160A	10	4	80	76	94	12	8	−	•	•	•	MOS in/out (3130=uncomp)
CA3410A	10	5.4	80	80	86	6	16	−	•	−	−	high speed 324-type replacement
CA3420A	0.5	0.5	60	70	86	2	15	−	•	•	•	low I_b, good input protec.
CA5160A	10	4	-	-	90	1	?	−	•	•	•	CMOS output
CA5420A	0.5	0.5	-	-	85	0.5	15	−	•	•	•	similar to 3420
CA5422	1	1	60	60	80	2	15	−	•	•	•	unusual 2-section design
ICL7612B	1.6	1.4	60	70	80	5[m]	18	•	•	•	•	programmable; in/out to both rails
ICL7641B	1.6	1.4	60	70	80	5[m]	18	•	−	•	•	gen purp, low voltage
MAX420E	0.5	0.5	120	120	120	+2,-15	33	−	•	•	•	±15V V_s; 0.1µV/mo; 430 has C_{int}
MAX422E	0.13	0.13	120	120	120	+0.2,-8	33	−	•	•	•	±15V V_s; 0.1µV/mo; 432 has C_{int}
LMC668A	2.5	1	120	120	120	+5,-15	16	−	•	•	•	
TSC900A	0.2	0.7	110	120	120	2.5	16	−	•	−	•	low power
TSC901	2	0.8	120	120	120	-	36	−	•	−	•	±15V supply; int caps
TSC911A	2.5	1.5	110	112	116	3.5	16	−	•	−	•	int caps, noisy
TSC915	0.5	0.5	120	120	120	10	36	−	•	−	•	±15V supply
TSC918	0.2	0.7	98	105	100	-	16	−	•	−	•	inexpensive
LTC1050	4	2.5	120	125	130	+3,-20	16	−	•	•	•	int caps; 50nV/√month
LTC1052	4	1.2	120	120	120	+5,-15	16	−	•	•	•	improved 7652; 0.1µV/month
ICL7650	2.5	2	110	120	120	+5,-20	16	−	•	•	•	0.1µV/month
ICL7650S	2.5	2	120	120	136	+4,-20	16	−	•	•	•	improved 7650; 0.1µV/month
ICL7652	0.5	0.4	110	110	120	+5,-20	16	−	−	•	•	0.15µV/month
ICL7652S	1	0.5	120	120	136	+4,-20	16	−	−	•	•	improved 7652; 0.15µV/month
TSC76HV52	0.5	0.5	120	120	120	10	32	−	−	•	•	±15V supply

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TABLE 4.1 (*cont'd*)

Type	Mfg[a]	# per pkg[b] 1	2	4	Trim	Ext comp[c]	Min gain[d]	Total supply voltage min (V)	Total supply voltage max (V)	Supp curr max (mA)	Voltage Offset typ (mV)	Voltage Offset max (mV)	Voltage Drift typ (μV/°C)	Voltage Drift max (μV/°C)	Current Bias max (nA)	Current Offset max (nA)	e_n @1kHz typ nV/√Hz
HIGH VOLTAGE																	
LM343	NS	•	–	–	•	–	1	10	68	5	2	8	-	-	40	10	35
LM344	NS	•	–	–	•	•	U	10	68	5	2	8	-	-	40	10	35
OPA445B	BB	•	–	–	•	–	1	20	100	4.5	1	3	10	-	0.05	0.01	16
1436	MO+	•	–	–	•	–	1	10	80	5	5	10	-	-	40	10	50
HA2645	HA	•	–	–	•	•	1	20	80	4.5	2	6	15	-	30	30	30
3580	BB	•	–	–	•	–	1	30	70	10	-	10	-	30	0.05	-	15
3581	BB	•	–	–	•	–	1	64	150	8	-	3	-	25	0.02	0.02	25
3582	BB	•	–	–	•	–	1	140	300	6.5	-	3	-	25	0.02	-	25
3583	BB	•	–	–	•	–	1	100	300	8.5	-	3	-	25	0.1	0.1	50
3584	BB	•	–	–	•	•	U	140	300	6.5	-	3	-	25	0.1	0.1	50
MONOLITHIC POWER																	
LM12	NS	•	–	–	–	–	1	20	80	80	2	7	-	50	300	100	90
OPA541B	BB	•	–	–	–	–	1	20	80	25	0.1	1	15	30	0.05	0.03	50
LM675	NS	•	–	–	–	–	10	16	60	50	1	10	25	-	2μA	500	-
SG1173	SG	•	–	–	–	–	1	10	50	20	2	4	-	30	500	150	-

[a] manufacturers are as follows (a "+" suffix designates multiple sources):

AD - Analog Devices
AL - Advanced Linear Devices
AM - Advanced Micro Devices
AN - Analogic
AP - Apex
BB - Burr-Brown
BT - Brooktree
CL - Comlinear
CR - Crystal Semiconductor
CY - Cypress
DA - Datel
EL - Elantec
FA - Fairchild (National)
FE - Ferranti
GE - General Electric
GI - General Instrument
HA - Harris
HI - Hitachi
HO - Honeywell
HS - Hybrid Systems
ID - Integrated Device Technology
IL - GE/Intersil
IN - Intel
IR - International Rectifier
KE - M.S.Kennedy Corp
LT - Linear Technology Corp
MA - Maxim
MN - Micro Networks
MO - Motorola
MP - Micro Power Systems
NE - NEC
NS - National Semiconductor
OE - Optical Electronics Inc
PL - Plessey
PM - Precision Monolithics
RA - Raytheon
RC - GE/RCA
RO - Rockwell
SG - Silicon General
SI - Siliconix
SN - Signetics
SO - Sony
ST - Supertex
TI - Texas Instruments
TM - Telmos
TO - Toshiba
TP - Teledyne Philbrick
TQ - TriQuint
TR - TRW
TS - Teledyne Semiconductor
VT - VTC
XI - Xicor
XR - Exar
ZI - Zilog

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Type	Slew rate[e] typ (V/µs)	f_T typ (MHz)	CMRR min (dB)	PSRR min (dB)	Gain min (dB)	Max output curr (mA)	Max diff'l input[f] (V)	Swing to supplies?[g] In +	In −	Out +	Out −	Comments
LM343	2.5	1	70	74	97	10	68	–	–	–	–	monolithic
LM344	30	10	70	74	97	10	68	–	–	–	–	uncomp 343
OPA445B	10	2	80	80	100	15	80	–	–	–	–	low-bias, monolithic
1436	2	1	70	80	97	10	80	–	–	–	–	monolithic
HA2645	5	4	74	74	100	10	37	–	–	–	–	monolithic
3580	15	5	86[t]	87[t]	106[t]	60	70	–	–	–	–	hybrid
3581	20	5	110[t]	105[t]	112[t]	30	150	–	–	–	–	hybrid
3582	20	5	110[t]	105[t]	118[t]	15	300	–	–	–	–	hybrid
3583	30	5	110[t]	84[t]	94	75	300	–	–	–	–	fast JFET, hybrid
3584	150	20	110[t]	84[t]	100	15	300	–	–	–	–	uncomp JFET, hybrid
LM12	9	0.7	75	80	94	10A	80	–	–	–	–	full output protection
OPA541B	10	1.6	95	100	90	10A	80	–	–	–	–	isolated case; no int. protec.
LM675	8	5.5	70	70	70	3000	60	–	–	–	–	full output protection
SG1173	0.8	1	76	80	92	3500	50	–	–	–	–	thermal shutdown

(b) the symbol • indicates the number of op-amps per package for the part number shown; an "A" indicates the availability of other quantities of op-amps per package from the same manufacturer; some electrical characteristics (particularly offset voltage) may be degraded somewhat in multiple packages.
(c) pins are provided for external compensation.
(d) a number gives the minimum closed-loop gain without instability. Op-amps with pins for external compensation can generally be operated at lower gain, if an appropriate ext comp network is used. The letter U means that the op-amp is uncompensated – external capacitance is necessary for any small value of closed-loop gain.
(e) at minimum stable closed-loop gain (usually unity gain), unless otherwise noted.
(f) the maximum value without damage to the chip; not to exceed the total supply voltage used, if that is less.
(g) a dot in an IN column means that the input operating common-mode range includes that supply rail; a dot in an OUT column means that the op-amp can swing its output all the way to the corresponding supply rail.
(h) resistor-diode network draws input current for input differential greater than ±1V.
(j) µV pp, 0.1-10Hz.
(k) current-sensing inverting input ("current feedback" configuration); the bias currents at the two inputs may differ widely. The listed bias current is for the non-inverting input.
(l) "raw" output (no current limit) available at pin 8, in addition to the conventional (protected) output at pin 6; the latter is limited to ±15mA.
(m) min/max (worst case).
(t) typical.

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TABLE 4.2. RECOMMENDED OP-AMPS

Type	Mfg[a]	Amps per package[b] 1	2	4	Offset voltage max (mV)	Offset drift max (μV/°C)	Input curr max (nA)	Total supply voltage min (V)	Total supply voltage max (V)	Supply curr max (mA)	e_n, typ 10Hz (nV/√Hz)	e_n, typ 1kHz (nV/√Hz)	Slew rate typ (V/μs)	f_T typ (MHz)	Comments
LF411	NS	•	A	–	2	20	0.2	10	36	3.4	50	25	15	4	general purpose jellybean
AD711K	AD	•	A	–	0.5	10	0.05	9	36	3	45	18	20	4	improved LF411
LM358A	NS+	–	•	A	3	20	100	3	32	1.2	–	–	0.5	1	single supply jellybean
TLC27M2A	TI	A	•	A	5	2[t]	0.001[t]	3	18	0.6	–	–	0.6	0.7	CMOS jellybean
OP-27E	PM+	•	A	A	0.025	0.6	40	8	44	5	3.5	3.0	2.8	8	precision, low-noise
OP-37E	PM+	•	A	–	0.025	0.6	40	8	44	5	3.5	3.0	17[h]	63[h]	ditto, faster (decomp, min. gain = 5)
HA5147A	HA	•	–	–	0.025	0.6	40	8	44	4	3.5	3.0	35[c]	140[c]	ditto, still faster (min. gain = 10)
OP-77E	PM	•	A	A	0.025	0.3	2	6	44	2	10.3	9.6	0.3	0.6	precision
LT1028A	LT	•	–	–	0.04	0.8	90	8	44	9.5	1.0	0.85	15	75	precision ultra-low-noise
LT1013A	LT	–	•	A	0.15	2	35	4	44	1	24	22	0.4	0.8	precision single-supply
LT1055A	LT	•	–	–	0.15	4	0.05	10	40	4	28	14	13	5	precision JFET
LT1012C	LT+	•	A	–	0.05	1.5	0.15	4	40	0.6	17	14	0.2	0.8	precision low-bias
OPA111B	BB	•	A	–	0.25	1	0.001	10	36	3.5	30	7	2	2	precision low-bias JFET
AD744K	AD	•	–	–	0.5	10	0.1	9	36	4	45	18	75[f]	13[f]	ultra low dist, stable, fast settle
LTC1052	IL+	•	–	–	0.005	0.05	0.03	4.8	16	2	–	–	4	1.2	chopper
OP-90E	PM	•	A	A	0.15	2	15	1.6	36	0.02	60	60	0.012	0.02	precision micropower
CA3440A	RC	•	–	–	5	4[t]	0.04	4	15	(d)	250	110	0.003[e]	0.005[e]	nanopower (programmable)
AD549L	AD	•	–	–	0.5	10	60fA	10	36	0.7	90	35	3	1	ultra low input current JFET
LM10	NS+	•	–	–	2	2[t]	20	1.1	40	0.4	50	46	0.1	0.4	low supply voltage, rail-to-rail output

[a] see footnotes to Table 4.1. [b] • = this part number; A = available. [c] G>10. [d] programmable 0.02μA–10μA. [e] at I_s=1μA. [f] G>2. [h] G>5.
[m] min/max. [t] typical.

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op-amps with the very lowest input currents (MOSFET types) generally have poor voltage offsets, and vice versa. Good circuit designers choose their components with the right trade-offs to optimize performance, without going overboard on unnecessary "gold-plated" parts.

Limitations imply trade-offs

The limitations of op-amp performance we have talked about will have an influence on component values in nearly all circuits. For instance, the feedback resistors must be large enough so that they don't load the

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"Here Yesterday, Gone Today"

In its untiring quest for better and fancier chips, the semiconductor industry can sometimes cause you great pain. It might go something like this: You've designed and prototyped a wonderful new gadget; debugging is complete, and you're ready to go into production. When you try to order the parts, you discover that a crucial IC has been discontinued by the manufacturer! An even worse nightmare goes like this: Customers have been complaining about late delivery on some instrument that you've been manufacturing for many years. When you go to the assembly area to find out what's wrong, you discover that a whole production run of boards is built, except for one IC that "hasn't come in yet." You then ask purchasing why they haven't expedited the order; turns out they have, just haven't received it. Then you learn from the distributor that the part was discontinued six months ago, and that none is available!

Why does this happen, and what do you do about it? We've generally found four reasons that ICs are discontinued:

1. Obsolescence: Much better parts come along, and it doesn't make much sense to keep making the old ones. This has been particularly true with digital memory chips (e.g., small static RAMs and EPROMs, which are superseded by denser and faster versions each year), though linear ICs have not entirely escaped the purge. In these cases there is often a pin-compatible improved version that you can plug into the old socket.

2. Not selling enough: Perfectly good ICs sometimes disappear. If you are persistent enough, you may get an explanation from the manufacturer – "there wasn't enough demand," or some such story. You might characterize this as a case of "discontinued for the convenience of the manufacturer." We've been particularly inconvenienced by Harris's discontinuation of their splendid HA4925 – a fine chip, the fastest quad comparator, now gone, with no replacement anything like it. Harris also discontinued the HA2705 – another great chip, the fastest low-power op-amp, now gone without a trace! Sometimes a good chip is discontinued when the wafer fabrication line changes over to a larger wafer size (e.g., from the original 3″ diameter wafer to a 5″ or 6″ wafer). We've noticed that Harris has a particular fondness for discontinuing excellent and unique chips; Intersil and GE have done the same thing.

3. Lost schematics: You might not believe it, but sometimes the semiconductor house loses track of the schematic diagram of some chip and can't make any more! This apparently happened with the Solid State Systems SSS-4404 CMOS 8-stage divider chip.

4. Manufacturer out of business: This also happened to the SSS-4404!

If you're stuck with a board and no available IC, you've got several choices. You can redesign the board (and perhaps the circuit) to use something that is available. This is probably best if you're going into production with a new design or if you are running a large production of an existing board. A cheap and dirty solution is to make a little "daughterboard" that plugs into the empty IC socket and includes whatever it takes to emulate the nonexistent chip. Although this latter solution isn't terribly elegant, it gets the job done.

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output significantly, but they must not be so large that input bias current produces sizable offsets. High impedances in the feedback network also increase susceptibility to capacitive pickup of interfering signals and increase the loading effects of stray capacitance. These trade-offs typically dictate resistor values of 2k to 100k with general-purpose op-amps.

Similar sorts of trade-offs are involved in almost all electronic design, including the simplest circuits constructed with transistors. For instance, the choice of quiescent current in a transistor amplifier is limited at the high end by device dissipation, increased input current, excessive supply current, and reduced current gain, whereas the lower limit of operating current is limited by leakage current, reduced current gain, and reduced speed (from stray capacitance in combination with the high resistance values). For these reasons you typically wind up with collector currents in the range of a few tens of microamps to a few tens of milliamps (higher for power circuits, sometimes a bit lower in "micropower" applications), as mentioned in Chapter 2.

In the next three chapters we will look more carefully at some of these problems in order to give you a good understanding of the trade-offs involved.

EXERCISE 4.6

Draw a dc-coupled inverting amplifier with gain of 100 and $Z_{in} = 10k$. Include compensation for input bias current, and show offset voltage trimming network (10k pot between pins 1 and 5, wiper tied to V_-). Now add circuitry so that $Z_{in} \geq 10^8$ ohms.

4.13 Low-power and programmable op-amps

For battery-powered applications there is a popular group of op-amps known as "programmable op-amps," because all of the internal operating currents are set by an externally applied current at a bias programming pin. The internal quiescent currents are all related to this bias current by current mirrors, rather than by internal resistor-programmed current sources. As a consequence, such amplifiers can be programmed to operate over a wide range of supply currents, typically from a few

POPULAR OP-AMPS

Sometimes a new op-amp comes along at just the right time, filling a vacuum with its combination of performance, convenience, and price. Several companies begin to manufacture it (it becomes "second-sourced"), designers become familiar with it, and you have a hit. Here is a list of some popular favorites of recent times:

301 First easy-to-use op-amp; first use of "lateral *pnp*." External compensation. National.

741 The industry standard for many years. Internal compensation. Fairchild.

1458 Motorola's answer to the 741; two 741s in a mini-DIP, with no offset pins.

308 National's precision op-amp. Low power, superbeta, guaranteed drift specifications.

324 Popular quad op-amp (358=dual, mini-DIP). Single-supply operation. National.

355 All-purpose bi-FET op-amp (356, 357 faster). Practically as precise as bipolar, but faster and lower input current. National. (Fairchild tried to get the FET ball rolling with their 740, which flopped because of poor performance. Would you believe 0.1V input offset?)

TL081 Texas Instruments' answer to the 355 series. Low-cost comprehensive series of singles, duals, quads; low power, low noise, many package styles.

LF411 National's improved bi-FET series. Low offset, low bias, fast, low distortion, high output current, low cost. Dual (LF412) and low-power variants (LF441/2/4).

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microamps to a few milliamps. The slew rate, gain-bandwidth product f_T, and input bias current are all roughly proportional to the programmed operating current. When programmed to operate at a few microamps, programmable op-amps are extremely useful in battery-powered circuits. We will treat micropower design in detail in Chapter 14.

The 4250 was the original programmable op-amp, and it is still a good unit for many applications. Developed by Union Carbide, this classic is now "second-sourced" by many manufacturers, and it even comes in duals and triples (the 8022 and 8023, respectively). As an example of the sort of performance you can expect for operation at low supply currents, let's look at the 4250 running at 10μA. To get that operating current, we have to supply a bias current of 1.5μA with an external resistor. When it is operated at that current, f_T is 75kHz, the slew rate is 0.05V/μs, and the input bias current I_B is 3nA. At low operating currents the output drive capability is reduced considerably, and the open-loop output impedance rises to astounding levels, in this case about 3.5k. At low

THE 741 AND ITS FRIENDS

Bob Widlar designed the first really successful monolithic op-amp back in 1965, the Fairchild μA709. It achieved great popularity, but it had some problems, in particular the tendency to go into a latch-up mode when the input was overdriven and its lack of output short-circuit protection. It also required external frequency compensation (two capacitors and one resistor) and had a clumsy offset trimming circuit (again requiring three external components). Finally, its differential input voltage was limited to 5 volts.

Widlar moved from Fairchild to National, where he went on to design the LM301, an improved op-amp with short-circuit protection, freedom from latch-up, and a 30-volt differential input range. Widlar didn't provide internal frequency compensation, however, because he liked the flexibility of user compensation. The 301 could be compensated with a single capacitor, but because there was only one unused pin remaining, it still required three external components for offset trimming.

Meanwhile, over at Fairchild the answer to the 301 (the now-famous 741) was taking shape. It had the advantages of the 301, but Fairchild engineers opted for internal frequency compensation, freeing two pins to allow simplified offset trimming with a single external trimmer. Since most circuit applications don't require offset trimming (Widlar was right), the 741 in normal use requires no components other than the feedback network itself. The rest is history – the 741 caught on like wildfire and became firmly entrenched as the industry standard.

There are now numerous 741-type amps, essentially similar in design and performance, but with various features such as FET inputs, dual or quad units, versions with improved specifications, decompensated and uncompensated versions, etc. We list some of them here for reference and as a demonstration of man's instinct to clutch onto the coattails of the famous (see Table 4.1 for a more complete listing).

Single units		*Dual units*		*Quad units*	
741S	fast (10V/μs)	747	dual 741	MC4741	quad 741(alias 348)
MC741N	low noise	OP-04	precision	OP-11	precision
OP-02	precision	1458	mini-DIP package	4136	fast (3MHz)
4132	low power (35μA)	4558	fast (15V/μs)	HA4605	fast (4V/μs)
LF13741	FET low input current	TL082	FET, fast (similar to LF353)	TL084	FET, fast (similar to LF347)
748	uncompensated				
NE530	fast (25V/μs)	LF412	FET, fast		
TL081	FET, fast (similar to LF351)				
LF411	FET, fast				

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operating currents the input noise voltage rises, while the input noise current drops (see Chapter 7). The 4250 specifications claim that it can run from as little as 1 volt total supply voltage, but the claimed minimum supply voltages of op-amps may not be terribly relevant in an actual circuit, particularly where any significant output swing or drive capability is needed.

The 776 (or 3476) is an upgraded 4250, with better output-stage performance at lower currents. The 346 is a nice quad programmable op-amp, with three sections programmed by one of the programming inputs, and the fourth programmed by the other. Some other programmable op-amps constructed with ordinary bipolar transistors are the OP-22, OP-32, HA2725, and CA3078. Programmable CMOS op-amps include the ICL7612, TLC251, MC14573, and CA3440. These feature operation at very low supply voltage (down to 1V for the TLC251) and, for the astounding 3440, operation at quiescent currents down to 20 *nano*amps. The 7612 and 251 use a variation of the usual programming scheme; their quiescent current is pin-selectable (10μA, 100μA, or 1mA), according to whether the programming pin is connected to V_+ or V_- or is left open.

In addition to these op-amps, there are several nonprogrammable op-amps that have been designed for low supply currents and low-voltage operation and should be considered for low-power applications. Notable among these is the outstanding bipolar LM10, an op-amp that is fully specified at 1 volt total supply voltage ($\pm$0.5V, for example). This is extraordinary, considering that V_{BE} increases with decreasing temperature and is close to 1 volt at $-55°C$, the lower limit of the LM10's operating range. Some other excellent "micropower" op-amps (and their operating currents) are the precision OP-20 (40μA), OP-90 (12μA), and LT1006 (90μA), the inexpensive quad LP324 (20μA per amplifier), the JFET LF441/2/4 (150μA per amplifier), and the MOSFET TLC27L4 (10μA per amplifier).

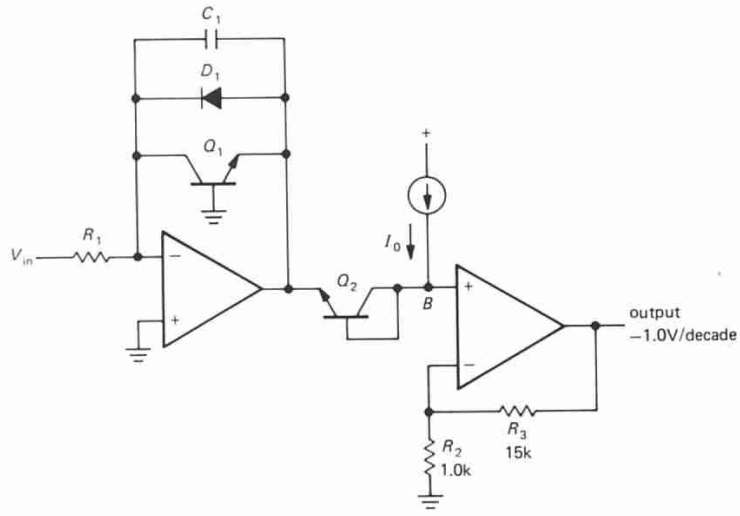


Figure 4.35. Logarithmic converter. Q_1 and Q_2 compose a monolithic matched pair.

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TABLE 4.3. HIGH-VOLTAGE OP-AMPS

Type	Mfg[a]	Total supply min (V)	Total supply max (V)	Diff'l input[b] max (V)	FET	Ext comp	Trim	f_T typ (MHz)	Slew rate typ (V/μs)	Output current max (mA)	P_{diss} (50°C) max (W)	Therm lim	Case[c]	Comments
LM675	NS	20	60	60	–	–	–	5.5	8	3000	40	•	TO-220	monolithic pwr op-amp
LM343	NS	10	68	68	–	–	•	1	2	20	0.6	–	TO-99	superbeta
LM344	NS	10	68	68	–	•	–	1	30[d]	20	0.6	–	TO-99	superbeta
3580	BB	30	70	70	•	–	•	5	15	60	4.5	•	TO-3I	
LM12	NS	20	80	80	–	–	–	0.7	9	10000	90	•	TO-3	monolithic high-power
PA19	AP	30	80	40	•	•	–	100[e]	650[d]	5000	70	•	TO-3I	VMOS output
OPA541	BB	20	80	80	•	–	–	2	10	10000	90	–	TO-3I	monolithic high-pwr
MC1436	MO	10	80	80	–	–	•	1	2	10	0.6	–	TO-99	original, still good
1460	TP	30	80	6	–	•	•	1000[e]	300[e]	150	2.5	–	TO-3	VMOS output
1461	TP	30	80	25	•	•	•	1000[e]	1200[e]	750		–	P-DIP	VMOS output
1463	TP	30	80	25	•	–	•	17	165	1000	40	–	TO-3	fast unity-gain comp
HA2645	HA	20	80	74	–	•	•	4	5	10	0.6	•	TO-99	same as Philbrick 1332
OPA445	BB	20	100	80	•	–	•	2	10	15	0.6	–	TO-99	monolithic; miniDIP also
1481	TP	30	150	150	•	–	•	4.5	25	80	15	–	TO-3	current limit
3581	BB	65	150	150	•	–	•	5	20	30	4.5	•	TO-3I	
PA04	AP	30	200	20	•	•	–	2	50	20000	160	–	P-DIP	VMOS output; curr lim
1480	TP	30	300	450	•	–	•	20	100	80		•	TO-3	
3582	BB	140	300	300	•	–	•	5	20	15	4.5	•	TO-3I	
3583	BB	80	300	300	•	–	•	5	30	75	10	•	TO-3	
3584	BB	140	300	300	•	•	•	20[e]	150[e]	15	4.5	•	TO-3	
PA08V	AP	30	340	50	•	–	•	5	30	150	18	•	TO-3I	low V_{os}, low e_n
PA88	AP	30	450	25	•	•	–	1[d]	30[e]	100	12	•	TO-3I	low I_Q, V_{os}, e_n, VMOS
PA85	AP	30	450	25	•	•	–	20[d]	1000[e]	200	28	•	TO-3I	low V_{os}, low e_n, VMOS

[a] see notes to Table 4.1. [b] not to exceed total supply voltage. [c] "I" = isolated. [d] when comp for G>10. [e] when comp for G>100.

A DETAILED LOOK AT SELECTED OP-AMP CIRCUITS

The performance of the next few circuits is affected significantly by the limitations of op-amps; we will go into a bit more detail in their description.

4.14 Logarithmic amplifier

The circuit shown in Figure 4.35 exploits the logarithmic dependence of V_{BE} on I_C to produce an output proportional to the logarithm of a positive input voltage. R_1 converts V_{in} to a current, owing to the virtual ground at the inverting input. That current flows through Q_1, putting its emitter one V_{BE} drop below ground, according to the Ebers-Moll equation. Q_2, which operates at a fixed current, provides a diode drop of correction voltage, which is essential for temperature compensation. The current source (which can be a resistor, since point B is always within a few tenths of a volt of ground) sets the input current at which the output voltage is zero. The second op-amp is a noninverting amplifier with a voltage gain of 16, in order to give an output voltage of -1.0 volt per decade of input current (recall that V_{BE} increases 60mV per decade of collector current).

Some further details: Q_1's base could have been connected to its collector, but the base current would then have caused an error (remember that I_C is an accurate exponential function of V_{BE}). In this

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TABLE 4.4. POWER OP-AMPS

Type	Mfg[a]	monolithic	FET	Trim?	Pkg[b]	I_{out} (A)	± V_{supply} min (V)	± V_{supply} max (V)	P_{diss} (W)	SR typ (V/µs)	f_T typ (MHz)	pwr BW (kHz)	V_{os}(max) (mV)	V_{os}(max) (µV/°C)	V_{os}(max) (µV/W)
PA03	AP	–	•	•	PD	30	15	75	500	10	5	70	3	30	20[t]
PA04A	AP	–	•	–	PD	20	15	100	200	50	2	90	5	30	10[t]
OPA512	BB	–	–	–	3I	15	10	50	125	4	4	20	3	40	20[t]
LM12	NS	•	–	–	3	10	10	40	90	9	0.7	60	7	50	50
OPA501	BB	–	–	–	3I	10	10	40	80	1.4[m]	1	16	5	40	35[t]
OPA512B	BB	–	–	–	3I	10	10	50	125	4	4	20	6	65	20[t]
OPA541B	BB	•	•	–	3I	10	10	40	90	10	2	55	2	30	60
1468	TP	–	–	–	3	10	10	50	125	4	4	20	6	65	20[t]
PA19A	AP	–	•	–	3I	5	15	40	70	900	100	3500	0.5	10	20[t]
OPA511	BB	–	–	–	3I	5	10	30	67	1.8	1	23	10	65	20[t]
PA09A	AP	–	•	•	3I	4	10	40	78	400	75	2500	0.5	10	
SG1173	SG	•	–	–	220	3.5	5	25	20	0.8	1		4	30	-
LM675	NS	•	–	–	220	3	8	30	40	8	5.5		10	25[t]	25[t]
LH0101	NS	–	•	–	3	2	5	20	62	10	5	300	3	10[t]	150[t]
3572	BB	–	•	–	3I	2	15	40	60	3	0.5	16	2	40	20[t]
3573	BB	–	–	–	3I	2	10	34	45	1.5	1	23	10	65	
LH0021	NS	–	–	–	3	1	5	15	23	3	1	20	3	25	15
MSK792	KE	–	–	•	3	1	5	22	5	2	1	11	0.1	2	-
1463	TP	–	•	•	3	1	15	40	40	165	17		5	20[t]	
1461	TP	–	•	•	PD	0.75	15	40		1200[u]	1000[u]		5	50	-
LH0061	NS	–	–	•	3	0.5	-	15	20	70	-	1000	4	5[t]	5[t]
WA01A	AP	–	–	•	3I	0.4	12	16	10	4000	1000	150000	5	25	10[t]
CLC203	CL	–	–	–	PD	0.2	9	20		6000	5000	60000	1.5	15	
1460	TP	–	–	•	3	0.15	15	40	2.5	300[u]	1000[u]	1500	5	50	-
3554B	BB	–	•	•	3I	0.15	5	18	5	1200	100	19000	1	15	-
HA2542	HA	•	–	•	D	0.1	5	15	1.6	375	120	4700[m]	10[m]	20	-
LH4101	NS	–	•	•	D	0.1	-	15	4	250	28	-	15	25[t]	-
LH4104	NS	–	•	•	C	0.1	-	15	2.5	40	18	-	5	20[t]	-
1480	TP	–	•	•	3	0.08	15	150		100	20	120	3	100	-
1481	TP	–	•	•	3	0.08	15	75	15	25	4.5	50	3	25	-
CA3450	RC	•	–	•	D	0.08	-	7	1.5	420	190	10000	15	-	-
3583	BB	–	•	•	3I	0.08	40	140	10	30	5	60	3	23	-
OP-50E	PM	•	–	•	D	0.07	5	18	0.5	3	25	20	0.03	0.3	-
3580	BB	–	•	•	3I	0.06	15	35	4.5	15	5	100	10	30	-
AMP-01E	PM	•	–	•	D	0.05	5	15	0.5	4.5	1	20	0.05	0.3	-
3581	BB	–	•	•	3I	0.03	32	75	4.5	20	5	60	3	25	-
3582/4	BB	–	•	•	3I	0.02	70	150	4.5	20/150	7	30/135	3	25	-

[a] see Table 4.1 notes. [b] 3 – TO-3; 220 – TO-220; PD – power DIP; D – DIP; I – isolated; C – metal can.
[c] current limit: T – thermal limit; E – external adjust. [m] min or max. [t] typical. [u] uncompensated.

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Type	I_b (max) @ 25°C (nA)	I_b (max) @ T_{max} (nA)	V_{sat} (V)	V_{sat} @ (A)	t_s (typ) (µs)	t_s (typ) to (%)	I_{lim}[c] (A)	Thermal limit	Comments
PA03	0.05	50	7	30	2	0.1	T	•	a mighty brute
PA04A	0.02	-	7.5	15	2.5	0.1	E	–	high voltage brute
OPA512	20	15	7	15	2	0.1	E	–	PA-12 similar
LM12	300	150	8	10			13	•	
OPA501	20	15	7	10			E	–	PA-51 similar
OPA512B	30	-	6	10	2	0.1	E	–	
OPA541B	0.05	40	4.5	5	2	0.1	E	–	monolithic JFET
1468	30	-	6	10	2	0.1	E	–	
PA19A	0.05	50	5	4	1.2	0.01	E	•	VMOS output, wideband, prec
OPA511	40	30	8	5	2	0.1	E	–	PA-01 similar
PA09A	0.02	20	8	2	0.3	0.1	4.5	•	fast
SG1173	500	300	6	2			3.5	•	
LM675	2µA		10	3.5			4	•	
LH0101	0.3	300	5	2	2	0.01	E	–	PA-02 similar
3572	0.1	100	5	2			E	•	PA-07 similar; 3571 to 1A
3573	40	30	5	2			E	–	PA-73 similar
LH0021	100	35	4	1	4	0.1	E	–	ext comp
MSK792	100	100	3.5	1			E	–	
1463	0.2	200	8	1	0.25	0.1	E	–	VMOS output
1461	0.1	100	9	0.5	0.4	0.1	E	–	VMOS output; ext comp
LH0061	100	35	5	0.5	0.8	0.1	E	–	ext comp
WA01A	10µA		5	0.4	0.02	0.1			
CLC203	20µA	20µA	4	0.2	15ns	0.2	E	–	fast settle, wideband, prec
1460	10µA	-	6	0.15	1	0.1	0.25	–	VMOS output; ext comp
3554B	0.05	50	5	0.1	0.2	0.01	0.15	–	fast
HA2542	35µA	-	-	-	0.1	0.1	-	–	decomp (G>2)
LH4101	0.5	500	-	-	0.3	0.1	-	–	
LH4104	0.6	25	5	0.1	0.5	0.01	-	–	LH4105 has V_{os}<0.5mV
1480	0.2	200	10	0.08	1.5	0.01	0.13	–	high voltage
1481	0.1	100	5	0.08	7.5	0.1	0.13	–	
CA3450	350	-	2	0.08	35ns	0.1	-	–	video amp
3583	0.02	20	10	0.08	12	0.1	0.1	•	high voltage
OP-50E	5	7[f]	2	0.03	30	0.01	0.06	•	low noise, precision
3580	0.05	50	5	0.06	12	0.1	0.1	•	
AMP-01E	3	10[f]	2	0.03	15	0.01	0.06	•	low noise, prec inst amp
3581	0.02	20	5	0.03	12	0.1	0.05	•	
3582/4	0.02	20	5	0.02	12	0.1	0.03	•	high voltage

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circuit the base is at the same voltage as the collector because of the virtual ground, but there is no base-current error. Q_1 and Q_2 should be a matched pair, thermally coupled (a matched monolithic pair like the LM394 or MAT-01 is ideal). This circuit will give accurate logarithmic output over seven decades of current or more (1nA to 10mA, approximately), providing that low-leakage transistors and a low-bias-current input op-amp are used. An op-amp like the 741 with 80nA of bias current is unsuitable, and a FET-input op-amp like the 411 is usually required to achieve the full seven decades of linearity. Furthermore, in order to give good performance at low input currents, the input op-amp must be accurately trimmed for zero offset voltage, since V_{in} may be as small as a few tens of microvolts at the lower limit of current. If possible, it is better to use a current input to this circuit, omitting R_1 altogether.

The capacitor C_1 is necessary to stabilize the feedback loop, since Q_1 contributes voltage gain inside the loop. Diode D_1 is necessary to prevent base-emitter breakdown (and destruction) of Q_1 in the event the input voltage goes negative, since Q_1 provides no feedback path for positive op-amp output voltage. Both these minor problems are avoided if Q_1 is wired as a diode, i.e., with its base tied to its collector.

Temperature compensation of gain

Q_2 compensates changes in Q_1's V_{BE} drop as the ambient temperature changes, but the changes in the slope of the curve of V_{BE} versus I_C are not compensated. In Section 2.10 we saw that the "60mV/decade" is proportional to absolute temperature. The output voltage of this circuit will look as shown in Figure 4.36. Compensation is perfect at an input current equal to I_0, Q_2's collector current. A change in temperature of 30°C causes a

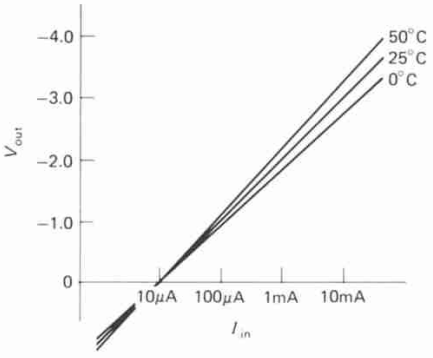


Figure 4.36

10% change in slope, with corresponding error in output voltage. The usual solution to this problem is to replace R_2 with a series combination of an ordinary resistor and a resistor of positive temperature coefficient. Knowing the temperature coefficient of the resistor (e.g., the TG 1/8 type manufactured by Texas Instruments has a coefficient of +0.67%/°C) allows you to calculate the value of the ordinary resistor to put in series in order to effect perfect compensation. For instance, with the 2.7k TG 1/8 type "sensistor" just mentioned, a 2.4k series resistor should be used.

There are several logarithmic converter modules available as complete integrated circuits. These offer very good performance, including internal temperature compensation. Some manufacturers are Analog Devices, Burr–Brown, Philbrick, Intersil, and National Semiconductor.

EXERCISE 4.7

Finish up the log converter circuit by (a) drawing the current source explicitly and (b) using a TG 1/8 resistor (+0.67%/°C tempco) for thermal slope compensation. Choose values so that $V_{out} = +1$ volt per decade, and provide an output offset control so that V_{out} can be set to zero for any desired input current (do this with an inverting amplifier offset circuit, not by adjusting I_0).

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4.15 Active peak detector

There are numerous applications in which it is necessary to determine the peak value of some input waveform. The simplest method is a diode and capacitor (Fig. 4.37). The highest point of the input waveform charges up C, which holds that value while the diode is back-biased.

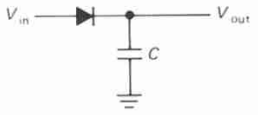


Figure 4.37

This method has some serious problems. The input impedance is variable and is very low during peaks of the input waveform. Also, the diode drop makes the circuit insensitive to peaks less than about 0.6 volt and inaccurate (by one diode drop) for larger peak voltages. Furthermore, since the diode drop depends on temperature and current, the circuit's inaccuracies depend on the ambient temperature and on the rate of change of output; recall that $I = C(dV/dt)$. An input emitter follower would improve the first problem only.

Figure 4.38 shows a better circuit, using feedback. By taking feedback from the voltage at the capacitor, the diode drop doesn't cause any problems. The sort of output waveform you might get is shown in Figure 4.39.

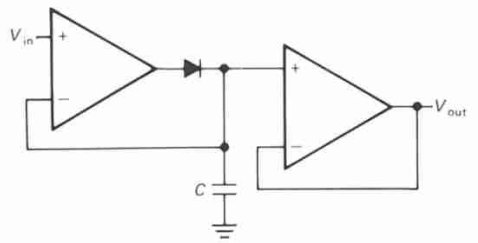


Figure 4.38. Op-amp peak detector.

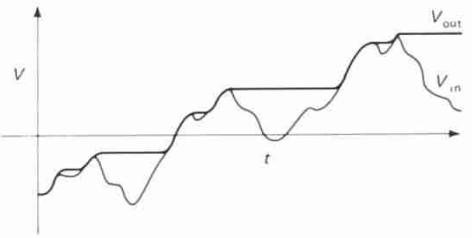


Figure 4.39

Op-amp limitations affect this circuit in three ways: (a) Finite op-amp slew rate causes a problem, even with relatively slow input waveforms. To understand this, note that the op-amp's output goes into negative saturation when the input is less positive than the output (try sketching the op-amp voltage on the graph; don't forget about diode forward drop). So the op-amp's output has to race back up to the output voltage (plus a diode drop) when the input waveform next exceeds the output. At slew rate S, this takes roughly $(V_0 - V_-)/S$, where V_- is the negative supply voltage and V_0 is the output voltage. (b) Input bias current causes a slow discharge (or charge, depending on the sign of the bias current) of the capacitor. This is sometimes called "droop," and it is best avoided by using op-amps with very low bias current. For the same reason, the diode must be a low-leakage type (e.g., the FJT1100, with less than 1pA reverse current at 20V, or a "FET diode" such as the PAD-1 from Siliconix or the ID101 from Intersil), and the following stage must also present high impedance (ideally it should also be a FET or FET-input op-amp). (c) The maximum op-amp output current limits the rate of change of voltage across the capacitor, i.e., the rate at which the output can follow a rising input. Thus, the choice of capacitor value is a compromise between low droop and high output slew rate.

For instance, a 1μF capacitor used in this circuit with the common 741 (which

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would be a poor choice because of its high bias current) would droop at $dV/dt = I_B/C = 0.08\text{V/s}$ and would follow input changes only up to $dV/dt = I_{\text{output}}/C = 0.02\text{V}/\mu s$. This maximum follow rate is much less than the op-amp's slew rate of $0.5\text{V}/\mu\text{s}$, being limited by the maximum output current of 20mA driving $1\mu\text{F}$. By decreasing C you could achieve greater output slewing rate at the expense of greater droop. A more realistic choice of components would be the popular LF355 FET-input op-amp as driver and output follower (30pA typical bias current, 20mA output current) and a value of $C = 0.01\mu\text{F}$. With this combination you would get a droop of only 0.006V/s and an overall circuit slew rate of $2\text{V}/\mu\text{s}$. For better performance, use a FET op-amp like the OPA111 or AD549, with input currents of 1pA or less. Capacitor leakage may then limit performance even if unusually good capacitors are used, e.g., polystyrene or polycarbonate (see Section 7.05).

□ *A circuit cure for diode leakage*

Quite often a clever circuit configuration can provide a solution to problems caused by nonideal behavior of circuit components. Such solutions are aesthetically pleasing as well as economical. At this point we yield to the temptation to take a closer look at such a high-performance design, rather than delaying until Chapter 7, where we treat such subjects under the heading of precision design.

Suppose we want the best possible performance in a peak detector, i.e., highest ratio of output slew rate to droop. If the lowest-input-current op-amps are used in a peak-detector circuit (some are available with bias currents as low as 0.01pA), the droop will be dominated by diode leakage; i.e., the best available diodes have higher leakage currents (see Table 1.1) than the op-amps' bias currents. Figure 4.40 shows a clever circuit solution. As before, the voltage on the capacitor follows a rising input waveform: IC_1 charges the capacitor through both diodes and is unaffected by IC_2's output. When the input drops below the peak value, IC_1 goes into negative saturation, but IC_2 holds point X at the capacitor voltage, eliminating leakage altogether in D_2. D_1's small leakage current flows through R_1, with negligible drop across the resistor. Of course, both op-amps must have low bias current. The OPA111B is a good choice here, with its combination of precision ($V_{os} = 250\mu\text{V}$, max) and low input current (1pA, max). This circuit is analogous to the so-called guard circuits used for high-impedance or small-signal measurements.

Note that the input op-amps in both peak-detector circuits spend most of their time in negative saturation, only popping up when the input level exceeds the peak voltage previously stored on the capacitor. However, as we saw in the active rectifier circuit (Section 4.10), the journey from negative saturation can take a while (e.g., $1\mu\text{s}$–$2\mu\text{s}$ for the LF411). This may restrict your choice to high-slew-rate op-amps.

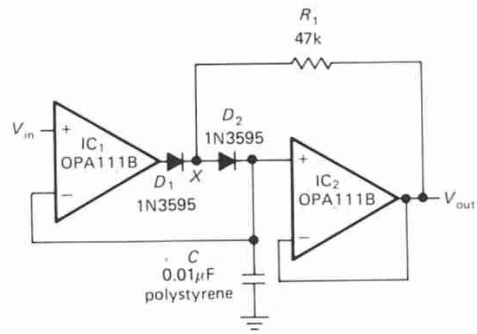


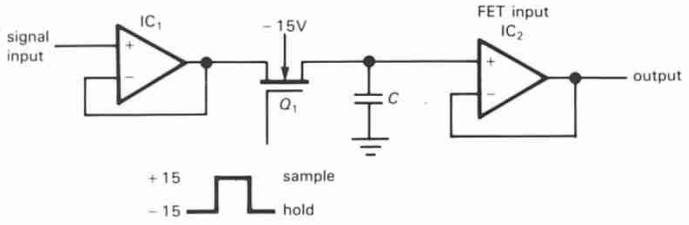
Figure 4.40

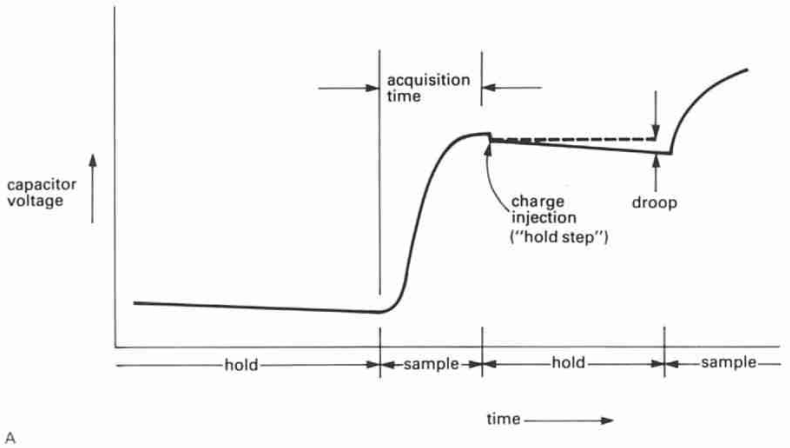
□ *Resetting a peak detector*

In practice it is usually desirable to reset the output of a peak detector in some way.

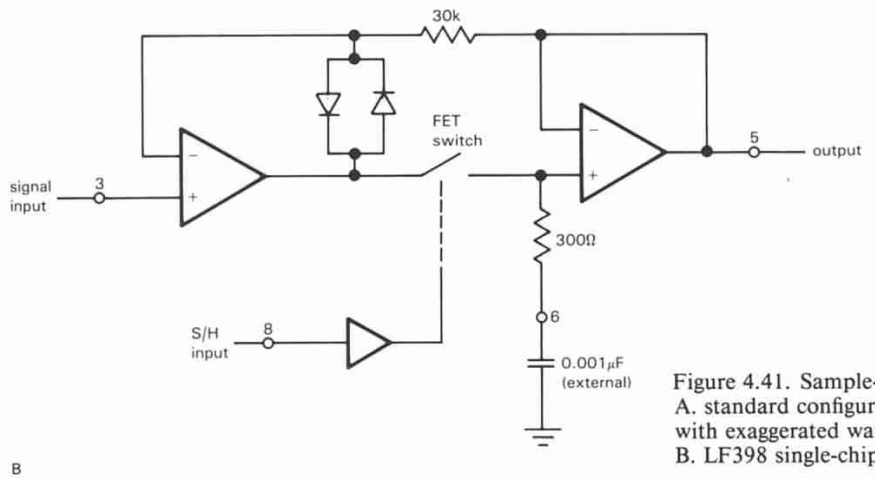
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One possibility is to put a resistor across the output so that the circuit's output decays with a time constant RC. In this way it holds only the most recent peak values. A better method is to put a transistor switch across C; a short pulse to the base then zeros the output. A FET switch is often used instead. For example, in Figure 4.38 you could connect an n-channel MOSFET across C; bringing the gate momentarily positive then zeros the capacitor voltage.





A



B

Figure 4.41. Sample-and-hold.
A. standard configuration, with exaggerated waveform.
B. LF398 single-chip S/H.

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4.16 Sample-and-hold

Closely related to the peak detector is the "sample-and-hold" (S/H) circuit (sometimes called "follow-and-hold"). These are especially popular in digital systems, where you want to convert one or more analog voltages to numbers so that a computer can digest them: The favorite method is to grab and hold the voltage(s), then do the digital conversion at your leisure. The basic ingredients of a S/H circuit are an op-amp and a FET switch; Figure 4.41A shows the idea. IC_1 is a follower to provide a low-impedance replica of the input. Q_1 passes the signal through during "sample" and disconnects it during "hold." Whatever signal was present when Q_1 was turned OFF is held on capacitor C. IC_2 is a high-input-impedance follower (FET inputs), so that capacitor current during "hold" is minimized. The value of C is a compromise: Leakage currents in Q_1 and the follower cause C's voltage to "droop" during the hold interval, according to $dV/dt = I_{\text{leakage}}/C$. Thus C should be large to minimize droop. But Q_1's ON resistance forms a low-pass filter in combination with C, so C should be small if high-speed signals are to be followed accurately. IC_1 must be able to supply C's charging current $I = CdV/dt$ and must have sufficient slew rate to follow the input signal. In practice, the slew rate of the whole circuit will usually be limited by IC_1's output current and Q_1's ON resistance.

EXERCISE 4.8

Suppose IC_1 can supply 10mA of output current, and $C = 0.01\mu F$. What is the maximum input slew rate the circuit can accurately follow? If Q_1 has 50 ohms ON resistance, what will be the output error for an input signal slewing at 0.1V/μs? If the combined leakage of Q_1 and

□ DIELECTRIC ABSORPTION

Capacitors are not perfect. The most commonly appreciated shortcomings are leakage (parallel resistance), series resistance and inductance, and nonzero temperature coefficient of capacitance. A more subtle problem is *dielectric absorption*, an effect that manifests itself clearly as follows: Take a large-value tantalum capacitor that is charged up to 10 volts or so, and rapidly discharge it by momentarily putting a 100 ohm resistor across it. Remove the resistor, and watch the capacitor's voltage on a high-impedance voltmeter. You will be amazed to see the capacitor *charge back up*, reaching perhaps a volt or so after a few seconds!

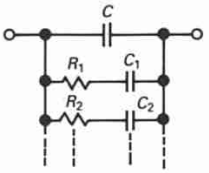
The origins of dielectric absorption (or dielectric *soakage*, dielectric *memory*) are not entirely understood, but the phenomenon is believed to be related to remnant polarization trapped on dielectric interfaces; mica, for example, with its layered structure, is particularly poor in this regard. From a circuit point of view, this extra polarization behaves like a set of additional series RCs across the capacitor (Fig. 4.42A), with time constants generally in the range of $\approx$100μs to several seconds. Dielectrics vary widely in their susceptibility to dielectric absorption; Figure 4.42B shows data for several high-quality dielectrics, plotted as voltage memory versus time after a 10 volt step of 100μs duration.

Dielectric absorption can cause significant errors in integrators and other analog circuits that rely on the ideal characteristics of capacitors. In the case of a sample/hold followed by precision analog-to-digital conversion, the effect can be devastating. In such situations the best approach is to choose your capacitors carefully (Teflon dielectric seems to be best), retaining a healthy skepticism until proven wrong. In extreme cases you may have to resort to tricks such as compensation networks that use carefully trimmed RCs to electrically cancel the capacitor's internal dielectric absorption. This approach is used in some high-quality sample/hold modules made by Hybrid Systems.

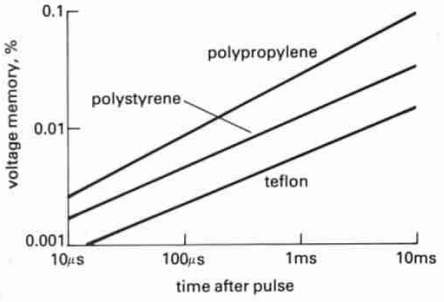
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IC_2 is 1nA, what is the droop rate during the "hold" state?

For both the sample/hold circuit and the peak detector, an op-amp drives a capacitive load. When designing such circuits, make sure you choose an op-amp that is stable at unity gain when loaded by the capacitor C. Some op-amps, (e.g., the LF355/6) are specifically designed to drive large (0.01μF) capacitive loads directly. Some other tricks you can use are discussed in Section 7.07 (see Fig. 7.17).



A



B

Figure 4.42. Dielectric absorption in capacitors. A. model B. measured properties for several dielectrics. (After Hybrid Systems HS9716 data sheet.)

You don't have to design S/H circuits from scratch, because there are nice monolithic ICs that contain all the parts you need except for the capacitor. National's LF398 is a popular part, containing the FET switch and two op-amps in an inexpensive ($2) 8-pin package. Figure 4.41B shows how to use it. Note how feedback closes the feedback loop around *both* op-amps. There are plenty of fancy S/H chips

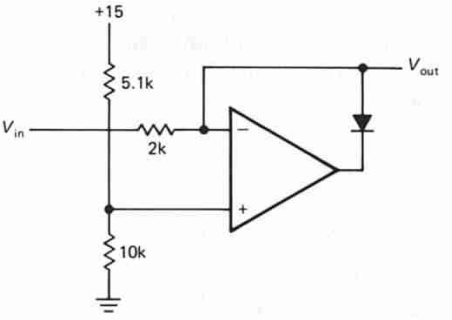


Figure 4.43

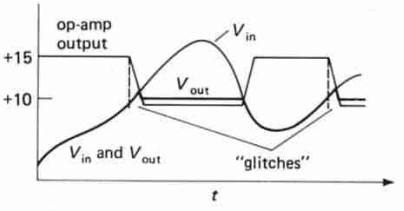


Figure 4.44

available, if you need better performance than the LF398 offers; for example, the AD585 from Analog Devices includes an internal capacitor and guarantees a maximum acquisition time of 3μs for 0.01% accuracy following a 10 volt step.

□ 4.17 Active clamp

Figure 4.43 shows a circuit that is an active version of the clamp function we discussed in Chapter 1. For the values shown, $V_{in} < +10$ volts puts the op-amp output at positive saturation, and $V_{out} = V_{in}$. When V_{in} exceeds +10 volts the diode closes the feedback loop, clamping the output at 10 volts. In this circuit, op-amp slew-rate limitations allow small glitches as the input reaches the clamp voltage from below (Fig. 4.44).

□ 4.18 Absolute-value circuit

The circuit shown in Figure 4.45 gives a positive output equal to the magnitude of

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the input signal; it is a full-wave rectifier. As usual, the use of op-amps and feedback eliminates the diode drops of a passive full-wave rectifier.

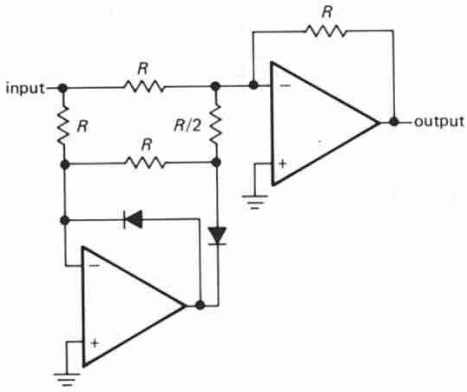


Figure 4.45. Active full-wave rectifier.

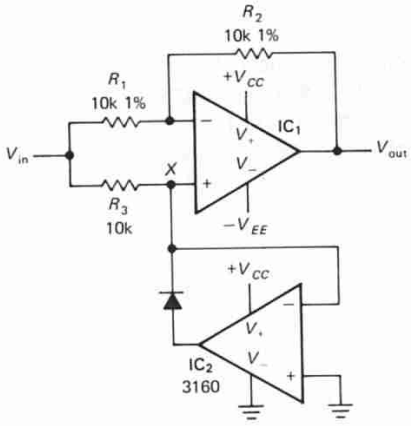


Figure 4.46

EXERCISE 4.9

Figure out how the circuit in Figure 4.45 works. Hint: Apply first a positive input voltage, and see what happens; then do negative.

Figure 4.46 shows another absolute-value circuit. It is readily understandable as a simple combination of an optional inverter (IC_1) and an active clamp (IC_2). For positive input levels the clamp is out of the circuit, with its output at negative saturation, making IC_1 a unity-gain inverter. Thus the output is equal to the absolute value of the input voltage. By running IC_2 from a single positive supply, you avoid problems of slew-rate limitations in the clamp, since its output moves over only one diode drop. Note that no great accuracy is required of R_3.

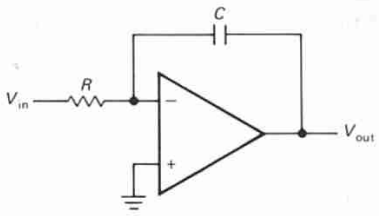


Figure 4.47. Integrator.

4.19 Integrators

Op-amps allow you to make nearly perfect integrators, without the restriction that $V_{out} \ll V_{in}$. Figure 4.47 shows how it's done. Input current V_{in}/R flows through C. Because the inverting input is a virtual ground, the output voltage is given by

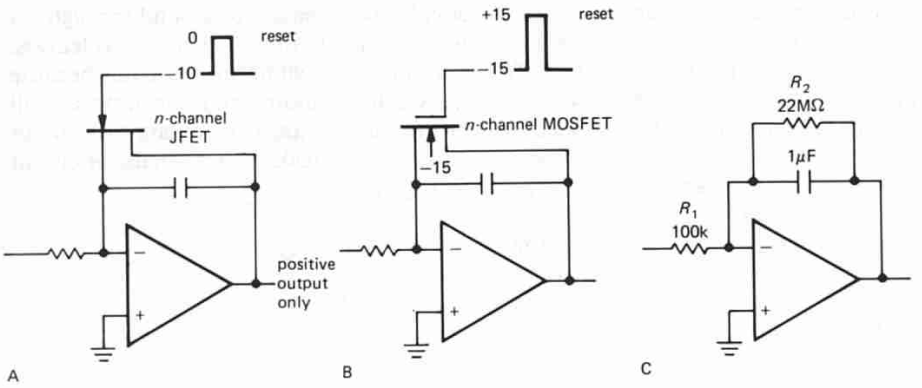
$$V_{in}/R = -C(dV_{out}/dt)$$

or

$$V_{out} = \frac{1}{RC}\int V_{in}\,dt + \text{constant}$$

The input can, of course, be a current, in which case R will be omitted. One problem with this circuit as drawn is that the output tends to wander off, even with the input grounded, due to op-amp offsets and bias current (there's no feedback at dc, which violates rule 3 in Section 4.08). This problem can be minimized by using a FET op-amp for low input current and offset, trimming the op-amp input offset voltage, and using large R and C values. In addition, in many applications the integrator is zeroed periodically by closing a

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4.48. Op-amp integrators with reset switches.

switch placed across the capacitor (usually a FET), so only the drift over short time scales matters. As an example, an inexpensive FET op-amp like the LF411 (25pA typical bias current) trimmed to a voltage offset of 0.2mV and used in an integrator with $R = 10\text{M}\Omega$ and $C = 10\mu\text{F}$ will produce an output drift of less than 0.003 volt in 1000 seconds.

If the residual drift of the integrator is still too large for a given application, it may be necessary to put a large resistor R_2 across C to provide dc feedback for stable biasing. The effect is to roll off the integrator action at very low frequencies, $f < 1/R_2C$. Figure 4.48 shows integrators with FET zeroing switch and with resistor bias stabilization. The feedback resistor may become rather large in this sort of application. Figure 4.49 shows a trick for producing the effect of a large feedback resistor using smaller values. In this case the feedback network behaves like a single 10MΩ resistor in the standard inverting amplifier circuit giving a voltage gain of −100. This technique has the advantage of using resistors of convenient values without the problems of stray capacitance, etc., that occur with very large resistor values. Note that this "T-network" trick may increase the effective input offset voltage, if used in a transresistance configuration (Section 4.09). For example, the circuit of Figure 4.49, driven from a high-impedance source (e.g., the current from a photodiode, with the input resistor omitted), has an output offset of 100 times V_{os}, whereas the same circuit with a 10MΩ feedback resistor has an output equal to V_{os} (assuming the offset due to input current is negligible).

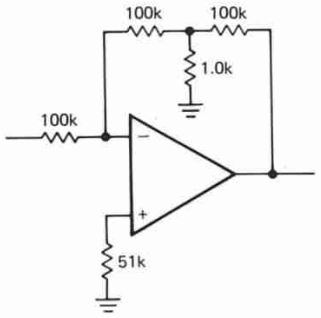


Figure 4.49

□ *A circuit cure for FET leakage*

In the integrator with a FET reset switch (Fig. 4.48), drain-source leakage sources a small current into the summing junction even when the FET is OFF. With an ultra-low-input-current op-amp and low-leakage

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capacitor, this can be the dominant error in the integrator. For example, the excellent AD549 JFET-input "electrometer" op-amp has a maximum input current of 0.06pA, and a high-quality 0.01μF metallized Teflon or polystyrene capacitor specifies leakage resistance as 10^7 *meg*ohms, minimum. Thus the integrator, exclusive of reset circuit, keeps stray currents at the summing junction below 1pA (for a worst-case 10V full-scale output), corresponding to an output dV/dt of less than 0.01mV/s. Compare this with the leakage contribution of a MOSFET such as the popular 2N4351 (enhancement mode), which specifies a maximum leakage current of 10nA at $V_{DS} = 10$V and $V_{GS} = 0$V! In other words, the FET contributes 10,000 times as much leakage as everything else combined.

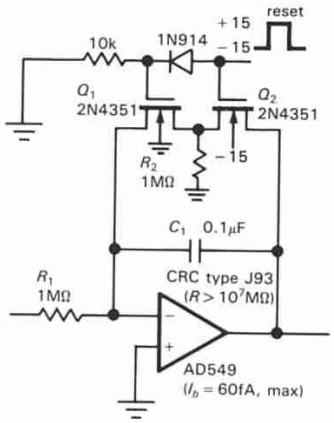


Figure 4.50

Figure 4.50 shows a clever circuit solution. Although both n-channel MOSFETs are switched together, Q_1 is switched with gate voltages of zero and +15 volts so that gate leakage (as well as drain-source leakage) is entirely eliminated during the OFF state (zero gate voltage). In the ON state the capacitor is discharged as before, but with twice R_{ON}. In the OFF state, Q_2's small leakage passes to ground through R_2 with negligible drop. There is no leakage current at the summing junction because Q_1's source, drain, and substrate are all at the same voltage. Compare this circuit with the zero-leakage peak-detector circuit of Figure 4.40.

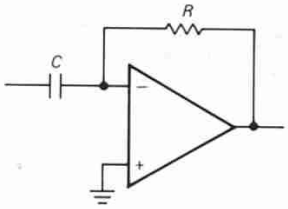


Figure 4.51

□ 4.20 Differentiators

Differentiators are similar to integrators, but with R and C reversed (Fig. 4.51). Since the inverting input is at ground, the rate of change of input voltage produces a current $I = C(dV_{in}/dt)$ and hence an output voltage

$$V_{out} = -RC\frac{dV_{in}}{dt}$$

Differentiators are bias-stable, but they generally have problems with noise and instabilities at high frequencies because of the op-amp's high gain and internal phase shifts. For this reason it is necessary to roll off the differentiator action at some maximum frequency. The usual method is shown in Figure 4.52. The choice of the rolloff components R_1 and C_2 depends on the noise level of the signal and the bandwidth of the op-amp. At high frequencies this circuit becomes an integrator, due to R_1 and C_2.

□ OP-AMP OPERATION WITH A SINGLE POWER SUPPLY

Op-amps don't *require* ±15 volt regulated supplies. They can be operated from split

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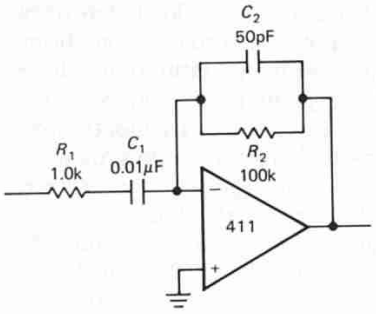


Figure 4.52

supplies of lower voltages, or from unsymmetrical supply voltages (e.g, +12 and −3), as long as the total supply voltage ($V_+ - V_-$) is within specifications (see Table 4.1). Unregulated supply voltages are often adequate because of the high "power-supply rejection ratio" you get from negative feedback (for the 411 it's 90dB typ). But there are many occasions when it would be nice to operate an op-amp from a single supply, say +12 volts. This can be done with ordinary op-amps by generating a "reference" voltage above ground, if you are careful about minimum supply voltages, output swing limitations, and maximum common-mode input range. With some of the more recent op-amps whose input and output ranges include the negative supply (i.e., ground, when run from a single positive supply), single-supply operation is attractive because of its simplicity. Keep in mind, though, that operation with symmetrical split supplies remains the usual technique for nearly all applications.

□ 4.21 Biasing single-supply ac amplifiers

For a general-purpose op-amp like the 411, the inputs and output can typically swing to within about 1.5 volts of either supply. With V_- connected to ground, you can't have either of the inputs or the output at ground. Instead, by generating a reference voltage (e.g., $0.5V_+$) you can bias the op-amp for successful operation (Fig. 4.53). This circuit is an audio amplifier with 40dB gain. $V_{ref} = 0.5V_+$ gives an output swing of about 17 volts pp before onset of clipping. Capacitive coupling is used at the input and output to block the dc level, which equals V_{ref}.

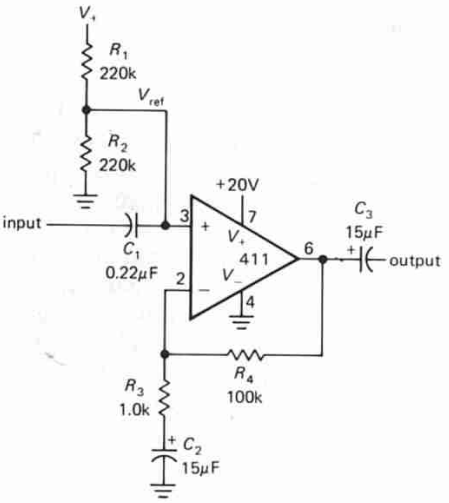


Figure 4.53

□ 4.22 Single-supply op-amps

There is a class of op-amps that permit simplified operation with a single positive supply, because they permit input voltages all the way down to the negative rail (normally tied to ground). They can be further divided into two types, according to the capability of the output stage: One type can swing all the way down to V_-, and the other type can swing all the way to *both* rails:

1. The LM324 (quad) / LM358 (dual), LT1013, and TLC270 types. These have input common-mode ranges all the way down to 0.3 volt *below* V_-, and the output can swing down to V_-. Both inputs and output can go to within 1.5 volts of V_+. If

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instead you need an input range up to V_+, use something like an LM301/307, OP-41, or a 355; an example is illustrated in Section 6.24 in the discussion of constant-current supplies. In order to understand some of the subtleties of this sort of op-amp, it is helpful to look at the schematic (Fig. 4.54). It is a reasonably straightforward differential amplifier, with current mirror active load on the input stage and push-pull complementary output stage with current limiting. The special things to remember are these (calling V_- ground):

Inputs: The *pnp* input structure allows swings of 0.3 volt below ground; if that is exceeded by either input, weird things happen at the output (it may go negative, for instance).

Output: Q_{13} pulls the output down and can sink plenty of current, but it goes only to within a diode drop of ground. Outputs below that are provided by the 50μA current sink, which means you can't drive a load that sources more than 50μA and get closer than a diode drop above ground. Even for "nice" loads (an open circuit, say), the current source won't bring the output lower than a saturation voltage (0.1V) above ground. If you want the output to go clear down to ground, the load should sink a small current to ground; it could be a resistor to ground, for instance. Recent additions to the family of *pnp*-input single-supply op-amps include the precision LT1006 and LT1014 (single and quad, respectively) and the micropower OP-20 and OP-90 (both single), and LP324 (quad).

We will illustrate the use of these op-amps with some circuits, after mentioning the other kind of op-amp that lends itself well to single-supply operation.

2. The LM10 (bipolar) or CA5130/5160 (MOSFET) complementary-output-stage op-amps. When saturated, they look like a small resistance from the output to the supply (V_+ or V_-). Thus the output can swing all the way to either supply. In addition, the inputs can go 0.5 volt below V_-. Unlike the LM10, the CA5130

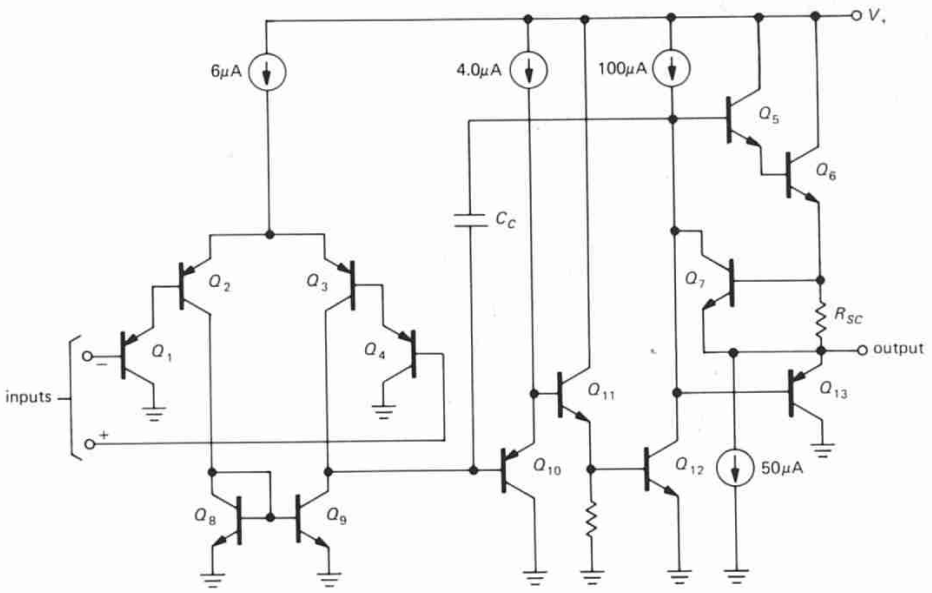


Figure 4.54. Schematic of the popular 324 and 358 op-amps. (National Semiconductor Corp.)

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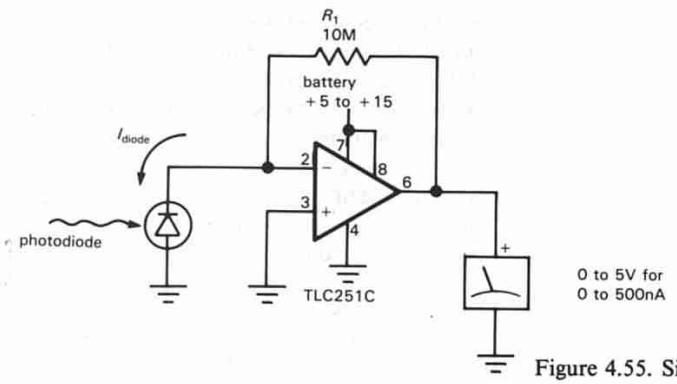


Figure 4.55. Single-supply photometer.

and 5160 are limited to 16 volts (max) total supply voltage and ±8 volts differential input voltage. Although most CMOS op-amps permit rail-to-rail output swings, watch out for some varieties that can only swing all the way to one rail; also note that the input common-mode range of most CMOS op-amps, like ordinary bipolar op-amps, includes at most one power-supply rail. For example, the popular TLC27*xx* series from TI has input and output capability to the negative rail only, whereas the LMC660 from National, along with the Intersil ICL76*xx* series and RCA's CMOS op-amps, has output swing to both rails (but input common-mode range only to the negative rail). Unique among op-amps are the CMOS ICL7612 and ALD1701/2, which claim both input and output operation to *both* rails.

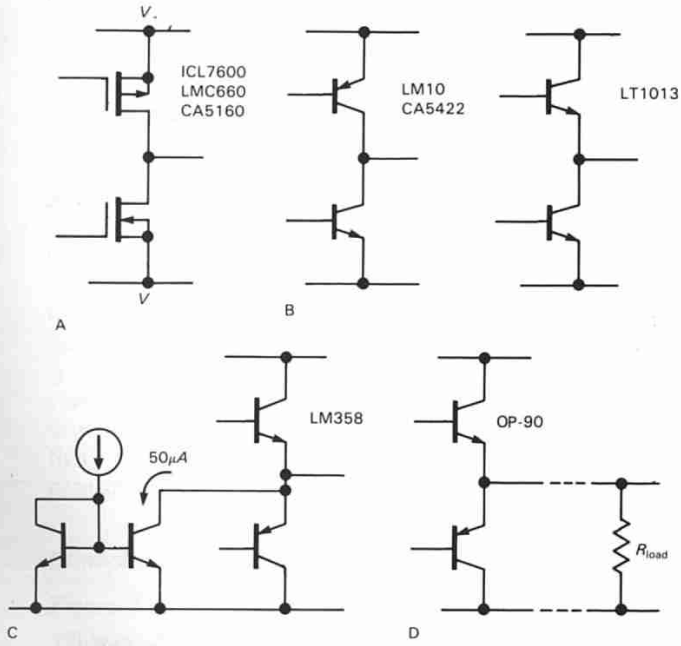


Figure 4.56. Output stages used in single-supply op-amps.

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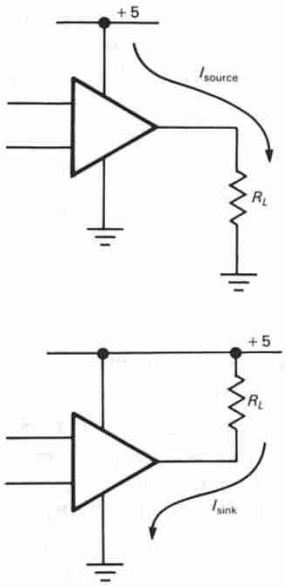


Figure 4.57. Connecting a load to a single-supply op-amp. All single-supply types (A–D) can swing all the way to ground while sourcing current. Some types (A and B) can swing nearly to ground while sinking moderate or substantial currents; type C can sink up to 50μA, and type D requires a load resistor returned to ground to operate near ground.

□ *Example: single-supply photometer*

Figure 4.55 shows a typical example of a circuit for which single-supply operation is convenient. We discussed a similar circuit earlier under the heading of current-to-voltage converters. Since a photocell circuit might well be used in a portable light-measuring instrument, and since the output is known to be positive only, this is a good candidate for a battery-operated single-supply circuit. R_1 sets the full- scale output at 5 volts for an input photocurrent of 0.5μA. No offset voltage trim is needed in this circuit, since the worst-case untrimmed offset of 10mV corresponds to a negligible 0.2% of full-scale meter indication. The TLC251 is an inexpensive micropower (10μA supply current) CMOS op-amp with input and output swings to the negative rail. Its low input current (1pA, typ, at room temperature) makes it good for low-current applications like this. Note that if you choose a bipolar op-amp for an application like this, better performance at low light levels results if the photodiode is connected as in the circuit shown in Figure 4.94J.

When using "single-supply" op-amps, watch out for misleading statements about output swing to the negative rail (ground). There are really four different kinds of output stages, all of which "swing down to ground," but they have very different properties (Fig. 4.56): (a) Op-amps with complementary MOS output transistors give true rail-to-rail swing; such a stage is

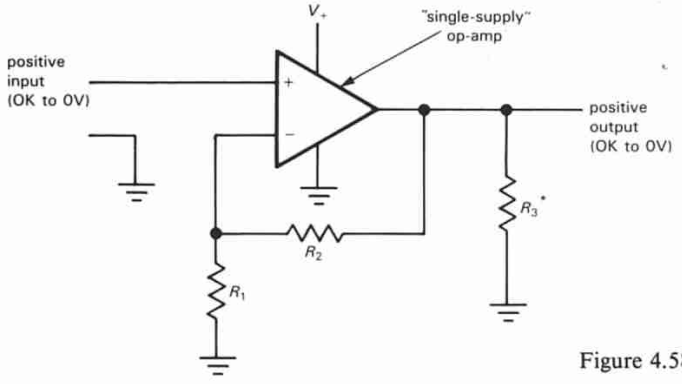


Figure 4.58. Single-supply dc amplifier.

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capable of pulling its output to ground, *even when sinking moderate current*. Some examples are the ICL76*xx*, the LMC660, and CA5160. (b) Op-amps with an *npn* common-emitter transistor to ground behave similarly, i.e., they can pull their output to ground even while sinking current. Examples are the LM10, CA5422, and LT1013/14. Both kinds of output stages can, of course, handle an open circuit or a load that *sinks* current to ground. (c) Some op-amps, notably the 358 and 324, use a *pnp* follower to ground (which can only pull down to within a diode drop of ground), in parallel with an *npn* current sink (with compliance clear to ground). In the 358, the internal current sink is set at 50μA. Such a circuit can swing clear down to ground as long as it doesn't have to sink more than 50μA from the load. If the load sources more current, the output only works to within a diode drop of ground. As before, this kind of output circuit is happy *sourcing* current to a load that is returned to ground (as in the photometer example earlier). (d) Finally, some single-supply op-amps (e.g., the OP-90) use a *pnp* follower to ground, without the parallel current sink. Such an output stage can swing to ground only if the load helps out by sinking current, i.e., by being returned to ground. If you want to use such an op-amp with a load that sources current, you have to add an external resistor to ground (Fig. 4.57).

A note of caution: Don't make the mistake of assuming that you can make any op-amp's output work down to the negative rail simply by providing an external current sink. In most cases the circuitry driving the output stage does not permit that. Look for explicit permission in the data sheet!

Example: single-supply dc amplifier

Figure 4.58 shows a typical single-supply noninverting amplifier to amplify an input signal of known positive polarity. The input, output, and positive supply are all referenced to ground, which is the negative supply voltage for the op-amp. The output "pulldown" resistor may be needed with what we called type-1 amplifiers to ensure output swing all the way to ground; the feedback network or the load itself could perform this function. An important point: Remember that the output cannot go negative; thus you cannot use this amplifier with, say, ac-coupled audio signals.

Single-supply op-amps are indispensable in battery-operated equipment. We'll have more to say about this in Chapter 14.

COMPARATORS AND SCHMITT TRIGGER

It is quite common to want to know which of two signals is larger, or to know when a given signal exceeds a predetermined value. For instance, the usual method of generating triangle waves is to supply positive or negative currents into a capacitor, reversing the polarity of the current when the amplitude reaches a preset peak value. Another example is a digital voltmeter. In order to convert a voltage to a number, the unknown voltage is applied to one input of a comparator, with a linear ramp (capacitor + current source) applied to the other. A digital counter counts cycles of an oscillator while the ramp is less than the unknown voltage and displays the result when equality of amplitudes is reached. The resultant count is proportional to the input voltage. This is called single-slope integration; in most sophisticated instruments a dual-slope integration is used (see Section 9.21).

4.23 Comparators

The simplest form of comparator is a high-gain differential amplifier, made either with transistors or with an op-amp (Fig. 4.59). The op-amp goes into positive or

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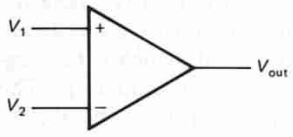


Figure 4.59

negative saturation according to the difference of the input voltages. Because the voltage gain typically exceeds 100,000, the inputs will have to be equal to within a fraction of a millivolt in order for the output not to be saturated. Although an ordinary op-amp can be used as a comparator (and frequently is), there are special integrated circuits intended for use as comparators. Some examples are the LM306, LM311, LM393, NE527, and TLC372. These chips are designed for very fast response and aren't even in the same league as op-amps. For example, the high-speed NE521 slews at several thousand volts per microsecond. With comparators, the term "slew rate" isn't usually used; you talk instead about "propagation delay versus input overdrive."

Comparators generally have more flexible output circuits than op-amps. Whereas an ordinary op-amp uses a push-pull output stage to swing between the supply voltages (±13V, say, for a 411 running from ±15V supplies), a comparator chip usually has an "open-collector" output with grounded emitter. By supplying an external "pullup" resistor (that's accepted terminology, believe it or not) connected to a voltage of your choice, you can have an output swing from +5 volts to ground, say. You will see later that logic circuits have well-defined voltages they like to operate between; the preceding example would be ideal for driving a TTL circuit, a popular type of digital logic. Figure 4.60 shows the circuit. The output switches from +5 volts to ground when the input signal goes negative. This use of a comparator is really an example of analog-to-digital conversion.

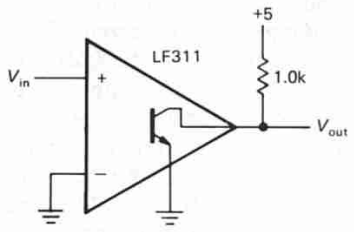


Figure 4.60

This is the first example we have presented of an *open-collector* output; this is a common configuration in logic circuits, as you will see throughout Chapters 8–11. If you like, you can think of the external pullup resistor as completing the comparator's internal circuit by providing a collector load resistor for an *npn* output transistor. Since the output transistor operates as a saturated switch, the resistor value is not at all critical, with values typically between a few hundred ohms and a few thousand ohms; small values yield improved switching speed and noise immunity at the expense of increased power dissipation. Incidentally, in spite of their superficial resemblance to op-amps, comparators are never used with negative feedback because they would not be stable (see Sections 4.32–4.34). However, some *positive* feedback is often used, as you will see in the next section.

Comments on comparators

Some points to remember: (a) Because there is no negative feedback, golden rule I is not obeyed. The inputs are not at the same voltage. (b) The absence of negative feedback means that the (differential) input impedance isn't bootstrapped to the high values characteristic of op-amp circuits. As a result, the input signal sees a changing load and changing (small) input current as the comparator switches; if the driving impedance is too high,

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strange things may happen. (c) Some comparators permit only limited differential input swings, as little as ±5 volts in some cases. Check the specs! See Table 9.3 and the discussion in Section 9.07 for the properties of some popular comparators.

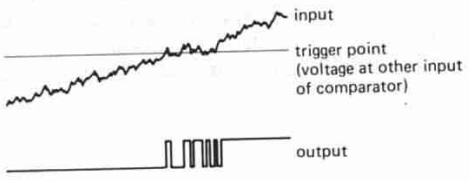


Figure 4.61

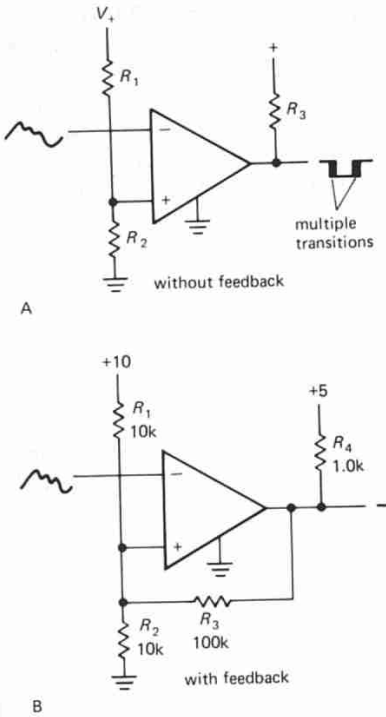


Figure 4.62

4.24 Schmitt trigger

The simple comparator circuit in Figure 4.60 has two disadvantages. For a very slowly varying input, the output swing can be rather slow. Worse still, if the input is noisy, the output may make several transitions as the input passes through the trigger point (Fig. 4.61). Both these problems can be remedied by the use of *positive* feedback (Fig. 4.62). The effect of R_3 is to make the circuit have two thresholds, depending on the output state. In the example shown, the threshold when the output is at ground (input high) is 4.76 volts, whereas the threshold with the output at +5 volts is 5.0 volts. A noisy input is less likely to produce multiple triggering (Fig. 4.63). Furthermore, the positive feedback ensures a rapid output transition, regardless of the speed of the input waveform. (A small "speedup" capacitor of 10–100pF is often connected across R_3 to enhance switching speed still further.) This configuration is known as a Schmitt trigger. (If an op-amp were used, the pullup would be omitted.)

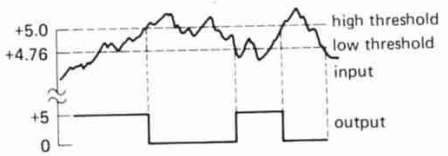


Figure 4.63

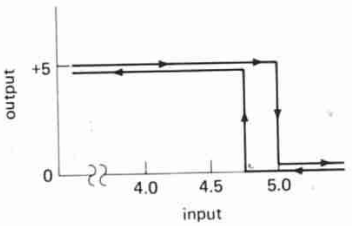


Figure 4.64

The output depends both on the input voltage and on its recent history, an effect called *hysteresis*. This can be illustrated with a diagram of output versus input, as in Figure 4.64. The design procedure

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is easy for Schmitt triggers that have a small amount of hysteresis. Use the circuit of Figure 4.62B. First choose a resistive divider (R_1, R_2) to put the threshold at approximately the right voltage; if you want the threshold near ground, just use a single resistor from noninverting input to ground. Next, choose the (positive) feedback resistor R_3 to produce the required hysteresis, noting that the hysteresis equals the output swing, attenuated by a resistive divider formed by R_3 and $R_1 \| R_2$. Finally, choose an output pullup resistor R_4 small enough to ensure nearly full supply swing, taking account of the loading by R_3. For the case where you want thresholds symmetrical about ground, connect an offsetting resistor of appropriate value from the noninverting input to the negative supply. You may wish to scale all resistor values in order to keep the output current and impedance levels within a reasonable range.

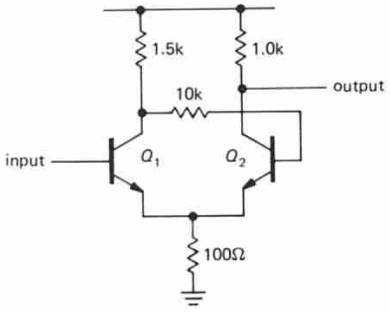


Figure 4.65

Discrete-transistor Schmitt trigger

A Schmitt trigger can also be made simply with transistors (Fig. 4.65). Q_1 and Q_2 share an emitter resistor. It is essential that Q_1's collector resistor be larger than Q_2's. In that way the threshold to turn on Q_1, which is one diode drop above the emitter voltage, rises when Q_1 is turned off, since the emitter current is higher with Q_2 conducting. This produces hysteresis in the trigger threshold, just as in the preceding integrated circuit Schmitt trigger.

EXERCISE 4.10

Design a Schmitt trigger using a 311 comparator (open-collector output) with thresholds at +1.0 volt and +1.5 volts. Use a 1.0k pullup resistor to +5 volts, and assume that the 311 is powered from ±15 volt supplies.

FEEDBACK WITH FINITE-GAIN AMPLIFIERS

We mentioned in Section 4.12 that the finite open-loop gain of an op-amp limits its performance in a feedback circuit. Specifically, the closed-loop gain can never exceed the open-loop gain, and as the open-loop gain approaches the closed-loop gain, the amplifier begins to depart from the ideal behavior we have come to expect. In this section we will quantify these statements so that you will be able to predict the performance of a feedback amplifier constructed with real (less than ideal) components. This is important also for feedback amplifiers constructed entirely with discrete components (transistors), where the open-loop gain is usually much less than with op-amps. In these cases the output impedance, for instance, will not be zero. Nonetheless, with a good understanding of feedback principles you will be able to achieve the performance required in any given circuit.

4.25 Gain equation

Let's begin by considering an amplifier of finite voltage gain, connected with feedback to form a noninverting amplifier (Fig. 4.66). The amplifier has open-loop voltage gain A, and the feedback network subtracts a fraction B of the output voltage from the input. (Later we will generalize

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things so that inputs and outputs can be currents or voltages.) The input to the gain block is then $V_{in} - BV_{out}$. But the output is just the input times A:

$$A(V_{in} - BV_{out}) = V_{out}$$

In other words,

$$V_{out} = \frac{A}{1 + AB} V_{in}$$

and the closed-loop voltage gain, V_{out}/V_{in}, is just

$$G = \frac{A}{1 + AB}$$

Some terminology: The standard designations for these quantities are as follows: G = closed-loop gain, A = open-loop gain, AB = loop gain, $1 + AB$ = return difference, or desensitivity. The feedback network is sometimes called the beta network (no relation to transistor beta, h_{fe}).

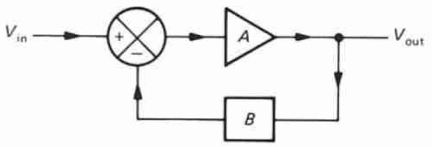


Figure 4.66

4.26 Effects of feedback on amplifier circuits

Let's look at the important effects of feedback. The most significant are predictability of gain (and reduction of distortion), changed input impedance, and changed output impedance.

Predictability of gain

The voltage gain is $A/(1 + AB)$. In the limit of infinite open-loop gain A, $G = 1/B$. We saw this result in the noninverting amplifier configuration, where a voltage divider on the output provided the signal to the inverting input (Fig. 4.69). The closed-loop voltage gain was just the inverse of the division ratio of the voltage divider. For finite gain A, feedback still acts to reduce the effects of variations of A (with frequency, temperature, amplitude, etc.). For instance, suppose A depends on frequency as in Figure 4.67. This

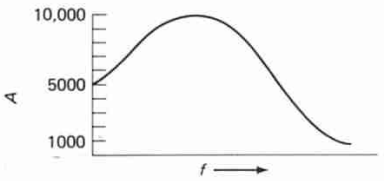


Figure 4.67

will surely satisfy anyone's definition of a poor amplifier (the gain varies over a factor of 10 with frequency). Now imagine we introduce feedback, with $B = 0.1$ (a simple voltage divider will do). The closed-loop voltage gain now varies from 1000/[1 +(1000×0.1)], or 9.90, to 10,000/[1 + (10,000×0.1)], or 9.99, a variation of just 1% over the same range of frequency! To put it in audio terms, the original amplifier is flat to ±10dB, whereas the feedback amplifier is flat to ±0.04dB. We can now recover the original gain of 1000 with nearly this linearity by just cascading three such stages. It was for just this reason (namely, the need for extremely flat telephone repeater amplifiers) that negative feedback was invented. As the inventor, Harold Black, described it in his first open publication on the invention (*Electrical Engineering*, 53:114, 1934), "by building an amplifier whose gain is made deliberately, say 40 decibels higher than necessary (10,000-fold excess on energy basis) and then feeding the output back to the input in such a way as to throw away the excess gain, it has been found possible to effect extraordinary improvement in constancy of amplification and freedom from nonlinearity."

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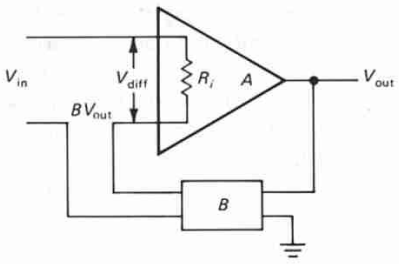


Figure 4.68

It is easy to show, by taking the partial derivative of G with respect to A ($\partial G/\partial A$), that relative variations in the open-loop gain are reduced by the desensitivity:

$$\frac{\Delta G}{G} = \frac{1}{1+AB}\frac{\Delta A}{A}$$

Thus, for good performance the loop gain AB should be much larger than 1. That's equivalent to saying that the open-loop gain should be much larger than the closed-loop gain.

A very important consequence of this is that nonlinearities, which are simply gain variations that depend on signal level, are reduced in exactly the same way.

Input impedance

Feedback can be arranged to subtract a voltage or a current from the input (these are sometimes called *series feedback* and *shunt feedback*, respectively). The noninverting op-amp configuration, for instance, subtracts a sample of the output voltage from the differential voltage appearing at the input, whereas in the inverting configuration a current is subtracted from the input. The effects on input impedance are opposite in the two cases: Voltage feedback multiplies the open-loop input impedance by $1 + AB$, whereas current feedback reduces it by the same factor. In the limit of infinite loop gain the input impedance (at the amplifier's input terminal) goes to infinity or zero, respectively. This is easy to understand, since voltage feedback tends to subtract signal from the input, resulting in a smaller change (by the factor AB) across the amplifier's input resistance; it's a form of bootstrapping. Current feedback reduces the input signal by bucking it with an equal current.

Let's see explicitly how the effective input impedance is changed by feedback. We will illustrate the case of voltage feedback only, since the derivations are similar for the two cases. We begin with an op-amp model with (finite) input resistance as shown in Figure 4.68. An input V_{in} is reduced by BV_{out}, putting a voltage $V_{diff} = V_{in} - BV_{out}$ across the inputs of the amplifier. The input current is therefore

$$I_{in} = \frac{V_{in} - BV_{out}}{R_i} = \frac{V_{in}\left(1 - B\frac{A}{1+AB}\right)}{R_i} = \frac{V_{in}}{(1+AB)R_i}$$

giving an effective input resistance

$$R_i' = V_{in}/I_{in} = (1+AB)R_i$$

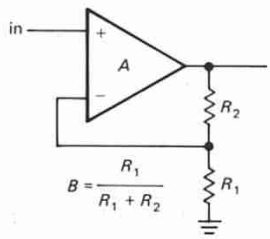


Figure 4.69

The classic op-amp noninverting amplifier is exactly this feedback configuration, as shown in Figure 4.69. In this circuit, $B = R_1/(R_1 + R_2)$, giving the usual voltage-gain expression $G_v = 1 + R_2/R_1$ and an infinite input impedance for the ideal case of infinite open-loop voltage gain

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A. For finite loop gain, the equations as previously derived apply.

The op-amp *inverting* amplifier circuit is different from the noninverting circuit and has to be analyzed separately. It's best to think of it as a combination of an input resistor driving a shunt feedback stage (Fig. 4.70). The shunt stage alone has its input at the "summing junction" (the inverting input of the amplifier), where the currents from feedback and input signals are combined (this amplifier connection is really a "transresistance" configuration; it converts a current input to a voltage output). Feedback reduces the impedance looking into the summing junction, R_2, by a factor of $1 + A$ (see if you can prove this). In cases of very high loop gain (e.g, an op-amp) the input impedance is reduced to a fraction of an ohm, a good characteristic for a current-input amplifier. Some good examples are the photometer amplifier in Section 4.22 and the logarithmic converter in Section 4.14.

The classic op-amp inverting amplifier connection is a combination of a shunt feedback transresistance amplifier and a series input resistor, as in the figure. As a result, the input impedance equals the sum of R_1 and the impedance looking into the summing junction. For high loop gain, R_{in} approximately equals R_1.

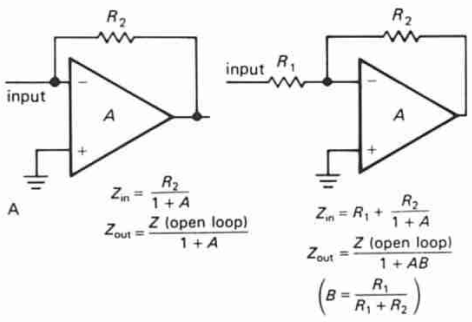


Figure 4.70. Input and output impedances for (A) transresistance amplifier and (B) inverting amplifier.

It is a straightforward exercise to derive an expression for the closed-loop voltage gain of the inverting amplifier with finite loop gain. The answer is

$$G = -A(1 - B)/(1 + AB)$$

where B is defined as before, $B = R_1/(R_1 + R_2)$. In the limit of large open-loop gain A, $G = -1/B + 1$ (i.e., $G = -R_2/R_1$).

EXERCISE 4.11

Derive the foregoing expressions for input impedance and gain of the inverting amplifier.

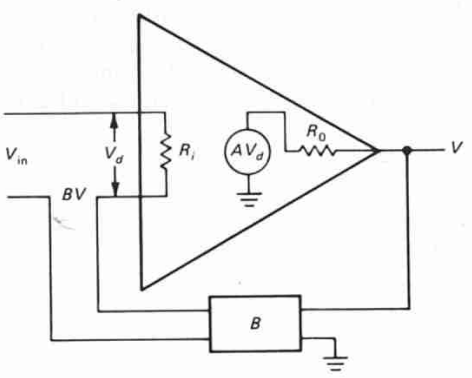


Figure 4.71

Output impedance

Again, feedback can extract a sample of the output voltage or the output current. In the first case the open-loop output impedance will be reduced by the factor $1 + AB$, whereas in the second case it will be increased by the same factor. We will illustrate this effect for the case of voltage sampling. We begin with the model shown in Figure 4.71. This time we have shown the output impedance explicitly. The calculation is simplified by a trick: Short the input, and apply a voltage V to the output; by calculating the output current I, we get the output impedance $R_0' = V/I$. Voltage V at the output

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puts a voltage $-BV$ across the amplifier's input, producing a voltage $-ABV$ in the amplifier's internal generator. The output current is therefore

$$I = \frac{V-(-ABV)}{R_0} = \frac{V(1+AB)}{R_0}$$

giving an effective output impedance

$$R_0' = V/I = R_0/(1+AB)$$

If feedback is connected instead to sample the output current, the expression becomes

$$R_0' = R_0(1+AB)$$

It is possible to have multiple feedback paths, sampling both voltage and current. In the general case the output impedance is given by Blackman's impedance relation

$$R_0' = R_0\frac{1+(AB)_{SC}}{1+(AB)_{OC}}$$

where $(AB)_{SC}$ is the loop gain with the output shorted to ground and $(AB)_{OC}$ is the loop gain with no load attached. Thus, feedback can be used to generate a desired output impedance. This equation reduces to the previous results for the usual situation in which feedback is derived from either the output voltage or the output current.

□ *Loading by the feedback network*

In feedback computations, you usually assume that the beta network doesn't load the amplifier's output. If it does, that must be taken into account in computing the open-loop gain. Likewise, if the connection of the beta network at the amplifier's input affects the open-loop gain (feedback removed, but network still connected), you must use the modified open-loop gain. Finally, the preceding expressions assume that the beta network is unidirectional, i.e., it does not couple signal from the input to the output.

□ 4.27 Two examples of transistor amplifiers with feedback

Figure 4.72 shows a transistor amplifier with negative feedback.

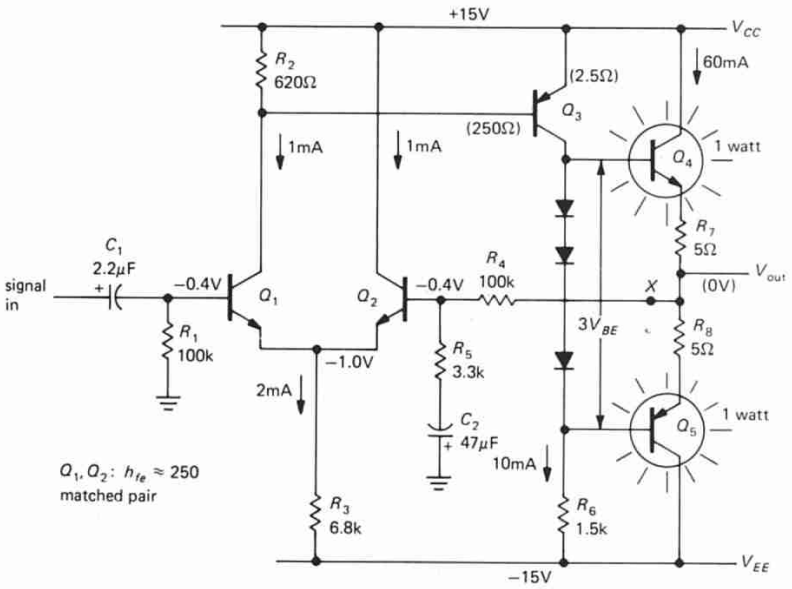


Figure 4.72. Transistor power amplifier with negative feedback.

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□ ***Circuit description***

It may look complicated, but it is extremely straightforward in design and is relatively easy to analyze. Q_1 and Q_2 form a differential pair, with common-emitter amplifier Q_3 amplifying its output. R_6 is Q_3's collector load resistor, and push-pull pair Q_4 and Q_5 form the output emitter follower. The output voltage is sampled by the feedback network consisting of voltage divider R_4 and R_5, with C_2 included to reduce the gain to unity at dc for stable biasing. R_3 sets the quiescent current in the differential pair, and since overall feedback guarantees that the quiescent output voltage is at ground, Q_3's quiescent current is easily seen to be 10mA (V_{EE} across R_6, approximately). As we have discussed earlier (Section 2.15), the diodes bias the push-pull pair into conduction, leaving one diode drop across the series pair R_7 and R_8, i.e., 60mA quiescent current. That's class AB operation, good for minimizing crossover distortion, at the cost of 1 watt standby dissipation in each output transistor.

From the point of view of our earlier circuits, the only unusual feature is Q_1's quiescent collector voltage, one diode drop below V_{CC}. That is where it must sit in order to hold Q_3 in conduction, and the feedback path ensures that it will. (For instance, if Q_1 were to pull its collector closer to ground, Q_3 would conduct heavily, raising the output voltage, which in turn would force Q_2 to conduct more heavily, reducing Q_1's collector current and hence restoring the status quo.) R_2 was chosen to give a diode drop at Q_1's quiescent current in order to keep the collector currents in the differential pair approximately equal at the quiescent point. In this transistor circuit the input bias current is not negligible (4μA), resulting in a 0.4 volt drop across the 100k input resistors. In transistor amplifier circuits like this, in which the input currents are considerably larger than in op-amps, it is particularly important to make sure that the dc resistances seen from the inputs are equal, as shown (a Darlington input stage would probably be better here).

□ ***Analysis***

Let's analyze this circuit in detail, determining the gain, input and output impedances, and distortion. To illustrate the utility of feedback, we will find these parameters for both the open-loop and closed-loop situations (recognizing that biasing would be hopeless in the open-loop case). To get a feeling for the linearizing effect of the feedback, the gain will be calculated at +10 volts and −10 volts output, as well as the quiescent point (zero volts).

□ *Open loop.* Input impedance: We cut the feedback at point X and ground the right side of R_4. The input signal sees 100k in parallel with the impedance looking into the base. The latter is h_{fe} times twice the intrinsic emitter resistance plus the impedance seen at Q_2's emitter due to the feedback network at Q_2's base. For $h_{fe} \approx 250$, $Z_{\text{in}} \approx 250\times[(2\times25)+(3.3\text{k}/250)]$; i.e., $Z_{\text{in}} \approx 16\text{k}$.

Output impedance: Since the impedance looking back into Q_3's collector is high, the output transistors are driven by a 1.5k source (R_6). The output impedance is about 15 ohms ($h_{fe} \approx 100$) plus the 5 ohm emitter resistance, or 20 ohms. The intrinsic emitter resistance of 0.4 ohm is negligible.

Gain: The differential input stage sees a load of R_2 paralleled by Q_3's base resistance. Since Q_3 is running 10mA quiescent current, its intrinsic emitter resistance is 2.5 ohms, giving a base impedance of about 250 ohms (again, $h_{fe} \approx 100$). The differential pair thus has a gain of

$$\frac{250\|620}{2\times25\Omega} \quad \text{or} \quad 3.5$$

The second stage, Q_3, has a voltage gain of 1.5k/2.5ohms, or 600. The overall voltage

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gain at the quiescent point is 3.5 × 600, or 2100. Since Q_3's gain depends on its collector current, there is substantial change of gain with signal swing, i.e., nonlinearity. The gain is tabulated in the following section for three values of output voltage.

□ *Closed loop.* Input impedance: This circuit uses series feedback, so the input impedance is raised by (1 + loop gain). The feedback network is a voltage divider with $B = 1/30$ at signal frequencies, so the loop gain AB is 70. The input impedance is therefore 70 × 16k, still paralleled by the 100k bias resistor, i.e., about 92k. The bias resistor now dominates the input impedance.

Output impedance: Since the output *voltage* is sampled, the output impedance is reduced by (1 + loop gain). The output impedance is therefore 0.3 ohm. Note that this is a small-signal impedance and does not mean that a 1 ohm load could be driven to nearly full swing, for instance. The 5 ohm emitter resistors in the output stage limit the large signal swing. For instance, a 4 ohm load could be driven only to 10 volts pp, approximately.

Gain: The gain is $A/(1+AB)$. At the quiescent point, that equals 30.84, using the exact value for B. In order to illustrate the gain stability achieved with negative feedback, the overall voltage gain of the circuit with and without feedback is tabulated at three values of output level at the end of this paragraph. It should be obvious that negative feedback has brought about considerable improvement in the amplifier's characteristics, although in fairness it should be pointed out that the amplifier could have been designed for better open-loop performance, e.g., by using a current source for Q_3's collector load and degenerating its emitter, by using a current source for the differential-pair emitter circuit, etc. Even so, feedback would still make a large improvement.

	Open loop			*Closed loop*		
V_{out}	−10	0	+10	−10	0	+10
Z_{in}	16k	16k	16k	92k	92k	92k
Z_{out}	20Ω	20Ω	20Ω	0.3Ω	0.3Ω	0.3Ω
Gain	1360	2100	2400	30.60	30.84	30.90

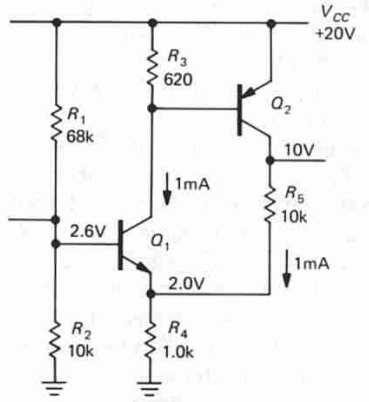


Figure 4.73

□ ***Series feedback pair***

Figure 4.73 shows another transistor amplifier with feedback. Thinking of Q_1 as an amplifier of its base-emitter voltage drop (thinking in the Ebers-Moll sense), the feedback samples the output voltage and subtracts a fraction of it from the input signal. This circuit is a bit tricky because Q_2's collector resistor doubles as the feedback network. Applying the techniques we used earlier, you should be able to show that G(open loop) ≈ 200, loop gain ≈ 20, Z_{out}(open loop) ≈10k, Z_{out}(closed loop) ≈ 500 ohms, and G(closed loop) ≈ 9.5.

SOME TYPICAL OP-AMP CIRCUITS

4.28 General-purpose lab amplifier

Figure 4.74 shows a dc-coupled "decade amplifier" with settable gain, bandwidth, and wide-range dc output offset. IC_1 is a FET-input op-amp with noninverting gain from unity (0dB) to ×100 (40dB) in

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accurately calibrated 10dB steps; a vernier is provided for variable gain. IC_2 is an inverting amplifier; it allows offsetting the output over a range of ±10 volts, accurately calibrated via R_{14}, by injecting current into the summing junction. $C_2 - C_4$ set the high-frequency rolloff, since it is often a nuisance to have excessive bandwidth (and noise). IC_5 is a power booster for driving low-impedance loads or cables; it can provide ±150mA output current.

Some interesting details: A 10MΩ input resistor is small enough, since the bias current of the 411 is 25pA (0.3mV error with open input). R_2, in combination with D_1 and D_2, limits the input voltage at the op-amp to the range V_- to $V_+ + 0.7$. D_3 is used to generate a clamp voltage at $V_- + 0.7$, since the input common mode range extends only to V_- (exceeding V_- causes the output to reverse phase). With the protection components shown, the input can go to ±150 volts without damage.

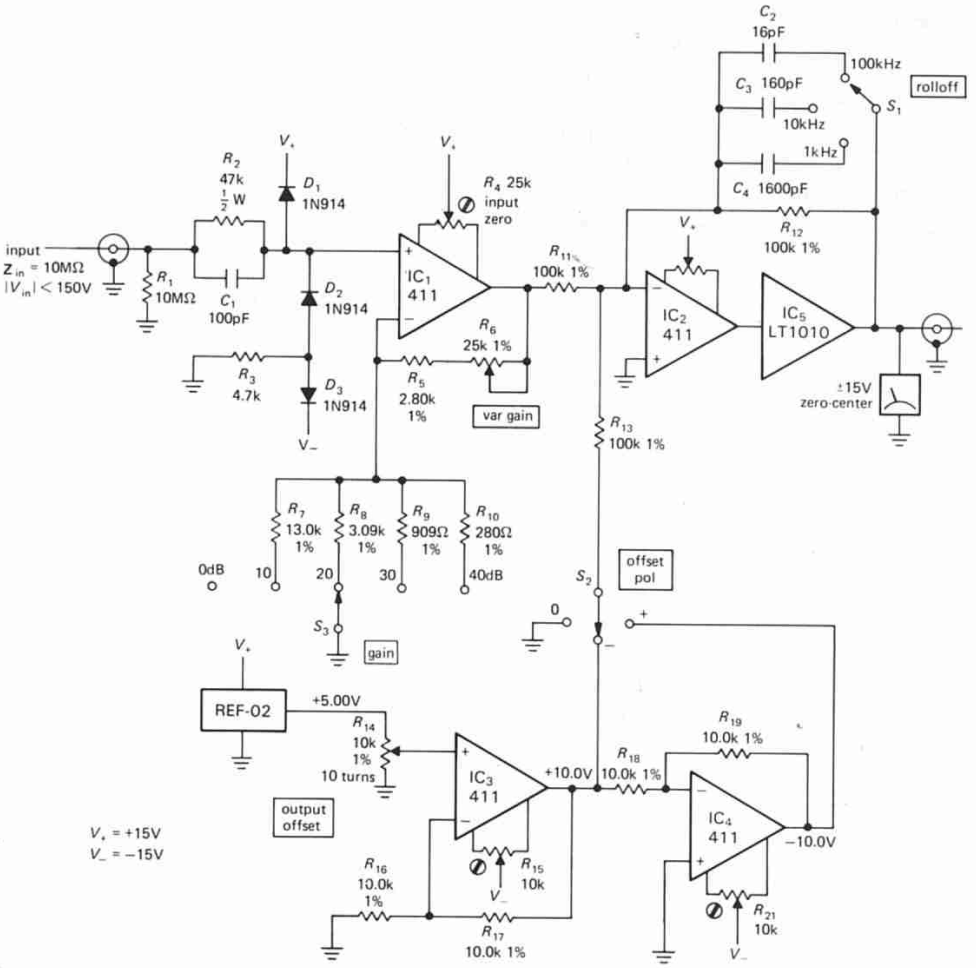


Figure 4.74. Laboratory dc amplifier with output offset.

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EXERCISE 4.12

Check that the gain is as advertised. How does the variable offset circuitry work?

4.29 Voltage-controlled oscillator

Figure 4.75 shows a clever circuit, borrowed from the application notes of several manufacturers. IC_1 is an integrator, rigged up so that the capacitor current (V_{in}/200k) changes sign, but not magnitude, when Q_1 conducts. IC_2 is connected as a Schmitt trigger, with thresholds at one-third and two-thirds of V_+. Q_1 is an n-channel MOSFET, used here as a switch; it is simpler to use than bipolar transistors in this sort of application, but an alternative circuit using npn transistors is shown in addition. In either case, the bottom side of R_4 is pulled to ground when the output is HIGH and open-circuited when the output is LOW.

An unusual feature of this circuit is its operation from a single positive supply. The 3160 (internally compensated version of the 3130) has FETs as output transistors, guaranteeing a full swing between V_+ and ground at the output; this ensures that the thresholds of the Schmitt don't drift, as they would with an op-amp of conventional output-stage design, with its ill-defined limits of output swing. In this case this means that the frequency and amplitude of the triangle wave will be stable. Note that the frequency depends on the ratio V_{in}/V_+; this means that if V_{in} is generated from V_+ by a resistive divider (made from some sort of resistive transducer, say), the output frequency won't vary with V_+, only with changes in resistance.

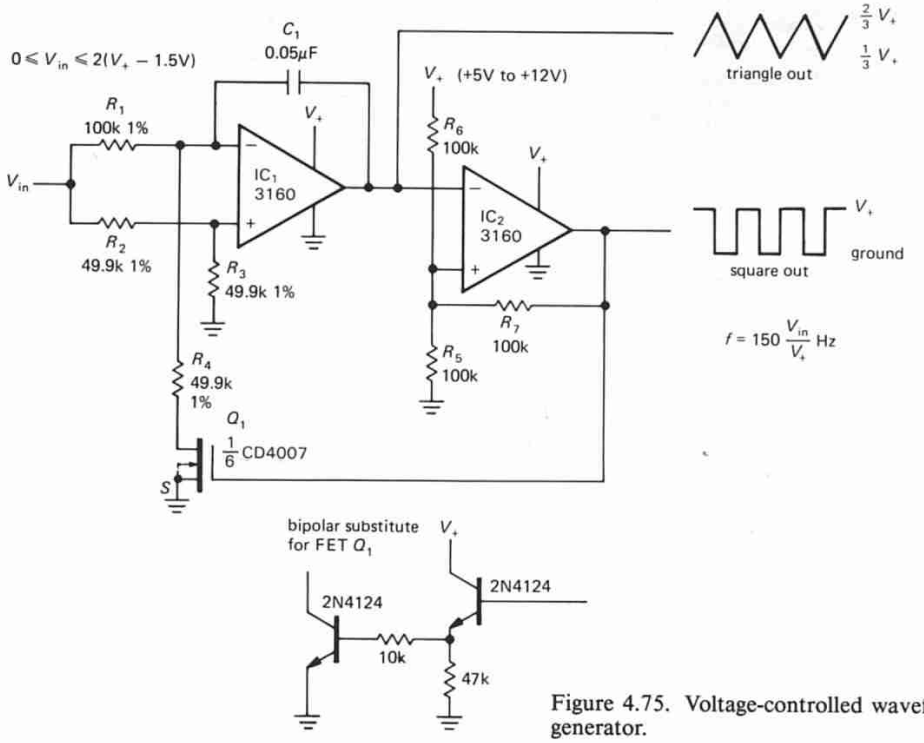


Figure 4.75. Voltage-controlled waveform generator.

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EXERCISE 4.13
Show that the output frequency is given by $f(\text{Hz}) = 150V_{in}/V_+$. Along the way, verify that the Schmitt thresholds and integrator currents are as advertised.

□ 4.30 JFET linear switch with R_{ON} compensation

In Chapter 3 we considered MOSFET linear switches in some detail. It is also possible to use JFETs as linear switches. However, you have to be more careful about gate signals so that gate conduction doesn't occur. Figure 4.76 shows a typical arrangement. The gate is held well below ground to keep the JFET pinched off. This means that if the input signals go negative, the gate must be held at least V_P below the most negative input swing. To bring the FET into conduction, the control input is brought more positive than the most positive input excursion. The diode is then reverse-biased, and the gate rides at source voltage via the 1M resistor.

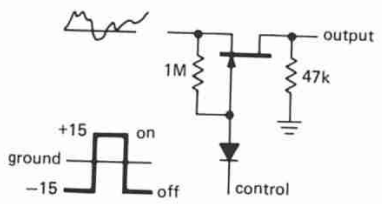


Figure 4.76

The awkwardness of this circuit probably accounts for much of the popularity of MOSFETs in linear switch applications. However, it is possible to devise an elegant JFET linear switch circuit if you use an op-amp, since you can tie the JFET source to the virtual ground at the summing junction of an inverting amplifier. Then you simply bring the gate to ground potential to turn the JFET on. This arrangement has the added advantage of providing a method of canceling precisely the errors caused by finite R_{ON} and its nonlinearity. Figure 4.77 shows the circuit.

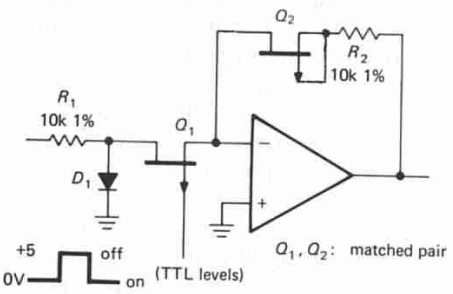


Figure 4.77. JFET-switched amplifier with R_{ON} cancellation.

There are two noteworthy features of this circuit: (a) When Q_1 is ON (gate grounded), the overall circuit is an inverter with identical impedances in the input and feedback circuits. That results in the cancellation of any effects of finite or nonlinear ON resistance, assuming the FETs are matched in R_{ON}. (b) Because of the low pinch-off voltage of JFETs, the circuit will work well with a control signal of zero to +5 volts, which is what you get with standard digital logic circuits (see Chapters 8 and 9). The inverting configuration, with Q_1's source connected to a virtual ground (the summing junction), simplifies circuit operation, since there are no signal swings on Q_1's source in the ON state; D_1 prevents FET turn-on for positive input swings when Q_1 is OFF, and it has no effect when the switch is closed.

There are p-channel JFETs with low pinch-off voltages available in useful configurations at low prices. For example, the IH5009–IH5024 family includes devices with four input FETs and one cancellation FET in a single DIP package, with R_{ON} of 100 ohms and a price less than two dollars. Add an op-amp and a few resistors and you've got a 4-input multiplexer. Note that the same R_{ON} cancellation trick can be used with MOSFET switches.

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□ 4.31 TTL zero-crossing detector

The circuit shown in Figure 4.78 generates an output square wave for use with TTL logic (zero to +5V range) from an input wave of any amplitude up to 100 volts. R_1, combined with D_1 and D_2, limits the input swing to −0.6 volt to +5.6 volts, approximately. Resistive divider R_2R_3 is necessary to limit negative swing to less than 0.3 volt, the limit for a 393 comparator. R_5 and R_6 provide hysteresis, with R_4 setting the trigger points symmetrically about ground. The input impedance is nearly constant, because of the large R_1 value relative to the other resistors in the input attenuator. A 393 is used because its inputs can go all the way to ground, making single-supply operation simple.

EXERCISE 4.14

Verify that the trigger points are at ±25mV at the input signal.

□ 4.32 Load-current-sensing circuit

The circuit shown in Figure 4.79 provides a voltage output proportional to load current, for use with a current regulator, metering circuit, or whatever. The voltage across the 4-terminal resistor R_S goes from zero to 0.1 volt, with probable common-mode offset due to the effects of resistance in the ground lead (note that the power supply is grounded at the output). For that reason the op-amp is wired as a differential amplifier, with gain of 100. Voltage offset is trimmed externally with R_8, since the LT1013 doesn't have internal trimming circuitry (the single LT1006 does, however). A zener reference with a few percent stability is adequate for trimming, since the trimming is itself a small correction (you hope!). The venerable 358 could have been chosen because both inputs and output also go all the way to ground. V_+ could be unregulated, since the power-supply rejection of the op-amp is more than adequate, 100dB (typ) in this case.

FEEDBACK AMPLIFIER FREQUENCY COMPENSATION

If you look at a graph of open-loop voltage gain versus frequency for several op-amps,

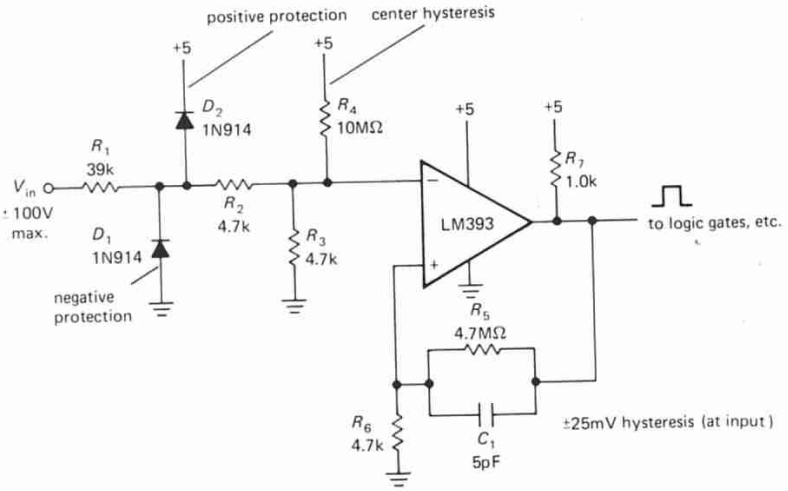


Figure 4.78. Zero-crossing level detector with input protection.

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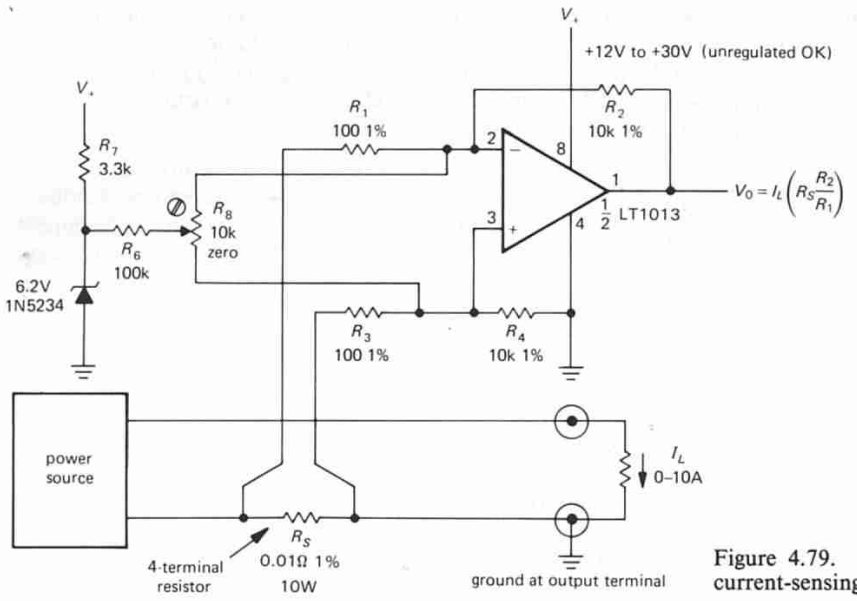


Figure 4.79. High-power current-sensing amplifier.

you'll see something like the curves in Figure 4.80. From a superficial look at such a *Bode plot* (a log-log plot of gain and phase versus frequency) you might conclude that the 741 is an inferior op-amp, since its open-loop gain drops off so rapidly with increasing frequency. In fact, that rolloff is built into the op-amp intentionally and is recognizable as the same −6db/octave curve characteristic of an *RC* low-pass filter. The 748, by comparison, is identical with the 741 except that it is *uncompensated* (as is the 739). Op-amps are generally available in internally compensated varieties and uncompensated varieties; let's take a look at this business of frequency compensation.

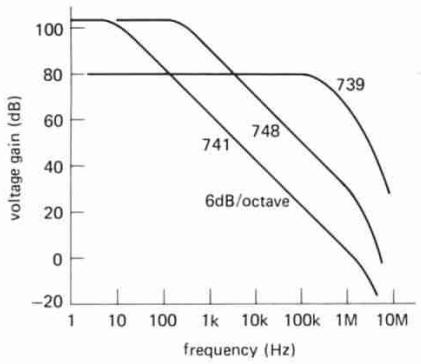


Figure 4.80

4.33 Gain and phase shift versus frequency

An op-amp (or, in general, any multistage amplifier) will begin to roll off at some frequency because of the low-pass filters formed by signals of finite source impedance driving capacitive loads within the amplifier stages. For instance, it is common to have an input stage consisting of a differential amplifier, perhaps with current mirror load (see the LM358 schematic in Fig. 4.54), driving a common-emitter second stage. For now, imagine that the capacitor labeled C_C in that circuit is removed. The high output impedance of the input stage, in combination with

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junction capacitance C_{ie} and feedback capacitance C_{cb} (Miller effect, see Sections 2.19 and 13.04) of the following stage, forms a low-pass filter whose 3dB point might fall somewhere in the range of 100Hz to 10kHz.

The decreasing reactance of the capacitor with increasing frequency gives rise to the characteristic 6db/octave rolloff: At sufficiently high frequencies (which may be below 1kHz), the capacitive loading dominates the collector load impedance, resulting in a voltage gain $G_V = g_m X_C$, i.e., the gain drops off as $1/f$. It also produces a 90° lagging phase shift at the output relative to the input signal. (You can think of this as the tail of an RC low-pass filter characteristic, where R represents the equivalent source impedance driving the capacitive load. However, it is not necessary to have any actual resistors in the circuit.)

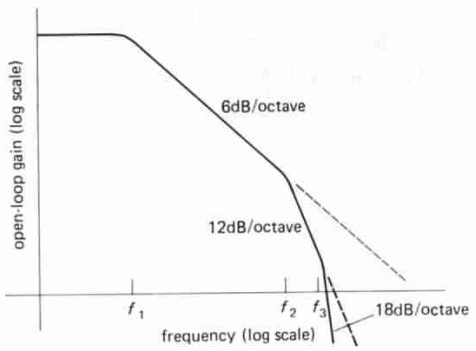


Figure 4.81

In a multistage amplifier there will be additional rolloffs at higher frequencies, caused by low-pass filter characteristics in the other amplifier stages, and the overall open-loop gain will look something like that shown in Figure 4.81. The open-loop gain begins dropping at 6dB/octave at some low frequency f_1, due to capacitive loading of the first-stage output. It continues dropping off with that slope until an internal RC of another stage rears its ugly head at frequency f_2, beyond which the rolloff goes at 12dB/octave, and so on.

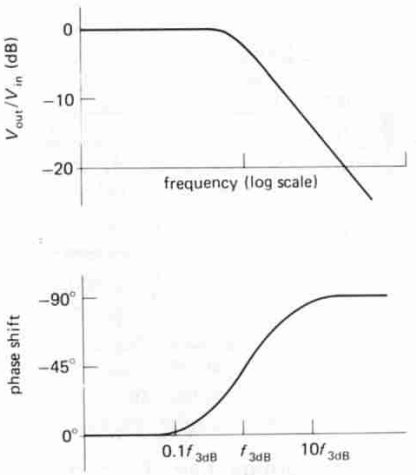


Figure 4.82. Bode plot: gain and phase versus frequency.

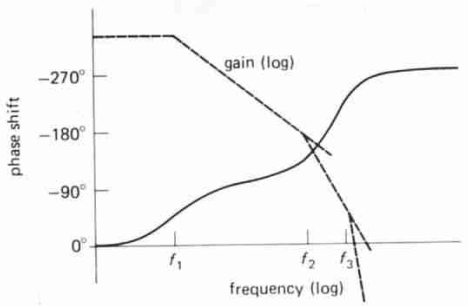


Figure 4.83

What is the significance of all this? Remember that an RC low-pass filter has a phase shift that looks as shown in Figure 4.82. Each low-pass filter within the amplifier has a similar phase-shift characteristic, so the overall phase shift of the hypothetical amplifier will be as shown in Figure 4.83.

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Now here's the problem: If you were to connect this amplifier as an op-amp follower, for instance, it would oscillate. That's because the open-loop phase shift reaches 180° at some frequency at which the gain is still greater than 1 (negative feedback becomes positive feedback at that frequency). That's all you need to generate an oscillation, since any signal whatsoever at that frequency builds up each time around the feedback loop, just like a public address system with the gain turned up too far.

Stability criterion

The criterion for stability against oscillation for a feedback amplifier is that its open-loop phase shift must be less than 180° at the frequency at which the loop gain is unity. This criterion is hardest to satisfy when the amplifier is connected as a follower, since the loop gain then equals the open-loop gain, the highest it can be. Internally compensated op-amps are designed to satisfy the stability criterion even when connected as followers; thus they are stable when connected for any closed-loop gain with a simple resistive feedback network. As we hinted earlier, this is accomplished by deliberately modifying an existing internal rolloff in order to put the 3dB point at some low frequency, typically 1Hz to 20Hz. Let's see how that works.

4.34 Amplifier compensation methods

Dominant-pole compensation

The goal is to keep the open-loop phase shift much less than 180° at all frequencies for which the loop gain is greater than 1. Assuming that the op-amp may be used as a follower, the words "loop gain" in the last sentence can be replaced by "open-loop gain." The easiest way to do this is to add enough capacitance at the point in the circuit that produces the initial 6dB/octave rolloff, so that the open-loop gain drops to unity at about the 3dB frequency of the next "natural" *RC* filter. In this way the open-loop phase shift is held at a constant 90° over most of the passband, increasing toward 180° only as the gain approaches unity. Figure 4.84

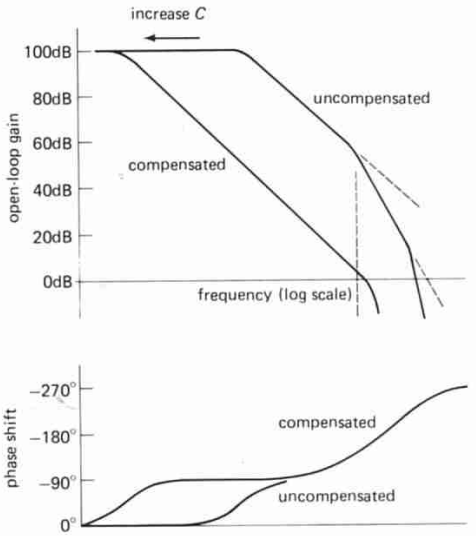


Figure 4.84

shows the idea. Without compensation the open-loop gain drops toward 1, first at 6dB/octave, then at 12dB/octave, etc., resulting in phase shifts of 180° or more before the gain has reached 1. By moving the first rolloff down in frequency (forming a "dominant pole"), the rolloff is controlled so that the phase shift begins to rise above 90° only as the open-loop gain approaches unity. Thus, by sacrificing open-loop gain, you buy stability. Since the natural rolloff of lowest frequency is usually caused by Miller effect in the stage driven by the input differential amplifier, the usual method of dominant-pole compensation consists simply of adding additional feedback capacitance around the second-stage transistor, so that the combined voltage gain of

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the two stages is $g_m X_C$ or $g_m/2\pi f C_{\text{comp}}$ over the compensated region of the amplifier's frequency response (Fig. 4.85). In practice, Darlington-connected transistors would probably be used for both stages.

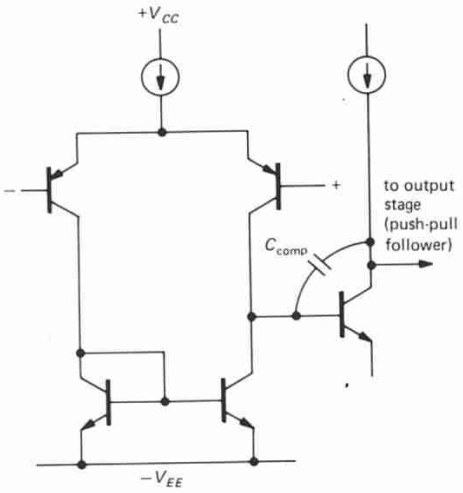


Figure 4.85. Classic op-amp input stage with compensation.

By putting the dominant-pole unity-gain crossing at the 3dB point of the next rolloff, you get a phase margin of about 45° in the worst case (follower), since a single RC filter has a 45° lagging phase shift at its 3dB frequency, i.e., the phase margin equals 180° − (90° + 45°), with the 90° coming from the dominant pole.

An additional advantage of using a Miller-effect pole for compensation is that the compensation is inherently insensitive to changes in voltage gain with temperature, or manufacturing spread of gain: Higher gain causes the feedback capacitance to look larger, moving the pole downward in frequency in exactly the right way to keep the unity-gain crossing frequency unchanged. In fact, the actual 3dB frequency of the compensation pole is quite irrelevant; what matters is the point at which it intersects the unity-gain axis (Fig. 4.86).

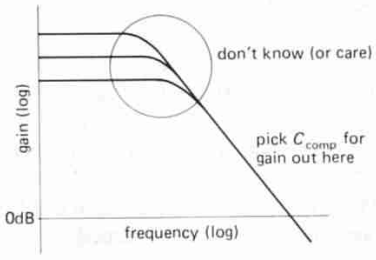


Figure 4.86

Uncompensated op-amps

If an op-amp is used in a circuit with closed-loop gain greater than 1 (i.e., not a follower), it is not necessary to put the pole (the term for the "corner frequency" of a low-pass filter) at such a low frequency, since the stability criterion is relaxed because of the lower loop gain. Figure 4.87 shows the situation graphically.

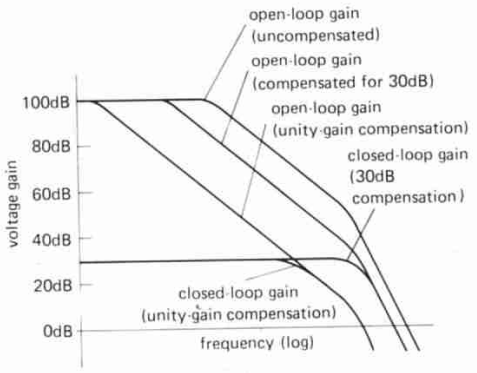


Figure 4.87

For a closed-loop gain of 30dB, the loop gain (which is the ratio of the open-loop gain to the closed-loop gain) is less than for a follower, so the dominant pole can be placed at a higher frequency. It is chosen

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so that the open-loop gain reaches 30dB (rather than 0dB) at the frequency of the next natural pole of the op-amp. As the graph shows, this means that the open-loop gain is higher over most of the frequency range, and the resultant amplifier will work at higher frequencies. Some op-amps are available in uncompensated versions [e.g., the 748 is an uncompensated 741; the same is true for the 308 (312), 3130 (3160), HA5102 (HA5112), etc.], with recommended external capacitance values for a selection of minimum closed-loop gains. They are worth using if you need the added bandwidth and your circuit operates at high gain. An alternative is to use "decompensated" (a better word might be "undercompensated") op-amps, such as the 357, which are internally compensated for closed-loop gains greater than some minimum ($A_V > 5$ in the case of the 357).

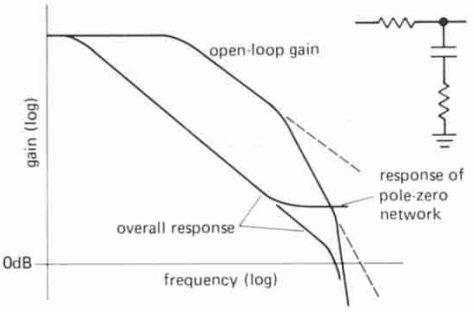


Figure 4.88

□ *Pole-zero compensation*

It is possible to do a bit better than with dominant-pole compensation by using a compensation network that begins dropping (6dB/octave, a "pole") at some low frequency, then flattens out again (it has a "zero") at the frequency of the second natural pole of the op-amp. In this way the amplifier's second pole is "canceled," giving a smooth 6dB/octave rolloff up to the amplifier's third pole. Figure 4.88 shows a frequency response plot. In practice, the zero is chosen to cancel the amplifier's second pole; then the position of the first pole is adjusted so that the overall response reaches unity gain at the frequency of the amplifier's third pole. A good set of data sheets will often give suggested component values (an R and a C) for pole-zero compensation, as well as the usual capacitor values for dominant-pole compensation.

As you will see in Section 13.06, moving the dominant pole downward in frequency actually causes the second pole of the amplifier to move upward somewhat in frequency, an effect known as "pole splitting." The frequency of the canceling zero will be chosen accordingly.

□ 4.35 Frequency response of the feedback network

In all of the discussion thus far we have assumed that the feedback network has a flat frequency response; this is usually the case, with the standard resistive voltage divider as a feedback network. However, there are occasions when some sort of equalization amplifier is desired (integrators and differentiators are in this category) or when the frequency response of the feedback network is modified to improve amplifier stability. In such cases it is important to remember that the Bode plot of loop gain versus frequency is what matters, rather than the curve of open-loop gain. To make a long story short, the curve of ideal closed-loop gain versus frequency should intersect the curve of open-loop gain, with a difference in slopes of 6dB/octave. As an example, it is common practice to put a small capacitor (a few picofarads) across the feedback resistor in the usual inverting or noninverting amplifier. Figure 4.89 shows the circuit and Bode plot.

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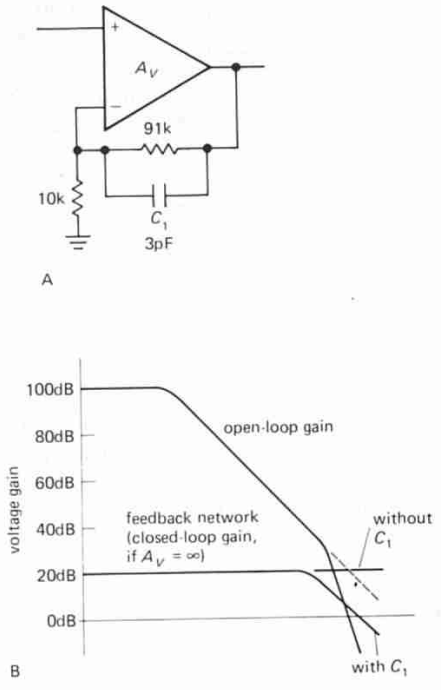


Figure 4.89

The amplifier would have been close to instability with a flat feedback network, since the loop gain would have been dropping at nearly 12dB/octave where the curves meet. The capacitor causes the loop gain to drop at 6dB/octave near the crossing, guaranteeing stability. This sort of consideration is very important when designing differentiators, since an ideal differentiator has a closed-loop gain that rises at 6dB/octave; it is necessary to roll off the differentiator action at some moderate frequency, preferably going over to a 6dB/octave rolloff at high frequencies. Integrators, by comparison, are very friendly in this respect, owing to their 6dB/octave closed-loop rolloff. It takes real talent to make a low-frequency integrator oscillate!

What to do

In summary, you are generally faced with the choice of internally compensated or uncompensated op-amps. It is simplest to use the compensated variety, and that's the usual choice. You might consider the internally compensated LF411 first. If you need greater bandwidth or slew rate, look for a faster compensated op-amp (see Table 4.1 or 7.3 for many choices). If it turns out that nothing is suitable, and the closed-loop gain is greater than unity (as it usually is), you can use an uncompensated op-amp, with an external capacitor as specified by the manufacturer for the gain you are using.

A number of op-amps offer another choice: a "decompensated" version, requiring no external compensation components, but only usable at some minimum gain greater than unity. For example, the popular OP-27 low-noise precision op-amp (unity-gain-compensated) is available as the decompensated OP-37 (minimum gain of 5), offering roughly seven times the speed, and also as the decompensated HA-5147 (minimum gain of 10), with 15 times the speed.

□ Example: 60Hz power source

Uncompensated op-amps also give you the flexibility of overcompensating, a simple solution to the problem of additional phase shifts introduced by other stuff in the feedback loop. Figure 4.90 shows a nice example. This is a low-frequency amplifier designed to generate a 115 volt ac power output from a variable 60Hz low-level sine-wave input (it goes with the 60Hz synthesizer circuit described in Section 8.31). The op-amp, together with R_2 and R_3, forms a $\times 100$ gain block; this is then used as the relatively low "open-loop gain" for overall feedback. The op-amp output drives the push-pull output stage, which in turn drives the transformer primary. Low-frequency feedback is taken from the transformer output via R_{10}, in order to generate low distortion and a stable output voltage under load variations. Because of

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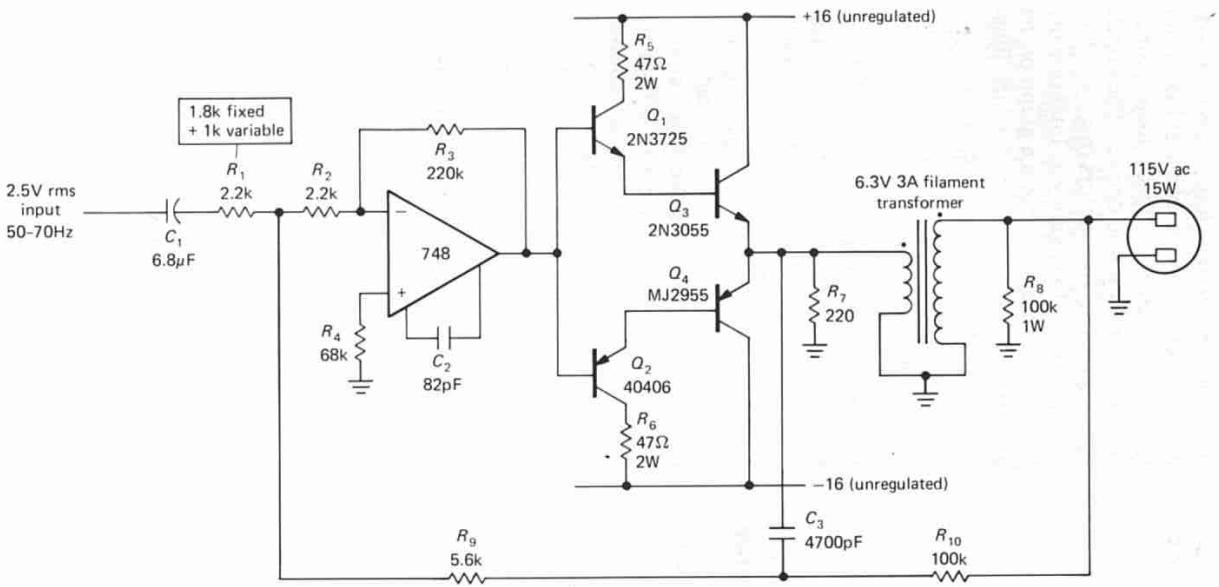


Figure 4.90. Output amplifier for 60Hz power source.

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the unacceptably large phase shifts of such a transformer at high frequencies, the circuit is rigged up so that at higher frequencies the feedback comes from the low-voltage input to the transformer, via C_3. The relative sizes of R_9 and R_{10} are chosen to keep the amount of feedback constant at all frequencies. Even though high-frequency feedback is taken directly from the push-pull output, there are still phase shifts associated with the reactive load (the transformer primary) seen by the transistors. In order to ensure good stability, even with reactive loads at the 115 volt output, the op-amp has been overcompensated with an 82pF capacitor (30pF is the normal value for unity gain compensation). The loss of bandwidth that results is unimportant in a low-frequency application like this.

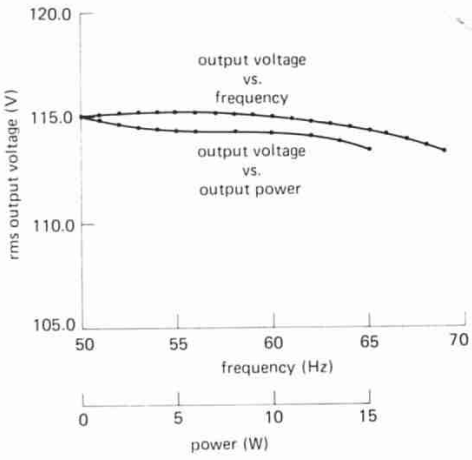


Figure 4.91

An application such as this represents a compromise, since ideally you would like to have plenty of loop gain to stabilize the output voltage against variations in load current. But a large loop gain increases the tendency of the amplifier to oscillate, especially if a reactive load is attached. This is because the reactive load, in combination with the transformer's finite output impedance, causes additional phase shifts within the low-frequency feedback loop. Since this circuit was built to derive a telescope's synchronous driving motors (highly inductive loads), the loop gain was intentionally kept low. Figure 4.91 shows a graph of the ac output voltage versus load, which illustrates good (but not great) regulation.

Motorboating

In ac-coupled feedback amplifiers, stability problems can also crop up at very low frequencies, due to the accumulated *leading* phase shifts caused by several capacitively coupled stages. Each blocking capacitor, in combination with the input resistance due to bias strings and the like, causes a leading phase shift that equals 45° at the low-frequency 3dB point and approaches 90° at lower frequencies. If there is enough loop gain, the system can go into a low-frequency oscillation picturesquely known as "motorboating." With the widespread use of dc-coupled amplifiers, motorboating is almost extinct. However, old-timers can tell you some good stories about it.

SELF-EXPLANATORY CIRCUITS

4.36 Circuit ideas

Some interesting circuit ideas, mostly lifted from manufacturers' data sheets, are shown in Figure 4.94.

4.37 Bad circuits

Figure 4.95 presents a zoo of intentional (mostly) blunders to amuse, amaze, and educate you. There are a few real howlers here this time. These circuits are guaranteed not to work. Figure out why. All op-amps run from ±15 volts unless shown otherwise.

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ADDITIONAL EXERCISES

(1) Design a "sensitive voltmeter" to have $Z_{in} = 1M\Omega$ and full-scale sensitivities of 10mV to 10V in four ranges. Use a 1mA meter movement and an op-amp. Trim voltage offsets if necessary, and calculate what the meter will read with input open, assuming **(a)** $I_B = 25pA$ (typical for a 411) and **(b)** $I_B = 80nA$ (typical for a 741). Use some form of meter protection (e.g., keep its current less than 200% of full scale), and protect the amplifier inputs from voltages outside the supply voltages. What do you conclude about the suitability of the 741 for low-level high-impedance measurements?

(2) Design an audio amplifier, using an OP-27 op-amp (low noise, good for audio), with the following characteristics: gain = 20dB, $Z_{in} = 10k$, $-3dB$ point = 20Hz. Use the noninverting configuration, and roll off the gain at low frequencies in such a way as to reduce the effects of input offset voltage. Use proper design to minimize the effects of input bias current on output offset. Assume that the signal source is capacitively coupled.

(3) Design a unity-gain phase splitter (see Chapter 2) using 411s. Strive for high input impedance and low output impedances. The circuit should be dc-coupled. At roughly what maximum frequency can you obtain full swing (27V pp, with $\pm 15V$ supplies), owing to slew rate limitations?

(4) El Cheapo brand loudspeakers are found to have a treble boost, beginning at 2kHz (+3dB point) and rising 6dB/octave. Design a simple *RC* filter, buffered with AD611 op-amps (another good audio chip) as necessary, to be placed between preamp and amplifier to compensate this rise. Assume that the preamp has $Z_{out} = 50k$ and that the amplifier has $Z_{in} = 10k$, approximately.

(5) A 741 is used as a simple comparator, with one input grounded; i.e., it is a zero-crossing detector. A 1 volt amplitude sine wave is fed into the other input (frequency1kHz). What voltage(s) will the input be when the output passes through zero volts? Assume that the slew rate is $0.5V/\mu s$ and that the op-amp's saturated output is ± 13 volts.

(6) The circuit in Figure 4.92 is an example of a "negative-impedance converter." **(a)** What is its input impedance? **(b)** If the op-amp's output range goes from V_+ to V_-, what range of input voltages will this circuit accommodate without saturation?

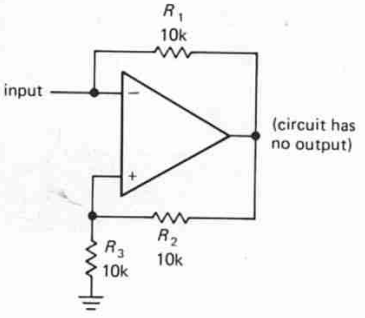


Figure 4.92

(7) Consider the circuit in the preceding problem as the 2-terminal black box (Fig. 4.93). Show how to make a dc amplifier with a gain of -10. Why can't you make a dc amplifier with a gain of $+10$? (Hint: The circuit is susceptible to a latchup condition for a certain range of source resistances. What is that range? Can you think of a remedy?)

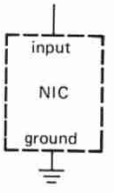
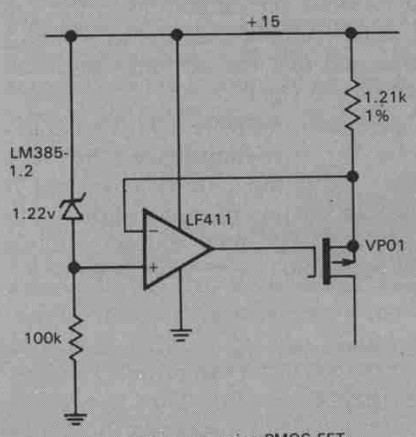


Figure 4.93

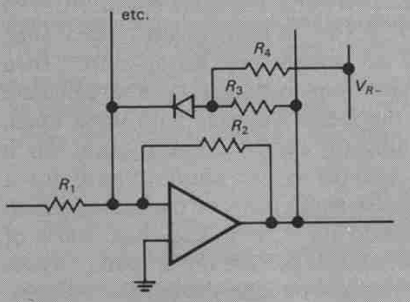
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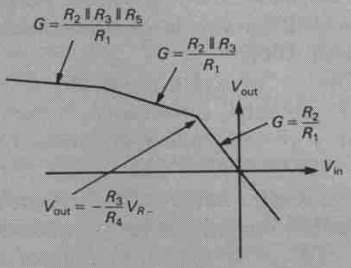
Circuit ideas



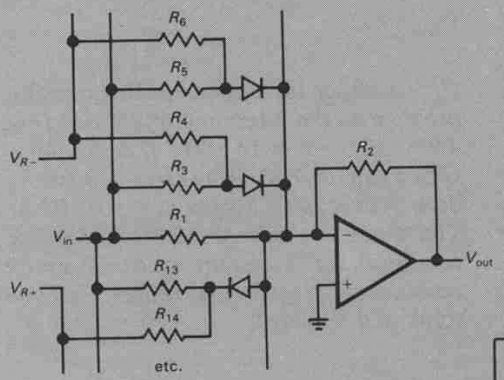
current source using PMOS FET

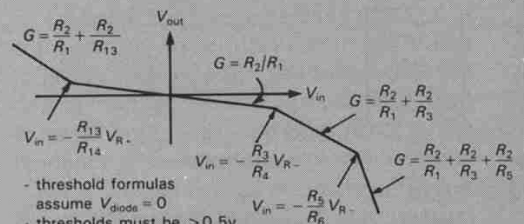
A. precision current source





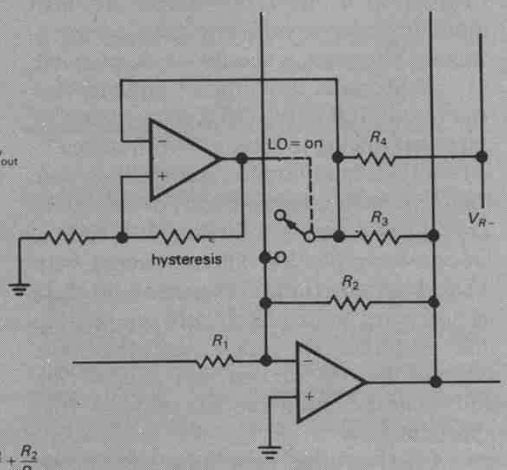
C. as in B, but gain decreases for outputs above threshold





- threshold formulas assume $V_{diode} = 0$
- thresholds must be >0.5v

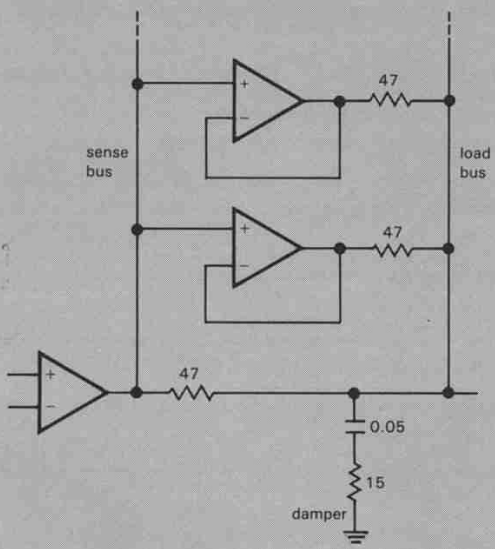
B. inverting piecewise-linear curve amplifier
G increases for inputs above threshold



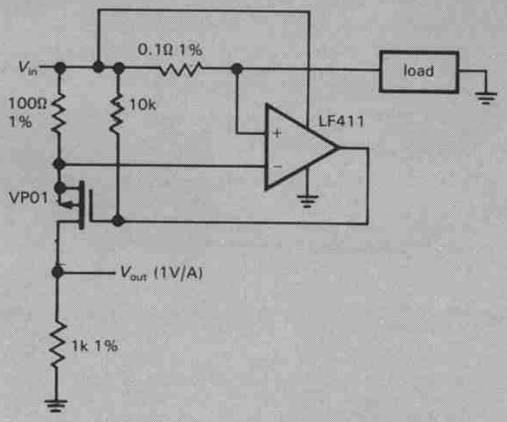
D. as in C, but with comparator and switch, acting as a "perfect" diode ($V_D = 0$)

Figure 4.94

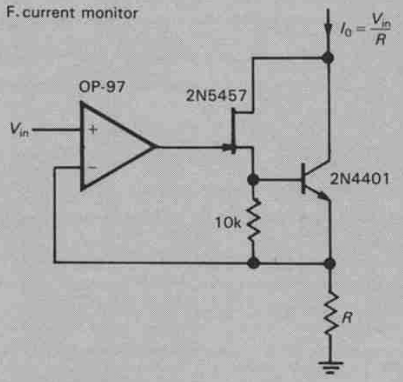
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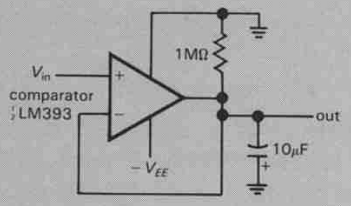
E. higher output current from additional op-amp sections; watch for excess heating



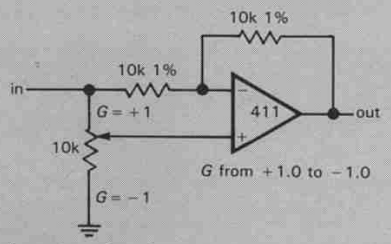
F. current monitor



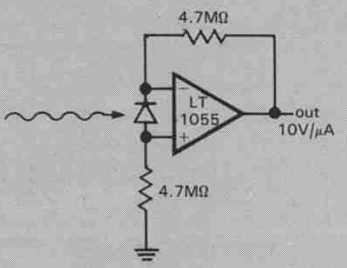
G. precision current sink



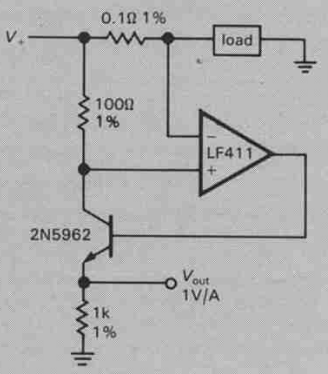
H. negative peak detector



I. continuously variable gain



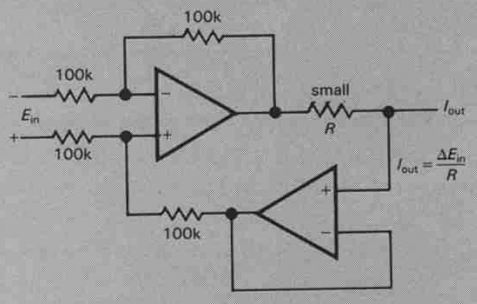
J. photodiode amplifier



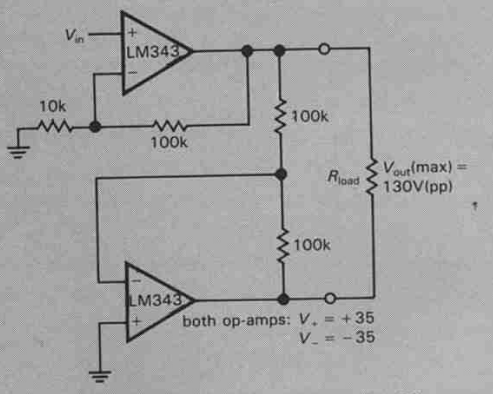
K. current monitor

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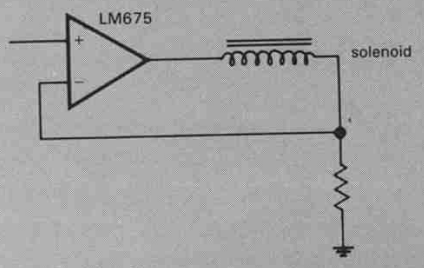
Circuit ideas (*cont.*)



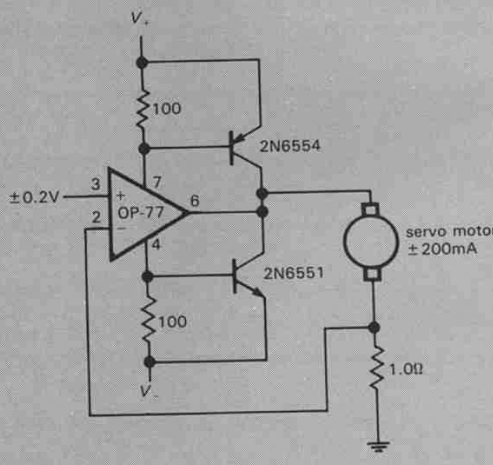
L. precision bipolarity current source



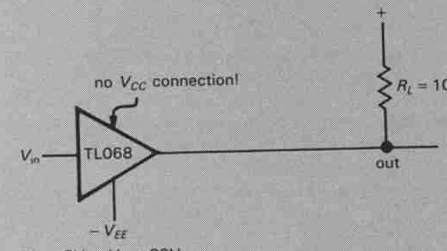
P. high-voltage (bridge) drive to floating load (gain = 22)



M. active solenoid

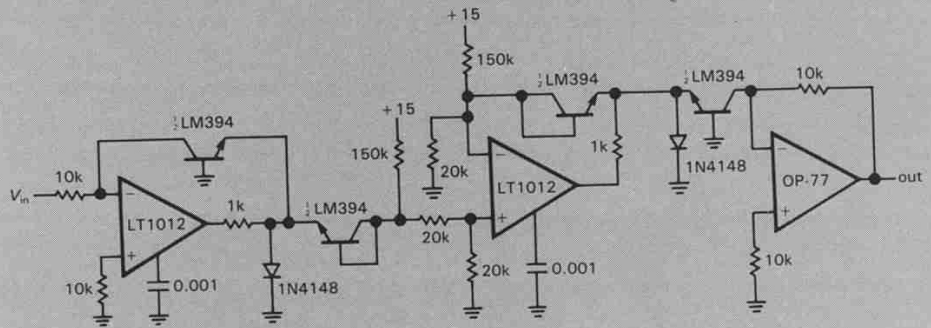


Q. 0.2A servo-motor amplifier



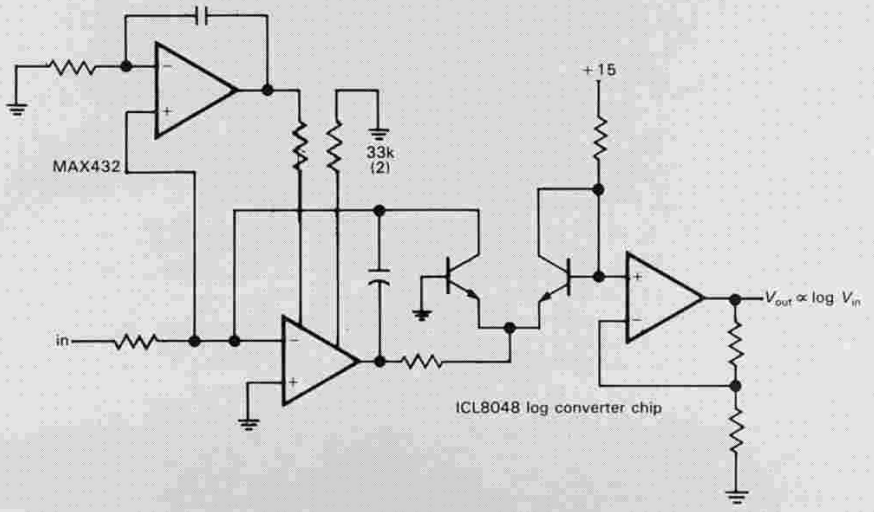
$V_{EE} + 3V < V_{in} < 30V$

N. unusual 3-pin JFET follower

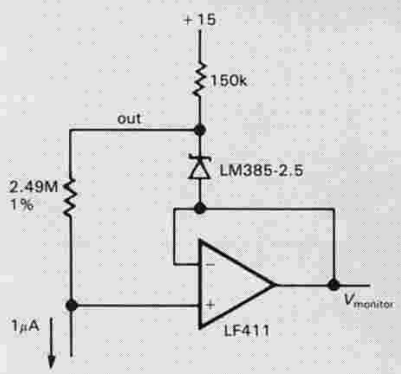


O. temperature-compensated log converter

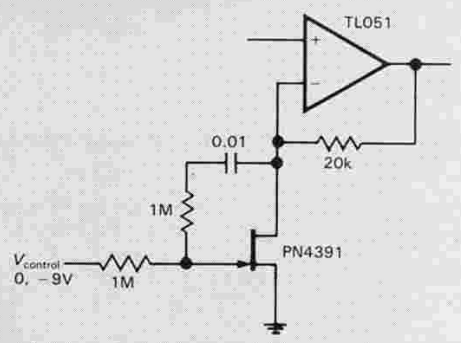
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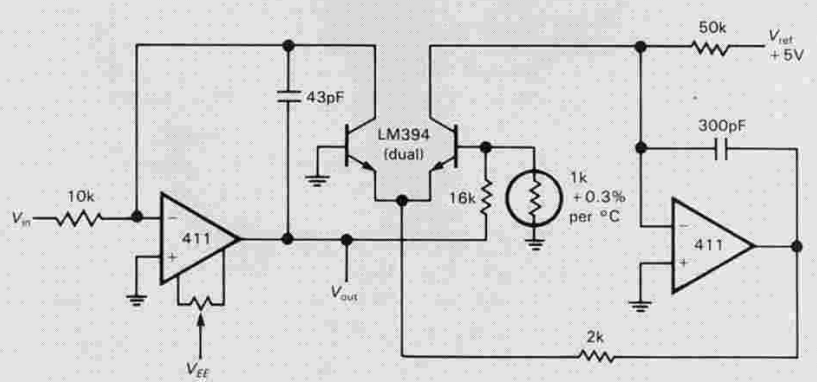
R. log converter with wide input range due to automatic nulling with a chopper amplifier



S. current source

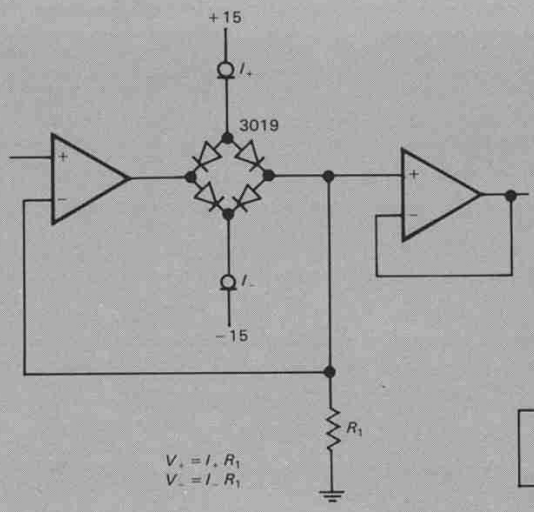


U. low-distortion variable-gain amplifier

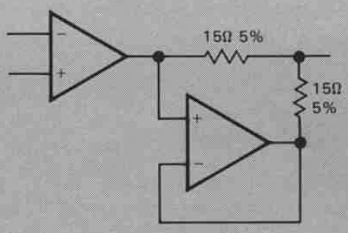


T. fast logarithmic converter

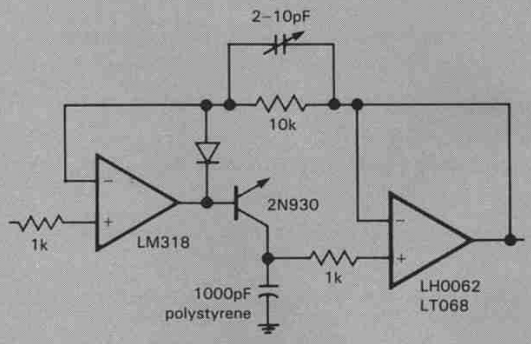
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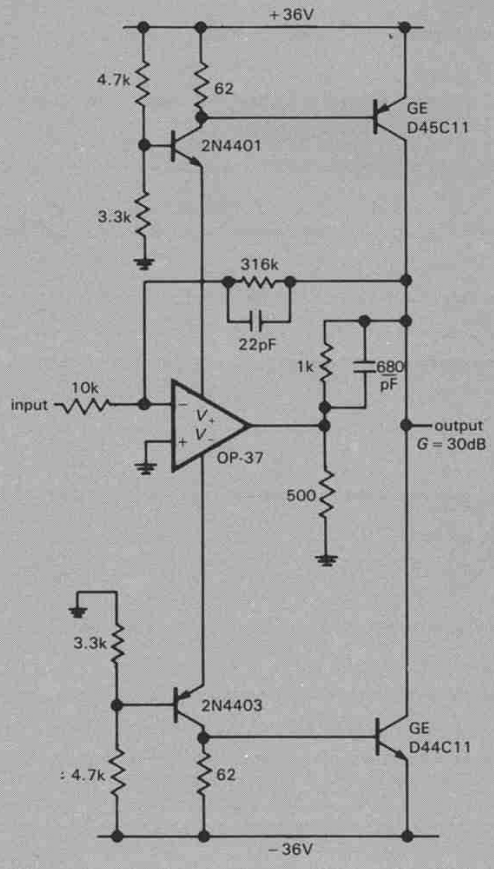
V. precision bipolarity limiter



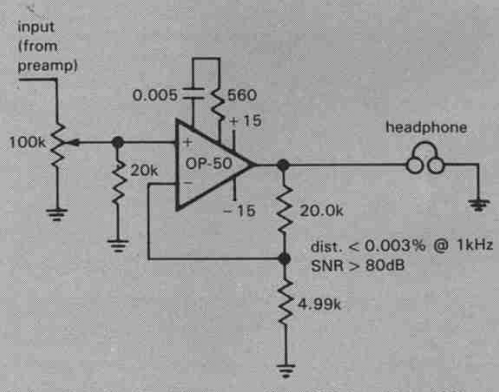
X. obtaining 2× output capability from a dual op-amp



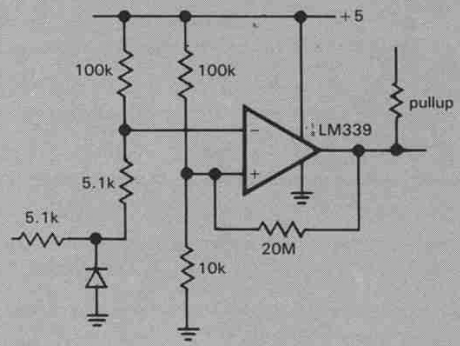
Y. high-speed peak detector



W. low-noise high-voltage op-amp (from PMI App. Note 106)

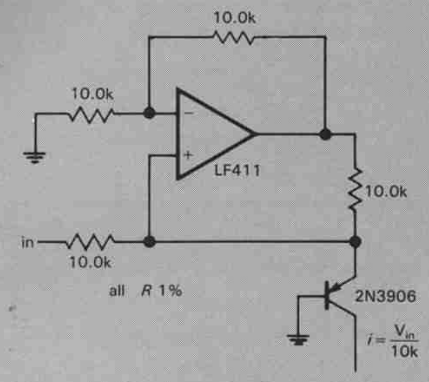


Z. low-distortion headphone amp (from PMI App. Note 106)

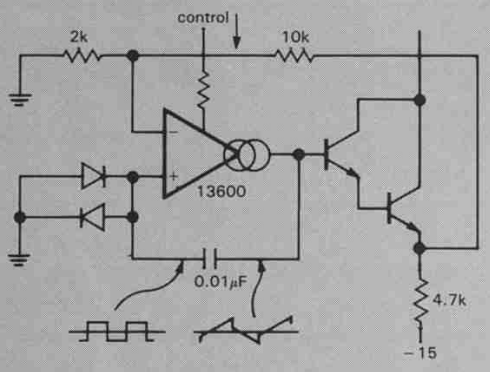


AA. zero-crossing detector, single supply

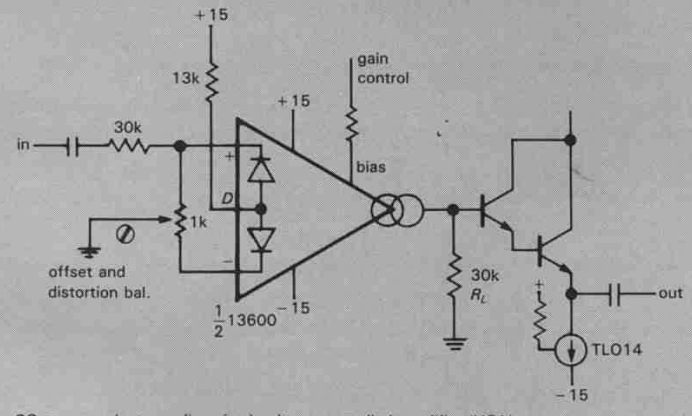
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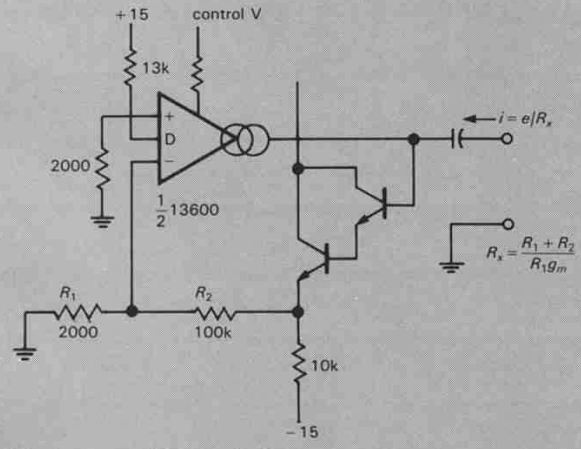
BB. Howland-style current source for transconductance voltage-current control circuits (1μA to 1mA)



EE. voltage-contolled oscillator with transconductance amplifier

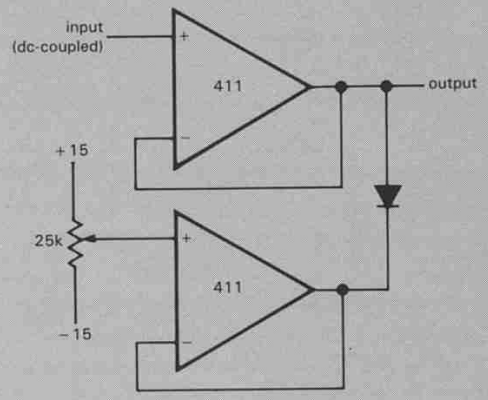


CC. transconductance linearized voltage-controlled amplifier (VCA)

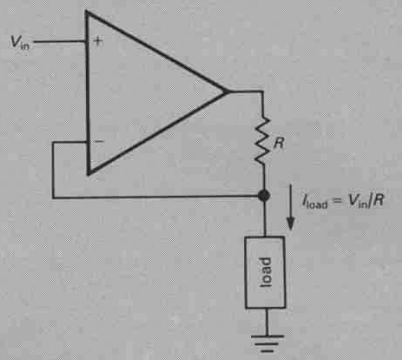


DD. voltage-controlled AC load resistor

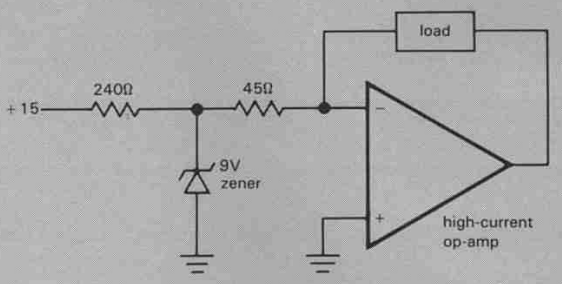
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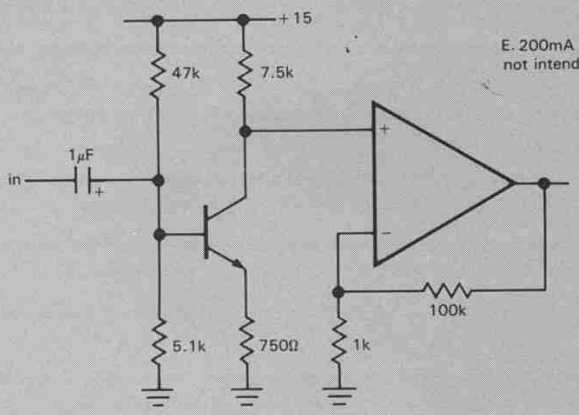
A. adjustable clamp



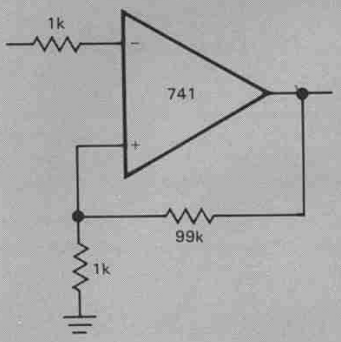
D. current source (voltage-programmed)



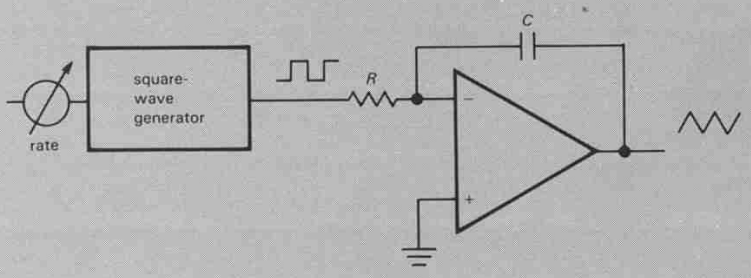
E. 200mA current source (from Diefenderfer, not intended as a "bad circuit")



B. × 100 op-amp output stage for audio amplifier



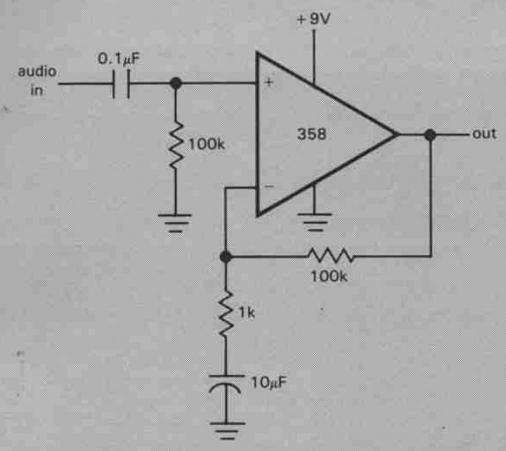
F. dc amplifier (× 100)



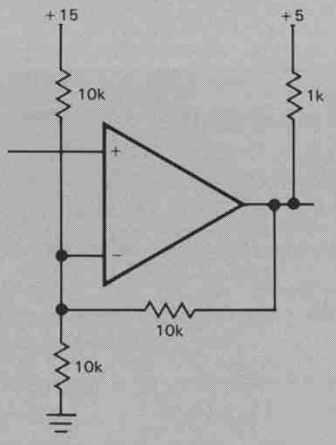
C. triangle wave-generator

Figure 4.95

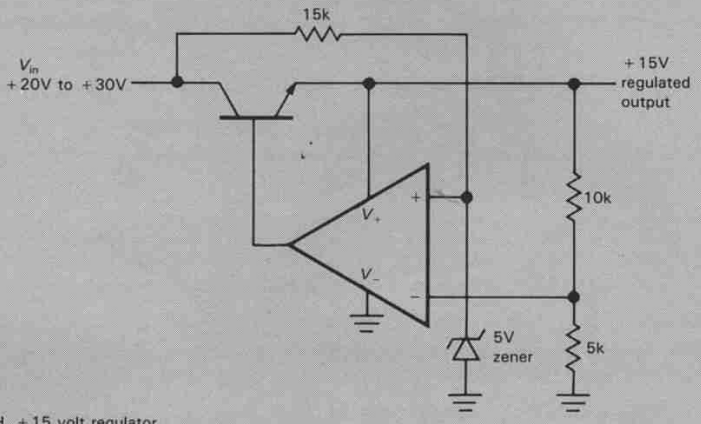
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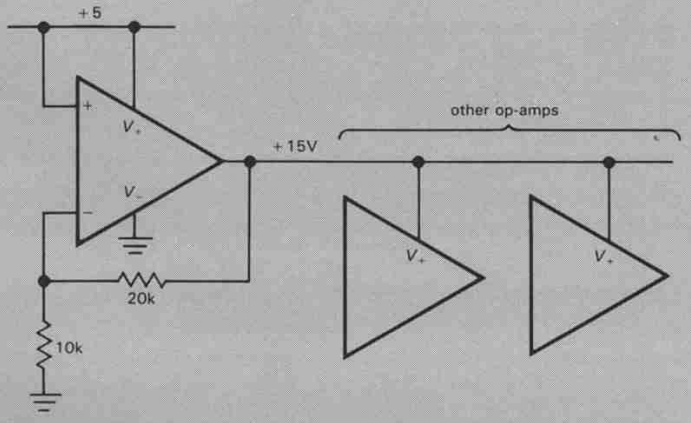
G. × 100 audio amplifier (single supply)



J. Schmitt trigger



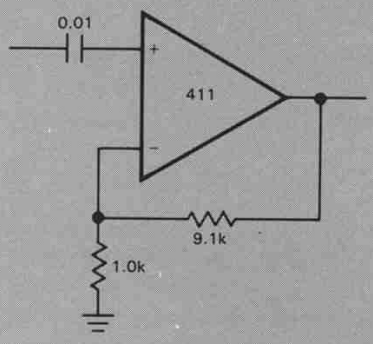
H. +15 volt regulator



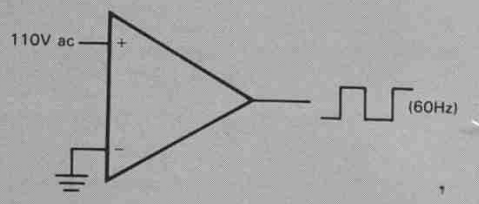
I. op-amp as +15V regulator

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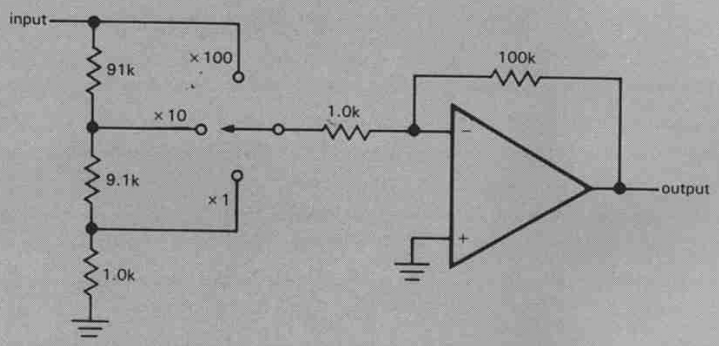
Bad circuits (*cont.*)



K. ac-coupled × 10 amplifier

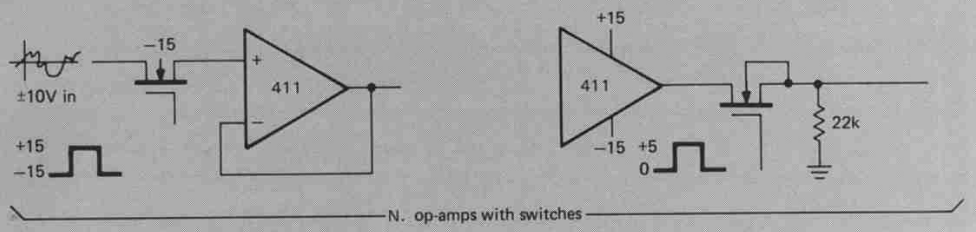


M. zero-crossing detector

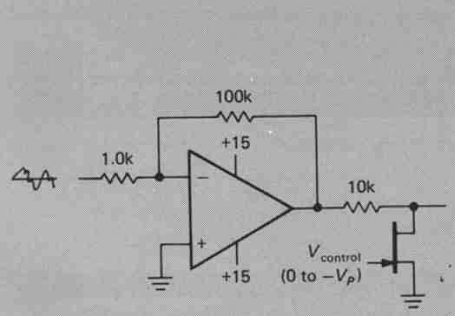


L. dc amplifier, selectable gains (× 1 to × 100)

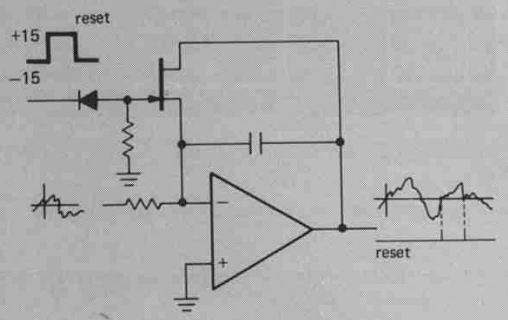
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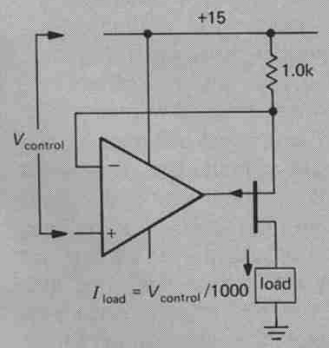
N. op-amps with switches



O. FET gain control



Q. integrator with reset



P. current source

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