

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

Petitioner

v.

MONOLITHIC POWER SYSTEMS, INC.

Patent Owner

IPR2024-01158

Patent No. 9,041,377

Filing Date:

Issue Date:

Title: PSEUDO CONSTANT ON TIME CONTROL
CIRCUIT AND STEP-DOWN REGULATOR

Inter Partes Review No.: IPR2024-01158

Exhibit 1003

Declaration of Douglas Holberg

TABLE OF CONTENTS

I.	INTRODUCTION	1
A.	Education and Relevant Experience.....	1
B.	Materials Considered.....	4
II.	LEGAL PRINCIPLES USED IN MY ANALYSIS.....	6
A.	Person Having Ordinary Skill in the Art.....	6
B.	The Prior Art	8
C.	Claim Construction Standard	8
D.	Anticipation	9
E.	Obviousness.....	9
III.	BACKGROUND OF THE TECHNOLOGY.....	15
A.	MOSFET	15
B.	Current Mirrors and Current Sources/Sinks.....	18
C.	DC-DC Converters	21
IV.	OVERVIEW OF THE '377 PATENT	25
A.	Brief Description	26
B.	Prosecution History	27
V.	OVERVIEW OF PRIOR ART	28
A.	U.S. Patent No. 8476887 to Tateishi.....	28
VI.	SPECIFIC GROUNDS FOR UNPATENTABILITY	33
A.	Ground 1: Claims 1-4, 9-14, and 17-18 are anticipated by Tateishi...33	
1.	Claim 1	33
2.	Claim 2.....	47
3.	Claim 3.....	50
4.	Claim 4.....	54
5.	Claim 9.....	56
6.	Claim 10.....	57

7.	Claim 11	60
8.	Claim 12	62
9.	Claim 13	63
10.	Claim 14	64
11.	Claim 17	65
12.	Claim 18	65
B.	Ground 2: Claims 5, 7-8, and 15 are rendered obvious by Tateishi ...	71
1.	Claim 5	71
2.	Claim 7	75
3.	Claim 8	75
4.	Claim 15	77
VII.	CONCLUDING STATEMENT	78

I. INTRODUCTION

1. I have been engaged by REED SEMICONDUCTOR CORP to opine on the patentability or otherwise of U.S. Patent No. 9,041,377 (the '377 Patent), titled PSEUDO CONSTANT ON TIME CONTROL CIRCUIT AND STEP-DOWN REGULATOR. My opinions are set forth herein. I submit this Declaration on behalf of REED SEMICONDUCTOR CORP in connection with its request for *inter partes* review of the '377 Patent.

A. Education and Relevant Experience

2. My education includes a B.S. in Electrical Engineering from Texas A&M University in 1977, followed by a M.S. in Electrical Engineering from the University of Texas at Austin in 1989. I earned a Ph.D. in Electrical Engineering from the University of Texas at Austin in 1992.

3. I have over 40 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Texas Micro Engineering (acquired by Crystal Semiconductor), Crystal Semiconductor, Cirrus Logic, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when they acquired Cygnal, which I co-founded in 1999.

4. I am a named inventor on 43 U.S. granted patents. I have held a variety of engineering positions throughout my career, from circuit designer,

design manager, Director of Engineering, Chief Technology Officer (CTO), Vice President (V.P.) of Engineering, and V.P. of Technology. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I taught CMOS analog and mixed-signal design for six years.

5. I am the co-author of the textbook CMOS Analog Circuit Design, the first edition of which published 1987. As explained in the Preface of the second edition, published in 2002, the objective of the textbook is to teach the fundamentals and background that are necessary to understand how a circuit works. It is now available in third edition and published in English and Chinese (first and second edition). This textbook is widely used throughout the world by new and experienced engineers in industry and by students in the classroom.

6. Upon graduating from Texas A&M University, I went to work for Mostek Corporation designing integrated circuits for telecommunications applications. I designed an integrated dual tone multi frequency (DTMF) generator. I received my first patent for this integrated DTMF generator. After leaving Mostek, I joined a startup company, Texas Micro Engineering, as the second employee. At Texas Micro Engineering, I designed, among other things, a dual-channel (atrium-ventricle) pacemaker sense amplifier/filter using discrete-time switched-capacitor technology.

7. While enrolled in the Masters/Ph.D. program at the University of Texas at Austin, I worked on the application of bipolar technology to dynamic random access memory (DRAM) sense-amplifier architectures and circuit-simulation algorithms. While at The University of Texas at Austin, I also designed and laid out the mask set (The Holberg Mask Set) still in use by the fabrication class/lab.

8. Upon graduating with a Ph.D. in Electrical Engineering, I went to work for Crystal Semiconductor/Cirrus Logic, where I designed high frequency synthesizers for hard-disk read-channel applications. I managed a group designing charge-coupled device (CCD) interface circuits for digital camera applications, as well as television encoder chips and CMOS imagers.

9. Upon leaving Cirrus, I started a company called Cygnal Integrated Products that developed mixed-signal microcontrollers. At Cygnal, I was the founder, CTO, V.P. of Engineering, and an individual contributor. While at Cygnal, I designed analog-to-digital converters (ADCs), Vbe temperature sensors, input/output (I/O) cells/pads (both design and layout), as well as many additional miscellaneous circuits. My company was later purchased by Silicon Labs, where I remained employed as a manager of the microcontroller group, followed by the position of V.P. of Technology.

10. I have significant experience with the technology described in the '377 patent, including resistors, capacitors, diodes, inductors, transistors, transformers, oscillators, operational amplifiers, comparators, general integrated-circuit technology, analog/digital mixed-signal circuits, DC-DC converters, device analysis and modeling, floor-planning, and layout of integrated circuits, and the tools used to design, and verify integrated circuits (CAD tools). In addition, I have experience with device modeling and characterization, which has been applied throughout my career.

11. My analyses set forth in this declaration are informed by my experience in the field of electrical engineering, including analog circuitry, ADCs, power circuits, and digital circuits. Based on my above-described experience, I believe that I am considered to be an expert in the field.

12. The '377 Patent is titled "Pseudo constant on time control circuit and step-down regulator." Prior to reviewing the '377 Patent, I was well familiar with the subject matter described and claimed therein. I am well familiar with circuits generally, such as disclosed in the '377 Patent.

B. Materials Considered

13. The analysis that I provide in this Declaration is based on my education and experience as an engineer, and upon my knowledge of general circuit analysis and design, as well as the documents I have considered, including

the '377 Patent (Ex.1001). I have reviewed the prosecution history for the '377 Patent (Ex.1002).

14. I have reviewed various publications from the prior art at the time of the alleged invention of the '377 Patent. These publications, along with other materials I have reviewed, include those listed in the table below:

Exhibit No.	Description
1001	U.S. Patent No. 9,041,377 B2 to Wang et al.
1002	Prosecution History of U.S. 9,041,377
1003	Declaration of Doug Holberg
1004	<i>Curriculum Vitae</i> of Doug Holberg
1005	U.S. Patent No. 8,476,887 B2 to Tateishi et al.
1006	Assignment of U.S. Patent No. 9,041,377 from Chengdu Monolithic Power Systems Co., Ltd. to Monolithic Power Systems, Inc.
1007	U.S. Patent Publication No. 2009/0140708 A1 to Tateishi et al.
1008	U.S. Patent No. 6,147,478 to Skelton et al.
1011	U.S. Patent No. 7,439,721 B2 to Weng et al. ("Weng")
1012	Paul Horowitz and Winfield Hill, "Art of Electronics" (Second Edition) ("AOE")
1013	TI Datasheet: "LM2696 3A, Constant On Time Buck Regulator" ("LM2696")
1014	TI Application report: "Adaptive Constant On-Time (D-CAP™) Control Study in Notebook Applications" ("DCAP")

Exhibit No.	Description
1015	Allen, Philip E., and Douglas R. Holberg. "CMOS Analog Circuit Design" (Second Edition) ("CMOS")

II. LEGAL PRINCIPLES USED IN MY ANALYSIS

15. I understand that in writing this Declaration I am obliged to follow existing applicable law. I have therefore been asked to apply the following legal principles to my analysis, and I have done so.

A. Person Having Ordinary Skill in the Art

16. I understand that my assessment of the claims of the '377 Patent must be undertaken from the perspective of what would have been known or understood by a person having ordinary skill in the art, reading the '377 Patent on its relevant filing date and in light of the specification and file history of that patent. I often refer to such a person as a POSITA in this Declaration.

17. I am informed and understand that various factors can be considered in determining a person having ordinary skill in the art (POSITA). I am informed and understand that those factors include: (1) the educational level of the inventor(s); (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) the rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the field.

18. I understand that REED SEMICONDUCTOR CORP proposed in the Petition that a person having ordinary skill in the art (POSITA) in the field of the '377 Patent as of June 30, 2011, would have been someone knowledgeable about and familiar with step-down regulator technology that is pertinent to the '377 Patent. A POSITA would have had a bachelor's degree in Electrical Engineering or equivalent training, and approximately two years of experience working in the field of step-down regulators or related technologies. Lack of work experience can be remedied by additional education, and vice versa.

19. I agree with this level of ordinary skill for the '377 Patent. Based on my experience, I understand and know of the capabilities of a person of this skill level as of the time the '377 Patent was filed. I am familiar with how a POSITA would have understood and used the terminology found in the '377 Patent at the time of its filing, and with the state of the art at that time.

20. My analysis and opinions presented herein regarding the claims of the '377 Patent have been and are based on the perspective of a POSITA as defined above as of June 30, 2011, the priority date for the '377 patent. As described above and as shown in my CV, I have extensive experience in the field of electronics in the relevant timeframe.

B. The Prior Art

21. I understand that applicable patent law provides categories of information that constitute prior art that may be used to anticipate patent claims or to render them obvious. I understand that for a reference to qualify as prior art to a particular patent claim under the relevant law, that reference must have been made, known, used, published, or patented, or must have been the subject of a patent application by another person, before the priority date of the patent, and in this matter, must satisfy one of the standards of pre-AIA 35 U.S.C. §102.

C. Claim Construction Standard

22. In making this Declaration, I have been asked to review the terms in the '377 Patent claims to determine what a POSITA would have understood those terms to have meant at the time of the alleged invention. In addition, I have been informed that, in an *inter partes* review proceeding, the claim terms under consideration are to be construed using the same claim construction standard used in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. I further understand that under the *Phillips* standard, the claim terms are given their ordinary and customary meaning, as would be understood by a POSITA at the time of the invention, consistent with the specification and the prosecution history. My opinions regarding the meaning of claim terms of the '377 Patent are based on the

construction of the claim terms using the *Phillips* standard in view of the specification and the prosecution history of the '377 Patent.

D. Anticipation

23. I understand that to be valid, a patent claim must be novel, and that a claim is invalid if it is anticipated by a single prior art reference. I further understand that a reference anticipates if it discloses each and every element of the claim and enables a POSITA to make and use the claimed invention without undue experimentation.

E. Obviousness

24. I also understand that even if a claim of a patent is not anticipated, that claim is still invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious to a POSITA at the time the invention was made.

25. I understand further that the condition “at the time the invention was made” in an obviousness determination is imposed to rule out impermissible hindsight. Accordingly, permissible reasoning takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned from the applicant’s disclosure in the patent under analysis. I also understand that an opining expert is

required to analyze prior art from the perspective of a POSITA and may not simply provide his or her own personal conclusions.

26. I also understand that an obviousness determination includes several factual inquiries, including: (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any secondary indicia (objective evidence) of non-obviousness.

27. I also understand that such objective evidence of non-obviousness may include: (1) a long felt but unsolved need that was satisfied by the claimed invention; (2) commercial success attributable to the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise by experts of the claimed invention with factual support; (5) taking of licenses under the patent by others for reasons related to the alleged non-obviousness of the claimed invention; (6) the failure of others; (7) the teaching away of others; (8) skepticism by experts; and (9) evidence that competitors in the marketplace have copied the invention instead of using the prior art. I also understand that, in order to establish non-obviousness, there must be a demonstrated relationship, or nexus, between any such secondary indicia and the claimed invention, i.e., there must be objective evidence of non-obviousness attributable to the claimed invention.

28. I further understand that near simultaneous invention by two or more equally talented inventors working independently may or may not be an indication of obviousness when considered in light of all the circumstances.

29. I understand that a conclusion of obviousness can be based on a combination of multiple prior art references. I understand that rationales that may support a conclusion of obviousness include:

(A) Combining prior art elements according to known methods to yield predictable results;

(B) Simply substituting one known element for another to obtain predictable results;

(C) Using known techniques to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) Using an obvious to try solution, i.e., choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Applying known work in one field of endeavor to yield variations of it for use in either the same field or a different one based on design

incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

(G) Applying some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference disclosures to arrive at the claimed invention.

30. I further understand that an analysis of obviousness should recognize that market demand, rather than scientific literature, often drives design trends.

31. I also understand that if a technique has been used to improve one device, and if a POSITA would recognize the technique would improve similar devices in the same way, then using that technique would be obvious to a POSITA unless actual application of that technique is beyond his or her skill.

32. I also understand that practical and common-sense considerations should guide an analysis of obviousness, because familiar items may have obvious uses beyond their primary purposes. I further understand that applying common sense does not require a specific hint or suggestion in a particular reference. Rather, applying common sense requires a reasoned explanation that avoids conclusory generalizations and false deductions.

33. I also understand that, when addressing a problem, a POSITA will often be able to fit together the disclosures of multiple publications. In this regard,

I understand that an analysis of obviousness may consider inferences and creative steps that a POSITA would normally employ.

34. I also understand that a particular combination of prior art may be proven obvious merely by showing that it was obvious for a POSITA to try that combination. For example, when there is a design need or a market pressure to solve a problem, and/or there exists a finite number of identified, predictable solutions with a reasonable expectation of success, a POSITA has good reason to pursue the known options within his or her technical grasp. I understand that if this leads to anticipated success, it is likely that the result is not of innovation but of ordinary skill and common sense.

35. I also understand that a combination of familiar elements according to known methods is presumed to be obvious when that combination does no more than yield predictable results. Work known in one field of endeavor may prompt variations of that work for use in either the same field or a different field, based on design incentives and other market forces. If a technique has been used to improve some device, and a POSITA can implement a predictable variation of that technique, then that variation is likely unpatentable.

36. I further understand that to be proper for use in an analysis of obviousness, a reference must teach art that is analogous to the claimed invention. I also understand that under a correct analysis, any need or problem known in the

field of endeavor at the time of the invention and addressed by the claimed invention can provide a reason for combining the elements in the manner claimed.

37. I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in that single reference can be supplied by the common sense or technical knowledge of a POSITA. For example, combining two embodiments disclosed adjacent to each other in a prior art patent likely does not require a leap of inventiveness.

38. I also understand that a claimed invention may be obvious if it merely involves simple substitution of one known element for another to obtain predictable results.

39. I understand further that, in an analysis of obviousness, two items of prior art need not be like two puzzle pieces that must fit together perfectly. For example, a claimed invention may be found obvious if a POSITA would view rearrangement as an obvious matter of design choice.

40. I also understand that an analysis of obviousness requires a comparison between the properly construed claim language and the prior art on a limitation-by-limitation basis.

III. BACKGROUND OF THE TECHNOLOGY

A. MOSFET

41. MOSFETS encompass a broad field well beyond the scope of the background necessary to understand the patents in this proceeding. Thus, only information germane to this declaration will be provided.

42. A MOSFET transistor is a four-terminal electrical device that is used as an amplifier or a switch. They are manufactured in fundamentally two varieties: P-channel and N-channel. Each can be implemented as enhancement-mode or depletion-mode. Only enhancement mode MOSFETs are of interest here. The symbol for a four-terminal N-channel and P-channel transistors along with voltage and current conventions are shown below (CMOS, P73).

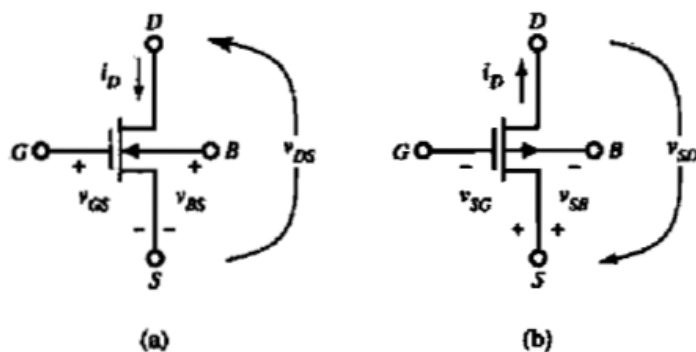


Figure 3.1-1 Positive sign convention for (a) n-channel and (b) p-channel MOS transistor.

43. The terminals are identified as Drain (D), Gate (G), Source (S), and Substrate (B).

44. A general MOSFET is a bi-directional device and as such, the drain and source can often be interchanged. This is particularly the case when

implemented on an integrated circuit. When manufactured as a discrete component, the manufacturer determines which terminal is the drain and source.

45. All of the MOSFETs considered in this declaration tie the substrate terminal to the source terminal. When configured this way, the terminal where the substrate is connected is considered the source.

46. N-channel MOSFETS conduct current from the drain to the source (conventional current flows into the drain and out the source). The amount of current that flows in a MOSFET is determined by the voltages on all four terminals. When configured with the substrate connected to the source terminal, and $v_{ds} < v_{GS} - V_T$, the amount of current can be approximated by the well known Shichman-Hodges model shown below (*See CMOS, P73*).

$$i_D = \frac{\mu_0 C_{ox} W}{L} \left[(v_{GS} - V_T) - \left(\frac{v_{DS}}{2} \right) \right] v_{DS} \quad (3.1-1)$$

Where

μ_0 =surface mobility

C_{ox} =oxide capacitance per unit area

W = effective channel width

L = effective channel length

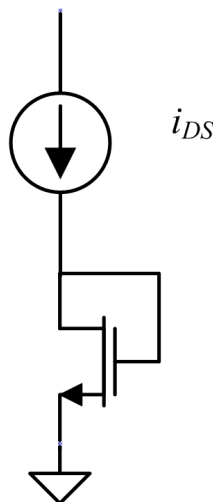
V_T =threshold voltage

47. Once the voltage $v_{ds} > v_{GS} - v_T$, the transistor begins to operate in what is called the “saturation” region. In this region, the drain current is modeled by the following equation (*See CMOS, P76*) commonly referred to as the square-law model.

$$i_D = K' \frac{W}{2L} (v_{GS} - V_T)^2, \quad 0 < (v_{GS} - V_T) \leq v_{DS} \quad (3.1-17)$$

Where $K' = \mu_0 C_{OX}$.

Consider the circuit below which is an N-channel transistor with gate and drain connected together (substrate not shown but tied to the source) and fed a current, i_{DS} .

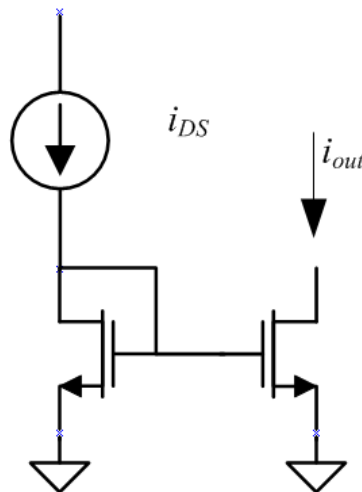


48. The feedback from drain to gate will cause the gate voltage to increase until the transistor can support the current forced into the drain. The resulting v_{GS} is derived from the square-law equation given above:

$$v_{GS} = \sqrt{\frac{i_{DS}}{K'W/2L}} + V_T$$

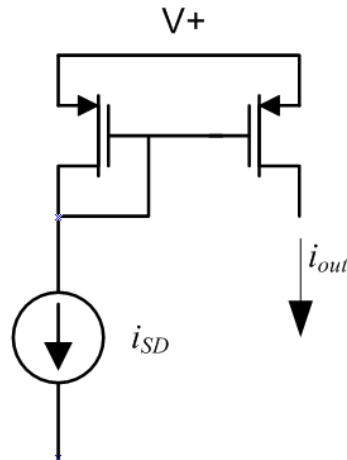
B. Current Mirrors and Current Sources/Sinks

49. Consider the circuit shown below where two transistors share a common gate and source (ground) while one of them has the gate and drain tied together. Assume both transistors have identical parameters (K' , W , and L).



50. Because both transistors have the same gate-to-source voltage, the drain currents of each will be identical. For this reason, this circuit is called a

current mirror. A similar circuit implemented with P-channel transistors (shown below) operates the same way.



51. It is very often the case where a current source (or sink) is needed. A very common implementation is shown below (See AOE, P181).

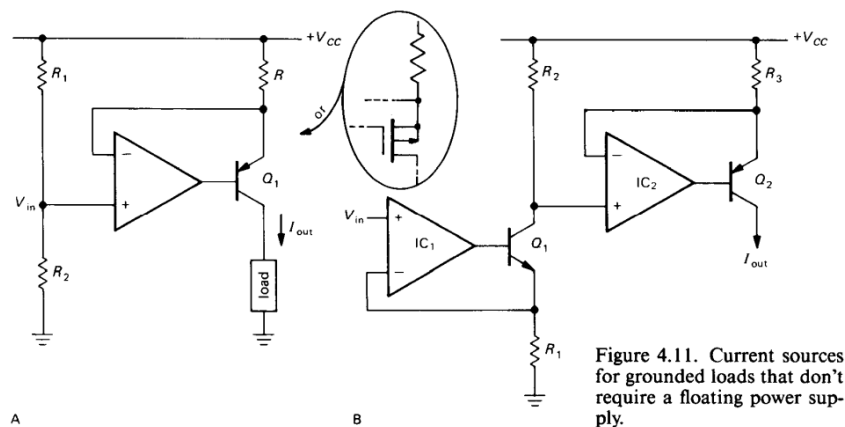
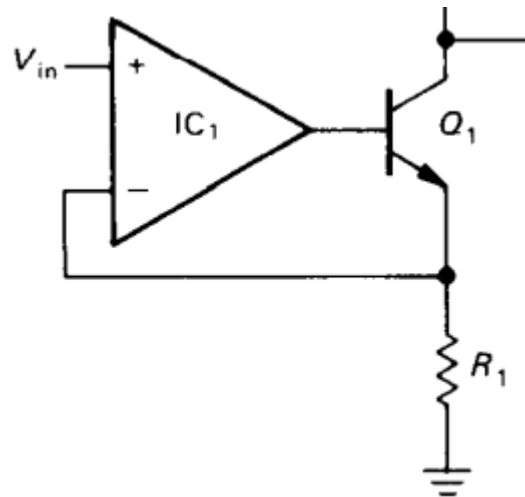
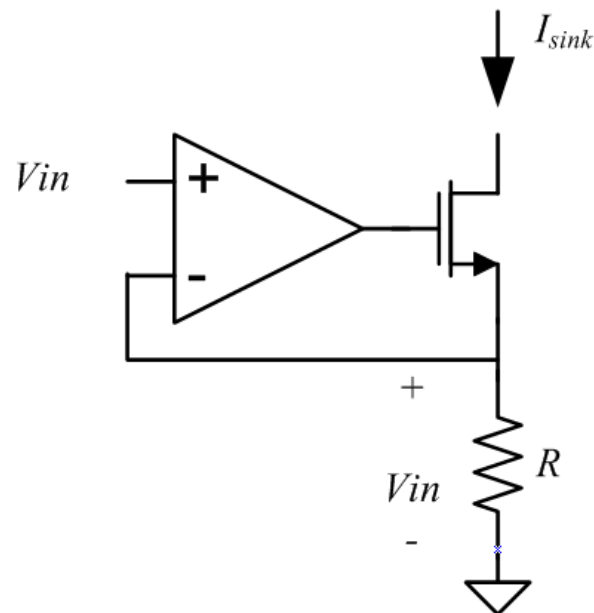


Figure 4.11. Current sources for grounded loads that don't require a floating power supply.

52. Consider, in particular, the current sink elements cropped below.



53. As noted in AOE, the bipolar transistor can be replaced with a MOSFET (as shown below) to achieve the same end results. The operational amplifier configuration imposes the input voltage across the resistor, R , resulting in a current sink at the drain of V_{in}/R .

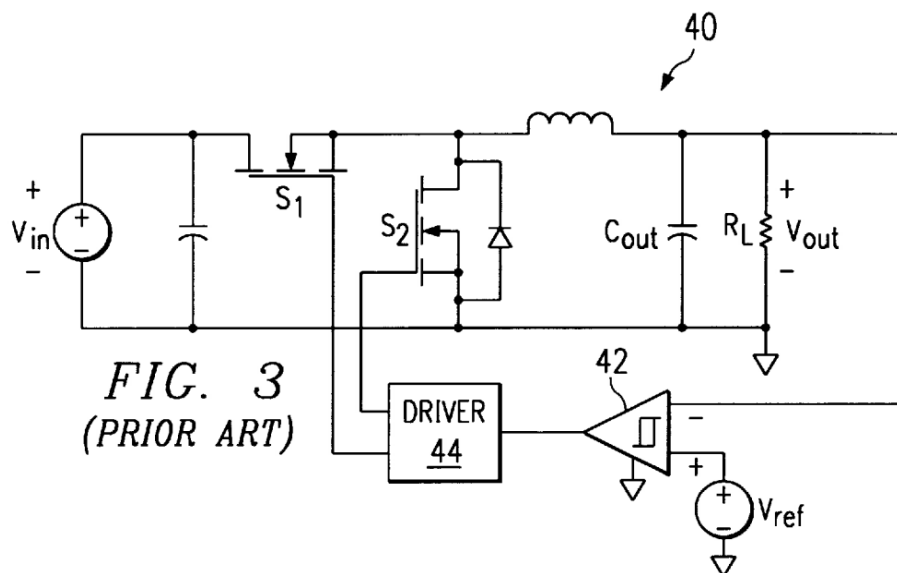


C. DC-DC Converters

54. DC-DC converters are also known by other names: Switch Mode Power Supply, (SMPS), switching regulator, switching power supply, switch-mode converter, DC/DC converter, and perhaps other names as well. These devices improve on the efficiency of linear converters (also called linear regulators) in that switch-mode converters consume less power than linear regulators in most conditions. A DC-DC converter takes an input and supplies an output. If the output is greater than the input, it is a step-up converter generally called a Boost converter whereas, if the output is less than the input, it is a step-down converter generally called a Buck converter.

55. There are a variety of control methods and topologies for DC-DC converters. Of interest in my declaration are those that use a constant on time control method. These types of converters are derived from hysteretic converters.

56. A simple hysteretic converter is disclosed as prior art in U.S. Patent 6,147,478 (Skelton , Ex. 1008), Fig. 3 shown below.



57. The operation of this topology is very simple. The output voltage is compared to a reference voltage using a comparator having two comparison thresholds, V_{th1} and V_{th2} where $V_{th2} > V_{th1}$. When the output voltage falls below the lower threshold, V_{th1} , the comparator turns S_1 on (and S_2 off) causing the output to rise until the output reaches the upper threshold, V_{th2} , when the comparator switches so as to turn S_1 off and S_2 on resulting in the output falling again as before. This continues during the operation of the hysteretic converter. The resulting output is a ripple voltage amplitude determined by the upper and lower thresholds of the comparator.

58. Hysteretic converters are very simple, but the frequency of the output ripple varies as a function of the output inductor and capacitor (See LM2696, P7). By introducing a constant on time (e.g., Weng) for the high side driver, better control of the ripple frequency can be achieved.

59. For a buck converter, the duty cycle determines the ratio of output voltage to input voltage (See LM2696, P8):

$$D = \frac{V_{out}}{V_{in}} = \frac{T_{on}}{T}, \text{ where } T \text{ is the period of the output ripple}$$

$$F = 1/T = D/T_{on}$$

60. For a fixed V_{in} and V_{out} , the frequency of the ripple is fixed to D/T_{on} . Thus, for a fixed T_{on} , the ripple frequency is also fixed.

61. Generally, a buck converter will not have a fixed input voltage. As such, the duty cycle, D , must adjust in order to maintain the desired regulated V_{out} resulting in a varying frequency of the output ripple. This can be remedied somewhat by modifying T_{on} so that it is inversely a function of V_{in} , i.e., $T_{on} = k/V_{in}$ (where k is a constant). Since V_{out} remains constant, the frequency of the ripple is then V_{out}/k .

62. This control mode can be further improved by making T_{on} a function of both V_{in} and V_{out} (See DCAP, P3). Consider the circuit shown in Fig. 7 of

DCAP shown below.

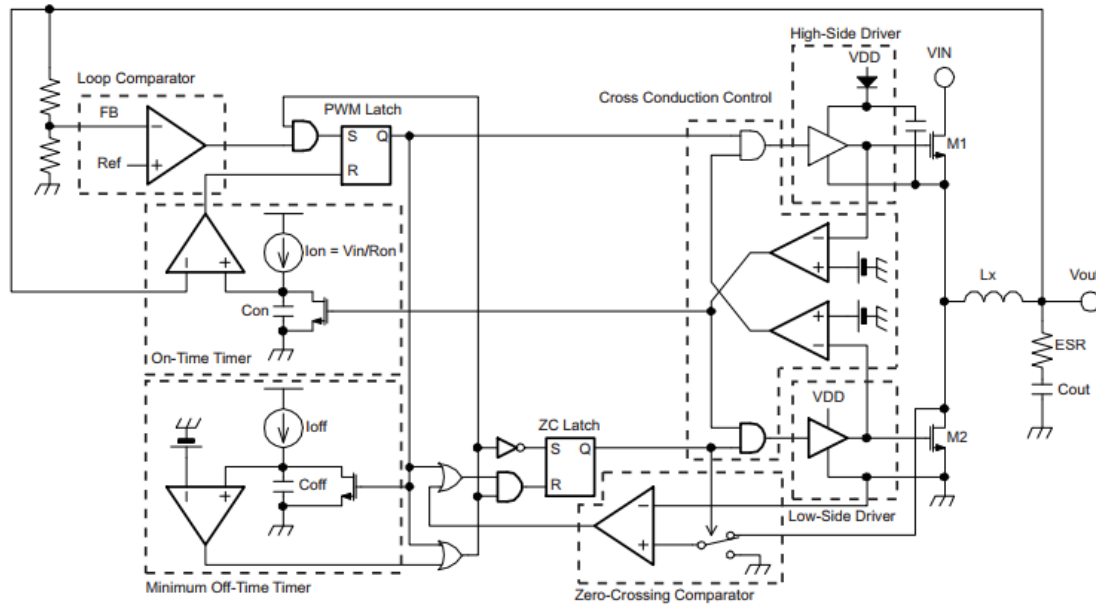


Figure 7. D-CAP™ Mode Block Diagram

63. This circuit operates as follows. When the FB terminal at the input of the Loop Comparator falls below Ref (voltage), the PWM latch is set turning on the high-side switch M1 and turning off the low-side switch M2. The shunt MOSFET in the on-Time Timer turns off allowing the capacitor *Con* to charge at a rate determined by $I_{on} = V_{in}/R_{on}$. Capacitor *Con* drives the non-inverting input of the On-Time comparator whose inverting input is driven by *Vout*. Once *Con* charges to a voltage equal to *Vout*, the comparator changes state and resets the PWM latch, turning off the high-side switch M1 and turning on the low-side switch M2. This operation is analyzed as follows.

$$I_{on} = V_{in}/R_{on}$$

Since I_{on} is a constant current, the voltage across C_{on} is a constant ramp starting at zero. Thus, $V_{C_{on}} = \Delta T \times I_{on}/C_{on}$.

Since ΔT is the on time, T_{on} , when $V_{C_{on}} = V_{out}$, the expression becomes

$$V_{out} = T_{on} \times I_{on}/C_{on} = T_{on} \times \frac{V_{in}}{R_{on}C_{on}}$$

$$V_{out}/V_{in} = \frac{T_{on}}{R_{on}C_{on}}$$

$$T_{on}/T = V_{out}/V_{in} = \frac{T_{on}}{R_{on}C_{on}}$$

$$1/T = \frac{1}{R_{on}C_{on}}$$

$$F = \frac{1}{R_{on}C_{on}}$$

64. Thus, for this architecture, the Frequency of the ripple is fixed based on design parameters, R_{on} and C_{on} .

IV. OVERVIEW OF THE '377 PATENT

65. The '377 Patent issued on May 26, 2015 from Patent Application Serial No. 13/538,815 (EX1002 at 8-38) ("the '815 Appl."), filed on June 29, 2012 by Chengdu Monolithic Power Systems Co., Ltd. The '377 Patent claims priority to Chinese Patent Application No. 201110181295.3, filed on June 30, 2011. For purposes of this proceeding and without conceding the issue, Petitioner assumes all

Challenged Claims of the '377 Patent have a priority date of June 30, 2011, and that they were effectively filed as of that date. The '377 Patent was assigned to Patent Owner on January 30, 2024.

A. Brief Description

66. The '377 patent is directed to switch-mode DC-DC voltage converters having pseudo constant-on-time (PCOT) control circuits that control their high-side and low-side switches. EX1001, 4:42-45, 8:32-34, FIG. 11. As explained in the BACKGROUND section, in PCOT control, the on time T_{on} of the regulator is proportional to the ratio of the output voltage V_{out} to the input voltage V_{in} . EX1001, 1:55-57. Prior-art step-down regulators included an output voltage pin VOUT to receive V_{out} . EX1001, 2:11-14, FIG. 1; In contrast, the disclosed PCOT control circuit receives information of V_{in} and V_{out} from (a) the switching signal SW of the step-down regulator and (b) the control signal Q. EX1001, 7:42-59, FIG. 2.

67. In particular, the '377 patent discloses an input voltage sensing circuit A that provides an input voltage sensing signal, an output voltage sensing circuit B that provides an output voltage sensing signal, and a comparator COMP that compares the two sensing signals. EX1001, 4:46-48, FIG. 2. The input voltage sensing circuit A receives the switching signal SW and the control signal Q and

provides a linear ramping signal, where the ramp rate is given by the charging current, which is proportional to V_{in} . EX1001, 6:59-7:34.

68. The output voltage sensing circuit B receives the switching signal SW and provides a low-pass filtered (i.e., averaged) version of SW as the output voltage sensing signal. EX1001, 5:4-13. As can be seen in FIG. 12, when the control signal Q is a logical high ($Q=1$), the input voltage sensing signal S11 begins to ramp up until it reaches the output voltage sensing signal S12, at which time the on-time signal S1 causes the control signal Q to become logical low ($Q=0$). EX1001, 8:42-58

69. Because the ramping rate of S11 is proportional to V_{in} , and because the average value of SW is V_{out} , the on-time of the high-side switch is, thus, proportional to V_{out}/V_{in} .

B. Prosecution History

70. During prosecution of Application No. 13/538,815 (which issued as the '377 Patent), no Information Disclosure Statement was submitted.

71. The Examiner cited to U.S. Patent Publication No. 2010/0134080 ("Ouyang"), in the singular Office Action issued, having a notification date of August 14, 2014. In the August 14, 2014, Office Action, the Ouyang reference was used by the patent Examiner in a 35 USC §102 rejection of independent claims 1

and 12. The Examiner asserted that claims 2-11 and 13-20 included allowable subject matter in the Office Action dated August 14, 2014.

72. Patent Owner amended the claims to incorporate allowable subject matter from claim 2 into claim 1 and incorporate allowable subject matter from claim 13 into claim 12, and cancelled claims 2 and 13.

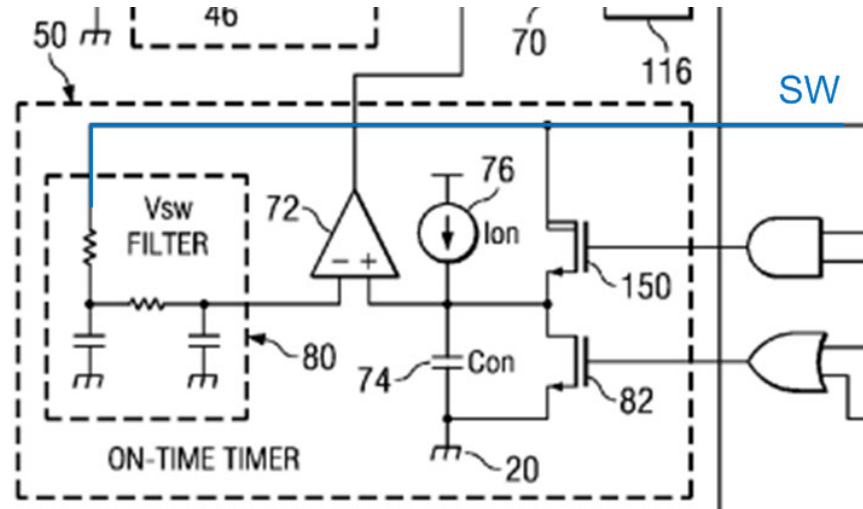
73. A notice of allowance was issued on January 22, 2015, and U.S. Patent Application No. 13/538,815 issued as U.S. Patent No. 9,041,377 B2 on May 26, 2015.

V. OVERVIEW OF PRIOR ART

A. U.S. Patent No. 8476887 to Tateishi

74. Tateishi is directed to DC to DC converters with pseudo constant switching frequency. EX1007, ¶5. In particular, Tateishi discloses using feedback from the switching node to establish the pseudo constant switching frequency, thus avoiding the need to provide a pin on the integrated circuit for direct feedback from the output node at the far end of the external filtering components. EX1007, ¶17. Tateishi discloses an on-time circuit 50 that establishes an on-time duration (T_{on}) that is proportional to the output voltage (V_{out}) and inversely proportional to the input voltage (V_{in}) without directly accessing V_{in} and V_{out} . EX1007, ¶32, FIG. 3 (reproduced and annotated below).

any desired manner, such as the two resistor, two capacitor example shown in FIG. 3, or with more or less resistors or capacitors, or any other desired implementation including even active filters.” EX1007, ¶49, FIG. 3 (a portion of which is reproduced and annotated below).



77. During the off-time, capacitor (Con) 74 is discharged to ground potential (20) by discharging transistor 82. EX1007, ¶51. During the on-time, capacitor Con 74 is charged up from ground potential with a current that is approximately proportional to V_{in} from current source 76. EX1007, ¶52. The on-time is terminated by the comparator 72 when the voltage on the capacitor Con 74 reaches approximately V_{out} , as generated by the V_{sw} filter 80. EX1007, ¶52.

78. Tateishi discloses several example embodiments of current source 76, one of which is shown in FIG. 4 below (cropped and annotated), which includes portions of the on-time circuit. EX1007, ¶62.

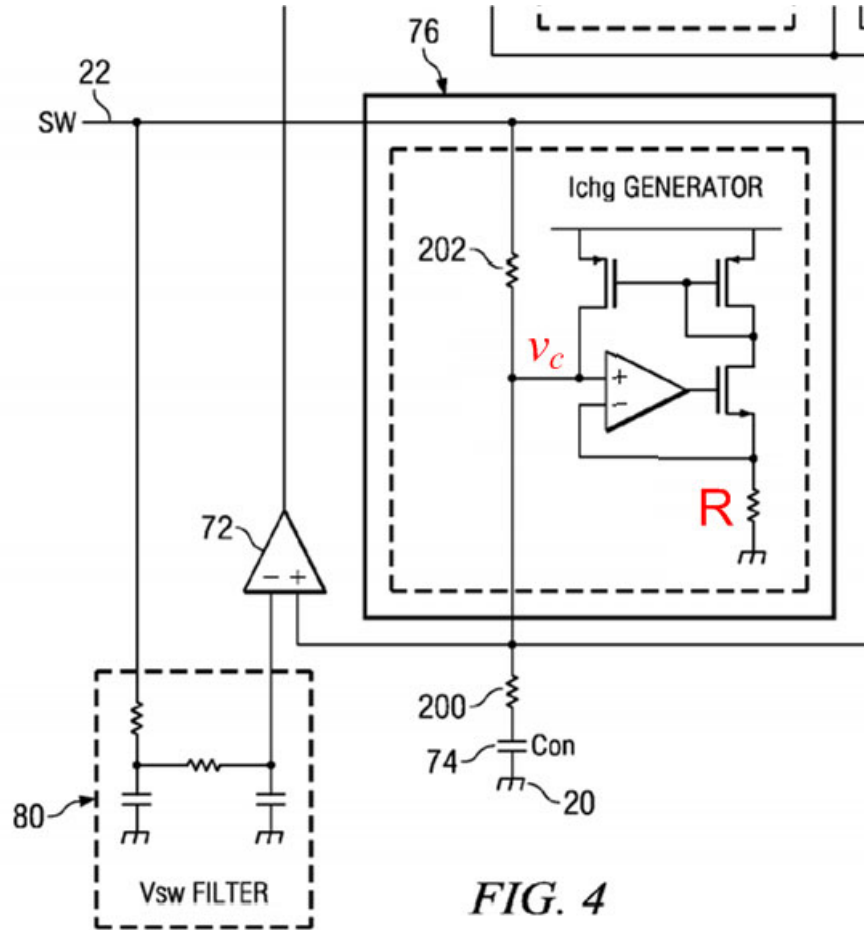


FIG. 4

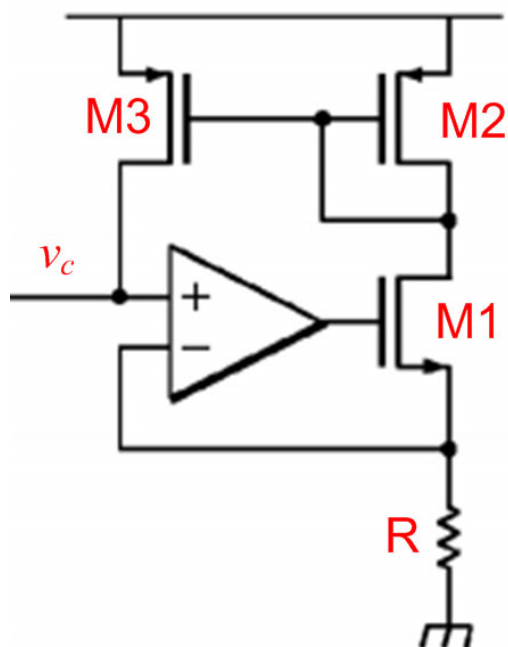
79. The specification also explains that the current source 76 may be embodied in other various configurations as desired to provide an output current that is approximately proportional to $v_{in}-v_{on1}$. EX1007, ¶62. This is explained as follows. The charging current for capacitor, Con, is given as:

$$i_C = \frac{v_{in}-v_{on1}-v_C}{R202} + \frac{v_C}{R} = \frac{v_{in}-v_{on1}}{R202}$$

where R is the unlabeled resistor in the *Ichg GENERATOR* and is equivalent to R202. Thus, the current that charges Con is a linear function of the input voltage

(voltage at node SW). For a given v_{in} , the current, i_c is constant (assuming v_{on1} is constant), thus the capacitor, C_{on} , charges linearly.

80. In the expression for i_c given above, the term, v_c/R is explained with the aid of the following cropped and annotated Fig. 4. The output of the opamp drives the gate of M1 which is configured as a source follower providing unity-gain feedback to the inverting input of the opamp. Thus, the combination of the opamp and M1 provides unity gain from the non-inverting input (v_c) to the upper node of resistor R. Based on Ohm's law, the current in resistor R is simply v_c/R . MOSFET M1 provides this current via transistor M2 which is connected in the well-known "diode" configuration. The gate/drain of M2 is also connected to the gate of M3 forming a well-known current mirror so that (assuming the geometries of M2 and M3 are the same), the current flowing in R would be reflected as an identical current flowing from the drain of M3 (at node v_c). *See III.B.* While Tateishi does not give specific values for the MOSFET geometries nor the value of R, in order to achieve a current proportional to $v_{in} - v_{on1}$, the transconductance I_{chg}/v_c must be $1/R$. While this can be achieved several ways, the most obvious choice by a POSITA would be to set $R=R_{202}$ and to set the gain of the current mirror to unity.



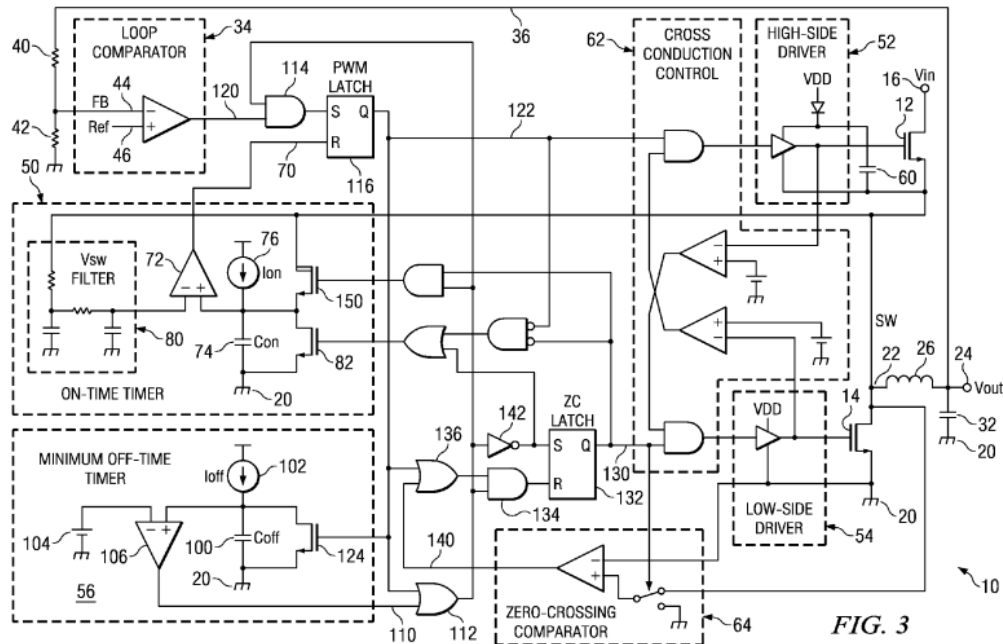
VI. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Ground 1: Claims 1-4, 9-14, and 17-18 are anticipated by Tateishi

1. Claim 1

a. Limitation 1[PRE]: A step-down regulator, comprising:

81. Limitation 1[PRE] recites a step-down regulator. To the extent that the preamble is limiting, Tateishi discloses a buck converter which is well known in the art as a step-down converter as illustrated in Fig. 3 below. *See* Tateishi ¶18. A buck converter is also understood by a POSITA as a regulator because it receives an input voltage and regulates it to a lower output voltage.



b. Limitation 1[A]: a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:

82. Limitation 1[A] recites a regulator (preamble) with pseudo constant on time control circuit. Tateishi discloses a pseudo constant converter using pseudo constant frequency (*Id.* ¶5). Furthermore, Tateishi implements a pseudo on time algorithm as follows (*Id.* ¶45-48):

$$T_{on}+T_{off}=T_{on}*(V_{in}-V_{on1})/(V_{out}+V_{dcr}) \quad (9)$$

[0045] Based upon equation (9), a pseudo on-time generation algorithm is obtained as follows:

[0046] Discharge capacitor Con 74 to 0V during off-time

[0047] Charge capacitor Con 74 during on-time with a current proportional to (Vin-Von1)

[0048] Terminate on-time when the voltage on capacitor Con 74 becomes (Vout+Vdcr)

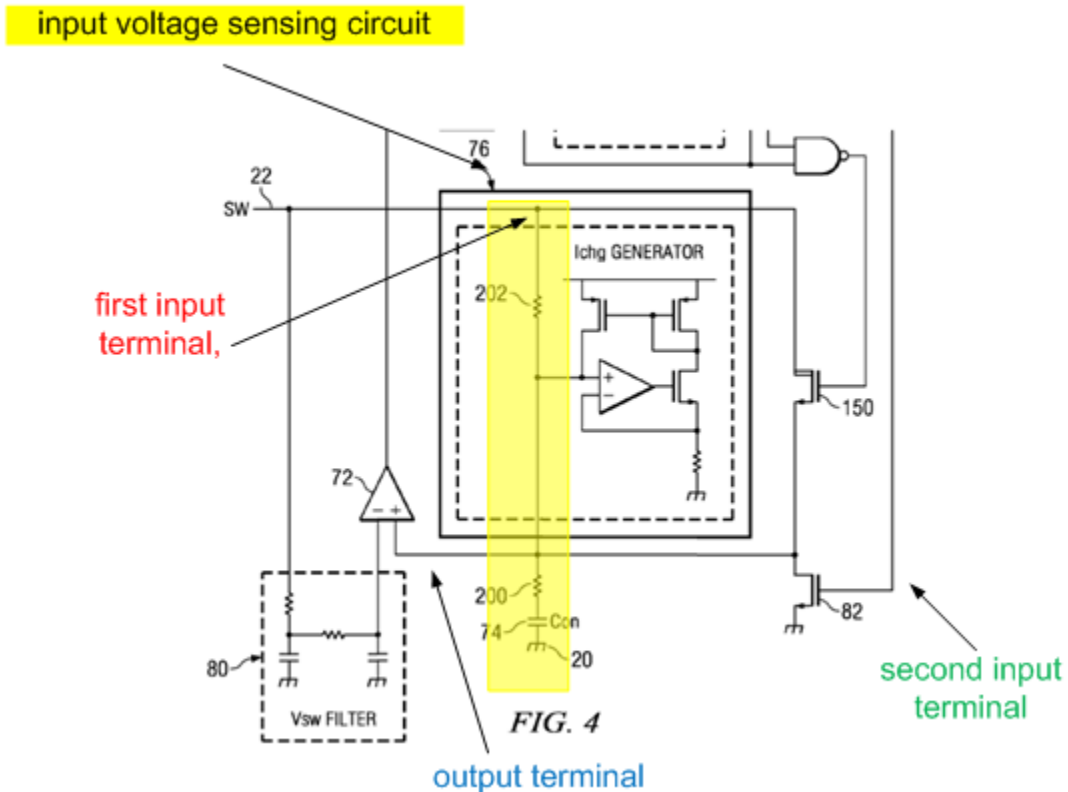
c. Limitation 1[B1]: an on-time generator comprising:

On-time generator



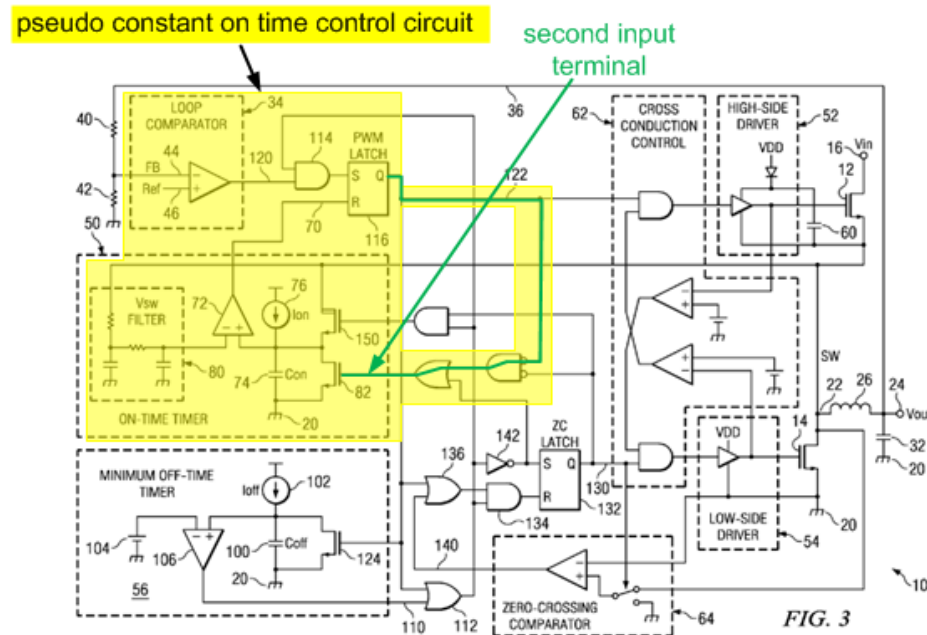
- d. Limitation 1[B2]: an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

84. Limitation 1[B2] recites structure of an input voltage sensing circuit of the on-time generator. Tateishi discloses this limitation. Firstly, Tateishi discloses an input voltage sensing circuit with first and second inputs and an output as shown below in Fig. 3 (cropped and annotated). It is my opinion that a POSITA would understand that a terminal is a point of electrical connection, e.g., an input or an output. The output of Tateishi's input voltage sensing circuit (as explained in more detail below) generates a signal that is related to the input voltage. *See* ¶85.

[illegible]

87. The second input terminal receives its input from PWM latch 116 in the on-time control circuit as illustrated below in Fig. 3 of Tateishi. *Id.* (annotated). Once an on-time is initiated by the loop comparator 34, the capacitor Con 74

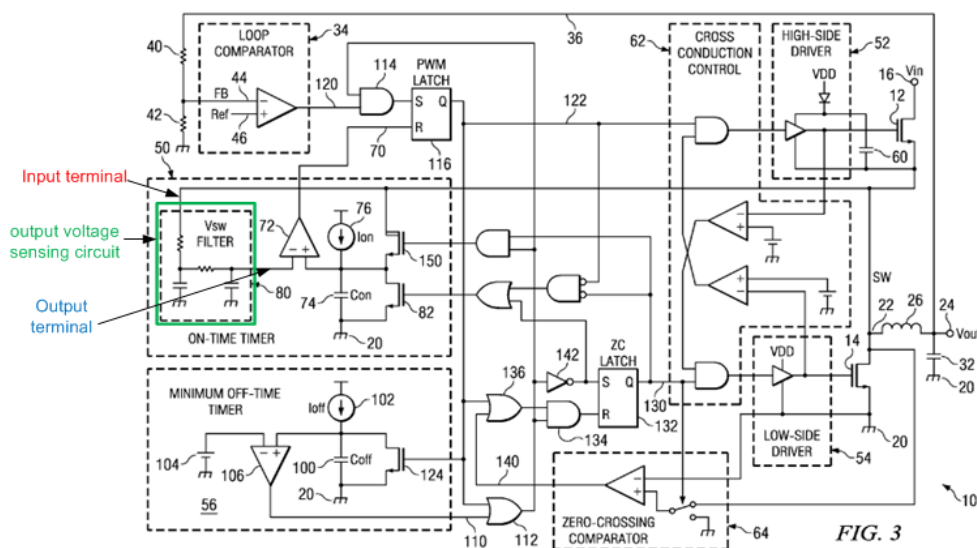
begins to charge up by the current from the current source 76 (which is proportional to the input voltage). *Id.* ¶33.



88. Thus, Tateishi discloses an input voltage sensing circuit having a first input terminal configured to receive a switching signal (SW) provided by the step-down regulator, a second input terminal configured to receive a control signal (SR latch output 122) provided by the pseudo constant on time control circuit, the input voltage sensing circuit generating an input voltage sensing signal (the voltage on the capacitor Con 74) at an output terminal (the non-grounded side of capacitor Con 74) based on the switching signal (SW) and the control signal (SR latch output 122). *See, e.g.*, EX1007, Fig. 4.

- e. **Limitation 1[B3]: an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and**

89. Limitation 1[B3] recites structure of an output voltage sensing circuit of the on-time generator. Tateishi discloses this limitation. In particular, Tateishi discloses generating the average voltage of the switching node 22 across an entire switching period by V_{sw} low-pass filter 80. See, e.g., EX1007, ¶¶49, 52, Fig. 3 shown below (annotated). *Id.*



90. The input terminal receives its input from the SW terminal and the output terminal is coupled to comparator 72.

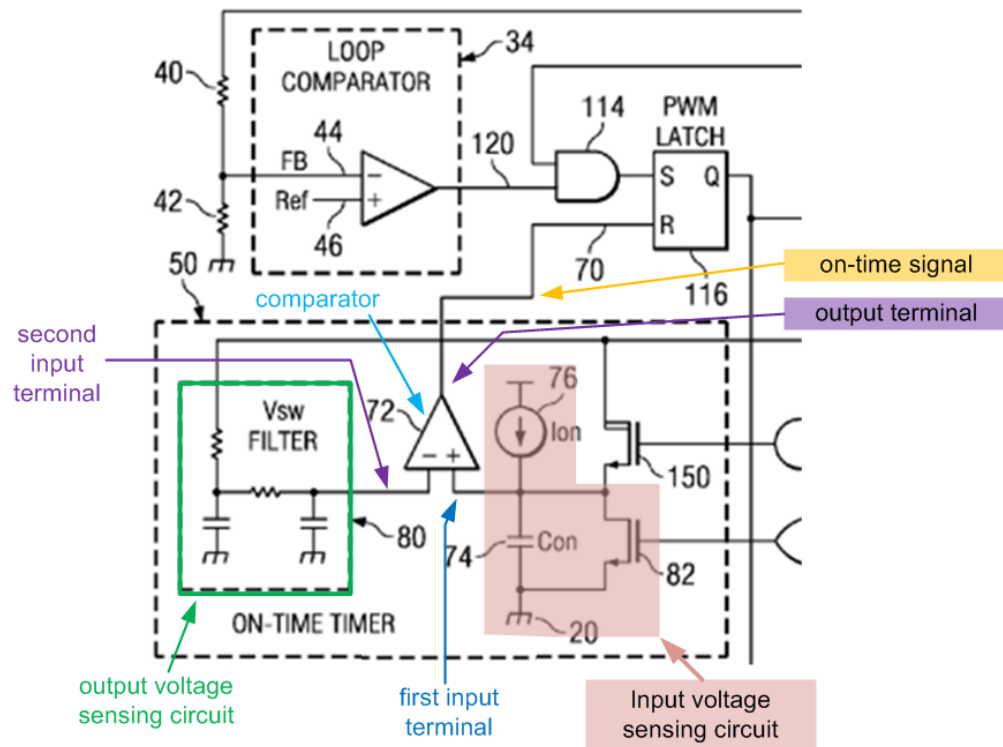
91. Thus, Tateishi discloses an output voltage sensing circuit having an input terminal configured to receive the switching signal (SW) and generating an

output voltage sensing signal based on the switching signal (low-pass filtered/averaged switching-node voltage) at an output terminal.

- f. **Limitation 1[B4]: a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;**

92. Limitation 1[B4] recites a comparator having a first input terminal coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, a second input terminal coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at an output terminal. Tateishi (in particular, Tateishi's comparator 72) discloses this limitation. *See, e.g.*, EX1007, ¶33 ("The on-time is generated using a comparator 72 ... The comparator 72 monitors the voltage of the capacitor Con 74 and asserts the on-time termination signal 70 to terminate the on-time when the voltage of the capacitor Con 74 reaches a reference voltage."), ¶49, ("The on-time is terminated by the comparator

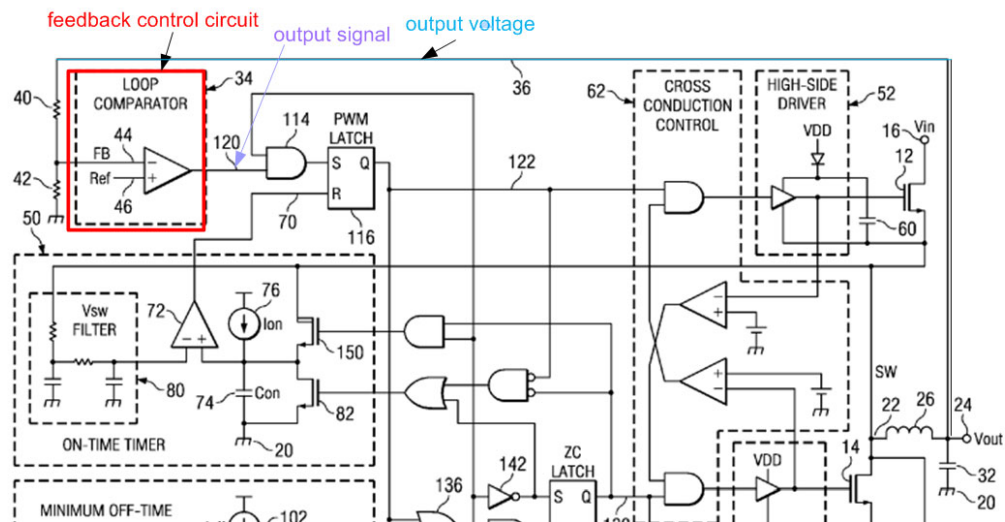
72 when the voltage on the capacitor Con 74 reaches $(V_{out} + V_{dcr})$ as generated by the Vsw filter 80.”), FIG. 3 below (cropped and annotated);



93. As shown in Fig. 3, Tateishi’s comparator 72 receives the output voltage sensing signal from Vsw filter 50 and receives the input voltage sensing signal from capacitor Con 74 and, based on those inputs, generates on-time termination signal 70. Thus, Tateishi discloses this limitation.

- g. **Limitation 1[C]: a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and**

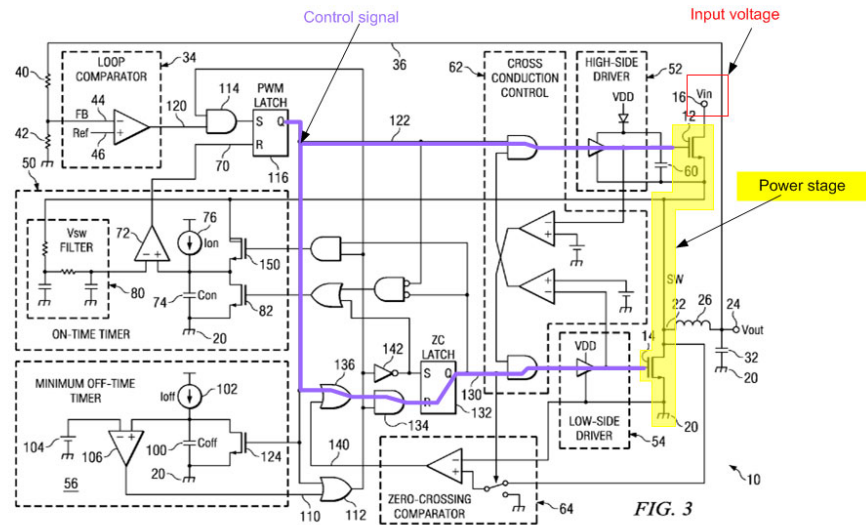
94. Limitation 1[C] recites a feedback control circuit configured to generate an output signal in accordance with a feedback signal representative of the output voltage of the step-down regulator. Tateishi (in particular, Tateishi's loop comparator 34) discloses this limitation. *See, e.g.*, ¶19 (“A loop comparator 34 in the DC to DC buck converter 10 begins each on-time based on a feedback signal 36 from the output Vout 24. The voltage of the feedback signal 36 is divided in an external voltage divider made up of an upper resistor 40 and a lower resistor 42.”), Fig. 3 below (cropped and annotated). A POSITA would understand that the output (FB) of the voltage divider is proportional to (i.e., representative of) the output voltage.



- h. Limitation 1[D]: a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and

95. Limitation 1[D] recites a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal of limitation 1[B4] and the output signal of limitation 1[C], wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal of limitation 1[B2]. Tateishi (in particular, Tateishi's PWM SR latch 116 – possibly in combination with AND gate 114) discloses this limitation. *See, e.g.*, EX1007, ¶51 (“The output 120 of the loop comparator 34 is combined with the output 110 of the minimum off-time timer 56 in the AND gate 114 at the input of the SR latch 116... The output 122 of the SR latch 116 is thus asserted, turning on the high side switch 12 and turning off the low side switch 14.”), ¶52 (“The on-time termination signal 70 is connected to the Reset input of the SR latch 116, turning off the output 122 of the SR latch 116.”), Fig. 3 below (cropped and annotated).

In particular, Tateishi discloses a cross-conduction circuit that receives the control signal 122 produced by PWM SR latch 116, high-side and low-side switch drivers (52, 54) and high-side and low-side power switches (12, 14) configured to perform synchronous rectification. EX1007, Fig. 3 below (annotated).



98. See, e.g., EX1007, ¶18 (“A high side switch 12 and a low side switch 14 are connected in series between an input V_{in} 16 and ground 20, with a switching node 22 between the high side switch 12 and the low side switch 14. An output V_{out} 24 is connected to the switching node 22 through an output filter. For example, the output filter may include an inductor 26 connected between the switching node 22 and the output V_{out} 24, and capacitor 32 connected in series between the output V_{out} 24 and ground 20.”), Fig. 3.

99. To the extent that Tateishi does not expressly refer to this disclosed arrangement of components as a “power stage,” it is my opinion that a POSITA

would understand that the arrangement of these components (illustrated and described in Fig. 3 and the associated written description) necessarily constitute the power stage of Tateishi's buck converter. The power stage receives an input voltage (Vin) 16 and control signal 122 and produces a voltage signal at the switching node (SW) 22 through the operation of high-side and low-side power switches. Thus, in my opinion, a POSITA would see that Tateishi anticipates claim 1.

2. Claim 2

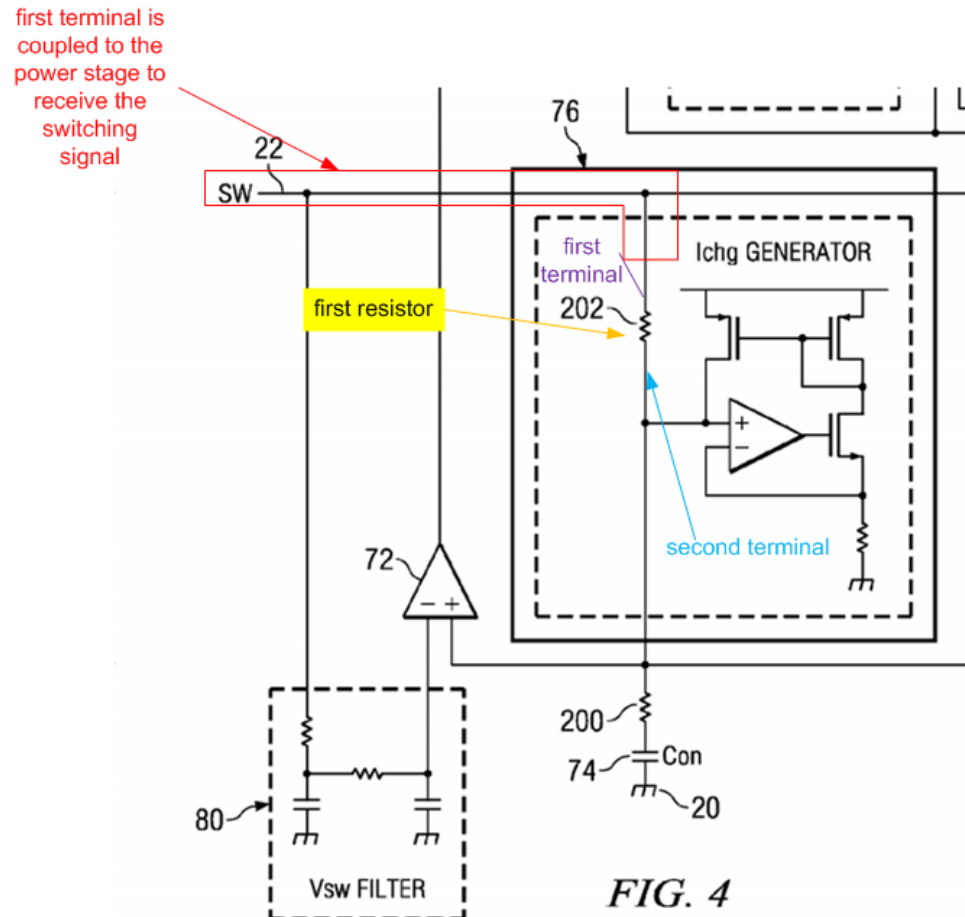
a. Limitation 2[PRE]: The step-down regulator of claim 1, wherein the input voltage sensing circuit comprises:

100. Claim 2 depends from claim 1. In my opinion, as demonstrated above, a POSITA would see that Tateishi anticipates claim 1. *See* VI.A.1.

b. Limitation 2[A]: a first resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the power stage to receive the switching signal;

101. Limitation 2[A] recites the input voltage sensing circuit including a first resistor coupled to the power stage to receive the switching signal. Tateishi discloses this limitation. *See, e.g.*, ¶62 (“Various elements of another embodiment of a DC to DC buck converter 10 are illustrated in FIG. 4... The input voltage to the amplifier 86 in the current source 76 is connected... to the switching node 22

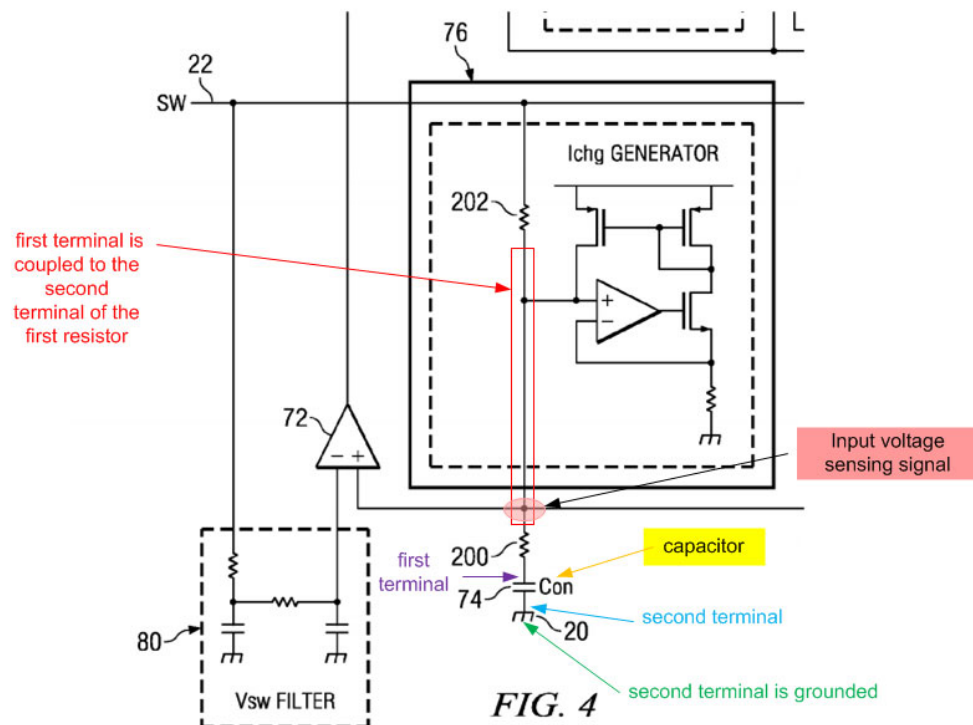
through a resistor 202”), Fig. 4 (a portion of which is reproduced and annotated below);



- c. **Limitation 2[B]: a capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first resistor and provides the input voltage sensing signal, and the second terminal is grounded; and**

102. Limitation 2[B] recites the input voltage sensing circuit including a capacitor coupled to the first resistor at one terminal and grounded at the other terminal. Tateishi (in particular, Tateishi’s capacitor Con 74) discloses this

limitation. *See, e.g.,* EX1007, Fig. 4 below (cropped and annotated) showing capacitor Con 74 coupled to resistor 202 through “resistor 200 connected in series with the capacitor Con 74 to compensate for circuit delays such as in comparators, drivers, external MOSFETS, etc [sic]” EX1007, ¶62. The embodiment of Fig. 3 shows capacitor Con 74 coupled directly to resistor 202. In either embodiment (Fig. 3 or Fig. 4), it is my opinion that a POSITA would understand from the disclosure of Tateishi that capacitor Con 74 is coupled to resistor 202.



- d. **Limitation 2[C]: a switch having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the logic control circuit to receive the control signal, the first terminal is coupled to the first terminal of the capacitor, and the second terminal is grounded.**

- b. Limitation 3[A]: the input voltage sensing circuit further comprises a linear current compensation circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, and wherein based on the input voltage sensing signal, the linear current compensation circuit provides a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage.

105. Limitation 3[a] recites the input voltage sensing circuit further comprising a linear current compensation circuit providing a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage. Tateishi discloses this limitation. See, e.g., EX1007, ¶62 (“The current source 76 may be embodied in other various configurations as desired to provide an output current that is proportional to $(V_{in}-V_{on1})$.”). As discussed with respect to the current-source embodiment of Fig. 2, “The voltage divider 90 and 92, voltage follower amplifier 86 and current mirror 94 all operate in a linear fashion, so the current output 84 of the current source 76 is proportional to the voltage of the switching node 22.” EX1007, ¶50.

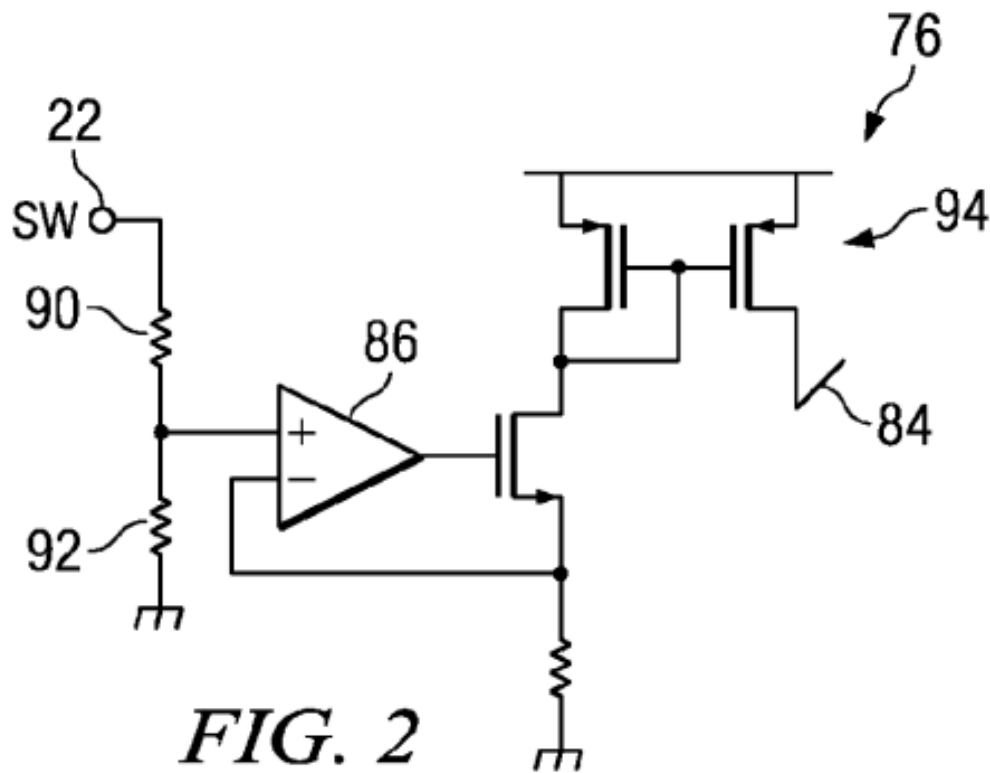
106. In my opinion, a POSITA would recognize that the input voltage sensing circuit of claim 2 would not operate in a linear fashion without additional circuitry to provide a compensating current. That is, as current flows from the switching node through the recited first resistor to the recited capacitor, the voltage

across the capacitor would necessarily increase as the capacitor “charges up” according to the equation:

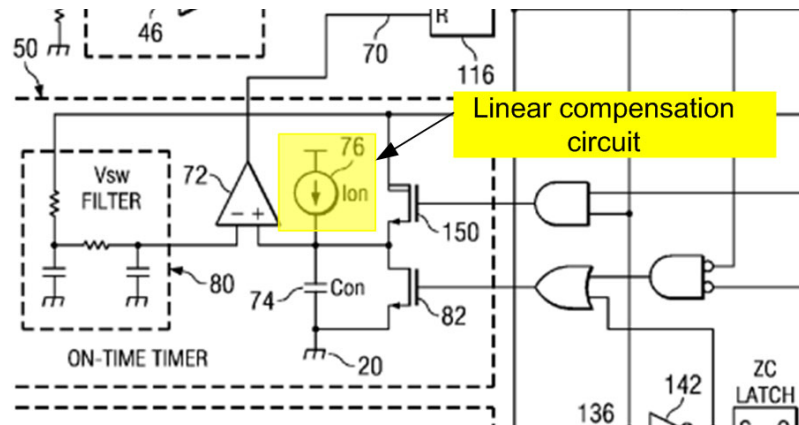
$$v_C = v_{in} \left(1 - e^{-t/\tau}\right) \text{ where } \tau = RC$$

As the capacitor charges up, the voltage across the capacitor increases in a nonlinear (exponential) fashion per the equation above. Thus, without compensating circuitry, the input voltage sensing signal would not vary linearly with the input voltage.

107. As shown in Fig. 4, Tateishi addresses this by adding a variation of the voltage follower amplifier 86 and current mirror 94 of the current-source embodiment described and disclosed in Fig. 2 (shown below). As explained with respect to Fig. 2, amplifier 86 is connected as a voltage follower, buffering the voltage at its positive terminal in the voltage follower amplifier 86 (at its negative terminal). EX1007, ¶50. By connecting the output of the amplifier 86 to ground through a resistor, “the amplifier 86 ... produces an output current that is proportional to the voltage at the switching node 22.” EX1007, ¶50. Because the current from the amplifier 86 is mirrored by a current mirror 94, the output of the current mirror is likewise proportional to the voltage at the switching node (which is connecting to the input voltage during the on-time). EX1007, ¶50.



108. In my opinion, a POSITA would understand that in the current-source embodiment of Fig. 4, the input to the voltage follower amplifier 86 is the voltage across capacitor Con 74. Therefore, the current mirror 94 produces an output current that is proportional to voltage across capacitor Con 74. Accordingly, in my opinion, a POSITA would understand that the current-mirror output current would necessarily increase as capacitor Con 74 charges up, thereby linearly compensating for the reduced current flowing through the first resistor due to charging of capacitor Con 74. In my opinion, a POSITA would see that Tateishi anticipates claim 3. *See, e.g.*, VI.A.2.c, Fig. 3 (below).



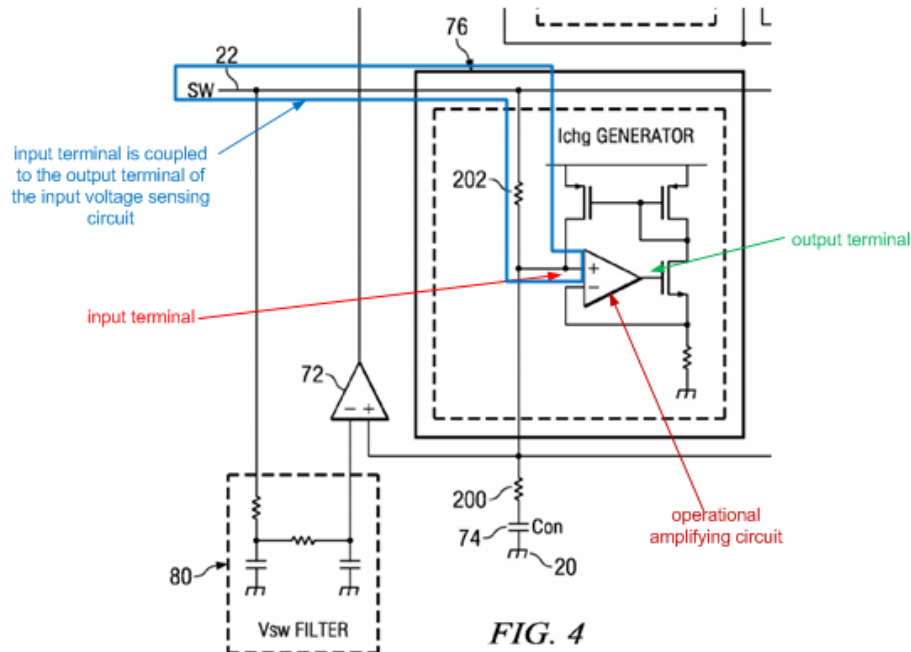
4. Claim 4

- a. Limitation 4[PRE]: The step-down regulator of claim 3, wherein the linear current compensation circuit comprises:

109. Claim 4 depends from claim 3. In my opinion, as demonstrated above, a POSITA would see that Tateishi anticipates claim 3. *See* VI.A.3.

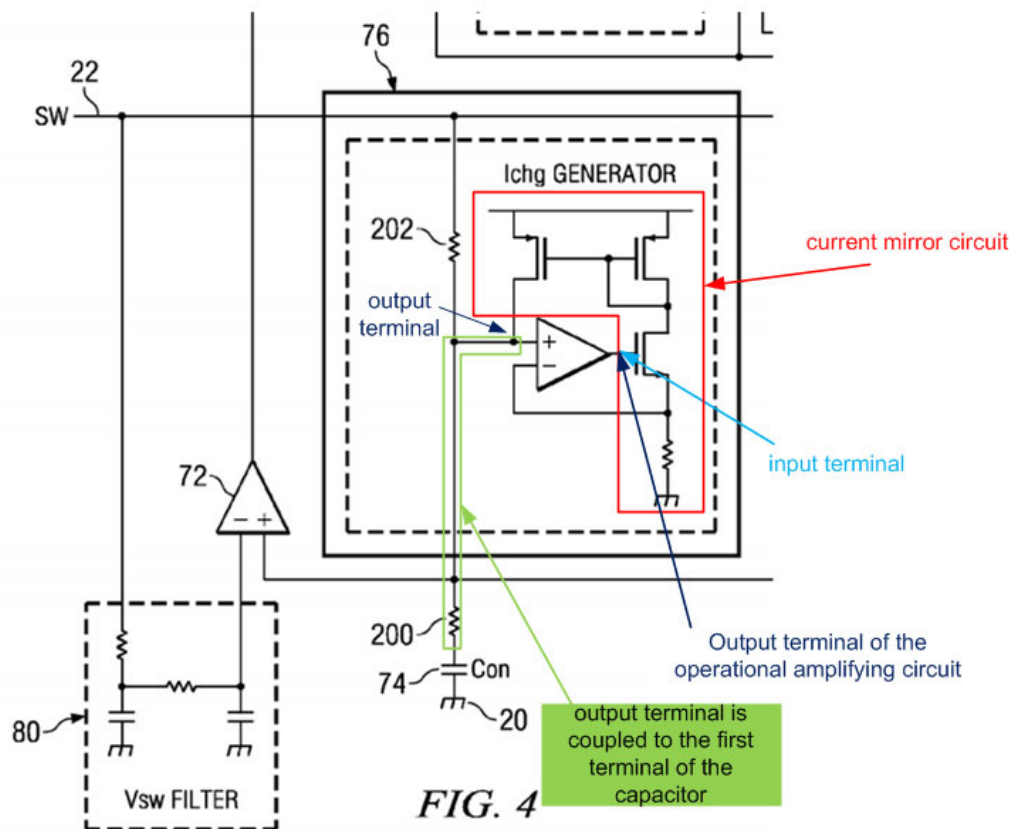
- b. Limitation 4[A]: an operational amplifying circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal; and

110. Limitation 4[A] recites the linear current compensation circuit comprising an operational amplifying circuit having an input terminal coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal of limitation 1[B2]. Tateishi (in particular, Tateishi's voltage follower amplifier 86) discloses this limitation. *See, e.g.,* EX1007, Fig. 4 below (cropped and annotated).



- c. **Limitation 4[B]: a current mirror circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the operational amplifying circuit, and the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current.**

111. Limitation 4[B] recites the linear current compensation circuit comprising a current mirror circuit having an input terminal coupled to the output terminal of the operational amplifying circuit, and an output terminal coupled to the first terminal of the capacitor to provide the linear compensation current. Tateishi discloses this limitation illustrated in Fig. 4 shown below (cropped and annotated). It is my opinion that a POSITA would recognize the three MOSFETs shown in Fig. 4 implement a current mirror circuit and thus Tateishi anticipates claim 4.



5. Claim 9

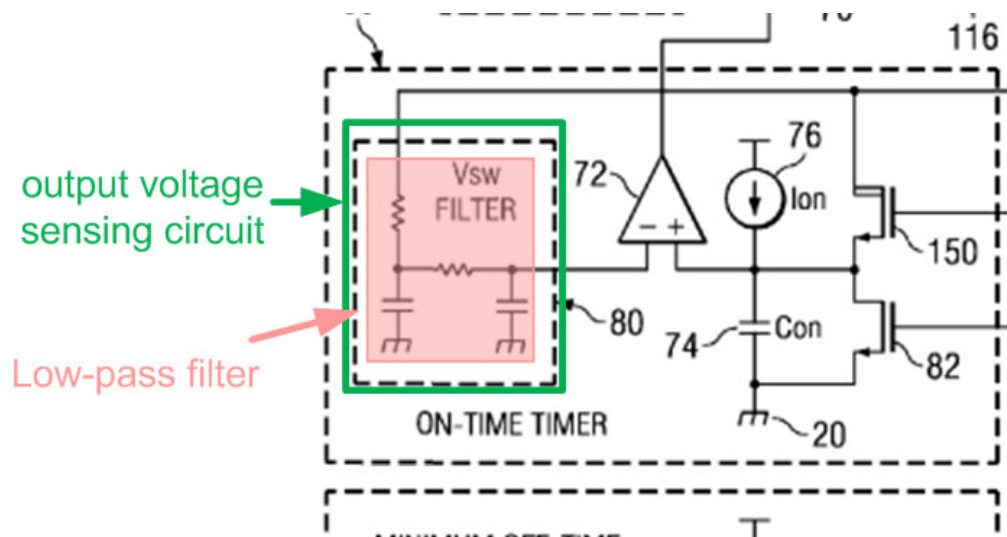
a. Limitation 9[PRE]: The step-down regulator of claim 1, wherein

112. Claim 9 depends from claim 1. In my opinion, as demonstrated above, a POSITA would see that Tateishi anticipates claim 1. *See* VI.A.1.

b. Limitation 9[A]: the output voltage sensing circuit comprises a low-pass filter.

113. Limitation 9[A] recites the output voltage sensing circuit comprising a low-pass filter. Tateishi discloses this limitation. In particular, Tateishi discloses

generating the average voltage of the switching node 22 across an entire switching period by a Vsw low-pass filter 80. *See, e.g.*, EX1007, ¶49 (“The Vsw filter 80 is a low pass filter that may be implemented in any desired manner, such as the two resistor, two capacitor example shown in FIG. 3, or with more or less resistors or capacitors, or any other desired implementation including even active filters. The time constant of the Vsw filter 80 is selected to be large enough against the switching period of the DC to DC buck converter 10 to achieve a stable voltage for the comparator 72.”), ¶44 (“the average Voltage of the Switching node 22 across an entire switching period as generated by the Vsw filter 80”), Fig. 3. In my opinion, a POSITA would see that Tateishi anticipates claim 9.



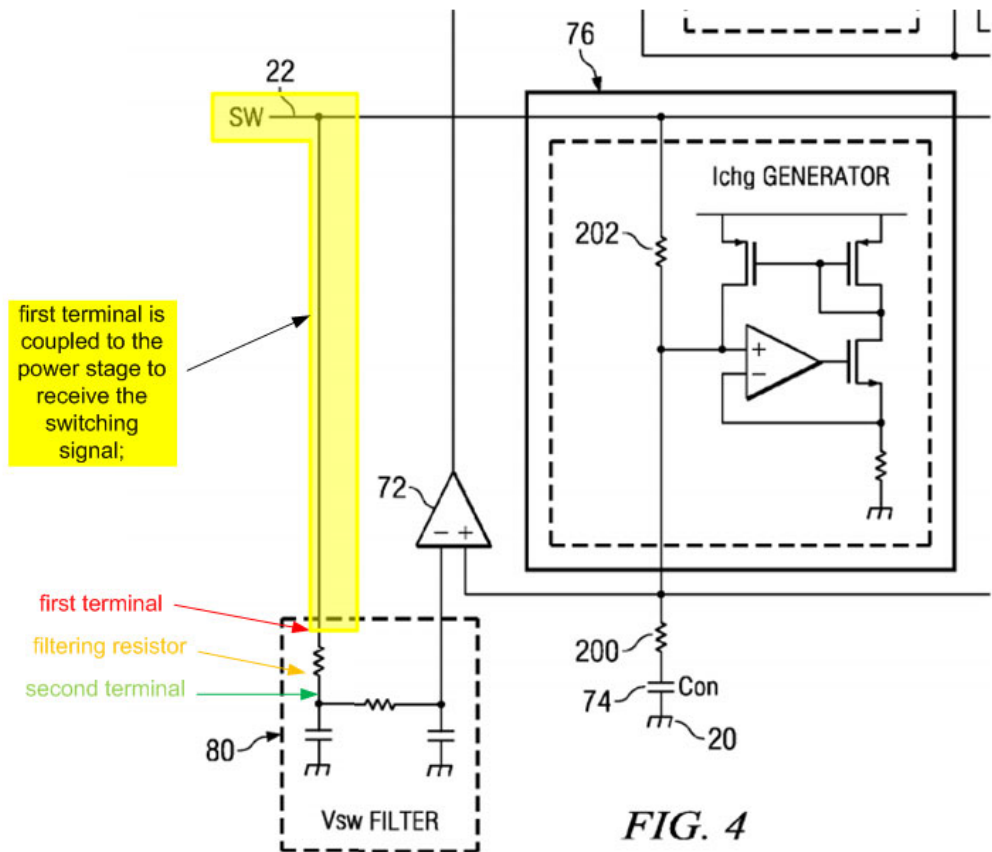
6. Claim 10

- a. Limitation 10[PRE]: The step-down regulator of claim 9, wherein the low-pass filter comprises:**

114. Claim 10 depends from claim 9. In my opinion, a POSITA would see that Tateishi anticipates claim 9. *See* VI.A.5. Low-pass filters are well known in the art, implemented both actively and passively. A POSITA would know that there are many ways to implement a passive low-pass filter—the simplest being a series resistor followed by a capacitor to ground.

b. **Limitation 10[A]: a filtering resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the power stage to receive the switching signal; and**

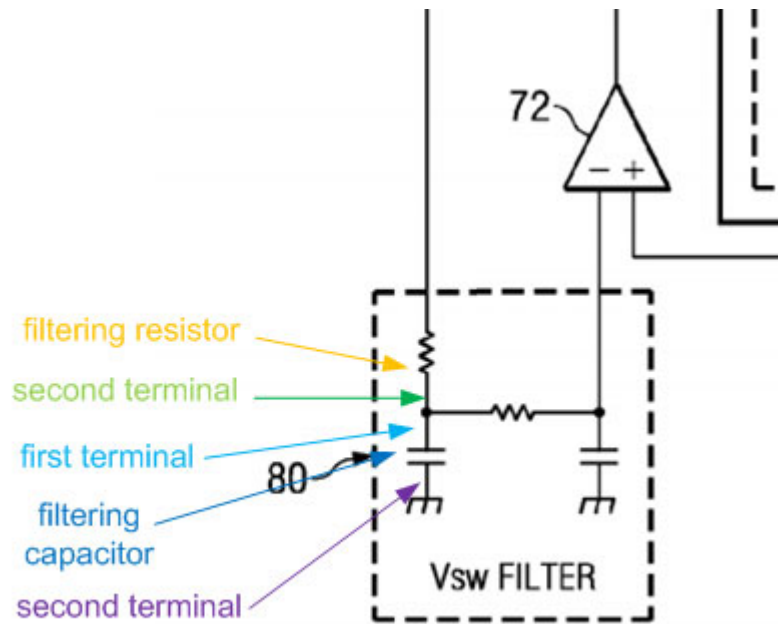
115. Limitation 10[A] recites the low-pass filter comprising a filtering resistor coupled to the power stage to receive the switching signal. Tateishi discloses this limitation. *See, e.g.,* EX1007, Fig. 4 (a portion of which is reproduced and annotated below). *See also,* EX1007, ¶49 (“The Vsw filter 80 is a low pass filter that may be implemented in any desired manner, such as the two resistor, two capacitor example shown in FIG. 3, or with more or less resistors or capacitors, or any other desired implementation including even active filters.”).



- c. **Limitation 10[B]: a filtering capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the filtering resistor and provides the output voltage sensing signal, and the second terminal is grounded.**

116. Limitation 10[B] recites the low-pass filter comprising a filtering capacitor coupled between the filtering resistor and ground, the capacitor providing the output voltage sensing signal. Tateishi discloses this limitation. *See, e.g.,* EX1007, Fig. 4 (a portion of which is reproduced and annotated below, showing a capacitor coupled to the resistor through another resistor).

117. See also, EX1007, ¶49 (“The Vsw filter 80 is a low pass filter that may be implemented in any desired manner, such as the two resistor, two capacitor example shown in FIG. 3, or with more or less resistors or capacitors, or any other desired implementation including even active filters.”). In my opinion, a POSITA would see that Tateishi anticipates claim 10.



7. Claim 11

a. Limitation 11[PRE]: A pseudo constant on time control circuit for a step-down regulator, comprising:

118. Limitation 11[PRE] recites a pseudo constant on time control circuit for a step-down regulator. To the extent the preamble is limiting, Tateishi discloses this limitation. See, e.g., EX1007, ¶5 (“Various apparatuses, methods and systems

for a DC-DC converter with a pseudo constant switching frequency are disclosed herein”). *See also* VI.A.1.a and VI.A.1.b.

b. **Limitation 11[A]: an on-time generator comprising:**

119. Tateishi discloses this limitation. *See, e.g.*, VI.A.1.c.

c. **Limitation 11[B1]: an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;**

120. Tateishi discloses this limitation. *See, e.g.*, VI.A.1.d.

d. **Limitation 11[B2]: an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and**

121. Tateishi discloses this limitation. *See, e.g.*, VI.A.1.e.

- e. Limitation 11[B3]: a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;

122. Tateishi discloses this limitation. *See, e.g.*, VI.A.1.f.

- f. Limitation 11[C]: a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and

123. Tateishi discloses this limitation. *See, e.g.*, VI.A.1.g.

- g. Limitation 11[D]: a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal.

124. Tateishi discloses this limitation. *See, e.g.*, VI.A.1.h.

8. Claim 12

- a. Limitation 12[PRE]: The pseudo constant on time control circuit of claim 11, wherein the input voltage sensing circuit comprises:

125. Claim 12 depends from claim 11. Tateishi anticipates claim 11. *See*
VI.A.7.

- b. **Limitation 12[A]: a first resistor having a first terminal and a second terminal, wherein the first terminal is configured to receive the switching signal;**

126. Tateishi discloses this limitation. *See, e.g.*, VI.A.2.b.

- c. **Limitation 12[B]: a capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first resistor and provides the input voltage sensing signal, and the second terminal is grounded; and**

127. Tateishi discloses this limitation. *See, e.g.*, VI.A.2.c.

- d. **Limitation 12[C]: a switch having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the logic control circuit to receive the control signal, the first terminal is coupled to the first terminal of the capacitor, the second terminal is grounded.**

128. Tateishi discloses this limitation. *See, e.g.*, VI.A.2.c. In my opinion, a POSITA would see that Tateishi anticipates claim 11.

9. **Claim 13**

- a. **Limitation 13[PRE]: The pseudo constant on time control circuit of claim 12, wherein**

129. Claim 13 depends from claim 12. In my opinion, a POSITA would see that Tateishi anticipates claim 12. *See* VI.A.8.

- b. **Limitation 13[A]: the input voltage sensing circuit further comprises a linear current compensation circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, and wherein based on the input voltage sensing signal, the linear current compensation circuit provides a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage.**

130. Tateishi discloses this limitation. See, *e.g.*, VI.A.3.b. In my opinion, a POSITA would see that Tateishi anticipates claim 13.

10. **Claim 14**

- a. **Limitation 14[PRE]: The pseudo constant on time control circuit of claim 13, wherein the linear current compensation circuit comprises:**

131. Claim 14 depends from claim 13. In my opinion, a POSITA would see that Tateishi anticipates claim 13. See VI.A.9.

- b. **Limitation 14[A]: an operational amplifying circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal; and**

132. Tateishi discloses this limitation. See, *e.g.*, VI.A.4.b.

- c. **Limitation 14[B]: a current mirror circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the operational amplifying circuit, and the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current.**

133. Tateishi discloses this limitation. *See, e.g.*, VI.A.4.b. In my opinion, a POSITA would see that Tateishi anticipates claim 14.

11. Claim 17

a. Limitation 17[PRE]: The pseudo constant on time control circuit of claim 11, wherein

134. Claim 17 depends from claim 11. In my opinion, a POSITA would see that Tateishi anticipates claim 11. *See* VI.A.7.

b. Limitation 17[A]: the output voltage sensing circuit comprises a low-pass filter.

135. Tateishi discloses this limitation. *See, e.g.*, VI.A.5.b. In my opinion, a POSITA would see that Tateishi anticipates claim 17.

12. Claim 18

a. Limitation 18[PRE]: A step-down regulator, comprising:

136. Limitation 18[PRE] recites a step-down regulator. To the extent the preamble is limiting, Tateishi discloses this limitation. *See, e.g.*, EX1007, ¶5 (“Various apparatuses, methods and systems for a DC to DC converter with a pseudo constant switching frequency are disclosed herein”). *See also* VI.A.1.a, VI.A.1.b.

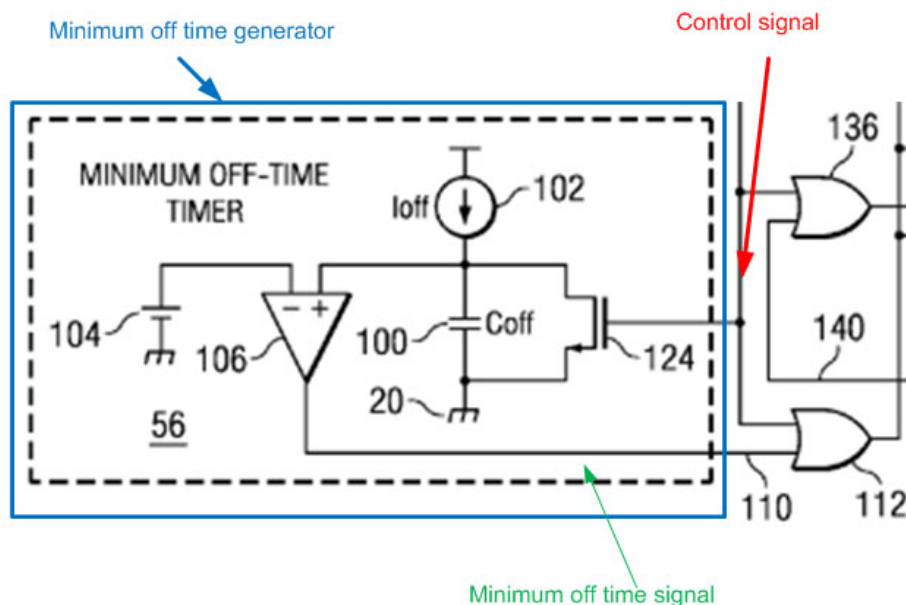
- b. **Limitation 18[A]: an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;**

137. Tateishi discloses this limitation. See, *e.g.*, VI.A.1.c, VI.A.1.d, VI.A.1.e, and VI.A.1.f.

- c. **Limitation 18[B]: a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;**

138. Limitation 18[B] recites a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal. Tateishi (in particular, Tateishi's minimum off-time timer 56) discloses this limitation. See, *e.g.*, EX1007, ¶51 ("The output 122 of the SR latch 116 also drives a discharging transistor 124 in the minimum off-time timer 56, discharging the capacitor Coff 100 to ground 20 when the on-time begins."), ¶52 ("the on-time termination signal 70 is connected to the Reset input of the SR latch 116, turning off the output 122 of the SR latch 116. This turns off the high side switch 12. This also turns off the discharging transistor 124 in the minimum off-time timer 56, allowing the capacitor Coff 100 to be charged by the reference current source 102."), ¶51 ("The minimum off-time may be detected when a capacitor Coff 100 is charged by a reference current source 102 to match a reference voltage 104. After the minimum

56”), Fig. 3 below (cropped and annotated).



139. Thus, Tateishi's minimum off-time timer 56 receives control signal 122 and generates a minimum off-time signal 110.

- d. Limitation 18[C]: a comparator configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to receive a reference signal, and wherein based on the feedback signal and the reference signal, the comparator generates a comparison signal;

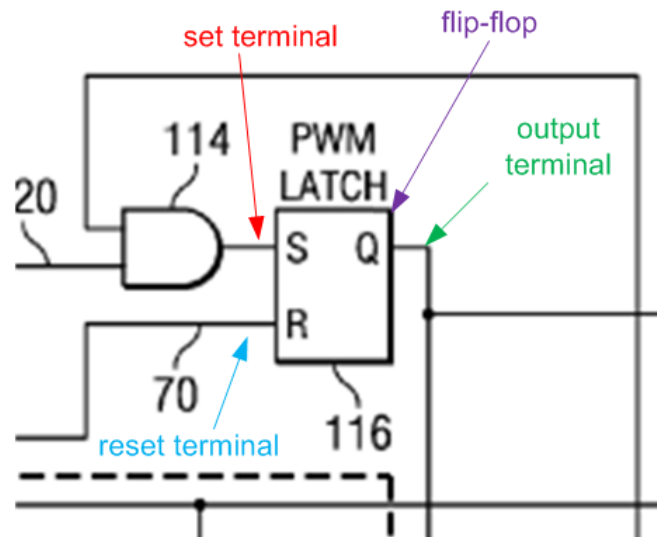
140. Tateishi discloses this limitation. *See, e.g.*, VI.A.1.g.

- e. **Limitation 18[D]: an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal, wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal;**

141. Limitation 18[D] recites an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal, wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal. Tateishi (in particular, Tateishi's AND gate 114) discloses this limitation. See, e.g., EX1007, ¶51 ("After the minimum off-time, a comparator 106 asserts the output 110 of the minimum off-time timer 56 which passes through an OR gate 112 to an AND gate 114 at the Set input of an SR latch 116. The output 120 of the loop comparator 34 is combined with the output 110 of the minimum off-time timer 56 in the AND gate 114 at the Set input of the SR latch 116."), Fig 3 below (cropped and annotated).

142. As shown in Fig. 3, the output 110 of the minimum off-time circuit is coupled to AND gate 114 through OR gate 112, and the output 120 of the loop comparator 34 is also coupled to AND gate 114.

and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal of limitation 18[B]. Tateishi (in particular, Tateishi's SR flip-flop 116) discloses this limitation. See, e.g., ("the output 110 of the minimum off-time timer 56 which passes through an OR gate 112 to an AND gate 114 at the Set input of an SR latch 116. The output 120 of the loop comparator 34 is combined with the output 110 of the minimum off-time timer 56 in the AND gate 114 at the [Set] input of the SR latch 116... The output 122 of the SR latch 116 is thus asserted, turning on the high side switch 12 and turning off the low side switch 14."), Fig 3 (a portion of which is reproduced and annotated below).



144. Thus, the Set (S) input of Tateishi's SR flip-flop 116 is coupled through AND gate 114 to the output of the minimum off-time timer 56, the Reset

(R) input is coupled to the on-time termination signal 70 of Tateishi's on-time circuit 50, and the SR flip-flop 116 produces 122, the control signal recited in limitation 18[B].

- g. **Limitation 18[F]: a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.**

145. Tateishi discloses this limitation. *See, e.g.,* VI.A.1.i. In my opinion, a POSITA would understand that Tateishi anticipates claim 18.

B. Ground 2: Claims 5, 7-8, and 15 are rendered obvious by Tateishi

1. Claim 5

- a. **Limitation 5[PRE]: The step-down regulator of claim 4, wherein the current mirror circuit comprises:**

146. Claim 5 depends from claim 4. In my opinion, a POSITA would see that Tateishi anticipates claim 4. *See* VI.A.4.

- b. **Limitation 5[A]: a current mirror having an input terminal and an output terminal, wherein the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current;**

147. Limitation 5[A] recites the current mirror circuit comprising a current mirror. Tateishi (in particular, Tateishi's current mirror 94) discloses this limitation. *See, e.g.,* EX1007, Fig. 4 below (cropped and annotated).

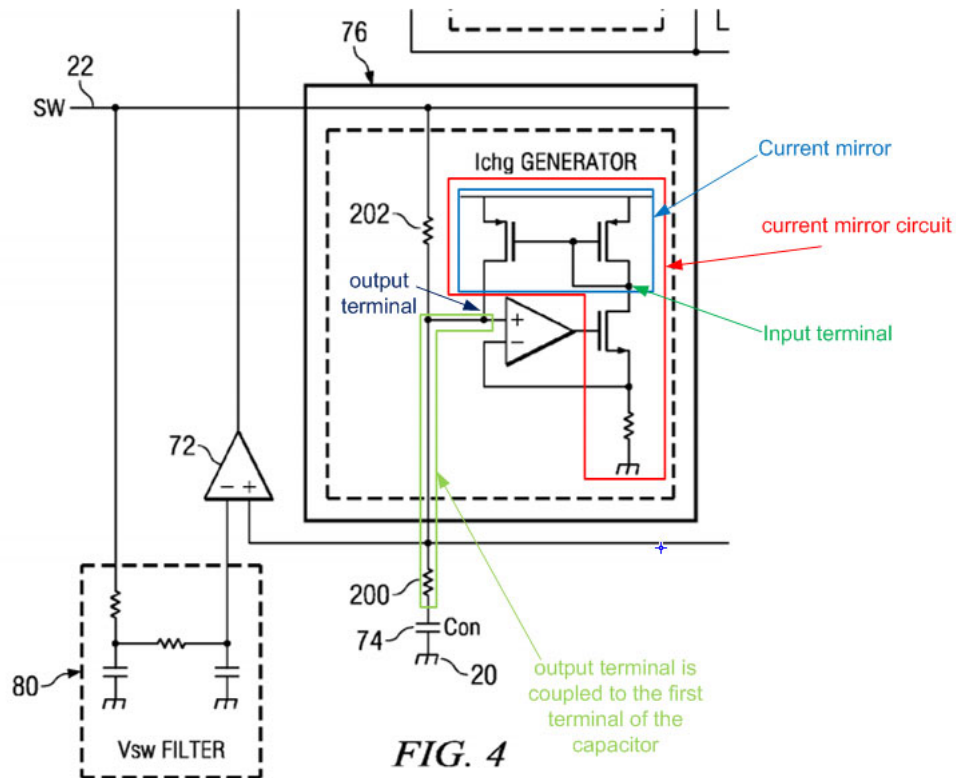


FIG. 4

- c. **Limitation 5[B]: a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying circuit, the first terminal is coupled to the input terminal of the current mirror; and**

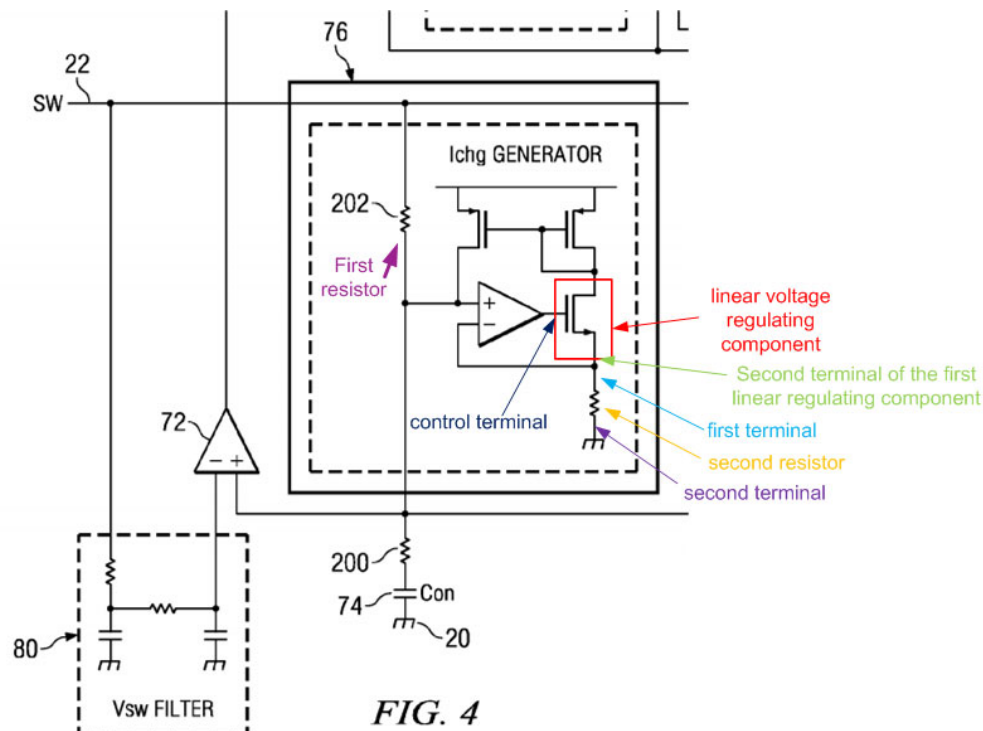
148. Limitation 5[B] recites the current mirror circuit comprising a first linear voltage regulating component having a control terminal coupled to the output terminal of the operational amplifying circuit and a first terminal coupled to the input terminal of the current mirror. Tateishi discloses this limitation. *See, e.g.,* EX1007, Fig. 4 below (cropped and annotated). That is, Tateishi discloses a MOSFET (first linear voltage regulating component) whose gate (control terminal)



- d. Limitation 5[C]: a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first resistor and the second resistor have the same resistance.

149. Limitation 5[C] recites the current mirror circuit comprising a second resistor coupled between the first linear voltage regulating component and ground, the first resistor and the second resistor having the same resistance. While Tateishi does not explicitly state that the two resistors have the same resistance, Tateishi

does state that the current generated by Ichg Generator is proportional to $v_{in} - v_{on1}$. See EX1007, ¶62. Therefore, the transconductance I_{chg}/v_c must be $1/R_{202}$. A POSITA would know that the best way to achieve this is to apply the unit matching principle (See CMOS pp 56-62) and set the two resistors equal and set the gain of the current mirror to unity. See ¶¶79, 80. Tateishi discloses this limitation and/or renders this limitation obvious. See, e.g., EX1007, Fig. 4 (reproduced and annotated below).



150. In my opinion, a POSITA would find claim 5 to be obvious over Tateishi.

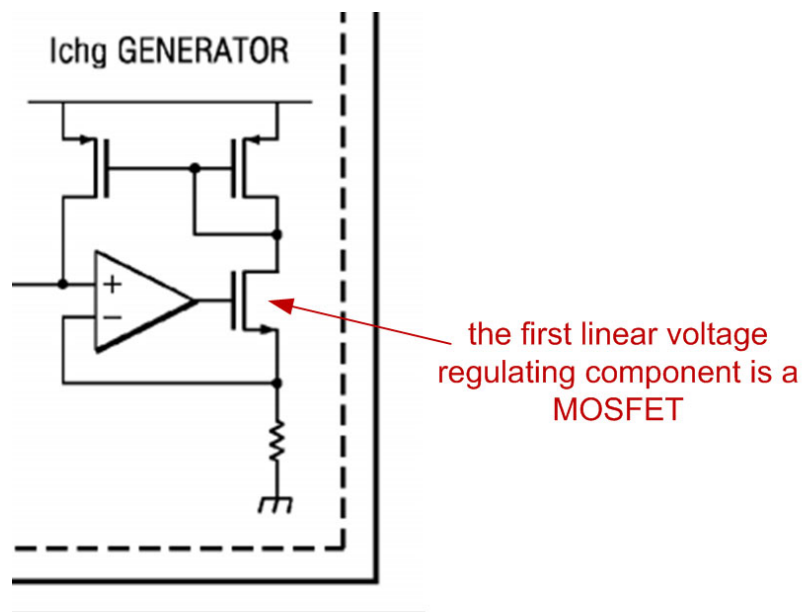
2. Claim 7

a. Limitation 7[PRE]: The step-down regulator of claim 5, wherein

151. Claim 7 depends from claim 5. In my opinion, a POSITA would understand that Tateishi renders claim 5 obvious. *See* VI.B.1.

b. Limitation 7[A]: the first linear voltage regulating component is a MOSFET or a BJT.

152. Limitation 7[A] recites the first linear voltage regulating component being a MOSFET or a BJT. Tateishi discloses this limitation. *See, e.g.,* EX1007, Fig. 4 below (cropped and annotated) illustrating the transistor as a MOSFET. In my opinion, a POSITA would find claim 7 to be obvious over Tateishi.



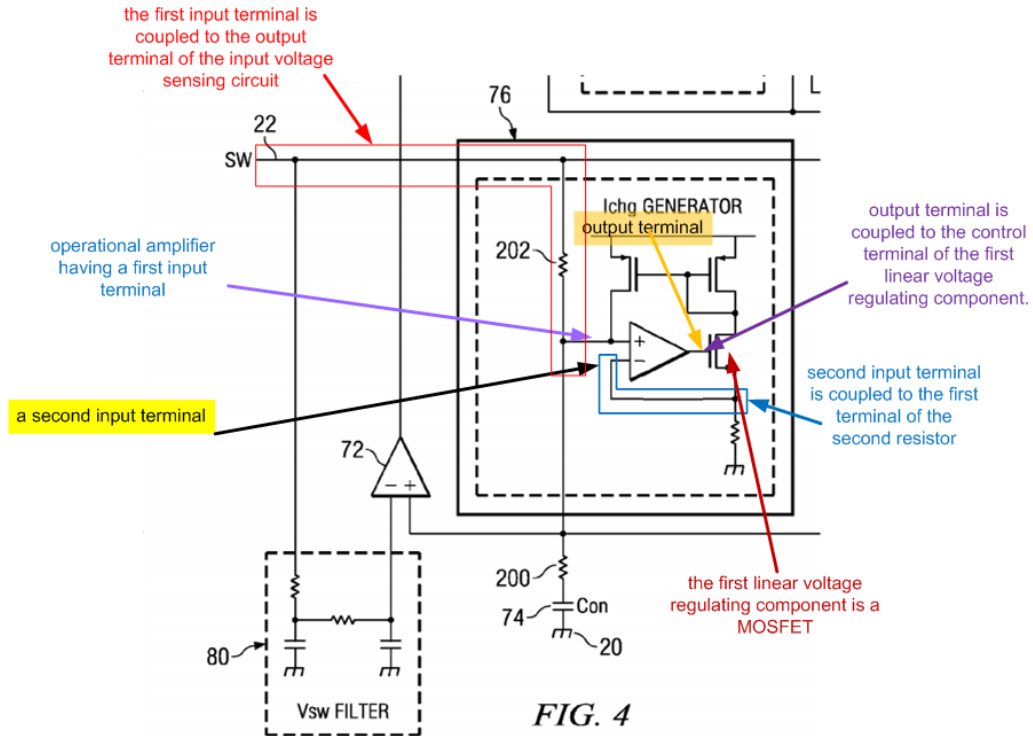
3. Claim 8

a. Limitation 8[PRE]: The step-down regulator of claim 5, wherein

153. Claim 8 depends from claim 5. In my opinion, a POSITA would understand that Tateishi renders claim 5 obvious. *See* VI.B.1.

- b. **Limitation 8[A]: the operational amplifying circuit comprises an operational amplifier having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the first terminal of the second resistor, and the output terminal is coupled to the control terminal of the first linear voltage regulating component.**

154. Limitation 8[A] recites the operational amplifying circuit comprises an operational amplifier having a first input terminal coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, a second input terminal coupled to the first terminal of the second resistor, and an output terminal coupled to the control terminal of the first linear voltage regulating component. Tateishi (in particular, Tateishi's voltage follower amplifier 86) discloses this limitation. *See, e.g.*, EX1007, Fig. 4 below (cropped and annotated). In my opinion, a POSITA would find that claim 8 is obvious over Tateishi.



4. Claim 15

- a. Limitation 15[PRE]: The pseudo constant on time control circuit of claim 14, wherein the current mirror circuit comprises:

155. Claim 15 depends from claim 14. In my opinion, a POSITA would see that Tateishi anticipates claim 14. *See* VI.A.10.

- b. Limitation 15[A]: a current mirror having an input terminal and an output terminal, wherein the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current;

156. Tateishi discloses this limitation. *See, e.g.,* VI.B.1.b.

- c. **Limitation 15[B]: a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying circuit, the first terminal is coupled to the input terminal of the current mirror; and**

157. Tateishi discloses this limitation. *See, e.g.*, VI.B.1.c.

- d. **Limitation 15[C]: a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first resistor and the second resistor have the same resistance.**

158. Tateishi discloses this limitation and/or renders this limitation obvious. *See, e.g.*, VI.B.1.d. In my opinion, a POSITA would find that claim 15 is obvious over Tateishi.

VII. CONCLUDING STATEMENT

159. Under penalty of perjury, all statements made herein of my own knowledge are true, and I believe that all statements made herein on information and belief to be true. I have been warned and I am aware that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code. In signing this Declaration, I understand that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in the case and that cross-

examination will take place in the United States. If cross examination is required of me, I undertake to appear within the United States during the time allotted for cross-examination, and within the limits of my ability so to do. I declare under penalty of perjury that the foregoing is true and correct.

Executed on July 23, 2024

A handwritten signature in cursive script, appearing to read "Douglas Holberg", is written over a horizontal line.

Douglas Holberg