

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

Petitioner

v.

MONOLITHIC POWER SYSTEMS, INC.

Patent Owner

IPR2024-01158
Patent No. 9,041,377

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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Petitioner's Exhibit List¹

Exhibit No.	Description
1001	U.S. Patent No. 9,041,377 B2 to Wang et al.
1002	Prosecution History of U.S. 9,041,377
1003	Declaration of Doug Holberg
1004	<i>Curriculum Vitae</i> of Doug Holberg
1005	U.S. Patent No. 8,476,887 B2 to Tateishi et al.
1006	Assignment of U.S. Patent No. 9,041,377 from Chengdu Monolithic Power Systems Co., Ltd. to Monolithic Power Systems, Inc.
1007	U.S. Patent Publication No. 2009/0140708 A1 to Tateishi et al.
1008	U.S. Patent No. 6,147,478 to Skelton et al.
1009	Reed Stipulation Regarding Invalidity Contentions (<i>Sotera</i> Stipulation)
1010	Nengda Stipulation Regarding Invalidity Contentions (<i>Sotera</i> Stipulation)
1011	U.S. Patent No. 7,439,721 B2 to Weng et al.
1012	Paul Horowitz and Winfield Hill, “Art of Electronics” (Second Edition) (“AOE”)
1013	LM2696 3A, Constant On Time Buck Regulator (annotated)

¹ Petitioner cites to exhibits' original page numbers. Unless otherwise noted, all emphasis in any quoted material has been added.

Exhibit No.	Description
1014	TI Application report: “Adaptive Constant On-Time (D-CAP™) Control Study in Notebook Applications” (“DCAP”)
1015	Allen, Philip E., and Douglas R. Holberg. “CMOS Analog Circuit Design” (Second Edition) (“CMOS”)

Claim Appendix

Claim Limitation	Claim Language
1[PRE]	1. A step-down regulator, comprising:
1[A]	a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:
1[B1]	an on-time generator comprising:
1[B2]	an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;
1[B3]	an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and
1[B4]	a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;
1[C]	a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and

	to generate an output signal in accordance with the feedback signal; and
1[D]	a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and
1[E]	a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.
2[PRE]	2. The step-down regulator of claim 1, wherein the input voltage sensing circuit comprises:
2[A]	a first resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the power stage to receive the switching signal;
2[B]	a capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first resistor and provides the input voltage sensing signal, and the second terminal is grounded; and
2[C]	a switch having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the logic control circuit to receive the control signal, the first terminal is coupled to the first terminal of the capacitor, and the second terminal is grounded.
3	3. The step-down regulator of claim 2, wherein the input voltage sensing circuit further comprises a linear current compensation circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, and wherein based on the input voltage sensing signal, the linear current

	compensation circuit provides a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage.
4[PRE]	4. The step-down regulator of claim 3, wherein the linear current compensation circuit comprises:
4[A]	an operational amplifying circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal; and
4[B]	a current mirror circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the operational amplifying circuit, and the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current.
5[PRE]	5. The step-down regulator of claim 4, wherein the current mirror circuit comprises:
5[A]	a current mirror having an input terminal and an output terminal, wherein the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current;
5[B]	a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying circuit, the first terminal is coupled to the input terminal of the current mirror; and
5[C]	a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is

	grounded, further wherein the first resistor and the second resistor have the same resistance.
6	6. The step-down regulator of claim 5, wherein the operational amplifying circuit comprises: a current source having an input terminal and an output terminal, wherein the input terminal is configured to receive a power supply voltage; and a second linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the first terminal is coupled to the output terminal of the current source and the control terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first and second linear voltage regulating components have opposite characteristic parameters.
7	7. The step-down regulator of claim 5, wherein the first linear voltage regulating component is a MOSFET or a BJT.
8	8. The step-down regulator of claim 5, wherein the operational amplifying circuit comprises an operational amplifier having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the first terminal of the second resistor, and the output terminal is coupled to the control terminal of the first linear voltage regulating component.

9	9. The step-down regulator of claim 1, wherein the output voltage sensing circuit comprises a low-pass filter.
10[PRE]	10. The step-down regulator of claim 9, wherein the low-pass filter comprises:
10[A]	a filtering resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the power stage to receive the switching signal; and
10[B]	a filtering capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the filtering resistor and provides the output voltage sensing signal, and the second terminal is grounded.
11[PRE]	11. A pseudo constant on time control circuit for a step-down regulator, comprising:
11[A]	an on-time generator comprising:
11[B1]	an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;
11[B2]	an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and

11[B3]	a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;
11[C]	a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and
11[D]	a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal.
12[PRE]	12. The pseudo constant on time control circuit of claim 11, wherein the input voltage sensing circuit comprises:
12[A]	a first resistor having a first terminal and a second terminal, wherein the first terminal is configured to receive the switching signal;
12[B]	a capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first resistor and provides the input voltage sensing signal, and the second terminal is grounded; and
12[C]	a switch having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the logic control circuit to receive the control signal, the first terminal is coupled to the first terminal of the capacitor, the second terminal is grounded.

13	13. The pseudo constant on time control circuit of claim 12, wherein the input voltage sensing circuit further comprises a linear current compensation circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, and wherein based on the input voltage sensing signal, the linear current compensation circuit provides a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage.
14[PRE]	14. The pseudo constant on time control circuit of claim 13, wherein the linear current compensation circuit comprises:
14[A]	an operational amplifying circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal; and
14[B]	a current mirror circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the operational amplifying circuit, and the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current.
15[PRE]	15. The pseudo constant on time control circuit of claim 14, wherein the current mirror circuit comprises:
15[A]	a current mirror having an input terminal and an output terminal, wherein the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current;
15[B]	a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying

	circuit, the first terminal is coupled to the input terminal of the current mirror; and
15[C]	a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first resistor and the second resistor have the same resistance.
16[PRE]	16. The pseudo constant on time control circuit of claim 15, wherein the operational amplifying circuit comprises:
16[A]	a current source having an input terminal and an output terminal wherein the input terminal is configured to receive a power supply voltage; and
16[B]	a second linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the first terminal is coupled to the output terminal of the current source and the control terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first and second linear voltage regulating components have opposite characteristic parameters.
17[PRE]	17. The pseudo constant on time control circuit of claim 11, wherein the output voltage sensing circuit comprises a low-pass filter.
18[PRE]	18. A step-down regulator, comprising:
18[A]	an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal,

	wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;
18[B]	a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;
18[C]	a comparator configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to receive a reference signal, and wherein based on the feedback signal and the reference signal, the comparator generates a comparison signal;
18[D]	an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal, wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal;
18[E]	a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and
18[F]	a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.

I. INTRODUCTION

Pursuant to 35 U.S.C. §§311, 314(a), and 37 C.F.R. §42.100, Reed Semiconductor Corp. (“Petitioner”) respectfully requests that the Board review and cancel claims 1-5, 7-15, and 17-18 (the “Challenged Claims”) of U.S. Patent No. 9,041,377 (“the ’377 Patent”) (EX1001) as unpatentable under 35 U.S.C. §§102 and/or 103.

II. PETITION REQUIREMENTS

A. Grounds For Standing and Timeliness

Petitioner certifies that the ’377 Patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR. 37 C.F.R. §42.104(a). The ’377 Patent was filed on June 29, 2012, and issued on May 26, 2015. It is not subject to the America Invents Act (“AIA”) and has been eligible for IPR upon issuance. *See* 37 C.F.R. §42.102(a)(2). This Petition is also filed within one year of Petitioner being served an allegation of infringement of the ’377 Patent. *See* Patent Owner Mandatory Notices, *infra*.

B. Payment of Fees

Pursuant to 37 C.F.R. §§42.103(a) and 42.15(a), the required fees are submitted herewith. If additional fees are due during this proceeding, the Office is authorized to charge Deposit Account 50-1943.

C. Identification of Challenge and Relief Requested

Pursuant to 37 C.F.R. §§ 42.22(a) and 42.104(b), Petitioner requests a final written decision that the Challenged Claims are unpatentable in view of the analysis below. *See* §VII, *infra* (incorporated here). The effective filing date of the '377 Patent, for purposes of this Petition only, is assumed to be June 30, 2011 (the “Effective Filing Date”). *See* §III, *infra* (incorporated here). The following is the prior art that anticipates and/or renders obvious the Challenged Claims.

Exhibit	Description	Operative Date
1007	U.S. Patent Publication No. 2009/0140708 (“Tateishi”)	June 4, 2009

Tateishi is prior art under (pre-AIA) §102(b) because it was published more than one year before the earliest effective filing date of the '377 Patent. Tateishi issued as U.S. Patent No. 8,476,887 (“Tateishi Patent”) on July 2, 2013. *See* EX1005. The Tateishi Patent is also prior art under (pre-AIA) §102(e) because it was filed (February 6, 2009) prior to the earliest effective filing date of the claimed invention.

Petitioner requests cancellation of the Challenged Claims on the following grounds:

Ground	Claims	Description
1	1-4, 9-14, and 17-18	Anticipated under §102 by Tateishi and/or the Tateishi Patent.
2	5, 7-8, and 15	Rendered obvious under §103 by Tateishi and/or the Tateishi Patent.

III. SUMMARY OF THE '377 PATENT

The '377 Patent issued on May 26, 2015, from Patent Application Serial No. 13/538,815 (EX1002 at 8-38) (“the '815 Appl.”), filed on June 29, 2012, by Chengdu Monolithic Power Systems Co., Ltd. The '377 Patent claims priority to Chinese Patent Application No. 201110181295.3, filed on June 30, 2011. For purposes of this proceeding and without conceding the issue, Petitioner assumes all Challenged Claims of the '377 Patent have a priority date of June 30, 2011, and that they were effectively filed as of that date. The '377 Patent was assigned to Patent Owner on January 30, 2024. *See* EX1006.

A. Overview of the '377 Patent

The '377 patent is directed to switch-mode DC-DC voltage converters having pseudo constant-on-time (PCOT) control circuits that control their high-side and low-side switches. EX1001, 4:42-45, 8:32-34, FIG. 11; EX1003, ¶66. As explained in the BACKGROUND section, in PCOT control, the on time T_{on} of the regulator is proportional to the ratio of the output voltage V_{out} to the input voltage V_{in} .

EX1001, 1:55-57; EX1003, ¶66. Prior-art step-down regulators included an output voltage pin VOUT to receive Vout. EX1001, 2:11-14, FIG. 1; EX1003, ¶66. In contrast, the disclosed PCOT control circuit receives information of Vin and Vout from (a) the switching signal SW of the step-down regulator and (b) the control signal Q. EX1001, 7:42-59, FIG. 2; EX1003, ¶66.

In particular, the '377 patent discloses an input voltage sensing circuit A that provides an input voltage sensing signal, an output voltage sensing circuit B that provides an output voltage sensing signal, and a comparator COMP that compares the two sensing signals. EX1001, 4:46-48, FIG. 2; EX1003, ¶67. The input voltage sensing circuit A receives the switching signal SW and the control signal Q and provides a linear ramping signal, where the ramping rate is given by the charging current, which is proportional to Vin. EX1001, 6:59-7:34; EX1003, ¶67.

The output voltage sensing circuit B receives the switching signal SW and provides a low-pass filtered (i.e., averaged) version of SW as the output voltage sensing signal. EX1001, 5:4-13; EX1003, ¶68. As can be seen in FIG. 12 (reproduced below), when the control signal Q is a logical high (Q=1), the input voltage sensing signal S11 begins to ramp up until it reaches the output voltage sensing signal S12, at which time the on-time signal S1 causes the control signal Q

to become logical low ($Q=0$). EX1001, 8:42-58, Fig. 12 (reproduced below); EX1003, ¶68.

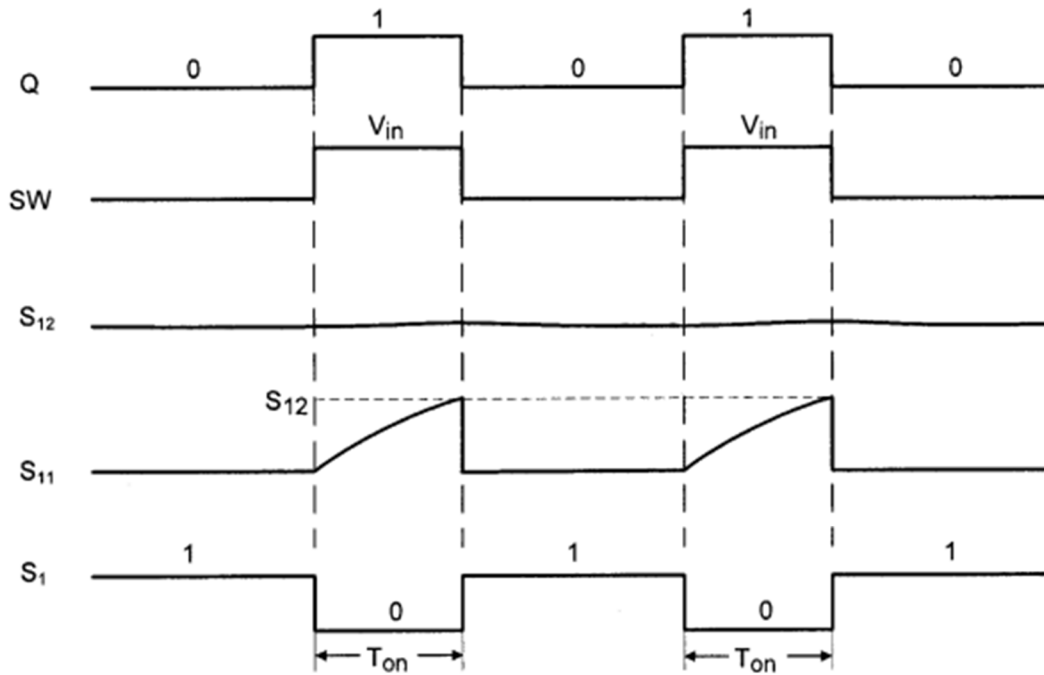


FIG. 12

Because the ramping rate of S₁₁ is proportional to V_{in} , and because the average value of SW is V_{out} , the on-time of the high-side switch is, thus, proportional to V_{out}/V_{in} . EX1003, ¶69.

B. Prosecution History

During prosecution of Application No. 13/538,815 (which issued as the '377 Patent), no Information Disclosure Statement was submitted.

The Examiner cited to U.S. Patent Publication No. 2010/0134080 (“Ouyang”), in the singular Office Action issued, having a notification date of August 14, 2014. In the Office Action of August 14, 2014, the Ouyang reference was used by the patent Examiner in a 35 USC §102 rejection of independent claims 1 and 12. The Examiner asserted that claims 2-11 and 13-20 included allowable subject matter in the Office Action of August 14, 2014.

Patent Owner amended the claims to incorporate allowable subject matter from claim 2 into claim 1 and incorporate allowable subject matter from claim 13 into claim 12, and cancelled claims 2 and 13.

A notice of allowance was issued on January 22, 2015, and U.S. Patent Application No. 13/538,815 issued as U.S. Patent No. 9,041,377 B2 on May 26, 2015.

IV. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) in the field of the ’377 Patent, as of its earliest possible filing date of June 30, 2011, would have been someone knowledgeable about and familiar with step-down regulator technology that is pertinent to the ’377 Patent. A POSITA would have had a bachelor’s degree in Electrical Engineering or equivalent training, and approximately two years of experience working in the field of step-down regulators or related technologies. Lack

of work experience can be remedied by additional education, and vice versa. EX1003, ¶¶18-19.

V. CLAIM CONSTRUCTION

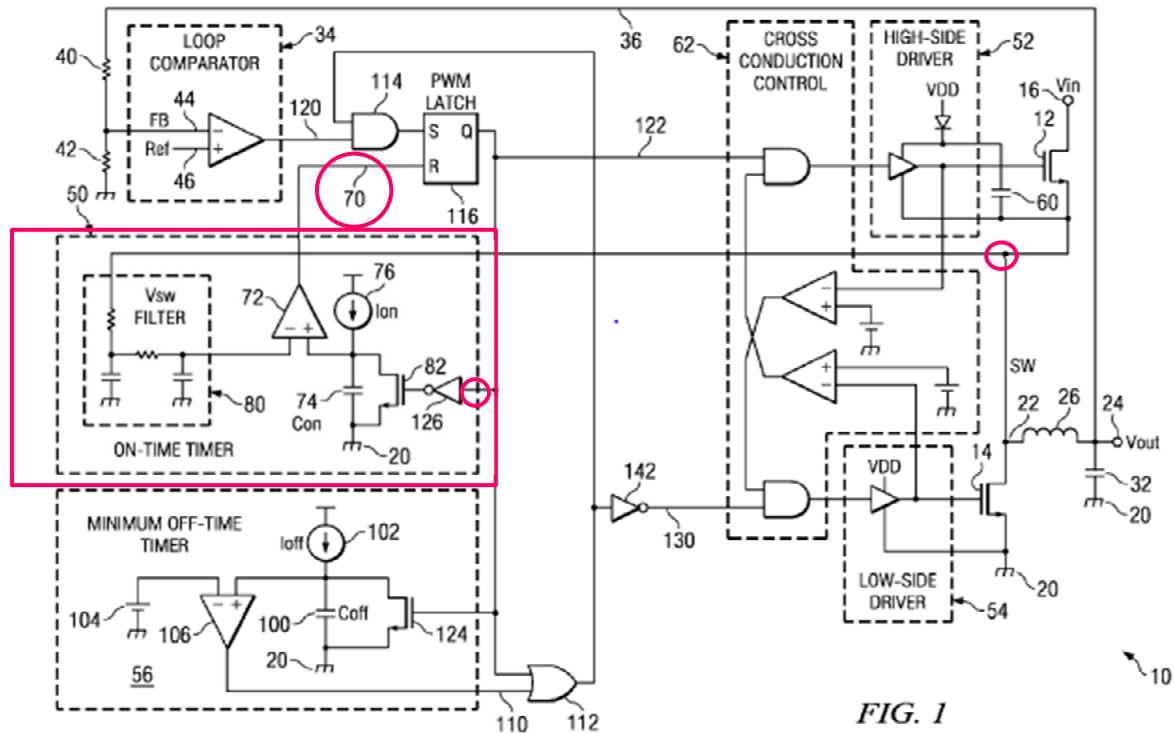
Claim terms in an IPR are construed according to their “ordinary and customary meaning” to those of skill in the art. 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Petitioner submits that, for the purposes of this proceeding and the grounds presented herein, no claim term requires express construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Instead, plain meaning should apply.

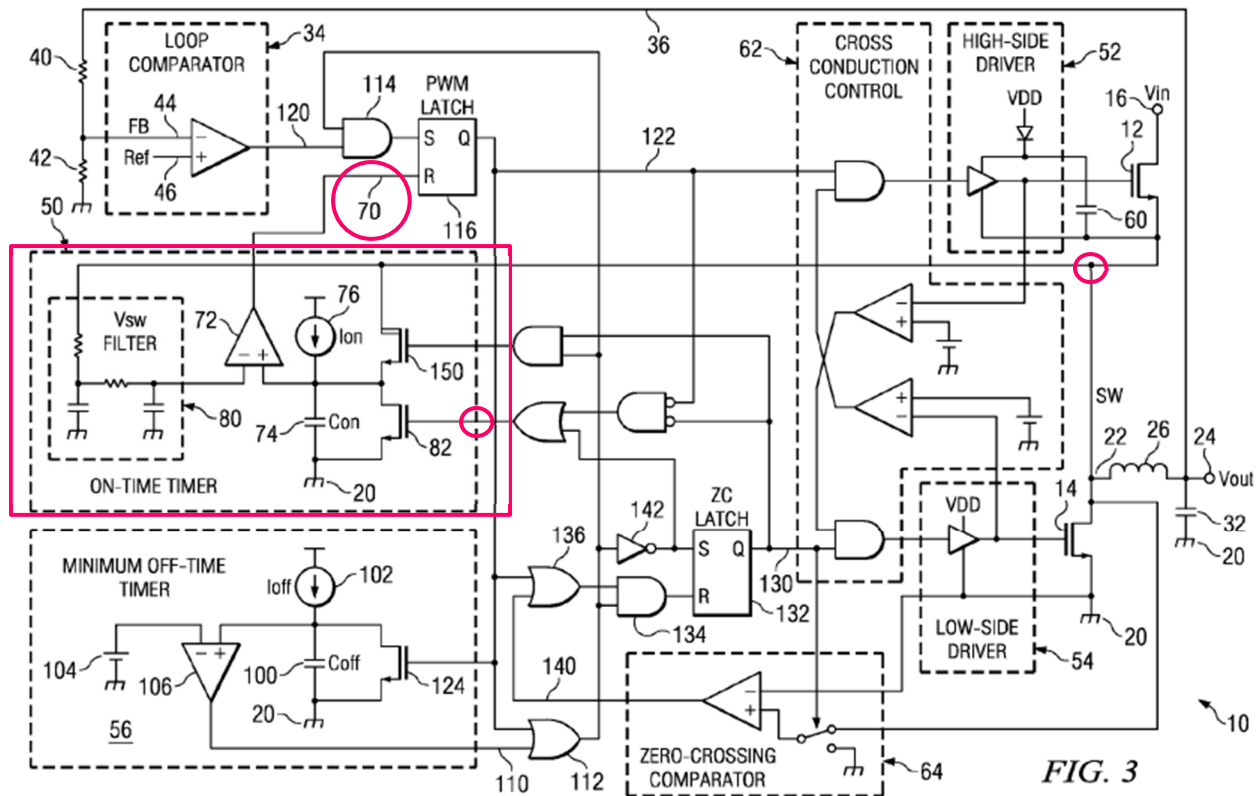
VI. SUMMARY OF THE PRIOR ART

A. Tateishi

Tateishi is directed to DC to DC converters with pseudo constant switching frequency. EX1007, ¶5; EX1003, ¶74. In particular, Tateishi discloses using feedback from the switching node to establish the pseudo constant switching frequency, thus avoiding the need to provide a pin on the integrated circuit for direct feedback from the output node at the far end of the external filtering components. EX1007, ¶17; EX1003, ¶74. Tateishi discloses an on-time circuit 50 that establishes an on-time duration (T_{on}) that is proportional to the output voltage (V_{out}) and inversely proportional to the input voltage (V_{in}) without directly

accessing V_{in} and V_{out} . EX1007, ¶32, Fig. 1 (reproduced and annotated below),
Fig. 3 (reproduced and annotated below); EX1003, ¶74.

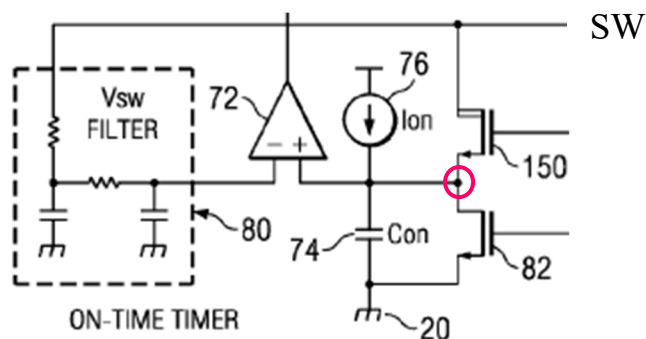




When the loop comparator 34 detects that a feedback signal (FB) 44 that is proportional to the voltage at the output (V_{out}) 24 has fallen below a reference voltage 46, the control signal 122 (output by SR latch 116) is asserted to begin an on-time of the high-side switch. The on-time circuit 50 receives the control signal 122 and the voltage at the switching node 22 and generates an on-time termination signal 70 that ends the on-time. EX1007, ¶¶19, 33; EX1003, ¶75.

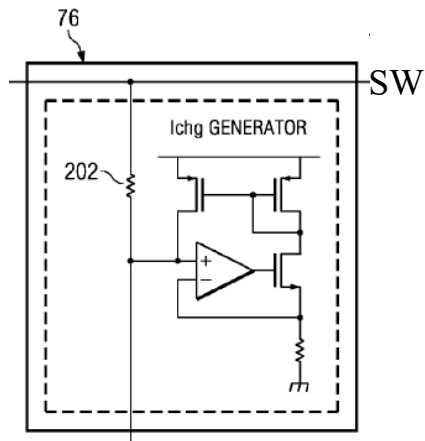
The on-time circuit 50 obtains V_{out} by averaging the voltage at the switching node 22 for an entire switching period. EX1007, ¶44; EX1003, ¶76. The averaging is performed by a switching node voltage filter (V_{sw}) 80 connected

between the switching node 22 and the comparator 72. EX1007, ¶44; EX1003, ¶76. As shown in FIGs. 1 and 3, the Vsw filter 80 comprises two resistors and two capacitors, but, as explained in the specification, “the Vsw filter 80 is a low pass filter that may be implemented in any desired manner, such as the two resistor, two capacitor example shown in FIG. 3, or with more or less resistors or capacitors, or any other desired implementation including even active filters.” EX1007, ¶49, Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶76.



During the off-time, capacitor (Con) 74 is discharged to ground by discharging transistor 82. EX1007, ¶51; EX1003, ¶77. During the on-time, capacitor Con 74 is charged from ground with a current that is approximately proportional to V_{in} from current source 76. EX1007, ¶52; EX1003, ¶77. The on-time is terminated by the comparator 72 when the voltage on the capacitor Con 74 reaches approximately V_{out} , as generated by the Vsw filter 80. EX1007, ¶52; EX1003, ¶77. “The DC to DC buck converter 10 of FIG. 3 operates in much the same manner as that of FIG. 1.” EX1007, ¶58.

Tateishi discloses several example embodiments of current source 76, one of which is shown in FIG. 4 (a portion of which is reproduced below), which includes portions of the on-time circuit. EX1007, ¶62; EX1003, ¶78.



The specification also explains that the current source 76 may be embodied in other various configurations as desired to provide an output current that is approximately proportional to V_{in} . EX1007, ¶62; EX1003, ¶79. As shown in FIG. 4, current source 76 receives the voltage at the switching node 22 through resistor 202 to capacitor Con 74. EX1007, ¶62; EX1003, ¶79. As shown in Fig. 4, the op-amp is connected as a voltage follower that buffers the voltage of capacitor Con 74 as the capacitor charges. EX1007, ¶50; EX1003, ¶¶79-80. The buffered voltage is connected to ground through a resistor. EX1003, ¶¶79-80. The current from the amplifier (through the resistor to ground) is mirrored by a current mirror whose output is then coupled to capacitor Con 74. EX1007, ¶50; EX1003, ¶80. The voltage follower amplifier and current mirror operate in a linear fashion, so the

current output of the current source 76 is proportional to the voltage of the switching node 22 during the on-time. EX1007, ¶50; EX1003, ¶¶79-80.

VII. IT IS MORE LIKELY THAN NOT THAT AT LEAST ONE OF THE CHALLENGED CLAIMS IS UNPATENTABLE

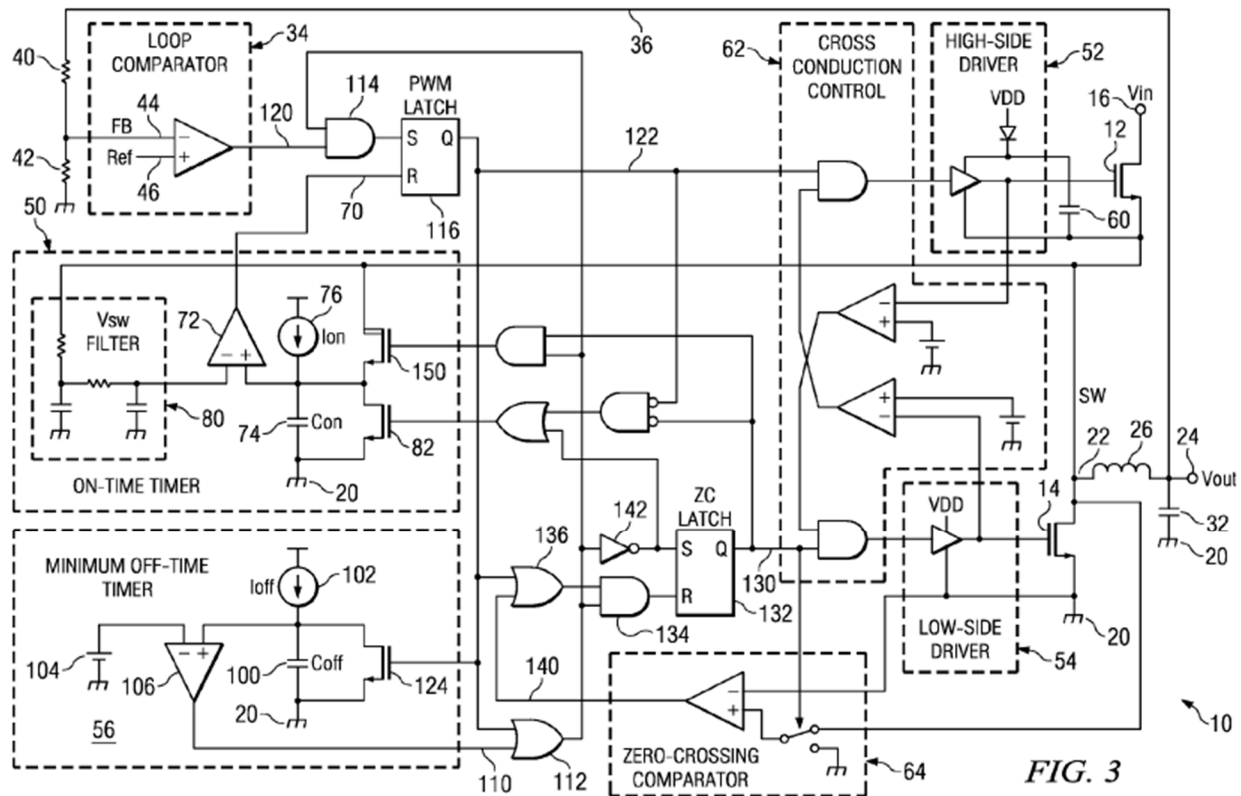
A. Ground 1: Claims 1-4, 9-14, and 17-18 are anticipated by Tateishi

As explained in greater detail in the following paragraphs, the buck-converter circuit disclosed by Tateishi is virtually identical to the recited step-down regulator and includes sub-circuits that are virtually identical to the recited pseudo constant on time control circuit and minimum off time generator.

1. Claim 1

a. Limitation 1[PRE]: A step-down regulator, comprising:

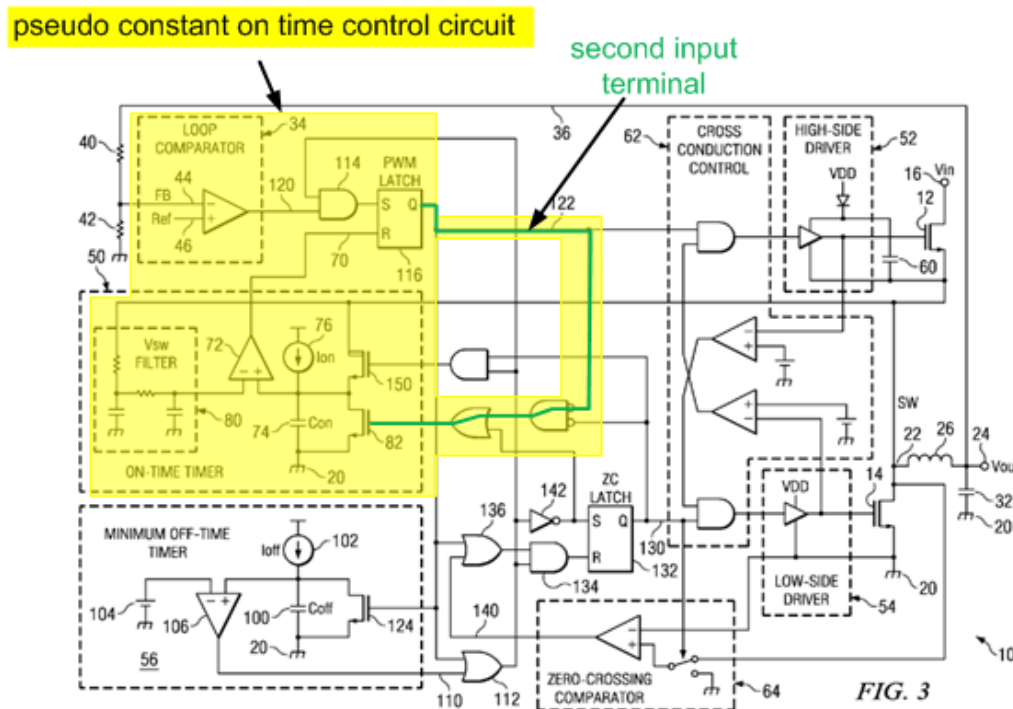
Limitation 1[PRE] recites a step-down regulator. EX1003, ¶81. To the extent the preamble is limiting, Tateishi discloses a DC-DC buck converter that receives an input voltage and regulates it down to a lower output voltage. *See, e.g.*, EX1007, ¶5 (“Various apparatuses, methods and systems for a DC to DC converter with a pseudo constant switching frequency are disclosed herein”); EX1003, ¶81. *See also* ¶18, Fig. 1, Fig. 3 (reproduced below).



b. Limitation 1[A]: a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:

Limitation 1[A] recites a pseudo-constant on-time control circuit. EX1003, ¶82. Tateishi discloses a loop comparator 34, an on-time timer 50, and other circuitry that generates signals that control the on-time of the buck converter according to “a pseudo on-time generation algorithm.” EX1007, ¶¶45-48; EX1003, ¶¶83-88. Tateishi’s on-time control circuit comprises at least on-time timer 50 and PWM latch 116, both of which will be described in more detail below. *See, e.g.*, EX1007, EX1007, ¶21 (“The operation of the on-time timer 50 in establishing a

pseudo constant switching frequency will now be described”), Fig. 3 (reproduced and annotated below); EX1003, ¶82.



c. Limitation 1[B1]: an on-time generator comprising:

Limitation 1[B1] recites an on-time generator. EX1003, ¶83. Tateishi discloses this limitation. *See, e.g.*, EX1007, ¶21 (“The operation of the on-time timer 50 in establishing a pseudo constant switching frequency will now be described”); EX1003, ¶83. That is, Tateishi’s pseudo-constant on-time control circuit includes on-time timer 50, which receives (a) control signal 122 (produced by SR latch 116) and (b) the voltage of the switching node 22 and produces on-

EX1007, ¶45, Fig. 3 (reproduced and annotated below); EX1003, ¶83.

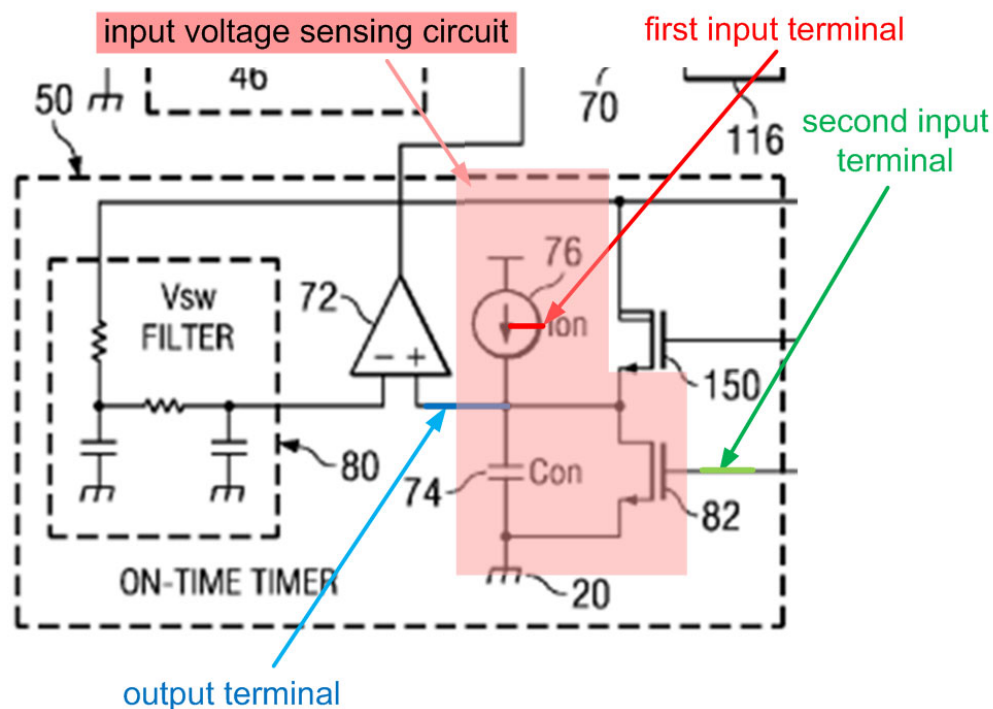


- d. Limitation 1[B2]: an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

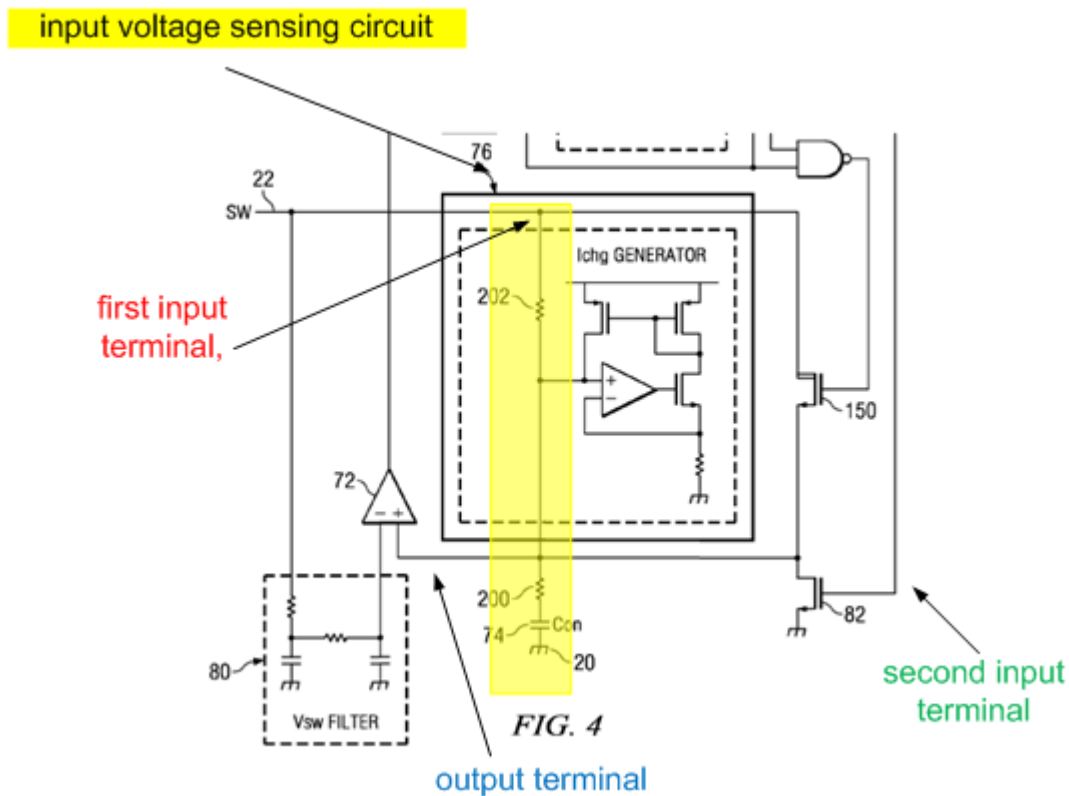
on-time generator, including a first input terminal (e.g., point of electrical

connection) configured to receive a switching signal provided by the step-down regulator, a second input terminal configured to receive a control signal provided by the pseudo constant on time (PCOT) control circuit, and an output terminal for the generated input voltage sensing signal. EX1003, ¶84. Tateishi discloses this limitation. EX1003, ¶¶84-87.

In particular, Tateishi discloses the on-time timer 50 comprising a capacitor Con 74, a discharging transistor 82 driven by the control signal 122, and a current source 76 that provides a charging current proportional to the input voltage of the power stage at input Vin 16. *See, e.g.*, EX1007, ¶32, ¶52, Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶85.



Tateishi discloses several example embodiments of current source 76, including those illustrated in Figs. 2 and 4 and described in the associated written description. *See, e.g.*, EX1007, ¶¶50, 62, Figs. 2, 4 (a portion of which is reproduced and annotated below); EX1003, ¶85.

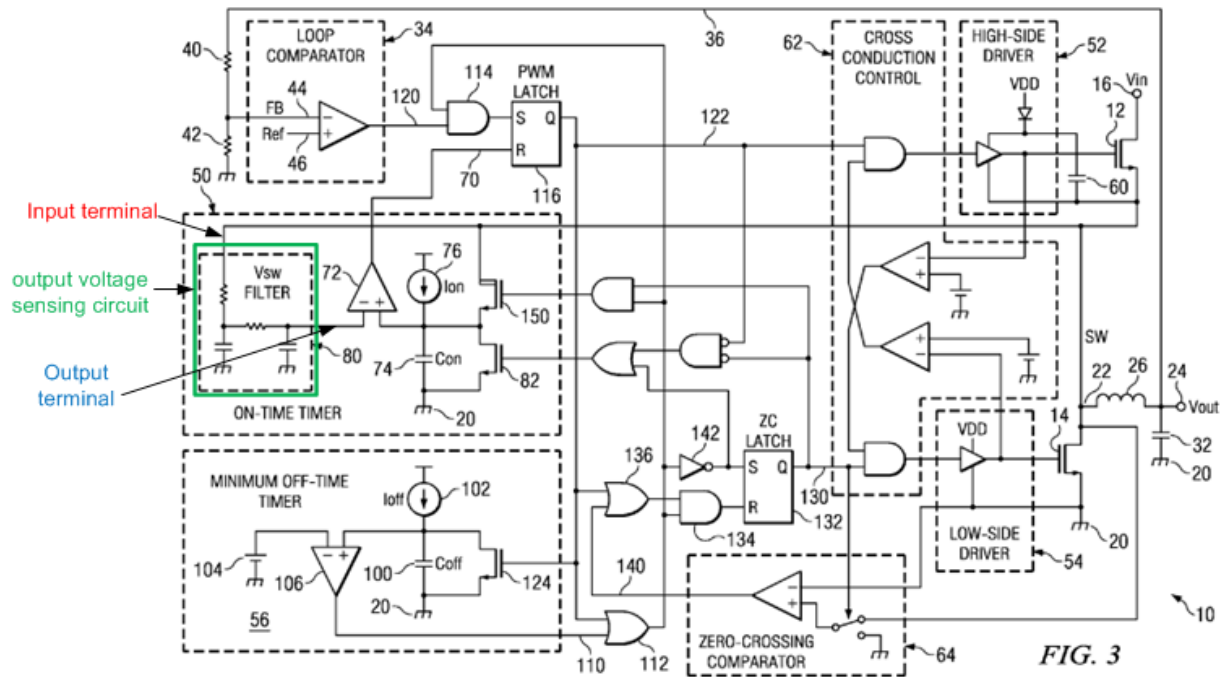


The embodiments of current source 76 illustrated in Figs. 2 and 4 receive the voltage at the point of connection with switching node 22, and they output a current that is proportional to the voltage of the switching node 22 (which, during the on-time, is connected to the input voltage, V_{in}). *See, e.g.*, EX1007, Figs. 2 and 4; EX1003, ¶¶85-86.

Thus, Tateishi discloses an input voltage sensing circuit having a first input terminal configured to receive a switching signal (SW) provided by the step-down regulator, a second input terminal configured to receive a control signal (SR latch output 122) provided by the pseudo constant on time control circuit, the input voltage sensing circuit generating an input voltage sensing signal (the voltage on the capacitor Con 74) at an output terminal (the non-grounded side of capacitor Con 74) based on the switching signal (SW) and the control signal (SR latch output 122). *See, e.g.*, EX1007, Figs. 2 and 4; EX1003, ¶88.

- e. **Limitation 1[B3]: an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and**

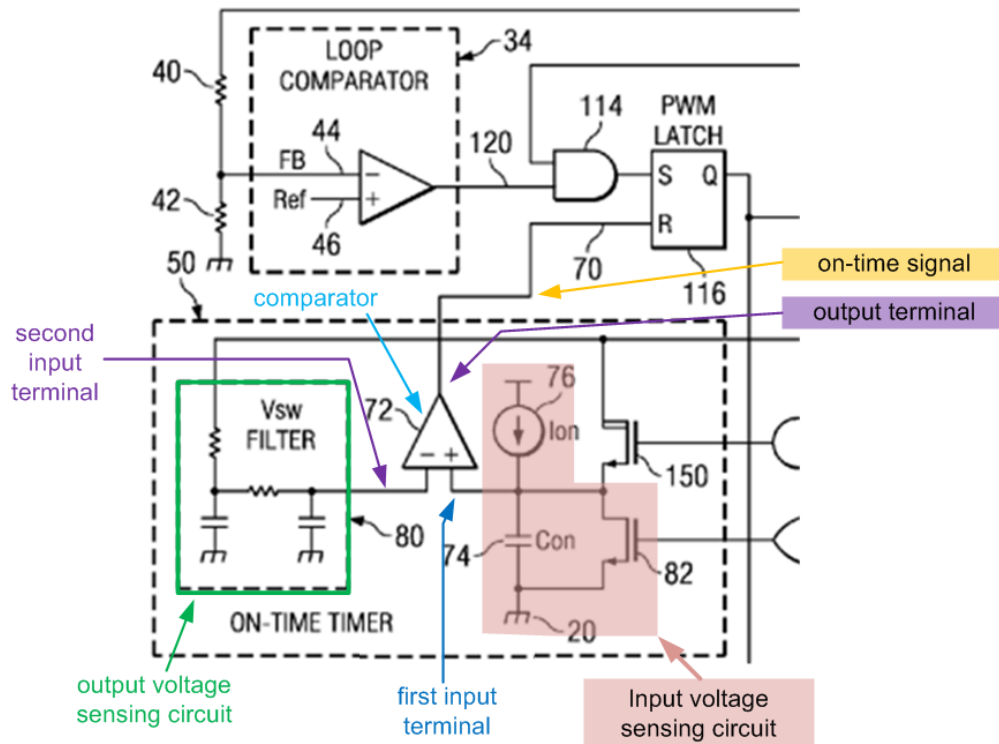
Limitation 1[B3] recites structure of an output voltage sensing circuit of the on-time generator. EX1003, ¶89. Tateishi discloses this limitation. EX1003, ¶89. In particular, Tateishi discloses generating the average voltage of the switching node 22 across an entire switching period by Vsw low-pass filter 80. *See, e.g.*, EX1007, ¶¶49, 52, Fig. 1, Fig. 3 (reproduced and annotated below); EX1003, ¶89.



Thus, Tateishi discloses an output voltage sensing circuit having an input terminal configured to receive the switching signal (SW) and generating an output voltage sensing signal based on the switching signal (low-pass filtered/averaged switching-node voltage) at an output terminal of low-pass filter 80. EX1003, ¶¶89-91.

- f. **Limitation 1[B4]: a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;**

Limitation 1[B4] recites a comparator that generates an on-time signal based on the input voltage sensing signal and the output voltage sensing signal. EX1003, ¶92. Tateishi (in particular, Tateishi's comparator 72) discloses this limitation. EX1003, ¶92. *See, e.g.*, EX1007, ¶33 ("The on-time is generated using a comparator 72 . . . The comparator 72 monitors the voltage of the capacitor Con 74 and asserts the on-time termination signal 70 to terminate the on-time when the voltage of the capacitor Con 74 reaches a reference voltage."), ¶49, ("The on-time is terminated by the comparator 72 when the voltage on the capacitor Con 74 reaches (Vout+Vdcr) as generated by the Vsw filter 80."), Fig. 1, Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶¶92-93.

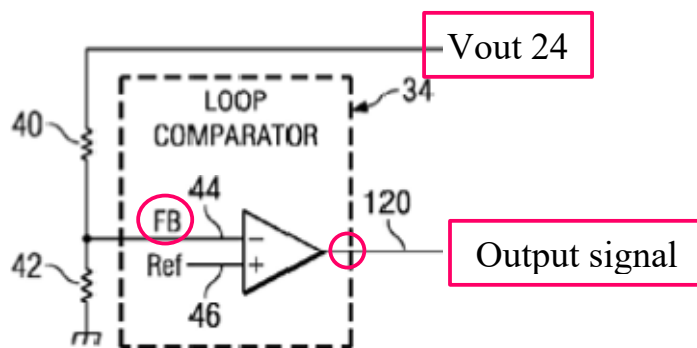


As shown in Fig. 3, Tateishi's comparator 72 receives the output voltage sensing signal from Vsw filter 50, receives the input voltage sensing signal from capacitor Con 74, and, based on those inputs, generates on-time termination signal 70. Thus, Tateishi discloses this limitation. EX1003, ¶93.

- g. **Limitation 1[C]: a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and**

Limitation 1[C] recites a feedback control circuit configured to generate an output signal in accordance with a feedback signal representative of the output voltage of the step-down regulator. EX1003, ¶94. Tateishi (in particular, Tateishi's

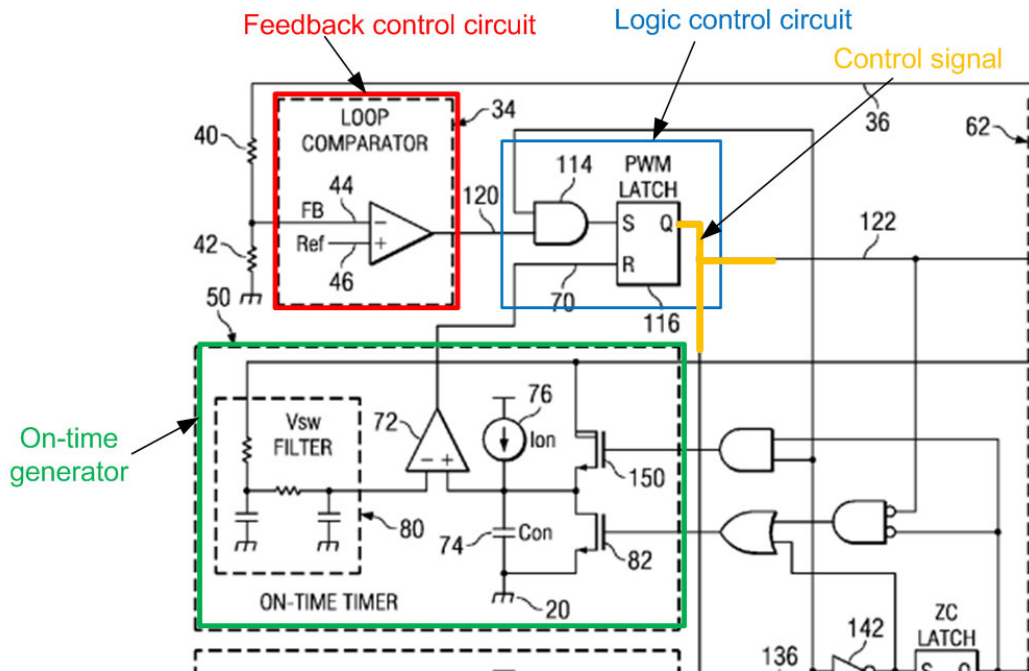
loop comparator 34) discloses this limitation. EX1003, ¶94. *See, e.g.*, ¶19 (“A loop comparator 34 in the DC to DC buck converter 10 begins each on-time based on a feedback signal 36 from the output Vout 24. The voltage of the feedback signal 36 is divided in an external voltage divider made up of an upper resistor 40 and a lower resistor 42.”), Fig. 1, Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶94. A POSITA would understand that the output (FB) of the voltage divider is proportional to (i.e., representative of) the output voltage. EX1003, ¶94.



- h. **Limitation 1[D]: a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and**

Limitation 1[D] recites a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal of

limitation 1[B4] and the output signal of limitation 1[C], wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal of limitation 1[B2]. EX1003, ¶95. Tateishi (in particular, Tateishi's PWM SR latch 116 – possibly in combination with AND gate 114) discloses this limitation. *See, e.g.*, EX1007, ¶51 (“The output 120 of the loop comparator 34 is combined with the output 110 of the minimum off-time timer 56 in the AND gate 114 at the input of the SR latch 116. . . . The output 122 of the SR latch 116 is thus asserted, turning on the high side switch 12 and turning off the low side switch 14.”), ¶52 (“The on-time termination signal 70 is connected to the Reset input of the SR latch 116, turning off the output 122 of the SR latch 116.”), Fig. 1, Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶95.



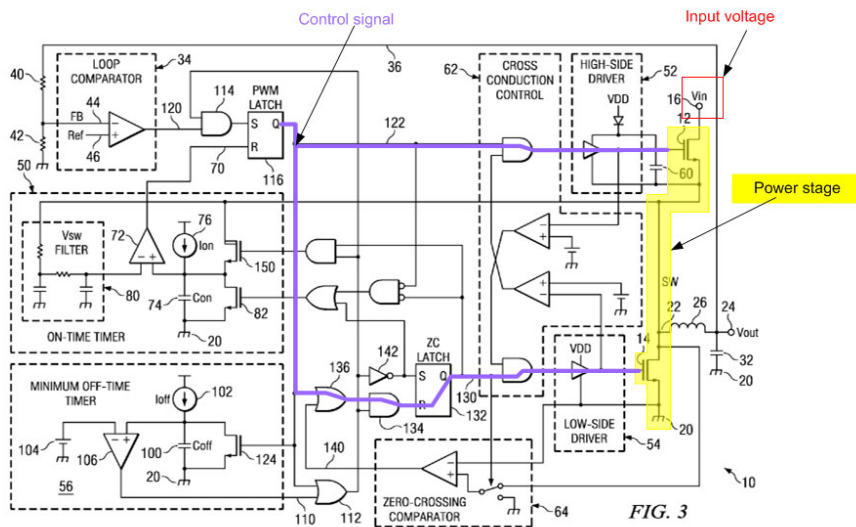
Thus, Tateishi's PWM SR latch 116 is coupled to the output 120 of the loop comparator 34 (through AND gate 114) to receive the output signal of limitation 1[C], and Tateishi's PWM SR latch 116 is coupled to the output of comparator 72 to receive the on-time signal of limitation 1[B4], and—based on these signals—Tateishi's PWM SR latch 116 produces the control signal 122 of limitation 1[B2].

EX1003, ¶96.

- i. **Limitation 1[E]: a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.**

Limitation 1[E] recites a power stage configured to receive an input voltage and the control signal of limitations 1[B2] and 1[D] and generates the switching

signal of limitations 1[B2] and 1[B3]. EX1003, ¶97. Tateishi discloses this limitation. EX1003, ¶97. In particular, Tateishi discloses a cross-conduction circuit that receives the control signal 122 produced by PWM SR latch 116, high-side and low-side switch drivers (52, 54) and high-side and low-side power switches (12, 14) configured to perform synchronous rectification. EX1007, Fig. 1, Fig. 3 (reproduced and annotated below); EX1003, ¶97.



Tateishi's high-side power switch 12 receives input voltage V_{in} and cooperates with Tateishi's low-side power switch 14 to generate switching signal SW. See, e.g., EX1007, ¶18 ("A high side switch 12 and a low side switch 14 are connected in series between an input V_{in} 16 and ground 20, with a switching node 22 between the high side switch 12 and the low side switch 14. An output V_{out} 24 is connected to the switching node 22 through an output filter. For example, the output filter may include an inductor 26 connected between the switching node 22

and the output Vout 24, and capacitor 32 connected in series between the output Vout 24 and ground 20.”), Fig. 1, Fig. 3; EX1003, ¶98.

A POSITA would understand that the arrangement of these components (illustrated and described in Fig. 3 and the associated written description) necessarily constitute the power stage of Tateishi’s buck converter, which receives an input voltage (Vin) 16 and control signal 122 and produces a voltage signal at the switching node (SW) 22. EX1003, ¶99.

2. **Claim 2**

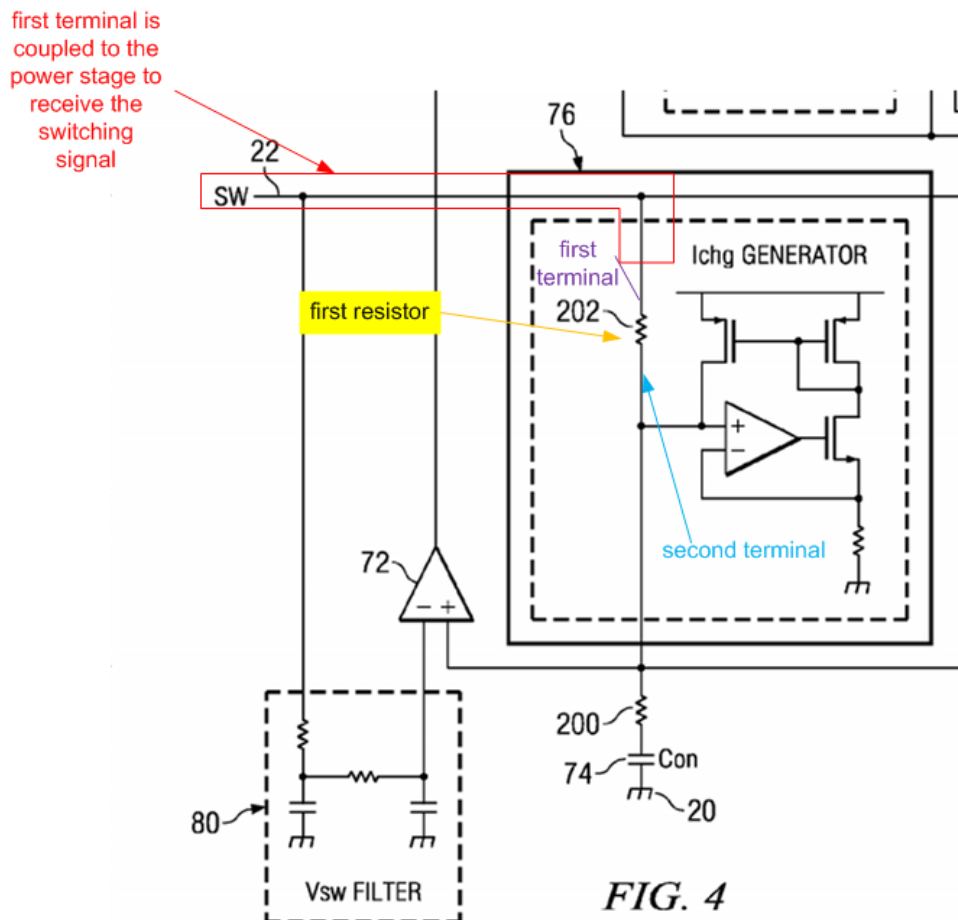
a. **Limitation 2[PRE]: The step-down regulator of claim 1, wherein the input voltage sensing circuit comprises:**

Claim 2 depends from claim 1. Tateishi anticipates claim 1. *See, e.g.*, VII.A.1, *supra* (incorporated here); EX1003, ¶100.

b. **Limitation 2[A]: a first resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the power stage to receive the switching signal;**

Limitation 2[A] recites the input voltage sensing circuit including a first resistor having a first terminal coupled to the power stage to receive the switching signal. EX1003, ¶101. Tateishi discloses this limitation. *See, e.g.*, ¶62 (“Various elements of another embodiment of a DC to DC buck converter 10 are illustrated in FIG. 4 . . . The input voltage to the amplifier 86 in the current source 76 is

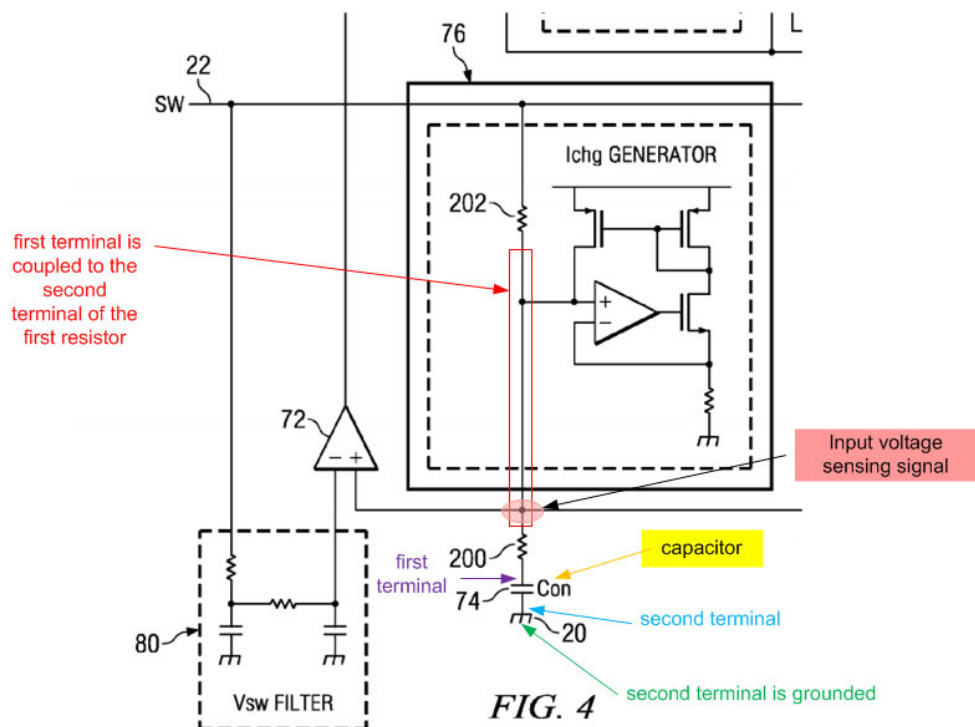
connected . . . to the switching node 22 through a resistor 202”, Fig. 4 (a portion of which is reproduced and annotated below); EX1003, ¶101.



- a. **Limitation 2[B]: a capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first resistor and provides the input voltage sensing signal, and the second terminal is grounded; and**

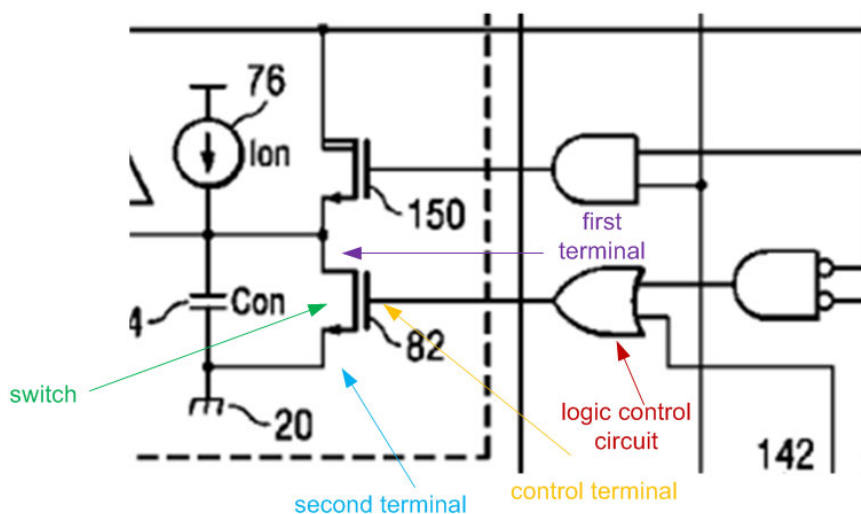
Limitation 2[B] recites the input voltage sensing circuit including a capacitor coupled to the first resistor at one terminal and grounded at the other terminal.

EX1003, ¶102. Tateishi (in particular, Tateishi's capacitor Con 74) discloses this limitation. *See, e.g.*, EX1007, Fig. 1, Fig. 3 (showing capacitor Con 74 coupled directly to current source 76); EX1003, ¶102. In other embodiments, capacitor Con 74 is coupled to resistor 202 through “resistor 200 connected in series with the capacitor Con 74 to compensate for circuit delays such as in comparators, drivers, external MOSFETS, etc [sic]” EX1007, ¶62, Fig. 4 (a portion of which is reproduced and annotated below); EX1003, ¶102. In either embodiment, capacitor Con 74 is coupled to resistor 202 at one point of connection and grounded (connected to ground 20 potential) at the other point of connection. EX1003, ¶102.



- b. **Limitation 2[C]: a switch having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the logic control circuit to receive the control signal, the first terminal is coupled to the first terminal of the capacitor, and the second terminal is grounded.**

Limitation 2[C] recites a switch having a control terminal coupled to the logic control circuit to receive the control signal, the switch having a first terminal coupled to the non-grounded terminal of the capacitor and a second terminal that is grounded (connected to ground 20 potential). EX1003, ¶103. Tateishi (in particular, Tateishi's discharging transistor 82) discloses this limitation. *See, e.g.*, EX1007, Fig. 1, Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶103. As shown, Tateishi's discharging transistor 82 is coupled to control signal 122. EX1003, ¶103.



3. **Claim 3: The step-down regulator of claim 2, wherein the input voltage sensing circuit further comprises a linear current compensation circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, and wherein based on the input voltage sensing signal, the linear current compensation circuit provides a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage.**

Claim 3 depends from claim 2. Tateishi anticipates claim 2. *See, e.g.*, VII.A.2, *supra* (incorporated here); EX1003, ¶104.

Claim 3 recites the input voltage sensing circuit further comprising a linear current compensation circuit providing a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage. EX1003, ¶105. Tateishi discloses this limitation. *See, e.g.*, EX1007, ¶62 (“The current source 76 may be embodied in other various configurations as desired to provide an output current that is proportional to $(V_{in} - V_{on1})$.”); EX1003, ¶105. As discussed with respect to the current-source embodiment of Fig. 2, “The voltage divider 90 and 92, voltage follower amplifier 86 and current mirror 94 all operate in a linear fashion, so the current output 84 of the current source 76 is proportional to the voltage of the switching node 22.” EX1007, ¶50.

Tateishi discloses additional circuitry to provide a compensating current so that the input voltage sensing circuit of claim 2 operates in a linear fashion.

EX1003, ¶106. That is, as current flows from the switching node through the recited first resistor to the recited capacitor, the voltage across the capacitor necessarily increases as the capacitor “charges up” according to the equation $V = Q / C$. EX1003, ¶106. As the capacitor charges up, the voltage across the capacitor increases and the voltage drop across the first resistor decreases by an equivalent amount, resulting in a proportional decrease in current flowing through the first resistor (according to Ohm’s Law, $V = I \times R$). EX1003, ¶106. That is, as the capacitor charges up, the current flowing through the first resistor into the capacitor decreases exponentially. EX1003, ¶106.

As shown in Fig. 4, Tateishi addresses this by adding a variation of the voltage follower amplifier 86 and current mirror 94 of the current-source embodiment described and disclosed in Fig. 2. EX1003, ¶107. As explained with respect to Fig. 2, amplifier 86 is connected as a voltage follower, buffering the voltage at its positive terminal in the voltage follower amplifier 86 (at its negative terminal). EX1007, ¶50; EX1003, ¶107. By connecting the output of the amplifier 86 to ground through a resistor, “the amplifier 86 . . . produces an output current that is proportional to the voltage at the switching node 22.” EX1007, ¶50; EX1003, ¶107. Because the current from the amplifier 86 is mirrored by a current

mirror 94, the output of the current mirror is likewise proportional to the voltage at the switching node. EX1007, ¶50; EX1003, ¶107.

A POSITA would understand that in the current-source embodiment of Fig. 4, the input to the voltage follower amplifier 86 is the voltage across capacitor Con 74. EX1003, ¶108. Therefore, the current mirror 94 produces an output current that is proportional to voltage across capacitor Con 74. EX1003, ¶108. Accordingly, a POSITA would understand that as capacitor Con 74 charges up, the current-mirror output current increases proportionally, thereby linearly compensating for the reduced current flowing through the first resistor due to charging of capacitor Con 74. EX1003, ¶108.

4. **Claim 4**

- a. **Limitation 4[PRE]: The step-down regulator of claim 3, wherein the linear current compensation circuit comprises**

Claim 4 depends from claim 3. Tateishi anticipates claim 3. *See, e.g.*, VII.A.3, *supra* (incorporated here); EX1003, ¶109.

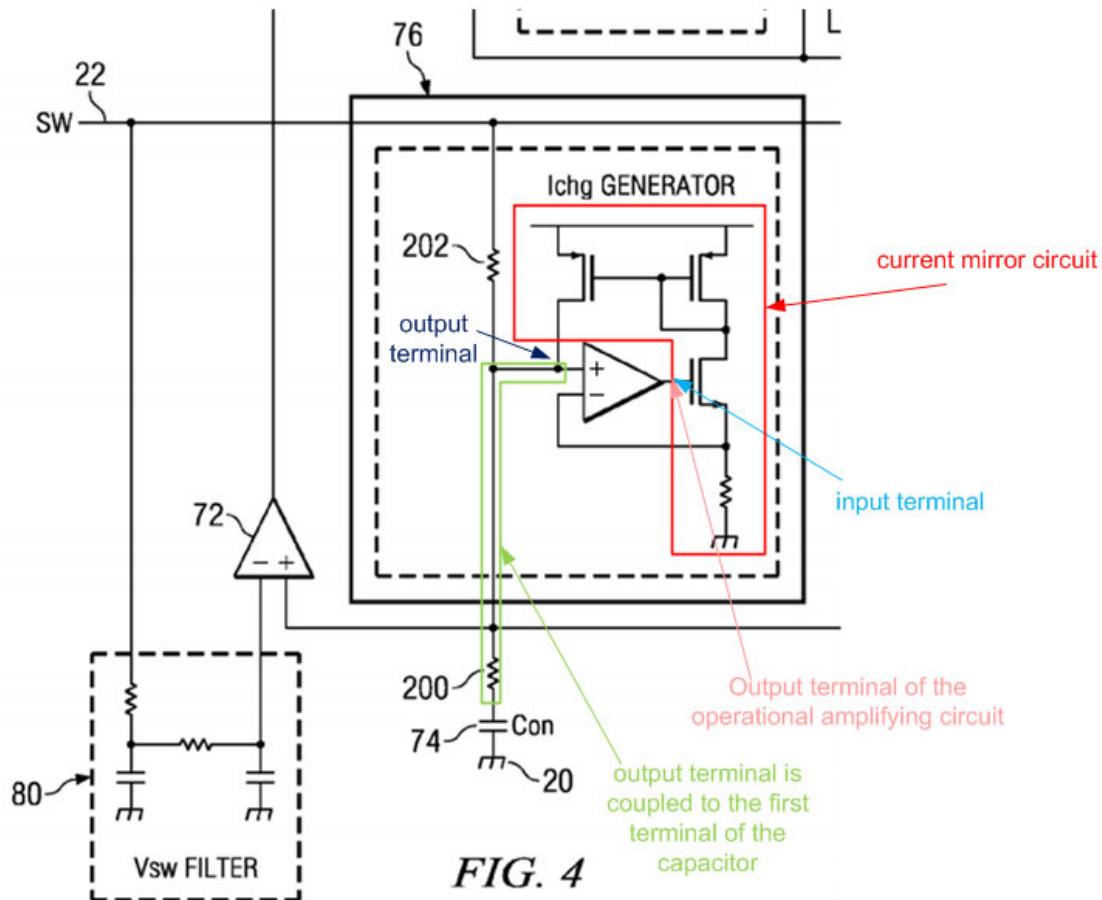
- Limitation 4[A] recites the linear current compensation circuit comprising an operational amplifying circuit having an input terminal coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal of limitation 1[B2]. EX1003, ¶110. Tateishi (in particular, Tateishi's voltage follower amplifier 86) discloses this limitation. *See, e.g.*, EX1007, Fig. 4 (a portion of which is reproduced and annotated below); EX1003, ¶110.



- c. **Limitation 4[B]: a current mirror circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the operational amplifying circuit, and the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current.**

Limitation 4[B] recites the linear current compensation circuit comprising a current mirror circuit having an input terminal coupled to the output terminal of the operational amplifying circuit, and an output terminal coupled to the first terminal of the capacitor to provide the linear compensation current. EX1003, ¶111.

Tateishi (in particular, Tateishi's current mirror 94 and associated circuitry) discloses this limitation. *See, e.g.*, EX1007, ¶50 ("The current from the amplifier 86 is mirrored by a current mirror 94."), Fig. 4 (a portion of which is reproduced and annotated below); EX1003, ¶111.

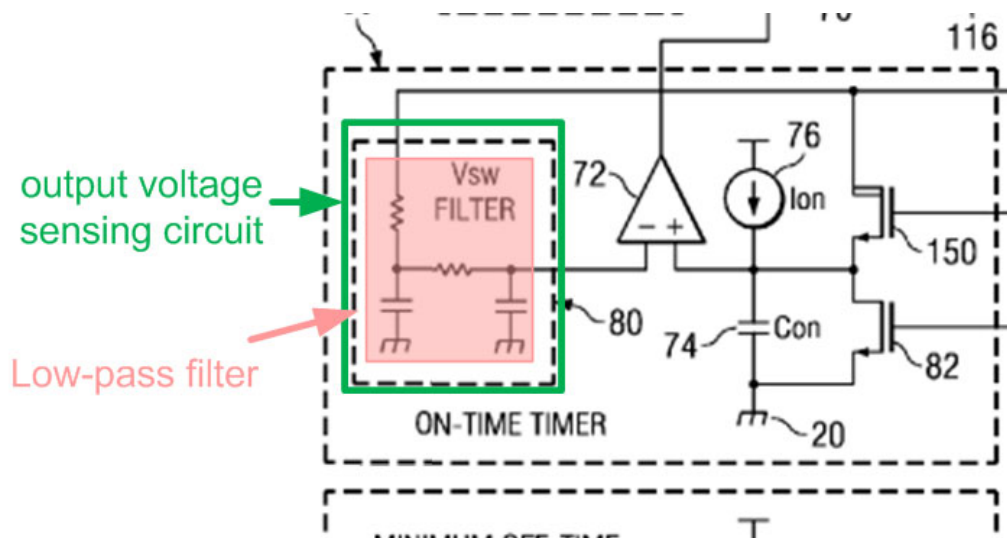


5. Claim 9: The step-down regulator of claim 1, wherein the output voltage sensing circuit comprises a low-pass filter.

Claim 9 depends from claim 1. Tateishi anticipates claim 1. *See, e.g.*, VII.A.1, *supra* (incorporated here); EX1003, ¶112.

Claim 9 recites the output voltage sensing circuit comprising a low-pass filter. EX1003, ¶113. Tateishi discloses this limitation. EX1003, ¶113. In particular, Tateishi discloses generating the average voltage of the switching node 22 across an entire switching period by a V_{sw} low-pass filter 80. *See, e.g.,*

EX1007, ¶49 (“The Vsw filter 80 is a low pass filter that may be implemented in any desired manner, such as the two resistor, two capacitor example shown in FIG. 3, or with more or less resistors or capacitors, or any other desired implementation including even active filters. The time constant of the Vsw filter 80 is selected to be large enough against the switching period of the DC to DC buck converter 10 to achieve a stable voltage for the comparator 72.”), ¶44 (“the average Voltage of the Switching node 22 across an entire switching period as generated by the Vsw filter 80”), Fig. 1, Fig. 3 (a portion of which is reproduced and annotated below);
EX1003, ¶113.



6. **Claim 10**

- a. **Limitation 10[PRE]: The step-down regulator of claim 9, wherein the low-pass filter comprises:**

Claim 10 depends from claim 9. Tateishi anticipates claim 9. *See, e.g.*, VII.A.5, *supra* (incorporated here); EX1003, ¶114.

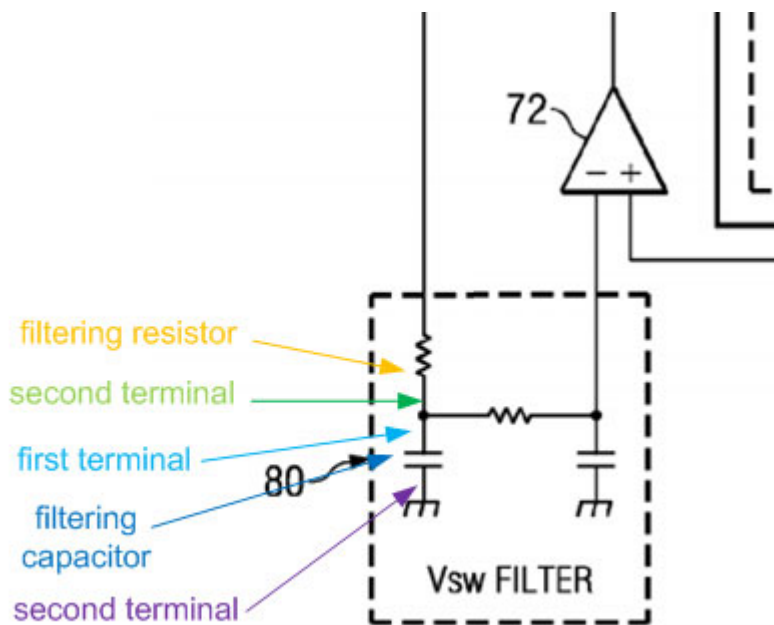
- b. **Limitation 10[A]: a filtering resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the power stage to receive the switching signal; and**

Limitation 10[A] recites the low-pass filter comprising a filtering resistor coupled to the power stage to receive the switching signal. EX1003, ¶115. Tateishi discloses this limitation. *See, e.g.*, EX1007, Fig. 4 (a portion of which is reproduced and annotated below). EX1003, ¶115. *See also*, EX1007, ¶49 (“The Vsw filter 80 is a low pass filter that may be implemented in any desired manner, such as the two resistor, two capacitor example shown in FIG. 3, or with more or less resistors or capacitors, or any other desired implementation including even active filters.”).



- Limitation 10[B] recites the low-pass filter comprising a filtering capacitor coupled between the filtering resistor and ground, the capacitor providing the output voltage sensing signal. EX1003, ¶116. Tateishi discloses this limitation. *See, e.g.*, EX1007, Fig. 4 (a portion of which is reproduced and annotated below, showing a

capacitor coupled to the resistor through another resistor). EX1003, ¶116; *see also*, EX1007, ¶49 (“The Vsw filter 80 is a low pass filter that may be implemented in any desired manner, such as the two resistor, two capacitor example shown in FIG. 3, or with more or less resistors or capacitors, or any other desired implementation including even active filters.”).



7. **Claim 11**

a. **Limitation 11[PRE]: A pseudo constant on time control circuit for a step-down regulator, comprising:**

Limitation 11[PRE] recites a pseudo constant on time control circuit for a step-down regulator. EX1003, ¶118. To the extent the preamble is limiting, Tateishi discloses this limitation. *See, e.g.*, EX1007, ¶5 (“Various apparatuses, methods and systems for a DC to DC converter with a pseudo constant switching

frequency are disclosed herein”); EX1003, ¶118. Tateishi discloses a loop comparator 34, an on-time timer 50, and other circuitry that generates signals that control the on-time of the buck converter according to “a pseudo on-time generation algorithm.” EX1007, ¶45; EX1003, ¶¶83-88. *See also* VII.A.1.a, VII.A.1.b, *supra* (both incorporated here).

b. Limitation 11[A]: an on-time generator comprising:

Tateishi discloses this limitation. *See, e.g.*, VII.A.1.c, *supra* (incorporated here); EX1003, ¶119.

c. Limitation 11[B1]: an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

Tateishi discloses this limitation. *See, e.g.*, VII.A.1.d, *supra* (incorporated here); EX1003, ¶120.

- d. **Limitation 11[B2]: an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and**

Tateishi discloses this limitation. *See, e.g., VII.A.1.e, supra* (incorporated here); EX1003, ¶121.

- e. **Limitation 11[B3]: a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;**

Tateishi discloses this limitation. *See, e.g., VII.A.1.f, supra* (incorporated here); EX1003, ¶122.

- f. **Limitation 11[C]: a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and**

Tateishi discloses this limitation. *See, e.g., VII.A.1.g, supra* (incorporated here); EX1003, ¶123.

- g. **Limitation 11[D]: a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal.**

Tateishi discloses this limitation. *See, e.g., VII.A.1.h, supra* (incorporated here); EX1003, ¶124.

8. **Claim 12**

- a. **Limitation 12[PRE]: The pseudo constant on time control circuit of claim 11, wherein the input voltage sensing circuit comprises:**

Claim 12 depends from claim 11. Tateishi anticipates claim 11. *See, e.g., VII.A.7, supra* (incorporated here); EX1003, ¶125.

- b. **Limitation 12[A]: a first resistor having a first terminal and a second terminal, wherein the first terminal is configured to receive the switching signal;**

Tateishi discloses this limitation. *See, e.g., VII.A.2.b, supra* (incorporated here); EX1003, ¶126.

- c. **Limitation 12[B]: a capacitor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first resistor and provides the input voltage sensing signal, and the second terminal is grounded; and**

Tateishi discloses this limitation. *See, e.g., VII.A.2.a, supra* (incorporated here); EX1003, ¶127.

- d. **Limitation 12[C]: a switch having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the logic control circuit to receive the control signal, the first terminal is coupled to the first terminal of the capacitor, the second terminal is grounded.**

Tateishi discloses this limitation. *See, e.g., VII.A.2.b, supra* (incorporated here); EX1003, ¶128.

9. **Claim 13: The pseudo constant on time control circuit of claim 12, wherein the input voltage sensing circuit further comprises a linear current compensation circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, and wherein based on the input voltage sensing signal, the linear current compensation circuit provides a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage.**

Claim 13 depends from claim 12. Tateishi anticipates claim 12. *See, e.g., VII.A.8, supra* (incorporated here); EX1003, ¶129. Claim 3 recites the input voltage sensing circuit further comprising a linear current compensation circuit providing a linear compensation current to the capacitor so that the input voltage sensing signal varies linearly with the input voltage. EX1003, ¶130. Tateishi discloses this limitation. *See, e.g., VII.A.3, supra* (incorporated here); EX1003, ¶130.

10. **Claim 14**

- a. **Limitation 14[PRE]: The pseudo constant on time control circuit of claim 13, wherein the linear current compensation circuit comprises:**

Claim 14 depends from claim 13. Tateishi anticipates claim 13. *See, e.g.*, VII.A.9, *supra* (incorporated here); EX1003, ¶131.

- b. **Limitation 14[A]: an operational amplifying circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal; and**

Tateishi discloses this limitation. *See, e.g.*, VII.A.4.b, *supra* (incorporated here); EX1003, ¶132.

- c. **Limitation 14[B]: Limitation 14[B]: a current mirror circuit having an input terminal and an output terminal, wherein the input terminal is coupled to the output terminal of the operational amplifying circuit, and the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current.**

Tateishi discloses this limitation. *See, e.g.*, VII.A.4.c, *supra* (incorporated here); EX1003, ¶133.

11. **Claim 17: The pseudo constant on time control circuit of claim 11, wherein the output voltage sensing circuit comprises a low-pass filter.**

Claim 17 depends from claim 11. Tateishi anticipates claim 11. *See, e.g.*, VII.A.7, *supra* (incorporated here); EX1003, ¶134. Claim 17 recites the output

voltage sensing circuit comprising a low-pass filter. Tateishi discloses this limitation. *See, e.g.*, VII.A.5, *supra* (incorporated here); EX1003, ¶135.

12. Claim 18

a. Limitation 18[PRE]: A step-down regulator, comprising:

Limitation 18[PRE] recites a step-down regulator. EX1003, ¶136. To the extent the preamble is limiting, Tateishi discloses this limitation. *See, e.g.*, EX1007, ¶5 (“Various apparatuses, methods and systems for a DC to DC converter with a pseudo constant switching frequency are disclosed herein”); EX1003, ¶140. *See also* VII.A.1.a, VII.A.1.b, *supra* (both incorporated here).

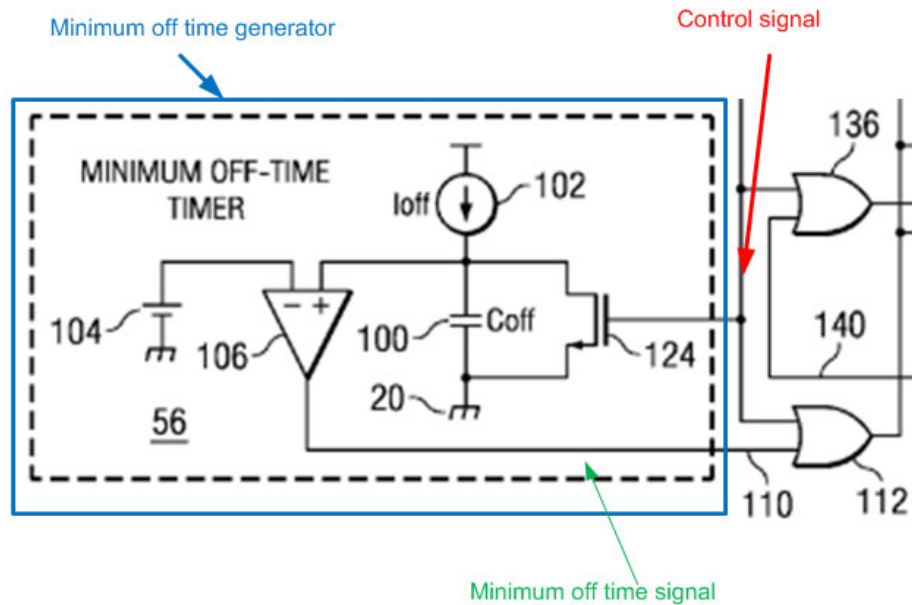
b. Limitation 18[A]: an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;

Tateishi discloses this limitation. *See, e.g.*, VII.A.1.c, VII.A.1.d, VII.A.1.e, VII.A.1.f, *supra* (all incorporated here); EX1003, ¶137.

c. Limitation 18[B]: a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;

Limitation 18[B] recites a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal. Tateishi (in particular, Tateishi’s minimum off-time timer 56) discloses this limitation. *See*,

e.g., EX1007, ¶51 (“The output 122 of the SR latch 116 also drives a discharging transistor 124 in the minimum off-time timer 56, discharging the capacitor Coff 100 to ground 20 when the on-time begins.”), ¶52 (“the on-time termination signal 70 is connected to the Reset input of the SR latch 116, turning off the output 122 of the SR latch 116. This turns off the high side switch 12. This also turns off the discharging transistor 124 in the minimum off-time timer 56, allowing the capacitor Coff 100 to be charged by the reference current source 102.”), ¶51 (“The minimum off-time may be detected when a capacitor Coff 100 is charged by a reference current source 102 to match a reference voltage 104. After the minimum off-time, a comparator 106 asserts the output 110 of the minimum off-time timer 56”), Fig. 1, Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶138.



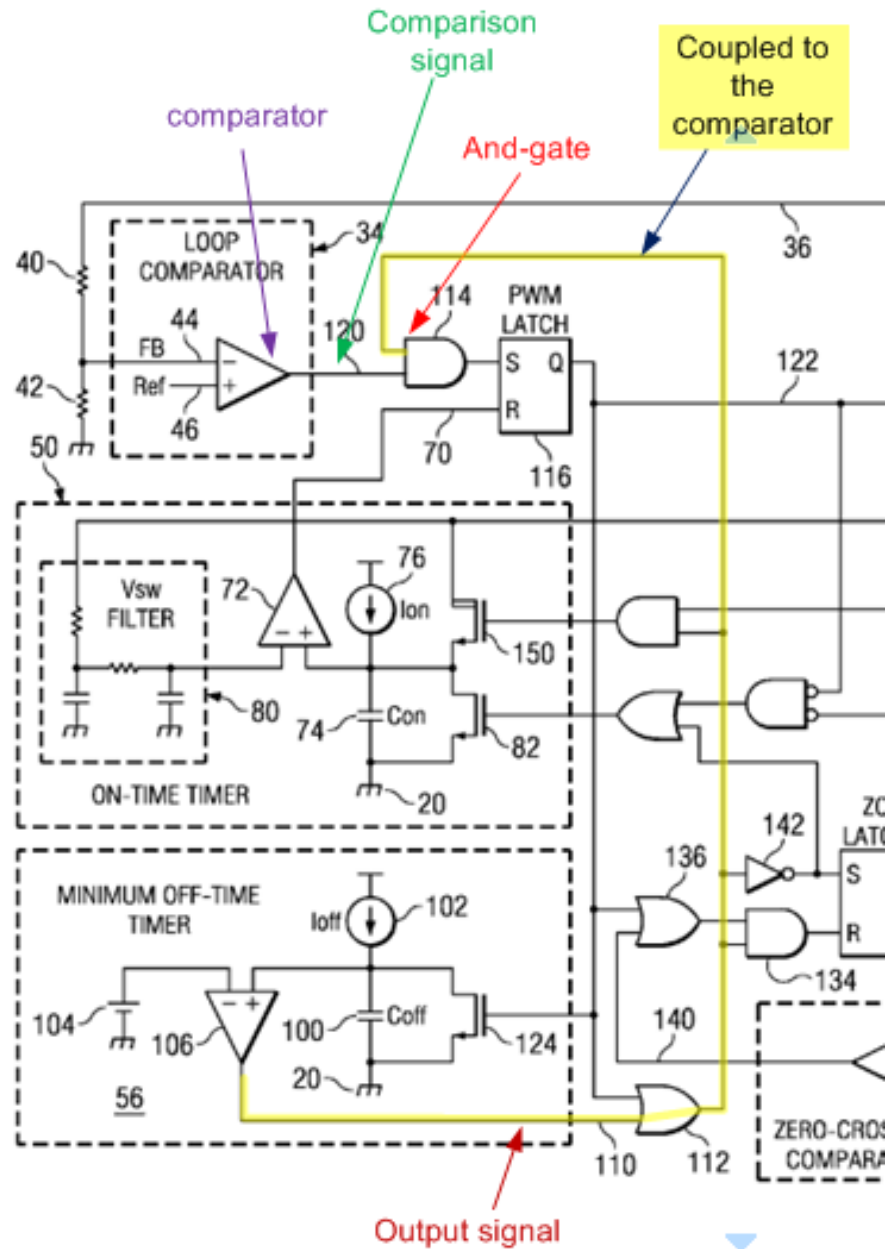
Thus, Tateishi's minimum off-time timer 56 receives control signal 122 and generates a minimum off-time signal 110. EX1003, ¶139.

- d. **Limitation 18[C]: a comparator configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to receive a reference signal, and wherein based on the feedback signal and the reference signal, the comparator generates a comparison signal;**

Tateishi discloses this limitation. *See, e.g., VII.A.1.g, supra* (incorporated here); EX1003, ¶140.

- e. **Limitation 18[D]: an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal, wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal;**

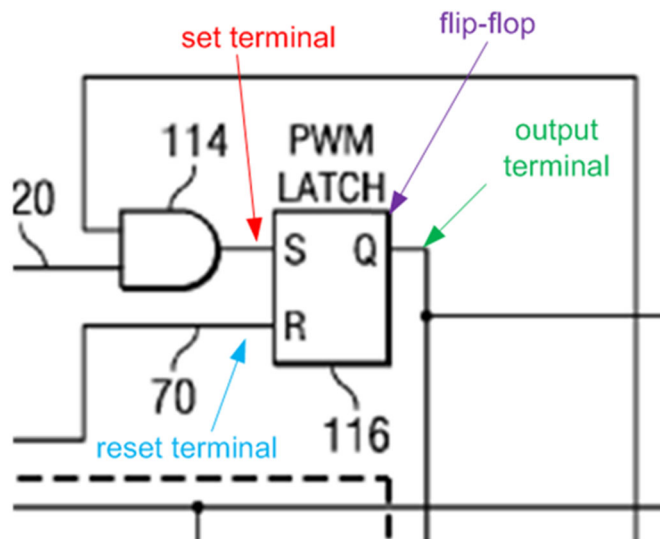
Limitation 18[D] recites an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal, wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal. Tateishi (in particular, Tateishi's AND gate 114) discloses this limitation. *See, e.g.*, EX1007, ¶51 (“After the minimum off-time, a comparator 106 asserts the output 110 of the minimum off-time timer 56 which passes through an OR gate 112 to an AND gate 114 at the Set input of an SR latch 116. The output 120 of the loop comparator 34 is combined with the output 110 of the minimum off-time timer 56 in the AND gate 114 at the S (Set) input of the SR latch 116.”), Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶141.



As shown in Fig. 3, the output 110 of the minimum off-time circuit is coupled to AND gate 114 through OR gate 112, and the output 120 of the loop comparator 34 is also coupled to AND gate 114. EX1003, ¶142.

- f. **Limitation 18[E]: a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and**

Limitation 18[E] recites a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal of limitation 18[B]. Tateishi (in particular, Tateishi's SR flip-flop 116) discloses this limitation. *See, e.g.*, ("the output 110 of the minimum off-time timer 56 which passes through an OR gate 112 to an AND gate 114 at the Set input of an SR latch 116. The output 120 of the loop comparator 34 is combined with the output 110 of the minimum off-time timer 56 in the AND gate 114 at the [Set] input of the SR latch 116. . . The output 122 of the SR latch 116 is thus asserted, turning on the high side switch 12 and turning off the low side switch 14."), Fig. 3 (a portion of which is reproduced and annotated below); EX1003, ¶143.



Thus, the Set (S) input of Tateishi's SR flip-flop 116 is coupled through AND gate 114 to the output of the minimum off-time timer 56, the Reset (R) input is coupled to the on-time termination signal 70 of Tateishi's on-time circuit 50, and the SR flip-flop 116 produces 122, the control signal recited in limitation 18[B]. EX1003, ¶144.

- g. **Limitation 18[F]: a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.**

Tateishi discloses this limitation. *See, e.g., VII.A.1.i, supra* (incorporated here); EX1003, ¶145.

B. Ground 2: Claims 5, 7-8, and 15 are rendered obvious by Tateishi

1. Claim 5

a. **Limitation 5[PRE]: The step-down regulator of claim 4, wherein the current mirror circuit comprises:**

Claim 5 depends from claim 4. Tateishi anticipates claim 4. *See, e.g.*, VII.A.4, *supra* (incorporated here); EX1003, ¶146.

b. **Limitation 5[A]: a current mirror having an input terminal and an output terminal, wherein the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current;**

Limitation 5[A] recites the current mirror circuit comprising a current mirror. EX1003, ¶147. Tateishi (in particular, Tateishi's current mirror 94) discloses this limitation. *See, e.g.*, EX1007, Fig. 4 (a portion of which is reproduced and annotated below); EX1003, ¶147.

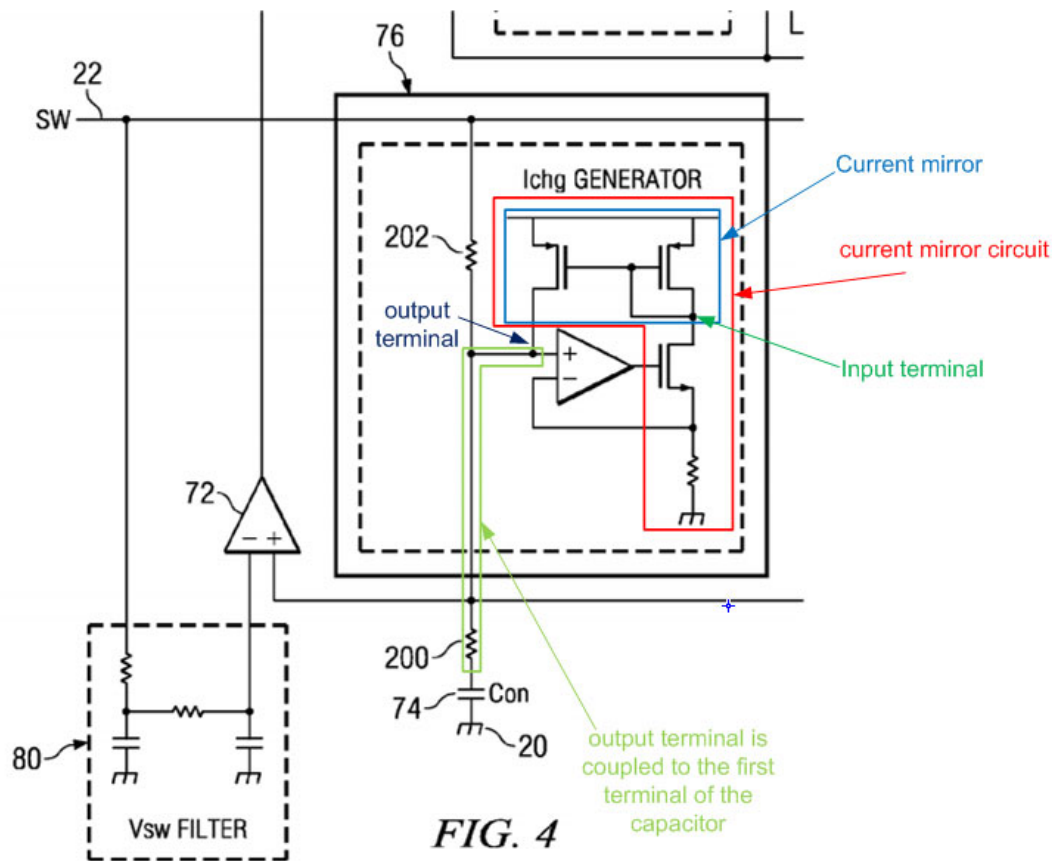
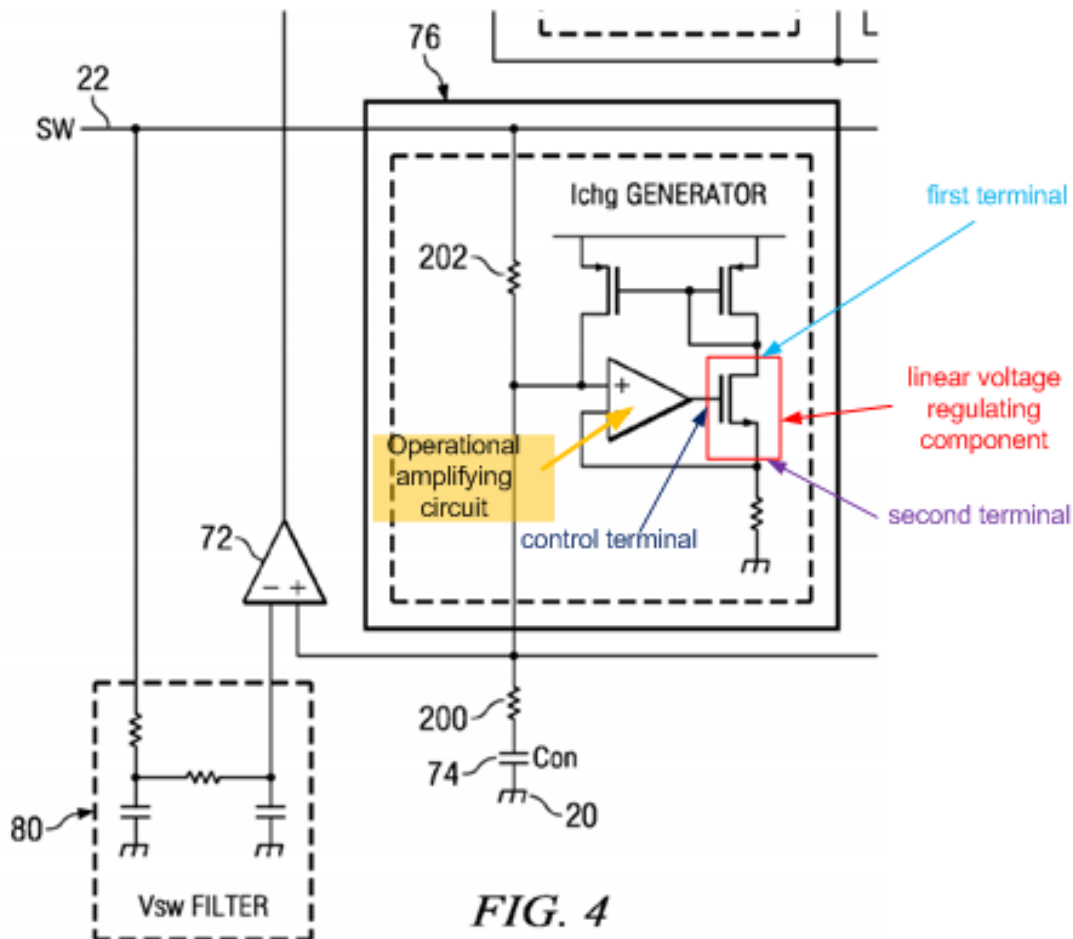


FIG. 4

- c. **Limitation 5[B]: a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying circuit, the first terminal is coupled to the input terminal of the current mirror; and**

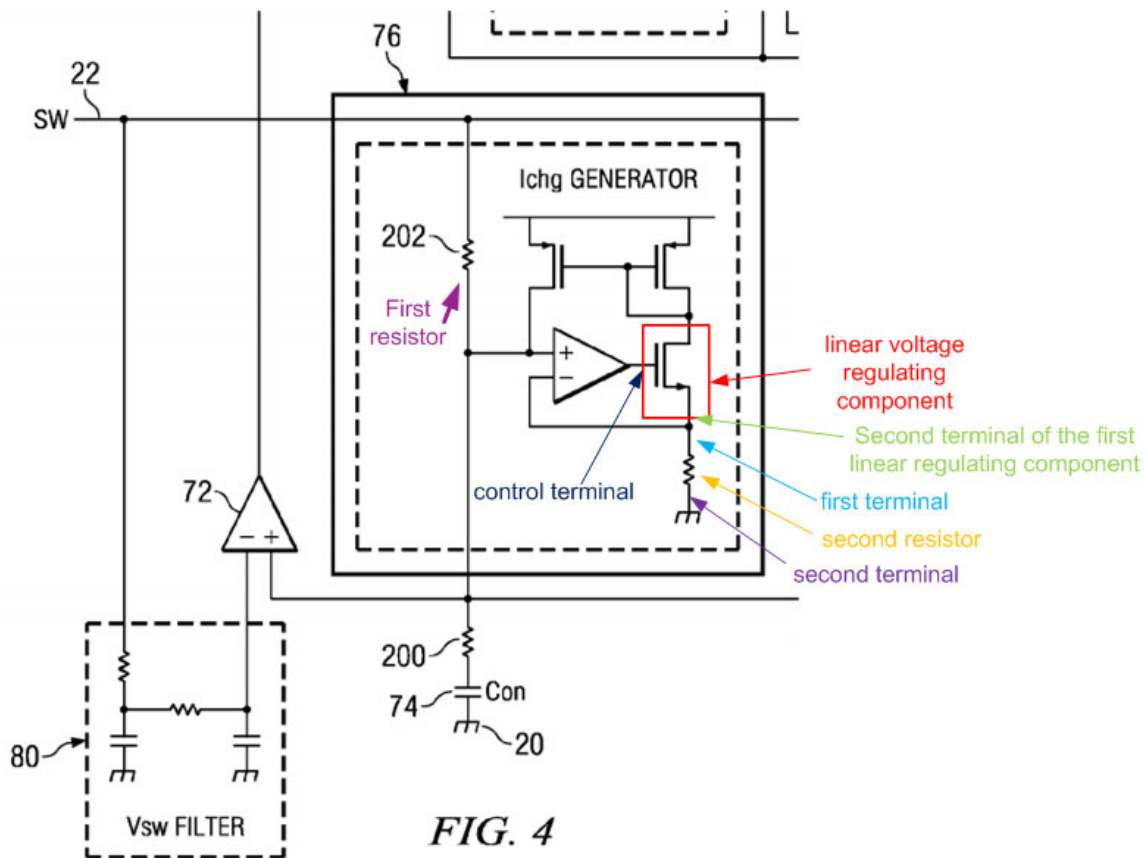
Limitation 5[B] recites the current mirror circuit comprising a first linear voltage regulating component having a control terminal coupled to the output terminal of the operational amplifying circuit and a first terminal coupled to the input terminal of the current mirror. EX1003, ¶148. Tateishi discloses this limitation. *See, e.g.,* EX1007, Fig. 4 (a portion of which is reproduced and

annotated below); EX1003, ¶148. That is, Tateishi discloses a MOSFET (first linear voltage regulating component) whose gate (control terminal) is coupled to the output of Tateishi's voltage follower amplifier 86. EX1003, ¶148. The MOSFET's drain is coupled to Tateishi's current mirror 94. EX1003, ¶148.



- d. **Limitation 5[C]: a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first resistor and the second resistor have the same resistance.**

Limitation 5[C] recites the current mirror circuit comprising a second resistor coupled between the first linear voltage regulating component and ground, the first resistor and the second resistor having the same resistance. EX1003, ¶149. Tateishi discloses this limitation and/or renders this limitation obvious. *See, e.g.*, EX1007, Fig. 4 (a portion of which is reproduced and annotated below); EX1003, ¶149.



A POSITA would understand that the voltage across capacitor Con 74 (neglecting resistor 200) and the voltage across resistor 202 sum to the voltage of the switching node. EX1003, ¶150. As discussed with respect to limitation 3[A], a POSITA would understand that as capacitor Con 74 charges up, the current flowing through resistor 202 decreases proportionally to the voltage across capacitor Con 74. *See, e.g., VII.A.3, supra* (incorporated here); EX1003, ¶150. That is, the decrease in current (according to Ohm's law) is the voltage across capacitor Con 74 divided by the resistance of resistor 202. EX1003, ¶150. Thus, a

POSITA would understand that for the current mirror to compensate for capacitor Con 74 charging up (so as to maintain a charging current proportional to the switching-node voltage), the current mirror should produce a current equal to the voltage across capacitor Con 74 divided by the resistance of resistor 202. *See, e.g.*, EX1007, Fig. 4 (reproduced and annotated above, showing equivalent voltage levels with equivalent colors); EX1003, ¶150.

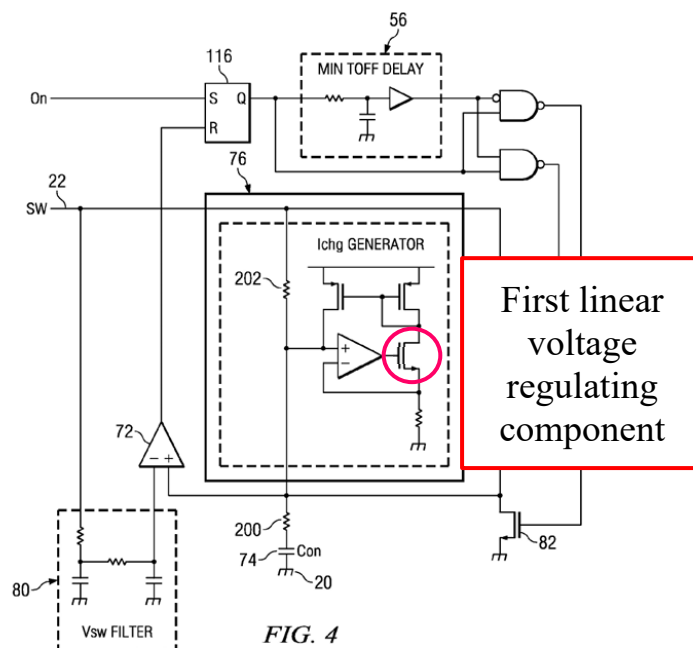
In particular, a POSITA would understand that for a current mirror 94 of unity gain (according to unit matching principles), the output current will be the input voltage buffered by Tateishi's voltage follower amplifier 86 (i.e., the voltage across Capacitor Con 74) divided by the resistance of the resistor that connects the output of Tateishi's voltage follower amplifier 86 to ground (unlabeled in Fig. 4). *See, e.g.*, EX1007, Fig. 4; EX1003, ¶151. Thus, to produce the required linear-compensation current (the voltage across capacitor Con 74 divided by the resistance of resistor 202), the unlabeled resistor should have a resistance that is the same as resistor 202 (again, according to unit matching principles). EX1003, ¶151. That is, if both resistors have the same value, then no matter what the voltage across the capacitor is, the sum of the currents flowing through resistor 202 and the unlabeled resistor will be proportional to the switching node voltage. EX1003,

¶151. For at least that reason, the first resistor and the second resistor having the same resistance would have been obvious to a POSITA. EX1003, ¶151.

2. **Claim 7: The step-down regulator of claim 5, wherein the first linear voltage regulating component is a MOSFET or a BJT.**

Claim 7 depends from claim 5. Tateishi renders claim 5 obvious. *See, e.g.*, VII.B.1, *supra* (incorporated here); EX1003, ¶152.

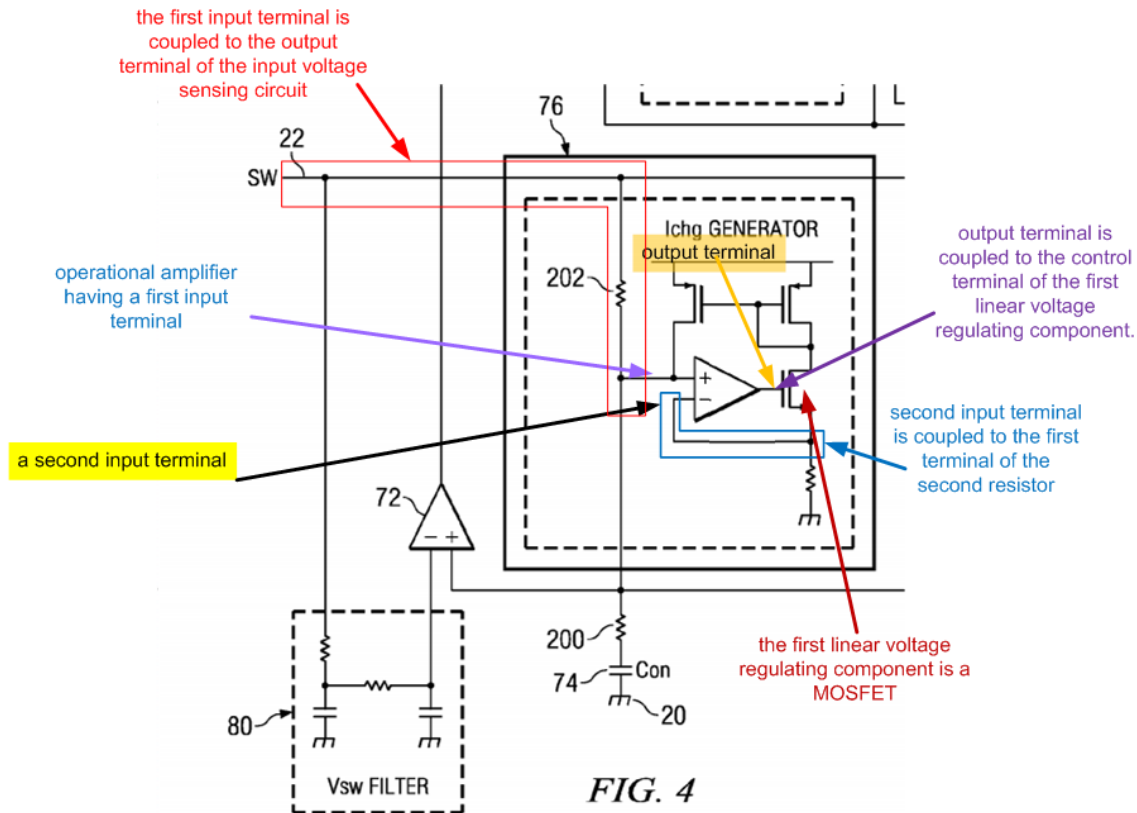
Claim 7 recites the first linear voltage regulating component being a MOSFET or a BJT. EX1003, ¶153. Tateishi discloses this limitation and/or renders this limitation obvious. *See, e.g.*, EX1007, Fig. 4 (reproduced and annotated below, illustrating the transistor as a MOSFET); EX1003, ¶153.



3. **Claim 8: The step-down regulator of claim 5, wherein the operational amplifying circuit comprises an operational amplifier having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the first terminal of the second resistor, and the output terminal is coupled to the control terminal of the first linear voltage regulating component.**

Claim 8 depends from claim 5. Tateishi renders claim 5 obvious. *See, e.g.*, VII.B.1, *supra* (incorporated here); EX1003, ¶154.

Claim 8 recites the operational amplifying circuit comprises an operational amplifier having a first input terminal coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, a second input terminal coupled to the first terminal of the second resistor, and an output terminal coupled to the control terminal of the first linear voltage regulating component. EX1003, ¶155. Tateishi (in particular, Tateishi's voltage follower amplifier 86) discloses this limitation. *See, e.g.*, EX1007, Fig. 4 (a portion of which is reproduced and annotated below); EX1003, ¶155.



1. Claim 15

- a. Limitation 15[PRE]: The pseudo constant on time control circuit of claim 14, wherein the current mirror circuit comprises:

Claim 15 depends from claim 14. Tateishi anticipates claim 14. *See, e.g.,* VII.A.10, *supra* (incorporated here); EX1003, ¶156.

- b. Limitation 15[A]: a current mirror having an input terminal and an output terminal, wherein the output terminal is coupled to the first terminal of the capacitor to provide the linear compensation current;

Tateishi discloses this limitation. *See, e.g.,* VII.B.1.b, *supra* (incorporated here); EX1003, ¶157.

- c. **Limitation 15[B]: a first linear voltage regulating component having a first terminal, a second terminal and a control terminal, wherein the control terminal is coupled to the output terminal of the operational amplifying circuit, the first terminal is coupled to the input terminal of the current mirror; and**

Tateishi discloses this limitation. *See, e.g., VII.B.1.c, supra* (incorporated here); EX1003, ¶158.

- d. **Limitation 15[C]: a second resistor having a first terminal and a second terminal, wherein the first terminal is coupled to the second terminal of the first linear voltage regulating component, and the second terminal is grounded, further wherein the first resistor and the second resistor have the same resistance.**

Tateishi discloses this limitation and/or renders this limitation obvious. *See, e.g., VII.B.1.d, supra* (incorporated here); EX1003, ¶159.

VIII. DISCRETIONARY DENIAL WOULD BE INAPPROPRIATE

A. Discretionary denial under the *Fintiv* factors is not appropriate

The *Fintiv* factors favor institution. (1) No motion to stay has been filed. (2) The trial date is irrelevant considering Petitioner's stipulation below, but in any case has not yet been set. (3) The copending litigations are in relatively early stages. (4) Petitioner hereby stipulates that, if instituted, Petitioner will not pursue in District Court the specific grounds asserted here, or on any other ground that was raised or could have been reasonably raised in this IPR. *See* EX1009, EX1010. For this reason

alone, the Board should not discretionarily deny institution in view of the parallel proceedings. *See* Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” 3 (June 21, 2022). (5) Petitioner’s involvement in the parallel proceeding should not be a basis for denying institution. (6) The merits of this case are compelling for the reasons described above (§VII, *supra* (incorporated here)) and below. Accordingly, discretionary denial is inappropriate.

Further, “[T]he PTAB will not deny institution [] under *Fintiv*... when a petition presents compelling evidence of unpatentability.” June 21, 2022, Director Memo, p. 9. As an example of compelling evidence, Ground 1 explains how Tateishi anticipates every independent claim of the ’377 patent and also anticipates or, at a minimum, renders obvious, the challenged dependent claims of the ’377 patent. The Petition therefore presents very compelling reasons of invalidity and should be instituted. Moreover, Tateishi was not examined by USPTO during prosecution. And this evidence, “if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable.” Therefore, the Board must decline to exercise its discretion under §314(a) to deny institution. June 21, 2022, Director Memo, p. 4; *PopSockets LLC v. Flygrip, Inc.*, IPR2022- 00938, Paper 8 at 9 (P.T.A.B. Nov. 1, 2022).

B. Discretionary denial under 35 U.S.C. § 325(d) is not appropriate

The Board uses a two-part framework to evaluate arguments under 35 U.S.C. § 325(d): “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential). This framework is assessed under the *Becton, Dickinson* factors. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph).

1. Petitioner does not rely on the same or substantially the same prior art and arguments

Becton, Dickinson factors (a), (b), and (d) each weigh against discretionary denial under the first part of the *Advanced Bionics* framework. Tateishi was not before the USPTO. “The Board frequently holds that a reference that ‘was neither applied against the claims nor discussed by the Examiner’ does not weigh in favor of exercising the Board’s discretion under § 325(d) to deny a petition.” *Amazon.com, Inc. v. M2M Sols. LLC*, IPR2019-01204, Paper 14 at 16 (PTAB. Jan. 23, 2020); see

also *Apotex Inc. v. UCB Biopharma SPRL*, IPR2019-00400, Paper 17 at 25 (PTAB July 15, 2019).

2. **The patent office materially erred in allowing the claims of the '377 patent**

To the extent the first Advanced Bionic prong is not dispositive of §325(d) discretionary denial, allowance of the challenged claims was also material error under the second prong of the *Advanced Bionics* framework which warrants against exercise of discretion under *Becton, Dickinson* factors (c), (e), and (f). Specifically, the allowance of claims 1-5, 7-15, and 17-18 demonstrates the Examiner did not sufficiently locate, evaluate, or appreciate relevant prior art, e.g., prior art teaching using feedback from the switching node to establish the pseudo constant switching frequency, avoiding directly accessing Vout. As discussed above, Tateishi—which was not before the Examiner—anticipates, or renders obvious, the independent claims. See *Samsung Electronics Co., Ltd. v. Headwater Research LLC*, IPR2023-01157, slip op. at 6-7 (Paper 9) (Jan. 22, 2024) (granting institution where non-cumulative art, which was not before the examiner, taught a missing limitation).

The Examiner was also not presented with the substantial evidence accompanying this Petition. This evidence demonstrates the known desirability and predictability of avoiding directly accessing Vout to establish the pseudo constant switching frequency. Nor did the Examiner substantively address similar evidence

that would render Petitioner's evidence cumulative. For example, the expert declaration of Dr. Holberg (EX1003) was not of record during prosecution. EX1001, [56] References Cited.

Petitioner respectfully submits the Board should decline to exercise discretionary denial under § 325(d).

IX. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable.

Respectfully submitted,

Dated: July 23, 2024

By: /s/ Ryan N. Miller
Ryan North Miller
Reg. No. 68,262

**Counsel for Petitioner
Reed Semiconductor Corp.**

PETITIONER MANDATORY NOTICES

Real Party-in-Interest

Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner certifies that the real party-in-interest is Reed Semiconductor Corp.

Nengda Microelectronics (Shenzen) Co., LTD. (“Nengda Microelectronics”) and Nengda Semiconductor Technology (Shenzen) Co., LTD. (“Nengda Semiconductor”) are also named as real parties-in-interest in this Petition. Nengda are defendants in a separate lawsuit brought by Patent Owner, filed as related to the lawsuit against Reed. *See* Related Matters, below. Petitioner does not believe either Nengda party rises to the level of real parties-in-interest as Nengda Semiconductor is non-operational and Nengda Microelectronics has not exercised any control over this Petition or Reed’s decision to file this Petition. However, because Nengda Microelectronics and Nengda Semiconductor agree to be bound by the estoppel provisions of 35 U.S.C. § 315(e), and to prevent a costly challenge by Patent Owner regarding whether these entities are real parties-in-interest, Nengda Microelectronics and Nengda Semiconductor have been named as real parties-in-interest.

Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), to the best knowledge of the Petitioner, the ’377 patent is involved in the following cases:

• *Monolithic Power Systems, Inc. v. Reed Semiconductor Corp.*, No. 1:24-cv-00165-JFM (D. Del. filed February 8, 2024)

• *Monolithic Power Systems, Inc. v. Nengda Microelectronics (Shenzhen) Co. LTD. et al.*, No. 1:24-cv-00166-JFM (D. Del. filed February 8, 2024)

Lead and Back-up Counsel and Service Information

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Please address all correspondence to lead and back-up counsel. Petitioner consents to service in this proceeding by email at the addresses above.

Respectfully submitted,

Dated: July 23, 2024

By: /s/ Ryan N. Miller
Ryan North Miller
Reg. No. 68,262

**Counsel for Petitioner
Reed Semiconductor Corp.**

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and in reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 9,764. Pursuant to 37 C.F.R. § 42.24(a)(1), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: July 23, 2024

/s/ Ryan N. Miller
Ryan N. Miller
Reg. No. 68,262
Counsel for Petitioner
Reed Semiconductor Corp.

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.205(b), the undersigned certifies that on the 23rd day of July, 2024, a complete and entire copy of this Petition for Post Grant Review and all supporting exhibits was provided via Federal Express to:

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