

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

Petitioner

v.

MONOLITHIC POWER SYSTEMS, INC.,

Patent Owner

Case No. IPR2024-01158

Patent No. 9,041,377

PATENT OWNER'S PRELIMINARY RESPONSE

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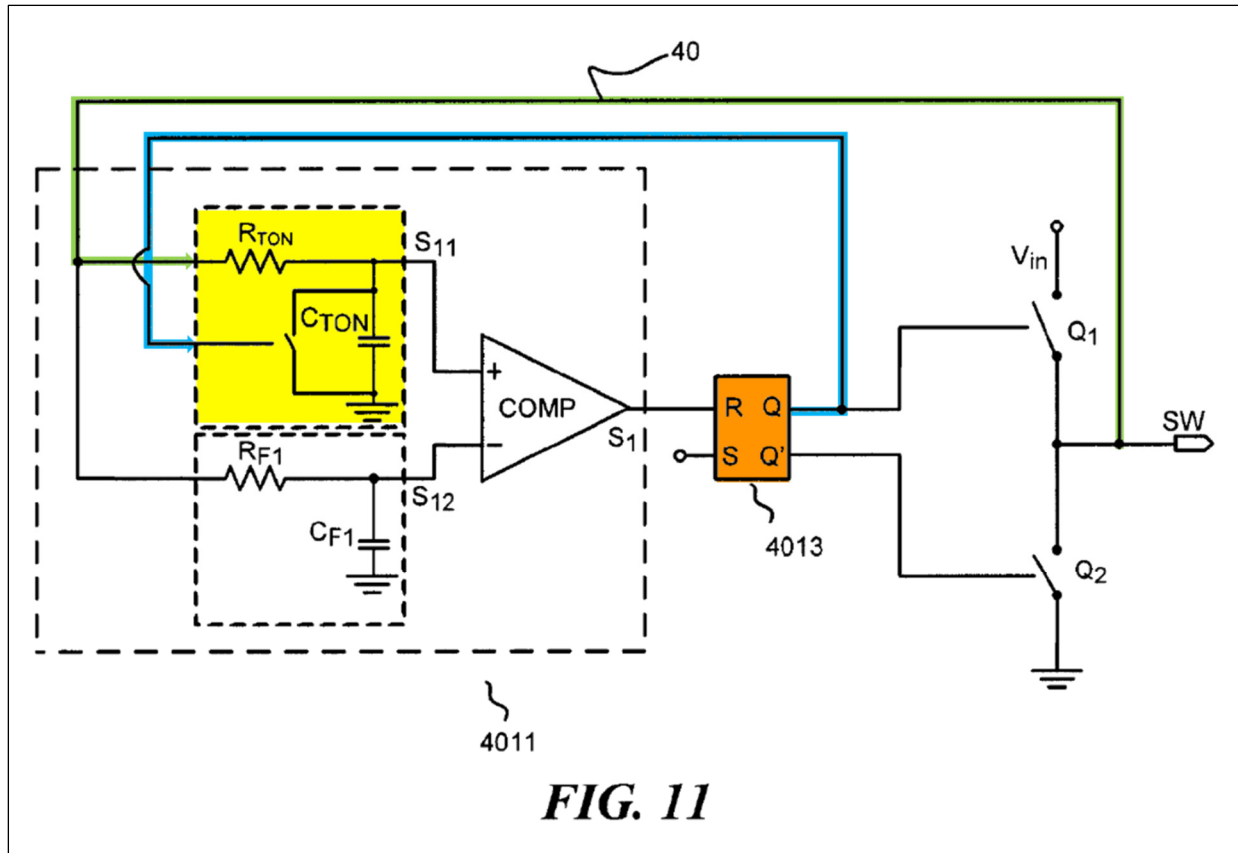
EXHIBIT LIST

Exhibit No.	Description
2001	Declaration of Joseph C. M ^c Alexander ^{III} , P.E.
2002	Curriculum Vitae of Joseph C. M ^c Alexander ^{III} , P.E.
2003	Wayback Machine May 27, 2010 Webpage Archive of Integrated Publishing's Electrical Engineering Training Series' Page Entitled "Variations of fundamental gates"
2004	Webpage of LibreTexts.org's University Physics II Text, Section 10.2, Entitled "Resistors in Series and Parallel"

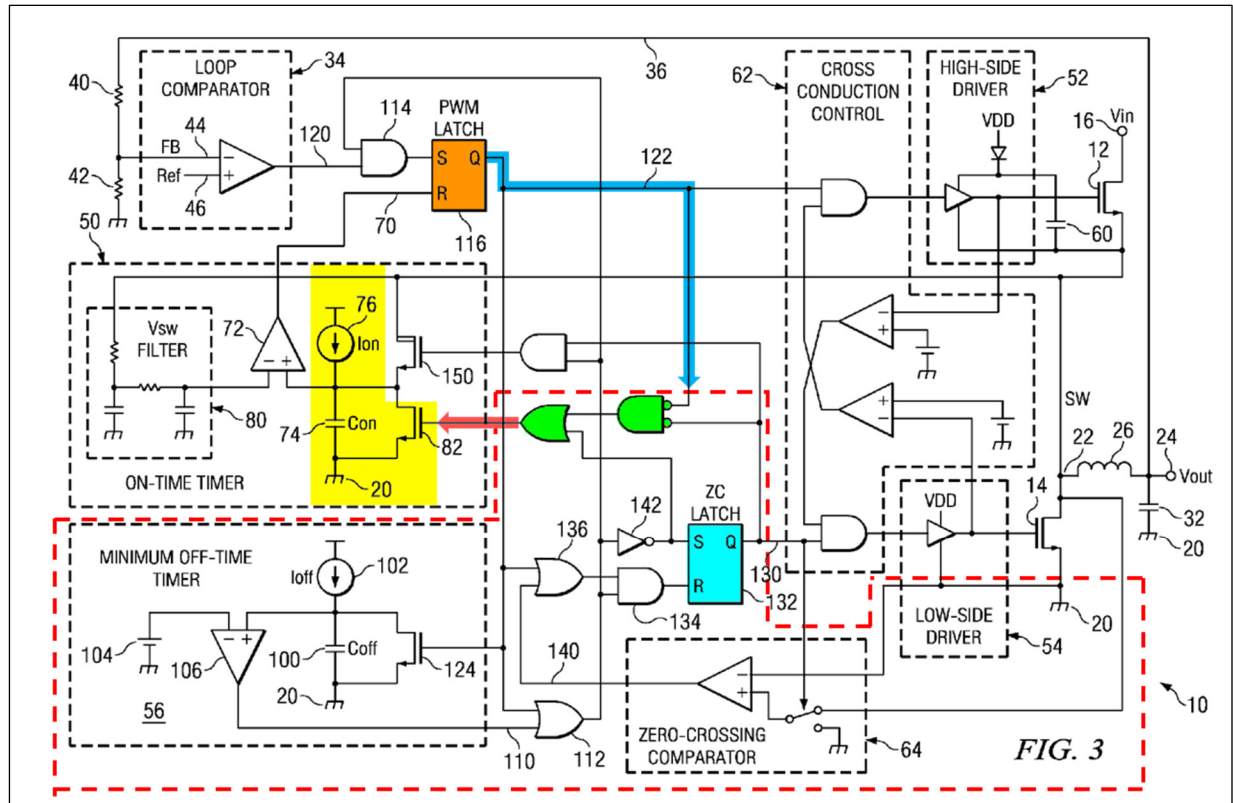
I. INTRODUCTION

Patent Owner Monolithic Power Systems, Inc. (“MPS”) hereby submits its preliminary response to the petition for *inter partes* review against U.S. Patent No. 9,041,377 (the “’377 Patent”). Petitioner’s Grounds 1 and 2 fail to present a reasonable likelihood of success, for the simple reason that Petitioner fails to identify a single signal in the prior art that corresponds to the claimed “control signal.” Instead, the Petitioner’s Grounds depend on cobbling together two different signals from the prior art to arrive at the claimed “control signal.” But this combination of two different signals does not anticipate the single “control signal.”

As shown below, the claims require—and FIG. 11 shows—a “logic control circuit” (orange) that outputs a “control signal” (blue arrow) which is then received at an “input voltage sensing circuit” (yellow) where the “input voltage sensing circuit” uses that “control signal” and another signal (a “switching signal”) (green arrow) to “generate an input voltage sensing signal.” The “control signal” is a single signal that goes from one control element as control for another.



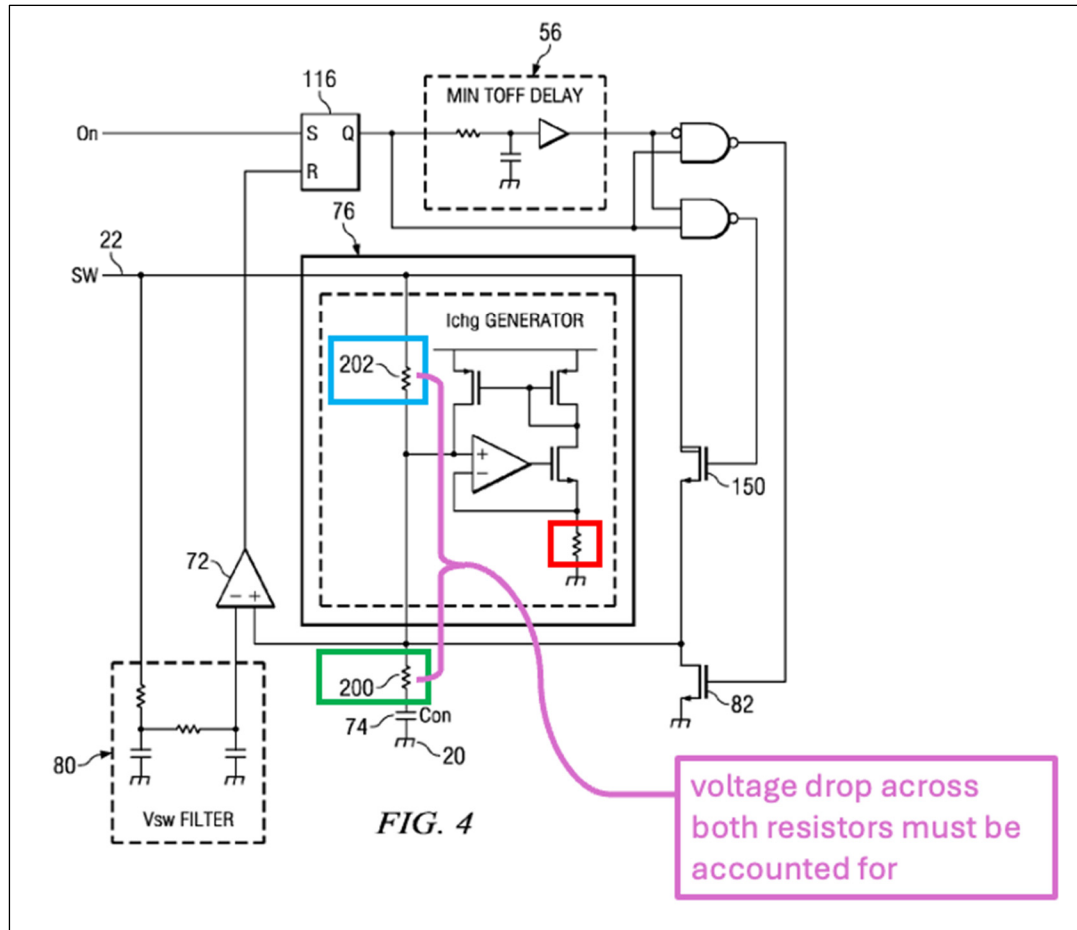
Petitioner has failed to show that this claimed structure is taught in Tateishi. Petitioner has, instead, mapped two entirely different signals—at two entirely different circuit locations—to arrive at the singularly claimed “control signal.” This is plain in the figures; Tateishi’s alleged “input voltage sensing circuit” (annotated in yellow) does not receive Petitioner’s identified “control signal” (blue arrow) from the identified “logic control circuit” (orange). Instead, the alleged “input voltage sensing circuit” receives an entirely separate logical signal (red arrow).



Here, the signal of the annotated red and blue arrows above are different logical signals; the output of a larger set of logic (annotated dashed-red above) is used as an input to the alleged “input voltage sensing circuit.” The red-arrow control signal is a result of signal from a zero-crossing latch (132) (aqua) output ANDed with inverting inputs (green) with the alleged “control signal” (blue arrow) from the alleged “logic circuit” (orange). The result of the AND (with inverting inputs) operation is further ORed (also green) with an output from another set of logical signals within logic of the dashed-red box. Petitioner treats the signals of the red and blue arrows as the same, but they are not. As a consequence, the Petition fails to demonstrate that Tateishi anticipates the claims, and therefore

Ground 1 fails.

Ground 2 challenges only the dependent claims and relies on Tateishi for the independent claims. As a consequence, Ground 2 also fails for the above reasons. Ground 2 further has another plain deficiency; claims 5, 7-8 (by dependency) and 15 require two resistors that have the same resistance values: “the first resistor and the second resistor have the same resistance.” In attempts to arrive at equivalent values for resistor 202 (annotated blue, below) and the red-annotated resistor, Petitioner applies an Ohm’s law calculation using resistor 202 but wholly ignores resistor 200 (green). Once resistor 200 is appropriately considered, resistor 202 and the red-annotated resistor are not the same value. Ground 2 thus fails to present a reasonable likelihood of success because it fails to show that Tateishi renders obvious “the first resistor and the second resistor have the same resistance.”

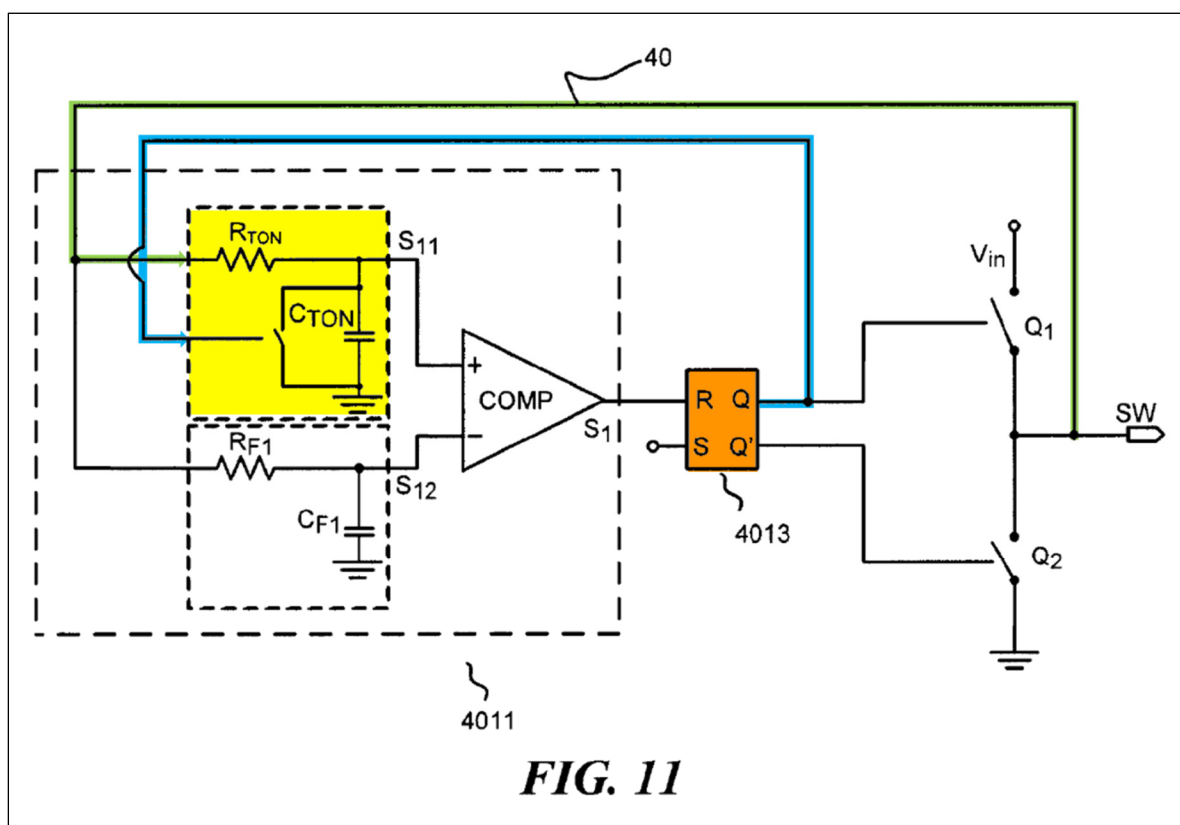


The '377 Patent and Petitioner's failures to present a reasonable likelihood of success for Grounds 1-2 are discussed in more detail below.

II. OVERVIEW OF THE '377 PATENT AND ITS RELATED TECHNOLOGY

The '377 Patent is directed towards “pseudo constant on time control circuit[s] ... [for] step-down regulators.” (EX1001 at 1:12-15; EX2001, ¶ 34.) It provides an on-time generator 4011 that has an input voltage sensing circuit (yellow) that receives a switching signal SW (green) and also a control signal (blue) from the flip-flop 4013 (orange). (EX1001 at 8:18-41; *see also id.* at FIG. 4;

EX2001, ¶ 36.) With this structure, the voltage converter does not need extra circuitry that the prior art devices needed (*e.g.*, an output voltage pin VOUT, a frequency setting pin FREQ, and the external frequency setting resistor), which reduces chip size and cost. (EX1001 at 7:65-66, 8:8-17; *see also* EX2001, ¶¶ 35-36 (describing the '377 Patent's discussion of failures in the art needing extra pins).)



Claim 1—color-coded to the above elements pertinent to this preliminary response—is annotated below.¹ (EX1001 at 9:36-10:13.)

¹ Independent claims 11 and 18 recite similar limitations. (*See generally* EX1001 at

1. A step-down regulator, comprising:

a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:

an on-time generator comprising:

an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and

a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;

a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-

11:41-12:13, 13:20-14:24.)

down regulator, and to generate an output signal in accordance with the feedback signal; and

a **logic control circuit** coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the **logic control circuit generates the control signal**; and

a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.

III. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) in the field of the ’377 Patent, as of its priority date of June 30, 2011, would have had a bachelor’s degree in Electric Engineering or equivalent, and approximately two years of experience working in the field of power converters, circuit design, device physics, or related technologies. Lack of work experience can be remedied by additional education, and vice versa. (EX2001, ¶ 32.)

IV. CLAIM CONSTRUCTION

The Board construes claims in accordance with their ordinary and customary meaning as understood by one of ordinary skill in the art. 37 C.F.R. § 42.100; *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). At this preliminary stage, and because the deficiencies of the Petition can be addressed absent construction, Patent Owner presents no constructions at this time. Patent Owner reserves the right to present constructions with the Patent Owner Response should

the Board institute the Petition.

**V. THE GROUNDS DO NOT PROVIDE A REASONABLE
LIKELIHOOD OF UNPATENTABILITY FOR ANY CLAIM**

**A. Ground 1: Petitioner has failed to show that limitation 1[B2] is
anticipated by Tateishi.**

As described below, Petitioner has failed to show that Tateishi anticipates the claimed “control signal” that is both received at the “second input terminal” of the “voltage sensing circuit” and generated by the “logic control circuit.”² (EX2001, ¶ 39.)

² Patent Owner focuses on limitation 1[B2] in its argument, but its arguments similarly apply to the other independent claims 11 and 18. Limitation 1[B2] requires that an input voltage sensing circuit (of an on-time generator) has a second input that receives a control signal, and based on the control signal, the input voltage sensing circuit generates an input voltage sensing signal. (See EX1001 at 9:39-50). Limitation 1[D], recites that a logic control circuit generates the switching signal. (EX1001 at 10:5-9). Limitations 11[B1], 11[D], 18[A], and 18[E] recite similar requirements. (See EX1001 at 11:44-53 (11[B1] similar to 1[B2]), 12:8-12 (11[D] similar to 1[D]), 13:21-25 (18[A] reciting an on-time generator receiving a control signal, and based on it, generates an on-time signal), 14:14-20 (18[E] reciting a flip-flop that generates the control signal).)

1. Anticipation Requires Each and Every Limitation in a Single Reference

“A patent claim is invalid for anticipation under 35 U.S.C. § 102 when one prior art reference describes ‘each and every claim limitation and enable[s] one of skill in the art to practice an embodiment of the claimed invention without undue experimentation.’” *In re Chudik*, 851 F.3d 1365, 1372 (Fed. Cir. 2017) (citing *ClearValue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1344 (Fed. Cir. 2012)). “[U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008).

“All of the elements and limitations of the claim must be shown in a single prior reference, arranged as in the claim.” *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). “‘It is not sufficient to constitute an anticipation that the device relied upon might, *by modification*, be made to accomplish the function performed by the patent in question, if it were not designed by its maker, nor adapted, nor actually used, for the performance of such functions.’ In other words, a prior art reference anticipates a claim only if it discloses all the elements ‘in the same form and order as in the claim.’” *In re Chudik*, 851 F.3d at 1372 (citing *Topliff v. Topliff*, 145 U.S. 156, 161 (1892) &

Abbott Labs. v. Sandoz, Inc., 544 F.3d 1341, 1345 (Fed. Cir. 2008)).

Indeed, the Federal Circuit has found against anticipation when a single reference did not disclose each and every limitation recited in the claim arranged in the same form as claimed. *See BlephEx, LLC v. Myco Indus., Inc.*, 24 F.4th 1391, 1400-02 (Fed. Cir. 2022) (affirming finding of no anticipation where prior art reference's first figure disclosed a wand and a second figure disclosed a hand-held device, but the references could not be combined to support anticipation of the claimed swab connected to an electromechanical device because no technical discussion other than attorney argument was presented to argue that a POSITA would at "at once envisage" the combination of the references); *Wonderland Nurserygoods Co. v. Baby Trend, Inc.*, 727 F. App'x 1017, 1019-20 (Fed. Cir. 2018) (reversing anticipation finding made in an IPR proceeding because the claims required that there was a single "enclosure member" (e.g., a single piece of fabric over a frame) and the prior art's disclosed netting over a frame was not continuous because the figure's depicted edges in the netting did not align); *Nidec Motor Corporation v. Zhongshan Broad Ocean Motor Co. Ltd*, 851 F.3d 1270, 1274-75 (Fed. Cir. 2017) (reversing anticipation finding made in an IPR proceeding because the claims and specification required that an "IQdr demand signal" in a "rotating frame of reference," but the petitioner only identified signals in a "stationary frame of reference" and the Board is not permitted to find

anticipation in view of a missing claim limitation); *In re Chudik*, 851 F.3d 1365, 1372-74 (Fed. Cir. 2017) (reversing the Board’s anticipation finding because the claim required that a protruding surface be “arranged to engage” (e.g., contact) a cavity, but this could only happen in the prior art if an element was removed); *Dell Inc. v. Acceleron, LLC*, 818 F.3d 1293, 1298-99 (Fed. Cir. 2016) (affirming the Board’s finding of no anticipation because, even though the prior art reference described that the CPU could boot from somewhere on the network, it did not teach booting *from the NAS*, as required by the claim); *Enfish, LLC v. Microsoft Corp.*, 822 F. 3d 1327, 1342-43 (Fed. Cir. 2016) (reversing a summary judgment granting anticipation because the claim required recited aspects of rows and columns for “a logical table,” and thus, the rows and columns needed to be in the same table, and the district court erred in construing the claim too broadly to permit the rows and columns to be from two tables); *Verve, LLC v. Crane Cams, Inc.*, 311 F.3d 1116, 1118, 1121 (Fed. Cir. 2002) (reversing anticipation finding because the prior art reference disclosed a rod that had a uniform diameter along its length (even though the ends had a smaller diameter) but the claims required a rod that had a diameter larger in the middle than towards the ends); *Gen. Elec. Co. v. Nintendo Co.*, 179 F.3d 1350, 1357 (Fed. Cir. 1999) (reversing finding of anticipation where the claims required that a television receive signals from an antenna and then to switch to receiving signals from a video player when the

player was turned on because the prior art reference did not expressly disclose the switching and defendant's argument that a POSITA would understand that this switching occurs in televisions was not sufficient to show that the limitation was actually disclosed in the reference).

The PTAB also strictly applies the requirements of anticipation. *See, e.g., U.S. Well Servs., LLC v. Halliburton Energy Servs., Inc.*, IPR2022-01163, Paper 9 at 12-14, 17, 24 (P.T.A.B. Dec. 20, 2022) (declining to institute IPR under anticipation where the claim required comparing *different* signals, but the portion of the reference cited by the petitioner only disclosed comparing *duplicate* signals); *Lenovo (United States) Inc. & Motorola Mobility LLC, v. Theta Ip, LLC*, IPR2023-00697, Paper 32 at 32-34, 37-38 (P.T.A.B. Oct. 16, 2024) (finding that a reference did not anticipate the claimed determining of signal strength of two channels at the same time because the cited portion of the reference disclosed determining the strength of *either* of two signals, but did not explicitly disclose determining strength of both at the same time); *K-40 Elecs., LLC, v. Escort, Inc.*, IPR2013-00240, Paper 37 at 34 (P.T.A.B. Sept. 29, 2014) (finding no anticipation where the claim required that a receiver receive the same signal continuously, but the portions cited by the petitioner in the reference disclosed identification from multiple sources, and thus, did not disclose a continuously received signal (but later finding the claims anticipated by another reference)); *see also Ex parte Ajay*

Mahajan and Sumeer Lal, Appeal 2010-008922 at 5 (Dec. 19, 2012) (reversing anticipation rejection because the claims required that two transducers received the *same* signal, but the alleged reference disclosed two transducers receiving *different* signals).

Finally, the Federal Circuit has held that a single claim term should be construed consistently within the claim (*i.e.*, it cannot mean multiple different elements). *Salazar v. AT&T Mobility LLC*, 64 F.4th 1311, 1317 (Fed. Cir.), cert. denied, 144 S. Ct. 422 (2023); *Rexnord Corp. v Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001); *Epcon Gas Sys., Inc. v. Bauer Compressors, Inc.*, 279 F.3d 1022, 1031 (Fed. Cir. 2002); *Harris Corp. v. Federal Exp. Corp.*, 2013 WL 174185, *4-*7 (Fed. Cir. 2013).

2. Petitioner Fails to Show that Tateishi Anticipates the Claims

Petitioner fails to show that Tateishi anticipates the single claimed “**control signal**” that is both received at the “**second input terminal**” of the “**input voltage sensing circuit**” and generated by the “**logic control circuit**,” because Petitioner relies on combining two different signals in Tateishi to reach the ’377 Patent’s “control signal.” (*See* EX2001, ¶ 39.) The fact that the two different signals in Tateishi are combined in Petitioner’s Ground 1 to arrive at the ’377 Patent’s single “control signal” means the Petition fails to demonstrate that Tateishi anticipates the ’377 Patent. *See Net MoneyIN*, 545 F.3d at 1371 (“Thus, it is not enough that the

prior art reference discloses part of the claimed invention, which an ordinary artisan might supplement to make the whole, or that it includes multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention.”).

The relevant '377 Patent limitations are annotated in the excerpt below, which plainly demonstrates limitations for the claimed apparatus that must be considered in the invalidity analysis. *In re Wilson*, 424 F.2d 1382, 1385 (1970) (“All words in a claim must be considered in judging the patentability of that claim against the prior art.”).

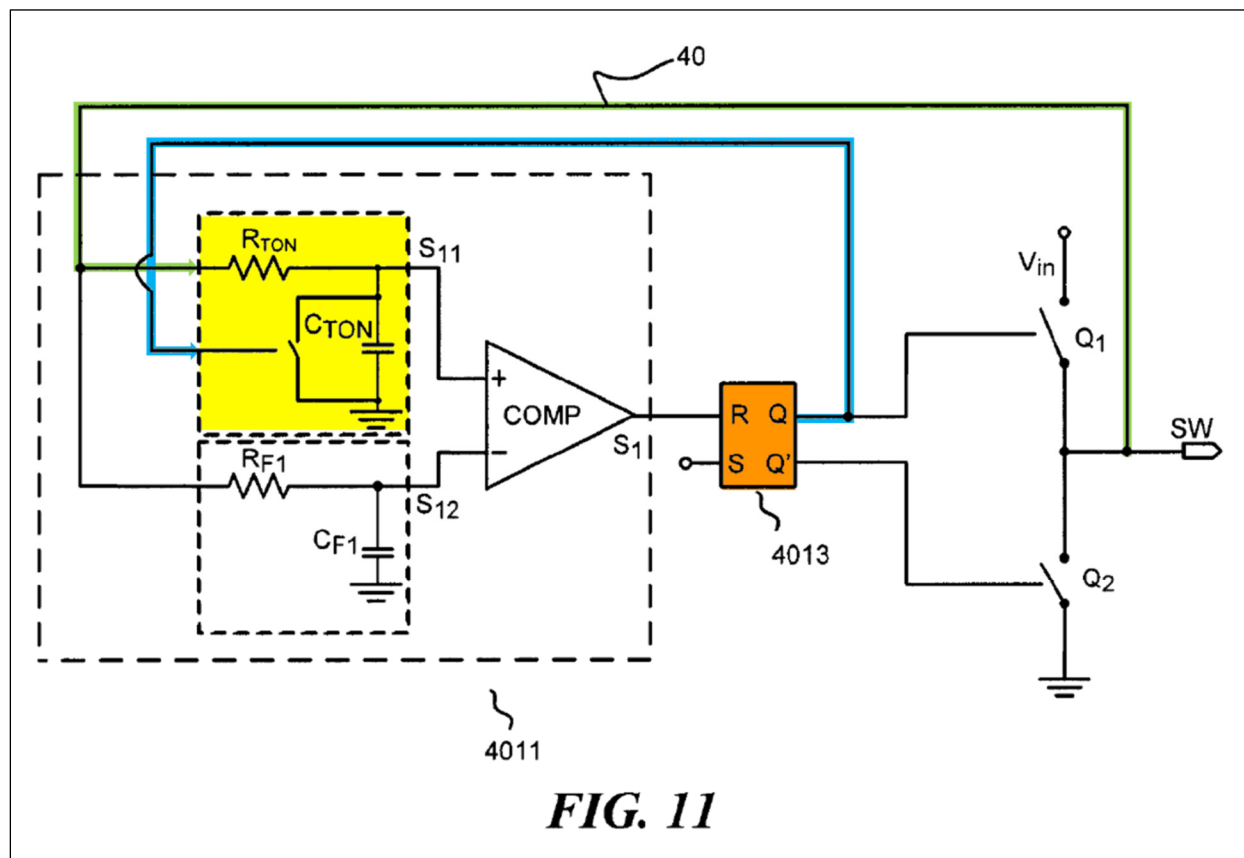
an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

....

a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and

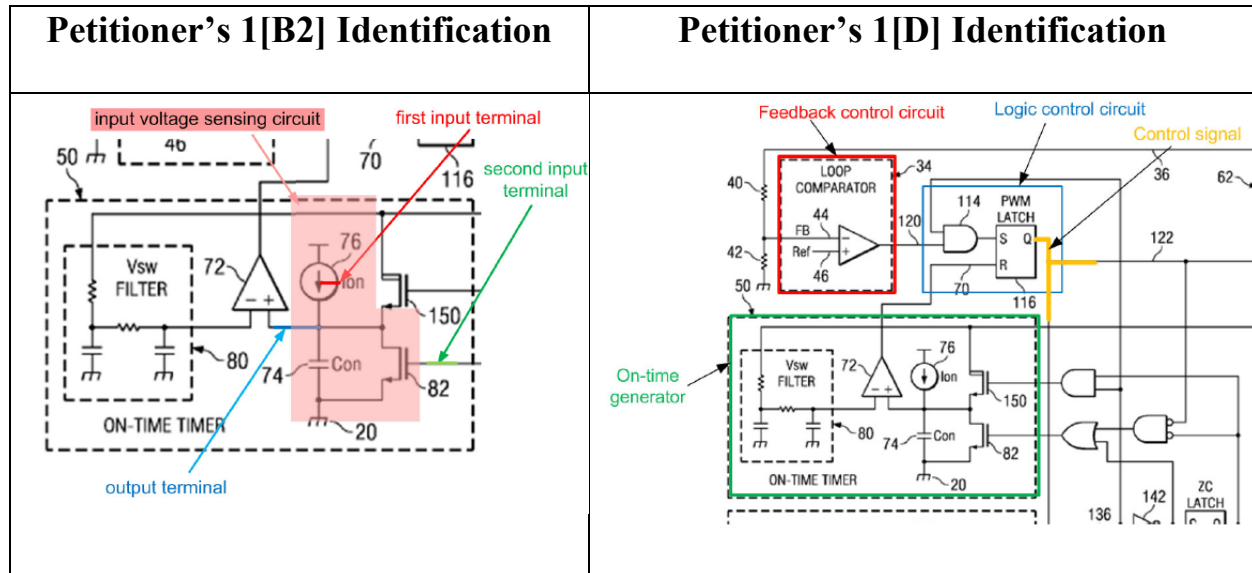
(Claim 1 (EX1001 at 9:40-50 & 10:5-9); *see* EX2001, ¶ 40.) FIG. 11 further illustrates these limitations. It teaches a “**logic control circuit**” (orange) that

outputs a “**control signal**” (blue) which is then received at a “**input voltage sensing circuit**” (yellow). ((EX1001 at 8:18-41; *see also id.* at FIG. 4; EX2001, ¶ 40.)



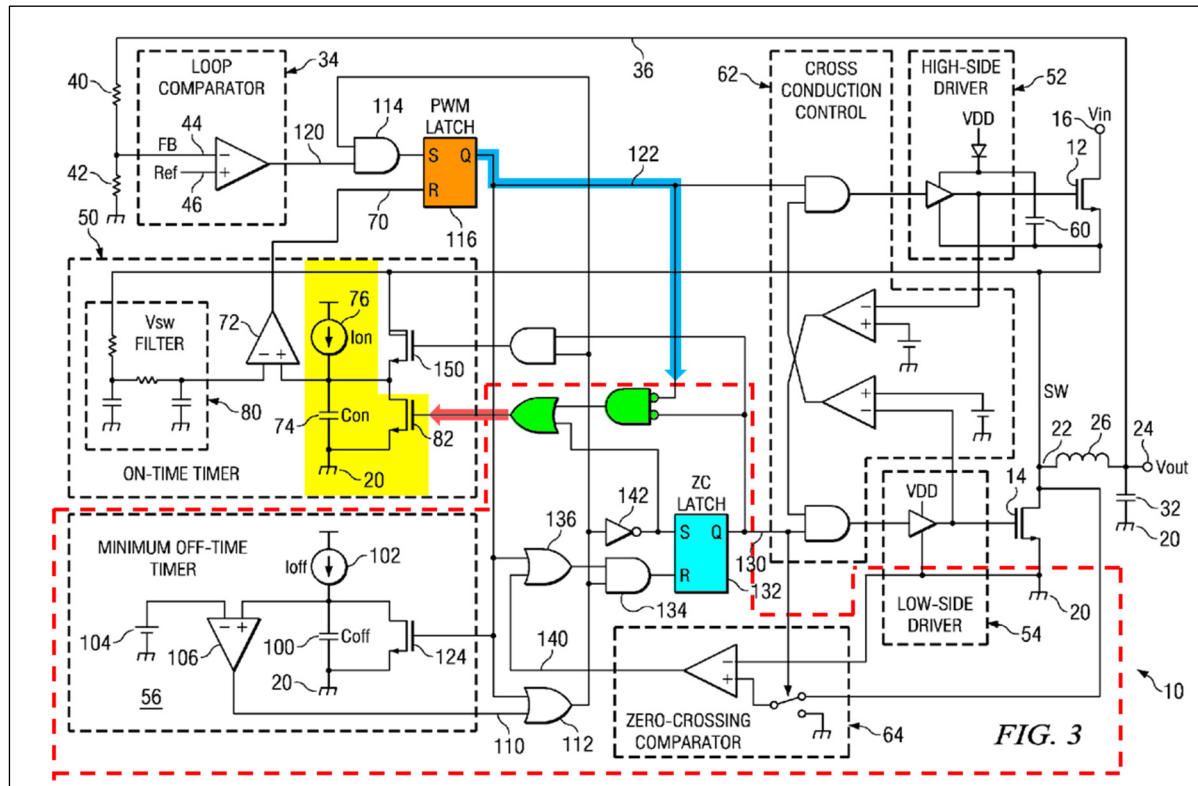
The Petition is deficient in showing that Tateishi anticipates these claim limitations. Petitioner and its expert rely on Tateishi’s FIG. 3 to teach the “second input terminal [that] is configured to receive a control signal” for limitation 1[B2]. (Paper 1 (“Pet.”) at 37 (citing FIG. 3 excerpt) (excerpted below-left); EX1003, ¶ 84; EX2001, ¶ 41.) Petitioner continues that the claimed “control signal” originates from the SR latch output 122. (Pet. at 37 (“a second input terminal configured to receive a control signal (SR latch output 122) provided by the pseudo

constant on time control circuit,”); EX1003, ¶ 84; EX2001, ¶ 42.) For limitation 1[D], Petitioner and its expert highlight the “control signal” coming from the “logic control circuit” from Tateishi’s FIG. 3. (Pet. at 45 (excerpted below-right); EX1003, ¶¶ 95-96; EX2001, ¶ 42.)



Petitioner and its expert have not shown that the Tateishi’s control signal Q, which is output from Tateishi’s PWM, is the same logical signal that enters the alleged input voltage sensing circuit. (EX2001, ¶ 43.) This is because in FIG. 3 of Tateishi (annotated below), the alleged “**control signal**” (annotated blue arrow) from the PWM latch, *i.e.*, the alleged “**logic control circuit**,” is not a pass-through signal that enters the alleged “**input voltage sensing circuit**” (yellow). (EX2001, ¶ 44.) Instead, the alleged “**control signal**” is logically processed with other signals from other logic blocks (annotated in **red-dashed**). (*Id.*) As a result, the

output logic signal that enters the “**input voltage sensing circuit**” (annotated with a **red arrow**) is different than the “**control signal**.”



The signal of the annotated **red** and **blue** arrows above are two different logical signals in Tateishi; a larger set of logic (annotated **dashed-red**) is used as an input to the alleged “**input voltage sensing circuit**.” (EX2001, ¶¶ 46-47.) The red-arrow signal is a result of signal from a zero-crossing latch (132)³ (aqua) Q

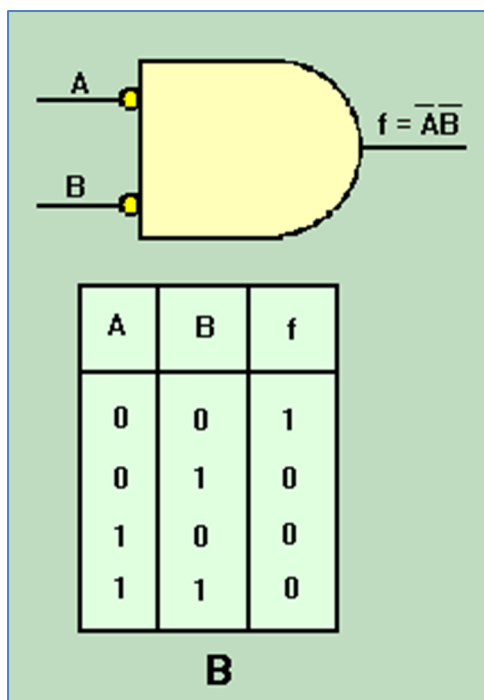
³ Tateishi further explicitly teaches that the zero-crossing comparator 64 (which affects the zero crossing latch 132) also controls the switch 82. (EX1007, ¶ 60 (“In another embodiment corresponding to the DC to DC buck converter of FIG. 3 a

output ANDed with inverting inputs (green) with the alleged “**control signal**” (blue arrow) from the alleged “**logic circuit**” (orange). (EX2001, ¶¶ 46-47.) The result of the AND with inverting inputs operation is further ORed (also green) with an output from another set of logical signals within logic of the dashed-red box. (EX2001, ¶¶ 46-47.)

Petitioner and its expert are wrong to assume that the signal Q (the alleged “control signal”) is logically the same signal that enters switch 82, particularly because the signal Q passes through the AND gate with inverting inputs. (EX2001, ¶¶ 45-46.) The truth table of a AND gate with inverting inputs shows that it only outputs a high signal (1) if both inputs are low (0), and that aside from that combination, any other change in the inputs does not change the output. (EX2001, ¶ 45; EX2003 at 2 (showing below a portion of Figure 2-18 for the AND gate with inverting inputs). Thus, control signal Q does not control the switch 82. (EX2001, ¶ 45.) Instead, the control signal Q must also be logically analyzed

zero crossing is detected. ... The zero-crossing comparator 64 detects this zero crossing and turns off the low side switch 14 through the zero crossing SR latch 132. At the same time, the precharging transistor 150 is turned off and the discharge switch 82 is turned on and maintains the voltage across the capacitor 100 at zero.”).

along with the signal that is output from ZC latch 132 (and the preceding zero-crossing comparator signal) which is affected by a larger set of computational logic. (EX2001, ¶ 45.) Petitioner’s expert never addresses this incorrect assumption and does not offer any additional discussion to remedy this shortcoming. (See EX1003, ¶¶84-88, 95-96.)



The existence of Tateishi’s AND gate with inverting inputs is further significant because the claims require that “the input voltage sensing circuit generates an input voltage sensing signal at the output terminal” “based on the switching signal and the control signal.” (See Claim 1[B2] (EX1001 at 9:47-50); EX2001, ¶ 48.) In other words, the “control signal” itself is involved in the operation to generate the “voltage sensing signal.” (EX2001, ¶ 48.) However, as depicted in the logic table above, because of Tateishi’s AND gate with inverting

inputs, the alleged control signal would not control the AND gate's output to 1 by itself (and it is instead dependent upon the value of the other signal). (EX2001, ¶ 48.) Petitioner's expert never addresses this and never offers additional discussion to remedy this issue either. (See EX1003, ¶¶84-88, 95-96.) Petitioner's identification of the "control signal" further fails for this reason. (See EX2001, ¶ 48.)

Like the Federal Circuit opinions above where the references did not anticipate the claims, the Petition here has failed to show that Tateishi's alleged "control signal" which is output from the PWM Latch 116 (the alleged "logic control circuit") is the same or equivalent logical signal that enters switch 82 (the alleged "second input terminal" of the "input voltage sensing circuit"). See, e.g., *Net MoneyIN*, 545 F.3d at 1371 (finding no anticipation where a single reference contained "multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention"); *Nidec Motor*, 851 F.3d at 1274-75 (reversing anticipation finding made in an IPR proceeding because the claims and specification required that an "IQdr demand signal" be in a "rotating frame of reference," but the petitioner only identified signals in a "stationary frame of reference" and the Board is not permitted to find anticipation in view of a missing claim limitation); *In re Chudik*, 851 F.3d at 1372-74 (reversing the Board's anticipation finding because the claim required that a protruding surface be

“arranged to engage” (e.g., contact) a cavity, but this could only happen in the prior art if an element was removed); *Dell*, 818 F.3d at 1298-99 (affirming the Board’s finding of no anticipation because, even though the prior art reference described that the CPU could boot from somewhere on the network, it did not teach booting *from the NAS*, as required by the claim).

Moreover, the Board should not venture to cure the defective petition by modifying the Petitioner’s grounds to something not presented by Petitioner. *See Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (“While the Board should not take an overly mechanistic view of a petition and decline to address an argument because the petitioner did not present it with ideal vigor and clarity, the Board should also not have to decode a petition to locate additional arguments beyond the ones clearly made.”); *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1336 (Fed. Cir. 2020) (“Although the Board is not limited by the exact language of the petition, ... the Board does not ‘enjoy[] a license to depart from the petition and institute a *different* inter partes review of his own design.’”) (citations omitted).

Petitioner’s analysis for the other independent claims (11 and 18) relies on its analysis of claim 1 and fail for the same reasons. (Pet. at 60-63; *see also id.* at 66 (relying on claim 1 analysis for the limitations of “on-time generator configured to receive ... a control signal”) and 71-72 (relying on the same flip-flop as in claim

1 to generate the control signal for the limitation of “the flip-flop generates the control signal”).)

Accordingly, Petitioner has failed to show that Tateishi anticipates the ’377 Patent’s independent claims and the Board should deny institution.

B. Ground 2: Petitioner has failed to show how dependent claims 5, 7-8, and 15 are rendered obvious by Tateishi.

Ground 2 addresses dependent claims. It does not cure the above-described deficiencies and fails for the same reasons. (*See also* EX2001, ¶ 50.)

Ground 2 further has a fatal deficiency that warrants denial of the entire Petition. It fails to show that Tateishi renders obvious “the first resistor and the second resistor have the same resistance” and Petitioner and its expert conduct impermissible hindsight when attempting to support their argument. *See Toyota Motor Corp. v. Gen. Elec. Co.*, IPR2019-00016, Paper 7 at 30 (PTAB Apr. 22, 2019) (citation omitted) (finding Petitioner did not sufficiently demonstrate why a POSITA would have been motivated to modify a reference because Petitioner and its expert relied on the challenged patent, and not the reference itself, for the support of the alleged modification); *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007) (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.”).

1. Petitioner has failed to show how dependent claims 5 and 15 are rendered obvious by Tateishi.

The Petition fails to show how Tateishi renders obvious the two resistors that have the *same* resistance as required by the claims. (See EX2001, ¶ 51.)

Specifically, claims 5 and 15 recite a current mirror that has a “second resistor” that must have the same resistance as a “first resistor” (which is first described in claims 2 and 12 respectively). (EX1001 at 10:14-18 (claim 2 reciting the first resistor), 10:62-67 (limitation 5[C] reciting the second resistor and that the first and second resistor have the same resistance), 12:13-18 (claim 12 reciting the first resistor), 12:62-67 (limitation 15[C] reciting the second resistor and that the first and second resistor have the same resistance); EX2001, ¶ 53.)

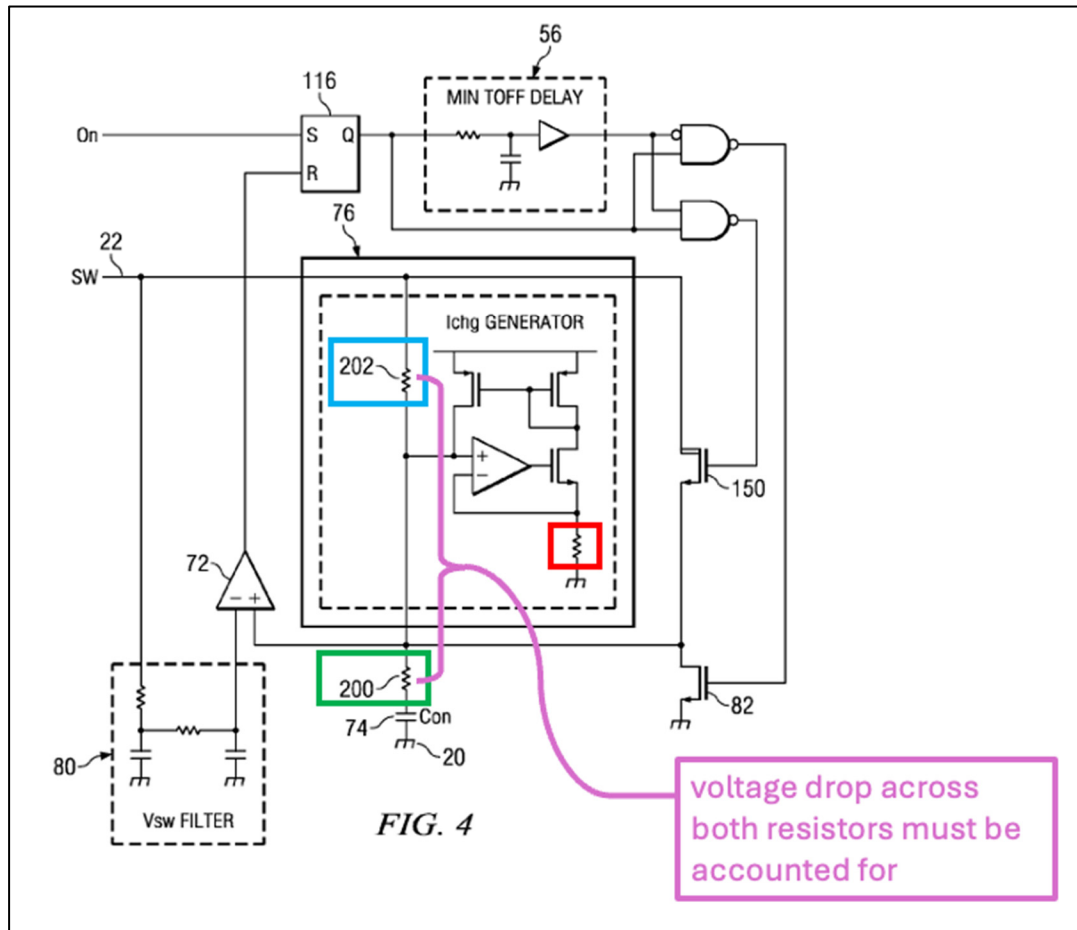
Petitioner alleges that Figure 4 of Tateishi renders limitations 5[C] and 15[C] obvious by arguing that two resistors must have the same resistance, but Petitioner explicitly ignores another resistor in Figure 4 that undermines its argument. (EX2001, ¶ 54.) As illustrated below in Figure 4, the Petition points to **resistor 202** as the “first resistor” and the **resistor in the red square** as the “second resistor.” (Pet. at 77; EX1003, ¶ 149 (same); EX2001, ¶ 55.) Petitioner argues that the **second resistor** must have the same resistance as the **first resistor**, but explicitly removes **resistor 200** from its analysis stating that:

“A POSITA would understand that the voltage across capacitor Con 74 (*neglecting resistor 200*) and the voltage across resistor 202 sum to the voltage of the switching

node.”

(Pet. at 77) (emphasis added); *see* EX2001, ¶ 54.) Petitioner’s expert also implicitly assumes that resistor 200 is not present in his discussion.

(*See* EX1003, ¶ 149.)



Petitioner cannot just “neglect” and remove **resistor 200** to make its argument that the **resistor 202** and the **second resistor** must have the same resistance. (EX2001, ¶ 56.) **Resistor 200** further cannot be removed from Figure 4 because Tateishi explains that **resistor 200** was explicitly included to

compensate for circuit delays. (EX1007 at ¶ 62 (“Specifically, this embodiment includes a resistor 200 connected in series with the capacitor Con 74 to compensate for circuit delays such as in comparators, drivers, external MOSFETS, etc., thereby reducing frequency dependence on the input Vin 16.”); EX2001, ¶ 56.) Petitioner cannot just remove an element from the Figure without conducting any analysis and assume that the circuit just works properly. (EX2001, ¶ 56.) Indeed, neither Petitioner nor its expert conduct any analysis to determine if removing resistor 200 presents issues. (*See* Pet. at 77-78; EX1003, ¶¶ 149-50; EX2001, ¶ 56.)

Because **resistor 200** cannot be removed, the voltage across both resistors **200** and **202** must be accounted for according to Ohm’s law. (EX2001, ¶ 57; *id.* (citing EX2004 at 1).) Petitioner’s argument that “the voltage across the capacitor Con 74 and **resistor 202** would sum to the voltage of the switching node (SW),” is wrong because it is the voltage across the capacitor Con 74, **resistor 200**, and **resistor 202** that would sum to the voltage of the switching node. (EX2001, ¶ 57.) Accordingly, **resistor 202** and the **second resistor** do not have the same resistance. (*Id.*)

Petitioner and its expert make no effort to explain why resistor 200 could be removed or why a POSITA would be motivated to do so. (*See* Pet. at 77-78; EX1003, ¶¶ 149-50; EX2001, ¶ 56.) This is plain improper hindsight bias using the ’377 Patent claims as a guide. “Such reliance on the challenged patent is

improper hindsight.” *Toyota*, IPR2019-00016, Paper 7 at 30 (citation omitted) (finding Petitioner did not sufficiently demonstrate why a POSITA would have been motivated to modify a reference because Petitioner and its expert relied on the challenged patent for the support of the alleged modification); *see KSR*, 550 U.S. 398 at 421 (“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.”); *Sensonics, Inc. v. Aerosonic Corp.*, 81 F.3d 1566, 1570 (Fed. Cir. 1996) (“To draw on hindsight knowledge of the patented invention, when the prior art does not contain or suggest that knowledge, is to use the invention as a template for its own reconstruction—an illogical and inappropriate process by which to determine patentability.”); *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992) (“It is impermissible to use the claimed invention as an instruction manual or ‘template’ to piece together the teachings of the prior art so that the claimed invention is rendered obvious.”); *Quanergy Sys., Inc. v. Velodyne Lidar, Inc.*, No. IPR2018-00255, Paper 62 at 21 (PTAB May 21, 2020) (“In an obviousness inquiry, ‘[t]he mere fact that a certain thing *may* result from a given set of circumstances is not sufficient.’ More aptly, rather than focus on whether a skilled artisan *could modify* the relevant art, the obviousness inquiry focuses on whether the skilled artisan *would have been led to modify* the relevant art.”) (citations omitted & emphasis in original).

Accordingly, Petitioner has failed to show that a first and second resistor have the same resistance as required by claims 5 and 15.

2. Petitioner has failed to show how dependent claims 7 and 8 are rendered obvious by Tateishi.

Dependent claims 7 and 8 stem from claim 5. For the same reasons that Petitioner has failed to show how claim 5 is rendered obvious by Tateishi, Petitioner thus has failed to show how claims 7 and 8 are rendered obvious. (*See also* EX2001, ¶ 52.)

VI. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Petition be denied.

Dated: October 29, 2024

Respectfully submitted,

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MONOLITHIC POWER SYSTEMS,
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CERTIFICATE OF WORD COUNT UNDER 37 CFR § 42.24(d)

Under 37 C.F.R. § 42.24(d), the undersigned certifies that the word count for this Patent Owner's Preliminary Response to the Petition for *inter partes* review totals 5,355, excluding the parts exempted by 37 C.F.R. § 42.24(a). The word count was made using the built-in word count function in the Microsoft® Word software used to prepare this document.

Dated: October 29, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served a true and correct copy of the foregoing: PATENT OWNER'S PRELIMINARY RESPONSE and accompanying exhibits by email to the electronic service addresses for Petitioner on the date indicated below:

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