

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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REED SEMICONDUCTOR CORP.,

PETITIONER

V.

MONOLITHIC POWER SYSTEMS, INC.,

Patent Owner.

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Case No. IPR2024-01158

Patent No. 9,041,377

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**DECLARATION OF JOSEPH C. MCALEXANDER III, P.E.**

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## LIST OF EXHIBITS

| Exhibit | Description                                                                                                                                                     |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2002    | Curriculum Vitae of Joseph C. M <sup>c</sup> Alexander <sup>III</sup> , P.E.                                                                                    |
| 2003    | Wayback Machine May 27, 2010 Webpage Archive of Integrated Publishing's Electrical Engineering Training Series' Page Entitled "Variations of fundamental gates" |
| 2004    | Webpage of LibreTexts.org's University Physics II Text, Section 10.2, Entitled "Resistors in Series and Parallel"                                               |

I, Joseph C. McAlexander<sup>III</sup> declare as follows:

1. I have been retained as an expert consultant by Perkins Coie LLP on behalf of Monolithic Power Systems, Inc. (“Patent Owner”) in this proceeding before the United States Patent and Trademark Office (“PTO”) initiated by Reed Semiconductor Corp. (“Petitioner”) regarding U.S. Patent No. 9,041,377 (“the ’377 Patent”) (Ex 1001). I have been asked to provide my technical review, analysis, insights, and opinions regarding the references that form the basis for the alleged grounds of unpatentability set forth in the Petition. For this service, I am being compensated for my time, and I am reimbursed for actual expenses. I have no interest in the outcome of this proceeding, and my compensation is not dependent on the content of my opinions or the outcome of this proceeding.

## **I. INTRODUCTION AND QUALIFICATIONS**

2. I am an independent consultant. All opinions stated in this Declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience relating to the technology referenced in this Declaration.

3. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current curriculum vitae, which includes a more detailed summary of my education and professional and academic experience is provided as Appendix A to this Declaration.

The following provides an overview of some of my experience that is relevant to the matters set forth in this Declaration.

**A. Qualifications**

4. I am a Registered Professional Engineer (#79454) and the President of M<sup>c</sup>Alexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 52 years and am a named inventor on 31 U.S. patents and a number of foreign patents.

5. I have extensive expertise in the subject matter area relevant to this matter, specifically the design, fabrication, and testing of integrated circuits, including that of power and timing control circuits embedded in integrated circuits. For example, I have over fourteen years of experience at Texas Instruments. There, I designed, developed and implemented circuits, processes, and procedures to assure product and process reliability. More specifically, I designed and managed the processing and productization of many types of integrated circuit devices, including, among others, dynamic and static storage devices, charge coupled devices (CCD) for imaging applications, electrically programmable and erasable non-volatile devices (EPROM / EEPROM) for instruction storage and access, logic devices, and controllers. I also was responsible for the design and use of many performance

boards used in testing and performance characterization of integrated circuits as well as the creation and implementation of the testing programs used to evaluate the performance characteristics of the integrated circuits. These boards required power control and signal stability for accurate assessment of device performance under various timing and power requirement conditions, adjusted according to specific, current circuit operation and load demands.

6. Additionally, while at EPI for 5 years, I managed activities which included board designs that required power and signal control. Specifically, my experience in the industry and with engineers practicing in the industry informs my opinion as to the level of skill of individuals and the general state of the art.

7. Specifically, I have:

designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both nonvolatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;

managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;

provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other), and products related to wireless tracking and geofencing; and

designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

8. I am qualified to reach the opinions and conclusions stated in this Declaration.

9. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

10. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae attached to this Declaration.

## **B. Materials Reviewed**

11. The opinions contained in this Declaration are based on the documents I have reviewed, my professional judgment, and my education, experience, and knowledge relating to power control and related fields. In forming my opinions, I

have reviewed all materials referenced by the Petition and Dr. Holberg's report and all materials listed in the List of Exhibits provided above (as well as any other materials and information I reference in this Declaration).

12. My opinions contained in this Declaration are based on the documents I have reviewed and considered, as well as my knowledge and professional judgment. My opinions have been guided by my appreciation of how a person of ordinary skill in the art ("POSITA") would have understood the state of the art, the prior art, and the claims and the specification of the '377 Patent at the time of the alleged invention.

13. The time of the alleged invention of the '377 Patent encompasses the time frames near and including June 30, 2011. I understand the application for the '377 Patent claims priority to a Chinese patent application (CN application No. 201110181295), which was filed on June 30, 2011. (Ex. 1001 at 1:7-9). My opinions reflect how a POSITA (which I describe below) would have understood the '377 Patent, the prior art to the '377 Patent, and the state of the art at the time of the alleged invention.

### **C. Summary of My Opinions**

14. The challenged claims of the '377 Patent are not anticipated or rendered obvious under 35 U.S.C. §§ 102 and 103 based on Petitioner's grounds shown in the table below:

| Ground | Claims               | Description                                                         |
|--------|----------------------|---------------------------------------------------------------------|
| 1      | 1-4, 9-14, and 17-18 | Anticipated under §102 by Tateishi and/or the Tateishi Patent.      |
| 2      | 5, 7-8, and 15       | Rendered obvious under §103 by Tateishi and/or the Tateishi Patent. |

15. Based on my experience and expertise, it is my opinion that the prior art fails to disclose and/or suggest all the limitations recited in challenged claims of the '377 Patent, as I discuss in detail below.

## **II. UNDERSTANDING OF LEGAL PRINCIPLES AND PERSPECTIVES**

16. I am not a lawyer, and I will not provide legal opinions. Although I am not a lawyer, I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

17. I understand that a patent claim is invalid if it is anticipated or rendered obvious over the prior art and that a claim can be unpatentable even if all requirements of the claim cannot be found in a single prior art reference. I further understand that invalidating a claim requires that the claim be anticipated or rendered obvious from the perspective of a POSITA at the time the invention was made.

18. In forming my analysis, opinions, and conclusions expressed in this Declaration, I have applied the legal principles set forth below, which were provided to me by counsel for Patent Owner.

**A. Types of Claims**

19. I understand that there are two types of U.S. patent claims: 1) independent claims, and 2) dependent claims. I understand that independent claims only include the aspects stated in the independent claim. I further understand that dependent claims include the aspects stated in the independent claim, and any other aspects stated in any claim from which that dependent claim depends, as well as any limitations required by the dependent claim.

**B. Anticipation**

20. I understand that a claim in an issued patent can be invalid if it is anticipated. In this case, “anticipation” means there is a single prior art reference that discloses every element of the claim, arranged in the way required by the claim, either expressly or inherently.

21. I understand that anticipation of a claim requires that every element of a claim is disclosed expressly or inherently in the single prior art reference. I understand that “inherent” disclosure means that the claim element, although not expressly described by the prior art reference, must necessarily be present based on the disclosure. I understand that a mere probability that the element is present is not sufficient to qualify as “inherent disclosure.”

**C. Obviousness**

22. I understand that a claim in an issued patent can be rendered invalid if it is obvious. Unlike anticipation, obviousness does not require that every element of the claim be in a single prior art reference. Instead, it is possible for claim elements to be described in different prior art references or that a claim element in a prior art reference might be modified, so long as there is motivation or sufficient reasoning to combine the references or make the modification and a reasonable expectation of success of doing so.

23. I understand that a claim is invalid for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious from the perspective of a person of ordinary skill in the relevant art at the time the invention was made. I also understand that, when evaluating obviousness, one must consider obviousness of the claim “as a whole.” This must be from the perspective of the person of ordinary skill in the relevant art at the time the invention was made.

24. I further understand that exemplary rationales that may support a conclusion of obviousness include:

- a) combining prior art elements according to known methods to yield predictable results;
- b) simple substitution of one known element for another to obtain predictable results;

- c) use of known technique(s) to improve similar devices (methods or products) in the same way;
- d) applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- e) “obvious to try” - choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- f) known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a POSITA; and
- g) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

25. In analyzing obviousness, I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any “secondary considerations” (described below). I also understand that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Although I understand that it is not required, there may also be a specific “teaching, suggestion or motivation” to combine any first prior art reference with a second prior art reference. Such a “teaching, suggestion, or motivation” to combine the first prior art reference with the second

prior art reference can be explicit or implicit and may provide further evidence of obviousness.

26. I understand that secondary (or objective) considerations are relevant to the determination of whether a claim is obvious. Such secondary (or objective) considerations can include evidence of commercial success caused by an invention, evidence of a long-felt need that was solved by an invention, evidence that others copied an invention, or evidence that an invention achieved a surprising or unexpected result, among others. I understand that such evidence must have a nexus, or causal relationship to the elements of a claim, to be relevant to a determination of obviousness of the claim.

27. I also understand that, at least in IPR proceedings, admissions in the patent or in the prosecution file history of the patent (Applicant Admitted Prior Art or “AAPA”) can be used to establish background knowledge possessed by a POSITA, to furnish a motivation to combine, to assess whether a patent’s claims would have been obvious, and/or to supply a missing limitation.

**D. Claim Construction**

28. I understand that, for purposes of my analysis, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning” at the time the alleged invention was made. In determining the ordinary and customary meaning, the words of a claim are given the plain meaning that those

words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to assist in the construction of a claim term. Additionally, treatises and dictionaries may be used, in limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing as long as such extrinsic input is consistent with the claim term as used in the claim.

29. For all claim terms considered in this Declaration, I have applied the ordinary and customary meaning of those terms as they would have been understood by a POSITA at the time the alleged invention was made. To the extent the Patent Owner proposes any constructions, or the Board construes any claims, I reserve the right to address such proposals or constructions. Under any reasonable construction of the claims, it is my opinion that the prior art does not disclose and/or suggest all the limitations recited in challenged claims of the '377 Patent.

**E. Person of Ordinary Skill in the Art**

30. I understand that my assessment and determination of invalidity must be undertaken from the perspective of what would have been known or understood by a POSITA at the time of the earliest patent application supporting the '377 Patent.

31. I have been informed and understand that the POSITA is not a real person, but rather a legal construct—a hypothetical person. This person is presumed to have known the relevant art at the time of the invention. I have been informed by

counsel that relevant factors in determining the level of ordinary skill include (1) the educational level of the inventor, (2) the type of problems encountered in the art, (3) prior art solutions to those problems, (4) the rapidity with which innovations are made, (5) sophistication of the technology, and (6) the educational level of active workers in the field. I further understand that the person of “ordinary skill” is not a person of extraordinary skill in the art. In other words, this person of ordinary skill is not necessarily an expert in the field.

32. As of the alleged June 30, 2011 priority date, a POSITA would have had a bachelor’s degree in Electric Engineering or equivalent, and approximately two years of experience working in the field of power converters, circuit design, device physics, or related technologies. Lack of work experience can be remedied by additional education, and vice versa.

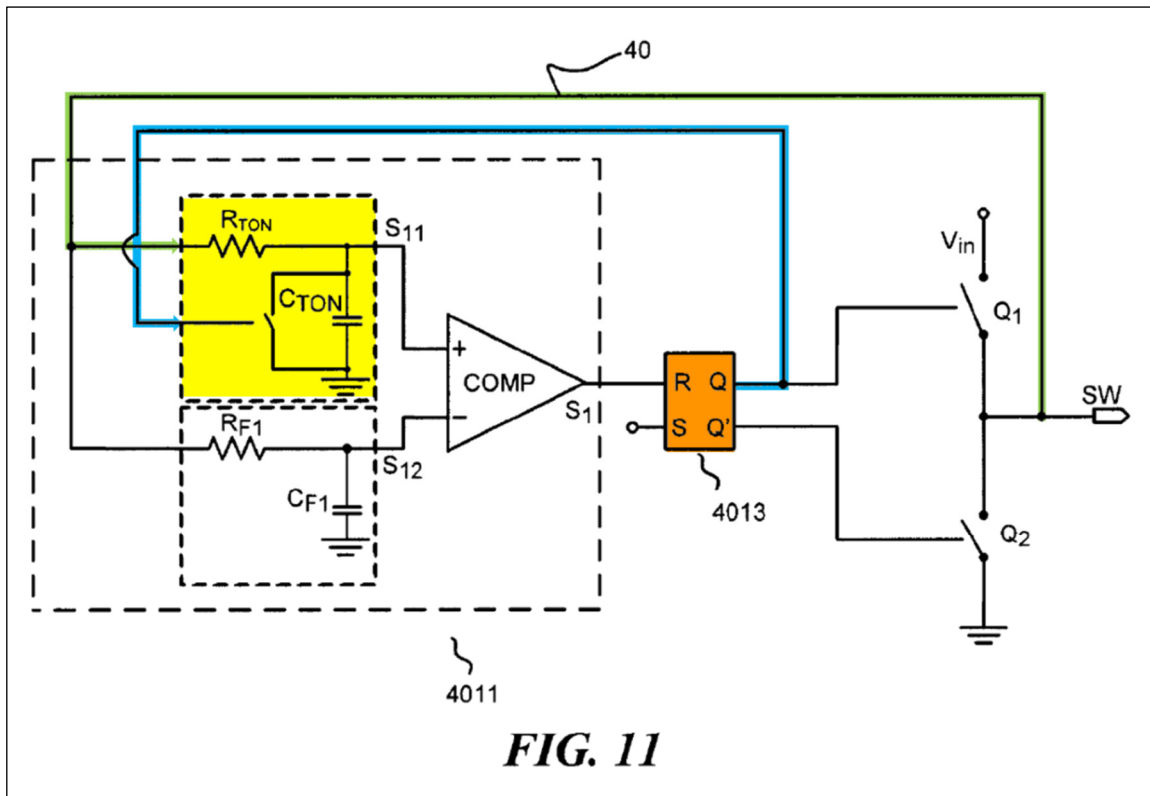
33. At the time of the alleged invention, I was a person of at least ordinary skill in the art, and I have applied the perspective of the POSITA in forming and expressing my opinions below.

### **III. BACKGROUND OF THE ’377 PATENT**

34. The ’377 Patent is directed towards switching circuits, and “more particularly but not exclusively to pseudo constant on time control circuit[s] and step-down regulators using it.” (EX1001 at 1:12-15).

35. The '377 Patent explains that in pseudo constant on time (PCOT) control types for regulator circuits, the “on-time” of the regulator must be proportional to the output voltage divided by the input voltage:  $V_{OUT}/V_{IN}$ . (EX1001 at 1:55-64). The '377 Patent also explains that the switching frequency of the regulator is constant and does not vary with the output power. (EX1001 at 2:6-10). To achieve these aspects, the '377 Patent explains that prior art regulators implementing PCOT control need an output voltage pin  $V_{OUT}$  in the chip and may also need a frequency setting pin along with an external frequency setting resistor. (EX1001 at 2:11-20). The output voltage pin and frequency setting pin increase the chip size and cost. (*Id.*).

36. The '377 Patent reduces the need for the output voltage pin and the frequency setting pin. The '377 Patent describes that one way it achieves this is by providing an on-time generator 4011 that has an input voltage sensing circuit (yellow) that receives a switching signal SW (green) and also a control signal (blue) from the flip-flop 4013 (orange) (EX1001 at 8:18-41; *see also id.* at FIG. 4). Accordingly, the voltage converter does not need an output voltage pin  $V_{OUT}$ , a frequency setting pin  $FREQ$ , and the external frequency setting resistor, which were needed by the prior art; this helps reduce chip size and cost. (EX1001 at 7:65-66, 8:8-17).



37. Independent claim 1 recites that there is an input voltage sensing circuit (of the pseudo constant on time control circuit) (highlighted in yellow, to match the highlighted figured above) that receives the switching signal (highlighted in green) and the control signal (highlighted in blue), and a logic control circuit (highlighted in orange) generates the control signal:

1. A step-down regulator, comprising:

a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:

an on-time generator comprising:

an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal

provided by the step-down regulator, **the second input terminal is configured to receive a control signal** provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and

a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;

a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and

**a logic control circuit** coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, **the logic control circuit generates the control signal**; and

a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.

38. Independent claims 11 and 18 have similar limitations, as discussed above.

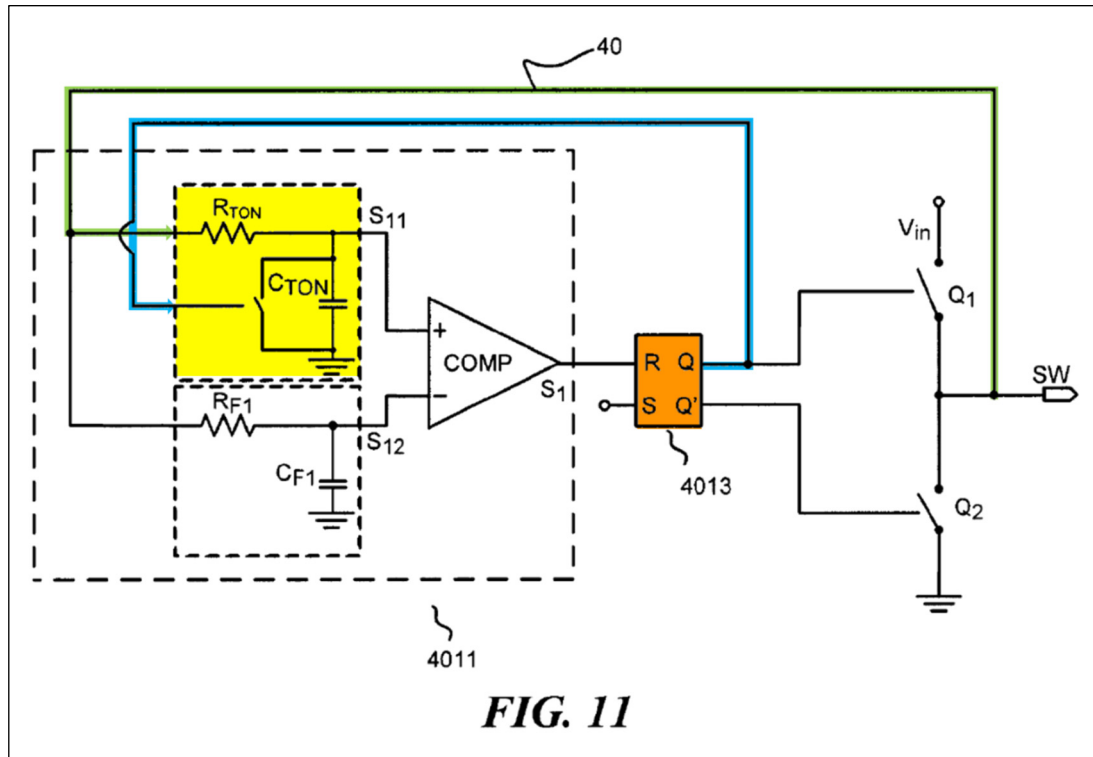
#### IV. REASONS FOR PATENTABILITY

**A. Ground 1: Petitioner has failed to show that Tateishi anticipates the independent claims of the '377 Patent.**

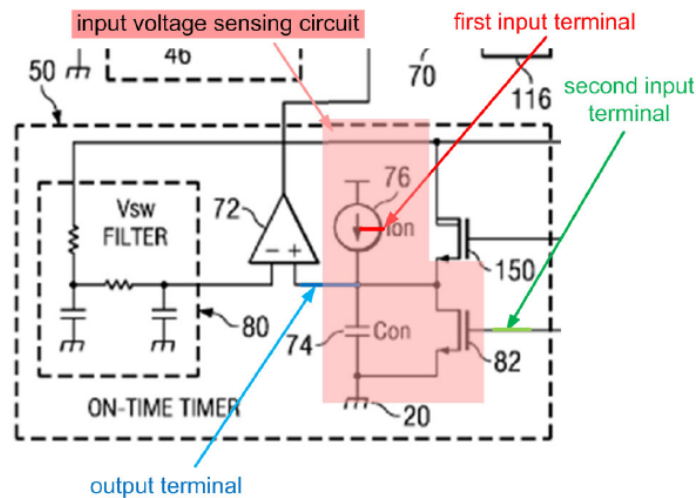
39. In my opinion, Petitioner has failed to show that Tateishi anticipates the independent claims of the '377 Patent. Specifically, as I described above, the claims require that the “second input terminal” of the “voltage sensing circuit” (or the “on-time generator” for the claim 18) receives a control signal. The independent claims also require that a “logic control circuit” (or flip flop for claim 18), generates the control signal. I understand that anticipation requires each and every limitation to be disclosed in a single reference. Petitioners, however, fail to show, in my opinion, that Tateishi anticipates the claimed “control signal” that is both received at the second input terminal of the input voltage sensing circuit (or, just the on-time generator for claim 18) and also generated by the logic control circuit (or by the flip-flop for claim 18). I will expand on my opinion in the following paragraphs.

40. I focus on claim 1 because it is representative of my position for all of the independent claims. (*Compare Claim 1 with Claims 11 and 18*). Claim 1 requires, as I described above, that there is a “**control signal**” that is both received at the “**second input terminal**” of the “**input voltage sensing circuit**” and generated by the “**logic control circuit.**” (*See claim 1 of the '377 Patent*). As a non-limiting

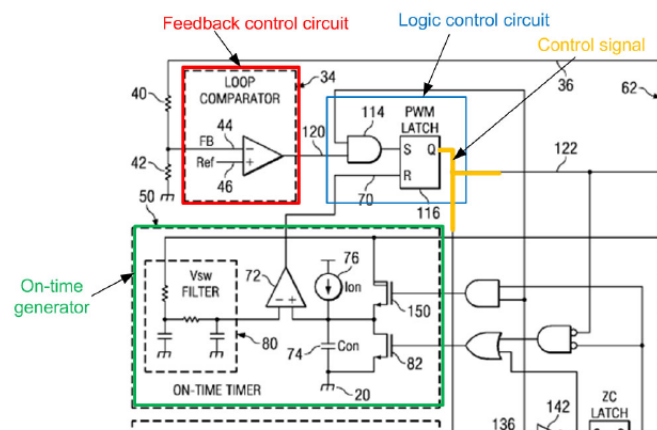
example, Figure 11 (annotated and reproduced below) of the '377 Patent illustrates this. A “**logic control circuit**” outputs a “**control signal**” which is then received at a “**input voltage sensing circuit.**” (EX1001 at 8:18-41; *see also id.* at FIG. 4).



41. Petitioner relies on Figure 3 of Tateishi to meet this claim language. Specifically, limitation 1[B2] requires that the “second input terminal is configured to receive a control signal,” and Petitioner relies on Figure 3 of Tateishi to identify the “second input terminal.” (Petition at 37). Petitioner’s annotation of Figure 3 is reproduced below. (See Petition at 37).

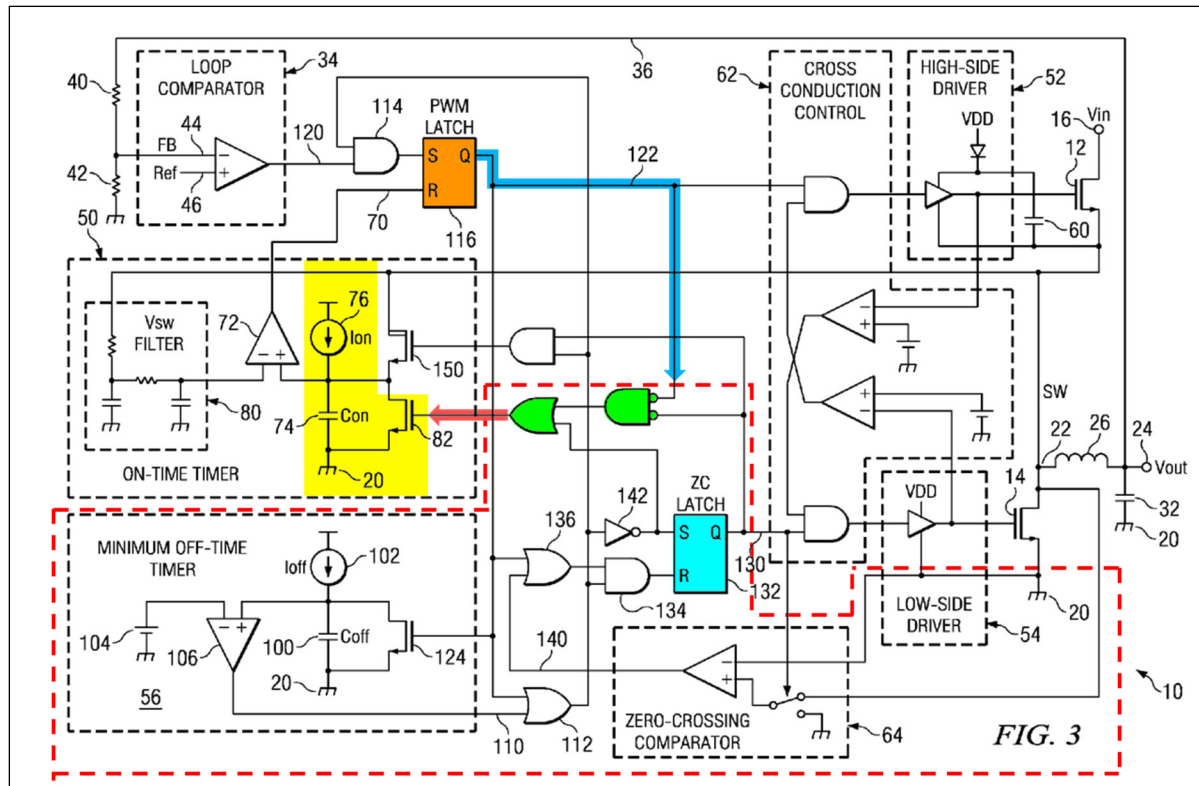


42. Petitioner also relies on Figure 3, for the requirement that a logic control circuit output the control signal. Petitioner alleges that the control signal 122 originates from the SR latch 116 output. (Petition at 37 (“a second input terminal configured to receive a control signal (SR latch output 122) provided by the pseudo constant on time control circuit”). Also, in limitation 1[D], Petitioner annotates and relies on Figure 3 (a copy of which is reproduced below), and Petitioner identifies the control signal is the signal output 122 from the PWM latch 116 in Figure 3. (Petition at 45).



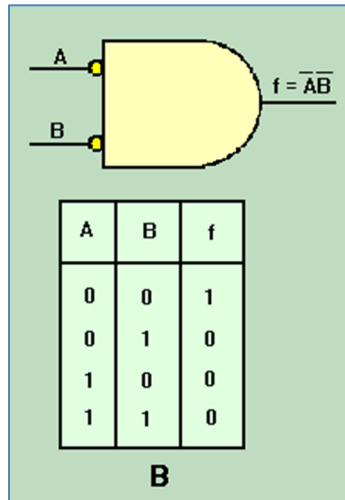
43. In my opinion, Petitioner has not shown that Tateishi's control signal that is output from the alleged "logic control circuit" is the control signal that enters the input voltage sensing circuit (of the on-time generator), as required by the claims. Specifically, Petitioner has not shown that the control signal Q, which is output from Tateishi's PWM latch 116 is the same logical signal that enters the second input of the input voltage sensing circuit, which is what Petitioner alleges is switch 82 of the on-time generator 50.

44. This is because, as shown in the reproduced and annotated Tateishi Figure 3 below, the alleged "**control signal**" from the PWM latch (which is the alleged "**logic control circuit**") is not, in my opinion, a pass-through signal that enters the alleged "**input voltage sensing circuit.**" The alleged "**control signal**" is logically processed with other signals from other logic blocks (annotated in **dashed-red-line**).



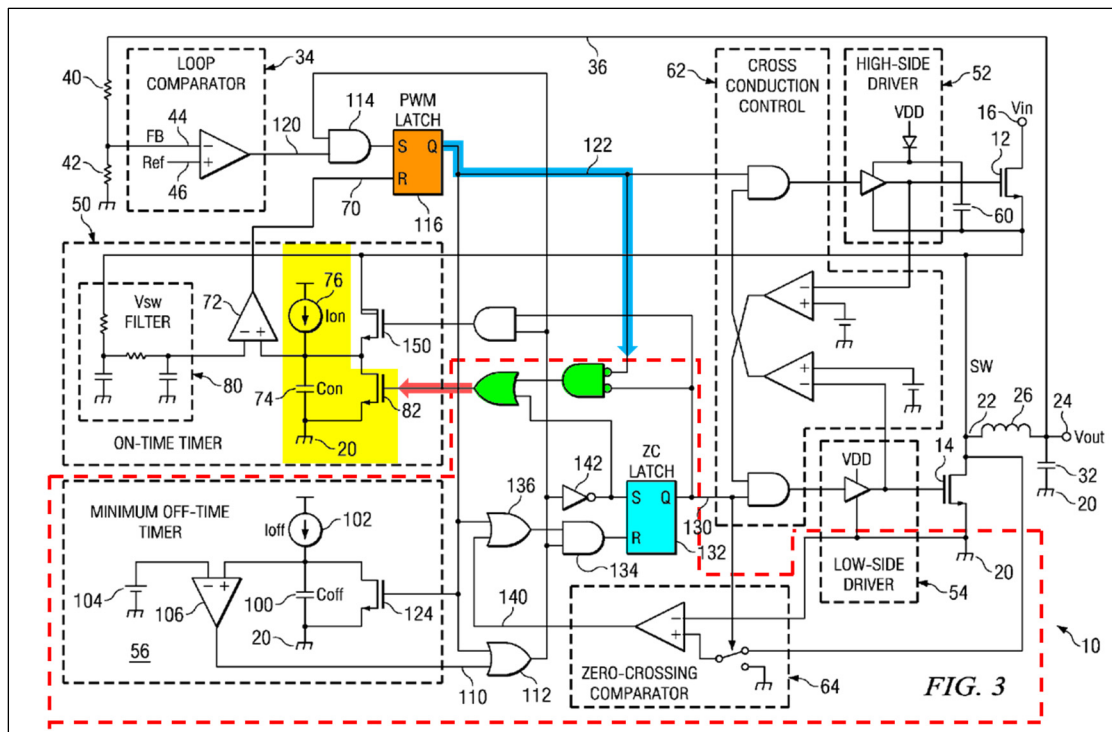
45. Specifically, the alleged “**control signal 122**” is one input into what is referred to as an **AND gate with inverting inputs**. Another inverted input to that **AND gate** is the output of the **ZC latch 132** (see above). An AND gate with inverting inputs only outputs a high signal if both input signals are low. This can be seen from what is referred to as the “truth table” of a logic device (such as an AND gate with inverting inputs). The truth table (shown below) illustrates that, with such a device, the AND gate only outputs a high signal if both input signals are low, and if any of the inputs are high, then the output is low. (Ex. 2003 at 3 (showing a portion of Figure 2-18 for the AND gate with inverting inputs)). Thus, a POSITA would understand that the output of the AND gate with inverting inputs is not just

dependent on whether the alleged control signal is high or low, but also whether the ZC latch output signal is high or low. If both signals become low, then the output of the AND gate with inverting inputs is high, but otherwise, if either the alleged control signal or the LC latch output signal goes high, then the entire AND gate (with inverting inputs), would go low.



46. Thus, the logical output of the **AND gate with inverting inputs** is dependent upon the logical values of *both* the alleged “**control signal 122**” and the output of **ZC latch 132** (see below). The **ZC latch 132 output Q** is dependent upon other signals from other logic blocks (annotated in the **dashed-red-line** below). For example, Tateishi states that the zero-crossing comparator 64, which affects the **ZC latch 132** input, also controls the effect of the input 122 to switch 82 and is thus, an arbitration input into the identified second input of the input voltage sensing circuit. (EX1007, ¶ 60 (“In another embodiment corresponding to the DC to DC buck

converter of FIG. 3 a zero crossing is detected. The zero-crossing comparator 64 detects this zero crossing and turns off the low side switch 14 through the zero crossing SR latch 132. At the same time, the precharging transistor 150 is turned off and the discharge switch 82 is turned on and maintains the voltage across the capacitor 100 at zero.”).



47. Thus, Petitioner has not shown, and cannot show, in my opinion, that the alleged **control signal Q** is the signal that enters the **input voltage sensing circuit**. The **red-arrow signal** (which is the signal entering the alleged **input voltage sensing circuit**) is a result of the signal from the **ZC latch 132 S input Ored** with the output of an **AND gate** which receives **inverting inputs** of the alleged “**control signal**” from the alleged **logic circuit** and the **ZC latch 132 Q output**. The

result of the **AND with inverting inputs** operation is, therefore, **ORed (also green)** with an output from another set of logical signals within logic of the dashed-red box. Accordingly, the alleged **control signal** is logically processed with other signals, and as a result, the **output logic signal** that enters the “**input voltage sensing circuit**” (annotated with a **red arrow**) is different than the **control signal**.

48. Additionally, independent claim 1 requires that “the input voltage sensing circuit generates an input voltage sensing signal at the output terminal” “based on the switching signal and the control signal.” (*See* Claim 1[B2]). Accordingly, the “control signal” helps generate the input voltage sensing signal that is output from the input voltage sensing circuit according to the claims. For Tateishi, however, as I described above, the alleged “control signal” does not enter the “input voltage sensing circuit” because the “control signal” enters the AND gate with inverting inputs and is combined with other logic. Thus, as I described above, even if the “control signal” changes from a high to low signal, the AND gate with inverting inputs still will not change its output from low to high until the other input (*e.g.*, the output from the ZC latch) also transitions to or is low. Thus, the input voltage sensing circuit’s output is not dependent on the control signal by itself and is instead dependent upon the value of the other signal (*e.g.*, the ZC latch output). Accordingly, the Petitioner has failed to address the significantly different AND gate with inverting inputs, and has thus failed to show how the input voltage sensing

signal is based on the control signal itself.

49. For the foregoing reasons, it is my opinion that the Petitioner has failed to show that Tateishi anticipates the independent claims of the '377 Patent.

50. Petitioner does not appear to use Ground 2 to fix any of these issues either.

**B. Ground 2: Petitioner has failed to show that Tateishi renders obvious dependent claims 5, 7-8, and 15 of the '377 Patent.**

51. It is my opinion that the Petitioner has failed to show that Tateishi renders obvious claims 5, 7-8, and 15.

52. Claims 7 and 8 depend from Claim 5. Claims 5 and 15 are similar. While I analyze claim 5, my discussion applies equally to claim 15. And because it is my opinion that claims 5 and 15 are not rendered obvious by Tateishi, claims 7 and 8 are also not rendered obvious because they depend from claim 5.

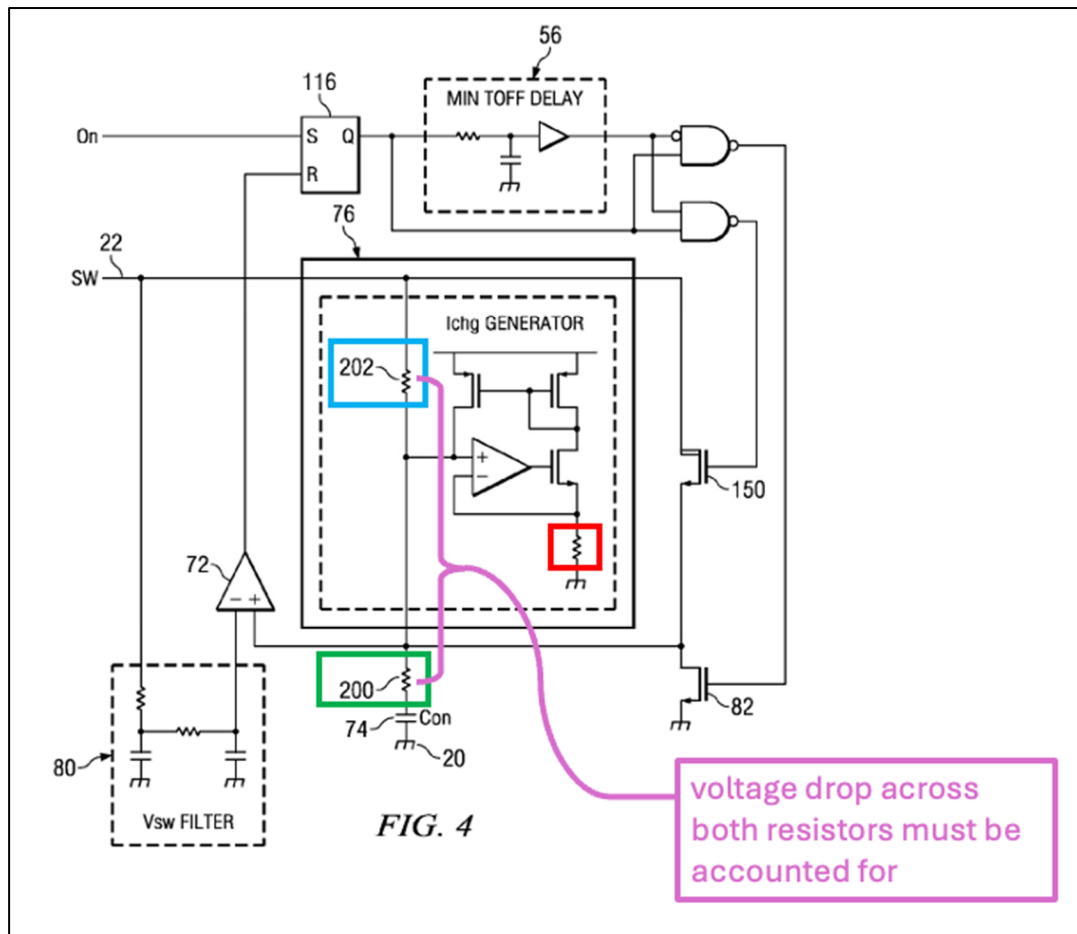
53. Claim 5 requires a current mirror that has a “second resistor” that must have the same resistance as a “first resistor” (which is first described in claims 2 and 12). (EX1001 at 10:14-18 (claim 2 reciting the first resistor), 10:62-67 (limitation 5[C] reciting the second resistor and that the first and second resistor have the same resistance)). Thus claim 5 (which 15 mirrors) requires that a first and second resistor have the same resistance.

54. Petitioner points to Tateishi Figure 4 to alleged support for this

requirement. Specifically, Petitioner argues that two resistors (which it identifies in Figure 4 of Tateishi) must have the same resistance, but Petitioner explicitly states that it ignores another resistor in order to make this assumption. (Petition at 77). Petitioner states: “A POSITA would understand that the voltage across capacitor Con 74 (*neglecting resistor 200*) and the voltage across resistor 202 sum to the voltage of the switching node.” (Pet. at 77 (emphasis added)).

55. Specifically, Petitioner points to **resistor 202 in the blue box** as the “first resistor” and the **resistor in the red square** as the “second resistor” and tries to remove consideration of **resistor 200** from Figure 4. (Petition at 77; *see* Figure 4 (annotated below)).

56. Petitioner cannot neglect **resistor 200**, in my opinion. First, I understand that Petitioner and its expert needed to explain why this resistor can be removed or why a POSITA would be motivated to do so. They did not. (*See* Petition at 77-78; EX1003, ¶¶ 149-50). Second, Tateishi explicitly states that resistor 200 was included to compensate for circuit delays. (EX1007, ¶ 62). I do not see anywhere in the Petitioner or in its expert’s report where they analyze the circuit of Figure 4 to conclude that a POSITA would be motivated to remove resistor 200, which is important especially where Tateishi specifically includes resistor 200 to account for delays. For example, are there situations where removing resistor 200 would cause issues because the circuit does not have a proper delay?



57. Because resistor 200 cannot be removed, the voltage across both resistors 200 and 202 must be taken into account according to Ohm's law. Petitioner argues that the resistance between the switching node (SW) and capacitor 72 must be equal to the resistance of the "first resistor" (in the red square), in order for the current mirror 76 to work properly. (See Petition at 77-78). Assuming that this is true (which I do not concede is correct), the resistance of both resistor 200 and resistor 202 would be considered collectively to determine the resistance of the "first resistor." According to Ohm's law, where there are multiple resistors in series (on

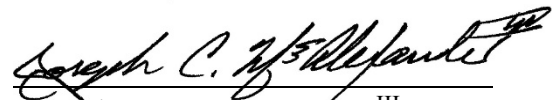
the same conductor), the resistors are considered together to determine the total resistance along the conductor. (Ex. 2004 at 1). Thus, even if the Petitioner is right that the resistance between the switching node (SW) and capacitor 72 must be equal to the resistance of the “first resistor” (in the red square), the resistance between the switching node (SW) and capacitor 72 would be equal to the sum of both resistors  $R_{202} + R_{200}$  because resistor 200 cannot just be removed as I describe above. Thus,  $R_{202} + R_{200} = R_{\text{FIRST\_RESISTOR}}$ , and  $R_{202} \neq R_{\text{FIRST\_RESISTOR}}$  as argued in the Petition.

58. For the foregoing reasons, it is my opinion that Petitioner and its expert have failed to show that Tateishi renders obvious claims 5, 7-8, and 15.

## V. CONCLUSION

I hereby declare that all the statements made in this declaration are based on my own true knowledge, that all statements made on information and belief are believed to be true, and that all statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under the penalty of perjury under the laws of the United States that all statements made in this declaration are true and correct.

Dated this 28 day of October, 2024

  
Joseph C. McAlexander III, P.E.