

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP

Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.

Patent Owner.

Case No. IPR2024-01158

U.S. Patent No. 9,041,377

PATENT OWNER'S RESPONSE

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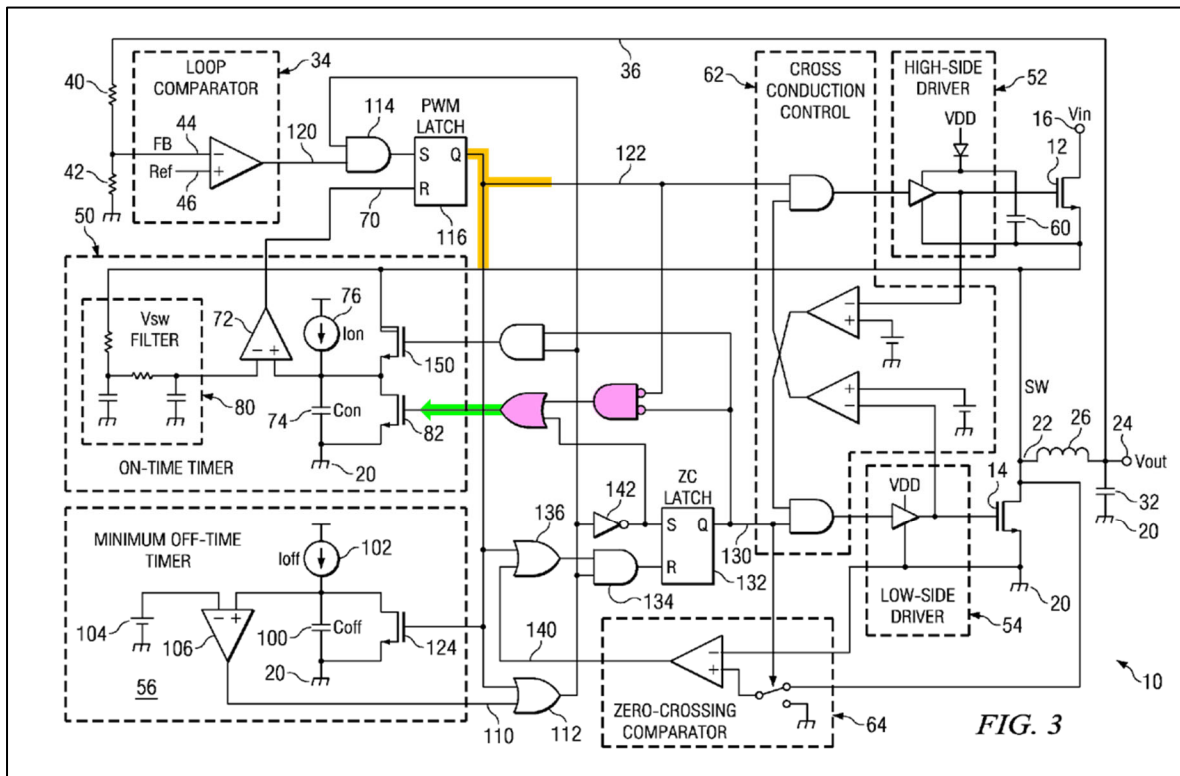
Exhibit	Reference
2001	Declaration of Joseph C. McAlexander ^{III} , P.E.
2002	Curriculum Vitae of Joseph C. McAlexander ^{III} , P.E.
2003	Wayback Machine May 27, 2010 Webpage Archive of Integrated Publishing's Electrical Engineering Training Series' Page Entitled "Variations of fundamental gates"
2004	Webpage of LibreTexts.org's University Physics II Text, Section 10.2, Entitled "Resistors in Series and Parallel"
NEW EXHIBITS	
2005	Second Declaration of Joseph C. McAlexander ^{III} , P.E.
2006	Excerpts of the April 9, 2025 - Deposition Transcript of Douglas R. Holberg, Ph.D.

I. INTRODUCTION

Patent Owner Monolithic Power Systems, Inc. ("MPS") hereby submits its Patent Owner Response for *inter partes* review against U.S. Patent No. 9,041,377 (the "'377 Patent"). Petitioner's Grounds 1 and 2 fail for several reasons.

Ground 1 does not demonstrate that Tateishi¹ anticipates the claimed "control signal." Claim 1 requires that "a control signal" be generated by a "logic control circuit" and that "the control signal" also be inputted into an "input voltage sensing circuit." Because Tateishi does not teach this, Petitioner relies on two separate logic signals (annotated in green and orange, below) as the "control signal" despite them being separated by logic gates (pink). Petitioner's analysis fails for several reasons.

¹ "Tateishi" throughout this Response refers to U.S. Patent App. Pub. No. 2009/0140708 (EX1007). The Board instituted with reference to EX1007 and not the Tateishi Patent (EX1005). (*See* Paper 6 at 38 ("Petitioner has not demonstrated a reasonable likelihood of prevailing on a Tateishi Patent anticipation challenge.")) The disclosures are substantively identical and the arguments apply to both.



First, Petitioner fails to track the antecedent basis of the “control signal” across the claim limitations. Petitioner identifies the above-annotated orange signal to meet the limitations of 1[D] but identifies the green signal to meet the limitations of 1[B2]. These are two separate logical signals; Petitioner’s analysis fails to track the claims term’s antecedent basis.

Second, even if the Board were to assume that both annotated signals can be the “control signal” at the same time, and they cannot, the Petition still fails to demonstrate that those combined signals satisfy a proper construction of the “control signal,” which is a “logic signal with two distinct states.” The two annotated signals have inconsistent logic states and serve different purposes. The green signal acts as

an output of the embodiment's internal logic to control switch 82. The signal's logical value is affected by the values of the orange signal along with two other logic signals from other logical blocks (the minimum off time circuit and a zero-crossing circuit). As a result, the green and orange signals cannot both constitute the claimed "control signal."

Third, the Petition's analysis of portions of the control signal further fails with respect to other phrases of the claim that recite the "control signal." Two separate output signals ("input voltage sensing signal" and "switching signal") are generated based on an operation with the "control signal" along with a separate logic signal ("switching signal" and "input voltage," respectively). Here, like for 1[B2] and 1[D], Petitioner takes each of the above-annotated signals and analyzes one signal in isolation of the other. This too fails to track the antecedent basis of the claimed "control signal" and is, moreover, improper under the proper construction because these are two logically incompatible signals.

Ground 1 further fails because the Petition presents an obviousness analysis in its anticipatory ground. The Petition picks and chooses elements from two separate embodiments (Figures 3 and 4) to create an amalgamation of features. Namely, it takes the "switching signal" of Figure 4 and injects it into Figure 3, but in doing so, Petitioner ignores that Figures 3 and 4 are distinctly different embodiments with different control schemes. Petitioner fails to demonstrate how the four corners of

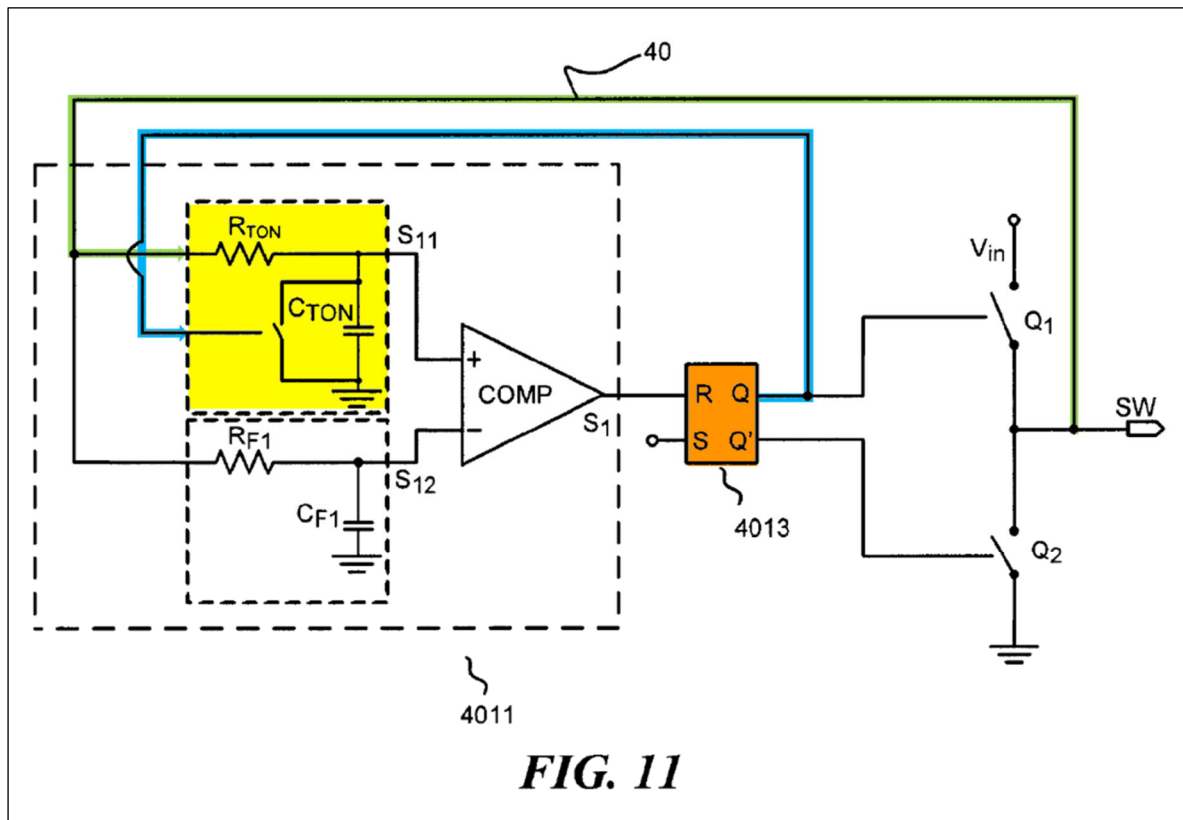
Tateishi discloses its combined embodiment and thus fails to present a ground of anticipation.

Ground 2 challenges only the dependent claims and relies on Tateishi for the independent claims which fail for the reasons presented above.

The '377 Patent and Petitioner's failures for Grounds 1-2 are discussed in more detail below.

II. OVERVIEW OF THE '377 PATENT AND ITS RELATED TECHNOLOGY

The '377 Patent is directed towards “pseudo constant on time control circuit[s] ... [for] step-down regulators.” (EX1001 at 1:12-15; EX2005, ¶ 34.) It provides an on-time generator 4011 that has an input voltage sensing circuit (yellow) that receives a switching signal SW (green) and also a control signal (blue) from the flip-flop 4013 (orange). (EX1001 at 8:18-41; *see also id.* at FIG. 4; EX2005, ¶ 36.) With this structure, the voltage converter does not need extra circuitry that the prior art devices needed (*e.g.*, an output voltage pin VOUT, a frequency setting pin FREQ, and the external frequency setting resistor), which reduces chip size and cost. (EX1001 at 7:65-66, 8:8-17; *see also* EX2005, ¶¶ 34–36 (describing the '377 Patent's discussion of failures in the art needing extra pins).)



Claim 1—color-coded to the above elements—is annotated below.² (EX1001 at 9:36-10:13; EX2005, ¶¶ 37–38.)

1. A step-down regulator, comprising:
 - a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:
 - an on-time generator comprising:
 - an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the

² Independent claims 11 and 18 recite similar limitations. (See generally EX1001 at 11:41-12:13, 13:20-14:24.)

control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;
an output voltage sensing circuit having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the output voltage sensing circuit generates an output voltage sensing signal at the output terminal; and
a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, the comparator generates an on-time signal at the output terminal;
a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal;
and
a **logic control circuit** coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the **logic control circuit generates the control signal;** and
a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.

III. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) in the field of the ’377 Patent, as of its priority date of June 30, 2011, would have had a bachelor’s degree in Electrical Engineering or equivalent, and approximately two years of experience working in the field of power converters, circuit design, device physics, or related technologies.

Lack of work experience can be remedied by additional education and vice versa.
(EX2005, ¶ 32.)

IV. CLAIM CONSTRUCTION

A. “control signal” is a “logic signal with two distinct states”

Claims should be construed “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. §42.100(b); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

A POSITA would have understood that the plain and ordinary meaning of the term “control signal” is a “logic signal with two distinct states.” (EX2005, ¶ 40.) Petitioner's usage of the term improperly interprets it to mean two signals that have multiple contradictory logic states at the same time. (EX2005, ¶ 57.)

The “control signal” required in the claims and described in the specification is a logic signal with two distinct states generated from—and provided to—specific hardware elements. (EX2005, ¶¶ 41–56.)

Patent Owner's construction is supported by the claims. (EX2005, ¶¶ 41–47.) In the claims, the control signal is generated by a logic control circuit (claim 1 at 1[D] (EX1001 at 10:8-9) (or a flip-flop (claim 18 at 18[E] (*id.* at 14:18-19))). The control signal is also connected to specific inputs, such as a second input terminal of the input voltage sensing circuit (claim 1 at 1[B2] (*id.* at 9:44-45) and an on-time

generator (claim 18 at 18[A] (*id.* at 13:22-23). The control signal is further used by other circuit elements to generate logic signals, *e.g.*, used by the power stage to generate a switching signal (claim 1 at 1[E] (*id.* at 10:10-13 and claim 18 at 18[F] (*id.* at 14:21-24).

Dr. Holberg (Petitioner's expert) agrees that the control signal is a logic signal with two distinct states. He testified that:

Q Back to the claim language. 10 5 through 9 states that “the logic control circuit generates a control signal.”

You see that?

A Yes.

Q Do you understand the control signal that is generated to be a two-state signal?...THE WITNESS: Yes.

(EX2006 at 22:11-19; *see also* EX2005, ¶ 48.)

Q If you could look at the control signal in column -- hold on. Let me see -- 14, lines 19 to 20. It says: “The flip-flop generates the control signal.”

A Yep, I see that.

Q In your opinion, is the control signal of claim 18 a two-state signal?

A Yes.

(EX2006 at 25:10-18; *see also id.* at 14:15-18:4 (stating that the signal Q from the specification is a two-state signal).)

The various components of the claims—control signal (blue), logic control circuit/flip-flop (orange), input voltage sensing circuit/on-time generator (yellow),

power stage (aqua)—are annotated below in the excerpted claim phrases.³ (EX2005, ¶¶ 45–46.) The “control signal” is generated via logic and provided as an input to various other circuit elements.

Claim 1

1. A step-down regulator, comprising:

...

an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive a control signal provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

...

a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and
a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.

³ Claim 11 recites the input voltage sensing circuit and logic control circuit but lacks a claimed power stage. (EX1001 at 11:41-12:13; EX2005, ¶ 44.) Claim 18 additionally recites an off-time generator. (EX1001 at 14:1-4; EX2005, ¶ 44.)

Claim 18

18. A step-down regulator, comprising:

an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;

a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;

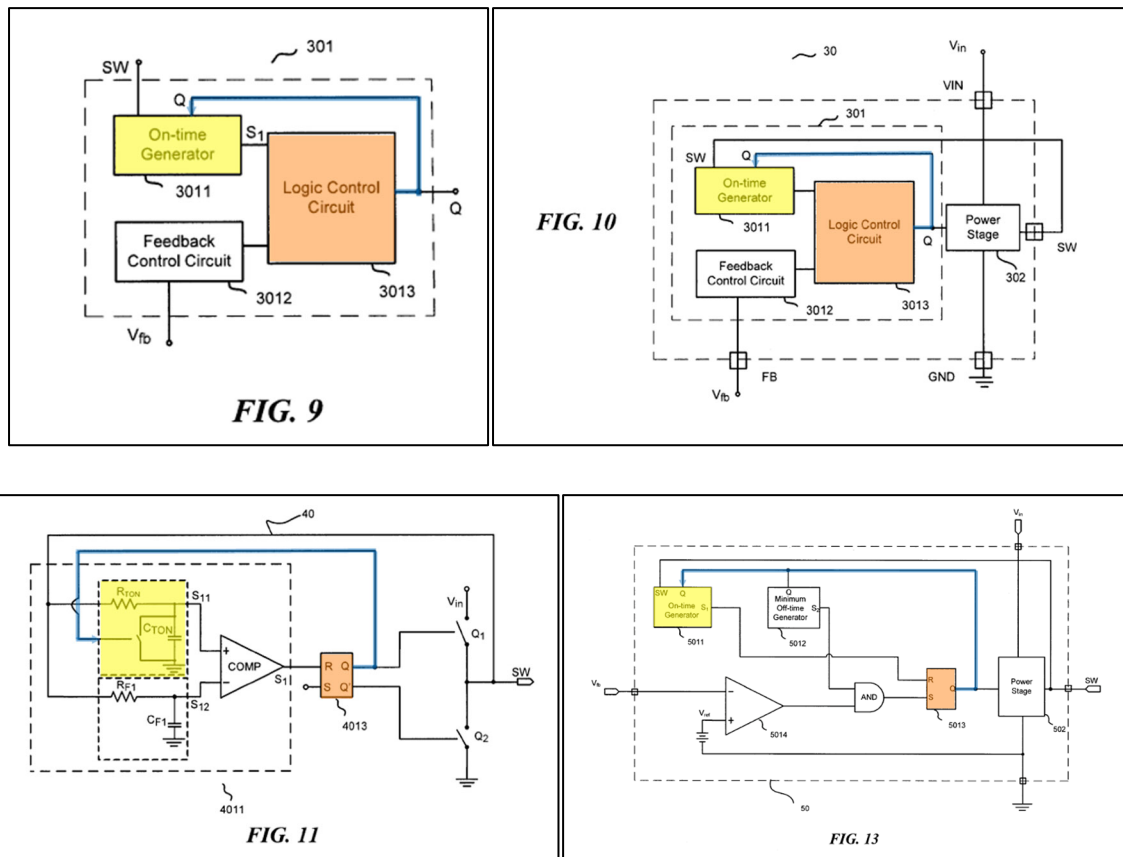
...

a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and

a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.

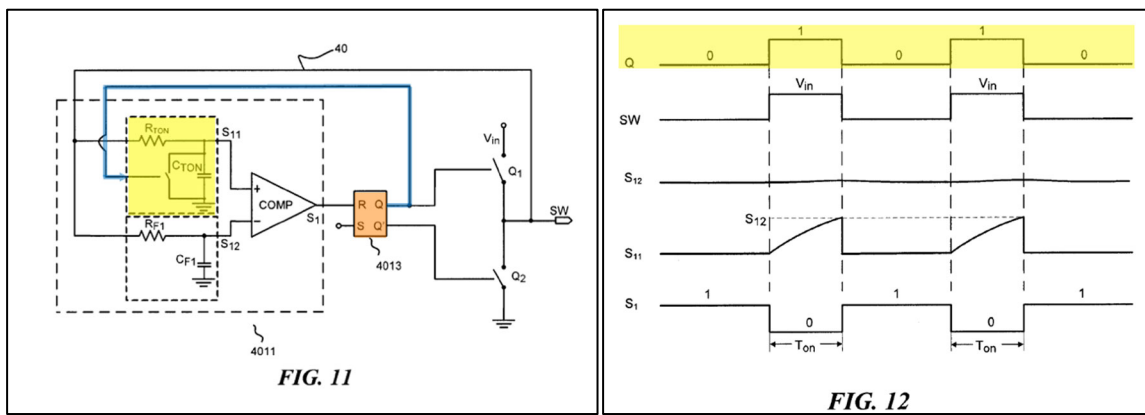
The “control signal” is similarly described in the specification as a logic signal with two distinct states. (EX2005, ¶¶ 49–54.) In the embodiments, *e.g.*, Figs. 9, 10, 11, and 13, the “control signal” Q is output from the logic control circuit (or flip-flop) and enters the on-time generator (or the on-time generator’s input voltage sensing circuit). (EX1001 at 7:44-47 (Fig. 9: “The on-time generator 3011 receives . . . a control signal Q provided by the PCOT control signal 301”), 7:65-66 (“FIG. 10 illustrates a step-down regulator 30 comprising the PCOT control circuit 301 of FIG. 9.”), 8:28-30 (“As shown in FIG. 11, the on-time generator 4011 receives . . . the

control signal Q provided by the flip-flop 4013”), 8:66-9:1 (FIG. 13: “The on-time generator 5011 receives . . . a control signal Q provided by the flip-flop 5013”).) These four figures are annotated below, with control signal Q (blue) between the logic control circuit (orange) and the on-time generator (yellow). (EX2005, ¶¶ 50–51.)



Figures 11 and 12 make-clear that the “control signal” is a logic signal with two distinct states. (EX2005, ¶¶ 52–53.) In Figure 11, the specification distinguishes Q from its inverse Q’, and thus, Q has a logical value of 0 or 1. (EX1001 at 8:32-34 (“The control signal Q controls the high-side switch Q1, and the

complementary signal Q' of the control signal Q controls the low-side switch Q_2 .”); *see also* EX1001 at 8:43-44, 8:53-55 (stating that flip-flop 4103 outputs a logic signal of a ‘1’ or a ‘0’).) Figure 12, moreover, provides timing diagrams describing the specific logical values (‘1’ or a ‘0’). (EX1001 at 8:43-44 (“As shown in FIG. 11 and FIG. 12, when $Q=1$, the high-side switch Q_1 is turned on . . .”), 8:53-56 (“The on-time signal S_1 resets the flip-flop 4013 to change the control signal Q into logical low ($Q=0$). Thus, the high-side switch Q_1 is turned off, and the low-side switch Q_2 is turned on . . .”).)



Dr. Holberg (Petitioner's expert) agrees that the embodiments describe the control signal as a logic signal with two distinct states. He testified that:

Q If I understand you correctly, you're stating that the signal Q from the logic control circuit is a two-state signal? . . .

THE WITNESS: . . . So the patent speaks of it in terms logical values 0 and 1.

(EX2006 at 16:19-17:21; EX2005, ¶ 54.)

Dr. Holberg, moreover, confirmed that the specification lacks any indication that the control signal would be an analog signal. (EX2005, ¶ 55.)

Q Is the signal an analog or digital signal? And this is, again, referring to signal Q of figure 10.

THE WITNESS: . . . So, in that sense, you know, you're asking is it analog or digital. Typically, when you think about a digital system, it's -- like in a 5-volt system, it's going to be -- the value's going to be 5 voltage or ground.

Of -- in this case -- so it has two states. Digital signals typically have two states, one of two states.

(EX2006 at 14:15-15:22.)

A POSITA would accordingly understand that the claimed control signal's plain and ordinary meaning is a logic signal with two distinct states. (EX2005, ¶ 56.)

V. ANTICIPATION REQUIRES EACH AND EVERY LIMITATION

As described below in section VI.A, the Petition fails to demonstrate anticipation because it fails to demonstrate the claimed "control signal" as described in the claims.

"A patent claim is invalid for anticipation under 35 U.S.C. § 102 when one prior art reference describes 'each and every claim limitation and enable[s] one of skill in the art to practice an embodiment of the claimed invention without undue experimentation.'" *In re Chudik*, 851 F.3d 1365, 1372 (Fed. Cir. 2017) (citing *ClearValue, Inc. v. Pearl River Polymers, Inc.*, 668 F.3d 1340, 1344 (Fed. Cir.

2012)). “[U]nless a reference discloses within the four corners of the document not only all of the limitations claimed but also all of the limitations arranged or combined in the same way as recited in the claim, it cannot be said to prove prior invention of the thing claimed and, thus, cannot anticipate under 35 U.S.C. § 102.” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1371 (Fed. Cir. 2008).

“All of the elements and limitations of the claim must be shown in a single prior reference, arranged as in the claim.” *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). “‘It is not sufficient to constitute an anticipation that the device relied upon might, *by modification*, be made to accomplish the function performed by the patent in question, if it were not designed by its maker, nor adapted, nor actually used, for the performance of such functions.’ In other words, a prior art reference anticipates a claim only if it discloses all the elements ‘in the same form and order as in the claim.’” *In re Chudik*, 851 F.3d at 1372 (citing *Topliff v. Topliff*, 145 U.S. 156, 161 (1892) & *Abbott Labs. v. Sandoz, Inc.*, 544 F.3d 1341, 1345 (Fed. Cir. 2008)).

Indeed, the Federal Circuit has found against anticipation when a single reference did not disclose each and every limitation recited in the claim arranged in the same form as claimed. *See BlephEx, LLC v. Myco Indus., Inc.*, 24 F.4th 1391, 1400-02 (Fed. Cir. 2022) (affirming finding of no anticipation where prior art reference’s first figure disclosed a wand and a second figure disclosed a hand-held device, but

the references could not be combined to support anticipation of the claimed swab connected to an electromechanical device because no technical discussion other than attorney argument was presented to argue that a POSITA would “at once envisage” the combination of the references); *Wonderland Nurserygoods Co. v. Baby Trend, Inc.*, 727 F. App’x 1017, 1019-20 (Fed. Cir. 2018) (reversing anticipation finding made in an IPR proceeding because the claims required that there was a single “enclosure member” (e.g., a single piece of fabric over a frame) and the prior art’s disclosed netting over a frame was not continuous because the figure’s depicted edges in the netting did not align); *Nidec Motor Corporation v. Zhongshan Broad Ocean Motor Co. Ltd*, 851 F.3d 1270, 1274-75 (Fed. Cir. 2017) (reversing anticipation finding made in an IPR proceeding because the claims and specification required that an “IQdr demand signal” in a “rotating frame of reference,” but the petitioner only identified signals in a “stationary frame of reference” and the Board is not permitted to find anticipation in view of a missing claim limitation); *In re Chudik*, 851 F.3d 1365, 1372-74 (Fed. Cir. 2017) (reversing the Board’s anticipation finding because the claim required that a protruding surface be “arranged to engage” (e.g., contact) a cavity, but this could only happen in the prior art if an element was removed); *Dell Inc. v. Acceleron, LLC*, 818 F.3d 1293, 1298-99 (Fed. Cir. 2016) (affirming the Board’s finding of no anticipation because, even though the prior art reference described that the CPU could boot from somewhere on the network, it did

not teach booting *from the NAS*, as required by the claim); *Enfish, LLC v. Microsoft Corp.*, 822 F. 3d 1327, 1342-43 (Fed. Cir. 2016) (reversing a summary judgment granting anticipation because the claim required recited aspects of rows and columns for “a logical table,” and thus, the rows and columns needed to be in the same table, and the district court erred in construing the claim too broadly to permit the rows and columns to be from two tables); *Verve, LLC v. Crane Cams, Inc.*, 311 F.3d 1116, 1118, 1121 (Fed. Cir. 2002) (reversing anticipation finding because the prior art reference disclosed a rod that had a uniform diameter along its length (even though the ends had a smaller diameter) but the claims required a rod that had a diameter larger in the middle than towards the ends); *Gen. Elec. Co. v. Nintendo Co.*, 179 F.3d 1350, 1357 (Fed. Cir. 1999) (reversing finding of anticipation where the claims required that a television receive signals from an antenna and then to switch to receiving signals from a video player when the player was turned on because the prior art reference did not expressly disclose the switching and defendant's argument that a POSITA would understand that this switching occurs in televisions was not sufficient to show that the limitation was actually disclosed in the reference).

The PTAB also strictly applies the requirements of anticipation. *See, e.g., U.S. Well Servs., LLC v. Halliburton Energy Servs., Inc.*, IPR2022-01163, Paper 9 at 12-14, 17, 24 (P.T.A.B. Dec. 20, 2022) (declining to institute IPR under anticipation where the claim required comparing *different* signals, but the portion of the

reference cited by the petitioner only disclosed comparing *duplicate* signals); *Lenovo (United States) Inc. & Motorola Mobility LLC, v. Theta Ip, LLC*, IPR2023-00697, Paper 32 at 32-34, 37-38 (P.T.A.B. Oct. 16, 2024) (finding that a reference did not anticipate the claimed determining of signal strength of two channels at the same time because the cited portion of the reference disclosed determining the strength of *either* of two signals, but did not explicitly disclose determining strength of both at the same time); *K-40 Elecs., LLC, v. Escort, Inc.*, IPR2013-00240, Paper 37 at 34 (P.T.A.B. Sept. 29, 2014) (finding no anticipation where the claim required that a receiver receive the same signal continuously, but the portions cited by the petitioner in the reference disclosed identification from multiple sources, and thus, did not disclose a continuously received signal (but later finding the claims anticipated by another reference)); *see also Ex parte Ajay Mahajan and Sumeer Lal*, Appeal 2010-008922 at 5 (Dec. 19, 2012) (reversing anticipation rejection because the claims required that two transducers received the *same* signal, but the alleged reference disclosed two transducers receiving *different* signals).

Finally, the Federal Circuit has held that a single claim term should be construed consistently within the claim (*i.e.*, it cannot mean multiple different elements). *Salazar v. AT&T Mobility LLC*, 64 F.4th 1311, 1317 (Fed. Cir.), cert. denied, 144 S. Ct. 422 (2023); *Rexnord Corp. v Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001); *Epcon Gas Sys., Inc. v. Bauer Compressors, Inc.*, 279 F.3d

1022, 1031 (Fed. Cir. 2002); *Harris Corp. v. Federal Exp. Corp.*, 2013 WL 174185, *4-*7 (Fed. Cir. 2013).

Here, the Petition has failed to demonstrate anticipation because it fails to demonstrate that claims 1, 11, and 18 are literally taught by Tateishi.

VI. THE GROUNDS DO NOT SHOW THAT TATEISHI ANTICIPATES ANY CLAIM

A. Ground 1: Tateishi does not anticipate the claims

Petitioner fails to demonstrate that Tateishi anticipates the claimed “control signal” for several independent reasons.

First, Petitioner’s analysis of the “control signal” in the Petition across claim phrases fails to track the control signal’s antecedent basis and fails to present a threshold case of anticipation. (*See also* EX2005, ¶ 59.)

Second, even if the Board found that Petitioner did not violate the antecedent basis of the “control signal” and that the control signal can comprise two logical signals, Tateishi still fails to anticipate the claims because the two signals have contradictory states. The two signals are not a “control signal” as determined by the proper construction that a control signal is a logic signal with two distinct states. (*See also* EX2005, ¶ 60.)

Third, the Petition fails because the claims require that the “control signal” be used by two different circuits to generate two different outputs ((1) “based on the

switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal” and (2) “wherein based on the input voltage and the control signal, the power stage generates the switching signal.”) Petitioner’s analysis, however, points to a first signal to satisfy phrase (1) when a second signal fails, but at the same time points to the second signal to satisfy phrase (2) when the first one fails. Here, Petitioner fails to track the antecedent basis for “control signal” and fails to identify the “control signal” under its proper construction. (*See also* EX2005, ¶ 61.)

The Petition also fails because it presents Tateishi as an anticipatory reference, but then modifies and combines several embodiments within Tateishi in a way that should be presented under an obviousness analysis. (*See also* EX2005, ¶ 62.)

This is described below.

1. The Petition fails to track the antecedent basis of the “control signal” in claims 1, 11 and 18 and fails at a threshold level

The Petition identifies several different signals as the “control signal” across various limitations. This is improper because a later identified element—which receives its antecedent basis from an earlier described element—must be the same throughout a claim. *E.g., Salazar v. AT&T Mobility LLC*, 64 F.4th 1311, 1317 (Fed. Cir.), cert. denied, 144 S. Ct. 422, 217 L. Ed. 2d 234 (2023); *Haemonetics Corp. v. Baxter Healthcare Corp.*, 607 F.3d 776, 781–82 (Fed. Cir. 2010) (“Claim

16 states: ‘A centrifugal unit comprising a centrifugal component and a plurality of tubes....’ . . . [I]t unambiguously defines ‘centrifugal unit’ as ‘comprising’ two structural components: a centrifugal component and a plurality of tubes. The claim then further recites, not the centrifugal component and not *a* centrifugal unit, but ‘*the* centrifugal unit’ as ‘having a radius between 25 and 50 mm and a height between 75 and 125% of the radius.’ Reading ‘the centrifugal unit’ in the context of the dimensional limitations to refer exclusively to the vessel, as the district court did, ignores the antecedent basis for ‘the centrifugal unit.’”); *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1356 (Fed. Cir. 1999) (“It is clear from the language of the claim itself that the term ‘a discharge rate’ in clause [b] is referring to the same rate as the term ‘the discharge rate’ in clause [d].”).

The ’377 Patent’s claims all recite the same control signal (as opposed to multiple different control signals). (EX2005, ¶ 64.) The claims introduce “a control signal” (claim 1 at 9:45, claim 11 at 11:49, claim 18 at 13:23) and “the control signal” is thereafter recited as being generated by specific hardware (*e.g.*, a logic control circuit or flip-flop) (claim 1 at 10:8-9, claim 11 at 12:12-13, and claim 18 at 14:18-19) and connected to other hardware (claim 1 at 10:11, claim 18 at 14:2, 14:22) to generate other signals (claim 1 at 10:11-13, claim 18 at 14:2-3, 14:22-24). The “control signal” must be the same signal throughout each respective claim. (EX2005, ¶ 64.)

Dr. Holberg (Petitioner's expert) agrees that "a control signal" provides antecedent basis for "the control signal" and that all recitations of the "control signal" must identify the same signal throughout each specific claim. (EX2005, ¶ 65.) He testified that:

Q In your opinion, do all instances of the language "control signal" in claim 1 refer to the same signal?

THE WITNESS: . . . So they would all be the same.

(EX2006 at 23:6-24:6.)

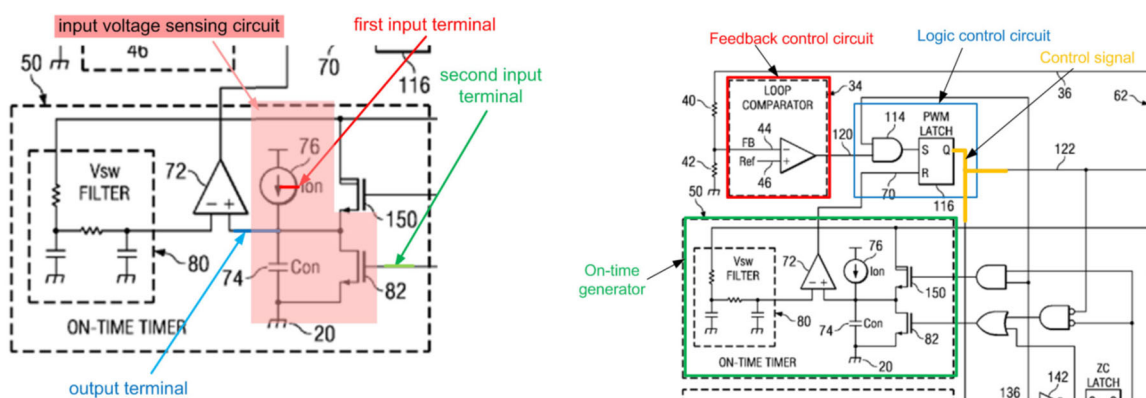
Q In your opinion, do all instances of the recited control signal in claim 18 refer to the same signal?

A Yeah. Every instance where it says "the control signal," it's -- the antecedent for that is "a control signal" found in line 21, 2, 3, of column 13.

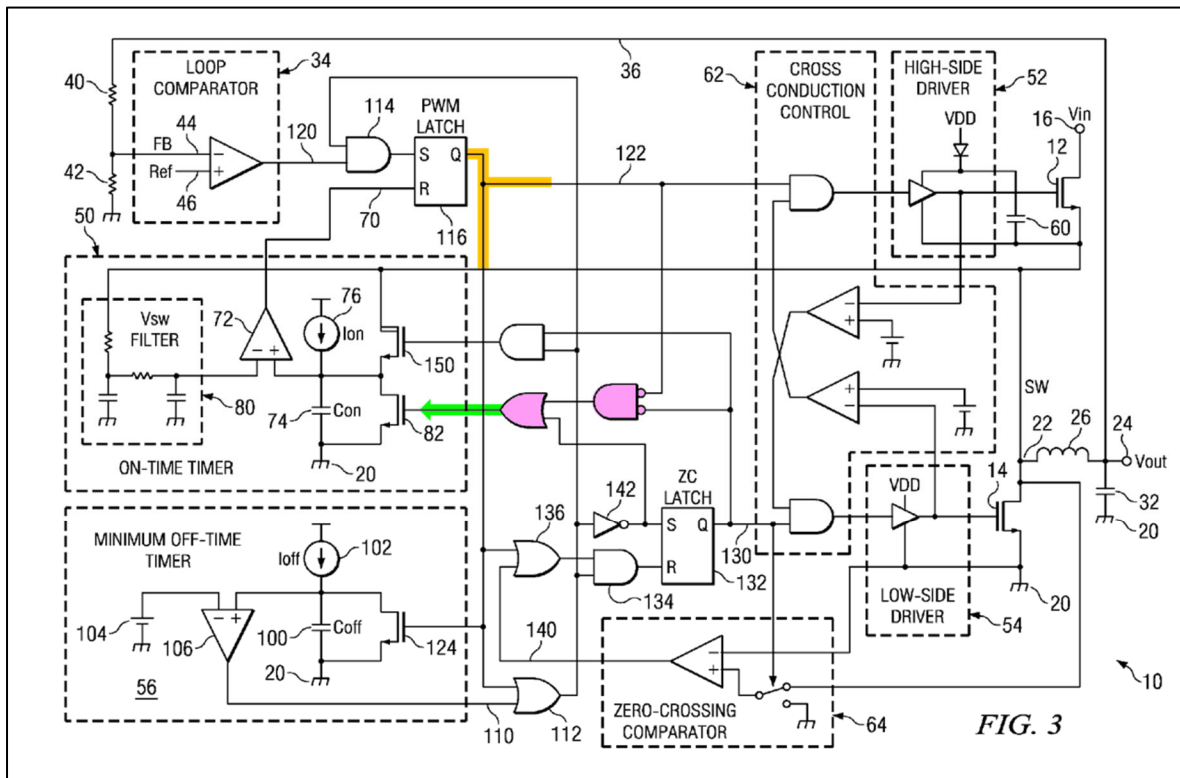
(EX2006 at 26:7-13.)

The Petition's claim analysis, however, identifies separate signals as the "control signal" when it presents Tateishi as anticipating the claims. (EX2005, ¶¶ 66– 68.) Specifically, the language of limitation **1[B2]** introduces "a control signal" giving it antecedent basis, and limitation **1[D]** later recites that "the logic control circuit generates the control signal." (EX1001 at 9:45, 10:8-9; EX2005, ¶¶ 66– 68.) For limitation **1[B2]**, Petitioner identifies the signal feeding into the claimed "second input terminal" as the claimed "control signal" to meet "the second input terminal is configured to receive a control signal." (Paper No. 1 ("Petition" or "Pet.") at 37.) This is shown in the excerpt provided below-left from

the Petition at 37 with Petitioner's green annotations showing where the "control signal" exists. (EX2005, ¶ 67.) For limitation 1[D]—in another excerpt of Figure 3—Petitioner identifies a wholly separate signal for the "control signal" (orange), the signal generated by the PWM latch 116 (blue). (Pet. at 45.) This is shown in the excerpt provided below-right. (EX2005, ¶ 68.)



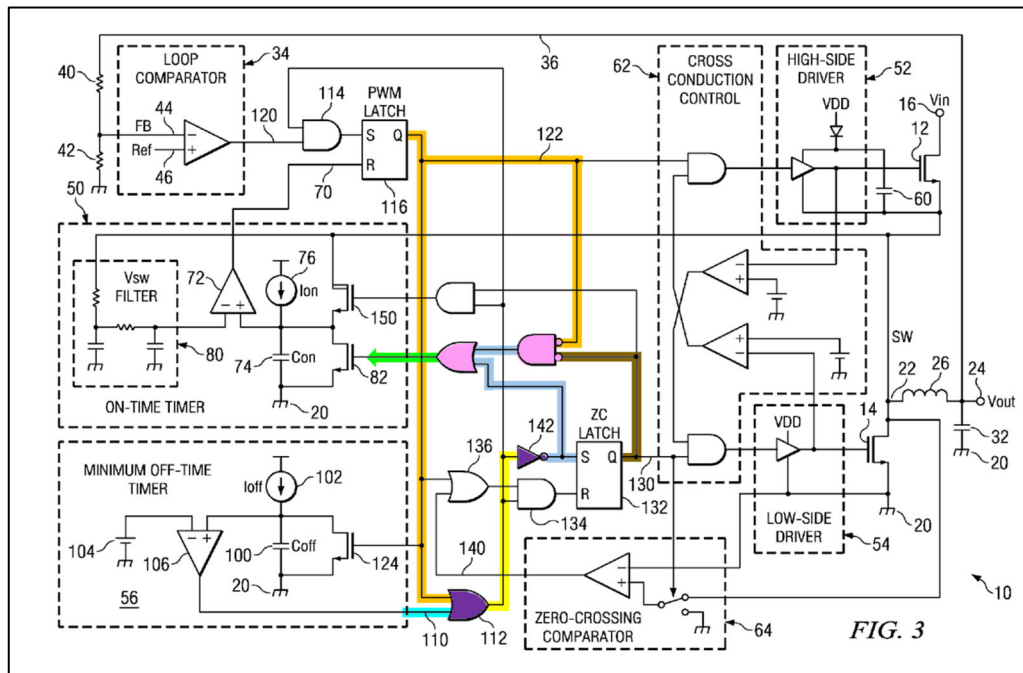
The signals identified by Petitioner for 1[B2] and 1[D] are two entirely different signals. (EX2005, ¶¶ 69–76.) The mismatch is apparent when Figure 3 is illustrated in its entirety (and not as mere excerpts separated by several pages). (EX2005, ¶ 69.) Shown below are Petitioner's two separate signals identified for 1[B2] (green) and 1[D] (orange) annotated onto Figure 3 by Patent Owner. (EX2005, ¶ 69.) As can be seen from the below, these two signals are separated by two logic gates, an OR gate and an inverting AND gate (both in pink). (EX2005, ¶¶ 70–72.) These two signals are not the same signal; a POSITA would understand that the separating logic makes them different logical signals. (EX2005, ¶¶ 70–72.)



Beyond being separated by the OR and inverting AND gates (pink), those gates have—as their inputs—other signals from other logic that affects their output. This other logic further demonstrates that Petitioner's two identified signals are not the same “control signal.” (EX2005, ¶¶ 73–76.)

The additional logic is shown via further annotation to Figure 3 provided below. (EX2005, ¶¶ 73–75.) Petitioner's identified “control signal” of 1[D] (orange) goes through another OR gate 112 (purple) along with yet another signal 110 (aqua). (*Id.*) The signal result (yellow) of that OR operation is later inverted via inverter 142 (also purple), whereupon that signal result (blue) is provided to the pink OR-gate. (*Id.*) The pink OR-gate's other input is from another signal (also

blue) that is the result of an inverting AND (pink) operation of the originally identified “control signal.” (*Id.*) The other input (brown) to the inverting AND is from the ZC latch 132. (*Id.*) There are other logical signals that affect the ZC latch 132 (its reset input, via the zero-crossing comparator) that are not annotated. There are a significant number of logical operations that occur between the two signals petitioner identified as the “control signal” in 1[B2] and 1[D]. (*Id.*, ¶ 76.) These two signals are not the same “control signal.” (*Id.*)



Finally, even if one were to assume that these two signals could theoretically end up as the same control signal despite all intervening logic (which is not the case as described in Section IV (Claim Construction)), Petitioner still fails to provide any explanation regarding why these two signals can both—at the same time—be the

same “control signal.” Petitioner bears the burden to do so and, as a consequence, fails to present a threshold theory of anticipation as to the “control signal.” 35 U.S.C. § 316(e) (Petitioner bears the burden of proof); 37 C.F.R. § 42.22(a)(2) (A Petitioner is required to include “[a] full statement of the reasons for relief requested, including a detailed explanation of the significance of the evidence including material facts”); 37 C.F.R. § 42.104(b)(3)–(4) (A Petition must explain “[h]ow the challenged claim is to be construed” and “must specify where each element of the claim is found in the prior art patents or printed publications.”); *see also Lab’y Corp. of Am. Holdings v. Ravgen, Inc.*, No. 2023-1517, 2025 WL 324749, at *4 (Fed. Cir. Jan. 29, 2025) (affirming patentability in IPR where petitioner failed to set forth persuasive evidence that a reference disclosed a required claim limitation that a “dextrose ... impede cell lysis”).

As a consequence, Petitioner fails to demonstrate that Tateishi anticipates claim 1. The same issue described above exists with respect to claims 11 and 18 where Petitioner mostly incorporates claim 1 analysis by reference. (EX2005, ¶ 77.) Specifically, limitation 11[B1] recites “second input terminal is configured to receive a control signal” while 11[D] recites that “the logic circuit generates the control signal.” (Pet. at 61 and 63 (incorporating claim 1 analysis).) Limitation 18[B] requires that the “minimum off time generator [is] configured to receive the control signal” while 18[E] requires that “the flip-flop generates the control signal.” (Pet.

at 66 and 71 (identifying the same elements).) Claims 11 and 18 suffer from the same problem and are also not anticipated by Tateishi. (EX2005, ¶ 77.)

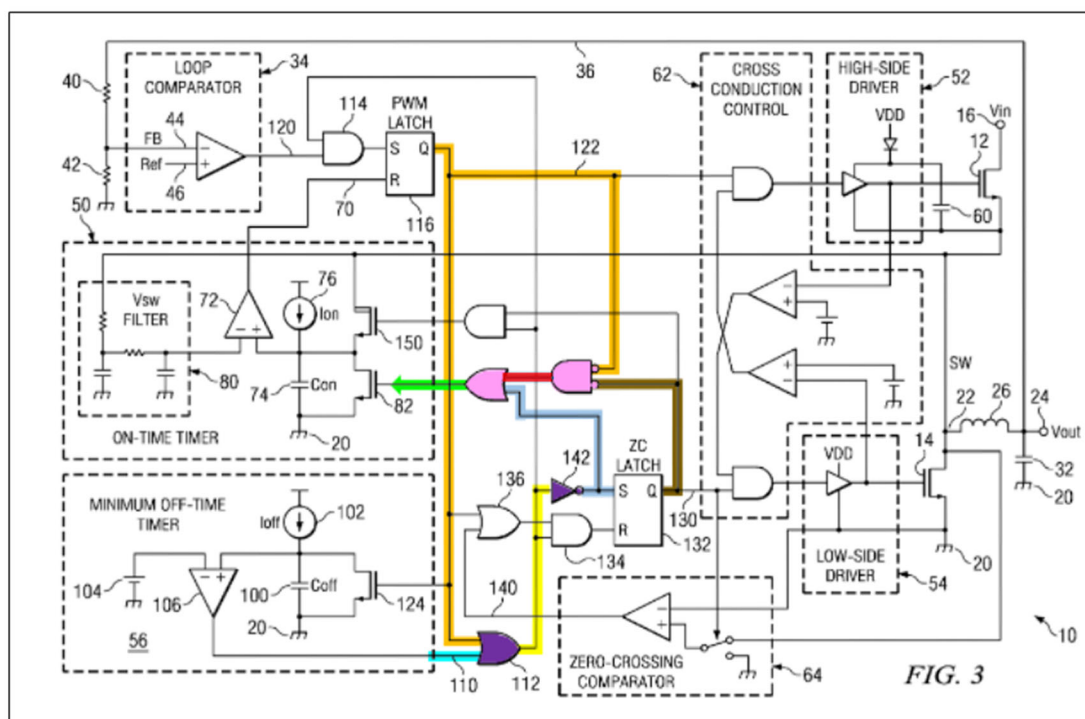
2. The Petition fails to demonstrate that Tateishi anticipates the claims under a proper construction of control signal

Even assuming that Petitioner's identification of the "control signal" is sufficient at a threshold level and that two distinctly different logic signals can be the same "control signal" at the same time, Petitioner's analysis still fails to demonstrate anticipation. (EX2005, ¶ 78.) Petitioner's analysis, in order to hold, would require that the signals identified be logically consistent, *i.e.*, its 1[D] signal would need to be logically consistent in some manner with the signal identified in 1[B2]. Petitioner would need—but failed—to demonstrate that its identified signal is a logic signal with two distinct states.

The signals identified by Petitioner have logic states that are inconsistent; the identified control signal is, *e.g.*, '0' while another part of it can be either '1' or '0' depending on other logic of the circuit. (EX2005, ¶ 78.) There is a breakdown in any sense of cohesive control the alleged control signal would have and Petitioner failed to identify a logic signal with two distinct states.

Petitioner's failure is demonstrated in the logic of Tateishi's Figure 3. (EX2005, ¶¶ 79–83.) As can be seen from the below circuit diagram (and the logic

table that follows), when the orange signal⁴ is ‘0,’ the green signal can either be ‘1’ or ‘0’ depending on the value of an entirely different signal, the minimum off-timer’s output 110 (aqua) and the ZC latch 132’s Q output 130 (brown). (EX2005, ¶¶ 79–84.) The logical state of the orange signal does not define the state of the green signal, and there is mismatch in states between the two signals. (EX2005, ¶¶ 79–87.) Because there is a logical mismatch in states, the orange and green signals cannot, at the same time, be the claimed control signal. (EX2005, ¶¶ 79–86); *see also* EX2005, ¶ 85 (describing the logic table in the form of a logic equation).



⁴ For ease of identification, the signals are often referred-to by their annotated color in this response.

Circuit Diagram

Orange	Brown	Red	Blue	Green	Aqua	Yellow
0	1* ⁵	0*	1	1	0	0
0	0	1	0*	1	1	1
0	1	0	0	0	1	1
1	0	0	0	0	0*	1
1	1	0	0	0	0*	1
1	0	0	0	0	1*	1

Logic Table

Moreover, the above-circumstance where Aqua and Brown implicate a change in Green is not mere theory, *i.e.*, these signals cannot simply be ignored. (EX2005, ¶ 88.) Dr. Holberg confirmed that the green signal's state is controlled via the off-timer's output 110 (aqua)'s state. (EX2006 at 37:3-6 ("Q And when logic – when 110 goes logic state high, the output of OR gate 112 will likewise go high, correct? A That is correct" (thus, by inverter 142, the green signal would be 0)); EX2006 at 37:10-18 ("For the next question, we'll assume logic 110 – the signal 110 is logic 0 and 122 is logic 0, as you stated in a previous answer today. A Correct. Q And when that occurs, you stated inverter 142 will be – will invert that 0 to 1, which will set the Q output to 1, correct? ... THE WITNESS: That is

⁵ The * represents a "don't care" meaning that the value does not affect the eventual green output. (EX2005, ¶ 83 n.1.)

correct.”.) He testified that, when the orange signal is initially triggered to ‘0,’ that the off-timer’s output 110 (aqua) will be ‘1’ some time after the Coff 100 charges. (EX2006 at 32:13-33:8, 34:10-37:18.) Coff 100 controls the minimum off-time 110. (EX2006 at 47:4-8, 48:6-9.) He, moreover, testified that the ZC latch 132’s output signal 130 (brown) will trigger to ‘0’ or ‘1’ based on a zero crossing, and that detection is dependent upon load. (EX2006 at 49:6-49:19.) In other words, the value of Coff and the load provide logical signals that affect the control of switch 82; it is not controlled via the orange signal. (EX2005, ¶ 88.)

The signals identified by Petitioner as the “control signal” are a collection of separate and distinct control signals, and they all cannot constitute the “control signal” under the proper construction of “control signal” which is a logic signal with two distinct states.

Petitioner’s mixing and matching of logical signals fails to show that Tateishi anticipates the independent claims. (EX2005, ¶ 90.)

Claim 1 is thusly not anticipated by Tateishi. Claims 11 and 18 are not anticipated for the same reasons. (EX2005, ¶ 89.)

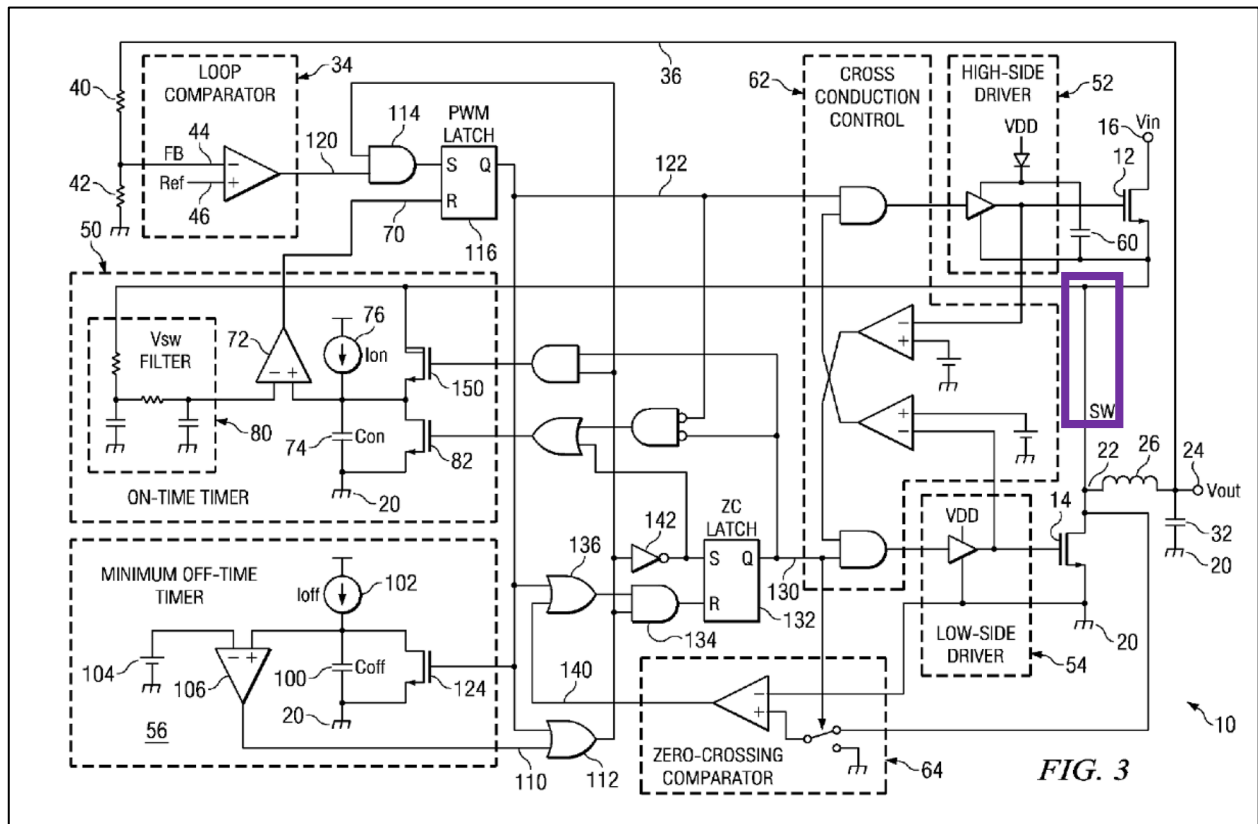
3. The other claim limitations emphasize Petitioner’s “control signal” deficiencies

Petitioner’s analysis of claim limitations that describe generating logic signals based on the “control signal” break down when both of the two different signals

identified by Petitioner for 1[B2] and 1[D] are considered at the same time. (EX2005, ¶¶ 91–102.)

Specifically, the claims further require that: **(1)** “based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal” (1[B2]; *see also* 18[A]) and **(2)** “wherein based on the input voltage and the control signal, the power stage generates the switching signal.” (1[E]; *see also* 18[F]; EX2005, ¶¶ 92–93.) Phrase **(1)** only makes sense within the Petition when the green-annotated signal is considered in isolation ignoring the orange signal, but phrase **(2)** only makes sense within the Petition when the orange signal is considered in isolation while ignoring the green signal. (EX2005, ¶ 94.) These are described in turn below with reference to the entirety of Figure 3.

For **(1)**, Petitioner identified the voltage signal on the capacitor 74 (red oval) as the “input voltage sensing signal” and the green signal as the control signal for the claim phrase “based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal.” (EX2005, ¶¶ 94–95.) Petitioner’s identification is because green signal controls switch 82, *i.e.*, a ‘1’ will discharge the voltage on the capacitor while a ‘0’ will charge the capacitor. (Pet. at 37; EX2005, ¶ 95.)



Petitioner’s analysis for phrase (1), however, breaks down when other signals identified as the “control signal,” *i.e.*, the orange signal for 1[D], are considered. (EX2005, ¶¶ 96.) Namely, as described in Section VI(A)(2), the orange signal does not define the logical state of the green signal which controls whether the capacitor 74 is discharged or not (*i.e.*, the orange signal does not control the green signal’s logical value); the logical value of the green signal depends on the value of both the aqua and brown signals, as confirmed in the above logic table. (*See also* EX2005, ¶¶ 96; logic table below.)

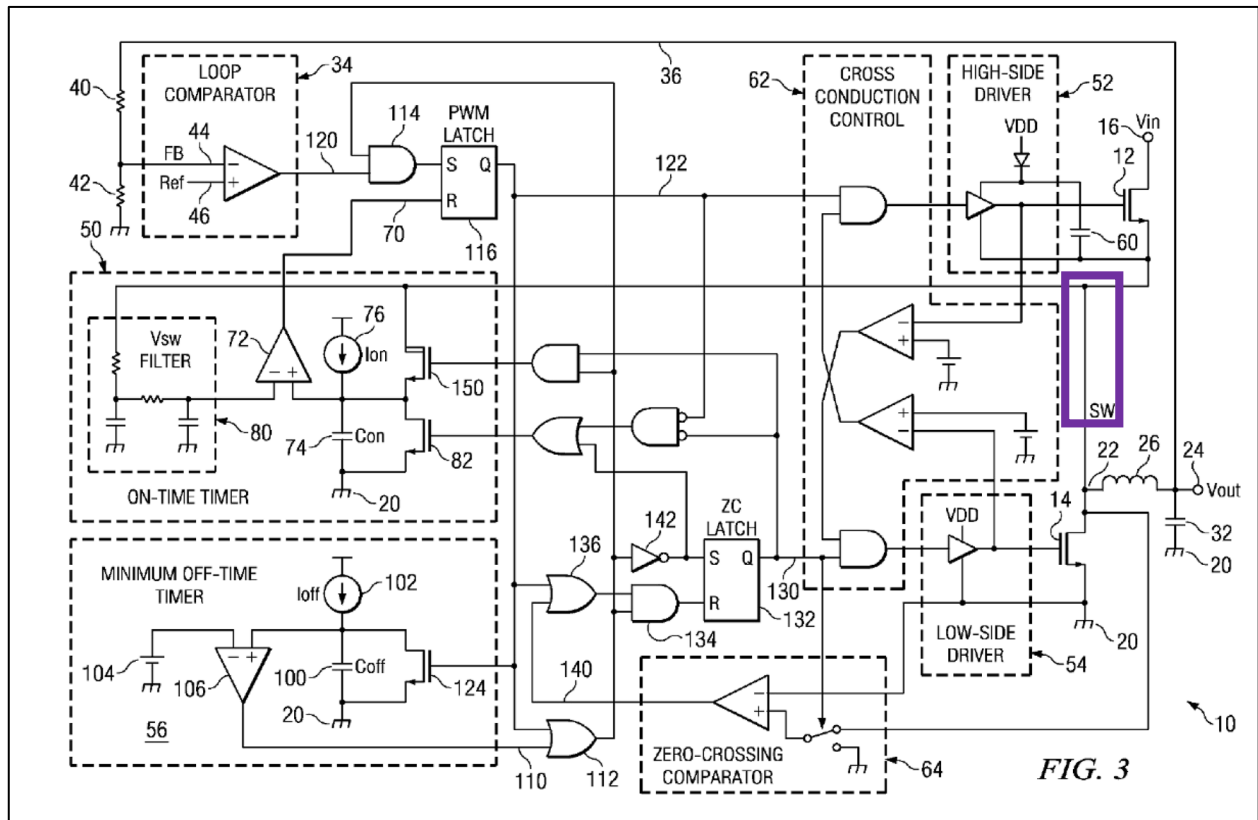
Orange	Aqua	Brown	Green
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0	0	*	1
0	1	0	1
0	1	1	0
1	*	*	0

Petitioner's failure is more evident when the control signal's logic states are considered in view of the claim language. (EX2005, ¶ 97.) The claim language recites: "based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal." However, the green signal can be '1' or '0' when the orange signal is '0.' It is entirely indeterminate to arrive at "an input voltage sensing signal" "based on the switching signal and the control signal" under these circumstances because the combined signals identified as the control signal are inconsistent. (*See id.*, ¶¶ 97–98.)

Petitioner's analysis for phrase (2) ("a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal") suffers the same fate (but does so in an inverse manner). (*See* EX2005, ¶¶ 99–100.) Petitioner's analysis falls apart when the orange signal is considered along with the green signal. As can be seen from the below, the orange signal itself is an input to the

identified “power stage” (yellow) which generates a “switching signal” (purple box). (EX2005, ¶¶ 100–01.) The green signal is not an input to the power stage, and the power stage does not generate the “switching signal” based on the green signal along with the “input voltage.” (*Id.*)



Petitioner's analysis for phase (2) suffers from the fact that its “control signal” provides inconsistent states. The limitation requires “based on the input voltage and the control signal, the power stage generates the switching signal” but the identified “control signal” has internally inconsistent logic states, *i.e.*, orange is ‘0’ when green can be ‘1’ or ‘0.’ (EX2005, ¶¶ 100–01.) Like its analysis for phrase (1), its analysis for phrase (2) fails.

As a consequence, Petitioner's identified control signal cannot at the same time satisfy both (1) "based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal" and (2) "wherein based on the input voltage and the control signal, the power stage generates the switching signal." (See EX2005, ¶ 102.) Claims 11 and 18 have similar language and the Petition suffers from the same deficiencies. (See EX2005, ¶¶ 98, 101.)

Claims 1, 11, and 18 are thusly not anticipated.

4. Petitioner combines several embodiments inconsistent with an anticipatory analysis

The Petition fails because it combines and modifies the separate embodiments of Figures 2, 3, and 4 to arrive at claim limitations directed towards the claimed "switching signal" and "control signal."

Claim limitations 1[B2], 11[B1], and 18[A] all require that an on-time generator (or its input voltage sensing circuit) receive a switching signal and a control signal (which is generated via logic control circuit / a flip-flop) (EX1001 at 9:40-50, 10:10-13, 11:44-53, 12:8-13, 13:21-25, 14:13-20; *see also* EX2005, ¶ 104.) For example, the relevant terms of 1[B2] are highlighted below:

an on-time generator comprising:
an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal,
wherein the first input terminal is configured to receive

a **switching signal** provided by the step-down regulator, the second input terminal is configured to receive a **control signal** provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;

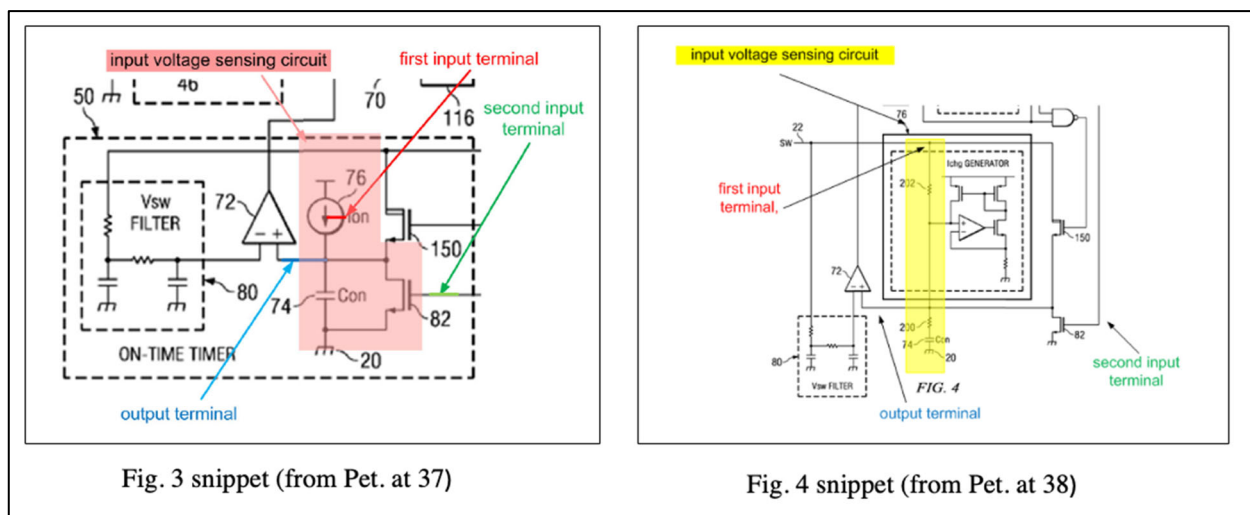
(EX1001 at 9:37-50; *see also* EX1001 at 10:10-13 (stating that the control signal is generated via a logic control circuit).) Similarly, 18[A] requires that the on-time generator receives a switching signal and control signal:

an on-time generator configured to receive a **switching signal** provided by the step-down regulator, and to receive **a control signal**, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;

(EX1001 at 13:21-25; *see also* EX1001 at 14:14-20 (stating that the control signal is generated via a flip-flop).)

Petitioner relies on a combination of Tateishi's Figures 3 and 4 to inject a switching signal into Figure 3's circuit while ignoring that the Figure 4 embodiment is distinctly different and provides separate control mechanisms and signals. (*See* Pet. at 36–39; EX2005, ¶ 105.) These two embodiments are inconsistent and it cannot be assumed that they are the same for an anticipatory analysis (as Petitioner has done).

Petitioner relies on Figure 3 (below-left) to teach several elements, but this circuit lacks a switching signal provided to the alleged first input terminal of the alleged input voltage sensing circuit, as required by the claims. (See Pet. at 37; EX2005, ¶¶ 105-06.) In attempt to remedy this, Petitioner takes a generator portion of the Figure 4 embodiment (below-right), that has a switching signal, and applies it to Figure 3's current source. (Pet. at 37–38; EX2005, ¶ 105.) Petitioner argues that Figure 3's current source 76 could be replaced with the generator portion of Figure 4's circuitry, which receives the switching signal SW, to suggest that Figure 3's current source 76 could receive a switching signal SW. (See Pet., 37–38 (and shown below on right side); EX2005, ¶ 106.)

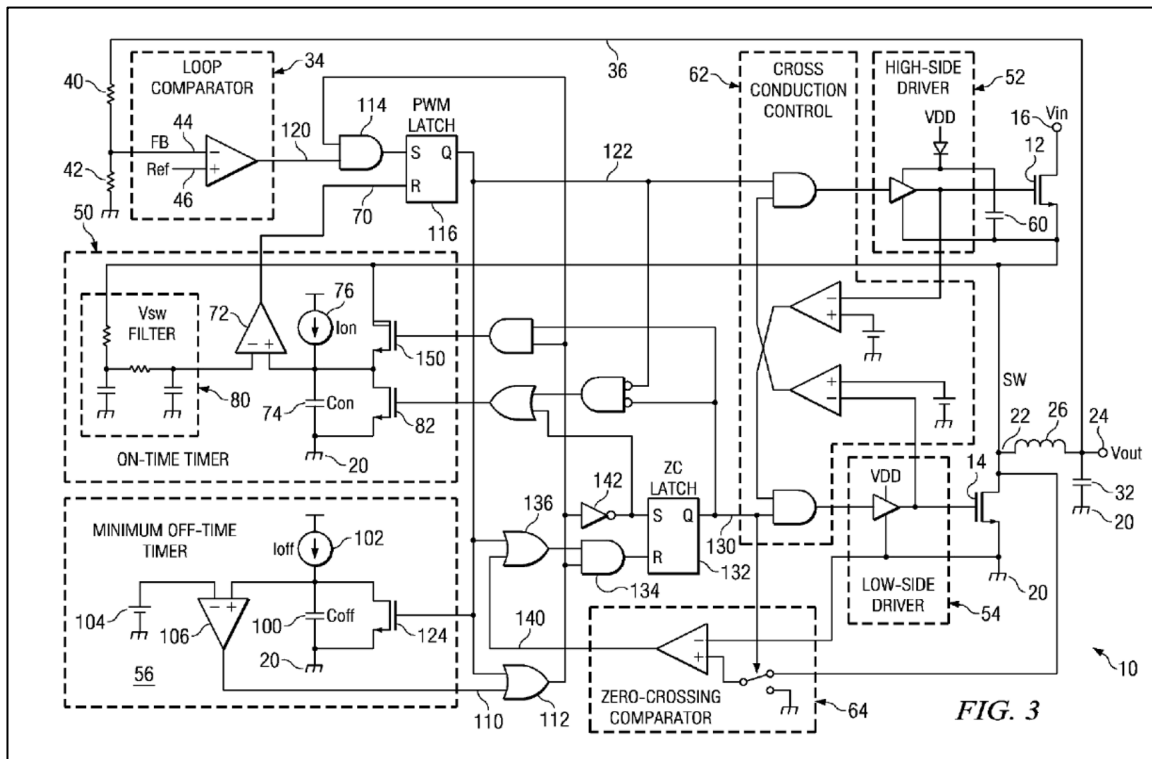


Petitioner's analysis fails because it modifies Figure 3 with a teaching that is not literally present in Tateishi. (See *Merck & Co., Inc. v. Teva Pharmaceuticals USA, Inc.*, 347 F.3d 1367, 1372 (Fed. Cir. 2003) ("An 'anticipating' reference must

describe all of the elements and limitations of the claim in a single reference, and enable one of skill in the field of the invention to make and use the claimed invention.”.) Petitioner’s modification injects what would be an obviousness-type analysis based on impermissible hindsight that is not present in the four-corners of the prior art reference and fails on its face to support anticipation. (*See Apple Inc. v. Corephotonics, Ltd.*, 861 F. App’x 443, 450 (Fed. Cir. 2021) (“As the Board correctly noted, ‘[p]rior art that must be modified to meet the disputed claim limitation does not anticipate the claim.’ Such modifications are permissible only in an obviousness analysis.”) (quoting *Enplas Display Device Corp. v. Seoul Semiconductor Co.*, 909 F.3d 398, 405 (Fed. Cir. 2008)); *In re Gates*, 787 F. App’x 741, 743–44 (Fed. Cir. 2019) (reversing anticipation rejection where prior art reference disclosed two distinct embodiments but nothing in the reference disclosed that the relevant features of the two devices could be combined, and thus, and anticipation theory was insufficient); *In re Chudik*, 851 F.3d at 1372–74 (reversing Board’s finding of anticipation because the prior art reference required a modification of what was disclosed, stating “[i]n other words, a prior art reference anticipates a claim only if it discloses all the elements ‘in the same form and order as in the claim.’”) (citations omitted)).) One cannot, as Petitioner has, piece together various embodiments to arrive at anticipation.

Furthermore, Figures 3 and 4 are entirely different embodiments. (EX2005, ¶ 107.) Tateishi describes Figure 4 as a different converter than that of Figure 3, stating that Figure 4 “depicts an example of various portions of *another* DC to DC buck converter ...” (emphasis added)). (EX1007, ¶ 0013). Modifying embodiments of a prior art reference is not appropriate for anticipation. *See Microsoft Corp. v. Biscotti, Inc.*, 878 F.3d 1052, 1069 (Fed. Cir. 2017) (“anticipation is not proven by ‘multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention.’”).

Second, Tateishi's Figures 3 and 4 are different embodiments—which Petitioner picks and chooses elements from—as evident by the control signals for their switches. (See EX2005, ¶¶ 108–10.) Figure 3 (below) is a whole circuit, with logic (aqua) that controls the on-time timer's switches (yellow). (Tateishi at Fig. 3 (annotated); EX2005, ¶ 108.)



Tateishi's Figure 4, in contrast, provides a separate set of logic (aqua) that controls the switches (yellow). (Tateishi at Fig. 4 (annotated); EX2005, ¶ 109.) Each embodiment has a different control mechanism.



Finally, Petitioner also modifies Figure 3 with Figure 2 to show that the current source 76 in Figure 3 receives a switching signal if replaced with Figure 2's current source. (Pet. at 38; EX2005, ¶ 111.) Tateishi never states that Figure 2's current source can be used in Figure 3's embodiment, stating only that "Fig. 2 depicts a reference current source that may be used in *the DC to DC buck converter of FIG.*

1.” (Tateishi, ¶ 11 (emphasis added); EX2005, ¶ 111.) Petitioner improperly relies on an amalgamation of several different embodiments for its anticipatory analysis.

Ground 1 fails because Petitioner relies on teachings not present within the four corners of Tateishi; Petitioner modifies embodiments in an obviousness analysis. (*See also* EX2005, ¶ 112.) Petitioner cannot modify several embodiments as it has done here to arrive at anticipation. *See Microsoft Corp.* 878 F.3d 1052 at 1069 (“anticipation is not proven by ‘multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention.’”). Ground 1 fails.

B. Ground 2: Petitioner has failed to show how dependent claims 5, 7-8, and 15 are rendered obvious by Tateishi.

Ground 2 addresses dependent claims. It does not cure the above-described deficiencies and fails for the same reasons. (*See also* EX2005, ¶ 114.)

VII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board find that Petitioner has not shown that Tateishi anticipates or renders obvious the claims of the '377 Patent.

Dated: April 21, 2025

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Under 37 C.F.R. §42.24(d), the undersigned certifies that the word count for this Patent Owner's Response to the Petition for inter partes review totals 8,141 excluding the parts exempted by 37 C.F.R. §42.24(a). The word count was made using the built-in word count function in the Microsoft® Word software used to prepare this document.

Dated: April 21, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on April 21, 2025, a copy of
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