

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

PETITIONER

V.

MONOLITHIC POWER SYSTEMS, INC.,

Patent Owner.

Case No. IPR2024-01158

Patent No. 9,041,377

DECLARATION OF JOSEPH C. MCALEXANDER III, P.E.

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LIST OF EXHIBITS

Exhibit	Reference
2001	Declaration of Joseph C. McAlexander ^{III} , P.E.
2002	Curriculum Vitae of Joseph C. McAlexander ^{III} , P.E.
2003	Wayback Machine May 27, 2010 Webpage Archive of Integrated Publishing's Electrical Engineering Training Series' Page Entitled "Variations of fundamental gates"
2004	Webpage of LibreTexts.org's University Physics II Text, Section 10.2, Entitled "Resistors in Series and Parallel"
NEW EXHIBITS	
2005	Second Declaration of Joseph C. McAlexander ^{III} , P.E.
2006	Excerpts of the April 9, 2025 - Deposition Transcript of Douglas R. Holberg, Ph.D.

I, Joseph C. McAlexander^{III} declare as follows:

1. I have been retained as an expert consultant by Perkins Coie LLP on behalf of Monolithic Power Systems, Inc. (“Patent Owner”) in this proceeding before the United States Patent and Trademark Office (“PTO”) initiated by Reed Semiconductor Corp. (“Petitioner”) regarding U.S. Patent No. 9,041,377 (“the ’377 Patent”) (Ex 1001). I have been asked to provide my technical review, analysis, insights, and opinions regarding the references that form the basis for the alleged grounds of unpatentability set forth in the Petition. For this service, I am being compensated for my time, and I am reimbursed for actual expenses. I have no interest in the outcome of this proceeding, and my compensation is not dependent on the content of my opinions or the outcome of this proceeding.

I. INTRODUCTION AND QUALIFICATIONS

2. I am an independent consultant. All opinions stated in this Declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience relating to the technology referenced in this Declaration.

3. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current curriculum vitae, which includes a more detailed summary of my education and professional and academic experience is provided as Appendix A to this Declaration.

The following provides an overview of some of my experience that is relevant to the matters set forth in this Declaration.

A. Qualifications

4. I am a Registered Professional Engineer (#79454) and the President of M^cAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 52 years and am a named inventor on 31 U.S. patents and a number of foreign patents.

5. I have extensive expertise in the subject matter area relevant to this matter, specifically the design, fabrication, and testing of integrated circuits, including that of power and timing control circuits embedded in integrated circuits. For example, I have over fourteen years of experience at Texas Instruments. There, I designed, developed and implemented circuits, processes, and procedures to assure product and process reliability. More specifically, I designed and managed the processing and productization of many types of integrated circuit devices, including, among others, dynamic and static storage devices, charge coupled devices (CCD) for imaging applications, electrically programmable and erasable non-volatile devices (EPROM / EEPROM) for instruction storage and access, logic devices, and controllers. I also was responsible for the design and use of many performance

boards used in testing and performance characterization of integrated circuits as well as the creation and implementation of the testing programs used to evaluate the performance characteristics of the integrated circuits. These boards required power control and signal stability for accurate assessment of device performance under various timing and power requirement conditions, adjusted according to specific, current circuit operation and load demands.

6. Additionally, while at EPI for 5 years, I managed activities which included board designs that required power and signal control. Specifically, my experience in the industry and with engineers practicing in the industry informs my opinion as to the level of skill of individuals and the general state of the art.

7. Specifically, I have:

designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both nonvolatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;

managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;

provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other), and products related to wireless tracking and geofencing; and

designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

8. I am qualified to reach the opinions and conclusions stated in this Declaration.

9. In forming my opinions, I rely on my knowledge and experience in the fields relevant to this Declaration. I further rely on documents and information referenced in this Declaration.

10. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae attached to this Declaration.

B. Materials Reviewed

11. The opinions contained in this Declaration are based on the documents I have reviewed, my professional judgment, and my education, experience, and knowledge relating to power control and related fields. In forming my opinions, I

have reviewed all materials referenced by the Petition and Dr. Holberg's report and all materials listed in the List of Exhibits provided above (as well as any other materials and information I reference in this Declaration).

12. My opinions contained in this Declaration are based on the documents I have reviewed and considered, as well as my knowledge and professional judgment. My opinions have been guided by my appreciation of how a person of ordinary skill in the art ("POSITA") would have understood the state of the art, the prior art, and the claims and the specification of the '377 Patent at the time of the alleged invention.

13. The time of the alleged invention of the '377 Patent encompasses the time frames near and including June 30, 2011. I understand the application for the '377 Patent claims priority to a Chinese patent application (CN application No. 201110181295), which was filed on June 30, 2011. (EX1001 at 1:7-9). My opinions reflect how a POSITA (which I describe below) would have understood the '377 Patent, the prior art to the '377 Patent, and the state of the art at the time of the alleged invention.

C. Summary of My Opinions

14. The challenged claims of the '377 Patent are not anticipated or rendered obvious under 35 U.S.C. §§ 102 and 103 based on Petitioner's grounds shown in the table below:

Ground	Claims	Description
1	1-4, 9-14, and 17-18	Anticipated under §102 by Tateishi and/or the Tateishi Patent.
2	5, 7-8, and 15	Rendered obvious under §103 by Tateishi and/or the Tateishi Patent.

15. Based on my experience and expertise, it is my opinion that the prior art fails to disclose and/or suggest all the limitations recited in challenged claims of the '377 Patent, as I discuss in detail below.

II. UNDERSTANDING OF LEGAL PRINCIPLES AND PERSPECTIVES

16. I am not a lawyer, and I will not provide legal opinions. Although I am not a lawyer, I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

17. I understand that a patent claim is invalid if it is anticipated or rendered obvious over the prior art and that a claim can be unpatentable even if all requirements of the claim cannot be found in a single prior art reference. I further understand that invalidating a claim requires that the claim be anticipated or rendered obvious from the perspective of a POSITA at the time the invention was made.

18. In forming my analysis, opinions, and conclusions expressed in this Declaration, I have applied the legal principles set forth below, which were provided to me by counsel for Patent Owner.

A. Types of Claims

19. I understand that there are two types of U.S. patent claims: 1) independent claims, and 2) dependent claims. I understand that independent claims only include the aspects stated in the independent claim. I further understand that dependent claims include the aspects stated in the independent claim, and any other aspects stated in any claim from which that dependent claim depends, as well as any limitations required by the dependent claim.

B. Anticipation

20. I understand that a claim in an issued patent can be invalid if it is anticipated. In this case, “anticipation” means there is a single prior art reference that discloses every element of the claim, arranged in the way required by the claim, either expressly or inherently.

21. I understand that anticipation of a claim requires that every element of a claim is disclosed expressly or inherently in the single prior art reference. I understand that “inherent” disclosure means that the claim element, although not expressly described by the prior art reference, must necessarily be present based on the disclosure. I understand that a mere probability that the element is present is not sufficient to qualify as “inherent disclosure.”

C. Obviousness

22. I understand that a claim in an issued patent can be rendered invalid if it is obvious. Unlike anticipation, obviousness does not require that every element of the claim be in a single prior art reference. Instead, it is possible for claim elements to be described in different prior art references or that a claim element in a prior art reference might be modified, so long as there is motivation or sufficient reasoning to combine the references or make the modification and a reasonable expectation of success of doing so.

23. I understand that a claim is invalid for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious from the perspective of a person of ordinary skill in the relevant art at the time the invention was made. I also understand that, when evaluating obviousness, one must consider obviousness of the claim “as a whole.” This must be from the perspective of the person of ordinary skill in the relevant art at the time the invention was made.

24. I further understand that exemplary rationales that may support a conclusion of obviousness include:

- a) combining prior art elements according to known methods to yield predictable results;
- b) simple substitution of one known element for another to obtain predictable results;

- c) use of known technique(s) to improve similar devices (methods or products) in the same way;
- d) applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- e) “obvious to try” - choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- f) known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a POSITA; and
- g) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

25. In analyzing obviousness, I understand that it is important to understand the scope of the claims, the level of skill in the relevant art, the scope and content of the prior art, the differences between the prior art and the claims, and any “secondary considerations” (described below). I also understand that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Although I understand that it is not required, there may also be a specific “teaching, suggestion or motivation” to combine any first prior art reference with a second prior art reference. Such a “teaching, suggestion, or motivation” to combine the first prior art reference with the second

prior art reference can be explicit or implicit and may provide further evidence of obviousness.

26. I understand that secondary (or objective) considerations are relevant to the determination of whether a claim is obvious. Such secondary (or objective) considerations can include evidence of commercial success caused by an invention, evidence of a long-felt need that was solved by an invention, evidence that others copied an invention, or evidence that an invention achieved a surprising or unexpected result, among others. I understand that such evidence must have a nexus, or causal relationship to the elements of a claim, to be relevant to a determination of obviousness of the claim.

27. I also understand that, at least in IPR proceedings, admissions in the patent or in the prosecution file history of the patent (Applicant Admitted Prior Art or “AAPA”) can be used to establish background knowledge possessed by a POSITA, to furnish a motivation to combine, to assess whether a patent’s claims would have been obvious, and/or to supply a missing limitation.

D. Claim Construction

28. I understand that, for purposes of my analysis, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning” at the time the alleged invention was made. In determining the ordinary and customary meaning, the words of a claim are given the plain meaning that those

words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to assist in the construction of a claim term. Additionally, treatises and dictionaries may be used, in limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing as long as such extrinsic input is consistent with the claim term as used in the claim.

29. For all claim terms considered in this Declaration, I have applied the ordinary and customary meaning of those terms as they would have been understood by a POSITA at the time the alleged invention was made. To the extent the Patent Owner or Petitioner proposes any constructions, or the Board construes any claims, I reserve the right to address such proposals or constructions. Under any reasonable construction of the claims, it is my opinion that the prior art does not disclose and/or suggest all the limitations recited in challenged claims of the '377 Patent.

E. Person of Ordinary Skill in the Art

30. I understand that my assessment and determination of invalidity must be undertaken from the perspective of what would have been known or understood by a POSITA at the time of the earliest patent application supporting the '377 Patent.

31. I have been informed and understand that the POSITA is not a real person, but rather a legal construct—a hypothetical person. This person is presumed to have known the relevant art at the time of the invention. I have been informed by

counsel that relevant factors in determining the level of ordinary skill include (1) the educational level of the inventor, (2) the type of problems encountered in the art, (3) prior art solutions to those problems, (4) the rapidity with which innovations are made, (5) sophistication of the technology, and (6) the educational level of active workers in the field. I further understand that the person of “ordinary skill” is not a person of extraordinary skill in the art. In other words, this person of ordinary skill is not necessarily an expert in the field.

32. As of the alleged June 30, 2011 priority date, a POSITA would have had a bachelor’s degree in Electric Engineering or equivalent, and approximately two years of experience working in the field of power converters, circuit design, device physics, or related technologies. Lack of work experience can be remedied by additional education, and vice versa.

33. At the time of the alleged invention, I was a person of at least ordinary skill in the art, and I have applied the perspective of the POSITA in forming and expressing my opinions below.

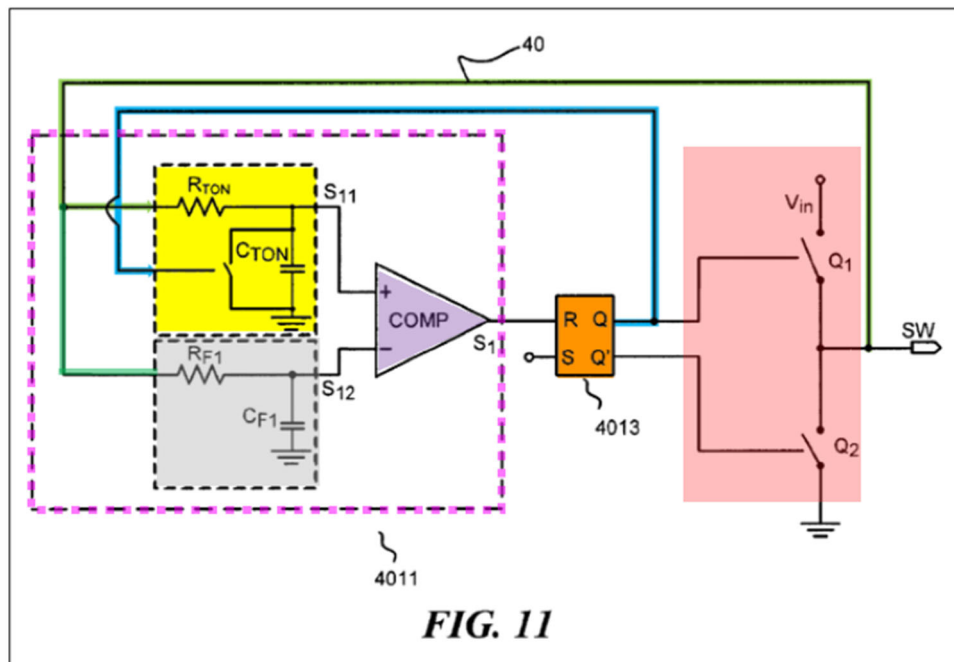
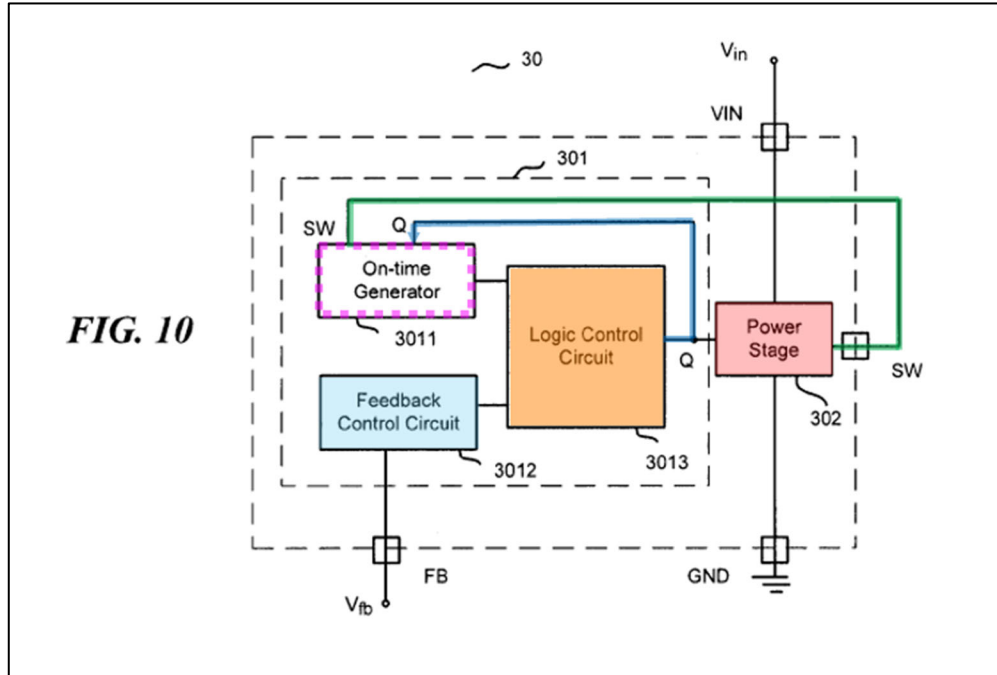
III. BACKGROUND OF THE ’377 PATENT

34. The ’377 Patent is directed towards switching circuits, and “more particularly but not exclusively to pseudo constant on time control circuit[s] and step-down regulators using it.” (EX1001 at 1:12-15).

35. The '377 Patent explains that, in pseudo constant on time (PCOT) control types for regulator circuits, the “on-time” of the regulator must be proportional to the output voltage divided by the input voltage: V_{OUT}/V_{IN} . (EX1001 at 1:55-64). The '377 Patent also explains that the switching frequency of the regulator is constant and does not vary with the output power. (EX1001 at 2:6-10). To achieve these aspects, the '377 Patent explains that prior art regulators implementing PCOT control need an output voltage pin V_{OUT} in the chip and may also need a frequency setting pin along with an external frequency setting resistor. (EX1001 at 2:11-20). The output voltage pin and frequency setting pin increase the chip size and cost. (*Id.*).

36. The '377 Patent reduces the need for the output voltage pin and the frequency setting pin. The '377 Patent describes that one way it achieves this is by providing an on-time generator 4011 that has an input voltage sensing circuit (yellow) that receives a switching signal SW (green) and also a control signal (blue) from the flip-flop 4013 (orange) (EX1001 at 8:18-41; *see also id.* at FIG. 4). Accordingly, the voltage converter does not need an output voltage pin V_{OUT} , a frequency setting pin $FREQ$, and the external frequency setting resistor, which were needed by the prior art; this helps reduce chip size and cost. (EX1001 at 7:65-66, 8:8-17).

37. Figures 10 and 11, which are reproduced and annotated below, illustrate these signals.



38. Independent claim 1 focuses on an input voltage sensing circuit (highlighted in yellow, to match the highlighted figure above) (which is a part of the pseudo constant on time control circuit (highlighted with the pink dashed box)) that receives the switching signal (highlighted in green) and the control signal (highlighted in blue), an output voltage sensing circuit (highlighted in gray) that receives the switching signal and generates an output voltage sensing signal, a comparator (highlighted in purple) that receives the outputs from the input voltage sensing circuit and the output voltage sensing circuit and generates an on-time signal, a feedback control circuit (highlighted in blue) that receives a feedback signal and generates an output signal, a logic control circuit (highlighted in orange) that receives the on-time signal and the output signal and generates the control signal, and a power stage (highlighted in soft red) that receives the control signal and generates the switching signal. Corresponding claim 1 limitations to the diagrams above are annotated below.

1. A step-down regulator, comprising:

a pseudo constant on time control circuit, wherein the pseudo constant on time control circuit comprises:

an on-time generator comprising:

an **input voltage sensing circuit** having a **first input terminal**, a **second input terminal** and an output terminal, wherein the **first input terminal is configured to receive a switching signal**

provided by the step-down regulator, the **second input terminal is configured to receive a control signal** provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the **input voltage sensing circuit generates an input voltage sensing signal** at the output terminal;

an **output voltage sensing circuit** having an input terminal and an output terminal, wherein the input terminal is configured to receive the switching signal, and wherein based on the switching signal, the **output voltage sensing circuit generates an output voltage sensing signal** at the output terminal; and

a **comparator** having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is coupled to the output terminal of the input voltage sensing circuit to receive the input voltage sensing signal, the second input terminal is coupled to the output terminal of the output voltage sensing circuit to receive the output voltage sensing signal, and wherein based on the input voltage sensing signal and the output voltage sensing signal, **the comparator generates an on-time signal** at the output terminal;

a feedback control circuit configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to generate an output signal in accordance with the feedback signal; and

a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the **logic control circuit generates the control signal**; and

a **power stage** configured to receive an input voltage and **the control signal**, wherein based on the input voltage and the control signal, the **power stage generates the switching signal**.

39. Independent claims 11 and 18 have similar limitations, as discussed above.

IV. CLAIM CONSTRUCTION

40. I understand that Patent Owner has proposed that the plain and ordinary meaning of the term “control signal” is a “logic signal with two distinct states.” I agree with this construction because it is described as such in the specification and claims. I elaborate on these reasons below.

41. Specifically, the claims support that the term “control signal” means a “logic signal with two distinct states.” For example, the control signal is generated by a logic control circuit” (for claims 1 and 11). (*E.g.*, EX1001 at 10:8-9 (limitation 1[D])). That control signal is connected to certain inputs, such as the second input terminal of a voltage sensing circuit. (*E.g.*, EX1001 at 9:44-45 (limitation 1[B2])). That control signal is also used by other circuit elements to generate other signals having logic values, such as the power stage that generates a switching signal based on the control signal. (*E.g.*, EX1001 at 10:10-13 (limitation 1[E])).

42. This is also true for claim 18 in which the control signal is generated by a flip flop (*e.g.*, EX1001 at 14:18-19 (limitation 18[E])), is used as an input into the on-time generator (*e.g.*, EX1001 at 13:22-23 (limitation 18[A])), and is used by the power stage to generate a switching signal (*e.g.*, EX1001 at 14:21-24 (limitation 18[F])).

43. This can be collectively seen in the claims as a whole. The claims, which have been highlighted below, show that the control signal (highlighted in blue), the logic control circuit (or flip flop) (highlighted in orange), the input voltage sensing circuit/on-time generator (highlighted in yellow), and the power stage (highlighted in soft red) are annotated below in the excerpted portions of claims 1 and 18.

44. I do not recite claim 11 below because it mirrors claim 1 only lacking the claimed power stage. (*See generally*, EX1001 at 11:41-12:13). Also, claim 18 recites a minimum off-time generator that receives the control signal and uses it to generate a minimum off-time signal. (EX1001 at 14:1-4).

45. An annotated showing of claim 1 is:

1. A step-down regulator, comprising:

...

an **input voltage sensing circuit** having a **first input terminal**, a **second input terminal** and an output terminal, wherein the **first input terminal is configured to receive a switching signal** provided by the step-down regulator, the **second input terminal is configured to receive a control signal** provided by the pseudo constant on time control circuit, and wherein based on the switching signal and the control signal, the **input voltage sensing circuit** generates an input voltage sensing signal at the output terminal;

...

a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates the control signal; and

a power stage configured to receive an input voltage and the control signal, wherein based on the input voltage and the control signal, the power stage generates the switching signal.

46. An annotated showing of claim 18 is:

18. A step-down regulator, comprising:

an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;

a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;

...

a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and

a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.

47. In my opinion, because of the foregoing (*e.g.*, the control signal is generated by a logic circuit (such as a flip flop), the control signal is an input into

the on-time generator, and the control signal is used by the power stage to control the switches (*e.g.*, to control them to turn off or on), so that they can generate a switching signal), the “control signal” is a logic signal with two distinct states. A POSITA would understand that such a “control signal” would be a digital signal with two states in order to control this claimed functionality. For example, the control signal could turn the high and low side switches off and on, meaning that it should have a logical high or low state (*e.g.*, a ‘1’ or ‘0’) to control the turning on and off of the switches in the power stage.

48. Petitioner’s expert agreed with this during his deposition. Specifically, Dr. Holberg testified:

Q Back to the claim language. 10 5 through 9 states that “the logic control circuit generates a control signal.”

You see that?

A Yes.

Q Do you understand the control signal that is generated to be a two-state signal?...THE WITNESS: Yes.

(EX2006 at 22:11-19).

Q If you could look at the control signal in column -- hold on. Let me see -- 14, lines 19 to 20. It says: “The flip-flop generates the control signal.”

A Yep, I see that.

Q In your opinion, is the control signal of claim 18 a two-state signal?

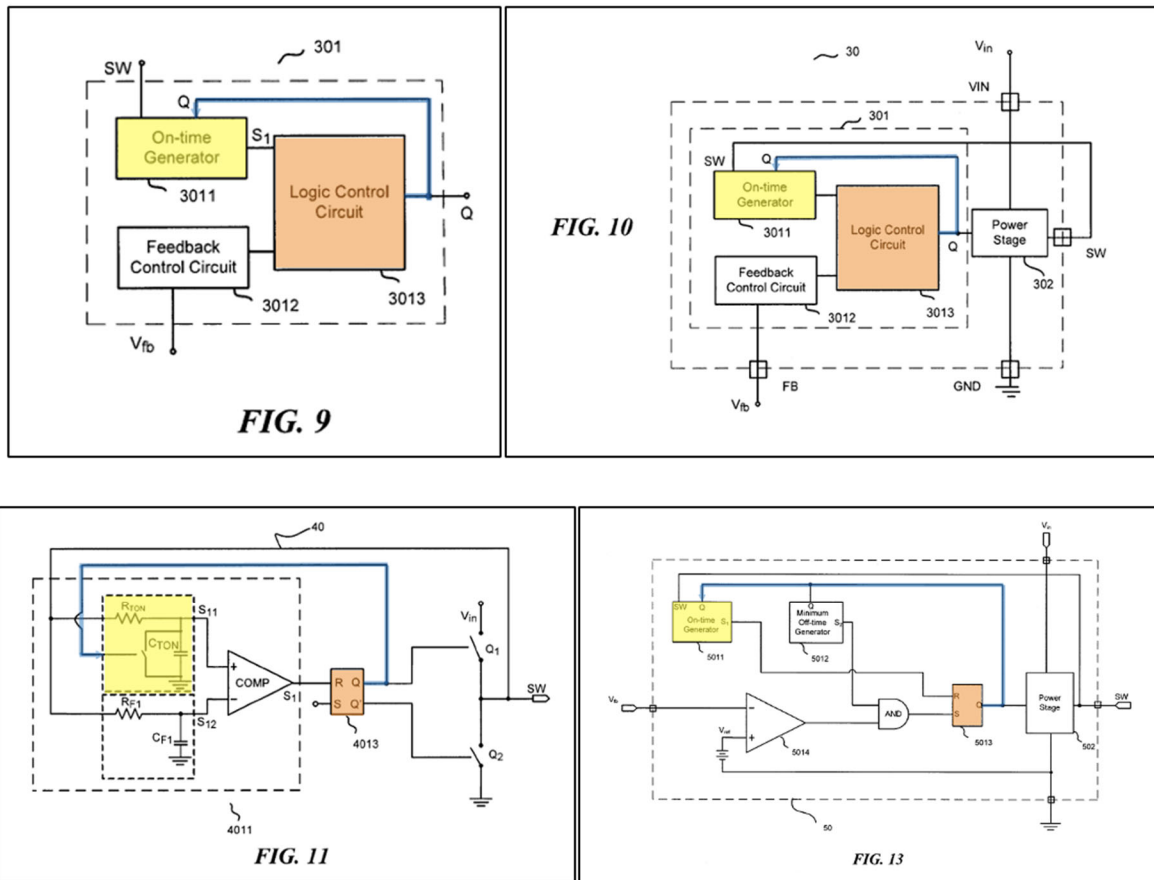
A Yes.

(EX2006 at 25:10-18; *see also id.* at 14:15-18:4 (stating that the signal Q from the specification is a two-state signal).)

49. The '377 Patent's specification also supports Patent Owner's construction that the plain and ordinary meaning of the term "control signal" is a "logic signal with two distinct states." The '377 Patent shows various embodiments of the system claimed in claims 1, 11 and 18. The four embodiments the '377 patent are shown in Figures 9, 10, 11, and 13. While I understand that the claims are not limited to these four embodiments, they are all consistent in that they describe the "control signal" as a logic signal with two distinct states.

50. In Figures 9, 10, 11, and 13, the control signal Q is output from the logic control circuit (or specifically, the flip-flop in claim 18), and enters the on-time generator's input voltage sensing circuit's second input (or just the on-time generator for claim 18). (EX1001 at 7:44-47 (stating for Fig. 9 that "[t]he on-time generator 3011 receives . . . a control signal Q provided by the PCOT control signal 301"), 7:65-66 ("FIG. 10 illustrates a step-down regulator 30 comprising the PCOT control circuit 301 of FIG. 9."), 8:28-30 ("As shown in FIG. 11, the on-time generator 4011 receives . . . the control signal Q provided by the flip-flop 4013"), 8:66-9:1 (stating for Figure 13 that "[t]he on-time generator 5011 receives . . . a control signal Q provided by the flip-flop 5013"))).

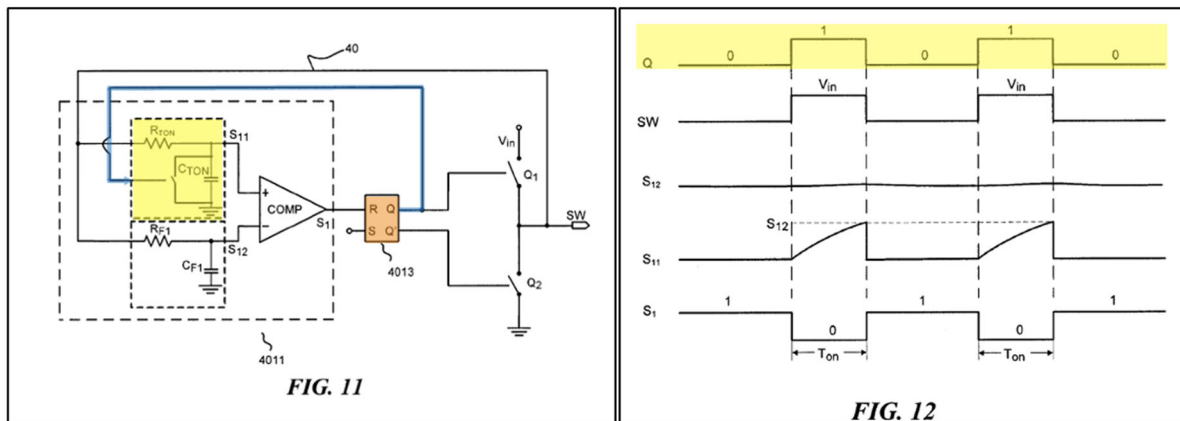
51. This is shown in the annotations of Figures 9, 10, 11, and 13 below. Specifically, the control signal is highlighted in blue and is between the logic control circuit (which is highlighted in orange) and the on-time generator (which is highlighted in yellow).



52. Figures 11 and 12 are clear that the “control signal” Q, which is highlighted in blue, is a logic signal with two distinct states. Specifically, the specification describes that, for Figure 11, the control signal Q has an inverse which is Q'. (EX1001 at 8:32-34 (“The control signal Q controls the high-side switch Q1,

and the complementary signal Q' of the control signal Q controls the low-side switch Q_2 .”). Accordingly, because Q' is the inverse of Q , Q must be a logic signal with distinct logic states. The specification further supports this, stating that the control signal Q can have a logic low (0) or logical high value (1), when it describes the output of the flip-flop 4013 (*e.g.*, the output of the flip-flop is the control signal). (EX1001 at 8:28-30 (“as shown in FIG. 11, the on-time generator 4011 receives the switching signal SW provided by the step-down regulator 40 and the control signal Q provided by the flip-flop 4013.”) 8:43-44 (“As shown in FIG. 11 and FIG. 12, when $Q=1$, the high-side Switch Q_1 is turned on”), 8:53-55 (“The on-time signal S_1 resets the flip-flop 4013 to change the control signal Q into logical low ($Q=0$). Thus, the high-side switch Q_1 is turned off”)).

53. Figure 12 is a timing diagram for Figure 11 and states that the control signal Q can have a value of 0 or 1 (*e.g.*, discrete logic states). (EX1001 at 8:43-44 (“As shown in FIG. 11 and FIG. 12, when $Q=1$, the high-side switch Q_1 is turned on”), 8:53-56 (“The on-time signal S_1 resets the flip-flop 4013 to change the control signal Q into logical low ($Q=0$). Thus, the high-side switch Q_1 is turned off, and the low-side switch Q_2 is turned on”).) This is reflected in the annotations of Figures 11 and 12 below.



54. While Figures 11 and 12 are clear that the “control signal” Q, which is highlighted in blue, is a logic signal with two distinct states, this is also true for Figures 9, 10, and 13. Petitioner’s expert Dr. Holberg agrees that all embodiments of the ’377 patent describe the control signal as a logical signal with two distinct logic states.

Q If I understand you correctly, you’re stating that the signal Q from the logic control circuit is a two-state signal? . . .

THE WITNESS: . . . So the patent speaks of it in terms logical values 0 and 1.

(EX2006 at 16:19-17:21).

55. Dr. Holberg also confirmed that the control signal would not be an analog signal according to the specification.

Q Is the signal an analog or digital signal? And this is, again, referring to signal Q of figure 10.

THE WITNESS: . . . So, in that sense, you know, you’re asking is it analog or digital. Typically, when you think

about a digital system, it's -- like in a 5-volt system, it's going to be -- the value's going to be 5 voltage or ground.

Of -- in this case -- so it has two states. Digital signals typically have two states, one of two states.

(EX2006 at 14:15-15:22).

Q In your opinion, is the control signal of claim 18 a two-state signal?

A Yes.

(EX2006 at 25:16-18).

56. In light of this evidence, a POSITA would understand that the plain and ordinary meaning of the claimed control signal is a logic signal with two distinct states.

57. Petitioner's use of the term "control signal" rests on an implied construction that is incorrect. For the reasons I list below, Petitioner would have the term "control signal" be a signal that has multiple contradictory logic states at the same time. I expand on this below.

V. REASONS FOR PATENTABILITY

A. Ground 1: Petitioner has failed to show that Tateishi anticipates the independent claims of the '377 Patent

58. In my opinion, Petitioner has failed to show that Tateishi anticipates the independent claims of the '377 Patent. Specifically, Petitioner has failed to show that Tateishi anticipates any of the claim limitations that invoke the claim term "control signal" for a few reasons.

59. First, I understand that, when a term is used in a claim and refers back to the same term introduced previously in that claim, it must refer to the same structure. This is called antecedent basis. In my opinion, Petitioner does not adhere to the antecedent basis requirement and is inconsistent in which signals are identified to make up a “control signal.” Petitioner impermissibly refers to different logical signals to meet the single, required claimed “control signal.”

60. Second, because the “control signal,” according to Petitioner, contains different logical signals, Tateishi does not anticipate the independent claims because those signals are distinctly different and are not always synchronized as to logical states. In other words, the logic comparison between the two different signals is contradictory, and thus, in my opinion, the two signals together could not be considered a “control signal” under the construction that I explained above—that “control signal” means a logical signal with two distinct states and cannot refer to completely different signals.

61. Third, the claims require that the same “control signal” is used by different circuits to generate certain other distinctly different signals. For example, the “input voltage circuit” uses the “control signal” and the switching signal to generate “an input voltage sensing signal.” Similarly, the “power stage” uses the “control signal” and an input voltage to generate “the switching signal.” The problem, though, is that Petitioner points to one of the logic signals to meet the

alleged “control signal” input into the “input voltage circuit” and points to another logic signal to meet the alleged “control signal” input into the “power stage.” As I described earlier, this violates the antecedent basis requirement, in my opinion. Different signals are respectively used to generate the alleged “input voltage sensing signal” and the “switching signal” even though the claims require that the same “control signal” be the one signal that the input voltage sensing circuit and the power stage use to generate their outputs.

62. Fourth, the Petition modifies Tateishi with a teaching that is not literally present in the reference. The Petition only asserts anticipation for the independent claims. I understand this is improper, because relying on a teaching not within the four corners of Tateishi should fall under an obviousness theory, not anticipation. Thus, the Petitioner further fails for this reason in my opinion.

1. Petitioner does not adhere to antecedent basis and is inconsistent in which signals make up a “control signal” in independent claims 1, 11, and 18

63. In my opinion, Petitioner has failed to show that Tateishi anticipates the independent claims of the '377 Patent because Petitioner identifies several different signals to be the single, claimed “control signal” and mixes and matches these signals for each limitation. I understand that this approach directly violates the requirements for antecedent basis and, therefore, should be dismissed.

64. The independent claims of the '377 Patent (EX1001) refer to a single

“control signal.” For example, independent claim 1 refers to an input voltage sensing circuit that receives the control signal and generates an input voltage sensing signal. (claim 1 at 9:40-50). That control signal is generated by the logic control circuit (claim 1 at 10:9). That same control signal is also an input to the power stage (claim 1 at 10:11) and, based on the control signal, the power stage generates a switching signal (claim 1 at 10:12-13). Independent claim 11 similarly recites that the on-time generator’s input voltage sensing circuit receives the control signal and based on the control signal, generates the input voltage sensing signal (claim 11 at 11:44-52). And the logic control circuit generates the control signal (claim 11 at 12:13). Independent claim 18 (the other independent claim) similarly recites that the control signal is an input into the on-time generator, and the on-time generator uses it to generate an on-time signal (claim 18 at 13:21-25). The minimum off time generator receives the control signal and uses it to generate a minimum off time signal (claim 18 at 14:1-4). The flip-flop generates the control signal (claim 18 at 14:18-19), and the power stage receives the control signal and generates the switching signal (claim 18 at 14:21-24). Accordingly, in my opinion, in all of these claims, the term “control signal” must be the same signal throughout each respective claim limitation.

65. Petitioner’s expert, Dr. Holberg, agrees that the term “control signal” must refer to the same signal throughout all of the claim limitations, and that the phrase “a control signal” in each respective claim provides the antecedent basis for

“the control signal” throughout the respective claim. Specifically, Dr. Holberg stated:

Q In your opinion, do all instances of the language "control signal" in claim 1 refer to the same signal?

THE WITNESS: . . . So they would all be the same.

(EX2006 at 23:6-24:6).

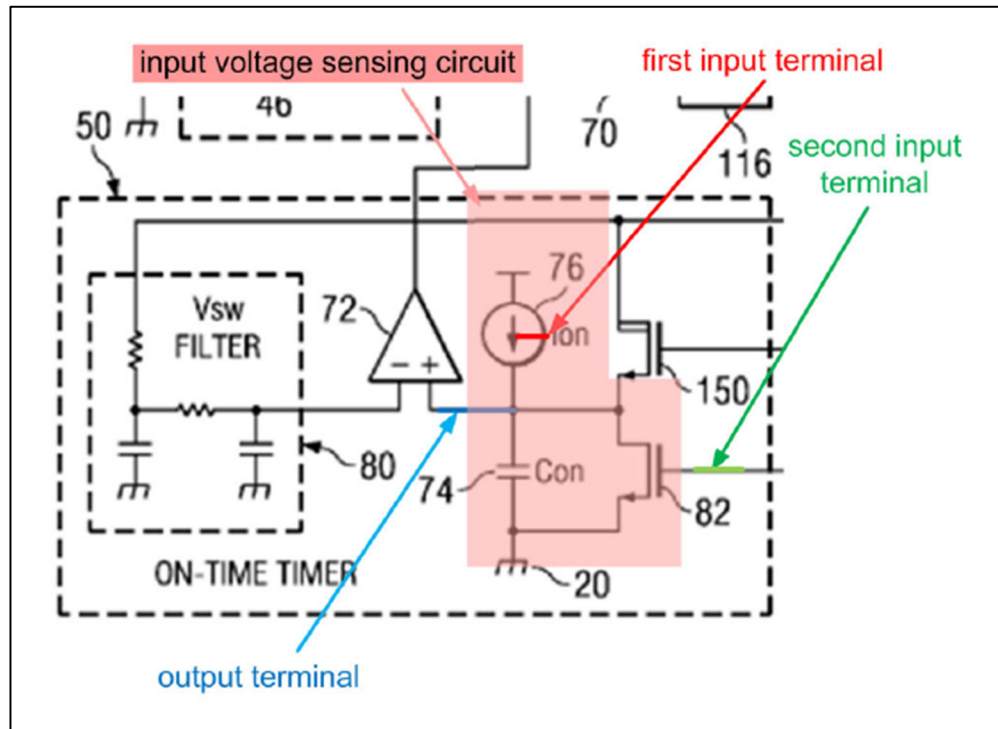
Q In your opinion, do all instances of the recited control signal in claim 18 refer to the same signal?

A Yeah. Every instance where it says “the control signal,” it's -- the antecedent for that is “a control signal” found in line 21, 2, 3, of column 13.

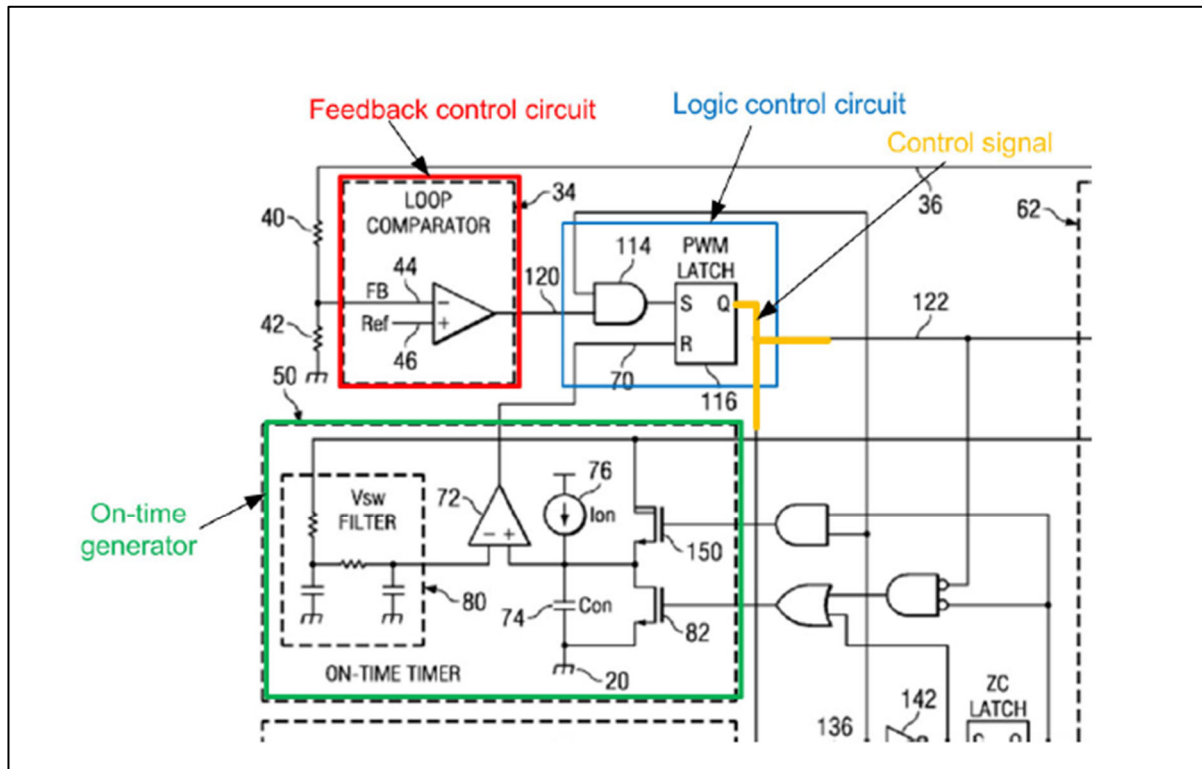
(EX2006 at 26:7-13).

66. The Petition, however, identifies separate signals instead of a single “control signal,” violating the antecedent basis requirement, in my opinion.

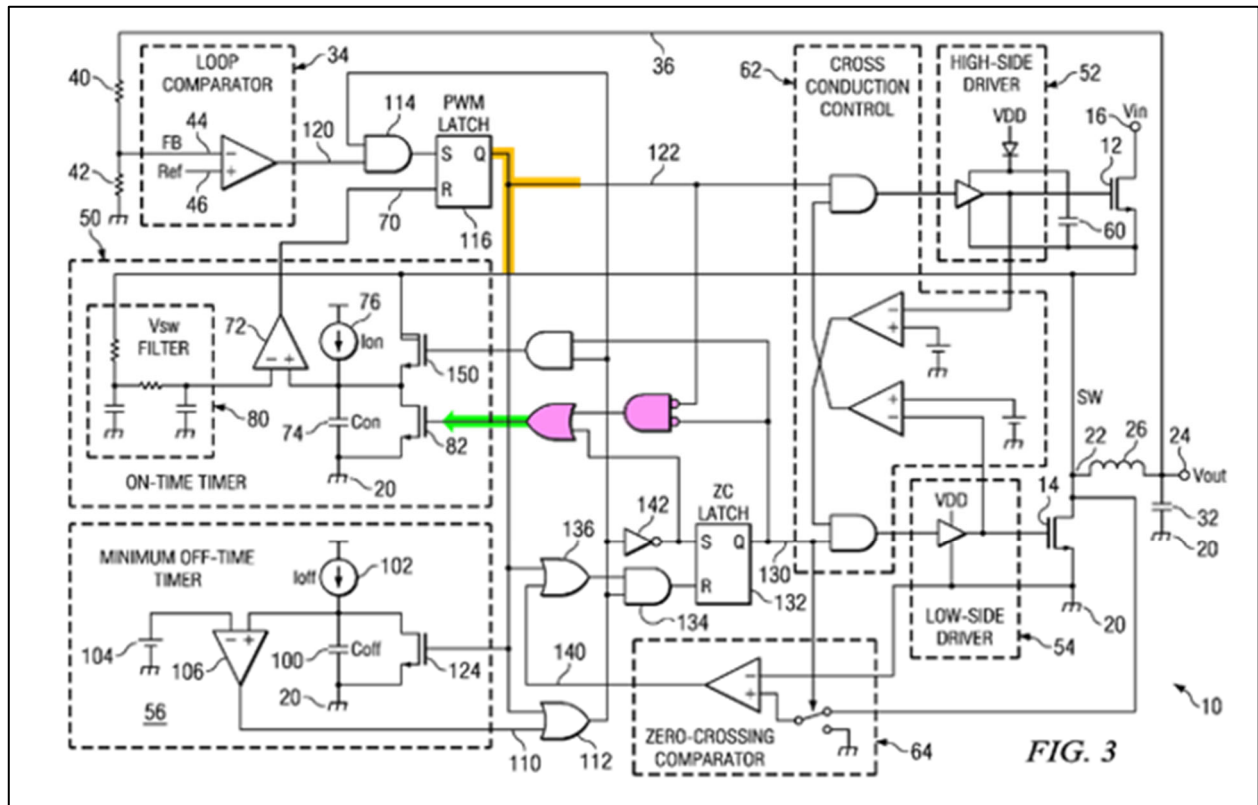
67. For example, limitation 1[B2], as I discuss above, requires that the second terminal of the input voltage sensing circuit receives the control signal. (EX1001 at 9:45). In analyzing limitation 1[B2], Petitioner identifies the signal entering the alleged “second input terminal” of the alleged input voltage sensing circuit as the claimed “control signal.” (Pet. at 37). Petitioner’s annotated image of Tateishi’s Figure 3 is reproduced below, showing the alleged control signal entering the green highlighted input terminal:



68. But Petitioner is not consistent in identifying the same signal when Petitioner analyzes limitation 1[D]. Limitation 1[D], as I explained above, recites that the control signal is generated by the logic control circuit. (EX1001 at 10:8-9). Petitioner, however, identifies a separate logic signal for this. (Pet. at 45). Petitioner's annotated image of Tateishi's Figure 3 is reproduced below, identifying the yellow highlighted signal, which is exiting the PWM Latch 116, as the alleged control signal:



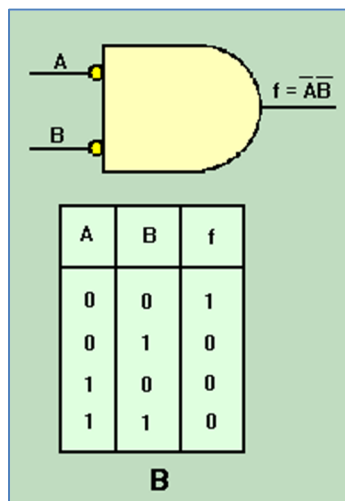
69. Petitioner identifies different logic signals in limitations 1[B2] and 1[D] even though the claim requires that they be the same signal. As can be seen from the full Figure 3 of Tateishi, reproduced and annotated below, the two different logical signals are shown. Specifically, Petitioner's alleged control signal to allegedly meet 1[B2] is shown in green, and the alleged control signal to allegedly meet 1[D] is shown in orange (annotated below).



70. In my opinion, the green signal and the orange signal are two different logical signals. The orange signal (122) passes to one of two inverting inputs of a logical AND gate the output of which provides one of two inputs to an OR gate (both logic devices of which are shown in pink). It is the output of this OR gate that Petitioner then references as a second, distinctly different logical signal output (shown in green).

71. The other inverting input to that AND gate is the output 130 of the ZC latch 132 (*see above*). An AND gate with inverting inputs only outputs a high signal if both input signals are low. (*See EX2003 at 3*). This can be seen from what is referred to as the “truth table” of a logic device (such as an AND gate with inverting

inputs). The truth table (shown below) illustrates that, with such a device, the AND gate only outputs a high signal if both input signals are low, and if any of the inputs are high, then the output is low. (EX2003 at 2 (showing a portion of Figure 2-18 for the AND gate with inverting inputs). Thus, a POSITA would understand that the output of the AND gate with inverting inputs is not just dependent on whether the alleged control signal is high or low, but also whether the ZC latch output signal is high or low. If both signals become low, then the output of the AND gate with inverting inputs is high, but otherwise, if either the alleged control signal or the LC latch output signal goes high, then the entire AND gate (with inverting inputs), would go low.



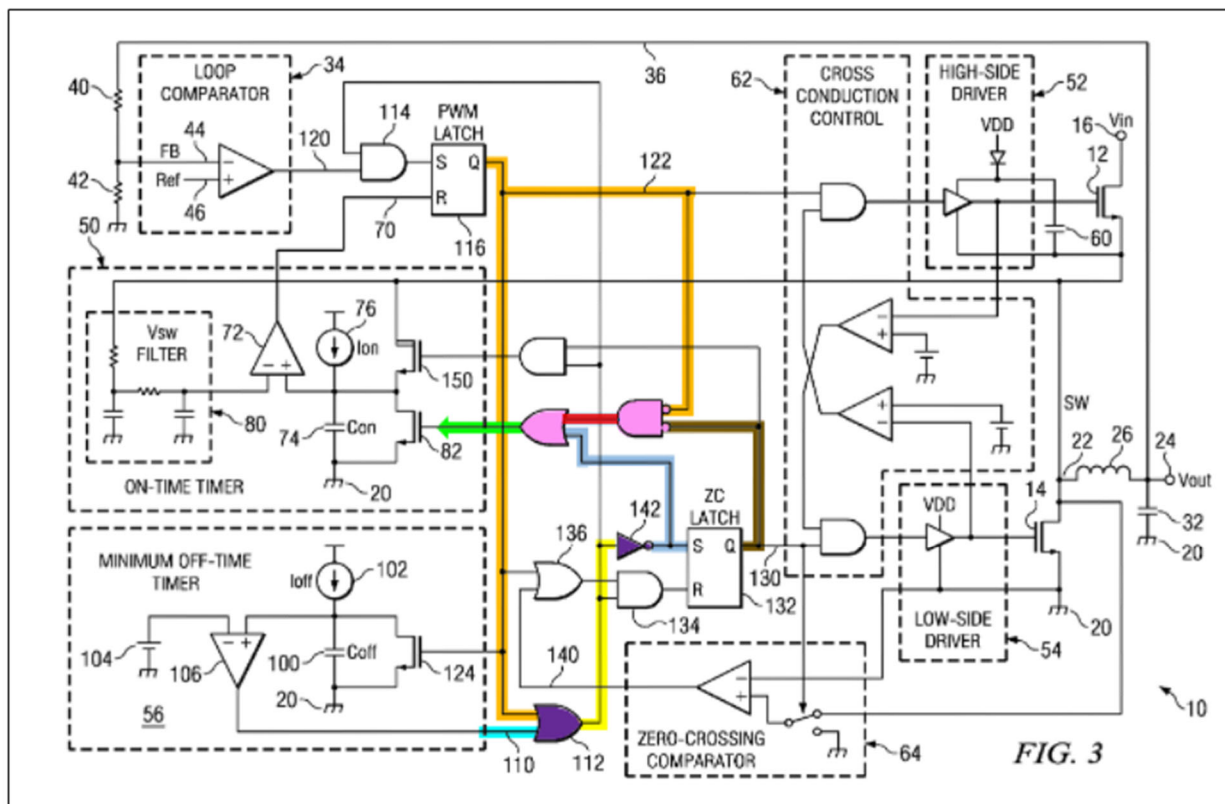
72. Thus, the logical output of the AND gate with inverting inputs is dependent upon the logical values of *both* the alleged “control signal 122” (shown in orange) and the output 130 of ZC latch 132 (shown in brown).

73. The signal difference is further demonstrated by Figure 3 annotated below. The ZC latch 132 output Q (shown in brown below) is dependent upon other signals from other logic blocks. For example, Tateishi states that the zero-crossing comparator 64, which affects the ZC latch 132 input, also controls the effect of the input 122 to switch 82 and is thus, an arbitration input into the identified second input of the input voltage sensing circuit. (EX1007, ¶ 60 (“In another embodiment corresponding to the DC to DC buck converter of FIG. 3 a zero crossing is detected. The zero-crossing comparator 64 detects this zero crossing and turns off the low side switch 14 through the zero crossing SR latch 132. At the same time, the precharging transistor 150 is turned off and the discharge switch 82 is turned on and maintains the voltage across the capacitor 100 at zero.”). Another input into the ZC latch 132 is the output of the OR gate 112, and also the output of the inverter 142 (shown in purple below).

74. Thus, the output of the AND gate with inverting inputs is dependent upon the orange signal 122 and the brown signal (which is the output of the ZC latch 132). The output of the AND gate with inverting inputs (shown in Pink) is also always 0 unless both the alleged control signal 122 and the ZC latch output are both 0.

75. Additionally, the output of the AND gate with inverting inputs is an input into the pink OR gate. The pink OR gate also has an input which is highlighted

in blue below. This blue signal is the result of other logic. Specifically, the signal 122 is ORed (112) with the output of the minimum off timer 110 (shown in aqua). This output of the OR gate 112 (shown in yellow) is then inverted at 142 (shown in purple). This inverted output enters the OR gate shown in pink, and that OR gate's output is the green signal entering the switch 82.



76. In view of the above, the green signal that is entering switch 82 is not the same logical signal as the orange signal 122, in my opinion. There are a number of logical operations that occur between the green and orange signals. The signals petitioner identifies as the “control signal” in 1[B2] and 1[D] are not actually the same logical signal. Petitioner and its expert Dr. Holberg do not address this

distinction. (*See* Pet. at 36-39, EX1003, ¶¶ 84-88, Pet. at 43-45, EX1003, ¶¶ 97-99).

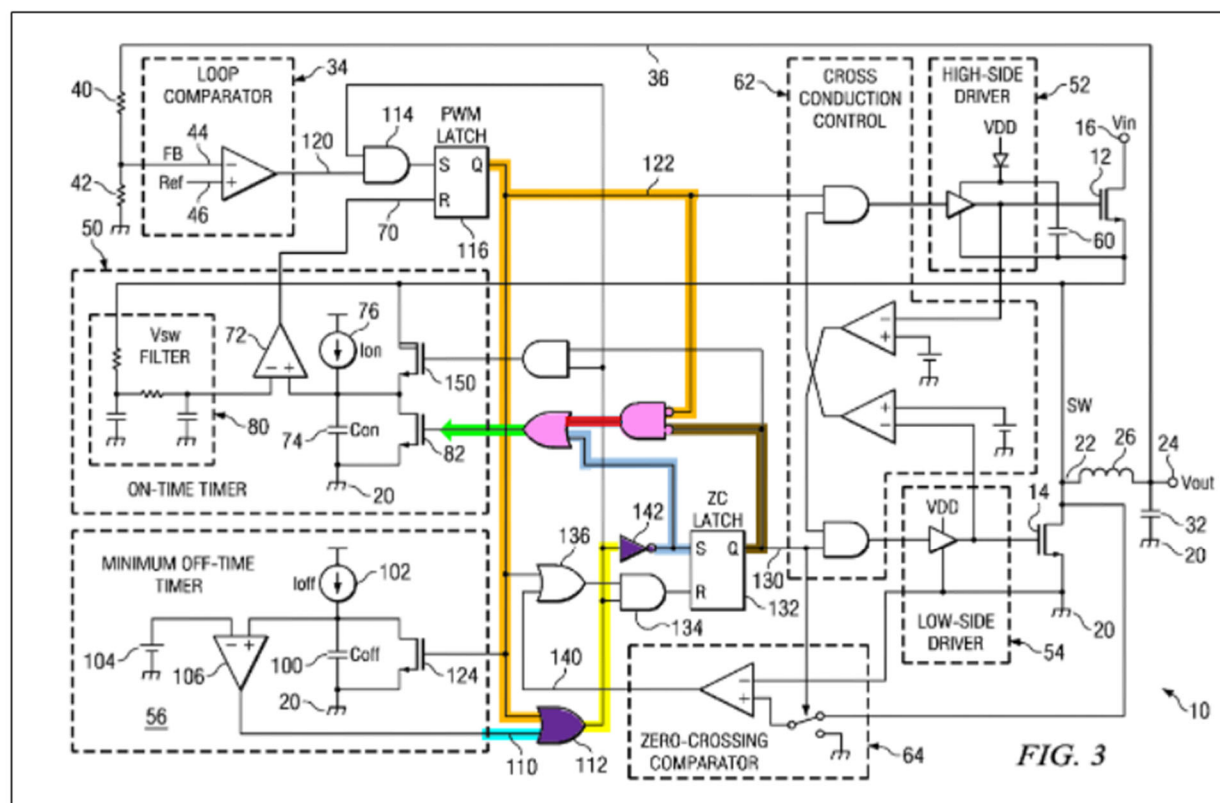
77. I describe the above issues with respect to claim 1, but claims 11 and 18 suffer from the same issues in Petitioner's analysis. For example, as I described above, limitation 11[B1] recites "second input terminal is configured to receive a control signal" while 11[D] recites that "the logic circuit generates the control signal." (Pet. at 61 and 63 (incorporating claim 1 analysis).) Limitation 18[B] requires that the "minimum off time generator [is] configured to receive the control signal" while 18[E] requires that "the flip-flop generates the control signal." (Pet. at 66 and 71 (identifying the same elements).) Accordingly, Petitioner has not shown that Tateishi anticipates claims 1, 11, or 18 in my opinion.

2. Petitioner and its expert fail to show that Tateishi anticipates the claims using a proper construction of control signal

78. Even if the Petitioner can point to two different logical signals and argue that they are the same "control signal," which they are not, it is my opinion that Petitioner still fails to show that Tateishi anticipates the independent claims. This is because the "control signal" that Petitioner identifies for 1[B2] is logically inconsistent with the alleged "control signal" that Petitioner identifies for 1[D]. The identified control signal is, *e.g.*, "0" while another part of it can be either "1" or "0" depending on other logic of Tateishi's circuit.

79. A logical analysis of Tateishi's Figure 3 conveys this logic discrepancy

among the signal that enters switch 82 (*e.g.*, the alleged 1[B2] control signal) and the signal 122 exiting the PWM Latch 116 (the alleged 1[D] control signal). An annotated Figure 3 of Tateishi is reproduced below to guide my discussion of the logic of the different signals.



80. Specifically, when the alleged 1[B2] control signal 122 (orange) is 0, the green signal (the alleged 1[D] control signal) can be “1” or “0” depending on the value of an entirely different signal, the minimum off-timer’s output 110 (aqua). To expand, assume that the orange signal 122 (the output of PWM Latch 116) is 0. This orange signal 122 provides an input to the OR gate 112 (purple). The output of that OR gate is 0, unless the output of the minimum off-time timer 110 (aqua) is 1. If the

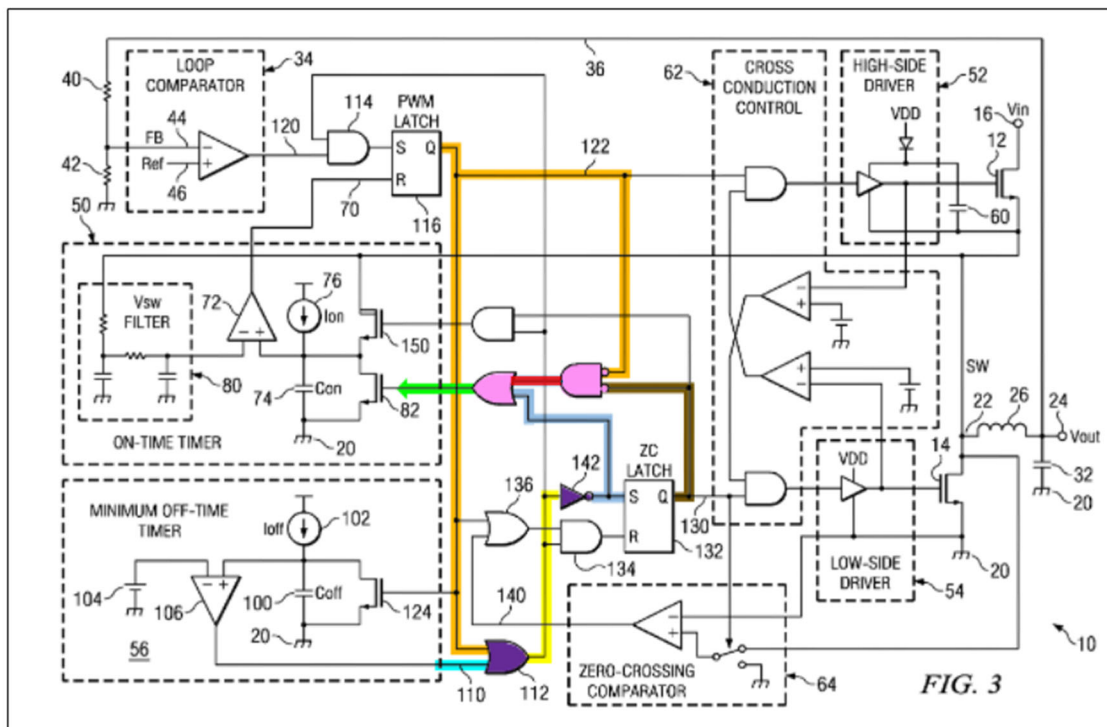
output 110 is 1, then the output (yellow) of the OR gate 112 (purple) is 1. That yellow signal passes to the inverter 142 (purple) which generates an output as the blue signal. If the output 110 is 1 (while orange signal 122 is 0), then this means the blue signal is 0. However, if the output 110 (aqua) is 0, then the blue signal is 1. The OR gate (pink) may output a 0 or 1 in this situation, but the control signal 122 does not alone have the same logic value as the green signal.

81. Additionally, when the alleged 1[B2] control signal 122 is still 0, the green signal (the alleged 1[D] control signal) can be “1” or “0” depending on the value of not just the minimum off-timer’s output 110 (aqua), but also the ZC latch 132’s Q output 130 (brown). If the ZC Latch 132’s output Q (brown) is 1, the output of the AND gate with inverting inputs (pink) is 0 (based on the logic described above regarding AND gates with inverting inputs). Thus, the green signal is 1 if the minimum off-time signal 110 is 0, and the green signal is not entirely dependent upon the signal 122 (orange)’s logical value. On the other hand, if the ZC latch output is 0, then the AND gate with inverting inputs will output a 1, and then green signal would have a logical value of 1 (because an OR gate always outputs a 1 unless both inputs are 0).

82. Thus, if the orange signal 122 is ‘0,’ the green signal may also not be controlled by the same logical value of ‘0.’ The green signal could be ‘1’ if the minimum off-time generator signal 110 (aqua) is also ‘0.’ Or, the minimum off-time

generator's signal 110 is '1,' and the output of the zero crossing comparator 140 is '1,' then the output of the ZC latch 130 (brown) would be '0' (because the ZC latch's reset button would have an input of 1 and then S input would have a value of '0'), and the green signal would have a value of '1' because the OR gate passes a '1' through it and the AND gate with inverting inputs would have both inputs (orange signal 122 and brown signal 130) be '0.'

83. This discussion above is reflected in the following truth table, which shows the logic of the different signals according to their annotated colors (to make it easier for readability).



Circuit Diagram

Orange	Brown	Red	Blue	Green	Aqua	Yellow
0	1* ¹	0*	1	1	0	0
0	0	1	0*	1	1	1
0	1	0	0	0	1	1
1	0	0	0	0	0*	1
1	1	0	0	0	0*	1
1	0	0	0	0	1*	1

Logic Table

84. This truth table illustrates that the green signal is not only logically dependent upon orange signal 122, but it is also dependent upon the minimum off-time output 110 (aqua) and the output of the ZC latch 130 (brown). Consequently, one cannot define the state of the green signal output based solely on the state of the orange signal 122. Further, it is clear from the logical arrangement between the orange signal and the green signal that the two signals' respective transitions between one state to another state do not occur at the same time since the green signal output depends in part upon the state transition of the orange signal.

85. In other words, a POSITA would understand that the green output signal is a function of the orange signal ("O"), the aqua signal ("A"), and the brown

¹ The * represents a "don't care" meaning that the value does not affect the eventual green output.

signal (“B”), and can be represented via logic equation by:

$$G = (\overline{A + O}) + (\overline{B} \times \overline{O}) = (\overline{A} \times \overline{O}) + (\overline{B} \times \overline{O}) = (\overline{A} + \overline{B}) \times \overline{O}$$

86. Green depends on values of Aqua and Brown, not just Orange. Green is distinct from Orange, and is not a mere delay or an inverse relationship. Taken further, by the way of analogy, Petitioner is in effect stating that any signal of a circuit can act as the “control signal” while another signal can be that “control signal” because there is some logical relationship. In other words, the size of the logical equation is not the issue, it is the fact that there is a logical equation—including other logical signals—that separates the two signals and makes them logically distinct states. A POSITA would not have understood an equation’s input (and its output) as both being the same control signal. Green and orange are not the same “control signal.”

87. Despite the green signal being a logically distinct signal from the orange signal, Petitioner seems to be arguing that one signal can be considered the same signal as the other signal if, under some conditions, both signals exhibit the same output level state. Such illogic is far from persuasive.

88. Petitioner’s expert Dr. Holberg confirmed that the aqua and brown signals can change the green signal’s logic values. Dr. Holberg testified that the green signal’s state is controlled via the off-timer’s output 110 (aqua)’s state.

(EX2006 at 37:3-6 (“Q And when logic – when 110 goes logic state high, the output of OR gate 112 will likewise go high, correct? A that is correct” (thus, by inverter 142, the green signal would be 0)); EX2006 at 37:10-18 (“For the next question, we’ll assume logic 110 – the signal 110 is logic 0 and 122 is logic 0, as you stated in a previous answer today. A Correct. Q And when that occurs, you stated inverter 142 will be – will invert that 0 to 1, which will set the Q output to 1, correct? ... THE WITNESS: That is correct.”)). He also testified that Coff 100 controls the minimum off-time. (EX2006 at 47:4-8, 48:6-9). And when the orange signal is initially triggered to “0,” that the off-timer’s output 110 (aqua) will be “1” some time after the Coff 100 charges (EX2006 at 32:13-33:8, 34:10-37:18). He also testified that the ZC latch 132’s output signal 130 (brown) will trigger to “0” or “1” based on a zero crossing, and that detection is dependent upon load. (EX2006 at 49:6-49:19). Thus, the value of Coff and the load provide logical signals that affect control of switch 82. The switch 82 is not controlled via the orange signal.

89. Petitioner’s analyses of independent claims 11 and 18 possess the same issues. Petitioner relies on its same analysis of 1[B2] and 1[D] to allegedly meet these claims. (*See* Pet. at 61, 63, 66, 71-72).

90. Accordingly, it is my opinion that Petitioner has failed to show that Tateishi anticipates the claims because Petitioner mixes and matches two distinctly different signals (the orange and green signals), each signal having distinct logic

states. As I explained above, the proper construction of the term “control signal” is a signal with two distinct logic states. The two signals (the orange and green signals) are separate and distinct, and they cannot both be a signal with two distinct logic states.

3. Other claim limitations further demonstrate why Petitioner cannot point to multiple signals to be the claimed “control signal”

91. In my opinion, other claim limitations further demonstrate why Petitioner cannot point to multiple signals as the claimed “control signal.”

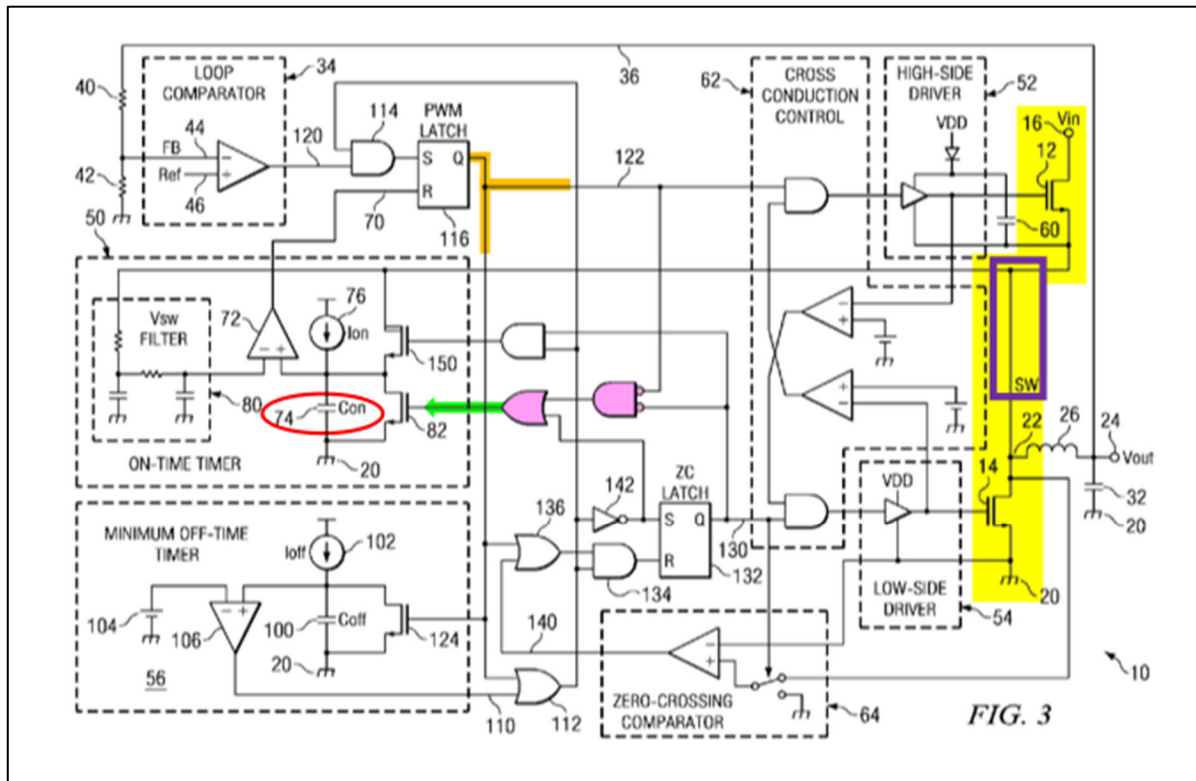
92. Specifically, the claims require that, “based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal” (Limitation 1[B2]). Claim 11 recites an identical requirement that “based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal” (Limitation 11[B1]). Claim 18 recites a similar requirement that “based on the switching signal and the control signal, the on-time generator generates an on-time signal” (Limitation 18[A]).

93. The claims also require that “wherein based on the input voltage and the control signal, the power stage generates the switching signal.” (Limitation 1[E]). Claim 18 recites a similar requirement that “wherein based on the control signal, the power stage converts an input voltage into the switching signal.” (Limitation 18[F]).

94. Petitioner shows support for the first requirement (that the input voltage sensing signal/on-time signal is generated based on the control signal) by pointing to the green-annotated signal. (Pet. at 36-39, 66). Petitioner also shows support for the second requirement (that the switching signal is generated based on the control signal) by analyzing the orange-annotated signal. (Pet. at 45-47, 72 (which the Petitioner identifies as purple)). Problematically, Petitioner's arguments do not make sense when viewing both the orange and green signals together. In other words, Petitioner's arguments only work when the green and the orange signals are viewed in isolation from each other.

95. With respect to the first requirement, and the limitation reciting that "based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal," (which is generally recited in claim 1, 11, and 18), Petitioner points to the voltage across the capacitor 74 as the voltage that generates the input voltage sensing signal. (Pet. at 37). Petitioner also points to the input into switch 82 as the alleged control signal. (Pet. at 37). Petitioner suggests that the green signal controls switch 82, and thus it generates the input voltage sensing signal because if the green signal is 1, the capacitor will discharge but a 0 would charge the capacitor. (*See* Pet. at 37). This is shown below in the annotated Figure 3 of Tateishi, which shows the capacitor 74 (*e.g.*, the capacitor that outputs an input voltage sensing signal) and the green signal

(e.g., the alleged control signal).



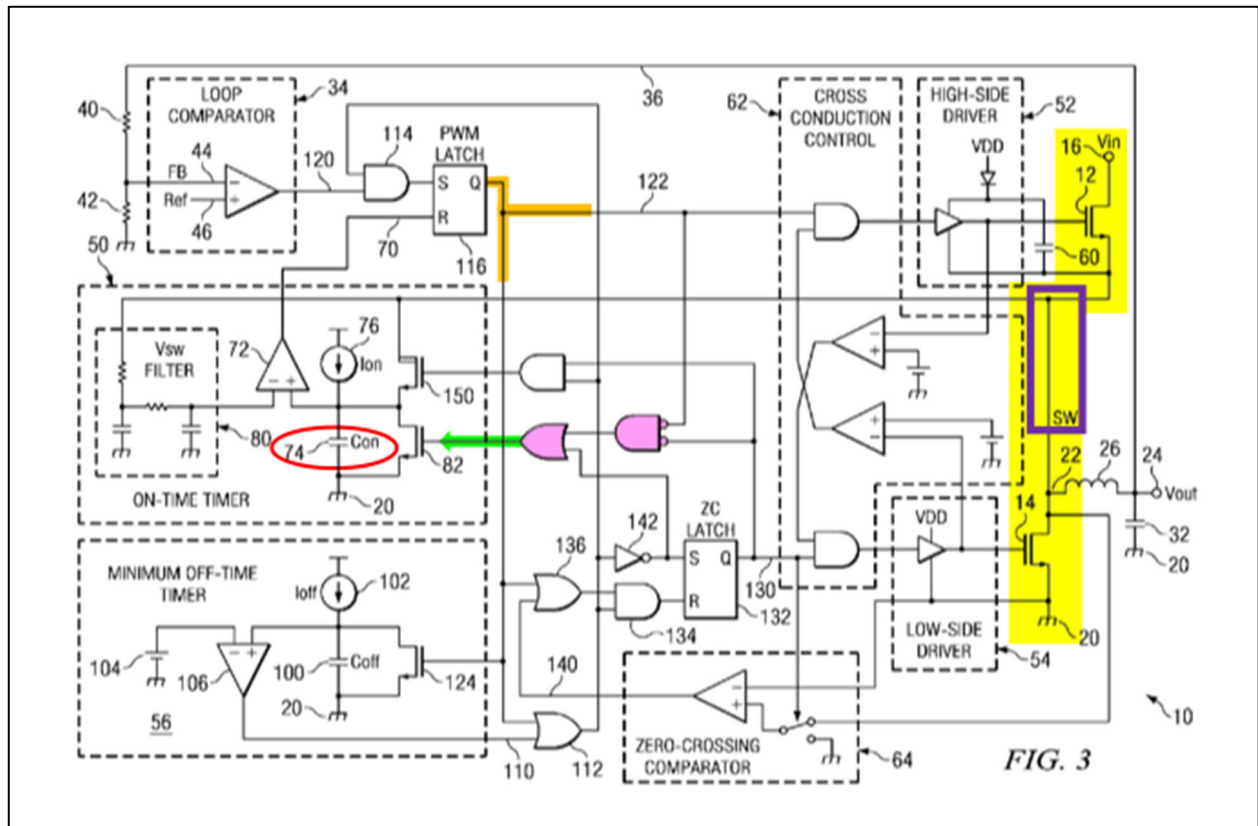
96. Petitioner’s arguments do not work, though, when considering the other claimed “control signal.” Specifically, the orange signal (which is the other claimed control signal) does not control whether the green signal is a 0 or 1. As I described above, the green signal depends on the value of both the aqua and brown signals shown in the above logic table.

97. Thus, the orange signal does not control whether the capacitor 74 is discharged (via the turning on or off of switch 82). The claim recites that, “based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal.” But the orange

alleged “control signal” does not affect the input voltage sensing signal because the green signal can be “1” or “0” when the orange signal is “0.” The “input voltage sensing signal” is not generated “based on the switching signal and the control signal” because it is based on the green signal, and not the orange signal as well.

98. Accordingly, Petitioner has failed to show that Tateishi anticipates claims 1, 11 and 18 for this reason.

99. With respect to the second requirement, and the limitation reciting that “wherein based on the input voltage and the control signal, the power stage generates the switching signal” (*e.g.*, Limitation 1[E]), Petitioner does not point to the green signal, but points to the orange signal. Specifically, petitioner argues that the orange signal (shown below, and shown as purple in the Petition) is an input into the power stage (highlighted in yellow below). (*See Pet.* at 46).



100. As can be seen from the annotated image of Figure 3 above, the green signal does not control the switches in the alleged power stage (e.g., the yellow highlighted area). As I described above when reciting the different orange and green signal states, the orange signal can be a logic ‘0’ when green can be ‘1’ or ‘0.’ Accordingly, the green signal does not meet the claimed requirement that requires “based on the input voltage and the control signal, the power stage generates the switching signal,” because the orange signal helps control the switches, and the green signal does not control those switches. The green signal can have different logical values even from the orange signal.

101. Accordingly, Petitioner has failed to show that Tateishi anticipates

claims 1 and 18 for this reason.

102. In sum, the two different alleged control signals (*e.g.*, the orange and the green signals) cannot both meet the single claimed “control signal” in my opinion because they have distinct logic states. The orange and green signals do not meet the claimed limitations when viewed together instead of in isolation.

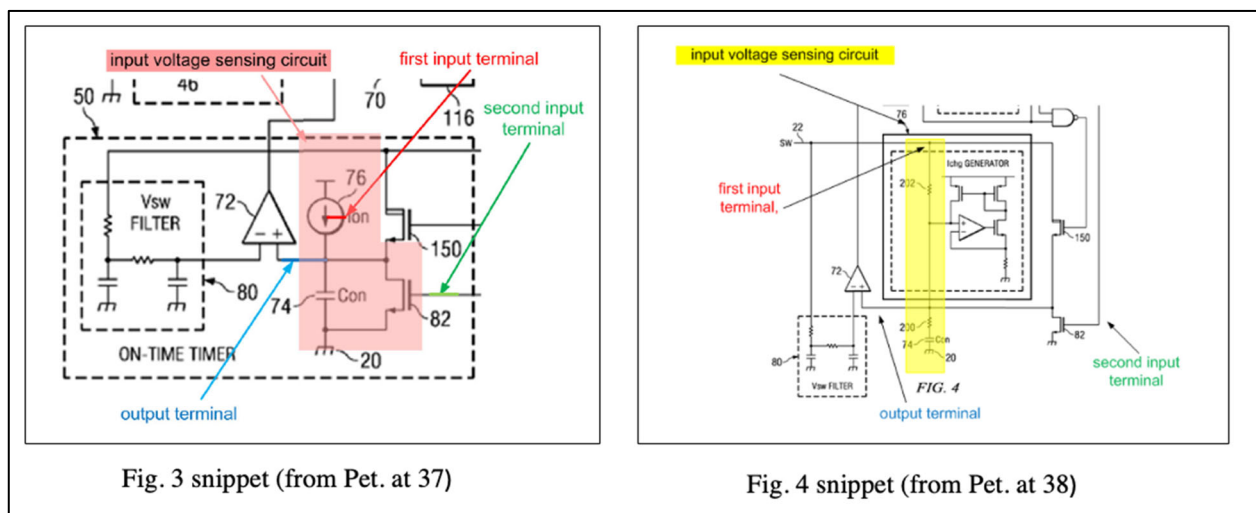
4. Petitioner combines several embodiments to meet its anticipation argument

103. I understand that the limitations of a claim must be literally present in a single reference in order for that reference to anticipate the claim. I also understand that it is not proper in an anticipation theory for a petitioner to modify an alleged prior art reference with a teaching that is not literally present in that reference. To do so would fall under an obviousness theory. Accordingly, it is my opinion that the Petitioner incorrectly combined distinct embodiments in its Ground 1 argument encompassed in just an anticipation theory without showing a teaching literally in *Tateishi* of why a POSITA would be motivated to combine those distinct embodiments.

104. The claims (1, 11, and 18) all require that an on-time generator (or its input voltage sensing circuit) receive a switching signal and a control signal (which is generated via logic control circuitry (or a flip-flop for claim 18)). (EX1001 at 9:40-50, 10:10-13, 11:44-53, 12:8-13, 13:21-25, 14:13-20).

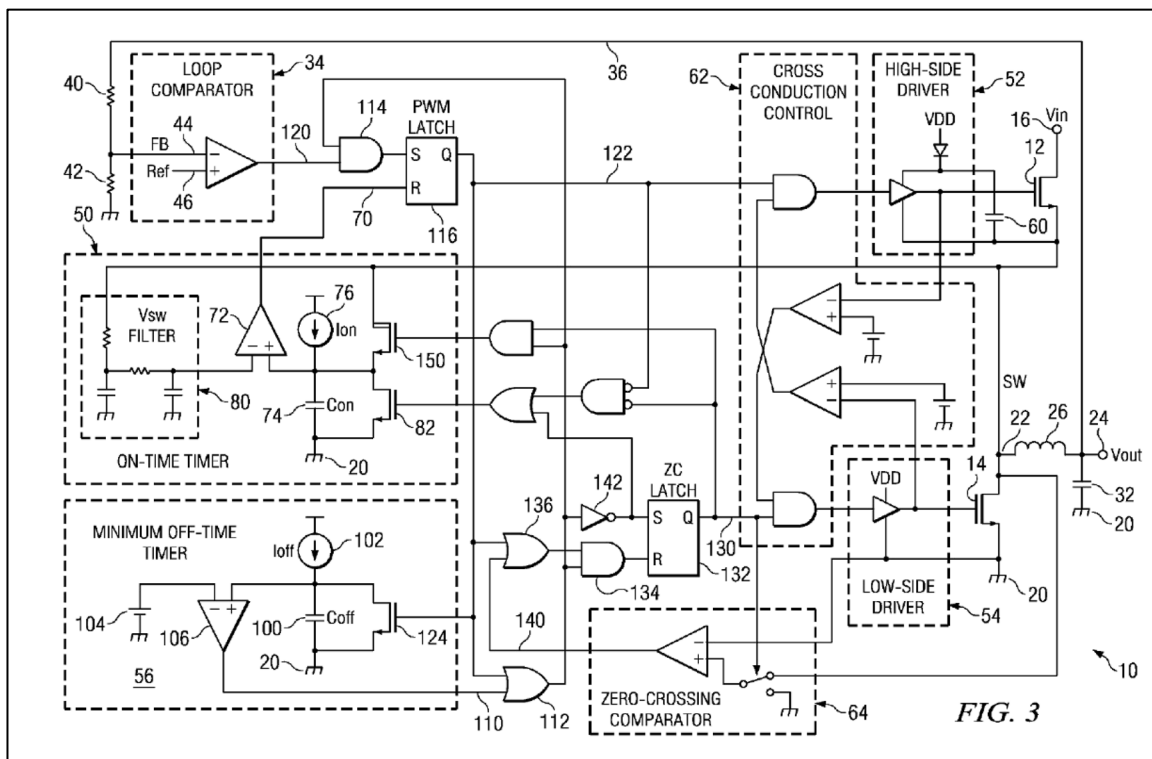
105. To allegedly meet these limitations, Petitioner relies on Figure 3 (below-left) to teach several elements, but this circuit lacks a switching signal provided to the alleged first input terminal of the alleged input voltage sensing circuit, as required by the claims. (Pet. at 37). To try to remedy this, Petitioner takes a generator portion of the Figure 4 embodiment (below-right), that has a switching signal, and applies it to Figure 3's current source. (Pet. at 37–38). Problematically, though, Petitioner ignores that the embodiments of Figure 3 and 4 are different.

106. Petitioner argues that Figure 3's current source 76 could be replaced with the generator portion of Figure 4's circuitry, which receives the switching signal SW, to suggest that Figure 3's current source 76 could receive a switching signal SW. (Pet. at 37-38). This is shown below in the snippets from Petition at 37 and 38 where the Figure 3 snippet is on the left and the Figure 4 snippet is on the right side.

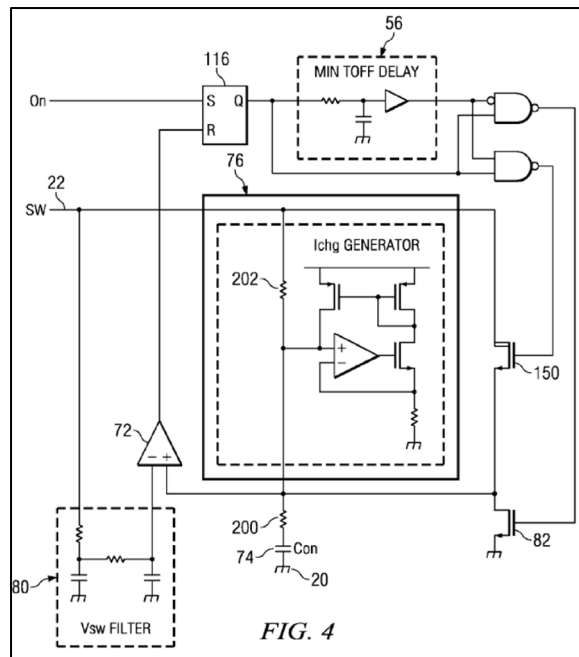


107. Figures 3 and 4 are different embodiments. Tateishi describes Figure 4 as a different converter than that of Figure 3, stating that Figure 4 “depicts an example of various portions of *another* DC to DC buck converter ...” (emphasis added)). (EX1007, ¶ 0013).Ne

108. Additionally, when analyzing both Figure 3 and 4 as a whole, it is clear that these Figures of Tateishi use different logic (and are thus different embodiments) to control the certain switches. For example, Figure 3’s circuit contains logic shown in aqua that control the switches highlighted in yellow.



109. Conversely, Figure 4’s logic (shown in aqua) is different and controls its switches (highlighted in yellow) with different logic from Figure 3.



110. Petitioner and its expert do not explain why a POSITA would be motivated to think of these two different embodiments as a single embodiment. (*See* Pet. at 37-38; EX1003, ¶¶ 84-88).

111. Additionally, Petitioner further modifies Figure 3 with Figure 2 to show that the current source 76 in Figure 3 receives a switching signal if replaced with Figure 2's current source. (Pet. at 38.) Tateishi never states that it can be used in Figure 3's embodiment, stating only that "Fig. 2 depicts a reference current source that may be used in *the DC to DC buck converter of FIG. 1.*" (Tateishi, ¶ 11 (emphasis added)).

112. Accordingly, in my opinion, Petitioner has attempted to make obviousness arguments instead of an anticipation argument (even though it only asserted anticipation) and it did not explain why distinct embodiments could be

treated as a single embodiment.

113. For the foregoing reasons, it is my opinion that the Petitioner has failed to show that Tateishi anticipates the independent claims of the '377 Patent.

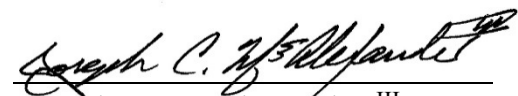
B. Ground 2: Petitioner has failed to show that Tateishi renders obvious dependent claims 5, 7-8, and 15 of the '377 Patent

114. Ground 2 only addresses the dependent claims 5, 7-8, and 15. Nothing in Petitioner's Ground 2 analysis fixes any of the issues I have described above. (*See generally*, Petition at 72-82 (describing only the dependent claims and not addressing the issues with the independent claims)). Accordingly, Ground 2 fails for the same reasons as Ground 1.

VI. CONCLUSION

I hereby declare that all the statements made in this declaration are based on my own true knowledge, that all statements made on information and belief are believed to be true, and that all statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under the penalty of perjury under the laws of the United States that all statements made in this declaration are true and correct.

Dated this 21st day of April, 2025


Joseph C. McAlexander III, P.E.