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# Transcript of Douglas R. Holberg, Ph.D.

**Date:** April 9, 2025

**Case:** Reed Semiconductor Corp. -v- Monolithic Power Systems, Inc. (PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

MPS EX. 2006

UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP., :  
Petitioner, : IPR2024-01158  
v. : Patent 9,041,377 B2  
MONOLITHIC POWER SYSTEMS, :  
INC., :  
Patent Owner. :  
:

Videoconference deposition of DOUGLAS R. HOLBERG, PH.D.  
via Zoom on Wednesday, April 9, 2025  
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Reported by: MARLA SHARP, RPR, CLR, CCRR,  
OR CSR 17-0446, CA CSR 11924, WA CSR 3408

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Videoconference deposition of DOUGLAS R.  
HOLBERG, PH.D., held via Zoom, pursuant to notice,  
before Marla Sharp, a certified stenographic  
reporter licensed in California, Oregon, and  
Washington.

A P P E A R A N C E S

(All parties appeared via videoconference.)

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1                   A P P E A R A N C E S (continued)  
2                   (All parties appeared via videoconference.)  
3  
4  
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1 or, rather, what -- strike that.

2 What is the functionality of the on-time  
3 generator 311 [sic]?

4 MR. DEVKAR: Objection. Form.

5 THE WITNESS: The purpose is to -- when the  
6 high-side switch is turned on, the on-time generator  
7 establishes the time that it remains on.

8 BY MR. BOMBACH:

9 Q And what is the purpose of the logic  
10 control circuit 3013?

11 A Well, the logic -- let me look back and see  
12 what 311 -- so I properly draw all the boxes.

13 Q All right.

14 A So 3011 -- so the logic control circuit  
15 takes input from feedback control circuit, takes  
16 inputs from the on-time control circuit. It  
17 provides outputs to the on-time control circuit.

18 So it's the logic that's managing the  
19 control of the switch mode power supply that's being  
20 described in this patent.

21 Q What is the signal Q on figure 10?

22 A When you say what is it, are you asking

1     what is its function? Or what is its -- well, it's  
2     the output of the logic control circuit, and it's  
3     the input to the power stage.

4             Q     What type of signal is it?

5             MR. DEVKAR: Objection. Form.

6             THE WITNESS: Well, when you say "type," do  
7     you mean is it an analog or a digital signal? Is  
8     there a current or a voltage? I guess it could be  
9     characterized a number of ways.

10            It's a signal that operates within the  
11    bounds of the supply voltages of the chip that  
12    enable it -- so that it's enabled to drive the power  
13    stage properly.

14    BY MR. BOMBACH:

15            Q     Is the signal an analog or a digital  
16    signal? And this is, again, referring to signal Q  
17    of figure 10.

18            MR. DEVKAR: Objection. Form.

19            THE WITNESS: Well, let me see if the '377  
20    characterizes itself what the Q value -- what's the  
21    nature of the Q.

22    ///

1 BY MR. BOMBACH:

2 Q Please take your time to --

3 A Okay.

4 Q -- as much time as you need.

5 A Okay.

6 So the control signal Q, as I stated a  
7 while ago, drives the power stage. And the power  
8 stage -- although I don't recall if Q1 and Q2 of the  
9 power stage are described as MOSFETs, but at -- or  
10 bipolar.

11 But, at any rate, in order to turn on Q1,  
12 for example, the volt -- the Q output has to be  
13 large enough so that it provides enough turn-on for  
14 that output transistor.

15 So, in that sense, you know, you're asking  
16 is it an analog or a digital. Typically, when you  
17 think about a digital signal, it's -- like in a  
18 5-volt system, it's going to be -- the value's going  
19 to be 5 volts or ground.

20 Of -- in this case -- so it has two states.  
21 Digital signals typically have two states, one of  
22 two states.

1           The Q output, in a similar sense, is going  
2   to either be in a -- a value that turns on Q1, which  
3   is -- or it's going to be a value that turns off Q1,  
4   similarly for Q2.

5           And in figure 11, you know, they show a  
6   little bit more detail. And they show the output, Q  
7   driving Q1 and Q bar driving Q2.

8           So both of those signals have to be at  
9   voltage levels sufficient to turn on their  
10   respective devices.

11          Internal to the circuit, the various  
12   components might operate at a lower voltage.  
13   There's no -- digitally at a lower voltage. I don't  
14   recall any guidance in the patent that goes into  
15   that detail.

16         Q     If I understand you correctly, you're  
17   stating that the logic control circuits -- well,  
18   strike that.

19                If I understand you correctly, you're  
20   stating that the signal Q from the logic control  
21   circuit is a two-state signal?

22                MR. DEVKAR: Objection. Form.

1           THE WITNESS: Well, at one point in the  
2 patent, which is column 8, starts in line, like,  
3 27-ish and goes all the way down mostly to the end  
4 of that column.

5           But it says:

6           "The on-time signal S1 resets the  
7 flip-flop 4013 to change the control  
8 signal Q into a logic low (Q=0). Thus,  
9 the high-side switch Q1 is turned off,  
10 and the low-side switch Q2 is turned on,  
11 the switching signal SW equals to 0."

12          And so that's one instance where it's  
13 showing the Q output state with respect to the Q2  
14 switch.

15          Earlier, around line 43 it says:

16          "Figure 12 illustrates the waveforms  
17 of the step-down regulator 40. As shown  
18 in figure 11 and figure 12, when Q=1,  
19 the high-side switch Q1 is turned on."

20          So the patent speaks of it in terms of  
21 logical values 0 and 1. So -- but that doesn't  
22 really represent what the voltage is going into

1 those switches.

2 I believe there's a timing diagram -- yeah.  
3 It's figure 12. And in that, they represent Qs as  
4 just 0s and 1s.

5 I think the -- in reality, it's -- those  
6 are just logical representations of what's driving  
7 the power stage, not representative of the actual  
8 voltages that are driving the transistors.

9 BY MR. BOMBACH:

10 Q Understood. Referring to figure 10 again,  
11 what is the purpose of the power stage 302?

12 MR. DEVKAR: Objection. Form.

13 THE WITNESS: Well, that is the actual  
14 power stage that's driving -- external to the  
15 circuit driving an inductor. So it's providing the  
16 power to the load.

17 BY MR. BOMBACH:

18 Q And then continuing on, what is the purpose  
19 of feedback control circuit 3012?

20 A So that circuit's monitoring a  
21 representative of the output voltage. Maybe it  
22 could be the output voltage, or it could be a

1 divided-down version of the output voltage.

2 And that's -- and it uses that value to  
3 determine whether the output needs to be driven high  
4 or driven low.

5 Q Does the '377 patent describe any  
6 zero-crossing circuitry?

7 MR. DEVKAR: Objection. Form.

8 THE WITNESS: I don't believe so.

9 BY MR. BOMBACH:

10 Q If we could take a look at the claim  
11 language, please.

12 A Okay.

13 Q And I'll focus mostly on claim 1 and 18 in  
14 my discussion, just for a preview. And, again, if  
15 you need any time to review the claim language or  
16 anything in the specification to educate your  
17 answer, please do so.

18 In the claim language, if you could look at  
19 claim 1, 10 8 to 9 -- or, rather, the whole phrase,  
20 10 5 to 9, if you could please look at that and  
21 review it again to yourself and let me know when  
22 you're --

1           A       This was spam. Let me turn my phone off.

2           Q       Yeah, and if that ever happens, please  
3 inform me. I mean no offense to the other attorneys  
4 on the phone. It's just basics.

5           A       Yeah. No, I understand. Okay. I have it  
6 in airplane mode now. Sorry about that.

7           Q       Yeah. In -- I guess more basics that I  
8 didn't go over.

9                   Do you have any messaging or email-type  
10 programs open on your computer? Or is it just  
11 limited to Zoom, the PDFs, and other just random  
12 background apps?

13          A       Yeah. No email. My browser is on, but  
14 it's part of this meeting, and I've got the two Zoom  
15 things, and then my PDF reader.

16          Q       Okay. Do you have any personal notes about  
17 this proceeding with you?

18          A       No, I do not.

19          Q       Do you have any printouts from -- related  
20 to this proceeding with you?

21          A       Yes, I do. I printed -- I didn't know I  
22 was going to get it online, but I printed the two

1 Tateishi, and these are clean copies. And I  
2 printed -- this is the second one. And I printed  
3 the '377. And I printed my declaration. So that's  
4 all I have, yeah.

5 Q Okay. And if it's easier for you to refer  
6 to your printouts as opposed to on the screen,  
7 please do so.

8 A Okay.

9 Q Just whatever's easier for you.

10 A Screen is better, yeah.

11 Q Back to the claim language. 10 5 through 9  
12 states that "the logic control circuit generates a  
13 control signal."

14 You see that?

15 A Yes.

16 Q Do you understand the control signal that  
17 is generated to be a two-state signal?

18 MR. DEVKAR: Objection. Form.

19 THE WITNESS: Yes.

20 BY MR. BOMBACH:

21 Q Okay. And if you could take a second to  
22 review claim 1 in its entirety to yourself and make

1     mental note of the several instances the control  
2     signal is referenced. I believe it's in five  
3     separate instances.

4             A     Okay.

5                     Okay.

6             Q     In your opinion, do all instances of the  
7     language "control signal" in claim 1 refer to the  
8     same signal?

9                     MR. DEVKAR: Objection. Form.

10                    THE WITNESS: Well, let me ponder that.

11                    All right. So the claim introduces the  
12    term "control signal" in line 45. It says "to  
13    receive a control signal."

14                    And then the next time it's referenced, it  
15    is in line 47, "the control signal," which is -- the  
16    antecedent of that is the "a control signal" that  
17    showed up in 45. Therefore, those would be the  
18    same.

19                    "Output voltage" (reading to self).

20                    The next time it shows up, if I'm not  
21    missing something, is line 9 where, again, it's "the  
22    control signal," which references back to "a control

1 signal" in 45 of column 9.

2 And then in line -- column 10, line 12,  
3 again, "the control signal" is mentioned. And it,  
4 again, is the -- hearkens back to the "a control  
5 signal" that first appears in line 45. So they  
6 would all be the same.

7 BY MR. BOMBACH:

8 Q And if you could look at the control signal  
9 with respect to the input-sensing circuit, which I  
10 believe is column 9, 47 -- or, rather, 40 to 50.

11 And my question to you is: How does the  
12 input-sensing circuit generate the input-sensing  
13 signal?

14 MR. DEVKAR: Objection. Form.

15 THE WITNESS: Okay. Let me -- how does it  
16 generate what?

17 BY MR. BOMBACH:

18 Q I'm sorry. Let me --

19 How does the input voltage-sensing circuit  
20 generate the input voltage-sensing signal?

21 A Okay. Well, the claim says:

22 "Based on the switching signal and

1           the control signal, the input voltage  
2           sensing circuit generates an input  
3           voltage sensing signal at the output  
4           terminal."

5           Q     Okay. And I want to look at claim 18 now.  
6     And if you could take a few seconds to just review  
7     it to yourself.

8           A     Okay.

9                 Okay.

10          Q     If you could look at the control signal in  
11     column -- hold on. Let me see -- 14, lines 19 to  
12     20. It says:

13                     "The flip-flop generates the control  
14                     signal."

15          A     Yep, I see that.

16          Q     In your opinion, is the control signal of  
17     claim 18 a two-state signal?

18          A     Yes.

19          Q     And I probably should have asked this to  
20     you before. But if you could look at claim 18 again  
21     and note the instances of "control signal"  
22     referenced throughout the claim.

1 I think I counted, personally, six, but  
2 don't take my word for it. If you could take a few  
3 seconds to look through.

4 A Okay.

5 One, two, three, four, five, six. Yeah, I  
6 found six. I didn't see any more.

7 Q In your opinion, do all instances of the  
8 recited control signal in claim 18 refer to the same  
9 signal?

10 A Yeah. Every instance where it says "the  
11 control signal," it's -- the antecedent for that is  
12 "a control signal" found in line 21, 2, 3, of  
13 column 13.

14 Q Okay. And, Dr. Holberg, I was about to  
15 switch gears to look at the prior art reference. I  
16 know you said you may want breaks.

17 Would you like to take a break now?

18 A I think I'm good. I'm good now. Yeah.

19 Q To take a break --

20 A No. I --

21 Q -- or continue?

22 A No. We can continue.

1 transistor 182, the other input that OR gate comes  
2 from the output of inverter 142. And the input  
3 converter 142, if you go back and look at the  
4 transcript to see how I described all this, is a 1.

5 So the output of inverter 142 is going to  
6 be a 0. And 0 allows whatever the output of the  
7 inverted input AND gate to pass through that OR  
8 gate.

9 So that's how the whole circuit works for  
10 the state you are interested in, the Q output state  
11 being 1.

12 BY MR. BOMBACH:

13 Q Okay. Thank you for your answer. And I  
14 apologize. Let me unpack it a little.

15 A Okay. Hope you were taking notes.

16 Q Oh, yeah. No, I -- we have the real-time  
17 providing us information of your testimony. So I  
18 will review that. Please bear with me for a second.

19 A Okay.

20 Q And if you wanted to take a quick break  
21 while I do that, that's okay.

22 A Okay. That would be a good idea.

1 MR. BOMBACH: Okay. Let's go off the  
2 record.

3 THE WITNESS: Okay.

4 (Recess taken from 10:01 a.m.  
5 to 10:08 a.m.)

6 BY MR. BOMBACH:

7 Q If we could please look at the same signal  
8 in PWM latch 116 signal Q. Previously you described  
9 when it is logic state 1.

10 And I'll ask the same -- a similar question  
11 to you with respect to logic state 0.

12 A Okay.

13 Q What control does signal 122 provide to  
14 switch 82 when it is 0?

15 Rather -- that was a convoluted question.  
16 Let me reask.

17 What control does signal 122 provide to  
18 switch 82 when signal 122 is logic state 0?

19 MR. DEVKAR: Objection. Form.

20 THE WITNESS: Okay. Let me take a moment  
21 to ponder that.

22 So when the signal at the output of the PWM

1 latch 116, the Q output, is 0, then that node 122  
2 and 110 down at the bottom of the diagram, those  
3 inputs go to the OR gate.

4 The output of the OR gate is a 0 as a  
5 result. And then it goes through inverter 142,  
6 which is going to be a logic state output of 1. And  
7 then that 1 will go into that unlabeled OR gate  
8 driving transistor 122, turning it on.

9 BY MR. BOMBACH:

10 Q And I believe you stated -- and, actually,  
11 I will quote -- that "that node 122 and 110 down at  
12 the bottom of the diagram, those inputs go to the OR  
13 gate."

14 And for clarity, I would like you to focus  
15 on figure 3, input 110, which is identified as the  
16 output of minimum off-time timer 106 as opposed to  
17 node 122.

18 Can you please explain why you stated that  
19 122 would go into both inputs of OR gate 112?

20 MR. DEVKAR: Objection. Form.

21 THE WITNESS: No, I don't think I said it  
22 that way.

1           122 doesn't go into both inputs of 112.

2           122 terminal is one of the inputs of 112,  
3 and the other input's 110.

4 BY MR. BOMBACH:

5           Q     Okay.

6           A     Does that clarify that? I don't think I  
7 said it wrong; but if I did, I'm fixing it now. OR  
8 gate 112 has two inputs. One of them is node 110,  
9 and one of them is node 122.

10          Q     Okay. And I guess -- well, let me trace  
11 this down slowly.

12                  When the PWM latch 116 Q output is 0, what  
13 is the logical input to gate 82 of the on-time  
14 timer?

15                  MR. DEVKAR: Objection. Form.

16                  THE WITNESS: Okay. Well, I think I  
17 answered that a while ago, but let me do it again.

18                  The Q output of logic state 0 -- I'll say  
19 it in a simpler way -- passes through OR gate 112 as  
20 a 0, and then is an input to inverter 142 as a 0,  
21 resulting in a logic state output of 142 as a 1.

22                  That 1 then goes into the unlabeled OR gate

1 just above it and to the left generating an output  
2 of 1 on -- of that OR gate, which is the gate of  
3 transistor 82.

4 BY MR. BOMBACH:

5 Q Okay. In your answer, you explain that 122  
6 being 0 would cause the output of OR gate 112 to  
7 likewise be 0.

8 And my question to you is: Can you please  
9 explain what occurs with signal -- the other input  
10 signal 110 --

11 MR. DEVKAR: Objection. Form.

12 BY MR. BOMBACH:

13 Q -- in that case?

14 A Yes, certainly. Well, before Q was a 0, it  
15 was a 1. When it was a 1, it turned on transistor  
16 124, which drives the noninverting input of that  
17 comparator to ground.

18 (Interruption by the stenographer.)

19 THE WITNESS: Noninverting input of  
20 comparator 106 to ground.

21 And it's compared to a voltage identified  
22 as 104. So that comparator's going to drive the

1 output to 0. And that output is 110.

2 BY MR. BOMBACH:

3 Q And what occurs to transistor 124 when its  
4 input is 0?

5 MR. DEVKAR: Objection. Form.

6 THE WITNESS: It's off.

7 BY MR. BOMBACH:

8 Q And what occurs to the output of comparator  
9 106 when 124 is off?

10 A Well, when 124 goes off, that's the  
11 start -- really kind of the start time of the  
12 minimum off-time timer.

13 And the current 102 Ioff is going to charge  
14 up the capacitor. And the output which is being  
15 compared -- the comparator is comparing that -- the  
16 voltage at that node to its inverting input, which  
17 comes from a volt some reference, I guess, of 104.  
18 I don't recall how the patent described it.

19 But the output of the comparator will  
20 remain low until the voltage at the noninverting  
21 input of the comparator goes above the voltage  
22 that's provided by the voltage source 104.

1           At that point 110 will go high, logic state  
2   high.

3           Q     And when logic -- when 110 goes logic state  
4   high, the output of OR gate 112 will likewise go  
5   high, correct?

6           A     That is correct.

7           Q     And, before, you stated -- and I'll switch  
8   gears from -- we'll assume a logic -- well, 110 --  
9   let me scratch that.

10           For the next question, we'll assume logic  
11   110 -- the signal 110 is logic 0 and 122 is logic 0,  
12   as you had stated in a previous answer today.

13           A     Correct.

14           Q     And when that occurs, you stated inverter  
15   142 will be -- will invert that 0 to 1, which will  
16   set the Q output to 1, correct?

17           MR. DEVKAR: Objection. Form.

18           THE WITNESS: That is correct.

19   BY MR. BOMBACH:

20           Q     What occurs when set -- the input to set on  
21   ZC latch 132 is 1 but the input R is set to 1 on  
22   132?

1 MR. DEVKAR: Objection. Form.

2 BY MR. BOMBACH:

3 Q Actually, let me reask that.

4 What occurs to the output Q of ZC latch 132  
5 when set is -- the input S is set at 1 but then R  
6 receives a logic 1?

7 MR. DEVKAR: Objection. Form.

8 THE WITNESS: Well, are you asking me -- in  
9 order for the set input to have a value of 1, which  
10 is the output of inverter 142, the input to inverter  
11 142 has to be a 0. The input to inverter 142 is in  
12 common with one of the inputs to AND gate 134. So  
13 if the input to 142 is 0, then that -- one of the  
14 inputs of 134 is 0, therefore, the reset input of  
15 the ZC latch is a 0.

16 I don't think there's a case where both  
17 inputs can be 1.

18 BY MR. BOMBACH:

19 Q Okay. What is the purpose of zero -- the  
20 zero-crossing circuitry with respect to controlling  
21 on or off time?

22 MR. DEVKAR: Objection. Form.

1     it, you stated signal 122 would be 0; is that  
2     correct?

3           A     Yeah. I mean, that comes from the patent  
4     itself. It says, "The zero-crossing comparator 64  
5     detects the zero crossing and turns off the low side  
6     switch," meaning that it must have been on.

7           Q     Okay. And then, in that case, prior to  
8     zero crossing, signal 130 would be a logic state of  
9     1 while signal 122 is logic state 0; is that right?

10           MR. DEVKAR: Objection. Form.

11           THE WITNESS: Let me go back to the  
12     diagram.

13                   Now I'm looking at the diagram again.  
14     You're saying 130 is a 0 and 122 is a 1? Is that  
15     what you said or --

16     BY MR. BOMBACH:

17           Q     Oh, no, no. Let me reask.

18                   Prior to -- immediately prior to zero  
19     crossing, logic -- signal 130 would be logic state 1  
20     while node 122 would be logic state 0, right?

21           A     Okay. Let me look at that.

22                   All right. Well, I'm not going to answer

1     it that way. I'm going to tell you -- let me just  
2     explain how it works. And you'll just have to bear  
3     with me.

4             So when 122 Q output of PWM latch was a  
5     0 -- was a 1 and it goes to 0, what happens?

6             Okay. Several things happen. Transistor  
7     124 turns off, allowing the current 102 to charge  
8     Coff. And so that's just -- set that aside. If I  
9     were drawing a timing diagram, you'd be able to see  
10    this. But I'm having to do this verbally.

11            So the node -- the noninverting input of  
12    comparator 106 is -- begins to rise in a linear  
13    fashion.

14            So the 0 at the input of 112 from node 122  
15    and the 0 node 110 because the comparator hasn't  
16    switched yet, both of those 0s will result in a 0  
17    output from OR gate 112. Okay.

18            So the -- at this point previously the  
19    output of the ZC latch was a 0, but the output of  
20    the -- and that being a 0, I believe it disables the  
21    zero-crossing comparator so it's not operative at  
22    that point.

1           And then the output 112 VO 1 -- inverter  
2   142 sets the ZC latch to turn the Q output 130 to a  
3   high. That then turns on the low-side transistor.  
4   At the same time, it enables the zero-crossing  
5   comparator.

6           Simultaneously with all this, you've got  
7   this noninverting input at comparator 106 rising.  
8   And at some point that signal 110 will go to a 1  
9   state which will put a 1 input to the 134 AND gate.

10           Now, the -- if -- since the zero-crossing  
11   comparator is operative, if a zero crossing is  
12   detected, then it will generate a 1 at the input of  
13   OR gate 136, and the 1 it input in combination with  
14   the 1 that came out from OR gate 112 will  
15   generate -- it's an AND gate, so it'll generate a 1  
16   at the output of 134.

17           It'll then reset the ZC latch back to 0.  
18   And then when that gets reset, it turns off the  
19   low-side switch.

20           Now, that all happens -- that was initiated  
21   by the Q output of PWM at node 122 going low.

22       Q     Okay. Understood. I have a follow-up

1 question to that.

2 The timing with respect to the  
3 zero-crossing comparator 140 going to logic state 1  
4 and the logic state 1 of signal 110 -- let me reask  
5 and something that --

6 What goes to logic state 1 first? The  
7 signal 140 or the signal 110?

8 MR. DEVKAR: Objection. Form.

9 THE WITNESS: I'm not sure I can know that  
10 without knowing the low condition because zero  
11 crossing is going to be a function of the load.

12 BY MR. BOMBACH:

13 Q Okay. Is it fair to say that sometimes it  
14 would be the other -- rather, sometimes it would be  
15 110, sometimes it would be 140 being the first to go  
16 high dependent upon what the load is?

17 MR. DEVKAR: Objection. Form.

18 THE WITNESS: Or it may never detect a zero  
19 crossing.

20 BY MR. BOMBACH:

21 Q Okay. So I guess -- well, let me -- so it  
22 might be the case that a zero crossing may never be

1 detected in the instance that 122 is 0, which would  
2 result in signal 110 going high prior to signal 140  
3 going high because 140 may never go high?

4 A Yeah. If the zero --

5 Q Is that right?

6 A If the zero crossing is not detected, 110  
7 is going to do -- it's going to time out, according  
8 to the minimum off-time timer. So if the zero  
9 crossing is not detected, then -- obviously, then,  
10 110 is going to change state before it.

11 Q And in that instance, would signal 130 be a  
12 logic state of high because the zero-crossing  
13 comparator 64 is activated?

14 MR. DEVKAR: Objection. Form.

15 THE WITNESS: To drive the zero-crossing  
16 latch, ZC latch, high requires the set input to go  
17 high and -- which requires the input of inverter 142  
18 to go low. And for 142 to go low, both 110 and 122  
19 have to be low.

20 BY MR. BOMBACH:

21 Q And, as I understand it from your  
22 explanation, that occurs when 122, I mean, at