

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,
Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.,
Patent Owner.

Case No. IPR2024-01158

Patent No. 9,041,377

Before KARL D. EASTHOM, KEN B. BARRETT, and LARRY J. HUME,
Administrative Patent Judges.

**PETITIONER'S REPLY TO
PATENT OWNER'S RESPONSE TO PETITION**

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PETITIONER’S EXHIBIT LIST (New Exhibits in *Italics*)

<u>Exhibit</u>	<u>Description</u>
Ex. 1001	U.S. Patent No. 9,041,377 B2 to Wang et al.
Ex. 1002	Prosecution History of U.S. 9,041,377
Ex. 1003	Declaration of Doug Holberg, Ph.D.
Ex. 1004	<i>Curriculum Vitae</i> of Doug Holberg, Ph.D.
Ex. 1005	U.S. Patent No. 8,476,887 B2 to Tateishi et al.
Ex. 1006	Assignment of U.S. Patent No. 9,041,377 from Chengdu Monolithic Power Systems Co., Ltd. to Monolithic Power Systems, Inc.
Ex. 1007	U.S. Patent Publication No. 2009/0140708 A1 to Tateishi et al.
Ex. 1008	U.S. Patent No. 6,147,478 to Skelton et al.
Ex. 1009	Reed Stipulation Regarding Invalidity Contentions (<i>Sotera</i> Stipulation)
Ex. 1010	Nengda Stipulation Regarding Invalidity Contentions (<i>Sotera</i> Stipulation)
Ex. 1011	U.S. Patent No. 7,439,721 B2 to Weng et al.
Ex. 1012	Paul Horowitz and Winfield Hill, “Art of Electronics” (Second Edition) (“AOE”)
Ex. 1013	LM2696 3A, Constant On Time Buck Regulator (annotated)
Ex. 1014	TI Application report: “Adaptive Constant On-Time (D-CAP™) Control Study in Notebook Applications” (“DCAP”)
Ex. 1015	Allen, Philip E., and Douglas R. Holberg. “CMOS Analog Circuit Design” (Second Edition) (“CMOS”)
<i>Ex. 1016</i>	<i>Supplemental Declaration of Doug Holberg, Ph.D.</i>
<i>Ex. 1017</i>	<i>Deposition Transcript of Joseph McAlexander</i>
<i>Ex. 1018</i>	<i>Wiley Electrical and Electronics Engineering Dictionary (2004)</i>

I. Introduction

The Challenged Claims of the '377 Patent¹ are unpatentable for the three reasons that the Board articulated in its Institution Decision.

First, in its Institution Decision, the Board rejected Patent Owner's attempt to limit the term "control signal" to a logic signal with two distinct states. The Board correctly found that such a construction is overly "narrow" and unsupported by the intrinsic record. But Patent Owner continues to propose this same construction, which not only injects overly narrow limitations into the claims, but also reads out the critical "control" function. The Board should maintain its rejection of this construction and adopt Petitioner's proposal, which is consistent with the intrinsic and extrinsic evidence and which Patent Owner's expert agrees is correct. The evidence confirms that the term "control signal" should be construed in accordance with its plain and ordinary meaning as a: "signal configured to control a circuit component."

Second, the Board correctly found in its Institution Decision that the Tateishi² reference discloses a control signal that satisfies the very construction that Petitioner

¹ Claims 1-5, 7, 9-15, 17, and 18 of U.S. Patent No. 9,041,377 (the "'377 Patent").

² U.S. Patent App. Pub. No. 2009/0140708 (Ex. 1007).

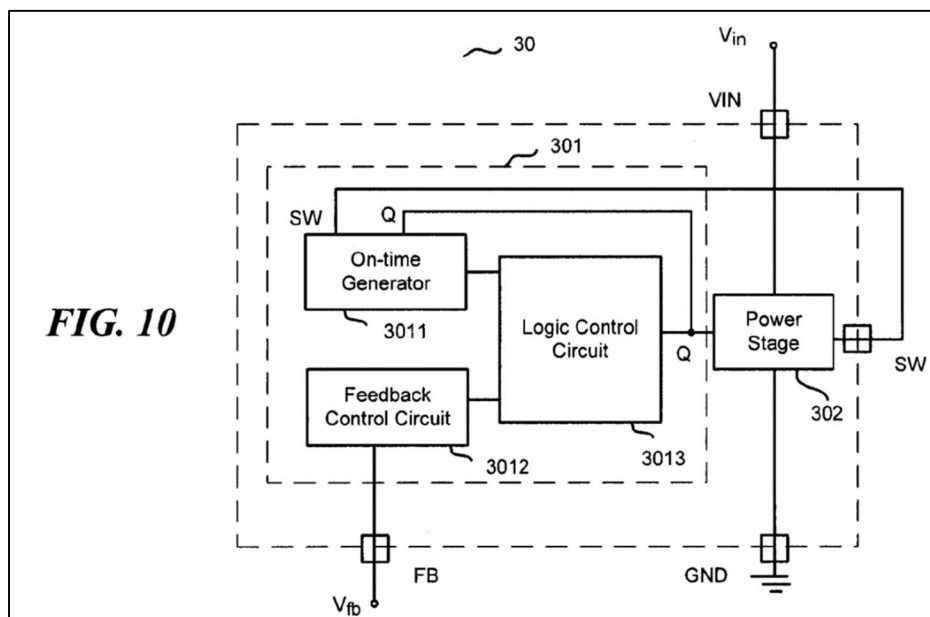
proposes. As the Board held, Tateishi's control signal is configured to control the "input voltage sensing circuit" and "power stage" recited in the claims because the control signal "drives" those components, both directly and indirectly (through logic gates). Patent Owner did not dispute the Board's findings.

Third, in concluding that Tateishi discloses the claimed control signal, both the Board and Petitioner analyzed Tateishi's Figure 1 and Figure 3. But Patent Owner chose not to address Figure 1, and therefore waived any argument that this figure does not disclose the claimed control signal. Instead, Patent Owner chose to focus solely on Figure 3, which Patent Owner argues includes logic gates that change the logical value of the control signal such that the limitation is not met under Patent Owner's (incorrect) construction. However, Figure 1 does not include these logic gates and discloses the claimed control signal without any of the alleged issues about which Patent Owner complains. Thus, it is undisputed that Tateishi's Figure 1 discloses the claimed control signal. In any event, Tateishi's Figure 3 also discloses the claimed control signal because the logic gates at issue do not change the signal's ability to perform its essential control function. The Challenged Claims are unpatentable.

II. Background

A. Relevant Overview of the '377 Patent

The '377 Patent is generally directed to switch-mode DC-DC (“direct current”) voltage converters that have pseudo constant-on-time (“PCOT”) control circuits for controlling a series of “high-side” and “low-side” switches. Pet. at 24 (citing Ex. 1001 at 4:42-45, 8:32-34, FIG. 11; Ex. 1003 at ¶ 66). To carry out this control functionality, the '377 Patent describes several embodiments in which a control signal “Q” is used to control the generation of a “switching signal” in the switches. For example, Figure 10 (below) illustrates PCOT control circuit 301 that provides control signal Q to power stage 302. Ex. 1001 at 8:4-8. Based on control signal “Q” and input voltage “ V_{in} ,” the power stage generates a switching signal “SW” that is fed back to on-time generator 3011. *Id.*



The claims of the '377 Patent capture similar control functionality. For example, limitations 1[B2] and 1[E] recite:

- Limitation 1[B2]: “a control signal provided by the pseudo constant on time control circuit, and wherein *based on* the switching signal and *the control signal, the input voltage sensing circuit generates an input voltage sensing signal* at the output terminal;” and
- Limitation 1[E]: “a power stage configured to receive an input voltage and the control signal, wherein *based on* the input voltage and *the control signal, the power stage generates the switching signal.*”

Ex. 1001 (emphasis added). These limitations require that the control signal be configured to control: (i) the input voltage sensing circuit to “generate[] an input voltage sensing signal at the output terminal;” and (ii) the power stage to “generate[] the switching signal.”

B. The Institution Decision and Patent Owner's Response

The Board instituted *inter partes* review of claims 1-5, 7-15, 17, and 18 of the '377 Patent as to all grounds of unpatentability set forth in the Petition. Paper 6 (Jan. 27, 2025) at 43. Ground 1 asserts that Tateishi anticipates claims 1-4, 9-14, 17, and 18 under pre-AIA 35 U.S.C. §§ 102(b) and 102(e). *See id.* at 9. Ground 2 asserts that Tateishi renders obvious claims 5, 7, 8, and 15 under pre-AIA 35 U.S.C. § 103. *See id.* In its Patent Owner's Response (“POR”), Patent Owner does not raise any

independent arguments directed to Ground 2, so the disputes are focused solely on Ground 1. *See* POR at 41.

Specifically, Patent Owner disputes: (i) how the term “control signal” should be construed; and (ii) how any such construction should be applied to Tateishi. As such, the Board asked the parties to brief the meaning of “control signal”:

To establish a clear record, the parties should discuss the meaning of “control signal” in further briefing authorized in the Scheduling Order, and should focus primarily on intrinsic evidence. If either party contends that the term should have its plain and ordinary meaning, the party shall clearly indicate what it contends is that plain and ordinary meaning.

Paper 6 (Jan. 27, 2025) at 17 (citing *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008)).

In its Institution Decision, the Board correctly rejected Patent Owner’s overly “narrow” construction of “control signal,” holding:

we decline to read the word “logical” into the term “control signal,” we do not construe the claim term as excluding logic gates between the logic control circuit output and the second input terminal of the input voltage sensing circuit, and we do not construe the claims such that the “control signal” must be the exclusively controlling factor of a component.

Paper 6 (Jan. 27, 2025) at 15, 17. But Patent Owner now proposes the same construction—"logic signal with two distinct states"—that the Board correctly declined at institution. POR at 7. As shown below, Patent Owner's construction improperly: (i) reads the word "logic" into the term; and (ii) excludes intervening logic gates along the path of the control signal. The Board should again reject Patent Owner's improper construction, and adopt Petitioner's proposal, which is supported by the intrinsic and extrinsic evidence.

III. Construction of the Term "Control Signal"

A. The Term "Control Signal" Should be Construed in Accordance With its Plain and Ordinary Meaning as a "Signal Configured to Control a Circuit Component"

The term "control signal" should be construed in accordance with its plain and ordinary meaning as a "signal configured to control a circuit component" because this construction is consistent with the intrinsic and extrinsic evidence. Indeed, Patent Owner's expert agrees that this construction is correct. *See* Ex. 1017 (McAlexander Dep. Tr.) at 121:1-4 ("Q. [I]n the context of the '377 patent, you would agree that a control signal is a signal that controls other circuit components, correct? A. I would agree with that, yes.").

First, the claim language supports Petitioner's construction. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 8 Independent claim 1 of the '377 Patent recites,³ *inter alia*:

- Limitation 1[B2]: “an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive *a control signal* provided by the pseudo constant on time control circuit, and wherein based on the switching signal and *the control signal*, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;”
- Limitation 1[D]: “a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the output signal, the logic control circuit generates *the control signal*;” and
- Limitation 1[E]: “a power stage configured to receive an input voltage and *the control signal*, wherein based on the input voltage and *the control signal*, the power stage generates the switching signal.”

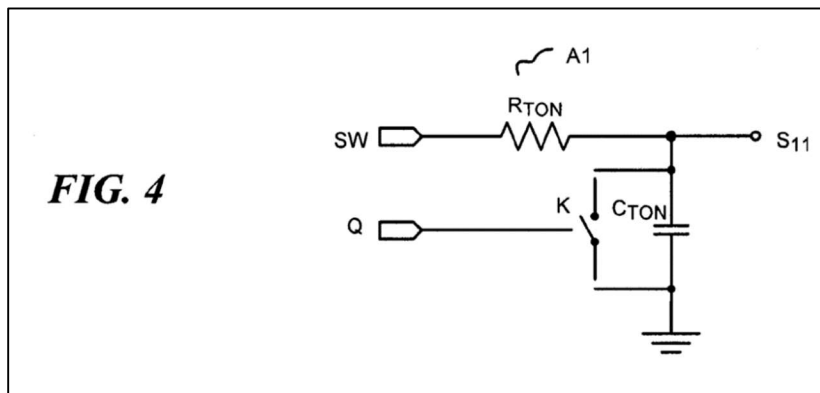
³ Independent claims 11 and 18 recite similar limitations. *See* Pet. at Claim App'x (limitations 11[B1], 11[D], 18[A], 18[E], 18[F]).

Ex. 1001 (emphasis added).

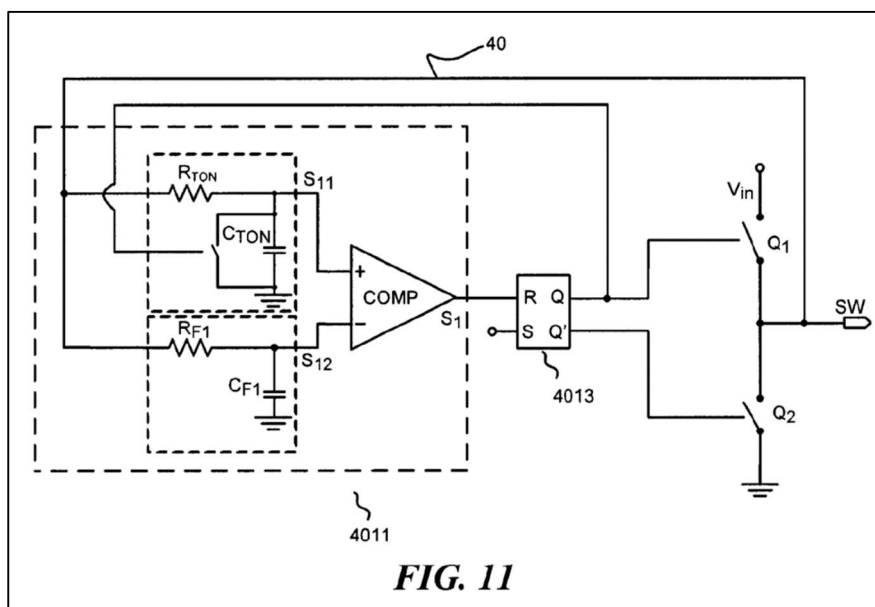
Independent claim 1 recites a “control signal” that serves several claimed functions, including: (i) “based on the switching signal and the control signal, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;” and (ii) “based on the input voltage and the control signal, the power stage generates the switching signal.” The parties agree that in these limitations, the control signal is configured to *control* the “input voltage sensing circuit” and “power stage” because their respective outputs are “based on” the control signal. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 8; Ex. 1017 (McAlexander Dep. Tr.) at 119:14-16; *see also id.* at 121:1-4. A person of ordinary skill in the art (“POSITA”) would have therefore understood that the plain and ordinary meaning of the term “control signal” must include a control function. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 8. In fact, as the Board held in its Institution Decision, Patent Owner has conceded as much. *See* Paper 6 (Jan. 27, 2025) at 14 (“Patent Owner asserts that the recited ‘control signal’ is ‘a single signal that goes from one control element as control for another.’”) (quoting Patent Owner’s Preliminary Response at 1).

Second, the specification further supports Petitioner’s construction. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶¶ 9-11. For example, in its description of Figure 4 (below), the specification teaches that “[t]he switch K is coupled to the capacitor

C_{TON} in parallel and *controlled by the control signal Q .*” Ex. 1001 at 5:21-23 (emphasis added).



As another example, in its description of Figure 11 (below), the specification teaches that “[t]he control signal Q controls the high-side switch Q_1 , and the complementary signal Q' of the control signal Q controls the low-side switch Q_2 .” *Id.* at 8:32-34 (emphasis added).



Thus, the parties agree that, with this language, the specification teaches that the control signal described in the '377 Patent is configured to “control” various components of the disclosed circuits, consistent with Petitioner's construction. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 11; Ex. 1017 (McAlexander Dep. Tr.) at 119:17-120:22.

Third, extrinsic evidence further supports Petitioner's construction. Ex. 1016 (Holberg Suppl. Decl.) at ¶ 13. For example, the Wiley Electrical and Electronics Engineering Dictionary (2004) defines the term “control signal” as “[a] signal utilized to control a device or process.” Ex. 1018. Like the claim language and specification, this definition also recites a control function and supports Petitioner's construction. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1322-23 (Fed. Cir. 2005) (finding it proper to “rely on dictionary definitions when construing claim terms, so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents”) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584 n. 6 (Fed. Cir. 1996)).

Accordingly, the term “control signal” should be construed in accordance with its plain and ordinary meaning as a: “signal configured to control a circuit component.”

B. Patent Owner's Construction of "Control Signal" as a "Logic Signal With Two Distinct States" is Inconsistent with the Teachings of the Specification and One of the Key Aspects of the Claimed Inventions

Patent Owner's construction of "control signal" as a "logic signal with two distinct states" should be rejected for several reasons.

First, Patent Owner's construction *reads out "control"* from the claims. A key aspect of this patent is to "control" the high-side and low-side switches—and this is the signal that serves that purpose. Indeed, as explained above, the intrinsic and extrinsic evidence establishes that the claimed "control signal" needs to include a control function. But Patent Owner's construction would eviscerate that function from the claims. This runs counter to well-settled claim construction precedent and should be rejected. *See, e.g., Snap-on Inc. v. Milwaukee Elec. Tool Corp.*, 722 Fed. App'x 1041, 1043 (Fed. Cir. 2018) (rejecting Board's construction because it read a term out of the claim).

Second, in addition to reading out limitations from the claims, Patent Owner's construction adds limitations that are not required. Specifically, Patent Owner has repeatedly described its construction as requiring a signal that: (i) must not pass through any logic gates from the point of transmission to the point of ultimate

receipt, and (ii) as a result, must always remain in the same logic state of 0 or 1.⁴ *See* Paper 6 (Jan. 27, 2025) at 15 (“According to Patent Owner, “the alleged ‘control signal’ is *logically processed* with other signals from other logic blocks.”) Paper 6 (Jan. 27, 2025) at 15 (quoting Patent Owner’s Preliminary Response at 17-18) (emphasis in Institution Decision); POR at 24-25 (“Petitioner still fails to provide any explanation regarding why these two signals can both—*at the same time*—be the same ‘control signal.’”) (emphasis added).

But the Board correctly rejected this overly “narrow” construction in its Institution Decision:

we decline to read the word “logical” into the term “control signal,” we do not construe the claim term as excluding logic gates between the logic control circuit output and the second input terminal of the input voltage sensing circuit, and we do not construe the claims such that the “control signal” must be the exclusively controlling factor of a component.

⁴ To the extent that this is an attempt to rewrite the claims to preserve their validity over Tateishi, this is improper and must be rejected. *See Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1349 (Fed. Cir. 2002) (“It is not our function to rewrite claims to preserve their validity.”).

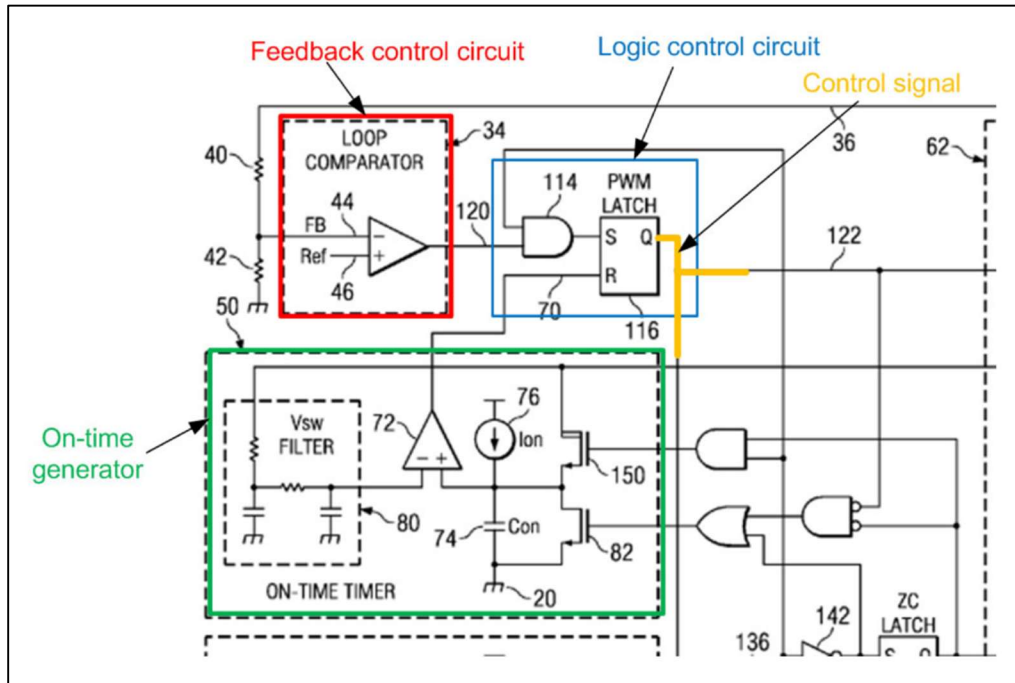
Paper 6 (Jan. 27, 2025) at 15, 17. The Board's conclusion was correct because the intrinsic and extrinsic evidence described above does not permit these overly narrow limitations to be imported into the claims.

Accordingly, Patent Owner's construction should be rejected.

IV. Under a Proper Construction of the Term “Control Signal,” Tateishi Discloses the Limitation and Anticipates Claims 1-4, 9-14, 17, and 18 of the '377 Patent (Ground 1)

To satisfy the “control signal” limitation under its proper construction, a signal must be configured to control a circuit component. The control signal may be impacted by other functionality of the circuit in performing its primary function of controlling the high-side and low-side switches. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 16. The control signal may pass through intervening logic gates and/or may change logical values along its path (*i.e.*, from 0 to 1, from 1 to 0). *See id.* Fundamentally, however, if the control function is present, and meets the other requirements recited in the claims, then the signal constitutes a “control signal.” *See id.*

Tateishi's control signal 122 is configured to control the “input voltage sensing circuit” and “power stage” recited in the claims. *See* Pet. at 36-39, 45-47. In its Institution Decision, the Board analyzed the functionality of Tateishi's control signal 122, shown below in yellow from Figure 3 of the reference:



Paper 6 (Jan. 27, 2025) at 34 (citing Pet. at 45).

The Board correctly found that, as explained in the Petition, control signal 122 “control[s]” or “drive[s]” transistor 82:

Tateishi ... speaks of output 122 at the Q terminal of SR latch 116 as **controlling** switch 82 as well as other components without regard to whether the circuit includes logical operators between the two terminals.

...

Tateishi's disclosure is more consistent with Petitioner's position that “Tateishi discloses the on-time timer 50 comprising a capacitor Con 74 [and] a discharging transistor 82 **driven by** the control signal 122,” and

with the capacitor's voltage being mapped to the recited "input voltage sensing signal.

Paper 6 (Jan. 27, 2025) at 27-29 (bold, underlining added; italics in Institution Decision) (quoting Pet. at 37, 39). This conclusion is consistent with Tateishi's description of control signal 122, which teaches:

The output 122 also drives the discharging transistor 82 in the on-time timer 50 through an inverter 126 so that during an off-time, the capacitor Con 74 is discharged to ground 20 and during an on-time, the discharging transistor 82 is turned off allowing the capacitor Con 74 to be charged by the current source 76.

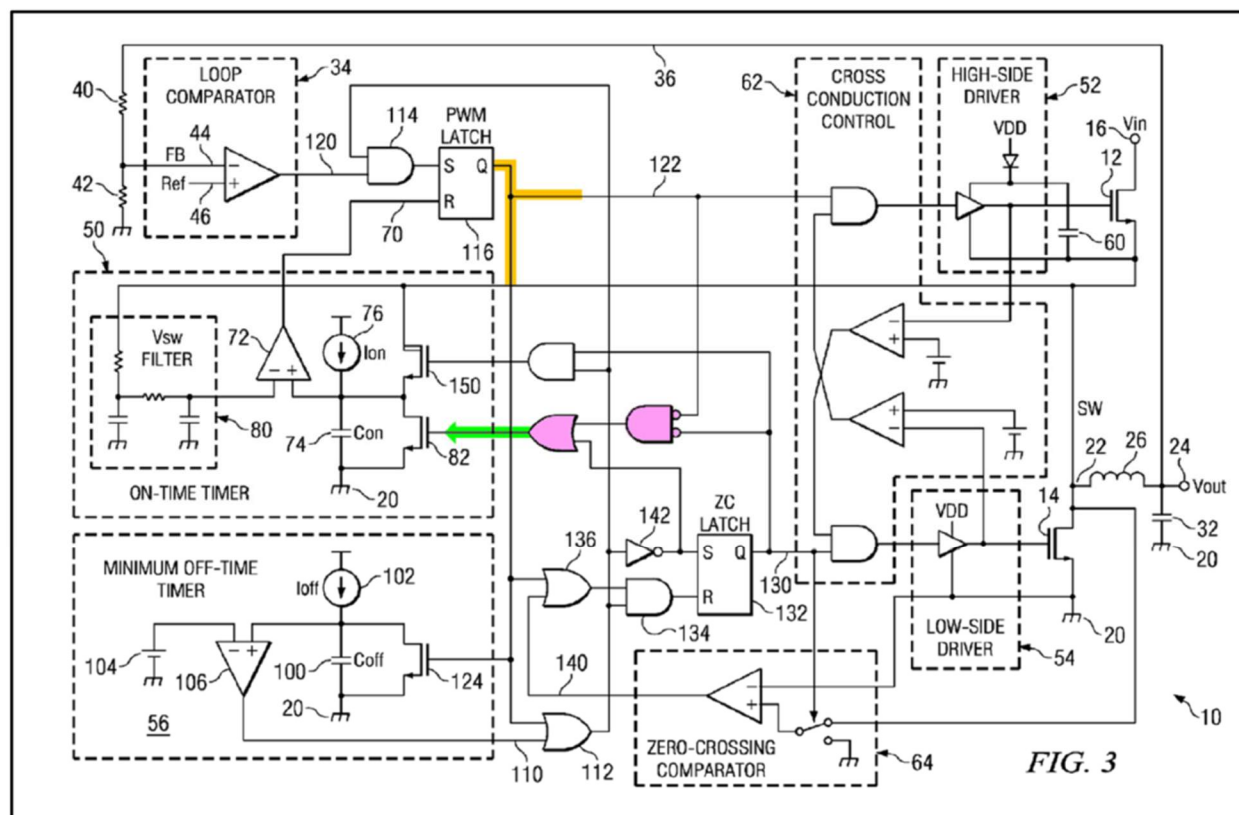
Ex. 1007 at ¶ 51 (emphasis added). Tateishi's signal 122 is a "control signal" because it carries out a control function in the circuit components to which it is transmitted. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶¶ 24-31.

Importantly, as emphasized above, the Board correctly found that the control signal carries out this control function "without regard to whether the circuit includes logical operators between the two terminals," contrary to Patent Owner's argument. Paper 6 (Jan. 27, 2025) at 28-29. In fact, the above-quoted passage from Tateishi confirms that the control function is present in the signal notwithstanding that it passes "through an inverter 126," which is a type of logic gate that inverts the logical value of a signal. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 19; Ex. 1017

(McAlexander Dep. Tr.) at 50:13-22. Indeed, the '377 Patent itself teaches an embodiment in which the control signal passes through an inverter, which is consistent with Tateishi's teachings. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶¶ 15-23. Thus, Tateishi discloses the claimed control signal even under Patent Owner's flawed construction that the control signal excludes logic gates along its path.

Patent Owner raises two overarching arguments in response to the Board's and Petitioner's analyses of Tateishi's Figure 3. For the following reasons, these arguments fail.

First, Patent Owner argues that Tateishi's Figure 3 fails to disclose the claimed control signal because the value of control signal 122 changes after passing through two logic gates (highlighted in pink below), thereby creating "contradictory logic states at the same time." POR at 7. This argument fails because it is premised on Patent Owner's incorrect claim construction as explained above, and further fails for the reasons set forth below.



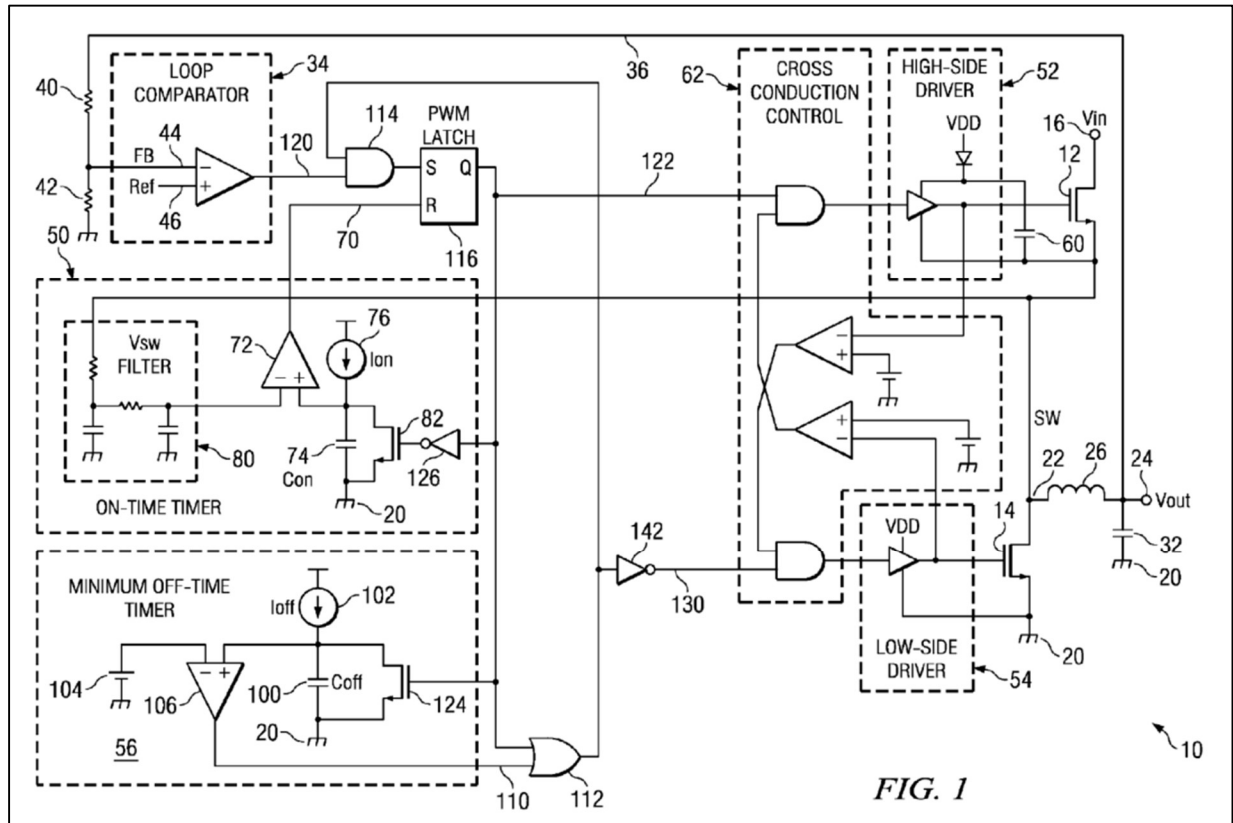
POR at 22-23.

Figure 1 of Tateishi does not include the logic gates that Patent Owner highlights in Figure 3 above. Figure 1, therefore, overcomes Patent Owner’s argument. Both the Petition and the Institution Decision repeatedly cite *both* Tateishi’s Figure 1 *and* Figure 3 throughout the claim 1 analysis. *See* Paper 6 (Jan. 27, 2025) at 19-21, 27-29; Pet. at 33, 39, 41, 43, 44, 46, 47.⁵ But Patent Owner chose

⁵ As the Board held in its Institution Decision, the Petition properly considered Tateishi’s Figures 1 and 3 together in its anticipation analysis because “the Figure 3

not to address Figure 1 in its Patent Owner's Response, and therefore, waived any argument that Figure 1 fails to anticipate or render obvious the Challenged Claims. *See, e.g.*, Paper 7 (Scheduling Order) (Jan. 27, 2025) at 9 ("Patent Owner is cautioned that any arguments not raised in the response may be deemed waived."); *In re NuVasive*, 842 F.3d 1376, 1380-81 (Fed. Cir. 2016) (upholding PTAB's finding that patent owner waived argument because it was not included in Patent Owner's Response); *Google LLC v. Uniloc 2017 LLC*, IPR2020-00447, Paper 24 at 9-10 n.6 (P.T.A.B. May 11, 2021) (same).

embodiment uses many of the same element numbers and "[t]he DC to DC buck converter 10 of FIG. 3 operates in much the same manner as that of FIG. 1." Paper 6 (Jan. 27, 2025) at 19 n.7 (quoting Ex. 1007 at ¶ 58); *see Microsoft Corp. v. Biscotti, Inc.*, 878 F.3d 1052, 1069-70 (Fed. Cir. 2017) ("[T]he Board did not err in considering the combination of Figures 2 and 4 of [the prior art patent reference], because the reference expressly described the components shown in those figures as part of a single embodiment. ... Therefore, the Board was permitted to consider Figures 2 and 4 together when analyzing whether [the reference] anticipated the asserted claims.").



Notwithstanding Patent Owner's choice not to address Tateishi's Figure 1, Patent Owner's analysis of Tateishi's Figure 3 is flawed because the intervening logic gates (pink above) do not interfere with the control signal's ability to perform its essential functions of controlling the high-side and low-side switches. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶¶ 24-31; Pet. at 36-39, 45-47. In support of its flawed analysis of Figure 3, Patent Owner includes a truth table that purports to list out the changing logical values of the control signal along its path. *See* POR at 27-28. However, none of these changes impact the signal's fundamental purpose and

ability to control other circuit components. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 16.

In any event, Patent Owner's truth table is incomplete. *See id.* at ¶¶ 32-39. In his declaration, Petitioner's expert Dr. Holberg includes a timing diagram that traces out the logical values of the control signal as it passes through various components in Tateishi's Figure 3. *See id.* at ¶ 34. Dr. Holberg concludes that four out of the six rows in Patent Owner's truth table are incorrect. *See id.* at ¶¶ 35-38. Thus, even if the changing logical values had any impact on the control signal's control functionality (they do not), Patent Owner's argument should be dismissed because it is incomplete.

Patent Owner's analysis of Tateishi's Figure 3 is further flawed because it fails to account for express teachings in the reference showing that control signal 122 does not necessarily change logical states in every situation. Tateishi teaches that "the DC to DC buck converter 10 of FIG. 3 operates in much the same manner as that of FIG. 1" when the output of element 64 in Figure 3 is 0. Ex. 1007 at ¶ 59. When this happens, control signal 122 acts as a "pass-through," such that the signal value has the same logical state along its path because the logic gates do not change the signal's beginning value. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 28; *see also* Pet. at 35 (Petition showing this pass-through scenario in green annotations).

Second, Patent Owner argues that the Petition improperly combines Tateishi's Figure 3 with Figures 2 and 4 in an anticipation ground because the Petition cites element 76 from each of the three figures. *See* POR at 34-41. Petitioner's citations to element 76 in Figures 2 and 4 are not an improper obviousness combination because all three figures refer to the same element—the “current source”—and all use the same reference numeral “76” to refer to this element. *See Ex parte Grabelsky*, Appeal No. 2012-004212, 2015 WL 252852, at *2-3 (P.T.A.B. Jan. 16, 2015) (“U.S. patent application disclosures apply identical reference characters to only an invention's ‘same’ features.”) (quoting 37 C.F.R. 1.84(p)(4)); Ex. 1016 (Holberg Suppl. Decl.) at ¶ 40.

Figure 3 illustrates current source 76 using the generic symbol for an “ideal current source,” while Figures 2 and 4 each show the detailed circuitry inside of current source 76. *See* Ex. 1016 (Holberg Suppl. Decl.) at ¶ 40. Notwithstanding these differing levels of detail, current source 76 refers to the same element in all three figures, as evidenced by the fact that the inventor used the same reference numeral in all three figures. *See Ex parte Grabelsky*, 2015 WL 252852, at *2-3. Thus, the Petition properly cited element 76 from each of the three figures in its anticipation ground. *See Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1236 (Fed. Cir. 2011) (finding claim anticipated by disclosures “distributed throughout”

a single reference and noting that anticipation does not require all elements to appear in a single figure or paragraph if the reference “sufficiently describes and enables the claimed invention”); *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1334-35 (Fed. Cir. 2008) (“Nothing in the law requires anticipation to be found in a single paragraph or figure, so long as the disclosure is within the four corners of the reference.”); *id.* at 1338 (finding anticipation based on disclosures in separate passages in a prior art reference because “one of ordinary skill in the art would read [the passages] in concert” such that “[the] passages refer to the same subject matter”).

Accordingly, Tateishi anticipates claims 1-4, 9-14, 17, and 18 of the '377 Patent under pre-AIA 35 U.S.C. §§ 102(b) and 102(e).

V. Tateishi Renders Claims 5, 7, 8, and 15 Obvious (Ground 2)

Patent Owner concedes that it does not raise any independent arguments directed to Ground 2. *See* POR at 41. For the reasons explained in the Petition, dependent claims 5, 7, 8, and 15 are unpatentable as obvious under pre-AIA 35 U.S.C. § 103.

VI. Conclusion

For the reasons explained above, and in the Petition, the Challenged Claims are unpatentable.

Dated: July 14, 2025

Respectfully Submitted,

/Andrew J. Gray IV/
Andrew J. Gray, IV (Reg. No. 41,796)
Lead Counsel for Petitioner
Reed Semiconductor Corp.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and in reliance on the word count provided by the word-processing system used to prepare this **PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE TO PETITION**, that the number of words in this paper is 4,123. Pursuant to 37 C.F.R. § 42.24(c)(1), this word count excludes the table of contents, table of authorities, certificate of service, certificate of word count, and appendix of exhibits.

Dated: July 14, 2025

Respectfully Submitted,

/Andrew J. Gray IV/
Andrew J. Gray, IV (Reg. No. 41,796)
Lead Counsel for Petitioner
Reed Semiconductor Corp.

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that a complete and entire copy of **PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE TO PETITION** was served on July 14, 2025 via email on Patent Owner's counsel of record in this proceeding:

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