

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

Petitioner,

v.

MONOLITHIC POWER SYSTEMS.

Patent Owner.

Case No. IPR2024-01158

Patent No. 9,041,377

**SUPPLEMENTAL DECLARATION OF DOUGLAS HOLBERG, PH.D. IN
SUPPORT OF PETITIONER'S REPLY TO PATENT OWNER'S
RESPONSE**

TABLE OF CONTENTS

I. INTRODUCTION.....	3
II. QUALIFICATIONS AND BACKGROUND	3
III. MATERIALS REVIEWED AND CONSIDERED IN FORMING MY OPINIONS	3
IV. LEGAL PRINCIPLES	4
V. OPINIONS IN SUPPORT OF PETITIONER’S REPLY TO PATENT OWNER’S RESPONSE.....	5
A. The term “control signal” should be construed in accordance with its plain and ordinary meaning as a “signal configured to control a circuit component”	5
B. The “control signal” of the ’377 Patent is configured to control switch “K” through an inverter	8
C. Tateishi’s Figures 1 and 3 both disclose the claimed “control signal”	11
D. Mr. McAlexander’s truth table analysis is incomplete	16
E. Current source 76 is the same element in each of Tateishi’s Figures 2, 3, and 4	20
VI. CONCLUSION	21

I. INTRODUCTION

1. I, Douglas Holberg, have been engaged by Petitioner Reed Semiconductor Corp. to opine on the patentability of U.S. Patent No. 9,041,377 (the '377 Patent), titled PSEUDO CONSTANT ON TIME CONTROL CIRCUIT AND STEPDOWN REGULATOR. In this declaration, I provide my opinions relating to Patent Owner's Response to the Petition for *Inter Partes* Review of the '377 Patent ("Response"), the opinions of Patent Owner's expert Mr. Joseph McAlexander, and the Board's Institution Decision.

II. QUALIFICATIONS AND BACKGROUND

2. I have provided my qualifications, prior testimony, and background information in my *curriculum vitae* (Ex. 1004) and in paragraphs 2-12 of my earlier declaration (Ex. 1003).

3. I am being compensated by Petitioner at my standard hourly consulting rate for my time spent on this matter. My compensation is not contingent on the outcome of the IPR or on the substance of my opinions. I have no financial interest in Petitioner.

III. MATERIALS REVIEWED AND CONSIDERED IN FORMING MY OPINIONS

4. In forming my opinions, I have reviewed and considered the following materials:

- Petition for *Inter Partes* Review (Paper 1);

- Patent Owner's Preliminary Response (Paper 5);
- Institution Decision (Paper 6);
- Petitioner's Exhibits 1001-1018; and
- Patent Owner's Exhibits 2001-2006.

5. My opinions are also based on my years of education, consulting experience, research, and teaching experience. My analysis is ongoing, and I will continue to review any new materials as they become available. This supplemental declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and based on my continuing analysis of relevant materials.

IV. LEGAL PRINCIPLES

6. For my opinions in this declaration, I understand that it requires applying various legal principles. As I am not an attorney, I have been informed about various legal principles that govern my analysis. I have used my understanding of those principles in forming my opinions. My understanding is set forth in paragraphs 15-40 of my earlier declaration (Ex. 1003).

V. OPINIONS IN SUPPORT OF PETITIONER’S REPLY TO PATENT OWNER’S RESPONSE

A. The term “control signal” should be construed in accordance with its plain and ordinary meaning as a “signal configured to control a circuit component”

7. For the following reasons, it is my opinion that the term “control signal” should be construed in accordance with its plain and ordinary meaning as a “signal configured to control a circuit component,” as Petitioner proposes.

8. The claim language supports Petitioner’s proposed construction. Independent claim 1 of the ’377 Patent recites in part:¹

- Limitation 1[B2]: “an input voltage sensing circuit having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal is configured to receive a switching signal provided by the step-down regulator, the second input terminal is configured to receive *a control signal* provided by the pseudo constant on time control circuit, and wherein based on the switching signal and *the control signal*, the input voltage sensing circuit generates an input voltage sensing signal at the output terminal;”
- Limitation 1[D]: “a logic control circuit coupled to the on-time generator and the feedback control circuit to receive the on-time signal and the output signal, wherein based on the on-time signal and the

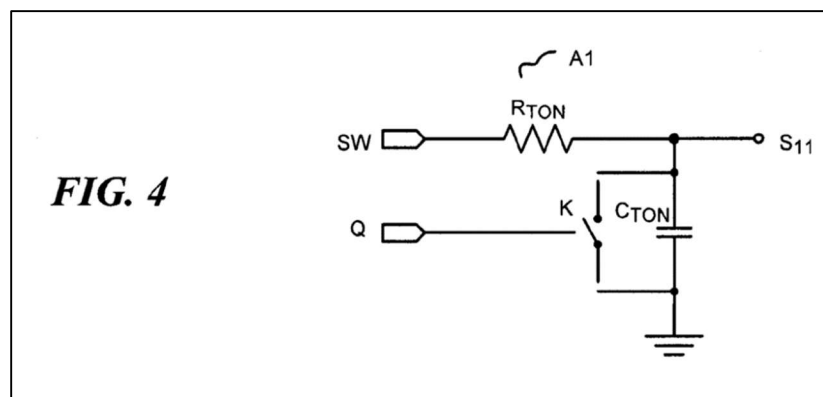
¹ Independent claims 11 and 18 recite similar limitations. See Pet. at Claim App’x (limitations 11[B1], 11[D], 18[A], 18[E], 18[F]).

output signal, the logic control circuit generates *the control signal*;
and

- Limitation 1[E]: “a power stage configured to receive an input voltage and *the control signal*, wherein based on the input voltage and *the control signal*, the power stage generates the switching signal.”

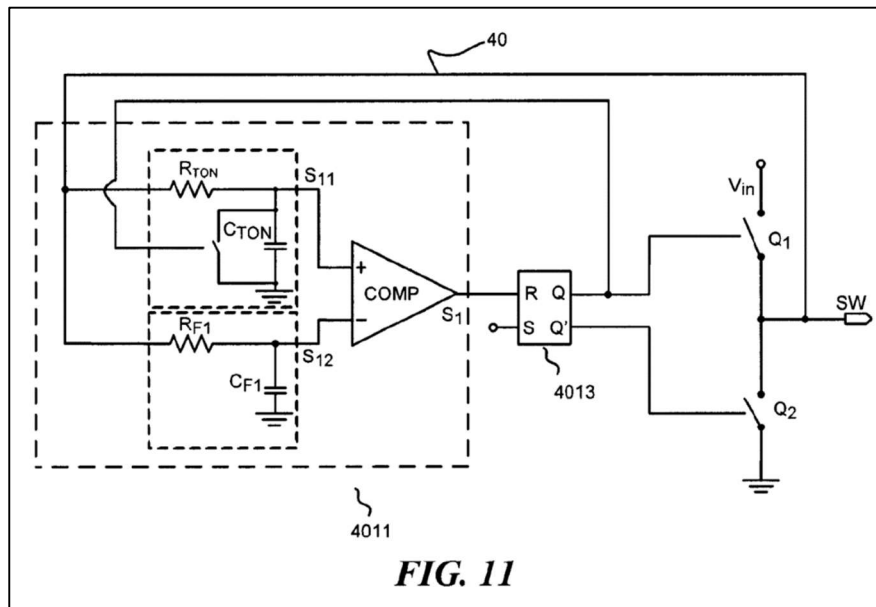
Ex. 1001 (emphasis added). In these limitations, the control signal is configured to control the “input voltage sensing circuit” and “power stage” because their respective outputs are “based on” the control signal.

9. The specification further supports Petitioner’s proposed construction. For example, in its description of Figure 4 (below), the specification teaches that “[t]he switch K is coupled to the capacitor C_{TON} in parallel and *controlled by the control signal Q*.” Ex. 1001 at 5:21-23 (emphasis added).



10. As another example, in its description of Figure 11 (below), the specification teaches that “[t]he control signal *Q* controls the high-side switch *Q*₁,

and the complementary signal Q' of the control signal Q controls the low-side switch Q₂.” Ex. 1001 at 8:32-34 (emphasis added).



11. Thus, the specification teaches that the control signal described in the '377 Patent is configured to “control” various components of the disclosed circuits, consistent with Petitioner’s proposed construction.

12. Extrinsic evidence further supports Petitioner’s proposed construction. For example, the Wiley Electrical and Electronics Engineering Dictionary (2004) defines the term “control signal” as “[a] signal utilized to control a device or process.” Ex. 1018.

13. Throughout my years of experience, I and other persons of ordinary skill in the art have used and encountered the term “control signal” regularly and I and other persons of ordinary skill in the art understand the plain and ordinary

meaning of “control signal” to be a “signal configured to control a circuit component.”

14. Accordingly, it is my opinion that the term “control signal” should be construed in accordance with its plain and ordinary meaning as: a “signal configured to control a circuit component.”

B. The “control signal” of the ’377 Patent is configured to control switch “K” through an inverter

15. For the following reasons, it is my opinion that the “control signal” disclosed in the ’377 Patent is configured to control switch “K” through an inverter.

16. Under Petitioner’s proposed construction, the claimed control signal may be impacted by other functionality of the circuit in performing its primary function of controlling the high-side and low-side switches. The control signal may pass through intervening logic gates and/or may change logical values along its path (*i.e.*, from 0 to 1, from 1 to 0). But if the control function is present, and meets the other requirements recited in the claims, then that signal constitutes a “control signal.”

17. The ’377 Patent teaches that when the control signal “Q” = 0, switch “K” is turned on:

Thus, the high-side switch Q is turned off, and the low-side switch Q is turned on, the switching signal SW equals to 0. Meanwhile, the switch K is turned on by the control

signal Q, the capacitor C_{TON} is discharged, and the Voltage at the non-inverting input terminal of.

Ex. 1001 at 8:55-59.

18. The '377 Patent further teaches that when the control signal $Q = 1$, switch “K” is turned off:

FIG. 12 illustrates the waveforms of the step-down regulator 40 of FIG. 11. As shown in FIG. 11 and FIG. 12, when $Q=1$, the high-side Switch Q1 is turned on, and the switching signal SW equals to the input voltage V_{in} . Meanwhile, the switch K is turned off by the control signal Q, the capacitor C_{TON} is charged. The input voltage sensing signal S11. ramps up, that is, the voltage at the non-inverting input terminal of the comparator COMP ramps up.

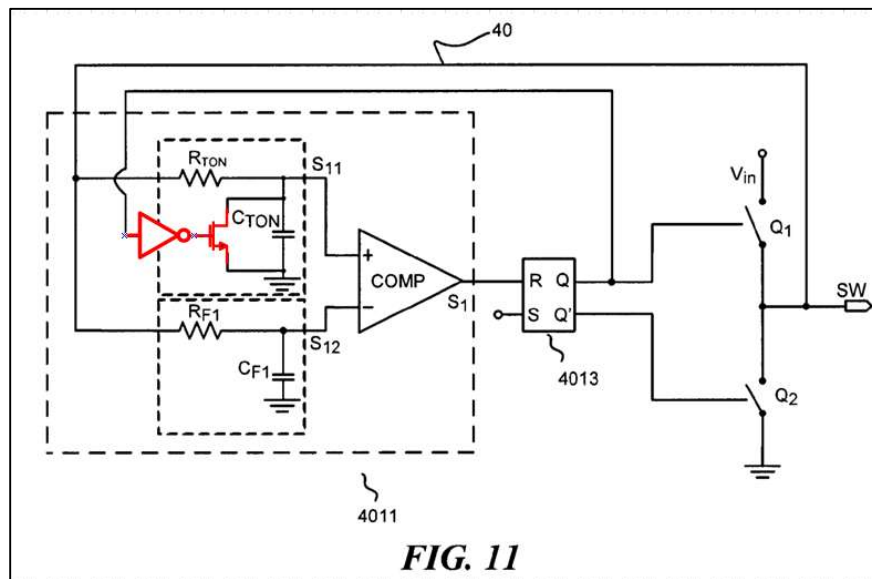
Ex. 1001 at 8:42-49.

19. Switch “K” in the '377 Patent is what is known as an N-channel MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), and not a P-channel MOSFET, because to achieve the pseudo-constant on-time disclosed in the '377 Patent, the control signal drives switch “K” through an inverter, which is a type of logic gate that inverts the logical value of a signal. Switch “K” cannot be a P-channel MOSFET because it does not fully discharge the capacitor C_{TON} .

20. Additionally, switch “K” is an N-channel transistor because it can achieve an arbitrarily low ON voltage simply by adjusting the transistor geometry. A person of ordinary skill in the art (a “POSITA”) would not have chosen a P-channel transistor over an N-channel transistor based on the specifications required in the ’377 Patent. A P-channel implementation of switch K would introduce an offset voltage (P-channel threshold voltage) that varies over process and temperature, which would result in a variable T_{ON} .

21. Given the choice between implementing the switch with an N-channel or P-channel transistor, an N-channel transistor is the only one that will operate in a way that is consistent with the universal understanding of a switch and according to the equations presented in the ’377 Patent.

22. Therefore, to turn an N-channel transistor off when $Q=1$, there must be an inverter between the output Q of element 4013 and the gate of the N-channel transistor implementing switch K as shown below. Therefore, the “control signal” turns the switch “K” on and off through an inverter.



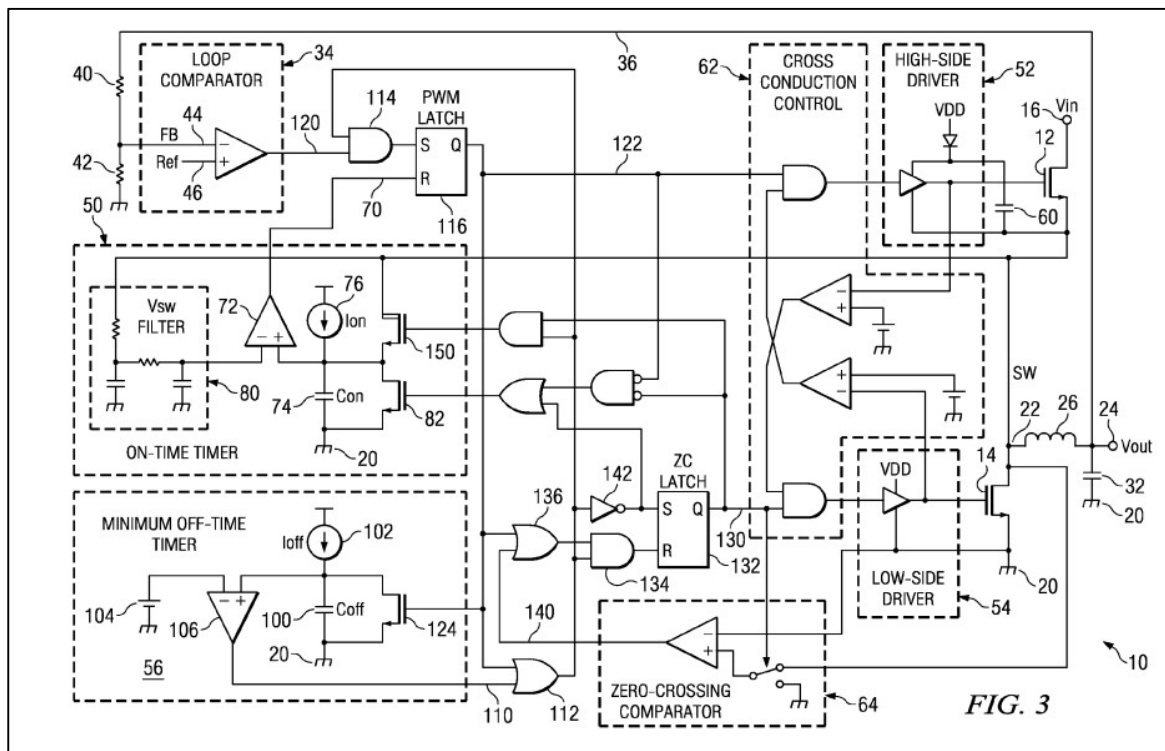
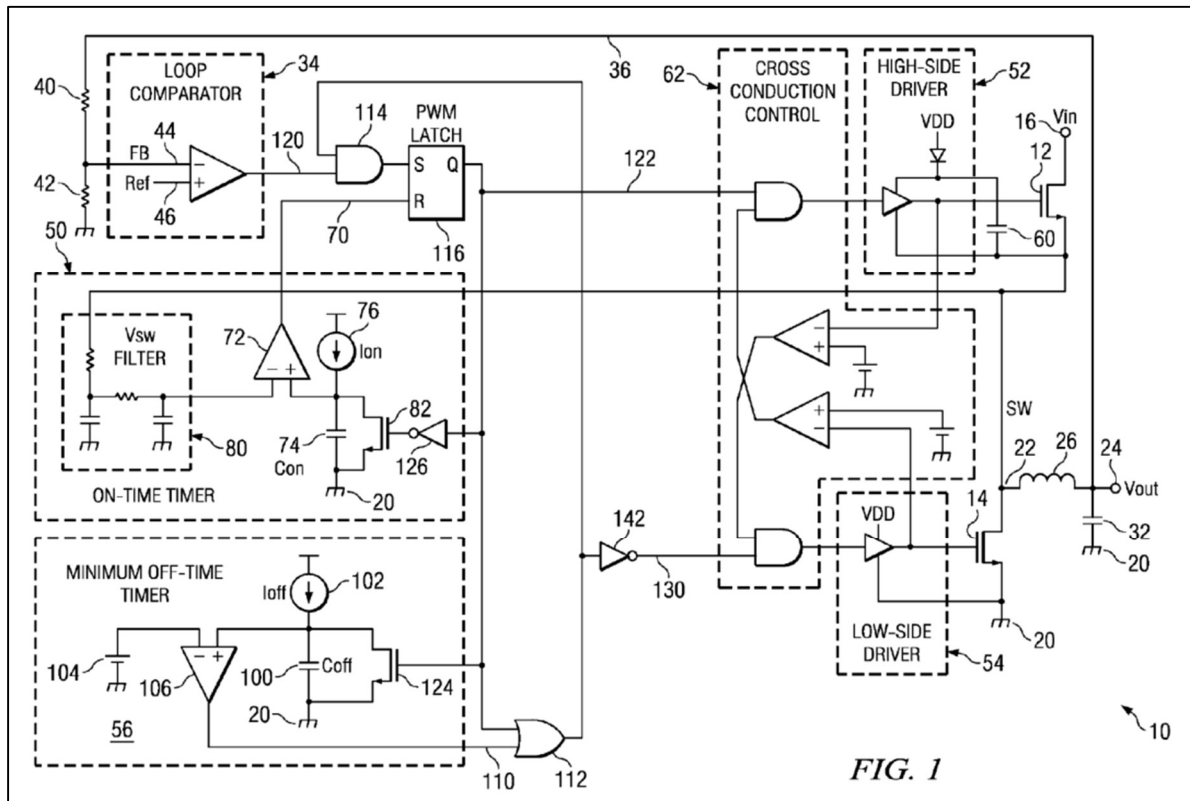
Ex. 1001 at Fig. 11 (annotation added).

23. Accordingly, it is my opinion that the “control signal” disclosed in the ’377 Patent is configured to control switch “K” through an inverter.

C. Tateishi’s Figures 1 and 3 both disclose the claimed “control signal”

24. For the following reasons, it is my opinion that the “Tateishi” prior art reference (Ex. 1007) discloses the claimed control signal in both Figures 1 and 3.

25. Tateishi’s Figures 1 and 3 operate in substantially the same manner. Tateishi’s Figures 1 and 3 are shown below:



26. Tateishi teaches that when the zero-crossing comparator 64 is not triggered, the circuit of Figure 3 operates much the same way as Figure 1. Tateishi uses the same notations in Figures 1 and 3 for key elements such as the current sources 76 and 102, the discharge transistors 82 and 124, PWM latch 116, and PWM Latch Q output 122. Additionally, paragraphs 58-59 of Tateishi teach:

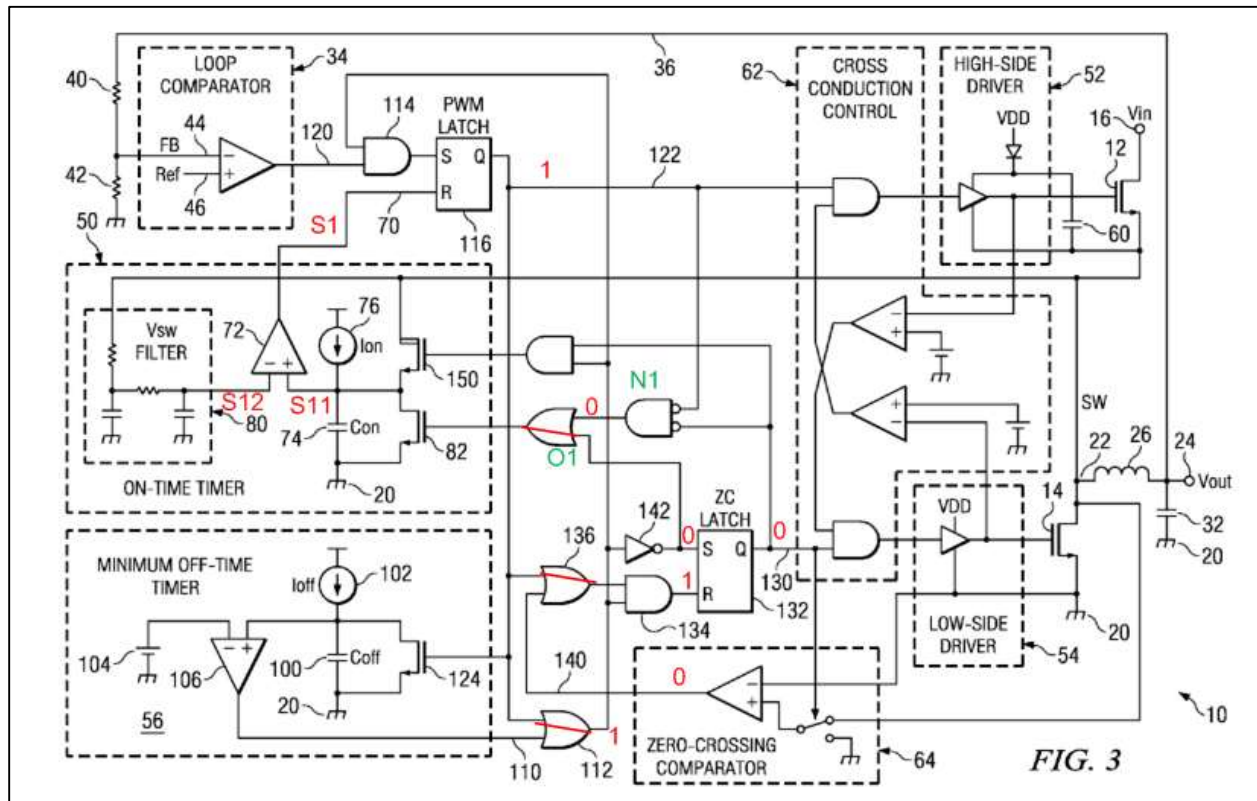
The DC to DC buck converter 10 of FIG. 3 operates in much the same manner as that of FIG.1.

Ex. 1007 at ¶ 58.

In an embodiment corresponding to the DC to DC buck converter 10 of FIG. 3 in which zero crossing is not detected. In this embodiment, the timing of the DC to DC buck converter 10 is adapted so that the inductor current is not allowed to reach zero so that no zero crossing is detected. In this embodiment, the capacitor Con 74 is left at a precharged level of $(-V_{on2})$. Again, the DC to DC buck converter 10 of FIG. 3 operates in much the same manner as that of FIG. 1.

Ex. 1007 at ¶ 59.

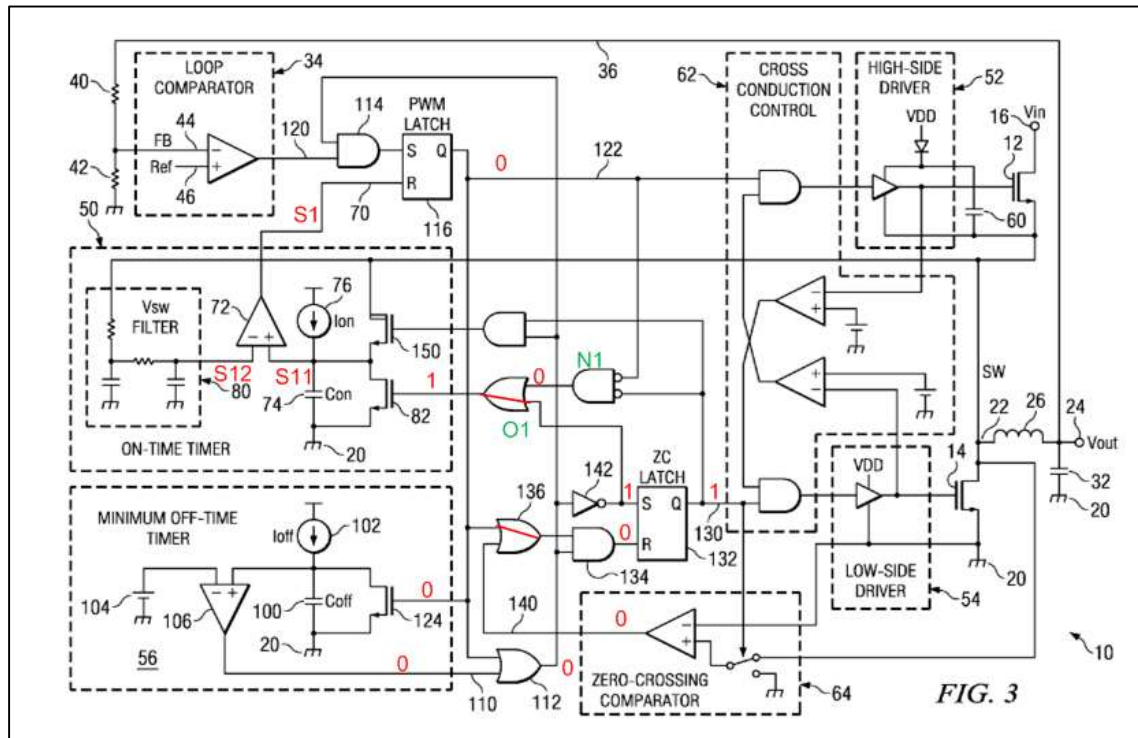
27. Tateishi's Figure 3 is annotated below for the state where the zero-crossing comparator output is 0 and the PWM LATCH Q output—control signal 122—is 1.



Ex. 1007 at Fig. 3 (annotations added).

28. In annotated Figure 3 above, I have illustrated where a particular input to a gate passes through to the output when the other input is in an enable state. For example, with a two-input OR gate with one input at logic 0, the other input will pass through. A logic 1 at the other input will pass through as a logic 1 at the output, and a logic 0 at the other input will pass through with a logic 0 at the output. I have annotated the drawing with red lines indicating which lines pass through in the current state. In this state, when Tateishi's control signal 122 equals 1, and no zero-crossing is detected (*i.e.*, the output of element 64 is 0), Figure 3 operates like Figure 1.

29. Tateishi's Figure 3 is annotated below for the state where the zero-crossing comparator 64 output is 0 and the control signal 122 equals 0. In this state, when Tateishi's control signal 122 equals 0, and no zero-crossing is detected (*i.e.*, the output of element 64 is 0), Figure 3 also operates like Figure 1.



Ex. 1007 at Fig. 3 (annotations added).

30. In both Figures 1 and 3, Tateishi's control signal 122 drives, or controls, the components to which it is transmitted. In Figure 1, this happens in the absence of each of the intervening logic gates I analyze above in Figure 3. In Figure 3, this happens even when: (a) the logical value of the control signal changes as it passes through the intervening logic gates or (b) remains unchanged. Thus, Tateishi's Figures 1 and 3 both disclose the claimed "control signal" because signal 122 is

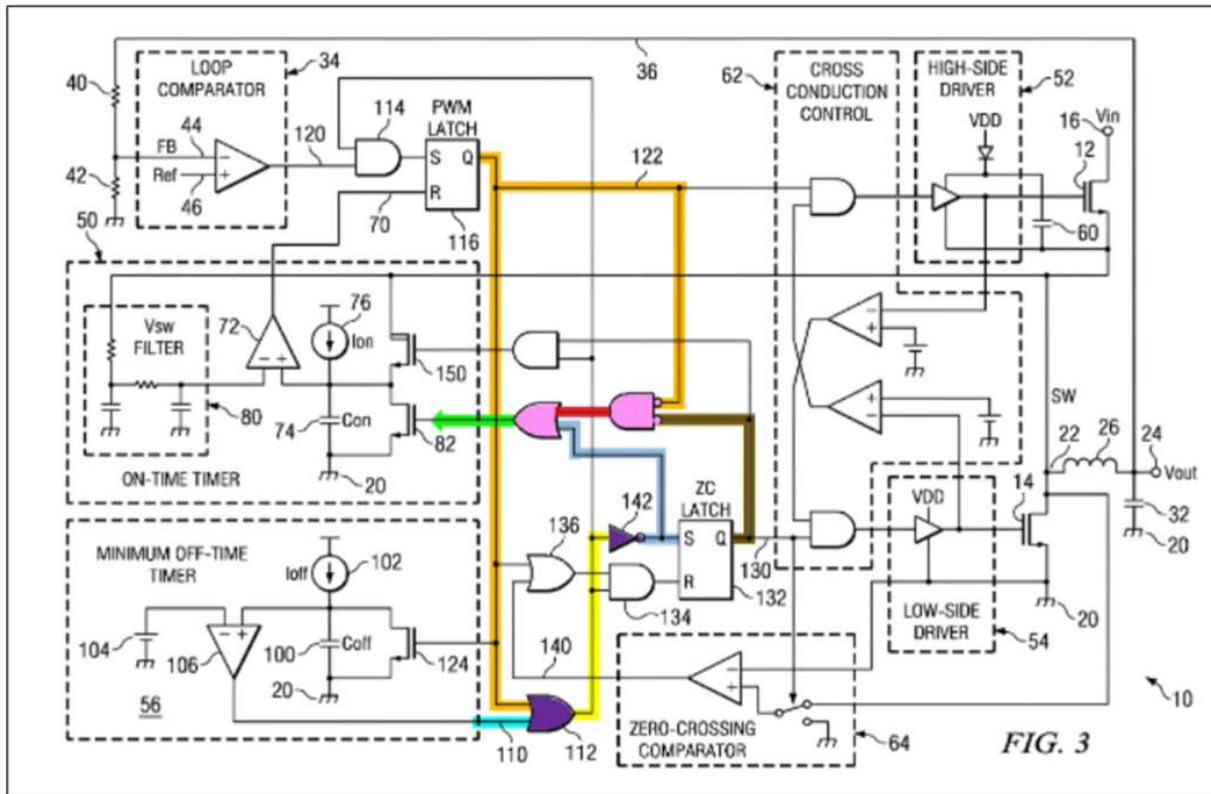
configured to control the claimed “input voltage sensing circuit” and “power stage” (which Tateishi discloses for the reasons explained in my previous declaration; Ex. 1003 at ¶¶ 84-88, 97-99).

31. Accordingly, it is my opinion that Tateishi discloses the claimed control signal in both Figures 1 and 3.

D. Mr. McAlexander’s truth table analysis is incomplete

32. On page 40 of his declaration (Ex. 2005), Mr. McAlexander presents a “truth table” purporting to show the logic states of different signals disclosed in Tateishi. For the following reasons, it is my opinion that Mr. McAlexander’s truth table analysis is incomplete.

33. An annotated version of Tateishi’s Figure 3 is reproduced below from Mr. McAlexander’s declaration. Ex. 2005 at ¶ 83. Mr. McAlexander provides a truth table (below) that he asserts “illustrates that the green signal [below] is not only logically dependent upon orange signal 122, but it is also dependent upon the minimum off-time output 110 (aqua) and the output 130 of the ZC latch 132 (brown). Consequently, one cannot define the state of the green signal output based solely on the state of the orange signal 122, thus the orange signal cannot be the control signal.” Ex. 2005 at ¶ 84.



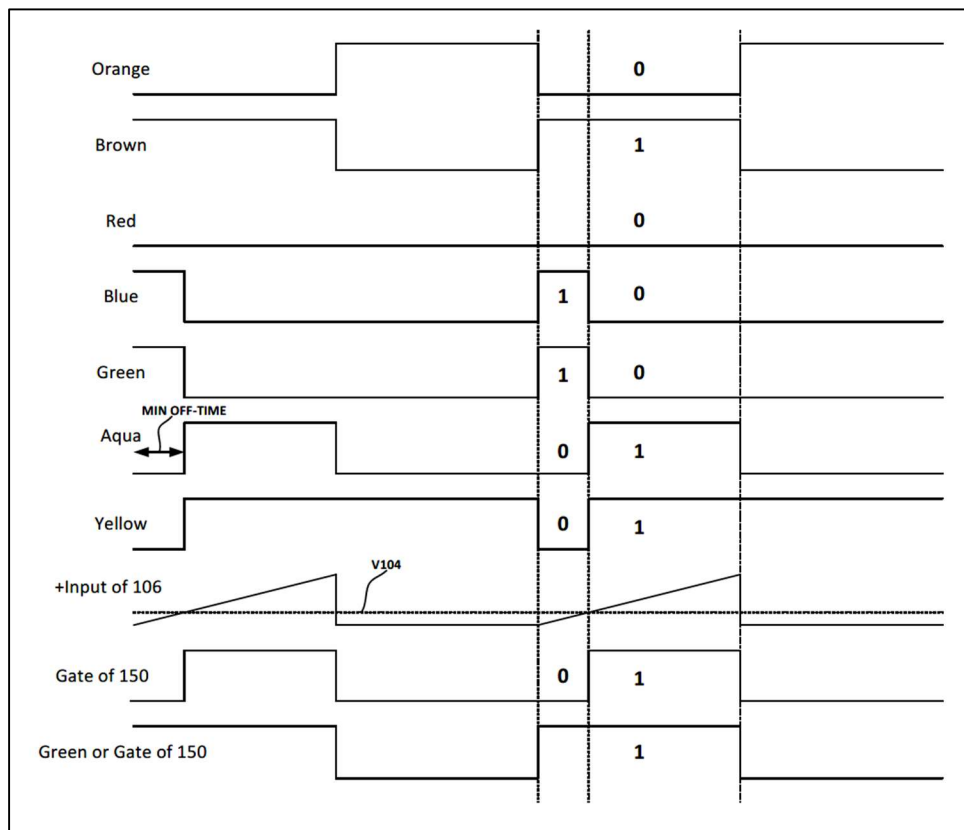
Orange	Brown	Red	Blue	Green	Aqua	Yellow
0	1 ^{*1}	0*	1	1	0	0
0	0	1	0*	1	1	1
0	1	0	0	0	1	1
1	0	0	0	0	0*	1
1	1	0	0	0	0*	1
1	0	0	0	0	1*	1

Logic Table

Ex. 2005 at ¶ 83.

34. This table provides an incomplete picture of the logical values of the signals that Mr. McAlexander analyzes. To illustrate this, I have prepared the timing

diagram shown below, which shows a more complete picture of the logical values of the signals that Mr. McAlexander analyzes. For this timing diagram, I assumed that there is no zero-crossing detection—*i.e.*, the signal 140 (the output of the zero-crossing comparator 64)—is 0. The diagram also ignores propagation delays through gates except for the case of the Aqua signal where it was necessary to illustrate its waveform. Ignoring propagation delays elsewhere has no impact on how the circuit performs. The Red signal is shown unchanging when it may have a very short pulse when Orange transitions to 0. It is inconsequential and will last only as long as it takes a signal to propagate through OR gate 112, inverter 142, and the ZC Latch 132 in Tateishi's Figure 3.



35. Consider Row 2 of Mr. McAlexander's Logic Table: 0010111. There is no time in the above timing diagram where this state exists. Red is never 1 for more than a transitional pulse (when there is no zero-crossing detection).

36. Consider Row 3 of Mr. McAlexander's Logic Table: 0100011. Row 3 of the Logic Table fails to consider the function of the transistor 150 in Figure 3. Specifically, the above timing diagram indicates that when the orange control signal is 0, the green signal exhibits two distinct states: a 1 during the leading portion and a 0 during the trailing portion. However, Row 3 of Mr. McAlexander's Logic Table reflects only the trailing state, making the logic table incomplete. Figure 3 of Tateishi supports additional features, including two discharge paths for discharging Con 74: one through transistor 82 during the leading portion and the other through transistor 150 during the trailing portion. As shown in the above timing diagram, when the green signal transitions to 0, the gate of transistor 150 goes to 1, turning on transistor 150. This connects C_{ON} 74 to the SW node, which is at 0 due to the low-side switch 14 being on, allowing C_{ON} 74 to be continuously discharged during the trailing portion of the PWM off time. In summary, when the orange control signal is 0, C_{ON} 74 is discharged sequentially through transistors 82 and 150. The functionality shown in Figure 3 is consistent with that shown in Figure 1 of Tateishi.

37. Consider Row 5 of Mr. McAlexander's Logic Table: 1100001. This row is incorrect. Orange and Brown cannot both be 1 at the same time.

38. Consider Row 6 of Mr. McAlexander's Logic Table: 1000011. This is incomplete because with Orange at 1, transistor 124 is on, capacitor C_{OFF} is discharged, and the output of comparator 106 (Aqua) is a 0. Aqua is not always 1 as the table suggests.

39. Accordingly, it is my opinion that Mr. McAlexander's truth table analysis is incomplete.

E. Current source 76 is the same element in each of Tateishi's Figures 2, 3, and 4

40. It is my opinion that current source 76 is the same element in each of Tateishi's Figures 2, 3, and 4. Tateishi's Figure 3 illustrates current source 76 using the generic symbol for an ideal current source. Figures 2 and 4 each show the detailed circuitry inside of current source 76. POSITAs would have understood that current source 76 refers to the same element in each of Tateishi's Figures 2, 3, and 4.

VI. CONCLUSION

I declare that all statements made herein of my knowledge are true, and that all statements made are believed to be true. I further declare that all statements made herein were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code.

In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross examination in the case and that cross examination will take place within the United States. If cross examination is required of me, I will appear for cross examination within the United States during the time allotted for cross examination.

A handwritten signature in black ink, appearing to read "Douglas Holberg", written in a cursive style.

Signed on July 14, 2025

By: Douglas Holberg, Ph.D.