

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,	:
Petitioner,	: IPR2024-01158
v.	: Patent 9,041,377 B2
MONOLITHIC POWER SYSTEMS, INC.,	:
Patent Owner.	:
	:

Videoconference deposition of

JOSEPH MCALEXANDER III

via Zoom

Tuesday, July 1, 2025

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Reported by: MARLA SHARP, RPR, CLR, CCRR,

OR CSR 17-0446, CA CSR 11924, WA CSR 3408

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5 Videoconference deposition of
6 JOSEPH MCALEXANDER III, held via Zoom,
7 pursuant to notice, before Marla Sharp,
8 a certified stenographic reporter
9 licensed in California, Oregon, and
10 Washington.
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A P P E A R A N C E S

(All parties appeared via videoconference.)

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A P P E A R A N C E S

(All parties appeared via videoconference.)

ALSO PRESENT:

Daniel Esparza, Remote Tech

Doug Holberg

I N D E X

EXAMINATION	PAGE
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(afternoon session)	127

DEPOSITION EXHIBITS

EXHIBIT	DESCRIPTION	PAGE
Exhibit 2005	Declaration of Joseph C. McAlexander III, P.E. (55 pages, not Bates stamped)	14

PREVIOUSLY MARKED DEPOSITION EXHIBITS

EXHIBIT	DESCRIPTION	PAGE
Exhibit 1001	U.S. Patent No. 9,041,377 B2 (16 pages, not Bates stamped)	18
Exhibit 1007	U.S. Patent Application Publication No. US 2009/0140708 A1 (13 pages, not Bates stamped)	49
Exhibit 2001	10-28-24 Declaration of Joseph C. McAlexander III, P.E. (30 pages, not Bates stamped)	127

1 P R O C E E D I N G S

2 - - -

3 DEPO TECH: Please stand by for technician
4 read-on and backup recording. Zoom will now prompt you
5 for your consent to video-record this meeting for backup
6 purposes.

7 Thank you to everyone for attending this
8 proceeding remotely, which we anticipate will run
9 smoothly.

10 Please remember to speak slow and do your best
11 not to talk over one another. Please be aware that we
12 are recording this proceeding for backup purposes. Any
13 off-the-record discussion should be had away from the
14 computer. Please remember to mute your mike for those
15 conversations.

16 Please have your video enabled to help our
17 reporter identify who is speaking. If you're unable to
18 connect with video and are connecting via phone, please
19 identify yourself each time before speaking.

20 We will provide a complimentary unedited
21 recording of this proceeding with the purchase of a
22 transcript.

1 I apologize in advance for any
2 technical-related interruptions. Thank you.

3 - - -

4 JOSEPH C. MCALEXANDER, III, P.E.,
5 having been first duly sworn,
6 was examined and testified as follows:

7 - - -

8 THE STENOGRAPHER: My name is Marla Sharp. I
9 am a stenographer licensed by the State of California.
10 My license number is 11924. Thank you.

11 Counsel, you may proceed.

12 EXAMINATION

13 BY MR. GRAY:

14 Q Mr. McAlexander, thank you for joining us
15 today. My name is Andrew Gray. I'm an attorney, and I
16 represent the defendants, Reed Semiconductor and -- in
17 this matter. I should say -- I forget we're in an ITC
18 proceeding -- I represent the petitioner.

19 So would you please state your full name for
20 the record, sir?

21 A Yes. Joseph Colby McAlexander III.

22 Q Approximately how many times have you been

1 deposed, sir?

2 A More than 200.

3 Q Please make sure that you answer all my
4 questions verbally and not with physical movements, like
5 a nod or a shrug. Okay?

6 A Understand. Sure.

7 Q As you know from 200 depositions, if you need
8 to have a question repeated, you can let me know, and
9 the court reporter will read it back to you. Okay?

10 A Yes, understand.

11 Q And if you do not understand one of my
12 questions, or if you need me to rephrase it, you can ask
13 me to do so. Okay?

14 A Certainly.

15 Q If you do not ask for clarification or
16 rephrasing of a question, then I will assume that you
17 understand that question. Okay?

18 A That is also okay.

19 Q While we cannot take a break while a question
20 is pending, please let me know whenever you need a break
21 today. And we'll accommodate it as promptly as
22 possible. Okay?

1 A Yes, sir. Of course.

2 Q And you understand that you're under oath
3 today, correct?

4 A Correct.

5 Q And you understand that you've sworn to tell
6 the truth today, correct?

7 A Correct.

8 Q Is there any reason why you can't give your
9 best testimony today?

10 A No. I know of no reason.

11 Q And where are you physically located for
12 today's deposition?

13 A I'm physically located in my home office.

14 Q Do you have any physical documents relating to
15 this proceeding with you currently?

16 A Yes, I do.

17 Q Which documents do you have with you?

18 A I have printed off a clean copy of the '377
19 Wang patent, the Tateishi Application Publication '708.

20 I also have a copy of the petition that was
21 filed in July of '24.

22 I also have the declaration of Douglas Holberg,

1 and I also have a copy of his deposition transcript.

2 I have a copy of the IPR decision that was
3 rendered in January of this year, copy of the patent
4 owner's preliminary response and the patent owner's
5 response.

6 And I also have a copy of both of my
7 declarations, the one from October of '24 and the one
8 from April of this year.

9 Q Are there any notes that you or someone else
10 has made on any of these documents?

11 A No, sir. They're all clean.

12 Q Do you have any electronic documents open on
13 your computer?

14 A I have Windows Explorer open for the purposes
15 of downloading any documents that you want to produce in
16 this matter.

17 Q And do you have any electronic documents open
18 on any other device?

19 A No, I do not.

20 Q Is anyone physically present in the room with
21 you?

22 A No. I'm alone.

1 Q What did you do to prepare for today's
2 deposition?

3 A Well, clearly I printed copies of the documents
4 that I had mentioned. I reviewed each of those
5 documents. And I also had a short meeting with counsel,
6 Miguel, who's on -- who's attending today.

7 Q Did you speak with any employees of MPS to
8 prepare for today?

9 A No, I did not.

10 Q And how much time did you spend preparing to
11 testify today?

12 A I would say preparation time total would be
13 maybe six or seven hours.

14 Q Did you search for any documents in connection
15 with this litigation?

16 A No, nothing other than just on my computer,
17 pulling these particular documents up and printing them.

18 Q Other than the documents that you have printed
19 out, did you review any other documents to prepare for
20 today's deposition?

21 A No, I did not.

22 Q So you understand that MPS has asserted

1 US Patent No. 9,041,377 against the petitioners in a
2 separate district court proceeding -- proceedings,
3 correct?

4 A Yes, I have that understanding.

5 Q All right. If I refer to the '377 patent
6 today, will you understand me to be referring to
7 US Patent No. 9,041,377?

8 A Yes.

9 Q What is your understanding of the invention to
10 which the '377 patent relates?

11 A Well, it is directed to a control circuit, for
12 example, a step-down regulator, specifically directed to
13 constant on-time.

14 THE STENOGRAPHER: I'm sorry. Specifically
15 related to what?

16 THE WITNESS: Constant on-time, sometimes
17 referred to as COT or "cot."

18 BY MR. GRAY:

19 Q Any other understandings?

20 A Well, it is specifically directed to what is
21 called pseudo COT. And that is p-s-e-u-d-o. Has a
22 number of embodiments directed to that. But

1 predominantly, as summarized in the invention with the
2 embodiments, it's directed to step-down regulators.

3 Q Anything else?

4 A I'm not sure what you mean by "anything else."
5 The patented claims themselves are directed to -- well,
6 let's call it a pseudo constant on-time control circuit
7 that's a part of -- comprised within the step-down
8 regulator.

9 And then there's specific claim limitations
10 that are directed to that -- each one of the types of
11 inventions that are described in Claims 1 through 18.

12 Q Do you have an understanding of what is novel
13 in the '377 patent over what came before?

14 A Well, there's several things that are novel. I
15 think the novelty is depend- -- is defined by the claims
16 themselves. Each claim is an invention.

17 And it certainly has addressed the art, the
18 prior art, the voltage and current type of feedback and
19 comparisons to regulation.

20 Also identifies the -- different forms of
21 constant on-time regulation and then provides a change
22 to that in addition to that. It's put in the category

1 of a pseudo constant on-time control circuit.

2 And has a specific way of feedback and
3 comparison. Specifically, it promotes the fact that
4 the -- that the former products that were designed based
5 upon prior ways of doing constant on-time where voltage
6 and current required an extra pin on the package so that
7 the Vout would be fed back in to -- so it could be
8 reviewed or analyzed and provided for a comparison basis
9 using error amplifiers.

10 In this case it excludes the need for having
11 that extra pin. So that's one of the novelties of the
12 invention.

13 Q Are there other novelties of the invention?

14 A I think the claim as a whole provides the
15 novelty of the invention, and each claim stands on its
16 own.

17 (Deposition Exhibit 2005 was marked for
18 identification.)

19 BY MR. GRAY:

20 Q I've uploaded into the chat Exhibit 2005, which
21 is your second declaration.

22 Would you please download Exhibit 2005 and take

1 a look at it, sir?

2 A Sure. Just a second.

3 Now, in the chat, I do not see any -- maybe I'm
4 missing something, but I do not see anything to
5 download.

6 Q It may be me. It may be me who's missing
7 something. Let me --

8 MR. BOMBACH: Yeah, I don't see it either.

9 MR. GRAY: Give me a second.

10 Can we go off the record real quick so I can
11 get some guidance on how to get this document shared?

12 (Recess taken from 9:21 a.m.
13 to 9:23 a.m.)

14 BY MR. GRAY:

15 Q So, Mr. McAlexander, will you please review
16 Exhibit 2005 and tell me if you are able to recognize
17 this document?

18 A Give me just a second to download it.

19 Okay. I have downloaded and I have
20 Exhibit 2005 in front of me.

21 Q What is Exhibit 2005?

22 A That is my declaration associated with the

1 IPR 2024-01158. My signature is on page 52 dated 21st
2 day of April 2025.

3 Q Will you please turn to paragraph 36 of your
4 declaration?

5 A I have it in front of me.

6 Q Okay. And do you recall writing paragraph 36?

7 A Yes, I do.

8 Q Okay. And if you'll turn your attention to the
9 next page, to figure 11.

10 A I see it.

11 Q And will you tell me what this figure 11 is on
12 page 14 of your declaration?

13 A And that figure 11 is shown in paragraph 37 and
14 specifically refers to No. 40, which is a step-down
15 regulator.

16 And it's just one of the disclosed embodiments
17 in the invention -- in the patent. Excuse me.

18 Q Has figure 11 been annotated?

19 A Yes, it has.

20 Q And who made these annotations?

21 A I made the annotations.

22 Q Okay. So do you see the blue line on

1 figure 11?

2 A Yes. That's -- the blue line extends from the
3 output of the flip-flop to the input of the yellow box,
4 which is the input voltage sensing circuit.

5 Q And do you identify the blue line as the
6 control signal that you discuss in paragraph 36 of your
7 declaration?

8 A That is correct.

9 Q And is it correct that you identify this
10 control signal as the Q output of block 4013?

11 A It would be the signal output from Q. That
12 would be correct.

13 Q Would it be fair to call where the output comes
14 from Q a node?

15 A You can refer generally to the Q output, the
16 structure, as a node.

17 Q And what is a node?

18 A Well, in computers it's a -- it's a particular
19 point of a connection to a network.

20 Here, that would be a point of connection to a
21 signal line, which is the black line coming from Q to
22 the gate of the Q1 device.

1 So that is a -- that is a line upon which a
2 signal can be transmitted. And Q can -- as the output
3 would be an output driving -- driver from that flip-flop
4 4013.

5 And so one can look at the output itself as a
6 node. It's a point for connection.

7 Q Is a line upon which a signal can be
8 transmitted a wire?

9 A It can be a wire.

10 MR. GRAY: Okay. I've uploaded Exhibit 1001
11 into the upload system. Mr. Esparza, will you please
12 share it in the chat for me?

13 DEPO TECH: Absolutely. Please stand by.

14 BY MR. GRAY:

15 Q Mr. McAlexander, would you please review
16 Exhibit 1001 and let me know if you recognize it?

17 A I've downloaded Exhibit 1001. And that is the
18 copy of the Wang '377 patent.

19 Q Please turn to page 3 of Exhibit 2001 [sic].
20 Do you see figure 4?

21 A I see figure 4, yes.

22 Q So keeping your thumb on that figure, will you

1 please turn to page 13 of the '37 [sic] patent and
2 please review the sentences in column 8, lines 18
3 through 23.

4 A All right. I've read column 8, lines 18
5 through 23. Actually, all the way to 27.

6 Q Okay. So based on this, do you understand that
7 figure 11 incorporates the on-time generator of
8 figure 4?

9 A Well, figure 4 is referred to as an input
10 voltage sensing circuit. I'm not sure what you mean by
11 an on-time generator of figure 4.

12 Q Does figure 4 contain an on-time generator?

13 A Figure 4 is directed to an input voltage
14 sensing circuit. And that's stated at line 23:

15 "...the input voltage sensing
16 circuit A1 of figure 4."

17 Q Okay. May I direct your attention to
18 line 22 --

19 A Sure.

20 Q -- of column 8.

21 And does it teach us that:

22 "The on-time generator 4011

1 comprises the input voltage sensing
2 circuit A1 of figure 4"?

3 A That's correct. And if you look at figure 11,
4 4011 is a dashed box that includes -- part of it would
5 be an input voltage sensing circuit, which is also
6 referenced as -- on line 23 as pulling it in from
7 figure 4 as part of the employment.

8 But the on-time generator 4011 is not the same
9 as the input voltage sensing circuit A1 of figure 4.
10 The input voltage sensing circuit A1 of figure 4 can be
11 used in -- within the on-time generator 4011.

12 Q Okay. Do you see the switch in figure 4
13 labeled K that's in parallel with CTON?

14 A I see that switch, yes.

15 Q Okay. And looking at figure 11, do you see a
16 switch in parallel with CTON in figure 11?

17 A Yes.

18 Q Is it your understanding that the switch in
19 figure 4 labeled K is the same switch that's in
20 figure 11?

21 A Well, the way it is drawn in figure 11, the
22 enti- -- the structure for the input voltage sensing

1 circuit of figure 4, which is the RTON, the CTON, and
2 the K switch are each one shown in figure 11, which is
3 consistent with the language in column 8.

4 Q Let's see what you said here.

5 So is a switch of figure 11 switch K of
6 figure 4?

7 A Well, the way the embodiment here is drawn is
8 pulling in figure 4 as a part of figure 11. And I see
9 nothing here that suggests that it's not a one-to-one
10 correspondence between what is in figure 4 and what is
11 incorporated in figure 11.

12 Q So the switch in figure 11 is a switch K of
13 figure 4?

14 A I would say that they are, from this
15 description, an embodiment that incorporates the switch
16 of figure 4. I see nothing that would say that it's
17 not.

18 I mean, it's what -- the entire thrust is
19 figure 11, implementing a on-time generator that
20 includes for this embodiment an input voltage sensing
21 circuit that it pulls from figure 4. I've seen nothing
22 that says that they're different.

1 Q Okay. So sticking with column 8 of the '377
2 patent, I'll ask you to please review lines 41 through
3 60.

4 A Okay.

5 Okay. I've read it.

6 Q Thank you. Do you see the reference to switch
7 K at line 46?

8 A Yes.

9 Q And do you see the reference to switch K at
10 line 57?

11 A Yes, I do.

12 Q Do you understand both of these references to
13 be to the same switch K?

14 A As described and as referenced in the figures,
15 yes. As an embodiment.

16 Q So still looking at these lines, but lines 41
17 through 47, to narrow it a bit, when Q equals 1, is
18 switch K turned off and the capacitor CTON charged?

19 A That is what it says, yes.

20 Q All right. And directing you to kind of
21 lines 53 through 60, when Q is 0, is switch K turned on
22 and capacitor CTON discharged?

1 A That is correct.

2 Q Okay. Now, I'm going to ask you to please turn
3 to page 6 of the '377 patent. And I'll direct your
4 attention to figure 8, please, sir.

5 A All right. I'm at sheet 5 of 8 on figure 8.

6 Q Do you know what a MOSFET is?

7 A Yes.

8 Q What is a MOSFET?

9 A Metal-oxide-semiconductor field-effect
10 transistor.

11 Q Looking to figure 8, do you see the dashed box
12 Y1?

13 A Yes, I do. It's a mirror circuit.

14 Q Are the components shown in Y1 MOSFET
15 transistors?

16 A The ones that are shown at Y1 are MOSFET
17 transistors, yes.

18 Q Okay. May I ask you to please turn your
19 attention to page 5 of the '377 patent and review
20 figure 7(2).

21 A Okay. I've looked at it.

22 Q Is the transistor labeled W prime in

1 figure 7(2) a MOSFET transistor?

2 A Yes, it is, a different type, but it is a
3 MOSFET transistor.

4 Q Okay. Thank you.

5 And could I ask you to please turn your
6 attention to page 3 of Exhibit -- of this exhibit and
7 point you to figure 4.

8 A Okay. I'm looking at figure 4.

9 Q So could switch K be implemented with a MOSFET
10 transistor?

11 A It could be.

12 Q Could switch K be implemented with -- do you
13 know what a bipolar junction transistor is?

14 A Yes.

15 Q Would you refer to a bipolar junction
16 transistor as a BJT transistor?

17 A It is often referred to as such, yes.

18 Q Could switch K be implemented with a BJT
19 transistor?

20 A It could be.

21 Q So to discharge CTON, an n-channel transistor
22 is used to implement switch K, correct?

1 A Well, if you -- again, it depends on what
2 you're referring to. Let's go -- let's look at in
3 combination. Figure 11 is what we were discussing
4 earlier in column 8.

5 In column 8, the way figure 4 is included into
6 figure 11 is such that -- just read the words here.
7 Just a second.

8 When the -- when we look at figure 11 -- I'm
9 answering your question. I'm just giving you the
10 context.

11 When you look at figure 11, which has a Q
12 output that turns the Q1 transistor on, that is
13 labeled -- that is identified in the embodiment as a
14 high level, a logic 1 as an output of Q.

15 I just want to make sure you're with me before
16 I go any further.

17 Q Keep going, sir.

18 A All right. That output of Q as a 1 is then
19 stated to turn K1 off. And to turn K1 off with a high
20 voltage level, that would be a PMOS or p-channel type
21 transistor, not an n-channel type MOSFET, if it was
22 implemented here.

1 Q Okay.

2 A And you could use either one. It just depends
3 upon the way you configure the circuitry.

4 Q Can a PMOS transistor fully discharge CTON?

5 A I would say transistors typically will
6 discharge within a threshold voltage of that ground
7 potential in this case.

8 Q Would you explain that to me further, sir?

9 A Well, p-chan- -- n-channel and p-channel
10 transistors have a threshold. It's called a point at
11 which they turn on, if I can be generically descriptive
12 of it.

13 And any voltage value that is less than or
14 greater than, dependent upon the n or the p-channel, the
15 switch will be on or off. The MOSFET will be on or off.

16 And that's determined by threshold. When it
17 reaches its threshold level, that's the switching point
18 between on and off.

19 And that switching point here, for the
20 p-channel transistor, would allow the switch to be
21 turned off under that condition where Q is high on
22 figure 4, which then allows the C of the capacitor CTON

1 to fully charge.

2 So K can be -- is -- the K, as implemented,
3 that K switch would be fully turned off, and it would
4 allow a full charge of the capacitor.

5 Q Would a PMOS transistor allow for CTON to be
6 fully discharged?

7 A It depends on the way in which you've arranged
8 it, but typically it will not be fully discharged
9 because it will turn off at a particular threshold.

10 So you can establish where that threshold is.
11 And then it depends upon the way in which you implement
12 the transistor. It can be trans- -- it can be a
13 transistor that's implemented where the back-gate bias
14 is the same as the ground or it could be lower than
15 ground. It depends upon the way you set it as to
16 whether or not it fully discharges or not.

17 In typical fashion, when it would turn off at a
18 particular threshold, it would not fully discharge, but
19 it would discharge it sufficiently.

20 Q If you were to use an NMOS transistor, would
21 that fully discharge CTON?

22 A If you used a n-channel transistor with the

1 source grounded, in other words, as position K, it would
2 then fully discharge CTON under that condition, yes.

3 And so, you know, any designer's going to
4 implement either p or n, dependent upon their circuit.
5 And they will associately -- associatively provide the
6 necessary circuitry to account for that.

7 I mean, the whole input -- the output S11 is
8 really the input to the comparator. And you
9 basically -- within the circuit configuration of the
10 comparator, you can determine whether or not fully
11 discharged is required or not.

12 But n or p, either one, can be used.

13 Q Okay. Please turn your attention to figure 12
14 of the '377 patent.

15 A Okay.

16 Q And do you see signal S11?

17 A I see figure -- I see figure 12, and I see S11,
18 yes.

19 Q Is this the same S11 that you were describing
20 to me a moment ago?

21 A Yes.

22 Q Can you show me where the threshold voltage you

1 described is shown in S11 on figure 12?

2 A The threshold voltage that we are speaking of
3 is associated with the switch K. That is not S11.

4 S11 is an output of the circuitry shown in
5 figure 4. So there's no representation of a threshold
6 as shown for S11. That would not make sense. It goes
7 from a low level to a high level, dependent upon whether
8 K is active or inactive.

9 Q And so what is the low level?

10 A It's a logic 0.

11 Q Is the low level ground?

12 A No. It's a logic 0.

13 It's going to be near ground. But for the
14 downstream comparator, the only thing it is looking for
15 is whether it is less than or equal or greater than S12.

16 So it doesn't have to be ground, because S12 is
17 higher than S11. So anything that's lower than S12 is
18 going to toggle the comparator in one logic state. And
19 when it is greater than S12, when it passes that, then
20 it's going to be a different -- comparator's going to
21 produce a different output result.

22 So the question about threshold is not material

1 here. The switch is either going to discharge or charge
2 the capacitor, and the thrust is charging it to a point
3 where it can exceed S12 or become S -- equal to or
4 greater than S12 or whether it's less than S12. But it
5 doesn't have to be 0 volts. It's a logic 0.

6 Q Wouldn't S12 also include this threshold in
7 order to achieve an accurate comparison?

8 A When you say is it going to use this threshold,
9 you're making an -- I'm assuming you're asking the
10 question as if the comparator is also using the same MOS
11 transistors?

12 Q Yes.

13 A It doesn't have to.

14 Q How else could it work?

15 A Well, you can use BJT. You can use
16 complementary MOS. You can use threshold that a
17 particular transistor transitions from a on to an off
18 state or off to on state.

19 Can be -- can be uniquely ascribed to a
20 transistor and different -- on a different transistor.
21 They don't all have to be the same threshold, the turn
22 on and turn off characteristics.

1 That's up to the designer. The designer's got
2 that in his toolbox -- his or her toolbox -- to design
3 his MOS technology and the transistors associated with
4 it to accommodate.

5 You also can change the sizes on the MOS
6 devices in order to change the on and off current
7 capability characteristics of it.

8 So there's a lot of flexibility built into the
9 design. They do not have to be the same threshold.

10 Q Is the threshold of a p-channel transistor
11 unchanging over process and temperature?

12 A No. It changes over process and temperature.

13 Q What about an n-channel transistor?

14 A Same.

15 Q Do you see Q on figure 12?

16 A Yes, I do.

17 Q When Q transitions from 1 to 0, CTON is
18 discharged, right?

19 A That is correct.

20 Q Okay. Can I turn your attention to column 5,
21 lines 27 through 40?

22 A Okay. I have it in front of me.

1 Q Please review those.

2 A Sure.

3 Okay. I've read it.

4 Q Do you see the term "nonlinear" in line 34?

5 A I see that.

6 Q What is meant by "nonlinear"?

7 A Nonlinear means it does not rise or fall in a
8 direct proportion.

9 Q So a p-channel threshold that varies with
10 process and temperature introduces a nonlinearity,
11 correct?

12 A Not exactly sure. Let me try to characterize
13 and answer this way. And if it doesn't respond to your
14 question, please ask it again.

15 You may have, from time to time, over a period
16 of time -- and I'm talking about minutes, hours, even
17 seconds -- you may have changes in temperature that
18 might change the characteristics slightly of a
19 particular transistor.

20 But when you're talking about within a
21 particular cycle, those fluctuations are de minimis.
22 They're not going to create a credible nonlinearity in

1 terms of the response characteristics of the device.

2 But the switches can be turning on and off and
3 certainly the threshold will be -- does have some change
4 to it based upon temperature, for example.

5 But within a particular cycle time, that
6 temperature variation would not create what I would call
7 a nonlinear response characteristics between two
8 turn-off -- turn-on and turn-off periods. But if it
9 does, the designer would take that into account.

10 But clearly the input voltage sensing circuit
11 here, which is a part of the invention that is shown in
12 figure 4, provides an output S11, which becomes an
13 input 2, the comparator circuit, for example, in
14 figure 11.

15 And so what we're looking at here is whether or
16 not you are charging and discharging the capacitor in
17 such a way that the signal S11 provides an input to the
18 comparator, so the comparator can determine whether --
19 where the level of S11 is as compared to the other level
20 S12.

21 But -- so I'm not exactly sure what you mean by
22 nonlinearity. There is a -- when you're turning the

1 transistor on, for instance, in a p-channel, I would say
2 for the time frame that we're talking about here, it
3 would be mostly linear but in terms of the response
4 characteristic of a transistor.

5 Q So by "nonlinearity," I meant as the term is
6 used on line 34 and as you described it.

7 A Mm-hmm.

8 Q Does that change your answer?

9 A No.

10 Q Okay. So going back to figure 12 -- and you
11 see while Q is -- while Q is 0, are you saying that the
12 S11 signal is not ground but is instead a p-channel
13 threshold?

14 A Well, the low level, when the -- when the
15 switch K1 -- when the switch K, excuse me, is turned on,
16 it will discharge the transistor toward the referenced
17 node ground. And it will get close to ground. So if --

18 Q But you're saying that --

19 A So for purposes --

20 Q -- that S11 is not ground?

21 A You're always going to have -- in a MOS
22 transistor, you're always going to have a drop of

1 resist -- a voltage drop across the channel of the
2 transistor. It's inherent in the transistor.

3 So you're -- you are going to essentially bring
4 that node S11 to ground. And it's going to always be a
5 little bit above, dependent upon the way in which you've
6 configured the transistor. But it is, in quotes,
7 forcing the S11 to a logic 0.

8 Q An n-channel transistor will be able to drive
9 S11 to ground, correct?

10 A There's still a voltage drop across the
11 channel. It's much smaller in this particular case, but
12 you still, in either way, are pulling it close to
13 ground. And it's certainly significantly below the
14 logic 1 level that would be required to trigger the
15 comparator downstream.

16 So whether it is at ground or close to ground
17 is irrelevant for this type of a circuit. This type of
18 a circuit comprehends the fact that it pulls it to a
19 logic 0 level, and that's sufficient.

20 Q For an n-channel, what is a typical voltage
21 drop across the channel in volts?

22 A It depends upon the particular design.

1 Q In the design disclosed in the '377 patent.

2 A The '377 patent, I don't recall it getting down
3 to the specifics of the way in which a transistor is
4 constructed in terms of that level of -- that level of
5 detail is a much higher granularity than is required by
6 this patent or this claim.

7 It's an n-channel or a p-channel transistor.
8 Can be equivalently with a BJT. And for purposes of
9 this, it is putting in place the type of switching that
10 will discharge or allow to charge the capacitor as an
11 input to the comparator. That's the level that's
12 required.

13 When a designer puts this in place, it depends
14 upon the node of the -- I'll use the word "node" here in
15 a different context. We'll talk about process nodes,
16 how state of the art it is, whether it's a feature size
17 transistor that is down in the nanometers or the
18 micrometers, like .1 mike versus 10 nanometers.

19 Those transistors are each different. And so
20 the designer's going to implement the NMOS and the PMOS
21 transistors, according to the level of technology that's
22 incorporated.

1 But there's not any specific one defined
2 threshold or one defined -- or RON resistance. That's
3 beyond the scope of this claim in this patent.

4 Q Do you know what a typical p-channel threshold
5 voltage would be?

6 A There is no typical. I've designed -- I've
7 designed circuits that have .2 volts for the threshold.
8 I've designed transistors that have 1. I've designed
9 transistors that have 2 and a half volts. It depends
10 upon the technology.

11 And I've designed transistors within integrated
12 circuits, and I'd say all integrated circuits I've
13 designed, I've had different thresholds, dependent upon
14 where a device was and what I was requiring of it.
15 There's not any precise signal threshold that's in an
16 integrated circuit design.

17 Q Turning to switch K, as a designer, would you
18 choose an n-channel transistor or a p-channel
19 transistor?

20 A Either. I could design with either one.

21 Q For figure 12, would you expect the Q equals 0
22 value to be ground?

1 A No. I would expect it to be point -- pulled
2 toward ground to discharge the transistor sufficiently
3 such that it switches the comparator. Doesn't have to
4 be ground.

5 Q If I could turn your attention to figure 4,
6 please.

7 A And I -- may I add one qualification to that?

8 Q Please.

9 A As a designer, you can get a faster response
10 characteristic out of a circuit if you do not fully
11 discharge it to ground and can compensate for it
12 elsewise through the comparator.

13 So you can design it pulling to ground, but
14 then it takes a lot -- much more time for the transition
15 to take place than if you turn it close to ground.

16 So, as a designer, I would probably design it
17 typically to be close to ground but not at ground. But
18 either one would work.

19 Q What is your understanding of what is taught by
20 the disclosure of the '377 patent?

21 A Logic 0 and logic 1, lower voltage and higher
22 voltage.

1 Q Does Q drive the power stage in figure 10?

2 A Q drives the power stage in 10. In figure 10,
3 you're talking about?

4 Q Yes, sir.

5 A Yes, it does. That's also shown driving the
6 power stage in figure 11.

7 Q Turning your attention to figure 4, one of the
8 terminals of CTON is connected to RTON, correct?

9 A Yes, that's correct. They serve -- that's a
10 common node.

11 Q Okay. Back to figure 10, would you expect
12 logic circuits in figure 10 in the power stage?

13 A Would I expect? It could be designed with or
14 without logic circuits. It depends upon the circuit
15 design implementation as to what you do in terms of
16 logic.

17 Q Would the logic gates work properly with
18 logic 0 not being ground?

19 A Say that again, please.

20 Q Would the logic gates work properly with
21 logic 0 not being ground?

22 A You're talking about in your hypothetical

1 implementation of logic gates?

2 Q Yes, sir.

3 A They could work without the logic 0 being
4 ground. Certainly.

5 Q Okay. Turning back to figure 4, we just
6 discussed that one terminal of CTON is connected to
7 RTON.

8 The other terminal of CTON is connected to
9 ground, correct?

10 A Yes, that's correct.

11 Q When CTON is discharged, the voltage as
12 observed on S11 would be the same voltage observed at
13 the terminal connected to ground, correct?

14 A No. It's discharged. It doesn't say it has to
15 be fully discharged. It's discharged.

16 Q If it were fully discharged, would it be
17 ground?

18 A One could fully discharge it to make it ground
19 to where you have the same potential in both sides.
20 Yes, you could do that.

21 Q When switch K is closed, S11 is connected to
22 ground, correct?

1 A S11 would be connected through switch K to
2 ground.

3 Q When Q equals 0, switch K is closed and S11 is
4 connected to ground, correct?

5 A In the figure 4 as shown and described in
6 figure 11 and 12, yes. When Q is low, switch K is
7 closed, and that would then connect S11 through K to the
8 ground.

9 Q Does the symbol shown in figure 4 for switch K
10 imply that there will be an offset voltage due to a
11 p-channel threshold?

12 A If you choose a p-channel device, it's inherent
13 within the structure of that p-channel device. Doesn't
14 have to be described.

15 Q Would you expect the switch symbol to represent
16 a short circuit when closed?

17 A No. It could, but it doesn't have to. If a
18 switch is used with a MOS-type transistor, it will not
19 necessarily be a short.

20 Q Why is that?

21 A Because it's a switch. It's a symbol. That
22 symbol does not -- does not by itself say, when I close

1 it, I now have a short.

2 It depends upon what you implement as your
3 switch as to how that discharge takes place.

4 It's one of the reasons you use something like
5 an MOS device, because it doesn't turn on exactly
6 immediately. It turns on gradually or turns off
7 gradually. So you have a discharge that you control
8 rather than an immediate short.

9 It would not be -- it would not be good
10 engineering to literally just produce an immediate S11
11 to ground short. That's -- that's not typically the way
12 it's done.

13 Q Do you know what a switch is?

14 A I hope so, yeah.

15 Q What is a switch?

16 A It is a device, an electrical device, that
17 connects or disconnects two different electrical
18 points -- two or more electrical points.

19 Q And within the industry, is there a standard
20 symbol that would be used on a schematic to represent a
21 switch?

22 A You can use something like what is shown in

1 figure 4. That's a representative symbol that is
2 understood in the industry as a switch.

3 Q And would a person of skill in the art, looking
4 at a switch symbol, know that it might have an offset
5 voltage?

6 A If you look at it from the perspective of the
7 person skilled in the art at the time of the invention
8 and before the invention and even today, if you had a
9 switch that was in the electrical arts, for -- art, for
10 instance, as a switch in a house, that electrical switch
11 would be known to the person skilled in the art as
12 connecting two conductors through a -- with a conductor
13 and, therefore, would be almost an immediate short.

14 If you look at the switch in the integrated
15 circuit art, you would not consider that necessarily to
16 be a direct short.

17 You would also know that the way in which you
18 implement that switch will have inherent characteristics
19 within that device as to the way it operates. And so
20 you make your selection, for instance, a MOS device
21 p-channel or n-channel, dependent upon the way you want
22 that discharge or charge to take place.

1 So the symbol is a generic symbol. And so,
2 yes, you would understand the constraints of that symbol
3 as applied to different technologies.

4 Q When a switch connects two electrical points,
5 is there typically an offset?

6 A Can you ask that question a different way? It
7 doesn't make sense to me.

8 Q When a switch connects two electrical points,
9 is there an offset?

10 A What do you mean, an offset? Where?

11 Q You used the word "offset." So in your use of
12 the word "offset." I'm just trying to understand.

13 You're saying that a switch that connects two
14 electrical points -- you said there's an offset. I want
15 to understand if that's, in fact, what you said.

16 A Okay. I -- I'll just restate because I don't
17 remember the context of that.

18 When a switch connects two electrical points
19 together, let's assume that the two electrical points
20 are not at the exact same voltage level. There's an
21 offset between the two.

22 If you were looking at a switch such as a light

1 switch in a house, connecting those two electrical
2 points would literally short one point to the other.
3 And so you discharge or charge based upon that
4 connection.

5 If you implemented it is an MOS device in an
6 integrated circuit, inherent within the MOS device are
7 MOS device parameters and characteristics that are
8 designed in to the way in which that switch operates.

9 And if it's MOS, then there will be threshold
10 voltage conditions to establish when that switch turns
11 on, when it turns off. To that extent, there is an
12 offset from ground or offset from some referenced
13 voltage as to the characteristic of that device turning
14 on and off.

15 So a designer that implements an MOS-type
16 implementation integrated circuit would understand these
17 inherent characteristics of the MOS device and would
18 design his circuitry accordingly. That's different type
19 of design than if you used it as an electrical switch in
20 a house.

21 So my comment was is that you can use the same
22 symbol, but its implementation would be distinctly

1 different depending upon the technology. And a designer
2 knows that.

3 Q Turning your attention to figure 11 of the '377
4 patent.

5 A Okay.

6 Q Would the circuit shown in figure 11 operate
7 differently if switch K were a p-channel or an
8 n-channel?

9 A All right. I think your question was looking
10 at the circuit at figure 11, would the figure 11 circuit
11 operate differently if it -- if K was a p-channel or an
12 n-channel; is that correct?

13 Q Yes, sir.

14 A Could design with either one. And you could
15 still end up with a -- with a consistent operation based
16 upon the way you design that circuitry. So you could
17 design it to be slightly different. You could design it
18 to be the same.

19 Q As shown in this design, would it operate
20 differently if switch K were a p-channel versus an
21 n-channel?

22 A The difference between using K as a p- or an

1 n-channel would change the discharge ramp rate slightly,
2 dependent upon the way in which you implemented it.

3 But you could actually compensate for that
4 based upon the size difference. For instance, if it's
5 an n-channel, you can get a faster discharge than if
6 it's a p-channel because the mobility of the n-channel
7 is faster than that of the p-channel.

8 But you can compensate for that by using a
9 larger transistor on the p-channel so you can get more
10 current per unit time and compensate for that to make
11 them -- make them actually perform in a similar fashion
12 to where the comparator downstream would not even know
13 the difference.

14 So I could use either one.

15 Q Okay. Returning to the specification, on
16 page 13 of the '377 patent, would you please review the
17 sentences in column 8 from lines 53 to 60.

18 A Okay.

19 Q And, actually, let me -- I'm going to expand
20 that. I'm going to ask you to look at 41 to 60.

21 A All right. So, basically, figure 12
22 description?

1 Q Yes.

2 Is switch K turned on when Q equals 0 and
3 turned off when Q equals 1?

4 A That is correct.

5 Q So what kind of circuit operates this way such
6 that switch K is turned on with an input Q equals 0 and
7 turned off when input Q equals 1?

8 A Well, what you're referencing is the way in
9 which figure 12 is described. Because when Q goes to 0,
10 the switch is turned on, which then discharges the
11 capacitor, which then pulls the signal line S11 from a
12 logic high to a logic low.

13 That's what's described in column 8 with regard
14 to figure 12 on lines 41 to 60 and it's consistent with
15 what is shown in the circuitry of figure 11.

16 Q Okay. I'm about to switch to a different
17 exhibit. If this would be a convenient time for a break
18 for you, we can take a break. Otherwise, we can keep
19 going.

20 A I'm willing to keep going.

21 Marla, others, weigh in. If you need a break,
22 let's take a break.

1 THE STENOGRAPHER: I'm okay. Thank you.

2 MR. GRAY: Okay. Mr. Esparza, I've uploaded
3 Exhibit 1007 into the repository. Would you please put
4 that in the chat, sir?

5 DEPO TECH: Sure. Please stand by.

6 Exhibit should be up on the chat.

7 BY MR. GRAY:

8 Q Mr. McAlexander, would you please review
9 Exhibit 1007 and tell me if you recognize it.

10 A Yes. This is the Tateishi Patent Application
11 Publication 2009/0140708 A1.

12 Q Please turn to page 2 of Exhibit 1007.
13 Do you see figure 1?

14 A One second.

15 All right. I see figure 1.

16 Q Kind of just to the left of center, do you see
17 the symbol identified with the number 126?

18 A If you can give me one second, I want to rotate
19 these couple pages so I can read them.

20 Okay. You're looking at figure 1; is that
21 correct?

22 Q Yes, sir.

1 A All right. And what's your question again,
2 please?

3 Q Do you see the symbol identified as 126 on
4 figure 1? It's just to the left of the center of the
5 page.

6 A Yes, I do.

7 Q And what is symbol 1- -- what symbol is 126
8 identifying?

9 A Figure 126 is the symbol that's used for an
10 inverter.

11 Q So inverter 126 is an inverter, right?

12 A Well stated, yes.

13 Q Okay. Inverter 126 drives the gate of the
14 transistor labeled 82, correct?

15 A That is correct.

16 Q All right. And let me just ask real quick.
17 Do you know what an inverter is?

18 A Yes.

19 Q What is an inverter?

20 A It's a logic circuit that produces the opposite
21 output as compared to the input. Takes the input and
22 then -- and changes it to the opposite logic state.

1 Q So when an inverter has a logical input of 0,
2 the logical output is a 1, correct?

3 A That's correct.

4 Q And when an inverter has a logical input of 1,
5 the logical output is a 0, correct?

6 A Correct.

7 Q So an inverter receives a signal with a first
8 logic state and outputs the signal with a second logic
9 state, right?

10 A Well, it outputs it with a second logic state
11 whereby the second logic state is different than the
12 first logic state.

13 Q Okay. So the input of the inverter is a signal
14 with the first logic state and the output of the
15 inverter is a signal with a second logic state?

16 A With the assumption that the logic states,
17 first and second, are a 10 or a 01, the answer's yes.

18 Q Yeah, so the control signal is a digital
19 signal, correct?

20 A Here in this representation, yes.

21 Q And as you just said, a digital signal is a 0
22 or a 1, correct?

1 A That's the way it's defined logically.

2 Q So the control signal can be a 0 or a 1,
3 correct?

4 A A control signal can be either of two states.

5 Q And what are those two states?

6 A Well, in this case when we're talking about
7 binary, a logic 0 and a logic 1.

8 Q Okay. May I refer you back to figure 11 of the
9 '377 patent?

10 A Okay. I have it.

11 Q Is the control signal at the Q output of block
12 4013 the same control signal that drives the switch in
13 parallel with CTON?

14 A I just now got figure 11 in front of me. Say
15 that again, please.

16 Q Is the control signal at the Q output of
17 block 4013 the same control signal that drives the
18 switch K or the switch that it's in parallel with CTON?

19 A The figure 11 embodiment shows that the signal
20 output from Q -- output from the 4013 circuit Q drives
21 the Q1. It also drives the transistor -- the switch K
22 back --

1 Q Okay.

2 A -- to the on-time generator circuit.

3 Q If switch K is an n-channel MOSFET and Q equals
4 0, then switch K is open, correct?

5 A That would be correct.

6 Q And when the switch K is open, the capacitor is
7 charging, correct?

8 A That is correct. When Q is open -- or when Q
9 is a 0 for an n-channel transistor, then the capacitor
10 CTON would be charging.

11 Q Okay. So back to column 8, please. And this
12 time looking at lines 53 through 58.

13 Let me know when you're with me, sir.

14 A Okay. In the '377 patent, line 53 through 58.
15 I'm there.

16 Q For the capacitor to discharge, switch K needs
17 to be closed, correct?

18 A For the capacitor to discharge, the CTON
19 capacitor for it to discharge K needs to be closed,
20 that's correct.

21 Q If switch K is an n-channel MOSFET, then
22 switch K is closed when Q equals 1, correct?

1 A That's correct.

2 Q So, therefore, if a capacitor's discharged,
3 does it have any charge left in it?

4 A It could, sure.

5 Q What does the word "discharged" mean to you?

6 A It means take the presence of a particular
7 quantity of charge and remove some of that charge --
8 some or all of that charge. If it's fully discharged,
9 then all of the charge that was represented on that
10 particular plate of the capacitor would be removed.

11 But discharge does not necessarily have to
12 remove all of the charge.

13 Q Okay. A moment ago you confirmed that if
14 switch K is an n-channel MOSFET, then when switch K is
15 clo- -- then switch K's closed when Q equals 1, right?
16 You remember that?

17 A When an n-channel Q is a 1, then you've got a
18 switch that's closed.

19 Q Therefore, there must be an inverter between
20 the output of block 4013 and the input of switch K when
21 Q equals 1 to effectively discharge the capacitor as
22 identified in the '377 patent, correct?

1 A If I understand your question correctly, if you
2 use a logic output Q of 1 that's going to represent a
3 discharge of K, then it is -- let me change that.

4 Because your output of Q is a 0, and that's
5 going to represent an attempt to -- discharge 1.

6 All right. If you're going to have an output
7 of 1 -- output Q of a 1 and that's going to represent a
8 discharge condition of K, then you could directly
9 connect it to an NMOS transistor.

10 If you were going to use a p-channel
11 transistor, PMOS transistor there, then you would have
12 to invert that signal before it goes to the gate of that
13 switch.

14 But depends upon the way in which you've
15 configured your logic as to whether you'd use an NMOS or
16 an equivalent -- or, excuse me, use a PMOS or an
17 equivalent inverter NMOS to get the same answer.

18 Q All right. So when Q equals 0, in order to
19 turn on an n-channel transistor, an inverter's needed,
20 right?

21 A Yes, yeah.

22 Q Okay. So does that mean that there's an

1 inverter between the output of block 4013 and the input
2 to switch K?

3 A Well, if you -- if you implement the
4 embodiment -- the embodiment in figure 11 incorporates
5 figure 4, as we discussed before.

6 And the way in which that logic is configured,
7 if I were to use a p-channel transistor, then I would
8 just insert -- I would replace that symbol K with a
9 p-channel transistor. If I want to replace it with an
10 n-channel, then I'd use an inverter.

11 Designer would know to do that.

12 Q Okay. Returning to the Tateishi publication in
13 figure 1.

14 A Okay. I've got it.

15 Q All right. So just below the center of that
16 figure, do you see an inverter labeled 142?

17 A And you're looking at the '708 Tateishi at
18 figure 1?

19 Q Yes, sir, Exhibit 1007. Just below the center
20 of figure 1.

21 A Oh, okay. Yes. Yes, I see that. Inverter
22 142, yes. Thank you.

1 Q And inverter 142 has an output labeled 130,
2 correct?

3 A That is correct.

4 Q Okay. So kind of in the -- not exactly, but
5 kind of in the upper right-hand corner, do you see the
6 transistor labeled 12?

7 A Yes, I do.

8 Q That's the high-side transistor, right?

9 A Yes, that's correct.

10 Q Okay. And now kind of in the bottom right
11 corner, do you see the transistor labeled 14?

12 A Yes.

13 Q And that's the low-side transistor, correct?

14 A That's correct.

15 Q So during normal operation, the high-side and
16 low-side transistors will not be on at the same time,
17 correct?

18 A Hopefully not. There sometimes will be an
19 overlap but hopefully not.

20 Q Okay. So kind of more upper left quadrant, you
21 see the SR latch 116 -- or PWM latch 116?

22 A Let me get this hard copy turned around here so

1 I can look at it.

2 You're referring to 113?

3 Q 116.

4 A 116. Okay. Yes, I -- now I'm with you. Was
5 looking for the wrong -- yes, I see it.

6 Q And 122 is the output of the SR latch 116,
7 correct?

8 A Yes, that's correct. That's the signal output
9 of the latch.

10 Q And the high-side transistor 12 is on when the
11 output 122 of the SR latch 116 is a logical value 1,
12 correct?

13 A Yes, that is correct.

14 Q And the low-side transistor 14 is on when the
15 output 122 of SR latch 116 is a logical value 0,
16 correct?

17 A Yes, sir, that's correct.

18 Q All right. And the low-side transistor 1 --
19 excuse me -- the low-side transistor 14 is on when the
20 output 130 of the inverter 142 is a logical value 1,
21 correct?

22 A That is correct.

1 Q Okay. Do you see OR gate 112? At the bottom.

2 A I see OR gate 112 at the bottom center
3 figure 1.

4 Q Yeah. So OR gate 112 receives the output 110
5 of the minimum off-time generator 56 generated by
6 comparator 106, correct?

7 A Yeah.

8 Q Okay. And OR gate 112 also receives the output
9 122 of the SR latch 116, correct?

10 A Yes, that is correct.

11 Q So if the logical value of output 110 is 0, the
12 output of OR gate 112 will have the same logical value
13 as output 122 of the SR latch 116, correct?

14 A Well, if the output value of 116 is a
15 logic 1 -- I believe that was your question, right, your
16 statement?

17 Q Well, no. So it's -- if the logical value of
18 110 is 0, then the output of OR gate 112 will have the
19 same logical value as output 122 of SR latch 116,
20 correct?

21 A That would be correct. If 110 is held low,
22 then the OR gate is going to switch -- generate a signal

1 output that would be a logic state comparable to what
2 the logic state of 122 is. Different signals, but it
3 would -- the output of 112 would follow the logic state
4 of the input to Q 122.

5 Q Okay. So when output 110 has a logical value
6 of 0 and output 122 has an output value of 0, the output
7 of OR gate 112 has a logical value of 0, correct?

8 A The output of 112 is going to reflect the
9 output lo- -- it's going to reflect the input logic
10 state of 122 under that condition.

11 Q So when output 110 has a logical value of 0 and
12 output 122 has a logical value of 0, the output of
13 OR gate 112 has a logical value of 0, correct?

14 A Under that condition, yes.

15 Q And when output 110 has a logical value of 0
16 and output 122 has a logical value of 1, the output of
17 OR gate 112 will have a logical value of 1, correct?

18 A Under that condition, yes.

19 Q All right. And when output 110 has a logical
20 value of 0, then the output of OR gate 112 will be
21 equivalent to the logical value at output 122, correct?

22 A They will have corresponding logic -- logic

1 values.

2 Q Okay. The input of inverter 142 is the output
3 of OR gate 112, correct?

4 A Correct.

5 Q When the input to inverter 142 is a logical 0,
6 the output 130 of inverter 142 is a logical 1, correct?

7 A The output of 112 is a logic 0. The output of
8 142 is a logic 1.

9 Q Because that's what inverters do?

10 A Correct.

11 Q And when output 110 has a logical value of 0
12 and output 122 has a logical value of 0, the output 130
13 of inverter 142 is a logical value of 1, correct?

14 A Right. It's going to reflect the opposite of
15 its input.

16 Q Make sure I'm not asking the same question
17 twice. These all kind of stack up.

18 When the output -- when output 110 has a
19 logical value of 0 and output 122 has a logical value of
20 1, the output 130 of inverter 142 has a logical value of
21 0, correct?

22 A Correct.

1 Q When output 110 has a logical value of 0 and
2 output 122 has a logical value of 0, output 130 will
3 have a logical value of 1, correct?

4 A Correct.

5 Q And when output 110 has a logical value of 0
6 and output 122 has a logical value of 1, output 130 will
7 have a logical value of 0, correct?

8 A That's asked before, but the answer's yes.

9 Q Did I ask that one before? Okay.

10 Inverter 126 receives output 122, correct?

11 A It does receive output 122, yes.

12 Q When output 122 has a logical value of 0, the
13 output of inverter 126 will have a logical value of 1,
14 correct?

15 A Correct.

16 Q And when output 122 has a logical value of 1,
17 the output of inverter 126 will have a logical value of
18 0, correct?

19 A Also correct.

20 Q And the output of inverter 126 connects to the
21 gate of transistor 82, correct?

22 A It does, yes.

1 Q When the logical output of inverter 126 is
2 logical 0, the gate of transistor 82 will have a logical
3 value of 0, correct?

4 A Say that one again, please.

5 Q When the logical value of inverter 126 is 0,
6 the gate of transistor 82 will have a logical value of
7 0, correct?

8 A Yeah. The input to that gate would be a
9 logic 0 because that's the output of inverter 126.

10 Q All right. And to the contrary, when the
11 logical output of inverter 126 is 1, the gate of
12 transistor 82 will have a logical value of 1, correct?

13 A At its input, yes.

14 Q When the gate of transistor 82 has a logical
15 value of 0, it's off, right?

16 A Correct.

17 Q And when the gate of transistor 82 has a
18 logical value of 1, it's on, right?

19 A Correct.

20 Q All right. Output 130 is an input to an AND
21 gate within the cross-conduction control block, correct?

22 A Say that one again, out -- with respect to

1 output 130.

2 Q Oh. So if you look kind of in the top of
3 figure 1, just off the right side, you see there's a --
4 there's a block identified, says "Cross Conduction
5 Control"?

6 A Yeah. It's reference figure 62.

7 Q 62. So output 130 is an input to an AND gate
8 within the cross-conduction control block, right?

9 A That is correct.

10 Q All right. And output 122 is an input to an
11 AND gate to the cross-conduction control block, correct?

12 A Output 130 is an input to an AND gate in the
13 cross-conduction control block, that's correct.

14 Q And output 122 is an input to an AND gate in
15 the cross-conduction control block, right?

16 A To a different AND gate, yes.

17 Q Yes, yes, different AND gate.

18 Okay. Returning to -- or turning to page 4,
19 figure 3 of Tateishi.

20 Okay. So looking at figure 3 of Tateishi, when
21 the logical value of output 122 is a logic value 0,
22 while the logic value of output 110 is 0, the output of

1 OR gate 112 is a 0, correct?

2 A In figure 3, with 110 held at a logic 0, the
3 output of 112 is going to reflect the input logic value
4 of 122. So if 122 input is a 0, then the output of 112
5 would be a 0.

6 Q Okay. When the logical value of output 122 is
7 0, while the logical value of 140 is 0, the output of
8 OR gate 136 is 0, correct?

9 A Yeah. The output signal -- the different
10 output signal out of OR gate 136 would also be a 0 logic
11 state based upon both the input 122 and 140 being 0.

12 Q Okay. And when the output of OR gate 112 is a
13 logical 0 and OR gate 136 is a logical 0, the output of
14 AND gate 134 is also logic value 0, correct?

15 A Yeah, both inputs -- if both inputs to logic
16 gate -- logic AND gate 134 are a 0, then the output of
17 134 is also going to be a 0. Different signal, but
18 it'll be the same logic state.

19 Q So when you say "different signals," what do
20 you mean?

21 A It's a different line. It's a different
22 signal. The inputs -- for instance, the inputs to the

1 134, which is the output of 112 and the output of 136,
2 those two inputs, they do not pass through AND gate 134.
3 They are inputs to 134. And then 134 internally
4 generates an output, a different signal output.

5 Q So what is a signal?

6 A A signal is a -- is a set of voltage values in
7 some type of a form that's propagated onto a conductor,
8 onto an -- onto in this case a wire, a connection point
9 between 136, 140, and 134.

10 Q A signal is information, right?

11 A A signal can provide information. There's
12 information content in a signal.

13 Q Okay. So when the output of OR gate 112 is
14 logical 0, the output of inverter gate 142 is a logical
15 value 1, correct?

16 A That's if the -- if we have the same assumption
17 that the -- the logic value of 110 is a 0?

18 Q Yes.

19 A Then the output of 112, with 122 being a 0, is
20 also a 0. And under that condition, then the output of
21 the inverter 142 would be the opposite in logic 1.

22 Q When the output of AND gate 134 is logical 0

1 and the output of inverter 142 is logical 1, the logical
2 output 130 of ZC latch 132 is logical 1, correct?

3 A Yeah. Once the input to the set latch is
4 changed to a logic 1, then it's going to be reflected on
5 a different signal line called the output Q. And that
6 would also be reflective of a logic 1.

7 Logic would be the same, different signal line,
8 but logic's the same.

9 Q When the logical output of inverter 142 is
10 logical 1, the output of the OR gate driving the gate of
11 transistor 82 is also logical 1, correct?

12 A Say that again, please.

13 Q When the logical output of inverter 142 is
14 logical 1, the output of the OR gate driving the gate of
15 transistor 82 is also a logical 1, correct?

16 A Yeah. If you go through that logic, you will
17 have a corresponding logic shift to the gate of 82,
18 which would also be a 1.

19 Q When the logical value of output 122 is logical
20 1, the output of OR gate 112 is 1, correct?

21 A Any input transition on the input of OR gate
22 112 will -- to a 1 will produce a 1 output.

1 Q All right. So when the logical value of output
2 122 is logical 1, the output of OR gate 136 is also
3 logical 1, correct?

4 A That is correct.

5 Q And when the output of OR gate 112 and OR gate
6 136 is logical 1, the output of AND gate 134 is
7 logical 1, correct?

8 A Also correct.

9 Q When the output of OR gate 112 is logical 1,
10 the output of gate 142 is logical 0, right?

11 A That is correct.

12 Q And when the output of AND gate 134 is logical
13 1 and the output of inverter 142 is logical 0, the
14 logical output of ZC latch 132, output 130, is
15 logical 0?

16 A Yes. The output of logic gate -- AND gate 134
17 being a 1 is to the reset input of the ZC latch, which
18 is going to create a 0 output on Q of 132.

19 Q Is output 130 an input to an AND gate in the
20 cross-conduction control block?

21 A Yes, it is.

22 Q And is output 122 an input to an AND gate in

1 the cross-conduction control block?

2 A A different AND gate, but the answer's yes.

3 Q All right. So if output 122 is a logic 1,
4 while output 130 is a logic 0, the output of the AND
5 gate which receives inverting inputs is logic 0,
6 correct?

7 A Say that again because we're dealing with two
8 different AND gates.

9 Q Yeah. If output 122 is a logic 1 --

10 A Okay.

11 Q -- while output 130 is a logic 0, the output of
12 the AND gate which receives inverting inputs is logic 0,
13 correct?

14 A I'm having difficulty understanding the last
15 phrase with regard to the inverting inputs. So maybe
16 you could explain it a different way?

17 MR. GRAY: Why don't we take five minutes.
18 It's 11:00 my time. So let's take a quick break, ten
19 minutes, please.

20 THE WITNESS: Okay.

21 (Recess taken from 10:59 a.m.
22 to 11:15 a.m.)

1 BY MR. GRAY:

2 Q So, Mr. McAlexander, may I turn your attention
3 to Exhibit 2005, which is your second declaration, and
4 paragraph 71 in that declaration?

5 A Okay. Sure. I'm on Exhibit 2005 at paragraph
6 71.

7 Q Okay. And you see in that paragraph, in your
8 second sentence, you wrote:

9 "An AND gate with inverting
10 inputs..."?

11 A Yes, I see that sentence.

12 Q Okay. At the top of page 32 is an annotated
13 copy of figure 3 from Tateishi; is that correct?

14 A Yes, that is correct. Figure 3.

15 Q Do you see the pink AND gate?

16 A It's represented as an -- as an AND gate with
17 inverting inputs, yes.

18 Q And so in paragraph 71, when you refer to "an
19 AND gate with inverting inputs," is that the pink gate
20 in your figure?

21 A Well, I have two pink gates. There's an AND
22 gate and an OR gate, but it's the one --

1 Q The pink AND gate.

2 A -- on the right.

3 I'm --

4 Q The pink AND gate.

5 A I'm sorry. I talked over you. Say it again.

6 Q The pink AND gate.

7 A That's correct.

8 Q Okay. If output 122 is a logic 1 while output
9 130 is a logic 0, the output of the pink AND gate is
10 logic 0, correct?

11 A Yes. If the output 122 is a 1, I think you
12 said --

13 Q Yes, sir.

14 A -- then it gets inverted, so it's a 0 input to
15 the AND gate, so you have a 0 output.

16 Q And if output 122 is a logic 0 while output 130
17 is a logic 1, the output of the pink AND gate is a
18 logic 0, correct?

19 A Yeah, if either inputs to the AND gate is a 0,
20 the output's going to be a 0.

21 Q Right. So the only condition where the pink
22 AND gate can have a logic 1 output is if both inputs are

1 logic 0, correct?

2 A Which means both inputs to the inverted side
3 have to be a logic 1.

4 Q I'm sorry. Could you explain that?

5 A The only way you can get a logic -- you said a
6 logic 1 output or logic 0?

7 Q A logic 1 output.

8 A Right. The logic 1 output, both inputs to the
9 AND gate have to be a logic 1, which means the inverting
10 side has to be a logic 0 for both inputs.

11 The input -- the two inputs, 122 and 130, get
12 inverted before they're input to the AND gate.

13 Q So the input to the bubbles have to be 0,
14 right?

15 A That is correct.

16 Q And if both inputs of the pink AND gate are
17 logic 0, then output 122 is logic 0 and output 130 is
18 logic 0, right?

19 A If the outputs 122 and 130 are both -- if the
20 signals 122 and 130 are both a logic 1, then you will
21 have a logic 0 output from the AND gate.

22 Q What about the input to the bubbles?

1 A Well, when I speak -- if you notice, lines 122
2 and 130 go to the bubble, not to the input to the AND
3 gate. They go to the bubble.

4 So if 122 and 130 signal lines going to the
5 bubble are a logic 1, then the opposite side of that
6 bubble is going to be a logic 0 to the AND gate, which
7 then produces a 0 output from that AND gate.

8 Q Okay. When output 120 is logic 0 and output
9 130 is logic 0, then -- excuse me -- when output 122 is
10 logic 0 and output 130 is logic 0, then both output
11 transistors 12 and 14 are off, correct?

12 A If the output from -- if the output signal 122
13 is a logic 0, then transistor 12 is turned off.

14 If the output 130 from the Z latch is a 0, then
15 under that condition, transistor 14 is turned off.

16 Q Please turn to page 7 of Tateishi,
17 Exhibit 1007.

18 A Is this at column 3 and 4?

19 Give me one second.

20 Q Well, the columns aren't numbered. But, yes,
21 technically it would be column 4. So I would ask you to
22 read paragraph 19, please. It begins "The DC to DC buck

1 converter 10."

2 Do you see paragraph 19?

3 A Okay. Paragraph, what, 19?

4 Q Yes, sir.

5 A Okay. I'm there.

6 Q Will you please read that paragraph?

7 A Okay. I've read paragraph 19.

8 Q Okay. Directing your attention to the second
9 sentence of paragraph 19, the on-time described by
10 Tateishi is when the high-side switch 12 is turned on
11 and the low-side switch 14 is turned off, correct?

12 A That's a correct reading.

13 Q So to turn the high-switch 12 on and the
14 low-side switch 14 off, output 122 must be logic 1 and
15 output 130 must be logic 1 as well, correct?

16 A I hope not.

17 Q Excuse me. And 130 must be logic 0?

18 A If you want to turn the high-side switch on,
19 122 has to be a 1. If you want to turn the low-side
20 switch off, 130 has to be a 0.

21 Q Thank you. When output 122 is a logical 1 and
22 output 130 is a logical 0, the output of OR gate 112 is

1 a logical 1 and the output of inverter 142 is a
2 logical 0, correct?

3 A If the output of 112 is a logic 1, the output
4 of 142 inverter would be the opposite logic 0.

5 Q And when output 122 is a logic 1 and output 130
6 is a logic 0, the output of the AND gate -- of the pink
7 gate is logic 0, correct?

8 A Okay. Now you're back to my -- my --

9 Q I'm just trying to identify which AND gate that
10 I'm referring to. But it's the -- it's the one in
11 Tateishi figure 3 that, in your declaration, you colored
12 pink.

13 A The reason I'm asking is because the paragraph
14 19 at Tateishi that we've been looking at is figure 1,
15 not figure 3. And on page 32, paragraph 69, the figure
16 that I'm showing is figure 3.

17 So there's two different figures that we're
18 talking about. That's why I want to make sure I'm
19 correctly understanding your question.

20 Q Okay. Let's look at the figure 3.

21 A Okay.

22 Q When output 122 is a logic 1 and output 130 is

1 logic 0, the output of the pink AND gate is logic 0,
2 correct?

3 A If the output 122 is a logic 0 --

4 Q No, 1, logic 1.

5 A If the output logic -- if output of 122 is a
6 logic 1 and the output of 130 is also a logic 1?

7 Q No, it was logic 0.

8 A Logic 0. All right. Well, if you have one 0,
9 then you're going to have a 0 output of the AND gate.

10 Q Okay. And when the output of the pink AND gate
11 is logic 0 and output of inverter 142 is logic 0, the
12 gate of transistor 82 must also be a logic 0, correct?

13 A If the output of the pink AND gate and the
14 output of -- and the other input to the OR gate -- if
15 both inputs to the OR gate that is -- that I've labeled
16 as pink are a 0, then the output that drives -- or the
17 OR gate that drives 80 -- transistor 82 is also 0.

18 Q Okay. So when the gate of transistor 82 is a
19 0, the transistor 82 is off, correct?

20 A That is correct.

21 Q And Con 74 charges while transistor 82 is off,
22 correct?

1 A That is correct.

2 Q And when transistor 82 is turned on, Con 74 is
3 discharged, correct?

4 A Yeah, when 82 is turned on, then that would
5 promote a discharge of the capacitor 74.

6 Q Okay. Let's return to your declaration and
7 page 40.

8 A Okay. I'm at page 40.

9 Q And you see the logic table at the top of page
10 40?

11 A Yes, I do.

12 Q All right. And on page 39, do you see the
13 annotated figure 3?

14 A Yes, I do.

15 Q And do the colors of the annotations in
16 figure 3 on page 39 of your declaration correspond to
17 the colors of the logic table on page 40 of your
18 declaration?

19 A Yes, they do.

20 Q All right. And does this truth table on page
21 40 represent your interpretation of how the circuit
22 diagram shown on page 39 operates?

1 A Yes.

2 Q Can I direct your attention to the fifth row of
3 your logic table?

4 A The green -- the fifth row?

5 Q Yes, sir.

6 A Two, three, four, five. Okay.

7 Q And it has values orange 1, brown 1, red 0,
8 blue 0, green 0, aqua 0, yellow 1?

9 A Yes, sir.

10 Q Now, orange annotated line shown on page 39 of
11 your declaration represents output 122 of the SR latch
12 116, correct?

13 A Correct.

14 Q And in row 5 of your logic table shown on page
15 40 of your declaration, output 142 -- the output 122 is
16 given the value of 1, correct?

17 A That is correct.

18 Q And the yellow annotated line on page 39 of
19 your declaration represents the output of OR gate 112,
20 correct?

21 A That's correct, also at a logic 1.

22 Q And in row 5 of your logic table, shown on

1 page 40 of your declaration, the output of OR gate 112
2 is given the value of 1, correct?

3 A That is correct.

4 Q All right. OR gate 136 receives output 122 as
5 an input, correct?

6 A 136 OR gate receives 122 as an input. That's
7 correct.

8 Q And when output 122, annotated in orange, has a
9 logic value of 1, the OR gate 136 has an output logic
10 value of 1, correct?

11 A That would be correct.

12 Q And AND gate 134 receives the output of gate
13 112 and OR gate 136, correct?

14 A That is correct.

15 Q So when the output of OR gate 112, which is
16 annotated in your circuit diagram in yellow, is a logic
17 value of 1 and the output of OR gate 136 is a logic
18 value of 1, the output of AND gate 134 is a logic value
19 of 1, correct?

20 A That would be correct.

21 Q And when output 122 is a logic value of 1, the
22 output of AND gate 134 is a 1, correct?

1 A That would be correct.

2 Q All right. As indicated in row 5 of your logic
3 table, inverter 142 receives the input of the OR gate
4 112, which is, again, annotated in yellow, and has a
5 logic value of 1, correct?

6 A Say that again, please.

7 Q Inverter 142 receives the output of the OR gate
8 112 and has a logic value of 1, correct?

9 A Yes, that's correct.

10 Q And when the output of OR gate 112 is 1,
11 inverter 142 has an output value of 0, correct?

12 A That is correct.

13 Q And the ZC latch S set receives the output of
14 inverter 142, correct?

15 A That is correct.

16 Q And the ZC latch S receives output of 142,
17 which under the parameters shown in your row 5 sets the
18 ZC latch S input to the logic value of 0, correct?

19 A Yeah, the output -- what I've shown here is
20 the -- under the condition where 1 -- from -- 122 is
21 high and the output of 112 is a 0, then I'm going to
22 propagate an output out of 132 brown, which is high,

1 which is what I show in the table.

2 Q You want to check that again?

3 A This is line 5, right?

4 Q Yeah.

5 A And I have orange as a logic 1. And the output
6 of 112, which is yellow, is a 1. That gives you a 0 to
7 the reset, gives you a 1 to the set, which is blue, and
8 that gives you a 1 output to the brown.

9 Q So 122 is high?

10 A Correct.

11 Q 112 output is high, right?

12 A 112 output is high, which gives you a 0 --
13 excuse me -- a 0 to the blue. And under that condition
14 that you just stated, we have a 0 to the blue as well as
15 a 1 to the reset, which is a 0.

16 So it's reset at one point in time, and then
17 it's set at another point in time.

18 Q Zero to the set, right?

19 A In this condition, it's a 0 to the set under
20 the one that you just framed, yes.

21 Q So the ZC latch S receives output of inverter
22 142, which, if you look at the parameters shown in

1 row 5, sets the ZC latch 132 S to a value logic of 0,
2 correct?

3 A That is correct.

4 Q S equals 0 and R equals 1 should be Q equals 0,
5 right?

6 A The Q equals 0 is depending upon -- excuse me.
7 When you follow through with the timing, it
8 eventually will be 0. It will be changed from a 1 to a
9 0 based upon the reset timing.

10 Q Is there any timing in your table?

11 A Oh, I don't show any timing in the table, no.
12 This is a condition -- this is a conditional table that
13 shows that the 122 itself and its data states are not
14 reflected in the green, which is a separate signal, and
15 does not correspond one-to-one to the orange. That was
16 the import -- that was the import of the table.

17 Q Are the conditions that S equals 0, R equals 1?

18 A The conditions you set was the 122 is high.
19 And when 122 is a logic 1, that's going to -- when that
20 transition occurs, it's going to not change the value on
21 the set. It'll be a 0 on the set, if that's what you're
22 asking.

1 Q So looking at your static table, latch S equals
2 0 and R equals 1, right?

3 A Under that condition, S equals 0, R equal 1.

4 Q That's what's in your table, right?

5 A That is correct.

6 Q And does a reset input to a latch reset Q to 0?

7 A Yes. It will take the output of Q, which is at
8 the 1 state, and then under this condition, when there's
9 a transition, then it will reset it to a 0 state.

10 Q All right. So Q -- a Q equals 0, right?

11 A When the -- when the transition occurs, yes, it
12 will be a 0.

13 Q But there's no transition shown in your table,
14 is there?

15 A Well, it's a logic table. There's not -- it's
16 not a logic table that is showing time domain. It's a
17 logic table, just showing a condition.

18 And there will be a condition in which 122 goes
19 high in which the output is still high. And at some
20 point later, after the logic is invoked, which is the
21 OR gate 112, the OR gate 136, the inverter 142, and the
22 AND gate 134, when all of that at a time delay occurs,

1 then you're going to get a transition on the output Q,
2 which will be a logic 0 at that time.

3 But they're not -- that will be a -- at a
4 certain point in time delay, there will be a 0 output on
5 that Q.

6 But it's not -- it doesn't correspond to the
7 122 because it's a different signal occurring at a
8 different time. They do not -- they do not correspond.
9 One is slave to the other, but they do not correspond.

10 Q Did you qualify this -- your table this way in
11 your declaration?

12 A I qualified in paragraph 84 that the -- looking
13 at the 122 -- the -- well, excuse me -- looking at the
14 green signal is not only logically dependent upon the
15 orange signal 122, but it is also dependent upon the
16 minimum offset -- minimum off-time output 110 aqua and
17 the output of the ZC latch 130 brown.

18 Consequently, one cannot define the state of
19 the green signal output based solely on the state of the
20 orange signal.

21 And then I said:

22 "Further, it is clear from the

1 logical arrangement between the orange
2 signal and the green signal that the two
3 signals' respective transitions between
4 one state to another state do not occur
5 at the same time since the green signal
6 output depends in part upon the state
7 transition of the orange signal."

8 So, yes, I did describe it.

9 Q Okay. So this is a static table, correct?

10 A I'm not sure what your use of the word "static"
11 is. It is a particular table. It represents a
12 condition under one set of conditions.

13 Q And you agree that S equals 0 and R equal 1,
14 right?

15 A Under that condition, yes.

16 Q And at this state, Q equals 0, right?

17 A Under that particular state, Q would equal 0 at
18 some time delay from when 122 goes to a logic 1, yes.

19 Q All right. But that's not what's shown in your
20 truth table, is it?

21 A Sir, once again, you have to look at the logic
22 table in light of paragraph 84, which I have described

1 the transitions.

2 I've also stated in paragraph 84 that there's
3 not a one-to-one correspondence between the output of
4 122 and the green line that goes to the gate of 82.
5 They're different, and they depend upon different set of
6 conditions.

7 And so at some point you may have the two
8 aligned at one delayed from the other, and other times
9 you may not. Because there are multiple other signals
10 upon which the green control signal to 82 depends for
11 its logic -- it's not a one-to-one correspondence to the
12 signal 122. That's what paragraph 84 says.

13 Q So are you saying that we cannot interpret this
14 logic table without a timing diagram?

15 MR. BOMBACH: Objection. Form.

16 THE WITNESS: Again, when I look at the logic
17 table, the very first words in paragraph 84 is:

18 "This truth...illustrates that the
19 green signal is not only logically
20 dependent upon the orange signal 122,
21 but...is also dependent upon the minimum
22 off-set [sic] output 110...and the

1 output of the ZC latch 130..."

2 I've made that statement. I've clearly
3 described what that table is. And I've also indicate
4 that it represents delays in transitions, and it just
5 further elaborates -- explains the fact that there is
6 not a one-to-one correspondence between the output 122,
7 the orange signal, and the input to the gate 82, the
8 green signal.

9 84 -- paragraph 84 explains the table in
10 detail.

11 BY MR. GRAY:

12 Q Turning your attention to paragraph 85, you
13 give an equation in paragraph 85. Do you see that?

14 A Yes, sir, I do.

15 Q Is there a variable in this equation that
16 represents timing?

17 A You know, I could show multiple different -- I
18 can apply this table at different times based upon
19 different values, but that -- it's a logic equation.
20 It's not a -- there's not a time listed in this table.
21 This is a logic equation.

22 You take that logic equation and you apply it

1 to the circuit of figure 3, then clearly you have a time
2 differentiation in terms of how that's applied.

3 Q Can I direct your attention to paragraph 71 of
4 your declaration?

5 A Sure.

6 Q And do you see on page 33 there's another
7 table?

8 A Yes. That's a representation of an AND gate.

9 Q Yeah. Is this table a static table?

10 A It is -- again, I'm not sure what you mean by
11 "static." It is a table that represents the -- the
12 logic output based upon input -- logic output F based
13 upon inputs A and B.

14 And so whenever any one of these rows of inputs
15 occurs over time, you will get that kind of a response
16 characteristic because there's AND gates.

17 So, in quotes, it's a static table in terms of
18 it represents what can occur at the time an A and B
19 input are of a certain value, what the output would be.

20 But that means that over time there could be
21 different values of the output, dependent upon that
22 condition at that time.

1 Q Right. But there -- so there's no timing in
2 this table in paragraph 71?

3 A It's understood by designer that you employ
4 this particular AND gate in a design, when the signals
5 are sent at a particular time at the inputs A and B to
6 this AND gate, then you are going to receive that type
7 of a logical output at that time.

8 Q So in reading your declaration, how should a
9 person of skill in the art interpret a table when one
10 has timing and one does not?

11 A Again, you're mixing words here. The logic
12 table represents the way a particular circuit responds
13 when inputs are at a particular position at a particular
14 time. That's the way logic works.

15 So I'm not trying to -- I'm certainly not
16 indicating that I'm using no time associated with one on
17 page 33 versus time on paragraph 84 on page 40. I'm
18 just indicating with paragraph 84 how that particular
19 circuit, when implemented, operates.

20 Q Okay. Let's turn your attention to row 6 of
21 the table on page 40 of your declaration.

22 A Row 6. Okay.

1 Q That's the bottom row.

2 A Okay.

3 Q In row 6 of your logic table shown on page 40
4 of your declaration, the output 122 annotated in orange
5 is given the value of 1, correct?

6 A Yes, that's correct.

7 Q And the gate of transistor 124 receives the
8 output of 122, correct?

9 A Yes. Down the minimum off-time timer, yes,
10 that's correct.

11 Q And the transistor 124 is an n-channel MOS
12 transistor, correct?

13 A Correct.

14 Q And the transistor 124 is on when the value at
15 the gate is logic value 1 and when output 122 is logic
16 value 1, correct?

17 A Yes.

18 Q And the drain terminal of transistor 124 is
19 driven to ground while transistor 124 is on, correct?

20 A It is.

21 Q And the noninverting input of comparator 106 is
22 connected to the drain of transistor 124, correct?

1 A Correct.

2 Q And when transistor 124 is on, the output of
3 comparator 106 is logic value 0, correct?

4 A Correct.

5 Q And the output of comparator 106 is the output
6 110 of the minimum off timer of 56, which you've
7 annotated in aqua, right?

8 A Yes. I've indicated in aqua is a "don't care"
9 because it's an OR gate. So since 122 we've already
10 a priori stated is a logic 1, then if that's a logic 1,
11 the OR gate is going to respond to that regardless of
12 what the state of 110 is.

13 So the minimum off timer is not even part of
14 this equation at all under the constraints --

15 Q Okay. As --

16 A -- that you've just placed.

17 THE STENOGRAPHER: "Under the" what?

18 THE WITNESS: Under the constraints that you've
19 just placed or just put in place.

20 BY MR. GRAY:

21 Q As shown in row 6 of your logic table, can you
22 explain how the output 110 of the minimum off timer 56

1 can have a logic value of 1 when the logic value in your
2 table also has a logic value of 1?

3 A Again, if you have the logic value of 1 on the
4 orange, it controls the state of OR gate 112 to deliver
5 a logic 1 on the output of that OR gate, which is
6 yellow. And it's irrespective of anything that occurs
7 on 110.

8 So 110, if it's during the -- if you'll notice,
9 the 122 orange going high is going to begin the
10 discharge in the minimum off-time timer, so at some time
11 later you will get a change in the result at 110.

12 But it doesn't matter because 122 already
13 rules -- governs the output of 112 to be a logic 1.
14 It's irrespective of what happens in the minimum
15 off-time timer for this particular state.

16 Q All right. So in comparator 106, when there's
17 an input of 0, there's a comparator output of 0, right?

18 A That's correct.

19 Q Not the one shown in your table, right?

20 A Incorrect because with the assumption that 124
21 has -- initially was off because 122 initially was
22 ground, was 0. So, therefore, that capacitor has been

1 charged generating a 1 output.

2 Now, at the time 122 transitions from a logic 0
3 to a logic 1, it immediately generates an output through
4 112 of logic 1 while 110 remains at a 1 because it's a
5 "don't care."

6 And then later, the minimum off timer is going
7 to show a discharge change in the state of 110 to a 0,
8 but it's a "don't care" because it's delayed and it's
9 out of -- it's out of the -- it just is a "don't care."

10 112 is -- can be slave to what on the input of
11 122 is a 1. It's going to generate an output of a 1
12 regardless of the current or the next state of 110.
13 It's a "don't care," which is what I indicated with the
14 asterisk.

15 Q So you're testifying that there's a time
16 element in row 6 as well?

17 A I'm indicating that -- I'm not -- again,
18 paragraph 84 describes that. But if you look at
19 paragraph 84, in light of the table in line 6, as it
20 applies to figure 3, which is what it does, is that the
21 state on the blue line 110 is a "don't care."

22 Whether it is a 0 or a 1 is irrelevant.

1 Whether the output of the comparator 106 is a 0 or 1, it
2 doesn't matter. Because 122, when it transitions, is
3 going to control the output of 112 regardless.

4 That's what's reflected in the chart. And
5 that's consistent with what's shown on circuit diagram
6 figure 3.

7 Q So when I look to your footnote that explains
8 the asterisk, it says that the value does not affect the
9 eventual green output; is that correct?

10 A That is correct. Under the condition where
11 orange 122 goes to a 1, it's going to control. But that
12 and the 110 is a "don't care." It's not part of the
13 equation at this point.

14 Q But the asterisk doesn't say that there's
15 anything that's going to change about the aqua column,
16 does it?

17 A What it says is -- is that it doesn't matter
18 where whether it's a 1 or a 0. It doesn't matter. I
19 mean, changes do occur in logic gates. They -- changes
20 do occur in the circuit of figure 3 at a time delay.
21 Once the discharge takes place, there's going to be a
22 change from a 1 to a 0.

1 At the time at which this is being propagated,
2 112 is ruled by 122 orange, period. And so regardless
3 of the state on 110 blue, it just doesn't matter. And
4 that's what I state in the table. It's what's in the
5 footnote.

6 Q But what you don't care about is the later
7 result. It's not the column entry that you don't care
8 about. It's not the aqua column entry that you don't
9 care about. It's the green column that you don't care
10 about?

11 A I don't understand that analysis. That
12 certainly is not consistent with what I've said. The
13 whole thrust of what I'm doing is showing you a
14 comparison between the state of 122 and the state of the
15 green signal that drives gate 82 in showing that they do
16 not correspond to each other and that the output logic
17 states that occur with green are different than the
18 output states that occur on the orange 122.

19 The table represents that. The circuit
20 represents that. And everything that I have said and
21 described is consistent with that point. So it's orange
22 versus green that I'm looking at.

1 Q All right. The aqua has a value, but you don't
2 care what it is?

3 A Yeah, I don't care what it is.

4 Q Okay. Let's turn your attention to row 3 of
5 your logic table on page 40 of your declaration.

6 A Okay.

7 Q Row 3 of the logic table shows that the yellow
8 annotated line has a logic value of 1 and the blue
9 annotated line has a logic value of 0, correct?

10 A This is line 1?

11 Q Row 3.

12 A Row 3. Excuse me. I'm sorry.

13 Okay.

14 Q And so it's a "yes"?

15 A Yeah, I mean, the table shows what these
16 signals are at that particular point.

17 Q And row 3 shows that the yellow annotated line
18 has a logic value of 1 and the blue annotated line has a
19 logic value of 0, right?

20 A What it shows under the condition where the
21 orange 122 is a 0, the yellow shows a logic 1 and the
22 blue shows a logic 0.

1 Q Okay. So row 3 shows that the yellow annotated
2 line has a logic value of 1 and the blue annotated line
3 has a logic value of 0, correct?

4 A That's correct, because the aqua -- under this
5 condition, the aqua line is a 1, which is going to
6 produce a 1 on the yellow line. That yellow line is
7 going to be inverted to the blue line, which gives that
8 a 0. The output of 142 is a 0. So that's correct.

9 Q So the blue annotated line represents the
10 output of inverter 142, correct?

11 A That's correct.

12 Q And so the blue annotated line represents the
13 set input to the ZC latch 132, correct?

14 A That's correct.

15 Q For the Q output of the ZC latch 132 to be a
16 logic value of 1, the set input must also be a logic
17 value of 1, correct?

18 A And it was a 1 because that's the value Q's
19 output. And so when we invert that set input, that says
20 the next time that the reset occurs, it's going to give
21 that other value.

22 Q So would you agree that there's an error in row

1 3 of your table?

2 A If you will notice under this conditional
3 line 3, I've stated the orange is a 0, which is
4 line 122, signal 122.

5 And if that logic 0 provides under that
6 condition a logic 0 to the AND gate 134, the reset value
7 is set to 0.

8 So under this condition, you've got the reset
9 at 0, which means it's not going to reset, and the set
10 is set to 0, which is not going to reset.

11 So the initial condition is the output brown Q
12 is a 1. Eventually it will be reset to a 0, but right
13 now, under this condition, it is a 1.

14 So, no, I disagree. I think it's right.

15 Q So there's a time element in this row as well?

16 A Well, again, when you say "time element," logic
17 applies to a particular condition at a set point in
18 time, period. And that condition -- that logic works in
19 a time domain when it's put into a circuit.

20 And so when you have different conditions as
21 inputs to that circuit, then you will transition to
22 different outputs.

1 The thrust of this is that the output 122,
2 which is the signal out of the PWM latch, does not
3 correspond to the green signal that drives the gate of
4 82. They're different signals occurring at different
5 times with different values. That's the thrust of what
6 this table is showing.

7 And I could provide other tables that show
8 other conditions that occur. But the -- but all that
9 does is continue to elevate the fact that the two
10 signals are not corresponding to each other because the
11 signal that drives the gate of 82, which is the green
12 signal, depends on a lot other factors than just the
13 output of 122.

14 They're not the same. They don't correspond to
15 each other. Their logic results are not the same. And
16 there's a time delay between them. They're different
17 signals. That's the point of that --

18 Q So you're saying this table -- oh, I'm sorry.
19 Continue.

20 A I'm sorry. That's the point -- that's the
21 overbearing point of the table is there's a -- there's a
22 difference between the two signals.

1 One does not correspond to the other. One does
2 not depend directly and only from the other. There are
3 other considerations that takes place.

4 And, yes, I could elaborate -- excuse me --
5 other conditions and add additional rows to this table,
6 which, again, just continues to establish the fact that
7 the two are different signals, two being 122 orange and
8 the gate driver, green -- the green signal drives gate
9 82.

10 Q So you're saying that this table does not
11 represent a specific moment in time?

12 A It represents a condition. And we live in a
13 four-dimensional world. And when you have a condition,
14 a set of structural conditions, that occurs at a
15 partic- -- how does that respond at a given time under
16 certain circumstances?

17 So you take the static aspect of the -- of the
18 logic and you -- and -- based on the different inputs at
19 different times, you will get different results.

20 Q So does this table represent a specific moment
21 in time?

22 A It represents a specific condition, a specific

1 set of conditions. And there are other conditions, but,
2 again, the more rows that I would add to this table to
3 look at other conditions just further differentiates the
4 green column from the orange column.

5 Q So if R equals 1 and S equals 0, does Q equal
6 0?

7 A If R is equal 1, Q is -- Q will become 0 when R
8 goes to 1. That's on the ZC latch 132, if that's what
9 you're referring to.

10 Q And when you use the word "will become," what
11 does that mean?

12 A Well, for instance, so this statement I'm going
13 to make would apply to latch 132 would also apply to the
14 latch 116 that drives the signal 122.

15 If I provide a logic 1 to the set input, it
16 will create, with that flip-flop, a set 1 -- it will --
17 it will create a 1 on the output Q in both instances.

18 If I have a reset signal that goes to 1, it's
19 going to reset that output Q to a logic 0 even if the
20 set input's still sitting at a 1. It's the reset
21 control.

22 So you can have -- you have a condition on a

1 latch where you have reset it.

2 Q All right. So when --

3 A For different conditions, different ways in
4 which it operates. And obviously whenever it operates,
5 there's a time element, but it's basically a set of
6 conditions gives you a result.

7 Q All right. And in the condition when R equals
8 1 and S equals 0, does Q equal 0?

9 A If R equals 1, Q will equal 0. It's a reset.

10 Q A latch is a memory element, correct?

11 A It can be viewed as a type of memory element.

12 Q Figure 3 of Tateishi includes ZC latch 132,
13 correct?

14 A That's correct.

15 Q And do I understand your testimony being that a
16 static truth table cannot fully describe the operation
17 of a logic circuit that contains a memory element?

18 A A logic table is a way in which one describes
19 the logical correspondence between an output and an
20 input of a particular logic circuit.

21 And it does describe that, does define it.

22 It's the way it operates.

1 Q So are you saying that a static truth table can
2 fully describe the operation of a logic circuit that
3 contains a memory element?

4 A If in that logic table you include all the
5 combinations.

6 Q At a single point in time?

7 A Well, when a condition -- when a set of
8 conditions occur, that will be the result. And that
9 will be the result whether it occurs in time 1 or time 2
10 or time 3 or time N.

11 Q A static truth table, like the one in your --
12 on page 40 of your declaration, can only describe
13 combinatorial logic circuits that do not contain memory
14 elements, right?

15 MR. BOMBACH: Objection. Form.

16 THE WITNESS: I don't understand that question.
17 You can define a logic based upon a memory element too.
18 If it's a memory element that stores a piece of
19 information that cannot be upset or changed, then you
20 may have other constraints, but here we're talking about
21 a flip-flop.

22 We're talking about something where you

1 establish an input and it sets to an output. And if you
2 submit a reset to it, then it will automatically force a
3 reset, which is a 0 output, to that memory element.

4 BY MR. GRAY:

5 Q Okay. So --

6 A So a logic table can describe that memory
7 element.

8 Q So if S equals 1 and R equals 0, Q equals 1,
9 right?

10 A Once you propagate S -- once you propagate a 1
11 to the S input, then it will generate a Q output equal
12 to 1.

13 Q And if S transitions to 0, while R equals 0, Q
14 will remain a 1, right?

15 A If you're using a standard flip-flop, then the
16 output Q is going to reflect what the input S is. So
17 you could -- if you change the S to a 0, it will go to a
18 0 on the output on a standard flip-flop.

19 Q All right. You've mentioned a flip-flop a
20 couple times here, but we're talking about a latch right
21 now, aren't we?

22 A Latches are implemented with flip-flops.

1 Q And --

2 A That's the most basic form of a -- of a latch.

3 Q And the S there is the memory in the latch?

4 A S is an input to the latch.

5 Q It's the memory in the latch?

6 A Well, it stores that input.

7 Q Is a flip-flop implemented with two latches
8 internally?

9 A Logically it describes back-to-back NAND gates,
10 but it can be implemented with one flip-flop.

11 Q You sure about that?

12 A Yes, I am.

13 Q In your declaration, did you provide a state
14 diagram?

15 A No, I don't believe so.

16 Q Okay. All right. So looking again at figure 3
17 in Tateishi, OR gate 112 receives signal output 122 and
18 signal output 110, correct?

19 A That is correct.

20 Q And when signal output 110 is logic value 0,
21 the signal output of OR gate 112 is equal to the signal
22 output 122, correct?

1 A The output 122 would be a -- would be an output
2 signal that corresponds to the input signal logic state
3 122.

4 Q And when you say "corresponds to" --

5 A Just so -- just so we're clear, in a logic to
6 gate like 112, the input is not passed through to the
7 output. They're not the same signal.

8 So the signal output of 112 would be responsive
9 to the input state of 122, assuming that 110 is a
10 logic 0.

11 Q But it would -- they would be equal, right?

12 A What do you mean "equal"?

13 Q So when the signal output 110 --

14 THE STENOGRAPHER: Sorry. Did you say, "It
15 would be equal," Mr. McAlexander?

16 THE WITNESS: I just asked him a question,
17 "What do you mean by 'equal'?"

18 BY MR. GRAY:

19 Q So when the signal output 110 is logic value 0,
20 the -- the signal output of OR gate 112 is equal to the
21 signal output 122, correct?

22 A Well, if you have a condition where the signal

1 input, not output, but the signal input 110 to OR gate
2 112 is a 0, and the -- and the logic state of 122 input
3 is a 0, then 112 reflects a combination of both of those
4 states being a logic 0.

5 So that output 112 would reflect both states,
6 110 and 122. But under the condition where 110 is a
7 logic 0 and 122 transitions to a logic 1, then the
8 output 112 would be a output signal that corresponds to
9 the -- to the logic state of the input 122, which is a
10 logic 1.

11 Q All right. When the signal value at output 122
12 is a logic value of 1, the signal at the output of 112
13 is also logic 1, correct?

14 A That is correct, yes.

15 Q And when a signal at output 122 is logic 1, the
16 signal level at the output of OR gate 136 is logic 1,
17 correct?

18 A Yes, that's correct.

19 Q And when the signal levels at the two inputs of
20 AND gate 134 is logic 1, the signal level at the output
21 of AND gate 134 is also logic 1, correct?

22 A Yes, that's correct.

1 Q And when the signal level at output 122 is
2 output -- let me start over.

3 When the signal level at output 122 is logic 1,
4 the signal level at the output of inverter 142 is
5 logic 0, correct?

6 A That is correct.

7 Q All right. And quick question. Regarding your
8 use of "signal," you're saying that a signal is a node,
9 correct?

10 A No. When we -- when you asked this question
11 before, I said a node is a connection point to a
12 circuit. Could be a connection point to a wire. It
13 could be the output of a transistor. Could be the input
14 of a transistor. That would be a node. It's a circuit
15 node. It's a point in a circuit.

16 So it's a structure but not a signal. A signal
17 is what you propagate from or to a node across some type
18 of conductive mechanism, such as a wire.

19 Q If you have a 1 going into an OR gate and the
20 output is a 1, is it a different signal?

21 A If you have a -- well, a 1 is a logic state.
22 If you have a signal that is at a voltage value

1 that's -- corresponds to a logic 1 on the input to an
2 OR gate, I think you said?

3 Q Yes, sir.

4 A Then the output of that OR gate is going to be
5 a different signal that's generated by the OR gate that
6 corresponds also to a logic 1.

7 But the input to an OR gate is not passed
8 through to the output. The input to the OR gate is an
9 input to gates in the transistor control gates that then
10 the OR gate generates a separate output signal based
11 upon that input.

12 Q So then the output of the OR gate is its own
13 signal?

14 A It's a separate signal.

15 Q Okay. So --

16 A For -- let me -- let me give you an example
17 because I want to make sure we're clear.

18 If you look at the circuit diagram on page 39,
19 figure 3, and look over at the far right at the -- at
20 the upper -- high-side driver, transistor 12, what --
21 the input to the transistor 12 is the input to the gate
22 of 12.

1 That's a signal line that comes out of that
2 buffer circuit. It's a NAND. And the cross-conduction
3 control generates an output. It gets buffered in the
4 high-side driver box by that little triangle. And then
5 it provides an input to the gate of 12. That's an
6 input.

7 The output of 12 is the switch signal 22. But
8 between the input of the gate 12 and the output source
9 or drain -- source in this case of that transistor is an
10 insulator. The two do not -- the input does not
11 propagate to the output. They are insulated from each
12 other. They're buffered from each other.

13 So the input creates a logic state at the input
14 to a circuit. The circuit then generates its own output
15 signal separate from that input. It's not a
16 pass-through. That's the same thing with an inverter,
17 the same thing with an AND gate, the same thing with an
18 OR gate.

19 Q Okay. Look at the low-side driver, block 54.

20 A Okay. Got it.

21 Q How many signals are shown in this block?

22 A Oh, my God. Low-side driver. In that box 54?

1 Q Yes, sir.

2 A You at least have an input signal to the -- the
3 triangle represents a buffer. If you -- the input to
4 that triangle is a signal. The output of that triangle
5 is a signal.

6 You at least have two signals -- there could be
7 more but at least have two from the diagram.

8 Q Sounds like signals are nodes; is that correct?

9 A No. The output of the buffer -- see the
10 triangle that has VDD as the power source to it?

11 Q I do.

12 A The right side of that triangle represents an
13 output of that buffer. That's an output node.

14 If you move over to transistor 14, you have a
15 gate. That's an input to that gate. That's a node.
16 What's connecting the two together is some type of
17 conductive mechanism. Could be polycrystalline silicon
18 as a semiconductor. Could be a metal. Let's just say
19 it's a conductor, like a wire.

20 And so you have a transmission mechanism
21 between the two, between the output node of the buffer
22 and the input node of the gate.

1 Those are structural components that are part
2 of the circuit. The signal is what's propagated from an
3 output to an input across the conductor. So signal and
4 node are not the same.

5 Q So how many nodes are in 54 -- in block 54?

6 A Well, there's more than is shown here because
7 it's a diagram. But you have a node that on the input
8 to transistor 14, you have a drain on transistor 14,
9 which is the upper side of the transistor.

10 You have a node on the -- on the bottom side of
11 the transistor that's connected to the ground. You have
12 a node on the output of the buffer, which is powered by
13 VDD. You have an input node to that buffer.

14 And I think I said you have a node also that's
15 connected from the buffer to ground. So --

16 Q So let's look only inside block --

17 A You also have a node connected to power, so
18 you've got one, two, three --

19 THE STENOGRAPHER: Sorry, you overlapped.
20 Could you repeat that?

21 THE WITNESS: You also have a node connected to
22 the power VDD. So you got one, two, three, four,

1 five -- at least -- you have at least six nodes in that
2 particular section.

3 BY MR. GRAY:

4 Q Only inside of block 54, how many nodes are
5 there?

6 A Inside block 54, you have at least four.

7 Q And turning back to an answer you gave a minute
8 ago, are you saying that the gate of 14 is not the same
9 node as the output of the buffer?

10 A No. They are two nodes electrically that are
11 connected together through some type of a conductor, in
12 this case via metal or a semiconductor type of trace or
13 combination thereof. They're displaced from each other.
14 They're not on top of each other. So they're not the
15 same. Electrically they may be similar, but they're not
16 the exact same, not the same node.

17 Q Okay.

18 A Now, when you do this in a CAD drawing, they're
19 separate structural nodes. When you do this in
20 electrical -- in electrical diagram, when you're doing
21 electrical stimulation, if there's not a large amount of
22 a resistance or capacitance difference between the

1 output of the buffer and the input of the gate 14, you
2 might represent them electrically as a common node,
3 electrically.

4 So it depends upon the framework of your
5 context as to what you call or don't call a node.
6 It's -- but it's structure.

7 Q Well, in the context of when we agreed earlier
8 that 122 is a node, in that context.

9 A If I ever said that, the answer's no. The
10 output of the latch 116 is an output node, which
11 generates the signal Q. 122 represents a -- is a -- is
12 a signal. It's representing the signal that's
13 propagated from that output of the latch to other
14 circuitry.

15 But the signal itself is not a node.

16 Q Okay. When the signal level at the S input of
17 ZC latch 132 is logic 0 and the signal level at the R
18 input of ZC latch 132 is logic 1, the Q output of the
19 ZC latch 132 is a logic 0, correct?

20 A That's correct.

21 Q And when the signal level at the Q output of
22 ZC latch 132 is 0 and the signal level of output 122 is

1 logic 1, the signal level at the output of the pink AND
2 gate will be logic 0, correct?

3 A Correct. That will become logic 0 once it's
4 logically analyzed, yes.

5 Q So when the two signal levels at the inputs of
6 the pink -- well, let me see. Let me look at this. Got
7 to make sure I'm talking to the right one.

8 So when the two signal levels at the input of
9 the R -- OR gate that drives the gate of transistor 82
10 are both logic 0, correct?

11 A All right. So that pink OR gate that has the
12 two inputs, if they're both 0, that's your question?

13 Q Yes.

14 A Then the green output to gate 82 will also be a
15 0 logic.

16 Q And when the signal levels at the two inputs of
17 this OR gate are logic 0, the signal level at the output
18 of the OR gate is logic 0, correct?

19 A Yes.

20 Q And when a signal level at the output of this
21 OR gate is 0, transistor 82 will be off, right?

22 A In this diagram of figure 3, that's correct.

1 Q Okay. Let me turn your attention to claim 1 of
2 the '377 patent.

3 A If I may before I forget it, when I was
4 preparing, I noticed that my final document, for some
5 reason, when it created this as served PDF, did not
6 highlight a couple of figures correctly.

7 Can I point those out to you just so it's in
8 the record?

9 Q Sure thing.

10 A Yeah. This is in paragraph 108 and 109.

11 What I said in paragraph 108 with regard to
12 figure 3, in the last sentence of 108, I said:

13 "For example, Figures 3" --

14 "Figure 3's circuit contains logic shown
15 in aqua..."

16 And I noticed in the PDF that was rendered, the
17 aqua's missing. I don't know why, but it is. So I just
18 want to represent that if you drew an aqua rectangle
19 between the right side of that hash box 50 and the left
20 side of the hash box 62 -- in other words, it's that
21 logic circuitry that's down the middle -- that was what
22 was supposed to be in aqua color.

1 Q Okay. Anything else?

2 A And the other one is on page -- in paragraph
3 109, also I show -- show in aqua the control signals.
4 If you look on page 51, the box that was supposed to be
5 aqua color is basically that cir- -- that logic
6 circuitry that sits up above the -- all the circuitry
7 sits up above that box 76.

8 Q Anything else?

9 A And the only other thing was in both of these,
10 the high-side, low-side driver switches, they were
11 supposed to be in yellow. That's it. Again, this
12 description in the language covers it, but I just want
13 to make sure it was clear when I have no idea why it
14 didn't print, but it didn't.

15 Q Okay. Looking at the time, is this a
16 convenient time for a lunch break or would you like to
17 continue going?

18 A Wow. Quarter to 3:00. I don't know. Whatever
19 you want to do is fine with me.

20 MR. GRAY: Miguel, what do you want to do?

21 MR. BOMBACH: It's up to you. Up to you and
22 Joe.

1 MR. GRAY: Why don't we go for another half
2 hour and stop then.

3 THE WITNESS: Okay.

4 BY MR. GRAY:

5 Q So turning your attention to claim 1 of the
6 '377 patent?

7 A Okay.

8 Q And -- got to figure out where my language is
9 here.

10 Okay. So in, you know, limitation 1[B2], so
11 that's where the language is.

12 "...based on the switching signal
13 and the control signal, the input
14 voltage sensing circuit generates an
15 input voltage sensing circuit at the
16 output terminal."

17 Do you see that language I'm talking about?

18 A Yes, I do.

19 Q So this claimed control signal controls the
20 input voltage-sensing circuit to generate an input
21 voltage-sensing signal, correct?

22 A Yeah, the -- this claim element as to the input

1 voltage-sensing circuit has two inputs, one connected to
2 switch -- switching signal. The second one receives a
3 control signal. And it generates an input
4 voltage-sensing signal at its output. That's what it
5 says.

6 Q Okay. And then turning to limitation 1[E] of
7 claim 1, where it says:

8 "...based on the input voltage and
9 the control signal, the power stage
10 generates the switching signal."

11 Do you see that?

12 A Yes, the power stage generates the switching
13 signal.

14 Q So this claimed control signal controls the
15 power stage to generate the switching signal, correct?

16 A That is correct.

17 Q Okay. Now, turning your attention to column 5
18 of the '377 patent and lines 21 through 23.

19 Do you see where it says:

20 "The switch K is coupled to the
21 capacitor CTON in parallel and
22 controlled by the control signal Q"?

1 A Yes.

2 Q So the specification here describes the control
3 signal Q as controlling switch K, correct?

4 A That's correct. The control signal that would
5 be generated.

6 Q Okay. So turning your attention to column 8
7 and look at lines 32 through 34. Do you see that?

8 A Yes, I do.

9 Q And this is referring to figure 11, correct?

10 A That is correct.

11 Q And you see where it says:

12 "The control signal Q controls the
13 high-side switch Q1, and the
14 complementary signal Q prime of the
15 control signal Q controls the low-side
16 switch Q2."

17 Do you see that?

18 A Yes, I see that.

19 Q So the specification here describes a control
20 signal Q as controlling the high-side switch Q1,
21 correct?

22 A That's correct.

1 Q So in the context of the '377 patent, you would
2 agree that a control signal is a signal that controls
3 other circuit components, correct?

4 A I would agree with that, yes.

5 Q Okay. So now turning your attention to
6 Tateishi. And if you would turn to paragraph 51, which
7 I'm nowhere near.

8 Yeah. You see where in paragraph 51 it says:

9 "The output 122" --

10 A 51 or --

11 Q -- "also drives" --

12 A 51 or 61?

13 Q Five-one.

14 A Okay. Thank you.

15 Q So it's in reference to figure 3. So do you
16 see where in paragraph 51, it says:

17 "The output 122 also drives the
18 discharging transistor 82 in the on-time
19 timer 50 through an inverter 126, so
20 that during an off-time, the capacitor
21 Con 74 is discharged to ground 20 and
22 during an on-time, the discharging

1 transistor 82 is turned off allowing the
2 capacitor Con 74 to be charged
3 by...current source 76."

4 Do you see that?

5 MR. BOMBACH: And I'll object to this question
6 on the basis of form and being outside the scope of
7 Mr. Alexander's -- McAlexander's declaration.

8 THE WITNESS: All right. You began reading in
9 paragraph 51, about two-thirds of the way down, "The
10 output 122"?

11 BY MR. GRAY:

12 Q Yes, sir.

13 A Okay. The output latch -- turn on --

14 THE STENOGRAPHER: If you're going to read,
15 read louder for me.

16 THE WITNESS: I was mumbling to myself. Sorry
17 about that. I was just reading the --

18 BY MR. GRAY:

19 Q It's at the bottom of that paragraph 51. It's
20 like the last sentence.

21 A "So that during an off-time, the
22 capacitor Con 74 is discharged to

1 ground...during on-time" -- "during
2 an on-time, discharge transistor 82
3 is turned off allowing the
4 capacitor...to be charged."
5 Okay. I see that.

6 Q So the output 122 drives discharging
7 transistor 82, correct?

8 MR. BOMBACH: And same objection with respect
9 to scope.

10 THE WITNESS: Well, I have to interpret the
11 paragraph 51 in light of figure 1, which is describing,
12 and 122 does not provide any direct drive to 82. It
13 does it through other logic.

14 But at the time that 122 is generated to the
15 point at which 82 is activated, under that condition,
16 you're going to discharge the transistor -- or discharge
17 the capacitor.

18 And during the on-time, the discharging
19 transistor 82 is turned off. And it's correct. I mean,
20 the charging and discharging of that capacitor is going
21 to be dependent upon the on or off condition of gate 82.
22 And, in part, that's going to be directed by the state

1 of 122. But clearly there's other logic that's
2 involved.

3 BY MR. GRAY:

4 Q So the output 122 controls discharging
5 transistor 82, correct?

6 MR. BOMBACH: Objection. Scope.

7 THE WITNESS: It provides an input to logic
8 that controls 82, but that logic that controls 82 is
9 also dependent upon other signals. It's not just 122
10 alone.

11 BY MR. GRAY:

12 Q Okay. And:

13 "The output 122...drives the
14 discharging transistor 82 in the on-time
15 timer 50 through an inverter 126."
16 Correct?

17 MR. BOMBACH: Same objection. Scope.

18 THE WITNESS: Where are you reading now,
19 please? It's line -- excuse me:

20 "The output 122 also drives the
21 discharging transistor 82 in the on-time
22 timer through an inverter 126..."

1 Yes, this is with regard to figure 1. That's
2 correct.

3 BY MR. GRAY:

4 Q You would agree that after output 122 passes
5 through inverter 126, that output 122 controls
6 discharging transistor 82, correct?

7 MR. BOMBACH: Objection. Scope.

8 THE WITNESS: Well, 122, in light of paragraph
9 51 and figure 1, which it refers to -- 122 provides a
10 logic state that is inverted by 126 that then provides
11 an input to the control of transistor 82 in figure 1.

12 BY MR. GRAY:

13 Q Okay. Turning to your declaration, at
14 paragraph 69 -- so I'll give you a minute to get there.

15 A Appreciate it.

16 You said paragraph 69?

17 Q Six-nine, yes, sir.

18 A Okay.

19 Q And now look at figure 3 below it, which would
20 be annotated.

21 A I see that.

22 Q And you highlight two logic gates in figure 3,

1 right --

2 A Yes.

3 Q -- in pink?

4 A Yes, that's correct.

5 Q And now returning to Tateishi, figure 1,
6 figure 1 does not include these two logic gates,
7 correct?

8 MR. BOMBACH: Objection. Scope.

9 THE WITNESS: No, figure 1 is a separate
10 embodiment from figure 3.

11 BY MR. GRAY:

12 Q Does figure 1 contain these two logic gates?

13 MR. BOMBACH: Objection. Scope.

14 THE WITNESS: The two pink logic gates are not
15 in figure 1. Figure 1 is a different embodiment.

16 BY MR. GRAY:

17 Q Okay. And, in fact, in figure 1, the logical
18 value of signal 122 is unchanged until it passes through
19 inverter 126, correct?

20 MR. BOMBACH: Objection. Scope.

21 THE WITNESS: 122 does not pass through 126. I
22 described that before. If you could maybe rephrase your

1 question.

2 BY MR. GRAY:

3 Q In figure 1, the logical value of signal 122 is
4 unchanged until it passes through inverter 126, correct?

5 MR. BOMBACH: Objection. Scope.

6 THE WITNESS: Again, the logic value of 122
7 remains unchanged. It is the logic value of 122. Now,
8 there is an inverter that receives the input of 122 and
9 generates a separate signal output to the gate of 82
10 that's an inversion of that.

11 So there's a state change on the output of the
12 inverter, but the state on 122 remains its state.

13 MR. GRAY: Okay. I'm at a stopping point. Why
14 don't we break for lunch.

15 (Lunch recess taken from 12:51 p.m. to
16 1:49 p.m.)

17 - - -

18 EXAMINATION

19 (resumed)

20 BY MR. GRAY:

21 Q Mr. McAlexander, I've uploaded Exhibit 2001,
22 which is your declaration, into the chat box.

1 Would you please download that and take a look
2 at it, sir?

3 A Okay. I have 2001 in front of me.

4 Q Can you tell me what Exhibit 2001 is, please,
5 sir?

6 A It's my initial declaration in this IPR matter.
7 I signed it on page 27. It's dated the 28th day of
8 October 2024.

9 Q Can I direct your attention, please, to the top
10 of page 22 of your declaration?

11 A Okay. I'm there.

12 Q Okay. So you see at the top of the page is a
13 continuation of paragraph 46, which began on the
14 preceding page?

15 A Yes.

16 Q You see the language:

17 "The zero-crossing comparator 64
18 detects this zero crossing and turns off
19 the low side switch 14 through the zero
20 crossing SR latch 132"?

21 A Yes.

22 Q So you're saying that the zero-crossing

1 comparator turns off the low-side switch 14, correct?

2 A That's correct.

3 Q All right. Continuing further:

4 "At the same time, the precharging
5 transistor 150 is turned off and the
6 discharge switch 82 is turned on..."

7 Correct?

8 A Correct.

9 Q And is the figure shown below this paragraph
10 the figure that we're talking about here?

11 A Yes, it is.

12 Q And there is intervening logic between the
13 zero-crossing comparator 64 and the low-side switch 14,
14 correct?

15 A Yes, there is.

16 Q Despite the intervening logic, the
17 zero-crossing comparator 64 controls the low-side
18 switch, correct?

19 MR. BOMBACH: Objection. Form.

20 THE WITNESS: Well, the zero-crossing
21 comparator provides an input to logic circuitry that
22 does provide a controlling input to the low-side switch

1 14.

2 There are other conditions, but under the
3 condition where you have a zero crossing, it does
4 provide a reset input to the latch 132, which propagates
5 to turn off transistor 14, the low-side driver.

6 MR. GRAY: All right. Let's go off the record,
7 take a five-minute break. I think I'm done, but I want
8 to check my notes.

9 THE WITNESS: Okay.

10 (Recess taken from 1:53 p.m.
11 to 1:58 p.m.)

12 MR. GRAY: Mr. McAlexander, thank you for your
13 time. We have no further questions at this time.

14 THE WITNESS: Thank you for your time.

15 MR. BOMBACH: And no questions from patent
16 owner. Thank you.

17 THE STENOGRAPHER: Really quickly, orders for
18 the transcript. Would you like regular two-week
19 delivery?

20 MR. GRAY: No, ma'am, I need expedited
21 delivery.

22 THE STENOGRAPHER: What date do you need it by?

1 MR. GRAY: Well, if you give me the rough
2 today, I think my brief's due on the 14th. So Monday?

3 THE STENOGRAPHER: Okay. And Mr. Bombach?

4 MR. BOMBACH: Yes.

5 THE STENOGRAPHER: Do you want a copy?

6 MR. BOMBACH: Yeah, please.

7 THE STENOGRAPHER: Do you need a rough draft?

8 MR. BOMBACH: No.

9 THE STENOGRAPHER: And do you need expedited
10 delivery as well?

11 MR. BOMBACH: No, I do not.

12 - - -

13 (Signature having not been reserved, the
14 deposition of JOSEPH MCALEXANDER III
15 concluded at 1:59 p.m. PDT)

16

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WITNESS CERTIFICATION

CASE: REED SEMICONDUCTOR CORP. vs. MONOLITHIC POWER
SYSTEMS, INC.

WITNESS: JOSEPH MCALEXANDER III

DATE: July 1, 2025

JOB NO.: 589902

I, JOSEPH MCALEXANDER III, having remotely
appeared for my videoconference deposition on July 1,
2025, hereby certify under penalty of perjury under the
laws of the United States of America that the foregoing
is true and correct.

IN WITNESS WHEREOF, I have hereunto subscribed
my name this _____ day of _____ 201____, at
_____, _____.
(city) (state)

JOSEPH MCALEXANDER III

CERTIFICATE OF CERTIFIED SHORTHAND REPORTER

CASE: REED SEMICONDUCTOR CORP. vs. MONOLITHIC
POWER SYSTEMS, INC.
DEPOSITION DATE: JULY 1, 2025
JOB NUMBER: 589902

I, Marla Sharp, certified stenographic
reporter licensed in California, Oregon, and Washington,
hereby certify that the foregoing videoconference
deposition of JOSEPH MCALEXANDER III was taken remotely
before me on July 1, 2025; that the witness was remotely
duly sworn by me; that all of the testimony, colloquy,
and objections made were recorded stenographically by me
and thereafter transcribed, said transcript being a true
copy of my shorthand notes thereof; that review of the
transcript was neither requested nor waived before
completion of the deposition; () that the witness has
failed or refused to approve the transcript; and that I
am neither financially interested in the action nor a
relative or employee of any party.

In witness whereof, I have subscribed my name
and signature this date, July 6, 2025.



Marla Sharp, RPR, CLR, CCRR
CA CSR 11924, OR CSR 17-0446, WA CSR 3408

E R R A T A S H E E T

CASE: REED SEMICONDUCTOR CORP. vs. MONOLITHIC POWER
SYSTEMS, INC.

SYSTEMS, INC.

WITNESS: JOSEPH MCALEXANDER III

DATE: July 1, 2025

JOB NO.: 589902

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