

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,
Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.,
Patent Owner.

IPR2024-01158
Patent 9,041,377 B2

Before KARL D. EASTHOM and KEN B. BARRETT,
Administrative Patent Judges.

BARRETT, *Administrative Patent Judge.*

ORDER
Denying Patent Owner's Motion to Strike
37 C.F.R. § 42.5

Patent Owner Monolithic Power Systems, Inc. filed a motion to strike portions of Petitioner’s Reply (Paper 26, “Pet. Reply”) that rely on Figure 1 of Tateishi. Paper 27 (“Motion” or “Mot.”). Petitioner Reed Semiconductor Corp. filed an opposition. Paper 28 (“Opposition” or “Opp.”).

A disputed issue in this case pertains to the “control signal” recited in the challenged claims. Claim 1, for example, recites, in limitation 1B2, “an input voltage sensing circuit having . . . a second input terminal . . . [that] is configured to receive *a control signal* provided by the pseudo constant on time control circuit,” and, in limitation 1D, “a logic control circuit . . . wherein . . . the logic control circuit generates *the control signal*.” Ex. 1001, 9:40–46, 10:5–9 (emphasis added).

In the Response to the Petition, Patent Owner asserts that Petitioner failed to meet its burden regarding these limitations, arguing, *inter alia*, that the Petition’s contentions regarding Tateishi’s Figure 3 result in a path between the purported “input voltage sensing circuit” and the purported “logic control circuit” that contains logic gates and therefore the signal generated is not the same signal that is received. *See* PO Resp. 21–25 (citing, *inter alia*, Pet. 37, 45). In its Reply, Petitioner reproduces Figure 1 and argues that:

Figure 1 of Tateishi does not include the logic gates that Patent Owner highlights in Figure 3 above. Figure 1, therefore, overcomes Patent Owner’s argument. Both the Petition and the Institution Decision repeatedly cite ***both*** Tateishi’s Figure 1 ***and*** Figure 3 throughout the claim 1 analysis. *See* Paper 6 (Jan. 27, 2025) at 19–21, 27–29; Pet. at 33, 39, 41, 43, 44, 46, 47.^[1] But Patent Owner chose not to address Figure 1 in its Patent Owner’s Response, and therefore, waived any argument

that Figure 1 fails to anticipate or render obvious^[1] the Challenged Claims. *See, e.g.*, Paper 7 (Scheduling Order) (Jan. 27, 2025) at 9 (“Patent Owner is cautioned that any arguments not raised in the response may be deemed waived.”).

Pet. Reply 17–19 (footnote and case citations omitted); *see also id.* at 2 (arguing, *inter alia*, that “it is undisputed that Tateishi’s Figure 1 discloses the claimed control signal.”).

Patent Owner, in its Motion, asserts that “Petitioner’s Reply introduces a new anticipation theory based on an embodiment (Figure 1) that is different than the embodiment relied on in the Petition,” and requests that the new Figure 1 arguments be stricken. Mot. 1–2. Petitioner opposes the motion, arguing that “Petitioner not only relied upon and cited to Figure 1 in its Petition, but the Board addressed Figure 1 in its Institution Decision,” and “[f]or both of these reasons, Petitioner is entitled to address Figure 1 in its Reply.” Opp. 1.

As to the first point, Petitioner asserts that “the Petition . . . repeatedly addressed Tateishi’s Figure 1 and Figure 3 throughout its analysis,” and provides a string cite to pages in the Petition where Figure 1 was cited. Opp. 2 (citing Pet. (Paper 1)) at 33, 39, 41, 43, 44, 46, 47). However, absent from Petitioner’s Opposition is a clear identification of where the Petition contains a contention that the purported “control signal” of Tateishi’s travels a path in Figure 1 between “a logic control circuit” and “an input voltage sensing circuit.” *Contra, e.g.*, Pet. 35 (contentions in the form of an annotated path in Figure 3). The Opposition’s list of pages where Figure 1 was cited does not include the pages of the Petition setting out contentions

¹ The challenged independent claims are only alleged to be anticipated. Pet. 24 (grounds table). Dependent claims 5, 7, 8, and 15 are the subject of an obviousness ground. *Id.*

for the input voltage sensing circuit’s “second input terminal” that receives the control signal. *Cf.* Pet. 36–39 (contentions for limitation 1B2 lacking any citation to Figure 1); *id.* at 37 (citing Figure 3 and providing an annotated portion of Figure 3 indicating Petitioner’s contention as to the “second input terminal”).

As to the second point, Petitioner argues that “the Board analyzed Tateishi’s Figure 1 in its Institution Decision in concluding that Tateishi discloses the claimed control signal.”² Opp. 1 (citing, *inter alia*, Paper 6 (“Institution Decision” or “Inst. Dec.”), 19–21, 27–29). In the portion of the Institution Decision describing the reference generally, we referred to Tateishi’s discussion of the Figure 1 embodiment for a description of aspects in common with the DC to DC buck converter of the Figure 3 embodiment and for a discussion of the operation of such a buck convertor.³ *See* Inst. Dec. 18–21. In the portion of the Institution Decision discussing limitation 1B2, we addressed what we understood to be Patent Owner’s implied claim construction arguments regarding “a control signal”—that the existence of

² In the Institution Decision, we did not finally conclude that Tateishi discloses the recited control signal. We “determine[d] that Petitioner has shown sufficiently for institution [i.e., under the reasonable likelihood standard] that Tateishi discloses this limitation 1B2.” Inst. Dec. 30. At the conclusion of this proceeding, we will, based on the entire record, determine whether Petitioner has demonstrated by a preponderance of the evidence that Tateishi discloses all of the limitations of the claims challenged as anticipated.

³ To the extent that Petitioner asserts that we made a finding that Figure 1 and Figure 3 are the same embodiment, that is incorrect. *See* Opp. 1 (Petitioner stating: “as also addressed in the Institution Decision, Tateishi’s Figure 1 and Figure 3 reference the same embodiment”). We referred to each as an embodiment, not as the same embodiment. *See, e.g.*, Paper 6, 19 n.7 (“Much of Tateishi’s descriptions are of the Figure 1 embodiment, but the Figure 3 embodiment uses many of the same element numbers . . .”).

logic gates in the path between two terminals precludes the generated control signal from being the same as the received signal. *See id.* at 26–30. For example, we stated:

Figure 1 shows output 122 of SR latch 116: 1) connecting to high side switch 12 through at least an AND gate (upper right of the figure); 2) directly connecting to discharging transistor 124 (bottom left of the figure); and 3) connecting to discharging transistor 82 through inverter 126 (middle left of the figure). Thus, Tateishi, in the block quote above [from paragraph 52], speaks of output 122 at the Q terminal of SR latch 116 as controlling switch 82 as well as other components without regard to whether the circuit includes logical operators between the two terminals. Although this disclosure is in the context of the Figure 1 embodiment (with an inverter at discharging transistor 82), Tateishi explains that “the DC to DC buck converter 10 of FIG. 3 operates in much the same manner as that of FIG. 1.” *Id.* ¶ 58; *see id.* (explaining that, in the Figure 3 embodiment, “[w]hen the off-state is initiated by the on-time timer 50, the discharging transistor 82 is turned on and the capacitor Con 74 is discharged to ground 20,” notwithstanding that there are logic gates between on-time timer 50 and discharging transistor 82); *see id.*, Fig. 3 (depicting on-time termination signal 70 of on-time timer 50 as an input to SR latch 116, which generates output 122, which, according to Petitioner, is the “control signal” that operates discharging transistor 82).

Id. at 28–29. We discussed this disclosure of the Figure 1 embodiment merely as potential evidence of how a person of ordinary skill in the art would understand “a control signal” in the context of a DC to DC buck converter. To the extent that Petitioner argues that the Board analyzed whether the Figure 1 embodiment anticipates the challenged claims, we did not.

We preliminarily determine that the Petition did not give notice to Patent Owner (or the Board) that Petitioner is presenting an anticipation theory based on the signal(s) path of Figure 1 or presented a contention that

Figure 1 discloses the recited “input voltage sensing” circuit of limitation 1B2. Our statements in the Institution Decision regarding Figure 1 did not open the door to any new theory. To the extent that Petitioner disagrees with this preliminary determination or considers the Reply Brief as within the proper scope of a reply to a claim construction argument, it may address the issue at oral argument, should one be held.

The Patent Trial and Appeal Board’s Consolidated Trial Practice Guide addresses motions to strike, stating:

In most cases, the Board is capable of identifying new issues or belatedly presented evidence when weighing the evidence at the close of trial, and disregarding any new issues or belatedly presented evidence that exceeds the proper scope of reply or sur-reply. As such, striking the entirety or a portion of a party’s brief is an exceptional remedy that the Board expects will be granted rarely.

Consolidated Trial Practice Guide at 80 (available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>). In this case, we are capable of identifying belatedly presented arguments, particularly where Patent Owner has raised the objection, and the exceptional remedy is not appropriate. In light of this, we decline to strike portions of Petitioner’s Reply. In reaching a final decision in this proceeding, we will consider only timely presented arguments and will *not* consider belatedly raised theories or any arguments that exceed the proper scope of the Reply.

Additionally, in light of the above, we disagree with Petitioner’s assertion that Patent Owner “has waived its argument relating to Figure 1.” Opp. 1. Patent Owner may, if chooses to do so and to the extent it deems appropriate, address arguments in Petitioner’s Reply and statements in the Institution Decision regarding the Figure 1 embodiment.

ORDER

For the foregoing reasons, it is

ORDERED that Patent Owner's Motion to Strike Portions of
Petitioner's Reply is *denied*.

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