UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.

Patent Owner,

Case No. IPR2024-01158
Patent No. 9,041,377

PATENT OWNER'S SUR-REPLY

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EXHIBIT LIST

Exhibit	Reference
2001	Declaration of Joseph C. McAlexander III, P.E.
2002	Curriculum Vitae of Joseph C. McAlexander III, P.E.
2003	Wayback Machine May 27, 2010 Webpage Archive of Integrated Publishing's Electrical Engineering Training Series' Page Entitled "Variations of fundamental gates"
2004	Webpage of LibreTexts.org's University Physics II Text, Section 10.2, Entitled "Resistors in Series and Parallel"
2005	Second Declaration of Joseph C. McAlexander III, P.E.
2006	Excerpts of the April 9, 2025 - Deposition Transcript of Douglas R. Holberg, Ph.D.
NEW EHXIBIT	
2007	Excerpts of the August 18, 2025 - Deposition Transcript of Douglas R. Holberg, Ph.D.

I. Introduction

Petitioner's anticipation theory fails because it does not demonstrate that Tateishi discloses the singular "control signal" that is connected between components as required by the claims.

The claims are recited plainly; they require a "control signal" generated by a "flip-flop" that is used as an input for "an on-time generator":

> 18[E]: "the flip-flop generates the control signal" and 18[A] "an on-time generator configured to receive … a control signal."

To arrive at this simple limitation, Petitioner improperly combines two different signals from Figure 3—the Q output of PWM latch 116 and the input to transistor 82—and calls them the same signal. They are not the same, nor are they logically equivalent. Petitioner's expert confirms; when Q is "0" the input to transistor 82 can be either "0" or "1" depending on other logic. This mismatch destroys anticipation under any construction.

Further, the proper construction of "control signal" is "logic signal with two distinct states," which Petitioner's signal amalgam does not meet. The specification and claims describe the control signal as being output by a logic circuit, *e.g.*, a flip flop that outputs only two states, that is used to control other circuits. Petitioner's construction is wrong; it is merely a rearrangement of terms while adding a non-limitation that the signal be for a "circuit component." Petitioner's Reply side-steps that the control signal is generated by a flip-flop, and

focuses on the inclusion/exclusion of control in Patent Owner's construction. But the concept is already implicit in Patent Owner's construction.

Even under Petitioner's construction, Tateishi fails to anticipate the challenged claims. Claim 18 requires (inputting Petitioner's construction in [brackets]) that "the flip flop generates the [signal configured to control a circuit component]" and that the "on-time generator … receive[s] … [the signal configured to control a circuit component]." Petitioner's construction does not cover a flip flop outputting a "0" when the on-time generator can receive an "0" or "1," depending on other interceding logic, as Tateishi does. Petitioner's construction makes the tie between the generated control signal and the device it controls even stronger.

Finally, Petitioner's criticisms of Patent Owner's expert emphasize the deficiencies of Petitioner's own analysis. Petitioner criticizes Patent Owner's expert as incorrect for not providing all scenarios in his logic truth table. But, Patent Owner's expert was tracing out examples to show when there was an inconsistency, not painting an entire picture of operation. Conversely, Petitioner advocated that two signals can be equated to arrive at a conclusion of equivalence, but its expert excluded many cases that provided for an inconsistency. This is backwards.

Petitioner's deficiencies are described in more detail below.

II. Tateishi Does Not Anticipate the Claims

A. Petitioner Fails to Track the Control Signal Across Limitations

The Reply does not adequately address Patent Owner's primary argument that the Petition fails to demonstrate anticipation because it identifies two separate signals of Figure 3 as the singularly recited "control signal" of 1[B2]/18[A] and 1[D]/18[E].[1] (POR at 21-26 (excerpting portions of Petition).) The Reply describes these two signals as merely trivial logic transitions (e.g., inversions). (Reply at 13-17 (citing EX1016 at ¶¶ 27, 29.)) These two signals are, however, not the same nor are they trivial logic transitions; when one signal is "0" the other can be either "0" or "1" depending on other logic. (*See, e.g.,* EX1016 at ¶ 34 (Petitioner's expert's timing diagram showing this with orange = "0" and green = "1" or "0"); EX2005 at ¶ 83 (Patent Owner's expert's logic table showing the same inconsistency in rows 1-3).) There is, accordingly, no logically consistent basis to tie these signals together as one signal. Anticipation based on Tateishi thusly fails.

[1] Claim 11 is substantively similar to claim 1. (EX1001 at 11:44-52, 12:8-13.) Claims 18 is referenced in more detail herein, but the arguments are equally as applicable to claims 1 and 11.

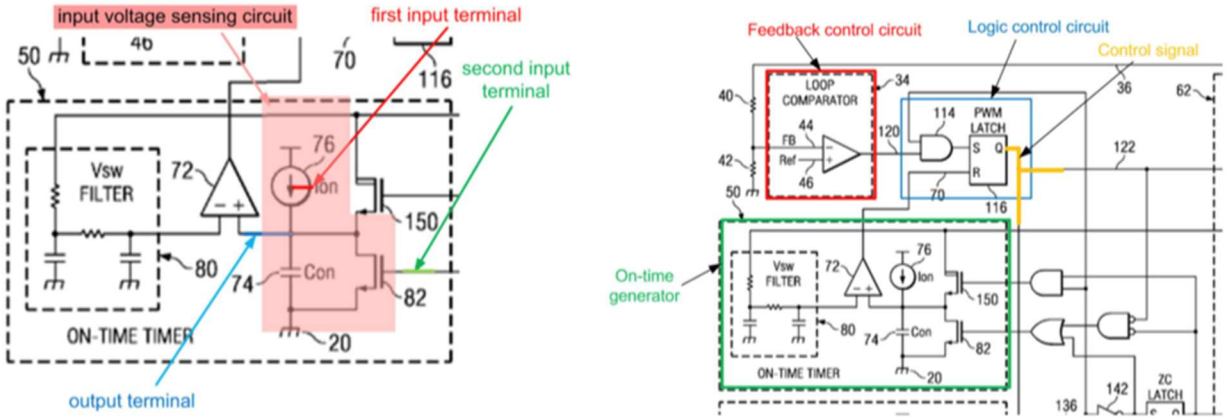
The "control signal" is the same element across the claims. Claim 18 requires that the "control signal" (blue) both be generated by the flip-flop (orange) and input to the "on time generator" (yellow).

18. A step-down regulator, comprising:

[18[A]] **an on-time generator configured** to receive a switching signal provided by the step-down regulator, and **to receive a control signal**, wherein based on the switching signal and **the control signal**, the on-time generator generates an on-time signal; …

[18[E]] **a flip-flop** having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, **the flip-flop generates the control signal**;

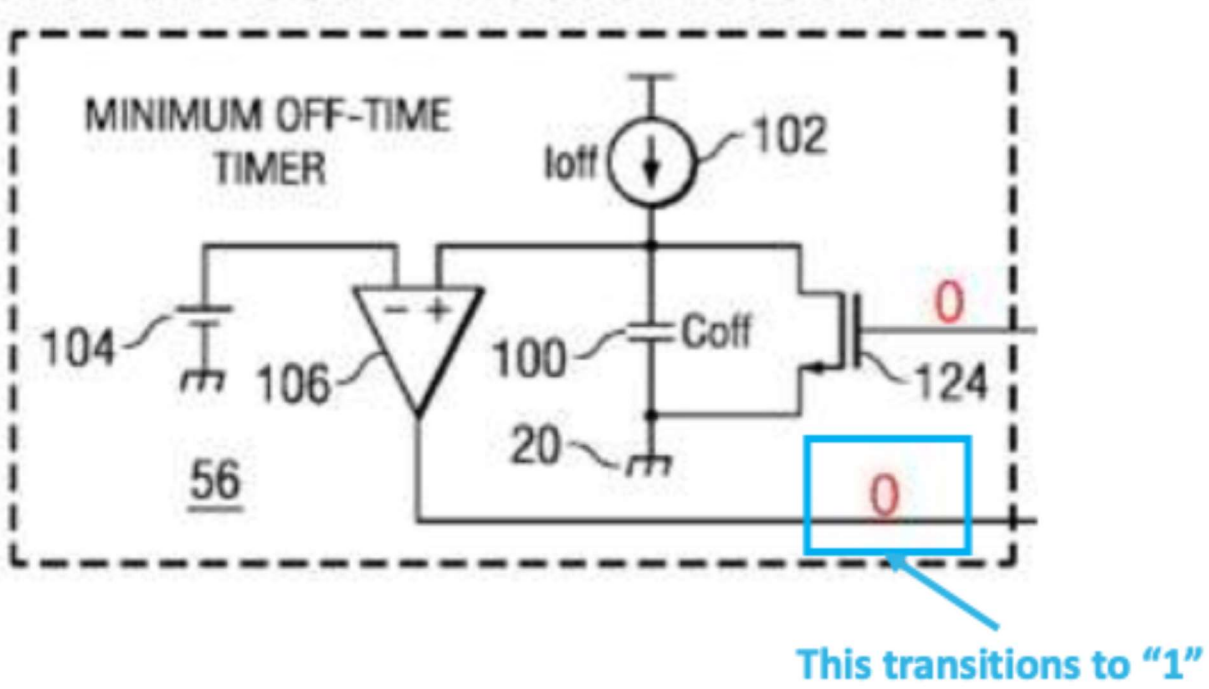
The Petition identified as the control signal the signal input to transistor 82 for 1[B2]/18[A] and the signal output from the PWM Latch 116 for 1[D]/18[E]. (Petition at 37, 66 *and* 43-44, 71-72.) The Reply continues this analysis. (*See generally* Reply.)



(Excerpts from Petition at 37 (left) and 45 (right))

The mismatch between these two signals is evident from Dr. Holberg's declaration and deposition testimony. His declaration assumes that Q is "0" (the signal for 1[D]/18[E]) and signal 110 will be "0," resulting in the input to transistor 82 being "1" (the signal for 1[B2]/18[A]). (EX1016 at ¶ 29.) These presumptions are incorrect: in deposition he confirmed that signal 110 transitions to "1" in operation which would drive the input to transistor 82 to "0." (EX2007 at xxx (“”)). This results in two separate conditions when Q is "0": transistor 82's input is "1" ***and*** transistor 82's input is "0." (EX1017 at ¶ 34 (showing Q as "Orange" which is "0" when input to transistor as "Green" is "1" or "0").) The value of transistor 82's input depends entirely on another set of logic. Q (1[D]/18[E]) and the input to transistor 82 (1[B2]/18[A]) are, consequently, not the same control signal.

The mismatch between the two is evident when the circuit's logic is traced through. When Q is "0" the input to transistor 124 is "0" and is turned off which causes Coff 100 to charge via Ioff 102 and comparator 106 to output a "1." (EX1005 at 7:57-60; *see also* EX2007 at 30:15-23.) As a result of this, signal 110 will change from "0" to "1," as illustrated in blue below. (EX2007 at 30:15-23.)



(EX1016 at ¶ 29 (excerpt with blue annotation added).)

This change of signal 110 to "1" changes the eventual input to transistor 82 to "1." Shown below in blue, when signal 110 is flipped to "1", the output of OR GATE 112 is "1" resulting the output of inverter 142 to go to "0," and driving the input to transistor 82 "0." (EX1016 at ¶ 34 (showing "Aqua," *i.e.*, signal 110 as "1" and "Green," *i.e.*, input to transistor 82 to be "0").) When Q is "0," the input signal to transistor 82 is either "0" or "1" (depending on the output of the minimum off-time timer).

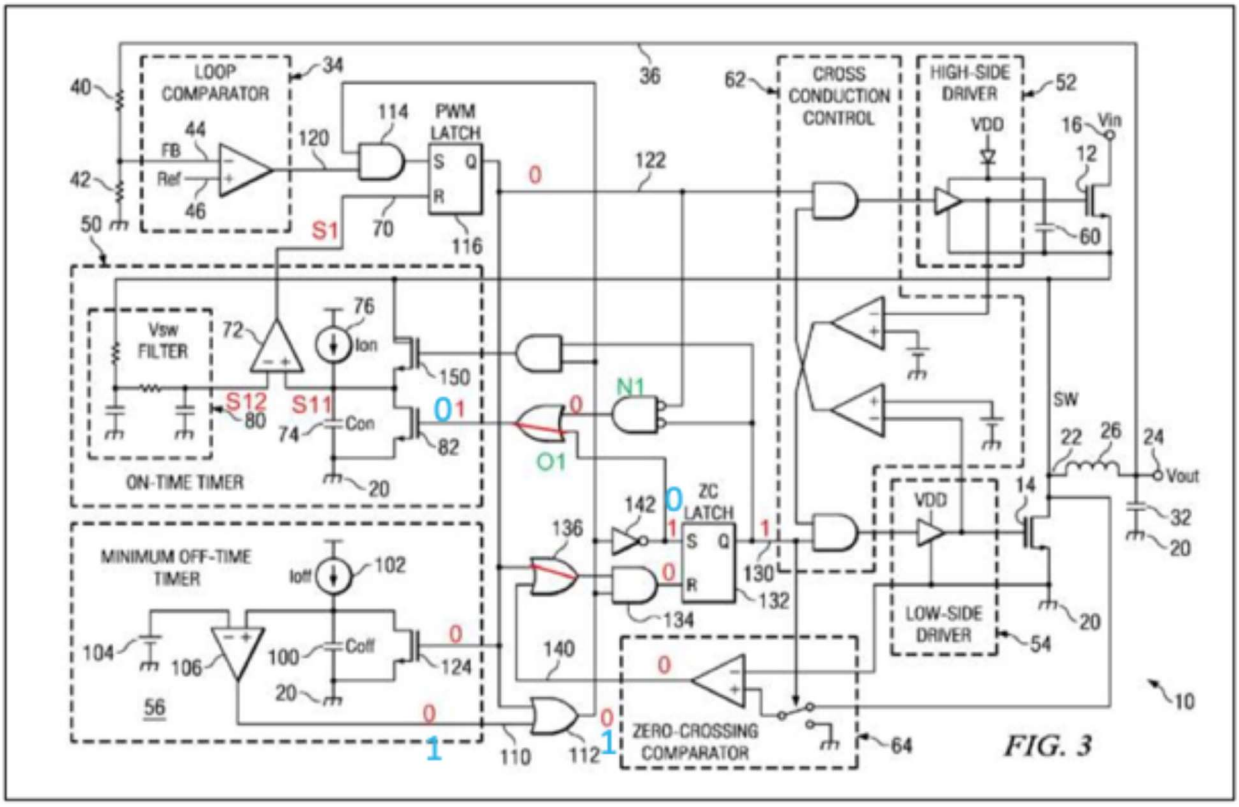
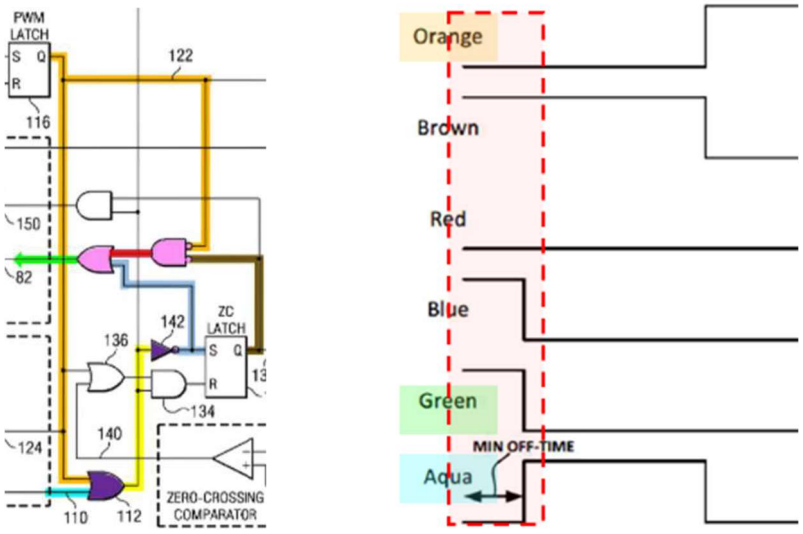


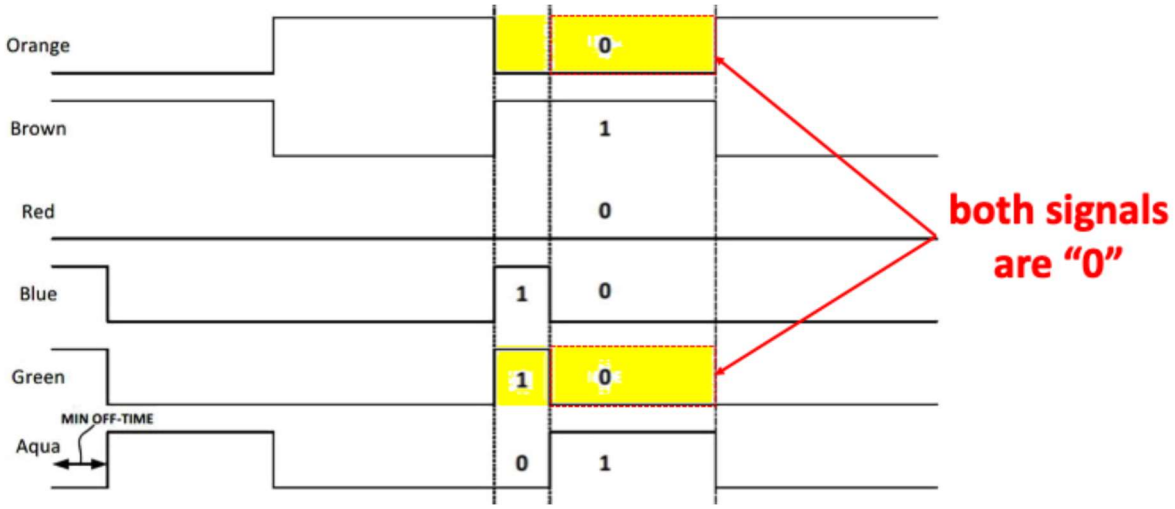
FIG. 3

(EX1016 at ¶ 29 (blue annotation added).)

Further, while not described in the text of his declaration, Dr. Holberg graphically reveals the signal inconsistency in his timing diagrams. Shown below-left is a circuit and below right is Dr. Holberg's timing diagrams. When the orange signal (*i.e.*, Q output identified for 1[D]/18[E]) is "0" the green signal (*i.e.*, input to transistor 82 identified for 1[B2]/18[A]) is "1" or "0" depending on the value of the aqua signal. (EX1016 at ¶ 34.)



Tellingly, Dr. Holberg depicts Orange (Q signal for 1[D]/18[E]) as "0" with Green (input to transistor 82 for 1[B2]/18[A]) as "1"—and not "0"—for most of the time. This is annotated in yellow and red, below, which shows that the Orange and Green signals do not logically track eachother. This contrasts with the arguments of Petitioner's Reply, *i.e.*, when Q is "0" the input to transistor 82 is "1" and when Q is "1" the input to transistor 82 is "0." (*See generally* Reply.)



The input to transistor 82 and Q cannot be thought of as the same control signal; they provide at least three different logical states: (1) Q = "1" and input to transistor 82 = "0" (EX1016 at ¶ 27); (2) Q = "0" and input to transistor 82 = "1" (*id.* at ¶ 29); and (3) Q = "0" and input to transistor 82 = "0" (*id.* at ¶ 34). The claimed control signal is, however, a plain logic 1 or 0 because "the flip-flop generates the control signal." (18[E].)

Dr. Holberg made other assumptions to eliminate circuits of Figure 3 to arrive at the claims. He only considered when the zero-crossing comparator (annotated in yellow, below)—which affects the entire circuit—is disabled. (EX1016 at ¶ 26 ("when the zero-crossing comparator 64 is not triggered, the circuit of Figure 3 operates much the same way as Figure 1"); *id.* at ¶ 27 and ¶ 27 (showing the zero-crossing comparator as zero); *see also* EX2007 at 17:24-18:2).) He, however, admits that there is a situation when the zero-crossing comparator is triggered when Q is "0." (EX2007 at 20:16-20, 23:11-15 (stating that "I didn't consider that case. I'd have to go back and analyze it under that situation")

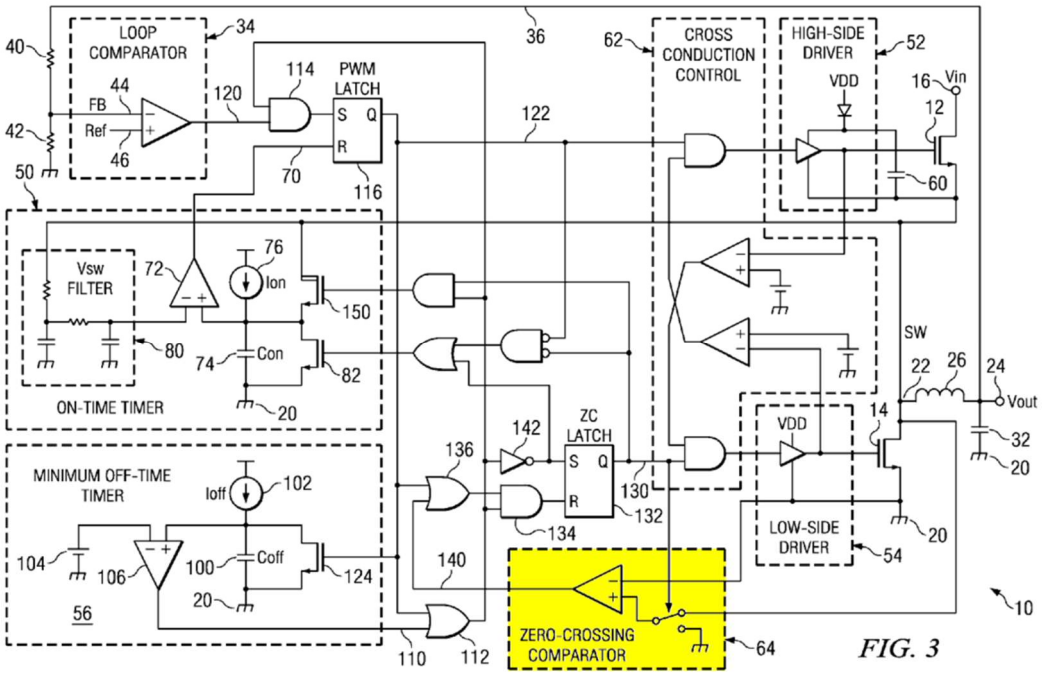


FIG. 3

His many assumptions demonstrate the fault in his analysis, and his identification of the "control signal," which he said can effectively be any and all signals of the circuit of Figure 3 (except for power and ground). (EX2007 at 10:1-6, 11:21-13:8, 13:20-25, 16:4-17:9; *see also* § II.B.3 (describing in more detail).)

Petitioner has thusly failed to show that the same control signal identified for 1[D]/18[E] is the same one identified for 1[B2]/18[A].

B. Petitioner fails to demonstrate anticipation under either construction of "control signal"

Petitioner's construction does not get at the crux of the dispute described above in § II.A. Under either parties' construction of "control signal," Tateishi fails to anticipate the claims. This is described below, with the constructions addressed first.

1. Claim Construction of "Control Signal"

Patent Owner's construction should be adopted because it describes the structure of the control signal ("logic signal with two distinct states") as opposed to Petitioner's construction that merely re-arranges words ("signal configured to control a circuit component").

While Petitioner's primary criticism appears to be that Patent Owner purportedly reads out "control" and the specification is replete with examples of "control" (*see generally* Reply at 6-10), the real issue appears to be whether "signal" itself should be a logical signal with two distinct states, or not.

The construction should describe the signal as Patent Owner's construction does. As described in the specification and claims, the control signal is generated by a logic circuit and the control signal is used as an input to other circuit elements. (POR at 7-13.) Further, Dr. Holberg agrees that the control signal in the claims is a two-state signal. (POR at 8 (citing EX2006 at 22:11-19, 25:10-18, 14:15-18:4).) That the "control signal" is a two-state signal is most evident in claim 18, where it is generated by a flip-flop, which outputs a binary signal (EX2006 at 22:11-19):

> 18[E]: "a flip-flop having a set terminal, a reset terminal and an output terminal … the flip-flop generates the control signal"

A flip-flop cannot output an amalgamation of signals as Petitioner attempts via its application of its construction.

Petitioner's Reply side-steps the primary dispute, and instead advocates heavily for the concept of control. (*See generally* Reply at 6-10.) Control is not the real dispute; implicit in Patent Owner's construction—and in context of the claims—is the concept of control. Patent Owner's construction describes "two distinct states" and, in context of the claims, it provides control to other devices. Petitioner's focus on "control" side-steps the main issues.[2]

Petitioner's construction, moreover, merely rearranges words and adds surplusage. It moves "signal" (yellow) to the front, "control" (aqua) to the back, and adds that it is for "a circuit component." The claims are plainly directed to circuits via their preamble and language (*see* EX1001 at claims 1, 11, 18), so addition that the signal is for a circuit component says nothing. Petitioner's construction does not appropriately describe the control signal.

- **Term:** control signal
- **Construction:** signal configured to control a circuit component

Finally, Petitioner's construction is incorrect because of Petitioner's apparent application of that term. Petitioner views this construction so broad as to

[2] Nonetheless, because "control" is implicit in Patent Owner's construction, its inclusion is still consistent and correct (*e.g.*, "logic signal with two distinct states *for control*")

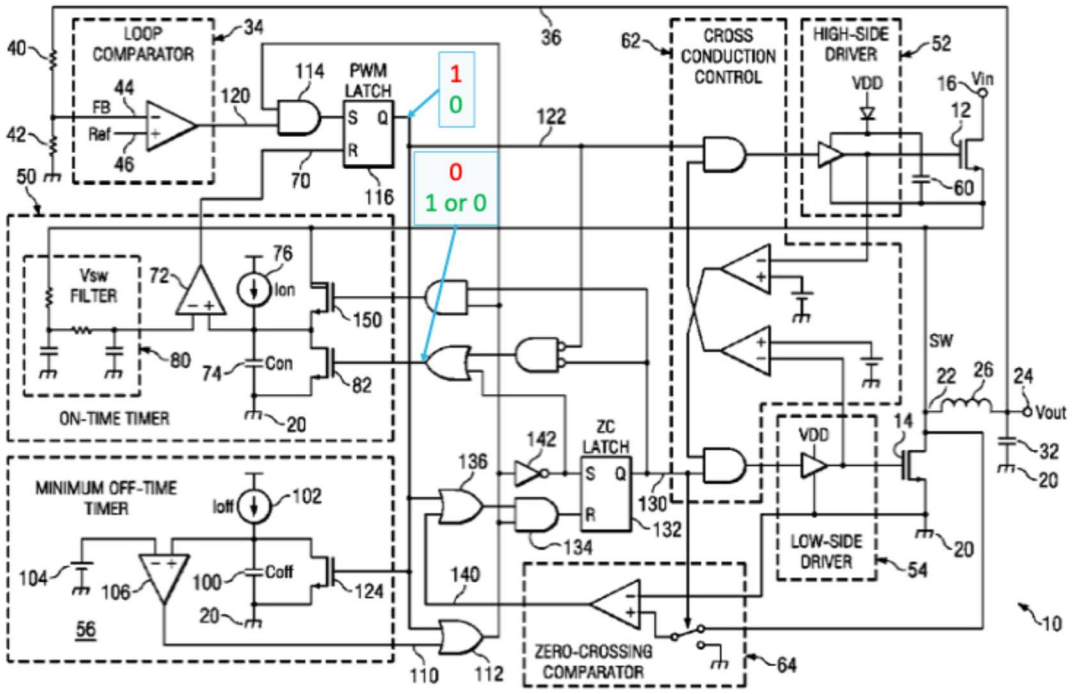
encompass any and all signals of Tateishi's Figure 3 (except for power and ground). (EX2007 at 16:23-17:9.). Petitioner removes any bounds—and interconnects—from this term and the claims.

Petitioner's construction is accordingly incorrect, and Patent Owner's construction should be adopted.

2. Petitioner fails to demonstrate anticipation of "control signal" under Patent Owner's construction

The proper construction of "control signal" is a "logic signal with two distinct states."

Tateishi's Figure 3 fails to anticipate the claims because it fails to teach the control signal under this construction. Petitioner's identified "control signal" does not have two distinct logic states, it has multiple. For example, when Q is **"1"** the input to transistor 82 is **"0"** and when Q is **"0"** the input to transistor 82 is **"1" or "0"** depending on other logic. (EX1016 at ¶ 34.) The proper construction of "control signal," describes a two-state signal and cannot be satisfied with a combination of signals that has at least three states.



Petitioner thusly fails to demonstrate anticipation by Tateishi.

3. Petitioner fails to demonstrate anticipation of "control signal" under Petitioner's construction

Petitioner's analysis—even assuming its construction is adopted—still fails because Petitioner identifies two separate signals as the claimed "control signal." (*See* § II.A (describing in more detail).)

Petitioner's construction, moreover, emphasizes the impropriety of its anticipation analysis. This becomes more evident when the "control signal" is replaced with Petitioner's construction, which requires "configured to control."

- Claim 18 recites "an on-time generator configured to receive … a [signal configured to control a circuit component]" and "the flip flop

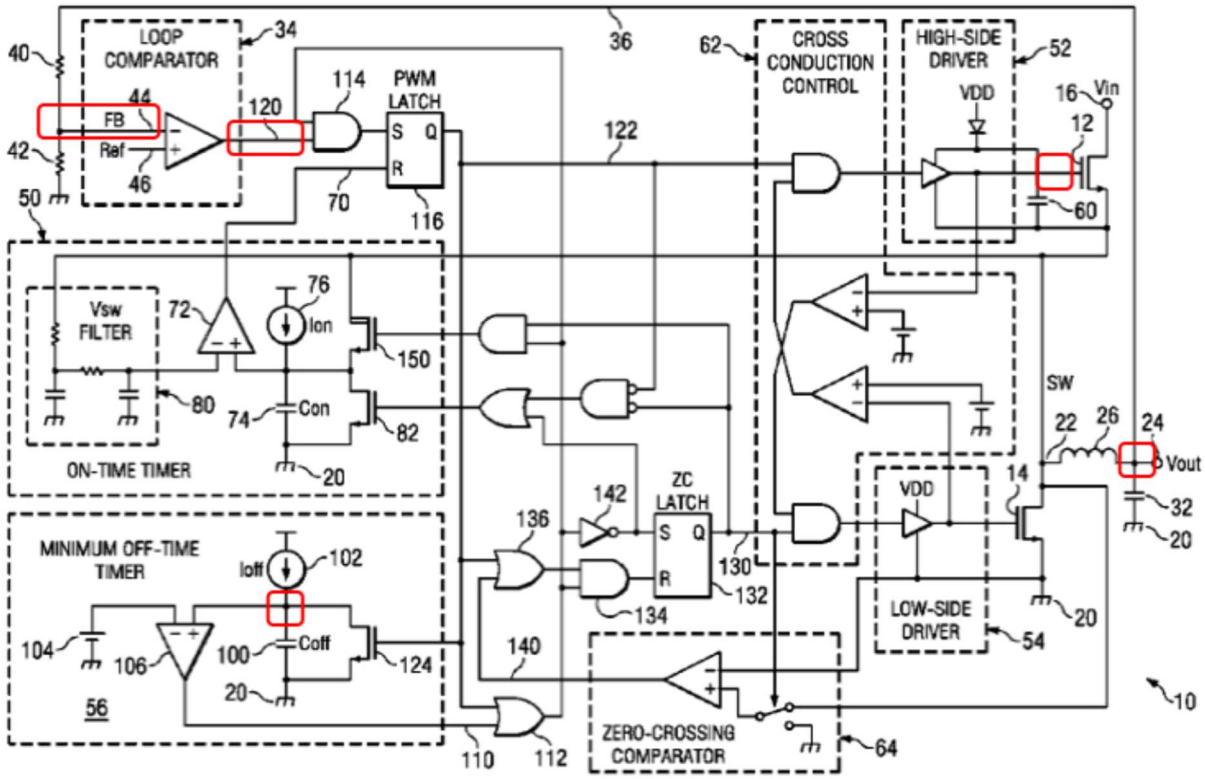
generates the [signal configured to control a circuit component]."

As described in § II.A, the generated signal Q is not "configured to control" the input to the transistor 82 (the "circuit component"). There is a logical dissimilarity between the two: when Q is "0" the input to transistor 82 can be either "1" or 0." (EX1016 at ¶ 34.)

Claim 18's control signal is generated by a flip-flop, which is explicitly a binary 1 or 0: the flip flop generates the [signal configured to control a circuit component]." A circuit like this can only be "configured to control" "1" or "0" states, and Petitioner's identification of a multitude of signals fails.

Finally, Petitioner's application of its own construction renders the term "control signal" itself superfluous within the context of the claim. Dr. Holberg testified that any signal—or combination of signals—within Figure 3 can be the same control signal (except for voltage power and ground). (EX2007 at 10:1-6, 11:21-13:8, 13:20-25, 16:4-17:9.) For instance, he testified that the positive input to comparator 106, the feedback signal 44, signal 120, Vout 24, and the input to transistor 12 are all the same control signal (annotated in red, below). (*Id.*) In effect, under Petitioner's application, PWM latch generates any signal in the circuit to meet the claim phrase, because any signal is the "control signal." Under Petitioner's application, any signal in a device can satisfy claim 18's "the flip flop generates the control signal" and "an on-time generator configured to receive … a

control signal," rendering this phrase meaningless. Petitioner's application demonstrates the impropriety of its theory.



Petitioner fails to demonstrate anticipation of Tateishi under its own construction.

III. Petitioner's Criticisms of Mr. McAlexander Demonstrate Petitioner's Own Flaw

Petitioner criticizes the majority of Mr. McAlexander's truth table as "incorrect," but that criticism demonstrates the flaw in Petitioner's own rationale. At most, Dr. Holberg stated that Mr. McAlexander's analysis was incomplete because it did not trace out all conditions. (EX2007 at 25:15-30:23.) But, Mr. McAlexander was not the party advocating that two entirely separate signals can

be thought of as the same signal; he merely needed to chart out inconsistencies to show they are not the same signal. Mr. McAlexander did that.

Petitioner, in contrast, advocates that two signals can be thought of as the same. Petitioner needed to demonstrate a logical parallel between the two (or that the difference is merely transients). However, in justification of that argument, Dr. Holberg analyzed very limited cases, *e.g.*, only when Q is 1 or 0 ***and*** the zero-crossing comparator 64 is 0, *i.e.*, disabled ***and*** signal 110 is 0 when Q is 1. He ignored those cases that showed inconsistency and conflicted with his analysis and conclusion. Dr. Holberg's and Petitioner's narrow confinement of use cases demonstrates that Q and the signal input into transistor 82 cannot be thought of as the same signal.

IV. Petitioner's Reliance on Figure 1 is Improper

Petitioner addresses Figure 1 in its Reply as an invalidating embodiment. (Reply at 17-19.) This is an improperly raised argument that was not presented in the Petition. *See, e.g.,* 37 C.F.R. § 42.23; Consolidated Trial Practice Guide at 80 (Available at https://www.uspto.gov/TrialPracticeGuideConsolidated/); *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.,* 821 F.3d 1359, 1369 (Fed. Cir. 2016); *Yita LLC v. MacNeil IP LLC*, 69 F.4th 1356, 1367 (Fed. Cir.); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1329 (Fed. Cir. 2019); *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1367 (Fed. Cir. 2015); *see also Juniper*

Networks, Inc. v. Swarm Technology LLC, IPR2021-01445 at 28-29 (Paper 62) (Feb. 7, 2023); *MOM Enterprises, LLC d/b/a Mommy's Bliss v. R Vieth et al.* IPR2023-00726 at 9 (Paper 89) (May 9, 2024).

As described by the Board, "the Petition did not give notice to Patent Owner (or the Board) that Petitioner is presenting an anticipation theory based on the signal(s) path of Figure 1 or presented a contention that Figure 1 discloses the recited 'input voltage sensing circuit' of limitation 1B2 [and] [the Board's] statements in the Institution Decision regarding Figure 1 did not open the door to any new theory." (Paper 29 at 5-6.)

Petitioner's Reply argument as to Figure 1 as an anticipating embodiment is, accordingly, improper and should not be considered.

V. Conclusion

The challenged claims are a valid for the reasons described above and for the reasons described in the Patent Owner Response.

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CERTIFICATE OF COMPLIANCE

Under 37 C.F.R. §42.24(d), the undersigned certifies that the word count for this Patent Owner's Sur-Reply for inter partes review totals 3,060 excluding the parts exempted by 37 C.F.R. §42.24(a). The word count was made using the built-in word count function in the Microsoft® Word software used to prepare this document.

Dated: August 25, 2025 Foley & Lardner LLP 11988 El Camino Real, Suite 400 San Diego, CA 92130 (858) 720-5700	Respectfully submitted, /Miguel Bombach/ Lead Counsel John P. Schnurer, Reg. No. 52,196 Back-Up Counsel Miguel Bombach, Reg. No. 68,636 John D. Esterhay, Reg. No. 73,512 *Attorneys for Petitioner* *Monolithic Power Systems, Inc.*

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on August 25, 2025, a copy of **PATENT OWNER'S SUR-REPLY** was served upon the below-listed counsel by electronic mail:

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Dated: August 25, 2025

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