

UNITED STATES PATENT AND TRADEMARK
OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REED SEMICONDUCTOR CORP.,

Petitioner,

v.

MONOLITHIC POWER SYSTEMS, INC.,

Patent Owner,

Case No. IPR2024-01158

Patent No. 9,041,377

DEPOSITION OF DR. DOUGLAS HOLBERG

Taken via Zoom

Monday, August 18, 2025

Reported by Jane Gallegos, CSR

Certificate No. 14676

Job No. 117382

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On Monday, August 18, 2025, commencing at the hour of
9:08 a.m., via Zoom, before me, Jane Gallegos, Certified
Shorthand Reporter in and for the State of California,
remotely appeared

DR. DOUGLAS HOLBERG,
called by the Patent Owner, who, being by me first duly
sworn, was thereupon examined as a witness in said cause.

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1 Monday, August 18, 2025, 9:08 a.m.

2 Reported Remotely in Los Angeles, California

3

4 THE REPORTER: On the record. Today is
5 August 18, 2025. The time is 9:08 a.m. I'm the court
6 reporter, Jane Gallegos, CSR 14676.

7 Before swearing in the witness, may I have
8 counsels state their appearances for the record, starting
9 with the noticing attorney.

10 MR. BOMBACH: I'm Miguel Bombach from Foley &
11 Lardner, representing patent owner Monolithic Power
12 Systems.

13 MR. GRAY: I'm Andrew Gray from Morgan Lewis,
14 representing the petitioner Reed Semiconductor. I'm
15 accompanied by my colleagues, Andrew Devkar and
16 Annaliese Parker.

17 THE REPORTER: I will now swear in the witness.

18 DOUGLAS HOLBERG, PhD,
19 was called as a witness and, having been first duly sworn,
20 was examined and testified as follows:

21 EXAMINATION

22 BY MR. BOMBACH:

23 Q Good morning, Dr. Holberg.

24 A Hey. Good morning, Miguel. Good to see you
25 again.

1 Q Same here.

2 A **This may be our last visit.**

3 Q Yeah, maybe.

4 So you've been through this process before and --
5 but if you have any questions or any concerns with respect
6 to any question I provide, if I am unclear, or you do not
7 understand a question, please ask me to clarify. My goal
8 is to have a clean record. Do you understand?

9 A **I do.**

10 Q And you were deposed in this matter prior;
11 correct?

12 A **Yes.**

13 Q Is there anything about your deposition or your
14 prior declaration that you had submitted that you would
15 like to address before we continue?

16 A **I can't think of anything. No.**

17 Q Okay. I'm going to primarily ask you about three
18 documents during -- and I'm going to upload them to the
19 chat box -- and throughout this process, if you need to
20 refer to any other document in this proceeding, please ask
21 me to provide it.

22 A **Okay. I didn't know what you were going to**
23 **upload. Just FYI for completeness, I do have a paper --**
24 **plain paper copies of the supplemental -- the two**
25 **Tateishi, the patent, and the -- and the application**

1 version; my prior declaration; and then the 377 Patent;
2 but if you're going to download them, I don't need to get
3 to those -- and allow me to download them; right?

4 Q And during the process, if you'd like to refer to
5 your paper copies, if it's easier, please do so.

6 A Okay.

7 Q And you don't have any -- do you have any
8 personal notes or annotations on those documents?

9 A No, I do not.

10 Q Okay. And then on your computer, do you have any
11 other programs open that would have notes or other
12 messaging?

13 A No, I do not.

14 Q Okay. And during this process, you understand
15 that you're not to communicate with your attorneys about
16 the substance of your testimony; correct?

17 A Yes. I understand that.

18 MR. BOMBACH: Okay. And I'm going to upload into
19 the chat box what has been premarked Exhibit 1005, 1016,
20 and 1001.

21 (Exhibits 1005, 1016, 1001 marked for
22 identification.)

23 BY MR. BOMBACH:

24 Q And I had just downloaded clean copies of these.
25 If you could, please download them and open them on your

1 machine.

2 A So I have the 377 patent open, my supplemental
3 open; and the third document was the Tateishi patent.
4 Okay. So I have those three documents open in my PDF
5 reader.

6 Q Okay. And Exhibit 1016 is your declaration that
7 you reviewed and signed; correct?

8 A Yes.

9 Q Are there any issues or errors in the declaration
10 that you'd like to address or otherwise correct at this
11 moment?

12 A There was one thing that was kind of a residual
13 that doesn't mean anything anymore. Let me find out where
14 that is.

15 Okay. Yeah. On page 18, which is paragraph 34,
16 I have a statement in here about the diagram also ignores
17 propagation delays through gates, except for the case of
18 the Aqua signal. That's no longer valid. That was an
19 earlier -- earlier draft of this, and it turns out I
20 didn't need to take that into account, so that's the only
21 thing.

22 Q Okay. What do you mean, you didn't need to take
23 it into account? Is...

24 A Well, in some of my earlier analysis, I thought
25 that it would have been -- it was important to take into

1 account the propagation delays associated with the path of
2 the Aqua signal, but I realized that was not the case.

3 Q Okay. Why is it not the case?

4 A Because it doesn't matter.

5 Q What do you mean, it does not matter? It does
6 not matter to what?

7 A The propagation delays associated with the Aqua
8 signal don't impact the -- the timing diagram that I
9 presented.

10 Q Okay. Let's just jump into the declaration. Can
11 you jump to paragraph 7, please.

12 A Yes. I'm there.

13 Q In your -- in your opinion, can the control
14 signal be multiple different signals?

15 A The control signal -- as I said in paragraph 7 --
16 and I'll read it for the record. "For the following
17 reasons, it's my opinion that the term 'control signal'
18 should be construed in accordance with its plain and
19 ordinary meaning as a signal configured to control a
20 circuit component."

21 When you say "signal" in your question -- could
22 you restate the question so that I can clarify my
23 response?

24 Q Yes. I don't remember exactly what I asked, but
25 I will re-ask.

1 In your opinion, can the control signal be
2 multiple different signals?

3 **A The control signal can manifest itself in**
4 **different locations along a path in the circuit. I don't**
5 **distinguish -- I mean, it's a control signal everywhere it**
6 **affects any of the downstream circuitry.**

7 Q Does an input voltage, such as VCC 2, a chip,
8 affect its -- the downstream voltage of all its
9 components?

10 **A Sorry. VCC 2 -- what are your --**

11 Q Does an input voltage that powers the chip also
12 affect its downstream components?

13 **A Certainly, the VCC powers all of the components.**

14 Q In --

15 **A So -- yeah. Go ahead.**

16 Q No. Sorry. I interrupted.

17 **A So in that sense, it affects them. Yes.**

18 Q Okay. At what point would you draw the line
19 between what is a control signal and what is a signal that
20 merely provides power for components?

21 **A Well, power -- theta would not normally consider**
22 **the power supply as a -- as a control signal in the way**
23 **that, you know, you'd normally think of a control signal.**

24 Q In your opinion -- or, rather, does a -- would
25 you consider a chip or a processor of sorts to have

1 multiple control signals, or do you view all of those
2 control signals as one control signal?

3 A Well, I didn't address, you know, something like
4 that in my declaration, so I qualify my response in that
5 sense; but there can be -- in a -- in some generic
6 hypothetical processor, there can be multiple control
7 signals.

8 Q Yeah. I guess we should -- instead of looking at
9 the hypothetical, we should probably just look at the
10 figure because it gives us a good figure of circuit
11 components. If we look at Figure 3 of Exhibit 1005 -- and
12 please let me know when you have that open.

13 A Yeah. I'll let you rotate it.

14 Okay. I have it open.

15 Q If you could look at the top-left portion of the
16 loop comparator, looking at Signal 120, would you consider
17 that to be a control signal?

18 A I don't think so. I mean, that is the result of
19 a comparison between attenuated output voltage and a
20 reference voltage in the feedback path, so...

21 Q Okay. The output of Endgate 114 -- you consider
22 that to be a control signal?

23 A Well, I mean, in the broadest sense of the
24 construction that I've provided, then -- I guess I could
25 argue that any signal that controls any other device is a

1 control signal -- backing up to your first question about,
2 is 120 a control signal.

3 In the basic construction that I've given, which
4 is a signal configured to control a circuit component, you
5 know, 120, I guess, could be a control signal, as well as
6 the output of the circuit you're talking about, as well as
7 the output of Endgate 114.

8 Q Okay. And then the input, top right to
9 Transistor 12 -- do you consider that signal to be a
10 control signal?

11 A In the -- in the context of my construction --
12 restating again, a signal configured to control a circuit
13 component that -- that could be a control signal -- and
14 all these are control signals -- would be -- they're all
15 different.

16 Q So would you consider the control signal under
17 the construction for -- well, let me start over.

18 Would you consider one -- let me start over
19 again.

20 Considering the construction provided, 120 is a
21 control signal; but, also, the input to transistor is a
22 control signal as well; right?

23 A The input to a transistor or...?

24 Q Transistor 12.

25 A Yes.

1 Q Would you consider the control signal -- those
2 two control signals to be the same control signal?

3 A Which two?

4 Q Yes. I was -- would you consider the Control
5 Signal 120 and the control signal input into Transistor 12
6 to be the same control signal under the construction you
7 provided for control signal?

8 A Yes.

9 Q Can you please explain why you would consider
10 them to be the same control signal.

11 A Because what happens at 120, in terms of the
12 logical value resulting from the comparator output --
13 it -- assuming that the other input of 114 is Logic 1,
14 then what happens -- the signal on 120 will set the PWM
15 latch Q output to 1, which will, in turn, cascade through
16 the cross conductor control and the high side driver to
17 the input of 12, so the signal -- the signaling event
18 is -- the 120 signal causes Transistor 12 to turn on in
19 the case of its setting the PWM latch to a 1.

20 Q And as another example at the bottom left, you
21 see Comparator 106. The signal -- the signal into the
22 positive terminal off of C-off 100 -- you would consider
23 that to be a control signal as well; correct?

24 A It is controlling the state of the comparator,
25 so, yes, that is a control signal.

1 Q And then if -- would you consider that control
2 signal off of Capacitor 100 to be the same control signal
3 into Transistor 12 under your construction of control
4 signals?

5 A Yes, because what happens at 122 -- you haven't
6 mentioned that node, but that is the Q output of the PWM
7 latch. The state of what happens at that node cascades
8 through a number of these circuits, logic gates; and in
9 this case, you're speaking of this Capacitor 100, the
10 minimum off-time timer. So that controls the status of
11 the minimum off-time timer in one mode.

12 So I'm not sure what the -- I got to remember
13 your question -- just know if it's a "yes" or a "no," but
14 I'll describe the way it works.

15 Q Yeah, yeah. And you might have asked that --
16 answered it, but I'll -- I'll re-ask it for clarity.

17 The control signal off of C-off 100 and the
18 control signal feeding into Transistor 12 at the top right
19 of Figure 3, under your construction of control signal --
20 those two can be thought of as the same control signal;
21 correct?

22 A Well, they are -- they are both controlled by a
23 common control signal at Node 122.

24 Q But --

25 A Because -- but because the input to Transistor 12

1 does not feed over to the -- the minimum off-time timer
2 circuit where C-off is, then I wouldn't consider -- I
3 wouldn't consider that signal at the gate of 12
4 controlling the minimum off-time timer at -- at the
5 noninverting input of 106.

6 Q Okay. Would you consider -- the minimum off-time
7 timer provides an output through 110 through -- or
8 Gate 112 that feeds back into Endgate 114. Do you see
9 that?

10 A I do.

11 Q And then would you consider the signal from C-off
12 as -- rather, let me -- the signal from C-off cascades and
13 provides control that would effectuate Transistor 12;
14 right?

15 A Well, so the way this circuit works is once --
16 when 122 goes low, Transistor 124 turns off. The C-off
17 charges by way of Current Source 102. When the voltage at
18 driving -- increasing the voltage across C-off in a linear
19 fashion. Once that voltage is greater -- approximately
20 greater than or equal to the Reference Voltage 104, the
21 output of 106 goes high. That high will go -- because
22 it's an OR gate, it will go to the output of the OR gate
23 as a high or Logic 1; and that will present a Logic 1 at
24 the input of Endgate 114. That makes Endgate 114
25 transparent to whatever logic level is at Node 120. So if

1 Node 120 is a 1, it will set the Q output of the PWM latch
2 to a 1 at Node 122; and that will then turn on the output
3 Transistor 12 that you identified.

4 Q So in -- so would the control signal off of
5 C-off 100 be considered the same control signal going into
6 Transistor 12 under your construction?

7 A I believe so.

8 Q And then if we can look off of the top left of --
9 where it has Loop Comparator 34, which at its negative
10 terminal receives Feedback 44, which is sourced -- if you
11 could see from -- and please correct me if I'm wrong --
12 V-out 24 at the right. Do you see that?

13 A I do.

14 Q Do you consider Feedback 44 to also be a control
15 signal?

16 A Yeah. It controls the output of comparator --
17 well, it's not labeled -- the comparator and the loop
18 comparator circuit. Yes.

19 Q And then would you consider that control signal
20 to be the same control signal going into Transistor 12
21 under your construction of control signal?

22 A Yes.

23 Q Looking at Figure 3 of Exhibit 1001 -- rather
24 1005 -- can you identify two control signals that you
25 would consider to not be the same control signal under

1 your construction of control signal.

2 A Ground would not be a control signal.

3 Q Okay. Any others?

4 A Well, at the -- at the beginning, you asked about
5 VDD or VCC or something; and I can't remember what I said;
6 but, I mean, normally, you wouldn't think of that as a
7 control signal.

8 Q Okay. Any others?

9 A No.

10 Q Okay. If you could -- let's go to the next
11 section. If you could, turn to paragraph 15, please.

12 A Of?

13 Q Of Exhibit 1016.

14 A Okay. I'm there.

15 Q Can you provide explanation for your statement
16 that -- "Configured to control Switch K through an
17 inverter"?

18 A Well, the control signal -- you know, we've been
19 talking about, you know, all these different control
20 signals so far and this -- so this specific control signal
21 that's cited in the 377, which drives the Switch K -- when
22 you look at the states described in the 377 patent, it's
23 clear that that signal -- it's clear, first of all,
24 that -- would be clear to the Switch K is an N-channel
25 MOSFET; and then in order to turn it on when the control

1 signal is low, you would need an inversion in series with
2 it, a.k.a. an inverter. So that's -- that's what that
3 means.

4 Q One second.

5 We're going to turn to the next section of your
6 declaration, starting at paragraph 24 and 31 -- through
7 31; and if you could, please turn to paragraph 26; and if
8 you need any time to just re-review anything, please let
9 me know.

10 A Well, let me read paragraph 26 to myself.

11 Q Okay.

12 A Okay.

13 Q And, actually, my question would be with respect
14 to all of paragraph 24 through 31. So, please -- if you
15 need to review any of that to answer my question, please
16 do.

17 My understanding and reading of paragraphs 24
18 through 31 is that the Zero-Crossing Comparator 64 is not
19 triggered; is that correct?

20 A Well, what I said is -- Tateishi states that when
21 zero-crossing comparator is not triggered, the circuit in
22 Figure 3 operates much the same way as Figure 1. That's
23 just what I said. That's what Tateishi says.

24 Q Okay. Does your analysis of paragraphs 24
25 through 31 consider the zero-crossing comparator to not be

1 triggered?

2 A Yes.

3 Q Why did you not consider the state when the
4 zero-crossing comparator is triggered and outputs a 1?

5 A Well, it simplifies the analysis; but you could
6 do the analysis with it and still 122, the Control Signal
7 122, controls even the zero-crossing comparator, so -- but
8 this was simple -- it just simplified the analysis.

9 Q Did you believe it was unnecessary to consider
10 the zero-crossing comparator outputting a 1; and if so,
11 can you please further expand upon that?

12 A Well, I didn't think it was necessary, but the
13 fact is, the zero-crossing comparator is only made active
14 when the Q output of the ZC latch is high, which is the
15 same signal that turns on the low -- the low-side
16 transistor. The ZC latch is controlled by the Control
17 Signal 122, so the zero-crossing comparator is downstream
18 under the control of the control signal at Node 122 that
19 emanates from Node 122, the output of the PWM latch.
20 So -- so the -- whether or not you assume the
21 zero-crossing comparator is or is not activated is based
22 on the output voltage. It doesn't matter. I just did one
23 of the -- one analysis.

24 Q Is there a state within Figure 3 where PWM latch
25 outputs 1 Q and zero-crossing comparator outputs 1 at the

1 same time?

2 A Let me look. For the ZC -- the zero-crossing
3 comparator output of 1, it has to be enabled, which is
4 the -- the switch that's shown at the noninverting input;
5 and that switch enables the connection to the Node SW when
6 the ZC latch Q output is 1, when the low-side driver is
7 on.

8 You would never have -- at least during, you
9 know, normal operation, you'd never have the low-side
10 driver on at the same as the high-side driver; therefore,
11 you wouldn't expect the ZC latch output to be a 1 at the
12 same time that the PWM latch output is 1; therefore, you
13 wouldn't expect that the zero-crossing detector output
14 would be a 1 at the same time that the PWM latch output is
15 a 1.

16 Q Okay. And if you could look at paragraph 29
17 where you have a -- a diagram describing PWM latch 0,
18 would there be a scenario where PWM latch outputs a 0 and
19 zero-crossing comparator outputs a 1?

20 A Yes.

21 Q Okay. And why was that not included in your
22 analysis?

23 A Well, the purpose of my analysis is to show the
24 similarities between Figure 1 and Figure 3 by showing how
25 these various gates become transparent under certain logic

1 states. So it wasn't necessary. I didn't need to.

2 Q But it's -- is it fair to say under PWM latch
3 output 0, that these extra logic gates do not become
4 transparent?

5 A Well, you'll have to clarify that question, I
6 think.

7 Q Yeah. Under -- I'll -- I'll re-ask it.

8 Under the condition that PWM latch outputs a 0,
9 the downstream components, such as the zero-crossing
10 comparator, could output a 1, and that -- then it would
11 not become, as you say, transparent; isn't that correct?

12 A That would be correct. Yes.

13 Q And then, also, I believe you -- when you --

14 A You're talking about OR Gate 136?

15 Q Oh, I'll re-ask because I actually was not
16 talking about OR Gate 136, but maybe my -- oh, yes. Let
17 me -- let me -- let me start over.

18 OR Gate -- OR Gate 136 receives zero-crossing
19 comparators input and -- when that is a 1, there is a
20 condition where that would be a 1 and PWM latch would be a
21 0; right?

22 A I'm not sure, and I'm not trying to be evasive
23 here, but you're confusing me.

24 If the output of the zero-crossing comparator is
25 a 1 and that inputs to OR Gate 136, that 1 determines the

1 **output of 136.**

2 Q Yeah. I'll start over because I think I have too
3 many variables in my head, and it's too early in the
4 morning.

5 I'll just -- so you testified that there's a
6 condition when 1 -- in this circuit of Figure 3, when 122,
7 which is the output of PWM latch is 0, there is a
8 condition when Zero-Crossing Comparator 64 would also
9 output a 1; right?

10 A Well, that's not the scenario that I illustrated.
11 As I said, I stated in the declaration, my assumption --
12 my premise was the zero-crossing comparator is not being
13 activated.

14 Q Okay.

15 A There's no zero-crossing detected, so that's the
16 premise for this analysis.

17 Q Okay. And when PWM Latch 122 is 0, the input to
18 Transistor 124 is also 0; and that would turn off
19 Switch 124; right?

20 A Correct.

21 Q And that would cause C-off to charge, thereby
22 outputting a 1 on 106; right?

23 A Eventually, yes. That's the case.

24 Q And why did you not trace out that case?

25 A Well, I just didn't. I mean, it's illustrated in

1 my timing diagram, so it's not like I'm hiding the ball.
2 I just showed the case where it's 0 before the
3 Comparator 106 trips.

4 Q Let me...

5 A And I'm not sure it would make a difference. I
6 mean, if you want to consider it to be a 1 -- the output
7 of 112 would be a 1 has no impact on Endgate 134. Both
8 the SR ZC latch inputs to 0, which means it would remain
9 in whatever state it was in. So I don't think it would
10 matter.

11 Q Okay. How would the zero-crossing comparator
12 being 1 affect the timing diagram that you display on
13 paragraph 34?

14 A I didn't consider that case. I'd have to go back
15 and analyze it under that situation.

16 Q Okay. If you could, turn to paragraph 35,
17 please.

18 A Okay.

19 Q And as I understand from paragraph 35 through 38,
20 you criticize Mr. McAlexander's logic table; is that
21 correct?

22 A Well, I'll -- I'll say it -- rather than say
23 "criticize," I observed that there appeared to be some
24 inconsistencies or incompleteness or, perhaps, errors. My
25 exact words were -- what did I say -- "the table provides

1 incomplete picture of the logic values, the signals that
2 he analyzes"; and then later on I say -- I don't know for
3 one of the -- like, growth in paragraph 37, Row 5 -- this
4 row is incorrect, so...

5 Q Okay. For -- excluding Row 5, is it fair to say
6 that your criticisms or commentary on paragraphs 35, 36,
7 and 38 are more towards incompleteness, as opposed to
8 inaccuracy?

9 A Well, I don't recall -- regard to paragraph 35, I
10 do not recall. I don't -- I don't think that
11 Mr. McAlexander gave -- I'm just -- I don't have it in
12 front of me, and I certainly don't have a printed copy,
13 but I don't know what conditions he set up a priori for
14 his table, but mine is with -- when there's no
15 zero-crossing detection, and that is important for this
16 particular row and the red -- and the red signal.

17 Q Okay. And might your answers change if you
18 consider a zero crossing?

19 A Well, yes. In fact, when there is a zero
20 crossing, the -- that's the state -- let me just use the
21 signal colors now that we're talking about this diagram,
22 and we've got all these nice signal colors to help us
23 identify what we're talking about. When the orange signal
24 is low, the high-side driver's off; the low-side driver is
25 on; and that is the situation where you might be

1 interested in a zero-crossing detection.

2 So the orange signal -- in that case the orange
3 signal will be low. The brown signal would be high,
4 because it's driving the low-side transistor; and if a
5 zero-crossing detection event occurs, the output of the ZC
6 detector comparator will go to a 1. That will drive the
7 output of 136 to a 1. I believe at that same time, yellow
8 is already a 1, so you have 1, 1 at the input of 134 that
9 reset the brown signal to 0; and under that situation
10 you've got both orange and brown that are 0, which
11 presents -- that's an inverting input Endgate, which
12 causes the red signal to go 1. So, yes, the zero
13 crossing -- that's when the red signal is important. In
14 fact, it was during a zero-crossing detection.

15 Q Okay. So paragraph 35, the red signal would be a
16 1 when there is an orange signal of 0 and a zero-crossing
17 event; right?

18 A Yes. But note that paragraph 35 that I wrote
19 was -- was under the assumption that there's no
20 zero-crossing detection, just to be clear.

21 Q Yeah. If you could, look at paragraph 36 where
22 you provide commentary on Row 3.

23 A Okay.

24 Q It's a longer paragraph, so you could take a
25 second to reacquaint yourself; and, also, if you -- if you

1 need or want a quick break, please let me know. I don't
2 think we'll take beyond the second hour.

3 A Yeah. No. I'm fine. All right. Ask the
4 question. I'll review it in the context of processing the
5 question.

6 Q Okay. So your criticism of Row 3 -- and as you
7 describe in paragraph 36, is that it only reflects the
8 trailing state; is that right?

9 A Yes.

10 Q In the trailing state, it does reflect a
11 condition where that -- where Row 3 would be correct,
12 though; right?

13 A Let me -- let me consider that.

14 Yeah. The 1 -- the leading portion is when green
15 is high and -- and the 0 is during the trailing portion,
16 and so he's in -- in his Row 3 of his truth table, he's
17 considering only the trailing portion. Yes.

18 Q Okay. If we could turn to paragraph 37 -- in
19 paragraph 37, you state that orange and brown cannot be 1
20 at the same time, so Row 5, you consider to be incorrect.
21 Is that fair?

22 A Yes.

23 Q When the orange signal is 0, the -- and for
24 reference, you could look at your timing diagram on
25 page 18. When the orange signal is 0, the brown signal

1 will be 1; is that correct?

2 A Correct.

3 Q When the orange signal goes to 1, how does the
4 brown signal transition to 0?

5 A Well, the -- all right. So there's a little
6 nuance here. Maybe you're trying to find -- find a
7 wedge -- place to drive a wedge. I don't know.

8 But this cross-control circuit is there to deal
9 with the situation where during -- as a result of a
10 circuit propagation delays that the -- the orange and
11 brown signal could be at the same value. I didn't
12 investigate this, but I can imagine it's possible.
13 Momentarily, based upon the propagation delays of the
14 circuits -- but, logically, you know, as you present in a
15 table, you would never capture that transient state.

16 That being said, when the orange -- I think you
17 asked this. So when the orange goes to a 1, the 1
18 presents itself as a 1 to the input of OR Gate 136, which
19 outputs a 1. That 1 also presents itself to the OR Gate
20 112, which outputs a 1. Those two 1s, the output of 136
21 and the output of 112 -- then it goes to an Endgate
22 driving the output of 134 to a 1, which is the reset input
23 to the ZC latch. At the same time, the 1 that's output to
24 112 presents a 1 to the input of Inverter 142, generating
25 an output of 0 into the set.

1 So you have the proper conditions for -- at the
2 input of SNR of the ZC latch to reset it, which drives the
3 Q output of the ZC latch, which is the brown signal to a
4 0. That's how it happens.

5 Q When the orange signal is 0 -- and then the brown
6 signal will be a 1, and then the orange signal -- when it
7 transitions to 1, there will be a propagation delay
8 between 112, 1 in the inputs to the ZC latch and the
9 ZC latch before the brown signal is changed to 0; right?

10 A That's correct. But you're not going to
11 represent that in a truth table. That's a transient.

12 Q Okay. And would you reconsider paragraph 38
13 if -- rather, let me start over.

14 Would you reconsider paragraph 37 and your
15 criticism of Row 5 had you considered the zero-crossing
16 comparator 64?

17 A Let me -- let me look and see. Let's see. We're
18 talking about Row 5; right? So orange and brown.

19 Q Yes, yes, yes.

20 A Well, let me ask you. What -- what are you -- I
21 need some clarification on your question. Are you asking
22 me would Row 5 be correct if the zero-crossing comparator
23 output were 1? Is that what you're asking me?

24 Q Yes. Is there a condition where it would be
25 correct if you considered zero-crossing comparator to be

1 1? Or, rather, I think you already answered that, but --

2 A So -- yeah. So the orange signal is a 1.

3 Therefore, that determines the output of one -- of

4 OR Gate 136, so it doesn't matter where the zero-crossing

5 comparator outputs a 1 or a 0. It's -- it's -- 136 output

6 is determined by control signal at 122, so...

7 Q Okay.

8 A It wouldn't make a difference, I don't think.

9 Q Okay. So just to conclude on paragraph 37,
10 orange and brown can be 1; but that's only under a
11 transient condition; and it's your opinion that you -- one
12 would not and should not include that in a truth table.

13 Therefore, Row 5 is incorrect. Is that a fair summation?

14 A Yes. That is a fair summation.

15 Q Is there anything to that you would like to
16 supplement or otherwise address?

17 A I'll just restate the -- the situation that
18 you're alluding to where there's -- when I think what
19 would happen -- let me -- let me figure out which -- which
20 case it happens, so -- if the orange signal goes to a 1
21 from a state of 0 and the brown signal were high from the
22 previous state, then there's going to be a -- the
23 propagation delay through -- 1 through OR Gate 112,
24 Endgate 134, and the ZC latch. That would probably be the
25 dominant path, although, possibly, it could be 136 and

1 134, but I think -- my guess would be -- it'd be 112, 134,
2 and the ZC latch that would drive, then, brown to 0. So
3 during that propagation delay through those three gates,
4 there would be some transient overlap.

5 Q And then we could turn to paragraph 38, please.

6 A Okay.

7 Q And as I understand your criticism of 38, it
8 doesn't -- it's that Row 6 didn't also consider Aqua to be
9 0; right? Or, rather, let me re-ask. That was kind of
10 confusing.

11 Paragraph 38, I can -- I understand your
12 criticism to be that Aqua can be 1 and at other times 0;
13 and Row 6 only considers the situation where Aqua is 1.
14 Is that a fair assessment?

15 A Let me say it another way. With my word, when
16 orange is 1, Transistor 124 is on driving the noninverting
17 input Comparator 106 to 0, which results in the Aqua
18 signal being a 0. So in order for the Aqua signal to be a
19 1, orange must first go to 0; and then sometime later, via
20 the charging of Current Source 102 into Capacitors 100,
21 the noninverting input of 106 rises, causing the
22 comparator to trip, driving the Aqua signal to a 1; but
23 that can't happen when the orange signal is a 1.

24 MR. BOMBACH: Okay. Why don't we go off the
25 record for a minute or two, and y'all could take a break,

1 and I just want to check my notes. I think I'm about
2 wrapped up.

3 (Recess.)

4 MR. BOMBACH: All right. Yeah. I have no
5 further questions.

6 Dr. Holberg, thank you very much for your time.

7 **THE WITNESS: Okay.**

8 MR. BOMBACH: And I pass the witness to Mr. Gray.

9 MR. GRAY: We have no questions.

10 (Reporter inquires for copy orders.)

11 MR. GRAY: Yes, ma'am, please. Just normal
12 turnaround.

13 MR. BOMBACH: Yeah. I would like a rush copy,
14 please. I think -- well, I think our deadline is the
15 25th, so if we could have it ASAP, please.

16 (Whereupon, the proceeding was
17 concluded at 10:23 a.m.)

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1 REPORTER'S CERTIFICATE

2 I, Jane Gallegos, CSR No. 14676, do hereby certify
3 that the foregoing deposition of Dr. Douglas Holberg,
4 was taken on August 18, 2025 via zoom videoconference before
5 me at 9:08 a.m. for the purpose in the caption stated; that
6 the Witness was first duly sworn to tell the truth, the
7 whole truth, and nothing but the truth; that the deposition
8 was taken before me stenographically and afterwards
9 transcribed under my direction; that the foregoing is a
10 full, true, and correct transcript of the said deposition
11 so given; that counsel for all parties were present at
12 the time of the deposition; that there was not a request
13 that the witness read and sign the transcript.

14 I further certify that i am neither of counsel nor
15 of kin to any of the parties to this action, and am in
16 no way interested in the outcome of said action.

17

18 Witness My Signature on August 19, 2025.

19

20

21

22

23

24

25



Jane Gallegos, CSR No. 14676

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