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**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

**EXPERT REPORT OF JOSEPH C. McALEXANDER III
REGARDING INFRINGEMENT OF U.S. PATENT NUMBERS
9,041,377 AND 9,590,608**

**MONOLITHIC POWER SYSTEMS, INC., a
Delaware corporation,**

v.

**REED SEMICONDUCTOR CORP., a
Delaware corporation,**

v.

**NENGDA MICROELECTRONICS (SHENZHEN) CO., LTD., a Chinese
Corporation; and NENGDA SEMICONDUCTOR TECHNOLOGY
(SHENZHEN) CO., LTD., a Chinese Corporation**

C.A. No.: 1:23-cv-01155-JFM; 1:24-cv-00165-JFM; 1:24-cv-00166-JFM

August 1, 2025

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

Defendants.

C.A. No.: 1:24-cv-00166-JFM

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201. In my opinion, the RS53319 (and all of the Accused Products) infringe the preamble.

202. The step-down regulator comprises each of the following claimed limitations, described below.

203. Thus, the Reed Accused Products practice Element 18

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[pre]
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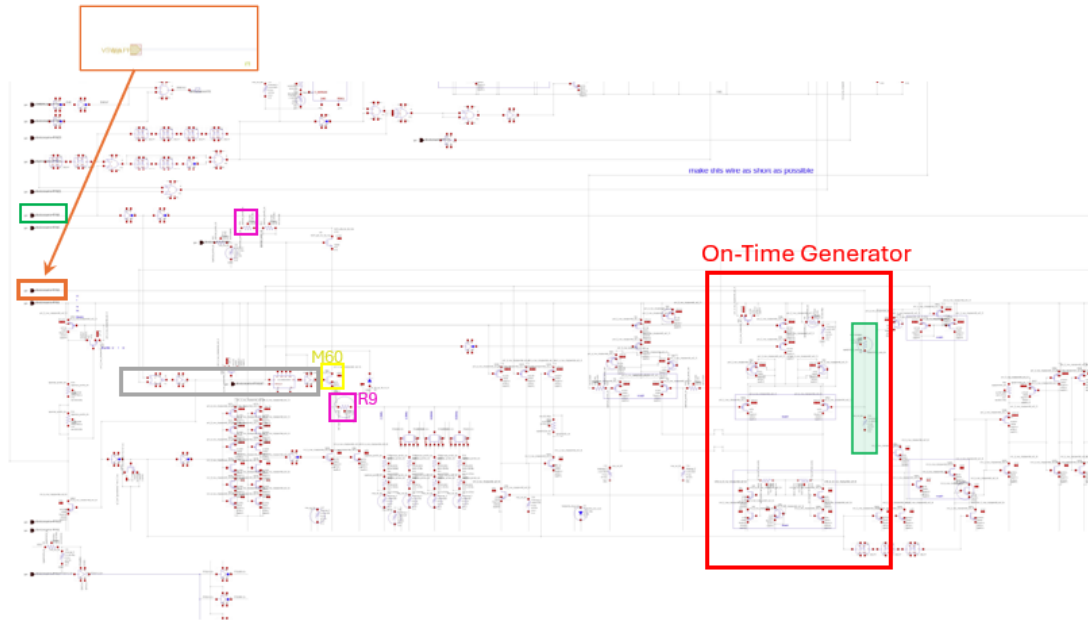
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8.3.4.1.2 Element 18[a]: “an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;”

204. The RS53319, as seen in the below schematics (REED1155_0007933 and REED0165_0000001), comprises an on-time generator (Red) configured to receive a switching signal VSW_LPF (orange) provided by the step-down regulator, and to receive a control signal—which includes at least the signal PWMHS (PWM) (green) found within LOOPTONGEN at REED1155_0007933 described below—wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal. The on-time generator includes a low pass filter (Green) and a TON (on-time) generator. The on-time generator generates an on-time signal COMPRAW, which is further output at LOOPTON/LOOPTON1 (Blue) and fed into the TON_Shot pin (Purple). The resistors for the TON generator are in pink. The resistor (R9) act as a principle input into the on-time generator based upon the output of the NOR gate within the gray box. The LOOPTON1 pin output has a corresponding output from the same latch feeding into the

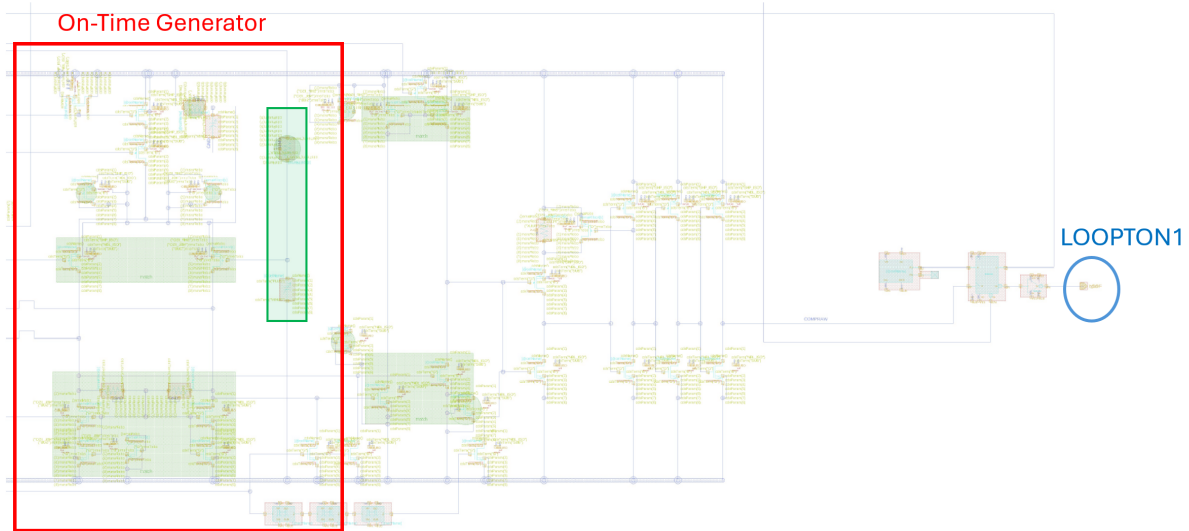
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NOR gate with a second input from PWM. The inputs to the NOR gate control the output from the NOR gate that drives the output transistor (M60) (yellow) that feeds the resistor (R9).¹³²



¹³² RS53319 at REED1155_0007933 and REED0165_0000001.

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205. Other accused products are substantially similar.¹³³

206. The schematic below is from RS53319's PWMSYNC schematic.¹³⁴

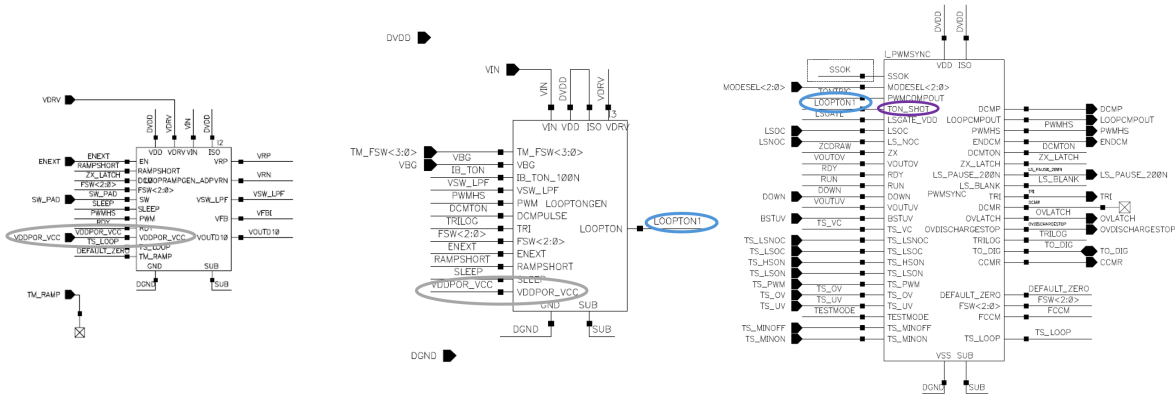
¹³³ See also REED1155_0007938 (RS53317's LOOPTONGEN_317 schematic); REED1155_0007933 (RS53318's LOOPTONGEN schematic); REED0165_0000001 (RS53318's LOOPTONGEN schematic); REED1155_0007933 (RS53328's LOOPTONGEN schematic); REED0165_0000001 (RS53328's LOOPTONGEN schematic); REED1155_0007933 (RS53355's LOOPTONGEN schematic); REED0165_0000001 (RS53355's LOOPTONGEN schematic); REED1155_0577882 (RS53417's LOOPTONGEN_417_B0 schematic); REED1155_0578114 (RS53419's LOOPTONGEN_B0 schematic); REED1155_0578352 (RS53428's LOOPTONGEN_B0 schematic); REED1155_0577164 (RS53385's LOOPTONGEN_385 schematic).

¹³⁴ REED1155_0008065; See also Fan Dep. Tr. at 171:24-172:4 (stating that the PWMSYNC provides logic related functionality).

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208. In addition, the output of the on-time signal at LOOPTON1 (Blue) is an input into the TON_Shot pin (Purple). The circuitry which responds to the TON_Shot input controls the generation of the PWMHS/PWMHSB signal that feeds the low side/high side blocks.¹³⁶



209. Other accused products are substantially similar.¹³⁷

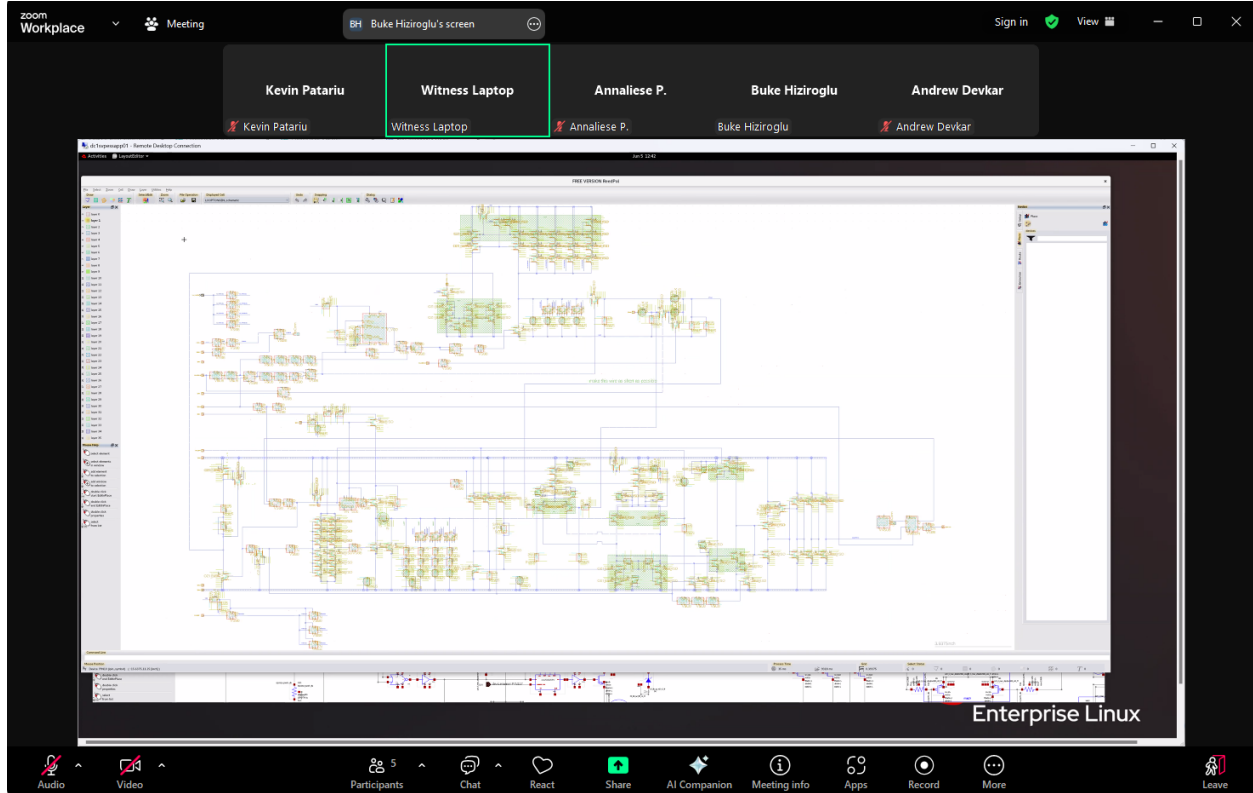
210. Jiwei Fan, Reed's 30(b)(6) witness testified that the above-identified LOOPTONGEN is present in REED1155_0007933 at his deposition.¹³⁸

¹³⁶ From RS53319's CTRLCORE ADP schematic at REED1155_0007776 (RS53319's CTRLCORE_ADAP's schematic); see also Fan Dep Tr. at 17:17-23 (stating that CTRLCORE_ADAP provides basic control function).

¹³⁷ See REED1155_0002176 at -2179 and REED1155_0007770 (RS53317's CTRLCORE_317 schematic); REED1155_0002184 at -2187 and REED1155_0007762 (RS53318's CTRLCORE schematic); REED1155_0002200 at 2203 (RS53328's CTRLCORE_ADAP_LQ schematic); REED1155_0002208 at 2211 and REED1155_0007776 (RS53355's CTRLCORE ADP schematic); REED1155_0577827 ("RS53417's CTRLCORE_417_LQ_B0 schematic); REED1155_0578058 (RS53419's CTRLCORE_ADAP_B0 schematic); REED1155_0578296 (RS53428's CTRLCORE_ADAP_LQ_B0 schematic); REED1155_0576742 (RS53385's CTRLCORE_ADAP schematic).

¹³⁸ Jiwei Fan Dep. Tr. at 147:16-148:18 (describing the above, and screen cap labeled as Exhibit 500 (excerpted below)).

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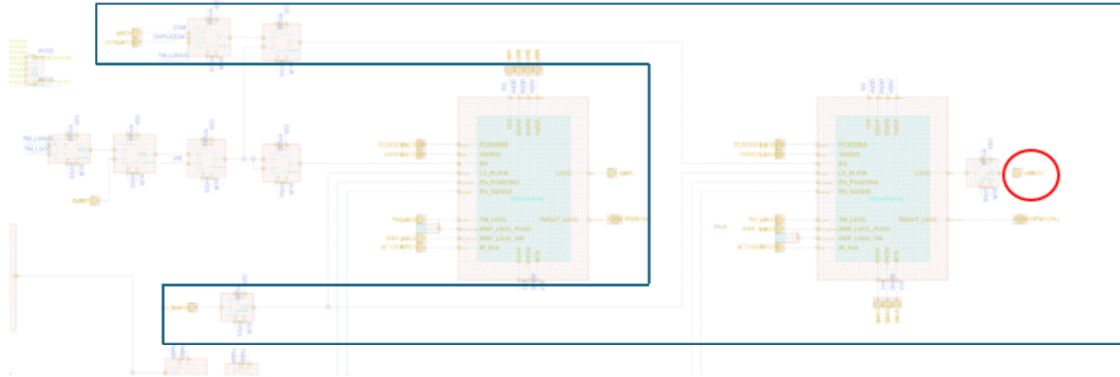
211. Thus, the Reed Accused Products practice Element 18[a].

8.3.4.1.3 Element 18[b]: “a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;”

212. The RS53319 has a minimum off time generator (blue box annotated in schematic below) configured to receive the control signal, and to generate a minimum off time signal (LSOC in Red) in accordance with the control signal.¹³⁹

¹³⁹ LSOC_NOC_15V at REED1155_0007977 and PWMSYNC at REED1155_0002192 at -2198. *See also* Jiwei Fan Dep. Tr. at 16:16-20 (stating that LSOC_NOC_15V provides overcurrent protection).

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213. Other accused products are substantially similar.¹⁴⁰

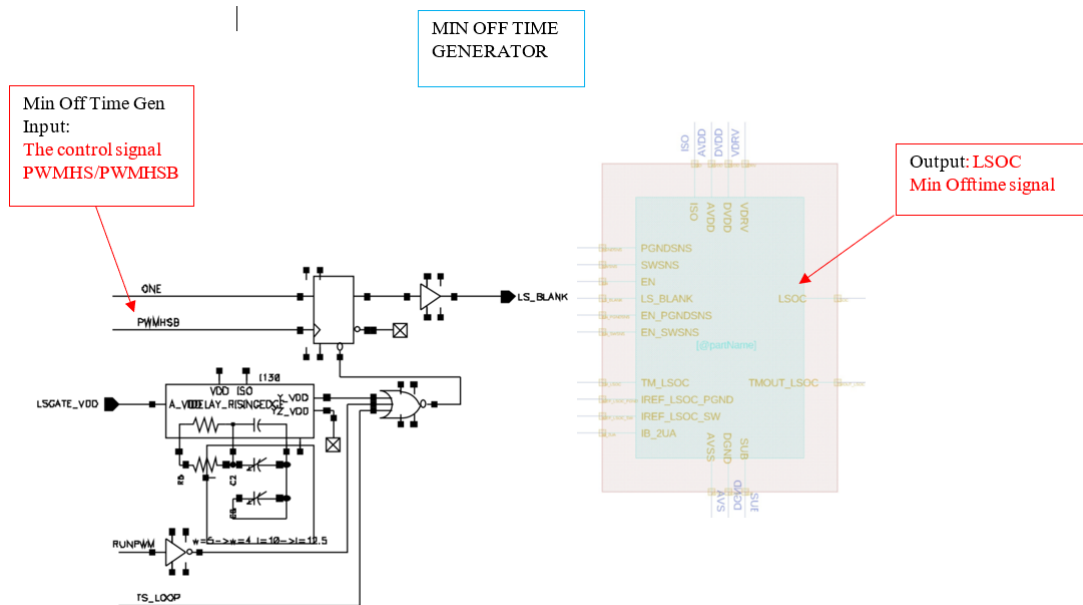
214. The control signal input to the minimum off time generator is highlighted below.

The claimed control signal controls the LS_BLANK input to the LSOC_NOC_15V schematic.¹⁴¹

¹⁴⁰ See REED1155_0007977 (RS53317's LSOC_NOC_15V schematic); REED1155_0007970 (RS53318's LSOC_NOC schematic); REED1155_0007977 (RS53328's LSOC_NOC_15V schematic); REED1155_0007977 (RS53355's LSOC_NOC_15V schematic); REED1155_0577906 (RS53417's LSOC_NOC_417 schematic); REED1155_0578134 (RS53419's LSOC_NOC_419 schematic); REED1155_0578377 (RS53428's LSOC_NOC_428 schematic); REED1155_0577203 (RS53385's schematic).

¹⁴¹ (Left) From RS53319's PWMSYNC schematic at REED1155_0008065 (RS53319's PWMSYNC schematic); (Right) From RS53319's LSOC_NOC_15V schematic at REED1155_0007977.

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215. Other accused products are substantially similar.¹⁴²

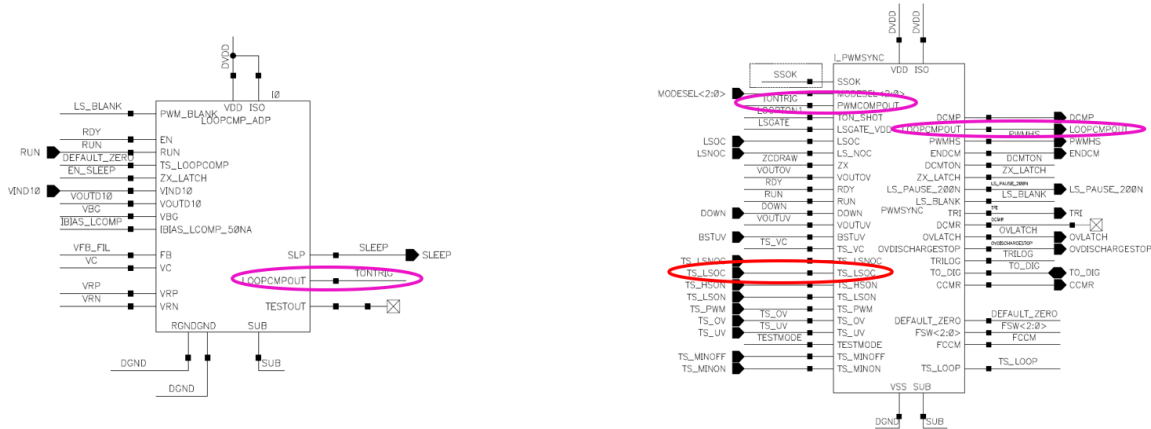
216. As shown in the schematic below, LSOC (red) inputs into logic circuitry which generates the output PWMHS/PWMHSB (blue).¹⁴³

¹⁴² (Left) See REED1155_0002176 at -2182 and REED1155_0008070 (RS53317's PWMSYNC_317 schematic); REED1155_0002184 at -2190 and REED1155_0008065 (RS53318's PWMSYNC schematic); REED1155_0002200 at 2206 and REED1155_0008065 (RS53328's PWMSYNC schematic); REED1155_0002208 at 2214 and REED1155_0008065 (RS53355's PWMSYNC schematic); REED1155_0577943 (RS53417's PWMSYNC_417_B0 schematic); REED1155_0578175 (RS53419's PWMSYNC_B0 schematic); REED1155_0578409 (RS53428's PWMSYNC_B0 schematic); REED1155_0577351 (RS53385's PWMSYNC_385 schematic).

(Right) See REED1155_0007977 (RS53317's LSOC_NOC_15V schematic); REED1155_0007970 (RS53318's LSOC_NOC schematic); REED1155_0007977 (RS53328's LSOC_NOC_15V schematic); REED1155_0007977 (RS53355's LSOC_NOC_15V schematic); REED1155_0577906 (RS53417's LSOC_NOC_417 schematic); REED1155_0578134 (RS53419's LSOC_NOC_419 schematic); REED1155_0578377 (RS53428's LSOC_NOC_428 schematic); REED1155_0577203 (RS53385's schematic).

¹⁴³ From RS53319's PWMSYNC schematic at REED1155_0008065 (RS53319's PWMSYNC schematic).

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237. Other accused products are substantially similar.¹⁶¹

238. Thus, the Reed Accused Products practice Element 18[d].

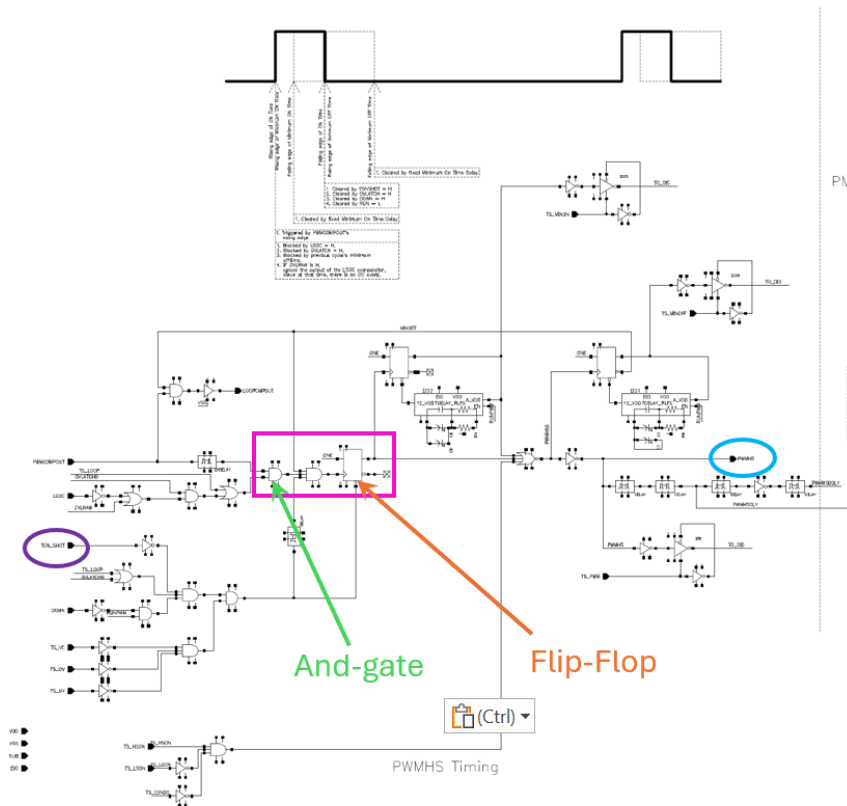
8.3.4.1.6 Element 18[e]: “a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and”

239. The RS53319 has a flip-flop, as annotated in the circuit schematic below, having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the

¹⁶¹ See REED1155_0002176 at -2179 and REED1155_0007770 (RS53317’s CTRLCORE_317 schematic); REED1155_0002184 at -2187 and REED1155_0007762 (RS53318’s CTRLCORE schematic); REED1155_0002200 at 2203 (RS53328’s CTRLCORE_ADP_LQ schematic); REED1155_0002208 at 2211 and REED1155_0007776 (RS53355’s CTRLCORE_ADP schematic); REED1155_0577827 (“RS53417’s CTRLCORE_417_LQ_B0 schematic); REED1155_0578058 (RS53419’s CTRLCORE_ADP_B0 schematic); REED1155_0578296 (RS53428’s CTRLCORE_ADP_LQ_B0 schematic); REED1155_0576742 (RS53385’s CTRLCORE_ADP schematic).

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on-time generator to receive the on-time signal (*e.g.*, TON_SHOT) (purple), and the set terminal is coupled to the and-gate (Green) to receive the AND output signal (collectively in pink), wherein based on the on-time signal and the AND output signal, the flip-flop generates the control signal (*e.g.*, PWMHS/PWMHSB).¹⁶²



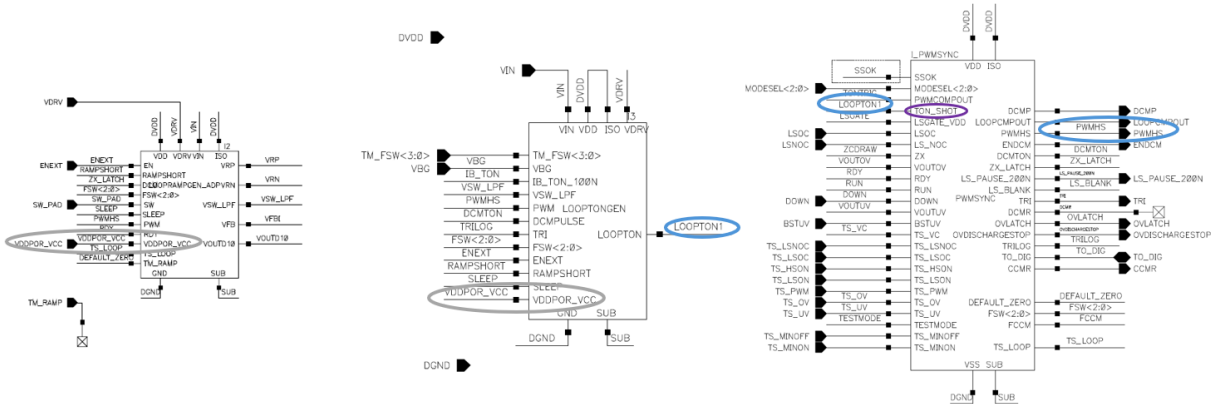
240. Other accused products are substantially similar.¹⁶³

¹⁶² From RS53319's PWMSYNC schematic at REED1155_0008065 (RS53319's PWMSYNC schematic).

¹⁶³ See REED1155_0002176 at -2182 and REED1155_0008070 (RS53317's PWMSYNC_317 schematic); REED1155_0002184 at -2190 and REED1155_0008065 (RS53318's PWMSYNC schematic); REED1155_0002200

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241. As shown below, the output of the on-time signal at LOOPTON1 (Blue) is fed into the TON_Shot pin (Purple).¹⁶⁴



242. Other accused products are substantially similar.¹⁶⁵

243. Thus, the Reed Accused Products practice Element 18[e].

8.3.4.1.7 Element 18[f]: “a power stage coupled to the output terminal of the flip-flop to receive the control signal,

at 2206 and REED1155_0008065 (RS53328’s PWMSYNC schematic); REED1155_0002208 at 2214 and REED1155_0008065 (RS53355’s PWMSYNC schematic); REED1155_0577943 (RS53417’s PWMSYNC_417_B0 schematic); REED1155_0578175 (RS53419’s PWMSYNC_B0 schematic); REED1155_0578409 (RS53428’s PWMSYNC_B0 schematic); REED1155_0577351 (RS53385’s PWMSYNC_385 schematic).

¹⁶⁴ From RS53319’s CTRLCORE ADP schematic at REED1155_0007776 (RS53319’s CTRLCORE_ADP’s schematic).

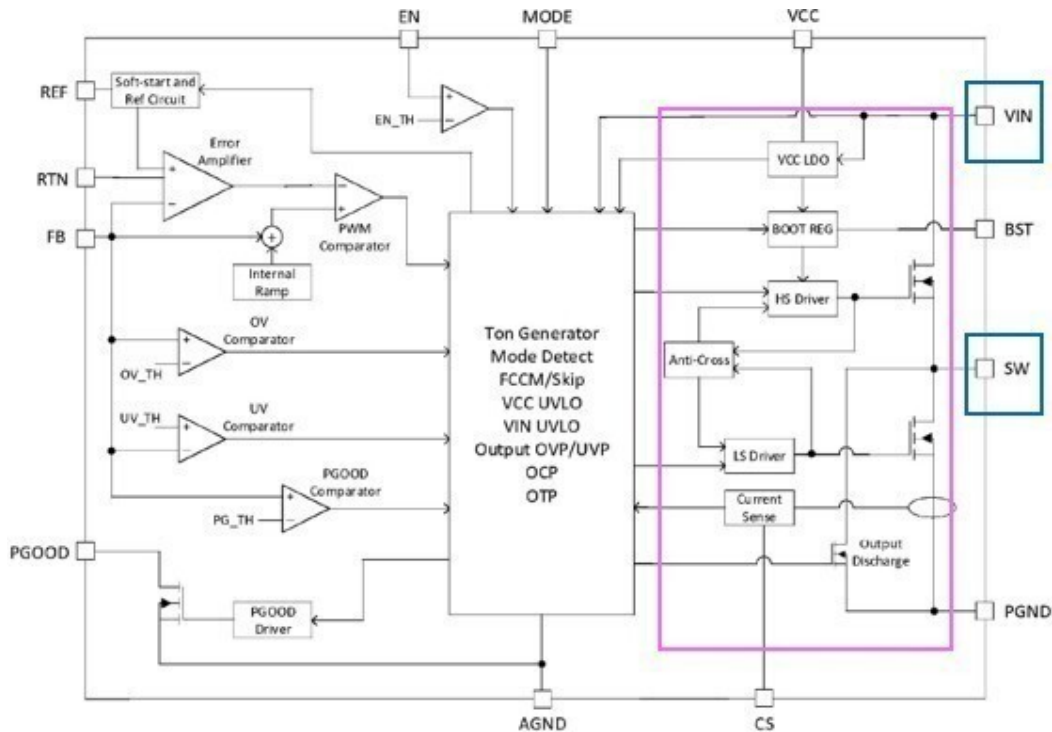
¹⁶⁵ See REED1155_0002176 at -2179 and REED1155_0007770 (RS53317’s CTRLCORE_317 schematic); REED1155_0002184 at -2187 and REED1155_0007762 (RS53318’s CTRLCORE schematic); REED1155_0002200 at 2203 (RS53328’s CTRLCORE_ADP_LQ schematic); REED1155_0002208 at 2211 and REED1155_0007776 (RS53355’s CTRLCORE_ADP schematic); REED1155_0577827 (“RS53417’s CTRLCORE_417_LQ_B0 schematic); REED1155_0578058 (RS53419’s CTRLCORE_ADP_B0 schematic); REED1155_0578296 (RS53428’s CTRLCORE_ADP_LQ_B0 schematic); REED1155_0576742 (RS53385’s CTRLCORE_ADP schematic).

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wherein based on the control signal, the power stage converts an input voltage into the switching signal.”

244. The RS53319 includes a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.

245. The power stage includes at least the devices within the pink box below.¹⁶⁶ The power stage converts the input voltage (VIN) into the switching signal (SW) based on the control signal, as annotated below.

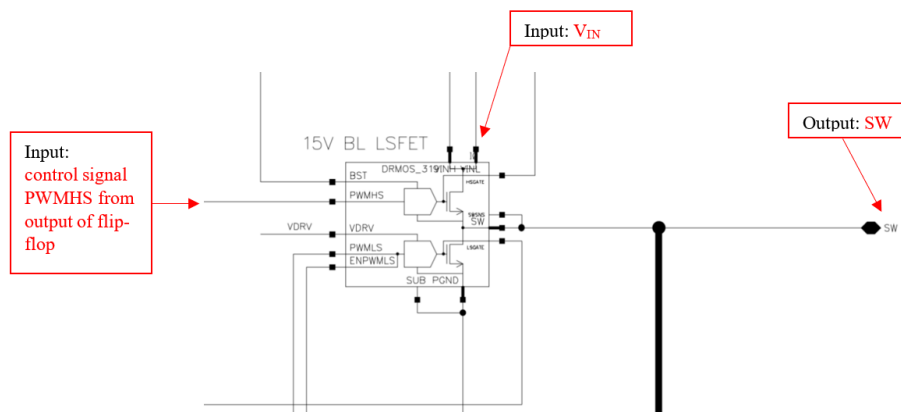
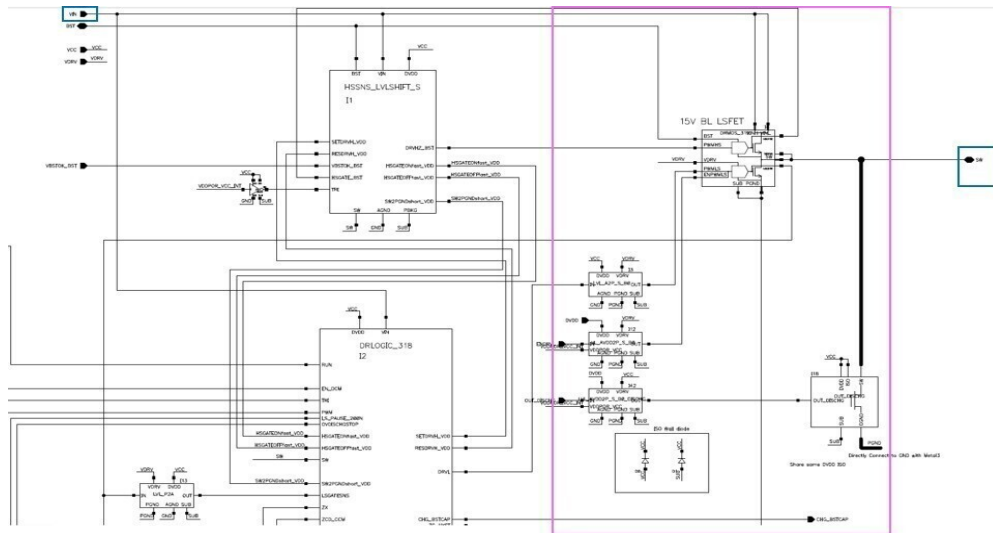


¹⁶⁶ From RS53319 Datasheet at REED1155_0000104.

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246. Other accused products are substantially similar.¹⁶⁷

247. The schematics below further verify the presence of the claimed power stage that converts the input voltage (VIN) into the switching signal (SW).¹⁶⁸



¹⁶⁷ See REED1155_0000053 (RS53317 datasheet); REED1155_0000077 (RS53318 datasheet); REED1155_0000130 (RS53328 datasheet); REED1155_0000152 (RS53355 datasheet); REED1155_0577784 (RS53417 datasheet); REED1155_0578014 (RS53419 datasheet); REED1155_0578251 (RS53428 datasheet); REED1155_0576671 (RS53385 datasheet).

¹⁶⁸ From RS53319's PWMDRMOS_319 schematic at REED1155_0008061 (RS53319's PWMDRMOS_319 schematic).

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248. Other accused products are substantially similar.¹⁶⁹ Thus, the Reed Accused Products practice Element 18[f].

249. In summary, each of the Reed Accused Products practices Claim 18 of the '377 Patent.

8.3.4.2 Reed Accused Products Infringe Asserted Apparatus Claim 18 of the '377 Patent Under the Doctrine of Equivalents

250. Provided below are items addressing certain doctrine of equivalents positions should Defendants argue that certain limitations are missing. They are nonetheless still met via the doctrine of equivalents because there are no substantial differences and each asserted claim element performs substantially the same function, in substantially the same way, to achieve substantially the same result.

8.3.4.2.1 “Control Signal” of 18(a), 18(b), 18(e), and 18(f)

251. To the extent that Defendants suggest that the Accused Products do not literally satisfy the control signal limitation (and its associated interconnects), then the Accused Products satisfy this element under the doctrine of equivalents.

¹⁶⁹ See REED1155_0002176 at -2177 (RS53317's PWMDRMOS schematic); REED1155_0008056 (RS53317's PWMDRMOS schematic); REED1155_0002184 at -2185 (RS53318's PWMDRMOS schematic); REED1155_0008056 (RS53318's PWMDRMOS schematic); REED1155_0002200 at 2201 (RS53328's PWMDRMOS schematic); REED1155_0008056 (RS53328's PWMDRMOS schematic); REED1155_0002208 at 2209 (RS53355's PWMDRMOS schematic); REED1155_0008056 (RS53355's PWMDRMOS schematic); REED1155_0577937 (RS53417's PWMDRMOS_417 schematic); REED1155_0578170 (RS53419's PWMDRMOS_419 schematic); REED1155_0578404 (RS53428's PWMDRMOS_428 schematic); REED1155_0577339 (RS53385's PWMDRMOS_385 schematic). See also Jiwei Fan Dep. Tr. at 171:4-8 (stating that PWMDRMOS_319 drives the control core and drives the power stage).

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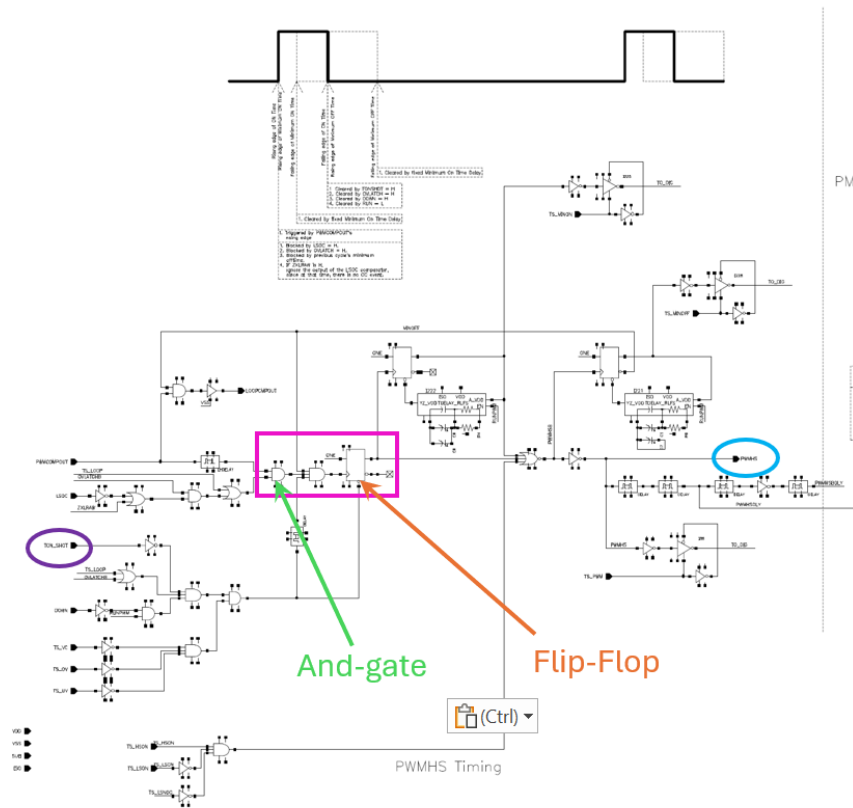
252. Claim 18(a), 18(b), 18(e), and 18(f) recite a control signal (blue) that is interconnected between several elements.

18. A step-down regulator, comprising:
an on-time generator configured to receive a switching signal provided by the step-down regulator, and to receive a control signal, wherein based on the switching signal and the control signal, the on-time generator generates an on-time signal;
a minimum off time generator configured to receive the control signal, and to generate a minimum off time signal in accordance with the control signal;
a comparator configured to receive a feedback signal representative of the output voltage of the step-down regulator, and to receive a reference signal, and wherein based on the feedback signal and the reference signal, the comparator generates a comparison signal;
an and-gate coupled to the comparator and the minimum off time generator to receive the comparison signal, and to receive the minimum off time signal, wherein based on the comparison signal and the minimum off time signal, the and-gate generates an output signal;
a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal; and
a power stage coupled to the output terminal of the flip-flop to receive the control signal, wherein based on the control signal, the power stage converts an input voltage into the switching signal.

253. As described previously in 18(e) and shown in the following schematic, the flip flop generates the control signal (*e.g.*, PWMHS/PWMHSB).¹⁷⁰

¹⁷⁰ From RS53319's PWMSYNC schematic at REED1155_0008065 (RS53319's PWMSYNC schematic).

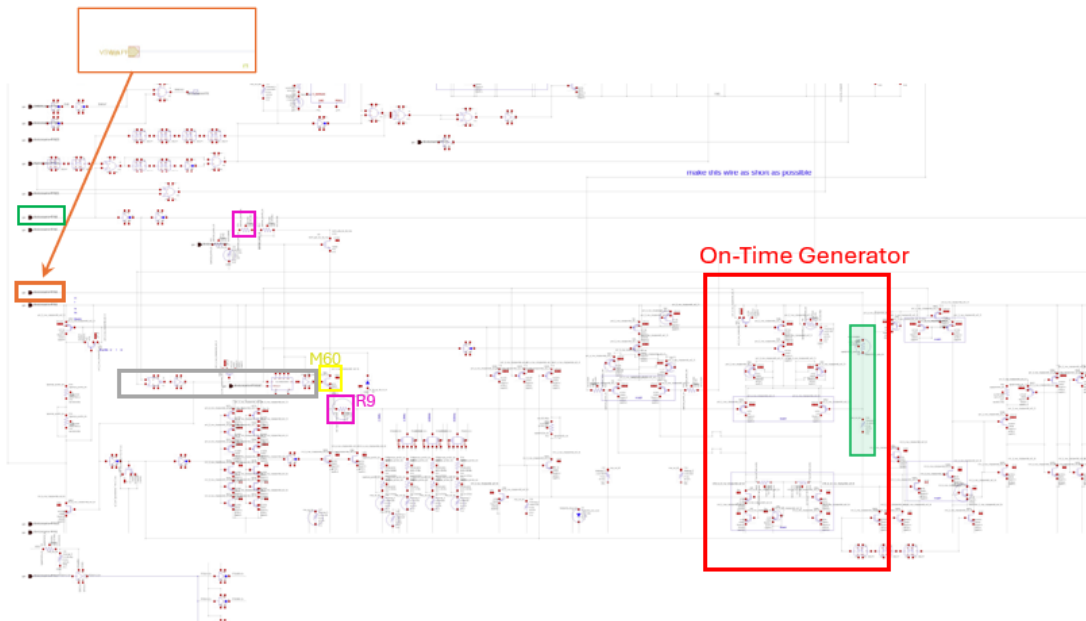
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254. As described in 18(a) and shown in the following schematic, PWMHS (green) found within LOOPTONGEN at REED1155_0007933 is used by the on-time generator to generate an on-time signal.¹⁷¹

¹⁷¹ RS53319 at REED1155_0007933 and REED0165_0000001.

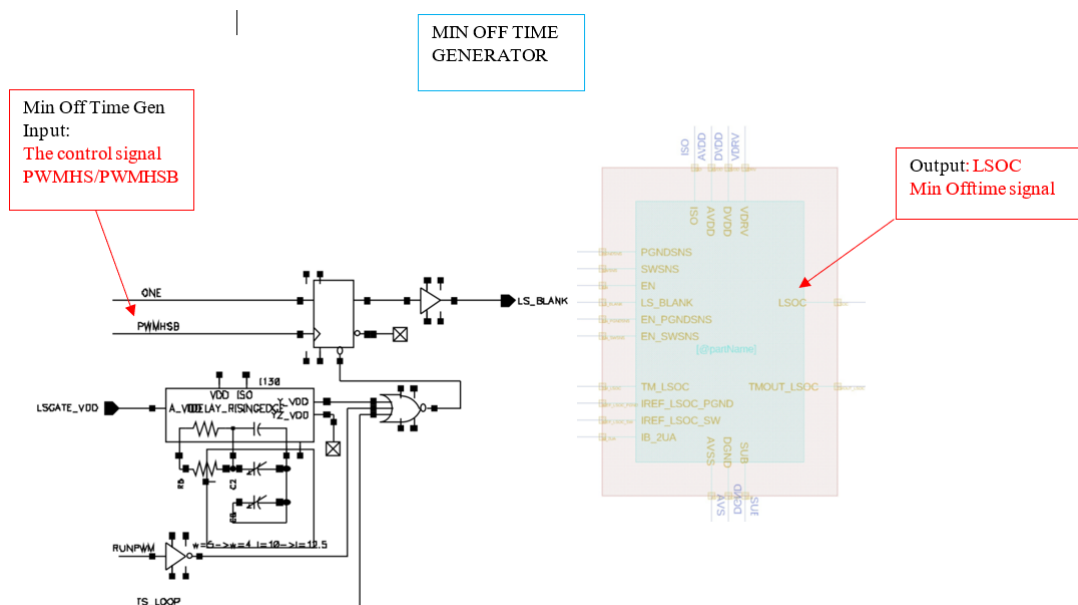
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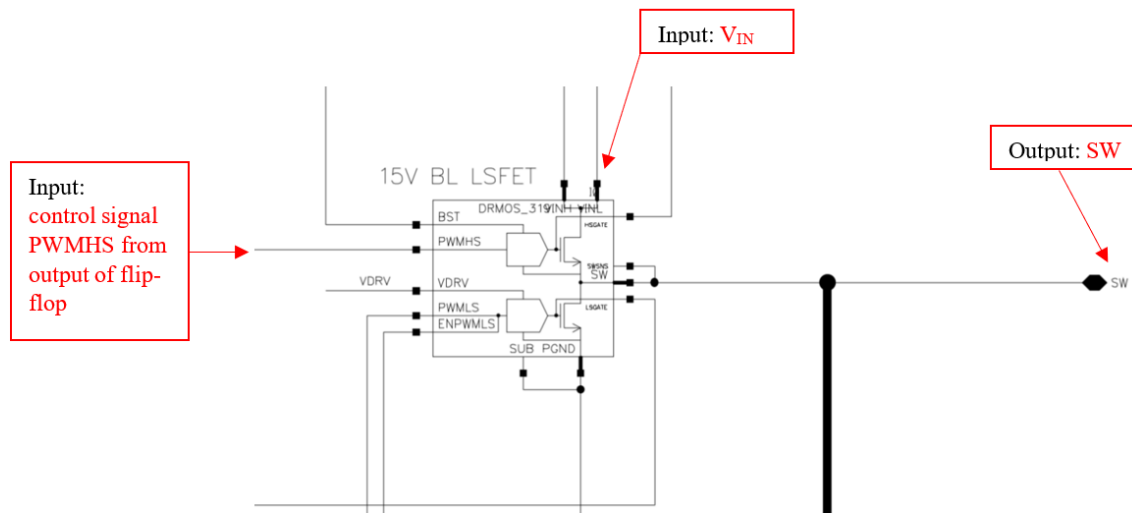
255. As described in 18(b), the PWMHS/PWMHSB is used by the min off time generator to generate a min off time signal.¹⁷²

¹⁷² (Left) From RS53319's PWMSYNC schematic at REED1155_0008065 (RS53319's PWMSYNC schematic); (Right) From RS53319's LSOC_NOC_15V schematic at REED1155_0007977.

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256. As shown in 18(f), the PWMHS signal is used to drive the power stage.¹⁷³



¹⁷³ From RS53319's PWMDRMOS_319 schematic at REED1155_0008061 (RS53319's PWMDRMOS_319 schematic).

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257. The differences, if any, between the accused Reed products and this claim element are insubstantial at most. One of ordinary skill in the art, to which the '377 Patent pertains, would understand that the corresponding elements are interchangeable or substitutable for the corresponding “control signal” element of this claim limitation; and this element of the Accused Products does not play a role which is substantially different.

258. Each of the Accused Products’ “control signal” provides substantially the same function, which is to provide control and logical connections to control the power stage (18(f)), on-time generator (18(a)), and minimum off-time generator (18(b)) in substantially the same way, which is to use control signals generated by the flip flop (18(e)) to drive and control the power stage (18(f)), on-time generator (18(a)), and minimum off-time generator (18(b)). This achieves substantially the same result, which is to effectuate control on those elements.

8.3.4.2.2 “flip flop” of 18(e)

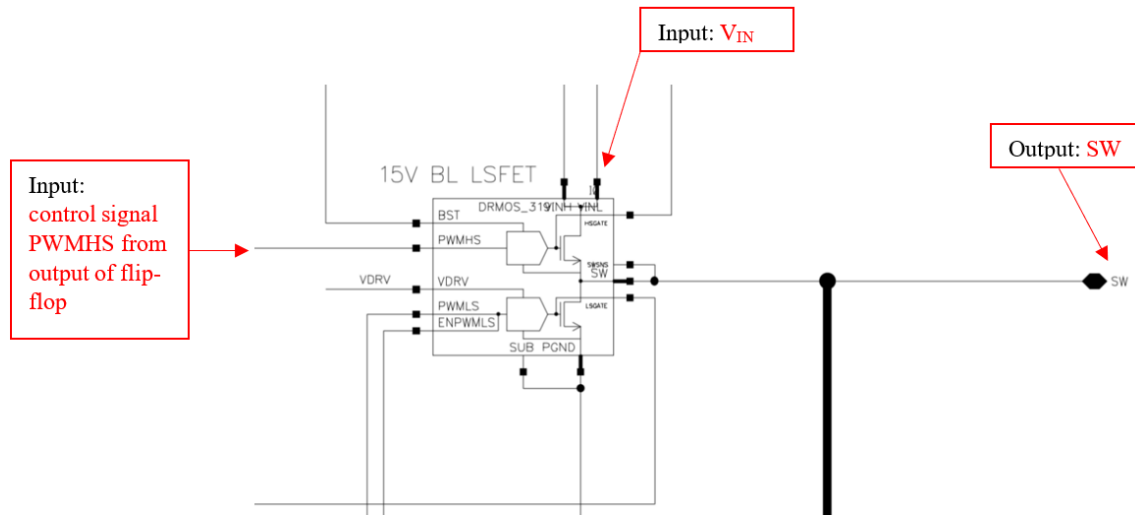
259. To the extent that Defendants suggest that the Accused Products do not literally satisfy the flip flop limitation (and its associated interconnects), then the Accused Products satisfy this element under the doctrine of equivalents. Claim 18(e) requires “a flip-flop having a set terminal, a reset terminal and an output terminal, wherein the reset terminal is coupled to the on-time generator to receive the on-time signal, and the set terminal is coupled to the and-gate to receive the output signal, wherein based on the on-time signal and the output signal, the flip-flop generates the control signal.”

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this claim limitation of claim 18, for the same reason.

284. As described in detail in 18(a) above, the on-time generator generates an on-time signal COMPRAW, which is further output at LOOPTON/LOOPTON1 (Blue) and fed into the TON_Shot pin (Purple). The circuitry which responds to the TON_Shot input controls the generation of the PWMHS/PWMHSB signal that feeds the low side/high side blocks.

285. And as shown in 18(f), the PWMHS signal is used to drive the power stage.¹⁸³ The “on time signal” is thusly practiced.



8.3.4.3.3 “a flip-flop having a set terminal, a reset terminal and an output terminal”

286. Defendants argued non-infringement based on this limitation. The whole of their interrogatory response is excerpted below:¹⁸⁴

¹⁸³ From RS53319’s PWMDRMOS_319 schematic at REED1155_0008061 (RS53319’s PWMDRMOS_319 schematic).

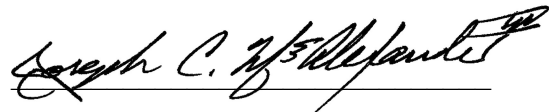
¹⁸⁴ Reed II Rog. 5 Resp. at pg. 13.

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10 CONCLUDING REMARKS

654. I understand that additional information may be forthcoming that may require me to amend or supplement my opinions. I will do so in a timely manner should a response to that additional information be warranted.

Dated: August 1, 2025


Joseph C. M^cAlexander III

Attachments:

- Attachment A – Findings of Product Infringement of 9,041,377 Patent Claims**
- Attachment B – Findings of Product Infringement of 9,590,608 Patent Claims**
- Attachment C – Documents Considered**
- Attachment D – Curriculum Vitae / Other Cases**
- Attachment E – Compensation**